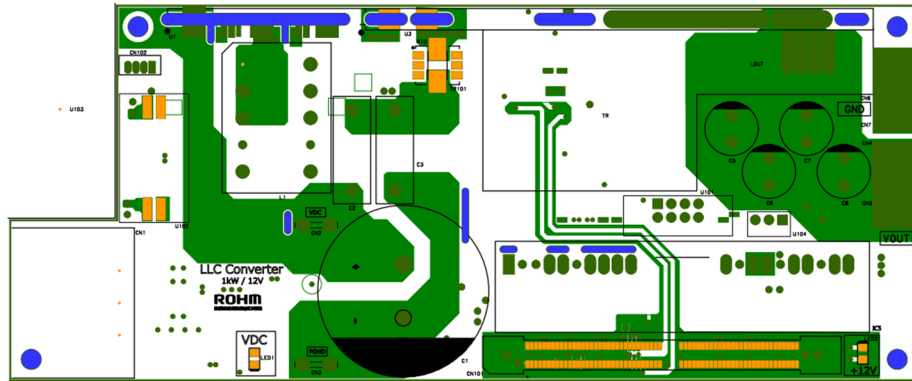


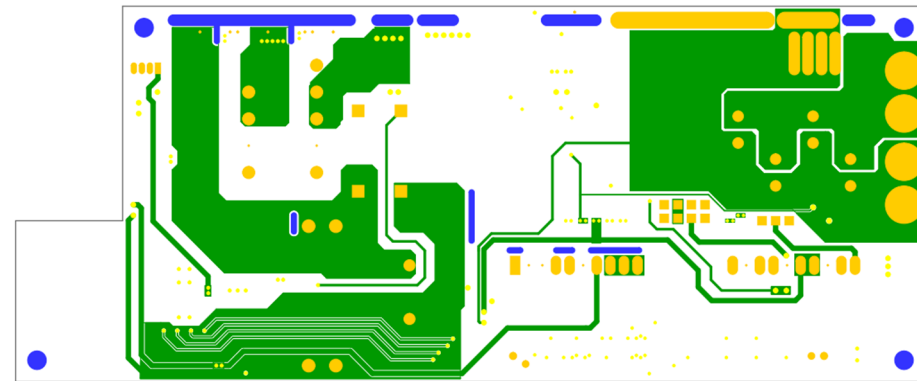
[HBLLC-TSB-001] Board layout

[Main Board]

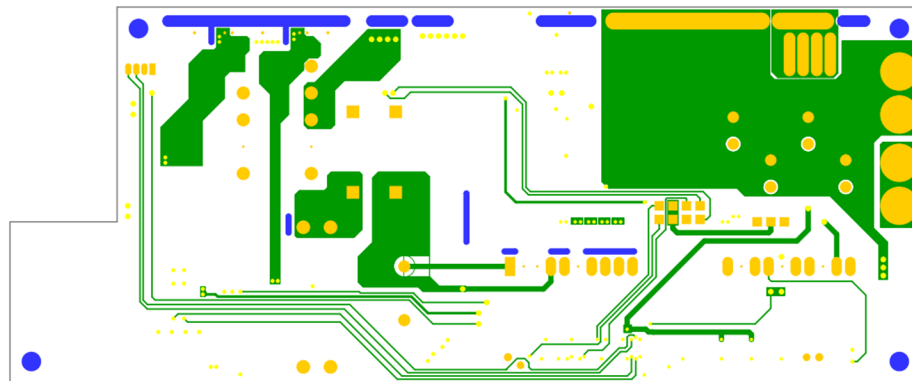
• Top layer



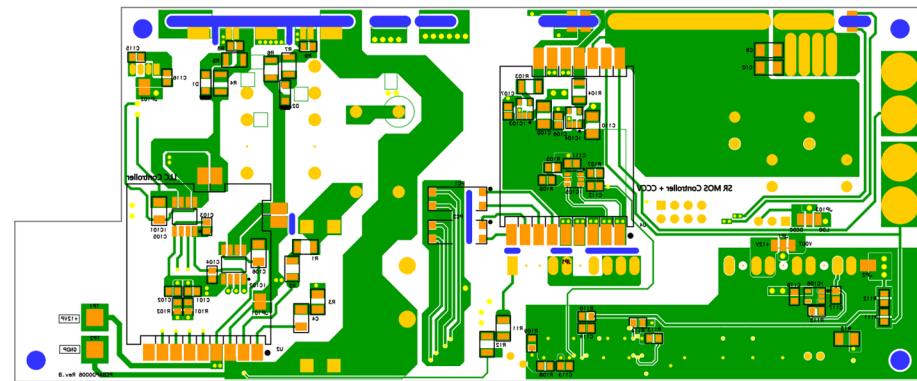
• 2nd layer



• 3rd layer



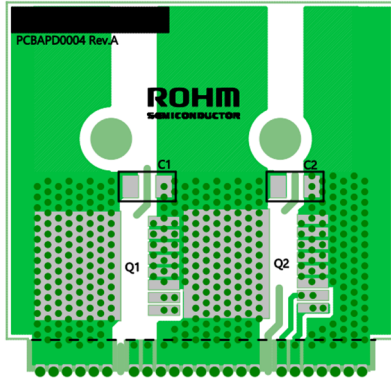
• Botom layer



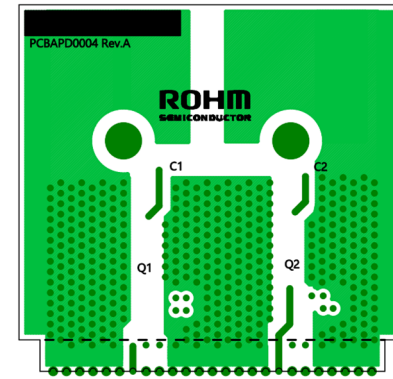
[HBLLC-TSB-001] Board layout

[LLCMOS Board]

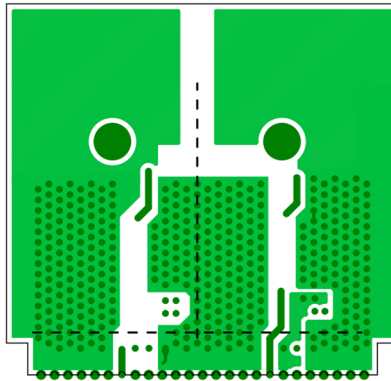
- Top layer



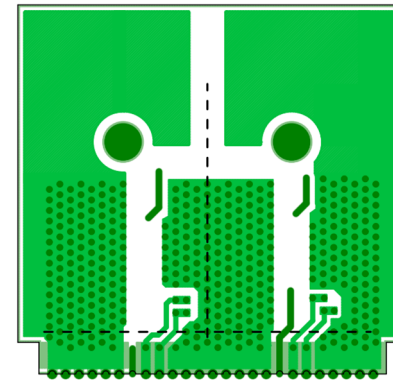
- 2nd layer



- 3rd layer



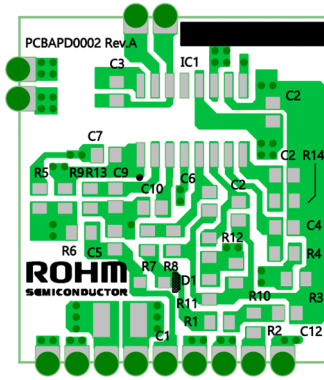
- Botom layer



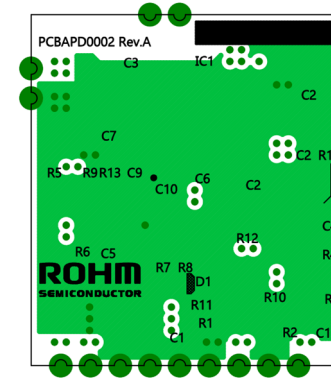
[HBLLC-TSB-001] Board layout

[LLCCONT Board]

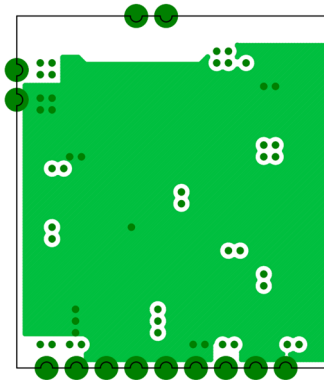
- Top layer



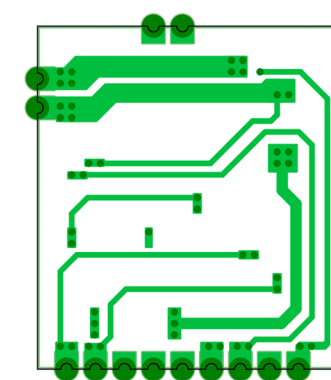
- 2nd layer



- 3rd layer



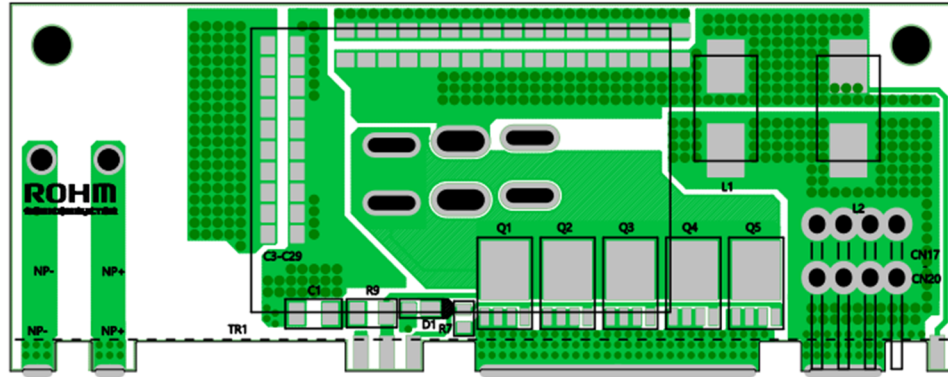
- Botom layer



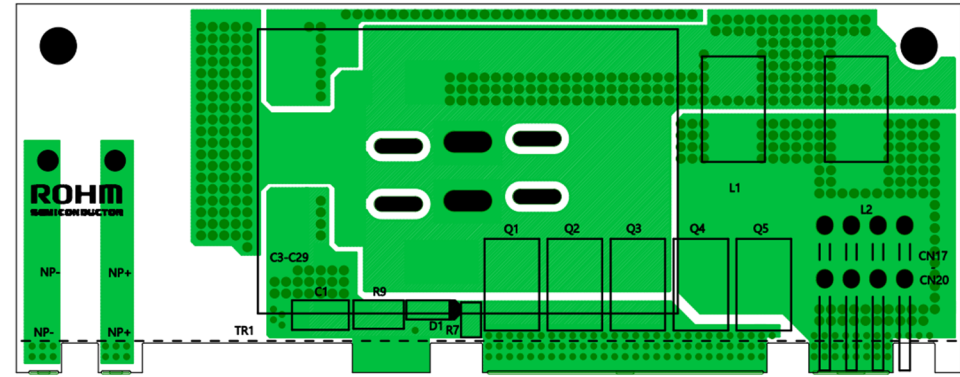
[HBLLC-TSB-001] Board layout

[SRMOS Board]

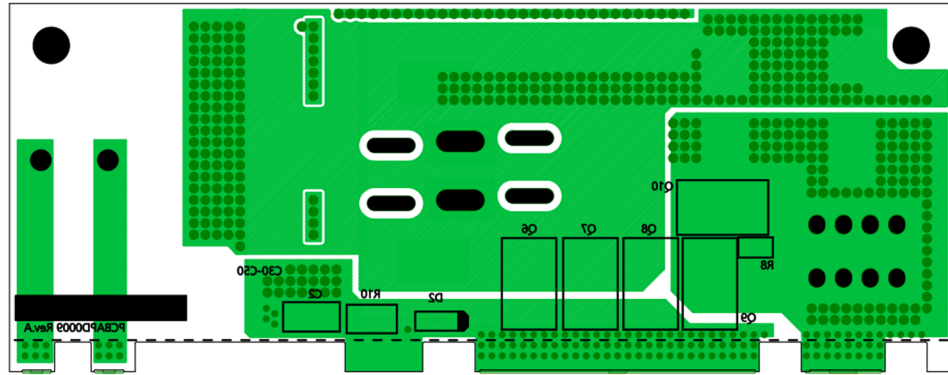
• Top layer



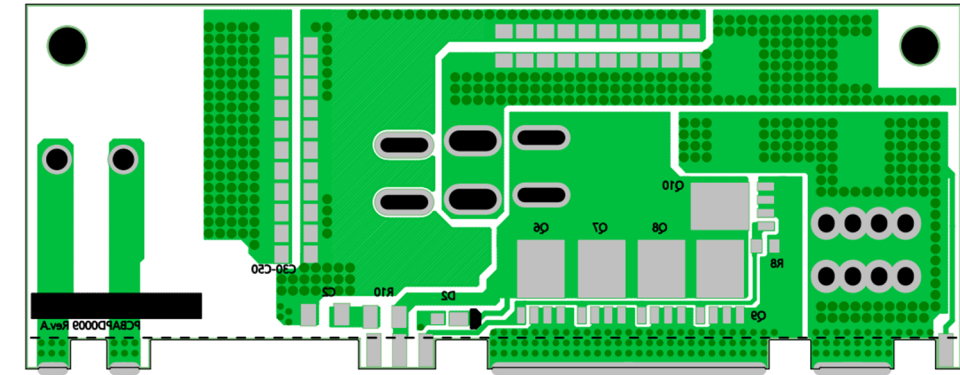
• 2nd layer



• 3rd layer



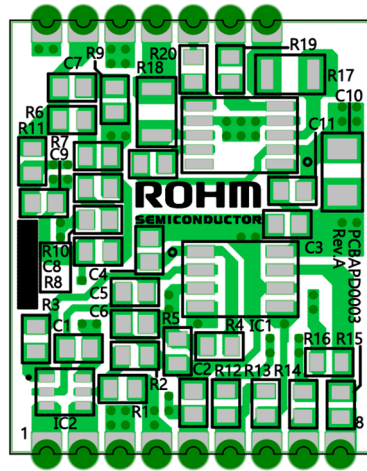
• Botom layer



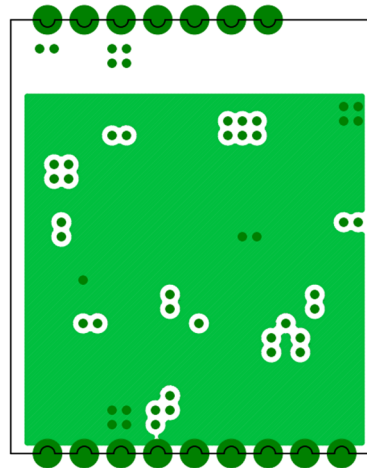
[HBLLC-TSB-001] Board layout

[CCCV Board]

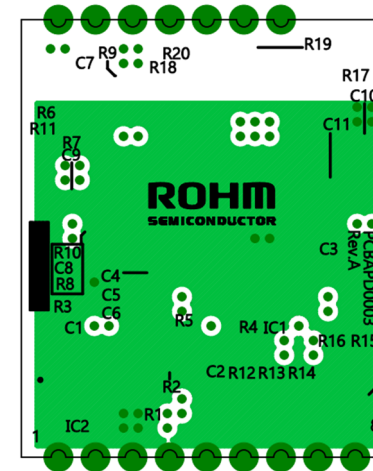
- Top layer



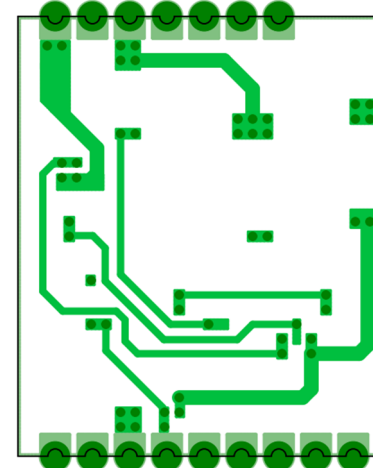
- 3rd layer



- 2nd layer



- Bottom layer



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