ROHM
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3.6 kW Totem Pole PFC with SiC MOSFETs Evaluation Board
TPPFCSIC-EVK-301-ug

User's Guide

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The TPPFCSIC-EVK-301 implements a single-phase AC/DC conversion stage in a Totem Pole PFC topology. Key components are ROHM's Gen. 4 SiC MOSFETs (SCT4045DR) as the main high-frequency switching elements, as well as the BM61S41 single-channel isolated gate driver IC. In addition, SJ MOSFETs (R6076ENZ4) and the BM2P101EK-LB PWM controller IC for the auxiliary power supply, among other components from ROHM, were utilized to create a high-performance AC/DC circuit for single-phase operation.
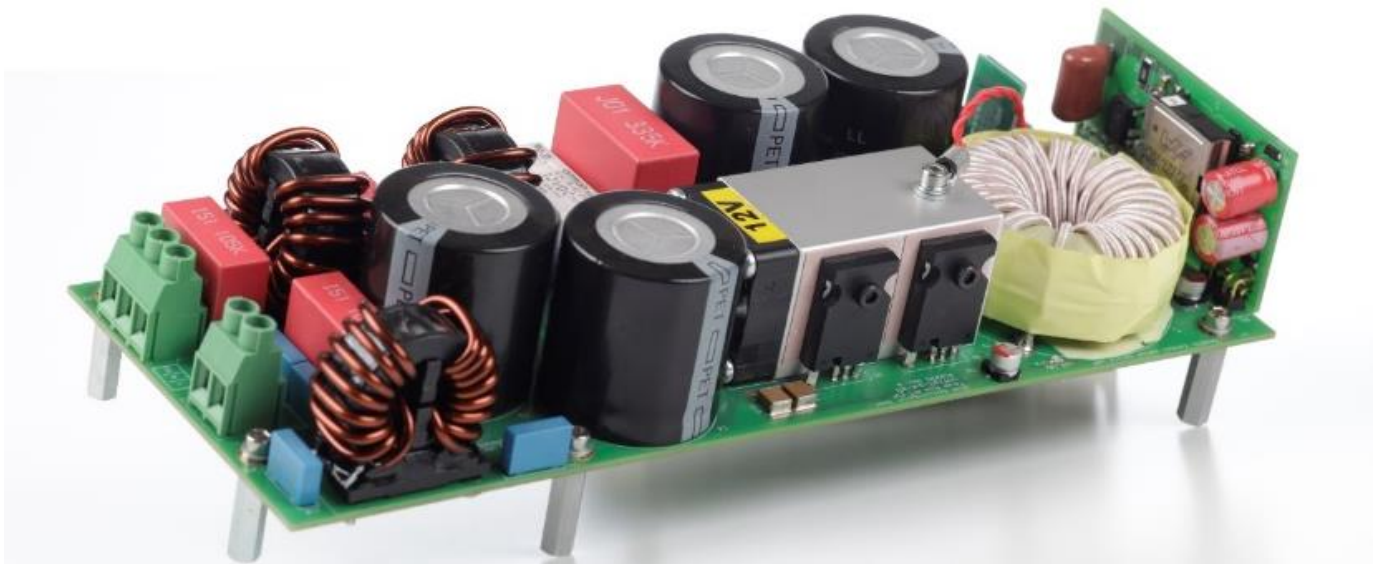

Figure 1: ROHM TPPFCSIC-EVK-301

This user guide will help you understand the connection, operating instructions and important notices and warnings that need to be carefully reviewed prior to the use of the board (Figure 1). Details about the hardware and firmware design of the main building blocks of this evaluation board will also be provided in addition to the schematic of the evaluation board, the Bill of Materials (BOM) as well as the layout and assembly drawing.

Important Notice

This evaluation board including any embedded software is intended for **product evaluation in a research and development environment only.** It is neither intended for resale to end consumers nor authorized to be used by end customer or for household use. This board may not comply with CE or similar standards, including but not limited to the EMC directive 2004/EC/108, and may not fulfil other requirements of the country in which it will be operated. The user is responsible for ensuring that the evaluation board is handled in a manner that is compliant with all standards and regulations in the country of operation.

The microcontroller contained within this EVK is pre-programmed with embedded control software. The user is not authorized to modify the embedded software or make attempts to use it for any other purpose than the operation of this evaluation board. This evaluation board and embedded software have only undergone functional testing under typical load conditions. The design of the board has been tested by ROHM only as described in the user guide. It has not been qualified in terms of safety requirements, manufacturing, and operation over the entire temperature range, or lifetime.

This evaluation board is intended for use only by authorized personnel who have been properly trained to recognize and handle the dangers associated with testing high-voltage equipment and experimenting with high-voltage circuits. It is important to review this user guide, as it contains essential safety warnings. At all times, follow the applicable safety rules for dealing with high voltages. Do not connect or disconnect any wires or probes to the evaluation board while it is connected to a power supply. Ensure that all capacitors on the board have fully discharged before touching any part of the board. Always place the evaluation board under appropriate covers to protect against accidental contact with high-voltage parts before energizing the board.

＜High Voltage Safety Precautions＞

◇ Read all safety precautions before use

Please note that this document covers only the TPPFCSIC-EVK-301 evaluation board and its functions. For additional information, please refer to the datasheets of the specific products.

To ensure safe operation, please carefully read all precautions before handling the evaluation board.

This board operates with lethal voltage levels.

Please read and follow all safety precautions described in the red box below.

Before Use

[1]   Please inspect the parts/components for any damage or missing pieces, which may have resulted from dropping.

[2]   Check that there are no conductive foreign objects on the board.

[3]   Avoid solder splashes when soldering the module and/or evaluation board to prevent damage to nearby components or the device's functionality.

[4]   Check that there is no condensation or water droplets on the circuit board.

During Use

[5]   Be careful not to allow conductive objects to come into contact with the board. This also includes conductive tools such as tweezers and screwdrivers.

[6]   **Brief accidental contact or even bringing your hand close to the board may result in discharge and lead to severe injury or death. Therefore, DO NOT touch the board with your bare hands or bring them too close to the board.**

[7]   If used beyond its rated voltage, the board may be damaged, resulting in malfunctions such as short-circuit, explosion, or other permanent damage.

[8]   Do not manipulate the board during operation and ensure that it is adequately covered to prevent accidental electrical shock, or injuries due to shrapnel in the event of an explosion.

[9]   Use suitable PPE when testing the board. Proper ear protection is a must, as a circuit malfunction can lead to an explosion that could damage your hearing.

After Use

[10] The evaluation board contains capacitors that can hold a hazardous voltage even after power is cut. Therefore, ensure that the circuit is fully discharged after use and confirm this by other means before handling the board.

[11] Even though the board should never be handled with charged capacitors, please wear insulated gloves when handling it as an additional safety measure to prevent electric shock."

This evaluation board is intended for use only in research and development facilities and should be handled **only by qualified personnel familiar with all safety and operating procedures.**

We recommend carrying out operation in a safe environment that includes the use of high voltage signage at all entrances, safety interlocks, and protective glasses.

Safety Precautions

Caution: This evaluation board may only be used by authorized personnel who are trained to recognize and deal with the dangers of testing high voltage equipment and experimenting with high voltage circuits. It should be used only in a laboratory environment equipped for the safe testing of power electronic systems at the relevant voltage levels. Failure to comply may result in damage to equipment, personal injury, or death.

Warning: The DC link and input voltage of this board can reach up to 450 V. Please use only appropriate high voltage differential probes to measure this voltage, especially if the board is connected directly to the grid. Failure to do so may result in equipment damage, personal injury, or death.

Warning: Before disconnecting, connecting, or reconnecting wires or measurement probes to the board, or before touching or manipulating the board in any way, ensure that all external power is removed or disconnected from the board. **Wait at least three minutes** to ensure that the capacitors have discharged to a safe level. Always check by other means that the circuit is fully discharged. Failure to do so may result in equipment damage, personal injury, or death.

Caution: The heatsink and some component surfaces on the evaluation board may become hot during testing and remain hot for a certain time after turn-off. Take appropriate measures while handling the board after use. Failure to do so may cause personal injury.

Caution: Incorrect connection of power supplies or loads can damage the board. Carefully review the board connection information in this document.

Caution: The ground reference (GND_REF) on this board is placed on AC live/neutral (depending on L/N connection). Do not connect the board to any voltage source (AC source) while a flashing tool is connected to the P9 connector. Additionally, do not establish a UART communication with the board through the unpopulated A4 connector. Failure to do so may result in equipment damage, personal injury, or death.
Bluetooth communication with the board is consistently recommended for safer operation.

Mandatory: It is strongly recommended to use ear protection to avoid potential hearing damage from any explosions that may occur due to a catastrophic failure of the board.

Contents

1. Introduction

1.1. Board overview

The TPPFCSIC-EVK-301 comes with an auxiliary power supply board and a Bluetooth communication module. Both are soldered onto the main board. Figure 2 gives an overview of the EVK with the main components highlighted.
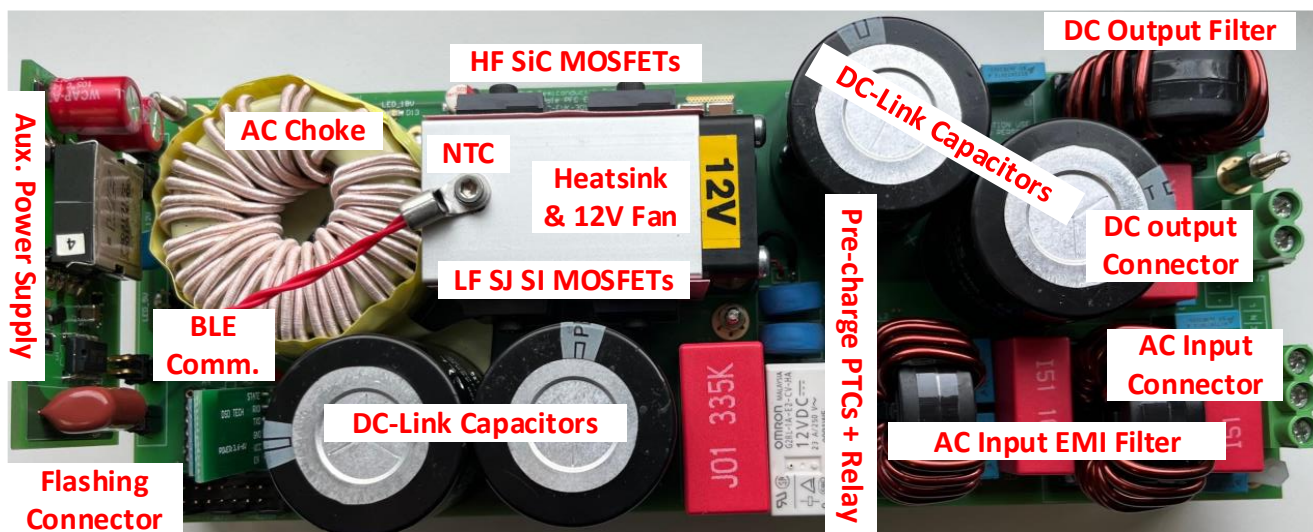

Figure 2: Board overview with main circuit functions

1.2. Circuit diagram

The circuit diagram of the totem pole PFC EVK is presented in figure 3. Where PCB3051 is the main PFC board and PCB3052 is the auxiliary power supply daughter board.
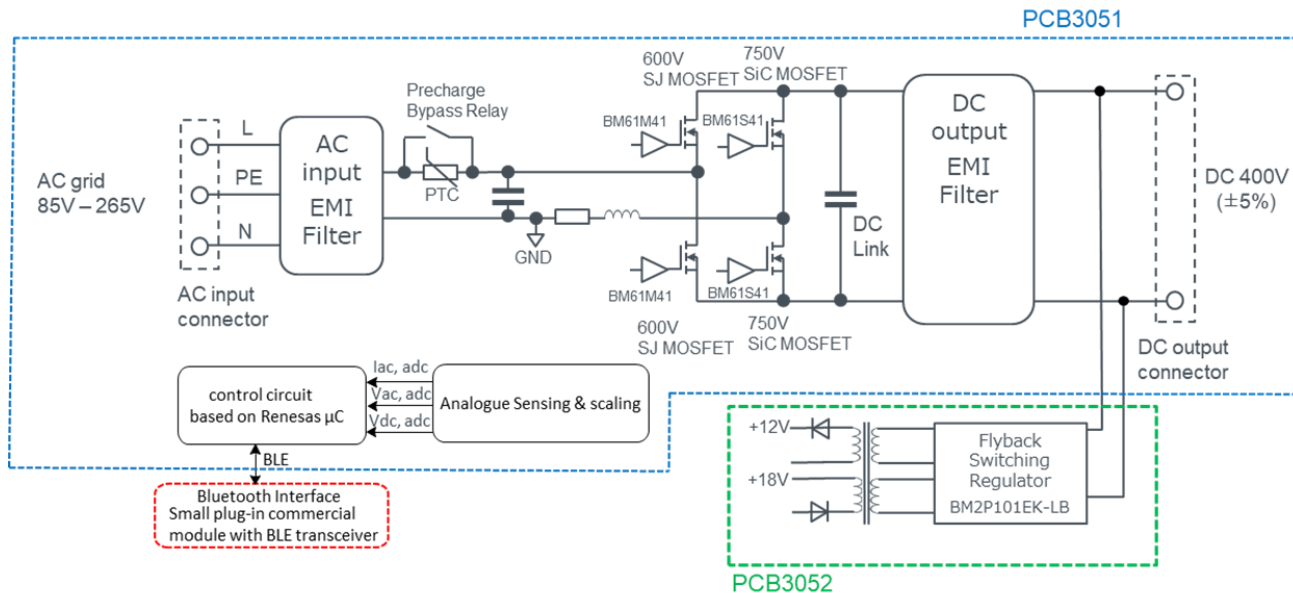

Figure 3: TPPFCSIC-EVK-301 circuit diagram

1.3. Main components

Table 1: Main ROHM products in the TP PFC EVK

Board	Board N°	Function	Part Number	Specification
Main PFC board	PCB3051	HF Switch	SCT4045DR	750V, 45mΩ SiC MOSFET, TO-247-4L
		LF Switch	R6076ENZ4	600V, 76A Si SJ-MOSFET, TO-247
		Gate Driver for SiC	BM61S41RFV-C	3750Vrms, Isolated Gate Driver
		Gate Driver for SJ-MOSFET	BM61M41RFV-C	3750Vrms, Isolated Gate Driver
		Current Sense Shunt Res.	PMR18EZPFV2 L00	3216, 1W Ultra-low Ohmic Chip Resistor 2mΩ
		OpAmp for current sense	LMR1802G-LB	Low offset OpAmp
		Super Fast Recovery Diode	RFN2LAM6STR	SOD-128, 600V
Aux. PS Board	PCB3052	Flyback Switching Regulator	BM2P101FK-LB	PWM DC/DC Converter integrated MOSFET

1.4. TP PFC specifications

Table 2: TP PFC EVK specifications

Parameter	Specification
Input voltage (freq.)	85 – 265 V_{AC} (50±3 Hz or 60±3 Hz)
Output voltage	400V (± 5% voltage ripple)
Output power	3.6 kW @ 230V_{AC}
Switching frequency	100 kHz
Efficiency (at half load & 230Vac)	98.5%
Cooling	Forced air, small fan
Topology	Totem Pole
High frequency switch (Q_3, Q_5)	SCT4045DR (TO-247-4L)
Low frequency switch (Q_4, Q_6)	R6076ENZ4 (TO-247)
Flyback switching regulator	BM2P101FK-LB
Form factor	233 x 89 x ca.40/45 mm*

[*) Depending on the availability of the DC bus capacitors, the total height of the board may change by +5mm.

2. Connections and operating instructions

2.1. Board connections

As discussed in the coming sections, the TP PFC EVK uses the auxiliary power supply (Aux PS) board as a discharge path to remove the stored energy quickly and safely from the DC bus capacitors. Therefore, for safety reasons, the EVK comes with a soldered Aux PS board. The Bluetooth (BLE) communication is also directly soldered as a daughter board onto the main PFC board to maintain reliable contact and communication with the microcontroller.

Thus, the user will only need to connect the AC supply lines (L, N, PE) and the DC load terminals to the DC connector as indicated in figure 4 (also indicated by silkscreen on the PCB).
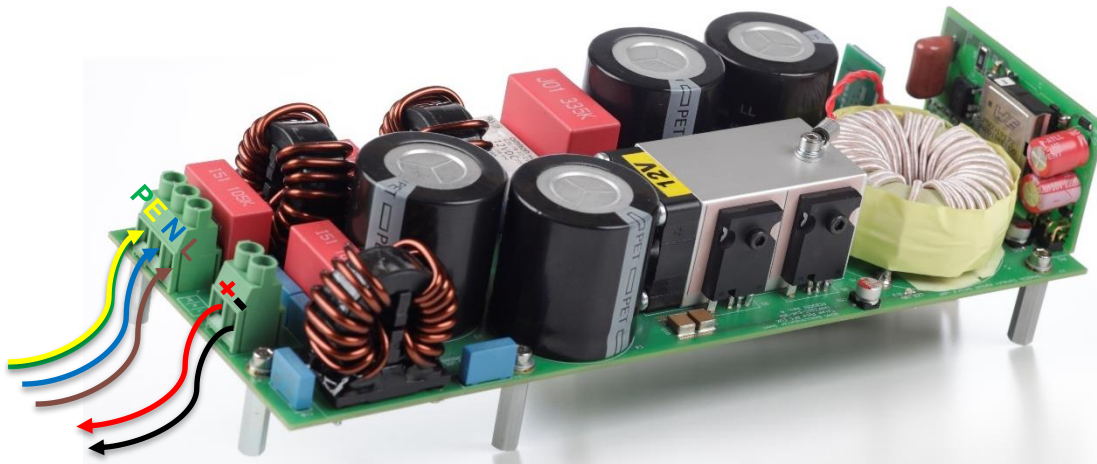

Figure 4: Board electrical wiring connections

To evaluate the board's performance, a laboratory set-up example is provided in figure 5. Note that this is just an example and not a requirement. Other test setups are possible. It is recommended to carefully plan the test set-up to avoid safety risks.
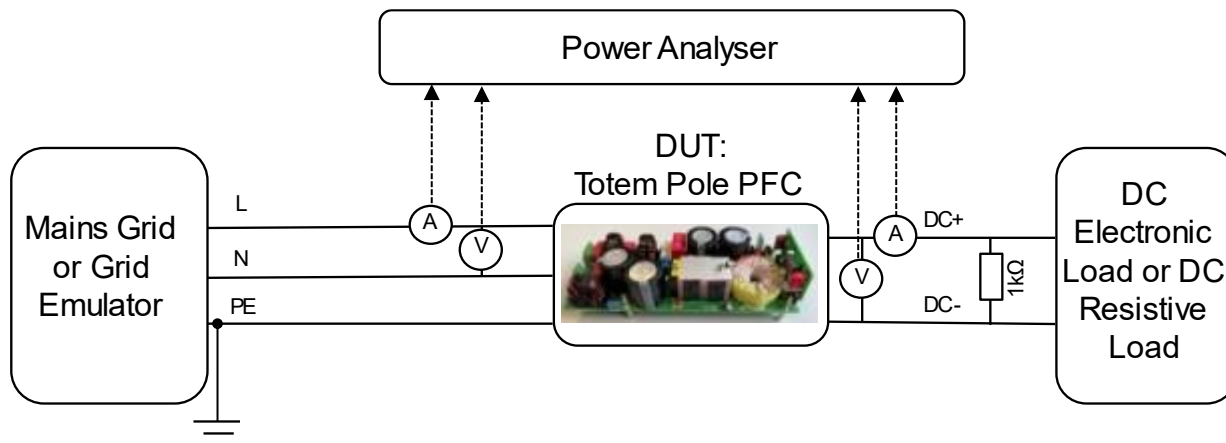

Figure 5: Totem Pole PFC test set up example

2.2. ROHM Graphical User Interface "GUI" SW

As introduced in the quick start guide [No. 66QS002E Rev.001] of this EVK, the user can control the PFC converter and have read/write access to the registers content in the flash memory. The ROHM EVK GUI SW is a powerful Windows-based desktop application, which provides an intuitive graphical user interface capable of displaying and logging the real-time device data and configuring the device functions through a graphical register editor, to name a few. To get the GUI up and running, please refer to the start-up procedure as explained in the quick start guide. Detailed explanation of the ROHM EVK GUI SW built-in functions can be found on the website: https://fscdn.rohm.com/en/products/databook/applinote/ic/sensor/rohm-evk-sw_ug-e.pdf

The detailed description of the TPPFCSIC-EVK-301 GUI registers is given in table 3:

Table 3: Totem Pole PFC EVK registers description

Access	Name	Values	Description
R	State	INIT	PFC in "Initial" state
		FAULT	PFC in a "Fault" condition
		READY	PFC is "Ready" to run
		PRERUN	PFC is "Initiating running" state
		RAMP_UP	PFC is "Ramping up" to set DC voltage
		RUN	PFC is "Running"
R	Status	PLL_Om_LOW	PLL calculated Omega is below the minimum threshold
		PLL_Om_HIGH	PLL calculated Omega is above the maximun threshold
		PLL_Vq_LOW	PLL Vq voltage is below the lower threshold
		PLL_Vq_HIGH	PLL Vq voltage is above the upper threshold
		PLL_Vd_LOW	PLL Vd voltage is below the lower threshold
		PLL_Vd_HIGH	PLL Vd voltage is above upper threshold
		TEMP_HIGH	SiC MOSFET reached the over temperature limit
		VDC_HIGH	The DC bus voltage is higher than OVP limit
		VDC_LOW	The DC bus voltage is below the UVLO limit
		IAC_HIGH	Input AC current peak is higher than the limit
R	v_ac_in		Instantaneous input AC voltage
R	v_dc_in		Instantaneous DC output voltage
R	i_ac_in		Instantaneous AC input current
R	v_ac_in_freq		AC input frequency (50Hz/60Hz)
R	v_dc_set		Output DC voltage set point
R/W	Freq	AUTO_DETECT	AC frequency auto-detection
		50Hz	AC Input frequency is fixed to 50Hz
		60Hz	AC Input frequency is fixed to 60Hz
R/W	Auto_mode		Automatic output enable
R	I_AC_MAX		Maximum allowable instantaneous AC input Current
R	UNDERVOLT-AGE_LIMIT		DC output undervoltage limit
R	OVERVOLT-AGE_LIMIT		DC output overvoltage limit
R	temp		Measured temperature at the heatsink
R	TEMP_FAN_EN_LIMIT		Temperature value to enable the cooling Fan
R	TEMP_FAN_DIS_LIMIT		Temperature value to disable the cooling Fan
R	TEMP_ERROR_LIMIT		SiC MOSFET over temperature limit

R/W	PLL_SOGI_alpha		PLL SOGI "Alpha" gain
R/W	PLL_SOGI_beta		PLL SOGI "Beta" gain
R/W	PLL_SOGI_gamma		PLL SOGI "Gamma" gain
R	PLL_omega		Estimated omega from the PLL
R/W	Kp_slew_rate		Slew rate applied to Kp gain to avoid a sudden change between transient gain and normal gain
R/W	PI_TRANS_V_Kp_LIM		Hysteresis upper limit for voltage loop during load transient
R/W	PI_NORM_V_Kp_LIM		Hysteresis lower limit for voltage loop during steady state
R/W	PI_TRANS_VOLT-AGE_Kp		Kp gain of the PI voltage controller during load transients
R/W	PI_VOLTAGE_Kp		Kp gain of the PI voltage controller during steady state
R/W	PI_VOLTAGE_Ki		Ki gain of the PI voltage controller
R/W	PI_VOLTAGE_Kt		Anti-windup gain at the PI voltage controller output
R	PI_VOLTAGE_out		PI voltage controller output
R	I_REF_MAX		Maximum allowable AC current reference
R/W	PR_CUR-RENT_out_LIMIT		PR controller output limit
R/W	PR_CURRENT_Klim		PR controller output anti-windup gain
R/W	PR_CURRENT_Kp		PR controller Kp gain
R/W	PR_CUR-RENT_Kr_1st		PR controller resonant gain of the 1st harmonic
R/W	PR_OMEGA_C_1st		PR controller resonant width of the 1st harmonic
R/W	PR_CUR-RENT_Kr_3rd		PR controller resonant gain of the 3rd harmonic
R/W	PR_OMEGA_C_3rd		PR controller resonant width of the 3rd harmonic
R/W	PR_CUR-RENT_Kr_5th		PR controller resonant gain of the 5th harmonic
R/W	PR_OMEGA_C_5th		PR controller resonant with of the 5th harmonic
R/W	PR_CUR-RENT_Kr_7th		PR controller resonant gain of the 7th harmonic
R/W	PR_OMEGA_C_7th		PR controller resonant width of the 7th harmonic
R/W	PR_CUR-RENT_Kr_9th		PR controller resonant gain of the 9th harmonic
R/W	PR_OMEGA_C_9th		PR controller resonant width of the 9th harmonic
R	PR_CURRENT_out		PR controller output
R	Notch_width_rad		Notch filter width in radians
R	v_dc_filtered		Filtered VDC value
R/W	Flash_ctrl_cmd	NONE	Flash control command: None
		FLASH_LOCKED	Flash control command: Locked
		FLASH_UNLOCKED	Flash control command: Unlocked
R/W	Execute_cmd	NONE	Flash execute command: None
		STORE_USER_PARAMS	Flash execute command: Store modified user parameters
		RESET_DE-FAULT_PARAMS	Flash execute command: Reset to default parameters
		RUN_OFFSET_CALI-BRATION	Flash execute command: Run AC measurements offset calibration

3. Totem Pole PFC hardware design

3.1. Input Inductor design

The totem PFC AC choke is designed to keep the current ripple at less than 30% of the maximum peak input current while maintaining CCM operation. The inductance value is a function of the converter switching frequency and the DC output voltage as well as the input current and the duty cycle. To maintain CCM operation, the minimum inductance value can be calculated when the duty cycle D=0.5 as given by equation 1:

$$L_{min} = \frac{\text{D x }(1-D)\text{ x V}_{out}}{\text{I}_{ripple}\%\text{ x F}_{sw}} = \frac{0.5\text{ x }(1-0.5)\text{ x }400}{0.3\text{ x }16\text{ x }\sqrt{2}\text{ x }100\text{ x }10^3} = 147\mu H$$

Equation 1: Calculation of minimum inductance value

$$I_{Lmax} = \frac{\sqrt{2}\times Pout}{V_{in}} \times \left[1 + \frac{\text{I}_{ripple}\%}{2}\right] = \frac{\sqrt{2}\times 3600}{230} \times \left[1 + \frac{0.25}{2}\right] = 26.2A$$

Equation 2: Calculation of maximum inductor current

In PFC applications, it is not only important to maintain a low THDi and a low EMI at full load but also at light loads where the inductor current is low, and the converter tends to work in DCM mode. For this purpose, a swinging choke is usually used as it provides a higher inductance at low DC bias current as well as a controlled inductance at high load.

In this design a custom-made inductor from Würth Elektronik is used. The winding is made of litz wire for its smaller form factor compared to flat wire as well as its low losses in high switching frequency. A ring core made of a soft metal powder with an initial permeability of 60 is selected. The powder core helps in achieving smaller inductor size, higher saturation currents, higher inductance at light loads and controlled inductance at high loads compared to ferrite cores [3].
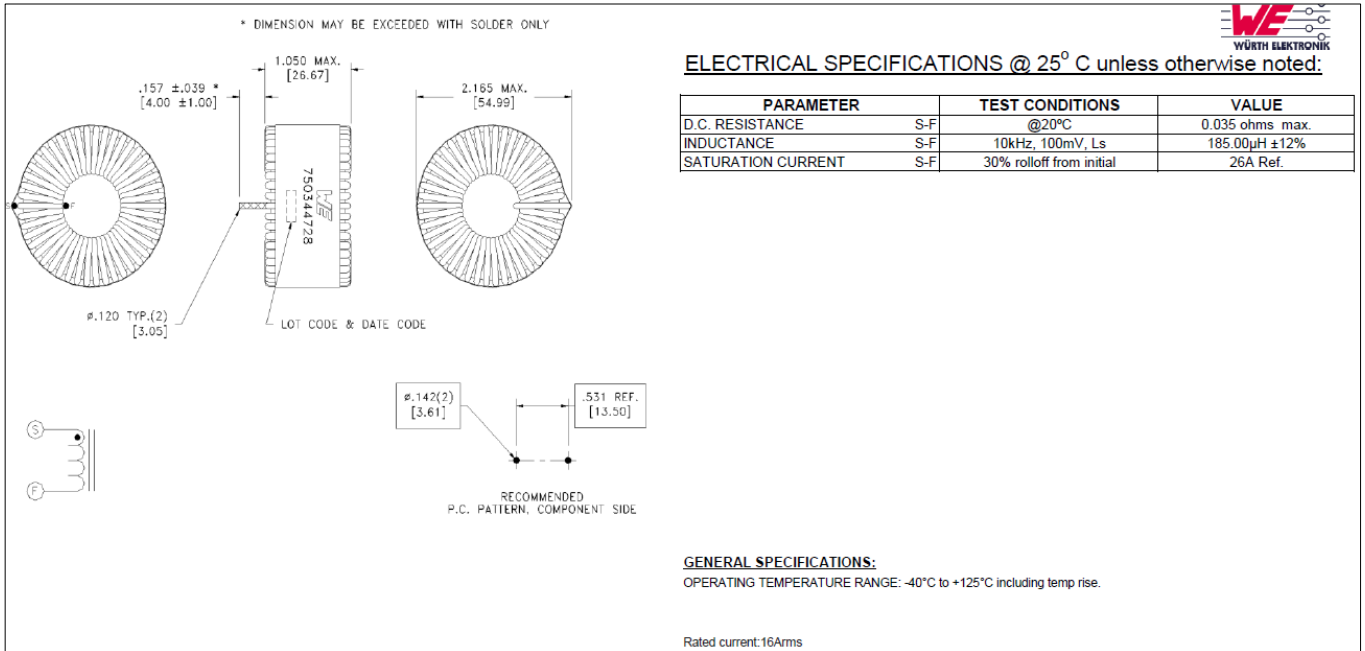

Figure 6: PFC Inductor dimensions and specifications

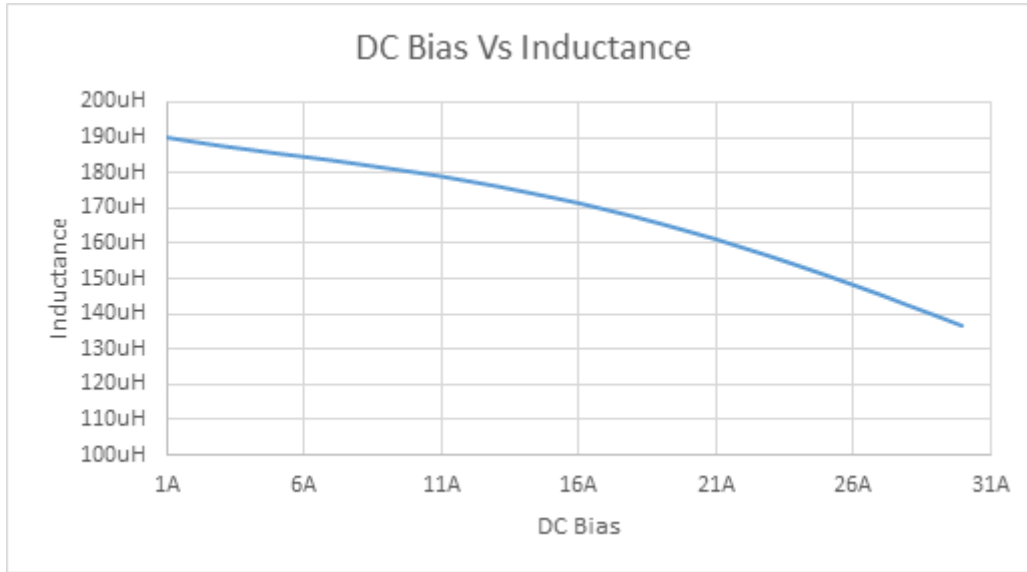The inductance vs DC bias of the AC choke is presented in figure 7.

Figure 7: PFC inductor: L vs DC bias

The inductor saturation current must be higher than the calculated maximum inductor current (26.2A for this design). The designed inductor has an initial inductance of 185μH ±12% that rolls off to ~148μH at the maximum peak input current, which is very close to the minimum required inductance value at peak current.

3.2. Output DC capacitor design

The output DC capacitors are normally designed to meet requirements on the minimum hold-up time and DC voltage ripple. The hold-up time is usually specified in milliseconds, and it indicates how long should the converter still operate in regulation after occurrence of an AC input failure. The DC voltage ripple measures the amplitude of the two-line frequency AC component in the rectified DC output.

$$C_{out} \geq \frac{2 * P_{out} * t_{hold}}{V_{out}^2 - V_{out.min}^2} = \frac{2 * 3600 * 10 * 10^{-3}}{400^2 - 345^2} = 1.76mF$$

Equation 3: Minimum DC output capacitance to meet 10ms hold-up time

$$C_{out} \geq \frac{P_{out}}{2 * \pi * f_{line} * \Delta V_{out} * V_{out}} = \frac{3600}{2 * \pi * 50 * 20 * 400} = 1.44mF$$

Equation 4: Minimum DC output capacitance to meet ±5% voltage ripple

Therefore, 1.76mF is the minimum required DC capacitance to fulfil these two criteria. To meet this design target, the TDK capacitor B43647B5567M05# was selected. It has a 560μF capacitance value, 450V rated voltage and 20% tolerance. Four pieces of this Aluminum capacitor are placed in parallel which gives a total nominal capacitance of 2.24mF and a minimum of 1.792mF considering the capacitor tolerance.

3.3. Analog sensing and scaling

3.3.1. Vac sensing

The AC input voltage is sensed with a differential amplifier stage as shown in figure 8. As will be described in the coming sections, this measurement will be used by the PLL to extract the AC phase angle which is essential for the controller to shape the AC line current to the AC line voltage.
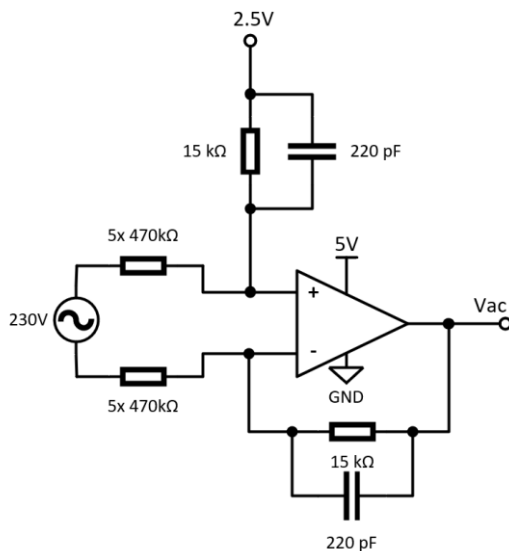
Figure 8: Vac measurement

3.3.2. Vdc sensing

A differential voltage measurement between DC positive and negative potentials provides the DC voltage as shown in figure 9.
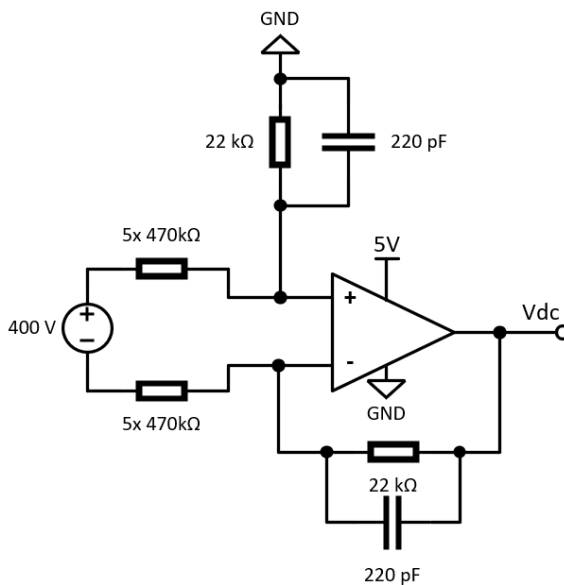
Figure 9: Vdc measurement

3.3.3. Iac sensing

The AC input current is measured by means of a 2mΩ shunt resistor placed on the AC neutral line. The low voltage drop across the shunt is then scaled by the differential amplifier stage as shown in figure 10.
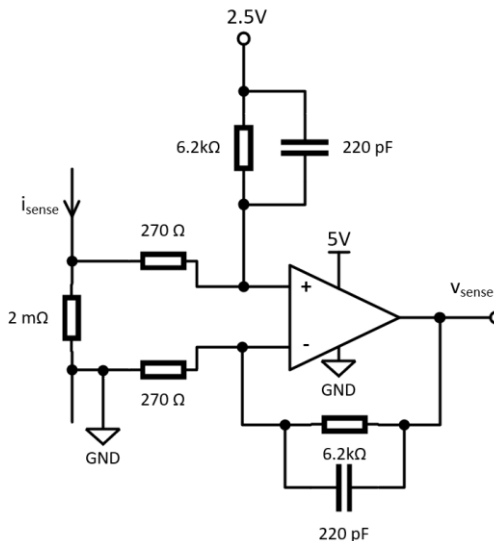

Figure 10: Input AC current measurement

3.3.4. Temperature sensing

The TPPFCSIC-EVK-301 is equipped with an eyelet style NTC thermistor, which is mounted on top of the MOSFETs heatsink. The NTC mounting whole was placed close to the SiC MOSFET for a better reading of the case temperature. The selected 10kΩ NTC (at 25°C) forms a 5V voltage divider with another 10kΩ resistor on the PCB. Table 4 provides the NTC thermistor resistance vs temperature and the corresponding ADC reading.

Table 4: NTC R/T Calculation

T [°C]	R nom [Ω]	Vadc(V)
0	32624,23	3,83
10	19896,9	3,33
20	12492,75	2,78
30	8055,96	2,23
40	5323,88	1,74
50	3598,72	1,32
60	2483,82	0,99
70	1747,65	0,74
80	1251,8	0,56
90	911,59	0,42
100	674,11	0,32
110	505,68	0,24
120	384,41	0,19
130	295,88	0,14
140	230,4	0,11
150	181,37	0,09

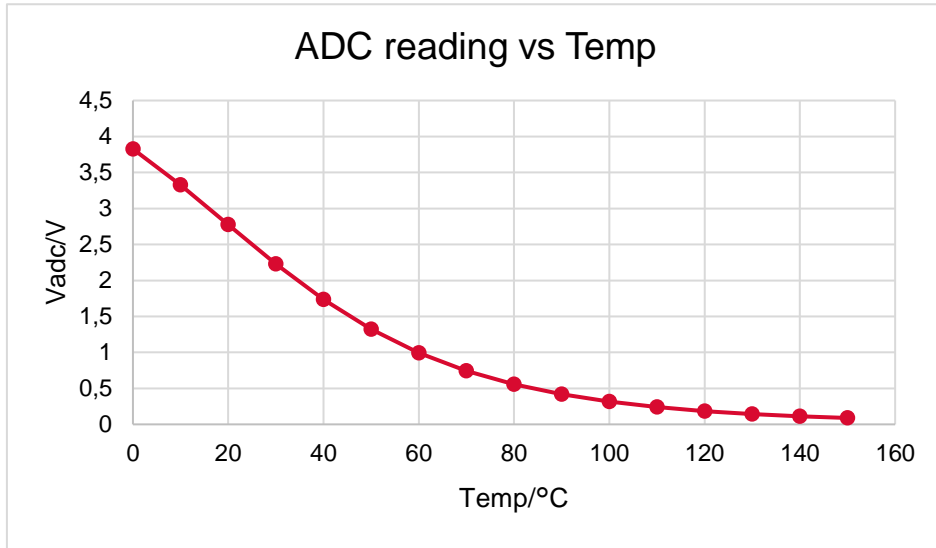Figure 11 represents the ADC voltage reading vs the measured heatsink temperature.

Figure 11: ADC reading vs heatsink temperature.

3.4. Gate driver design

The fast leg switches are driven by ROHM's BM61S41RFV-CE2 gate driver. This single channel gate driver comes with an isolation voltage of 3750Vrms, an UnderVoltage LockOut (UVLO) of 15V (typ.) which is more suitable for driving SiC MOSFETs. It also features an active Miller clamp protection for the driven MOSFET. The primary and secondary sides of the gate driver are powered up by 5V and 18V respectively.
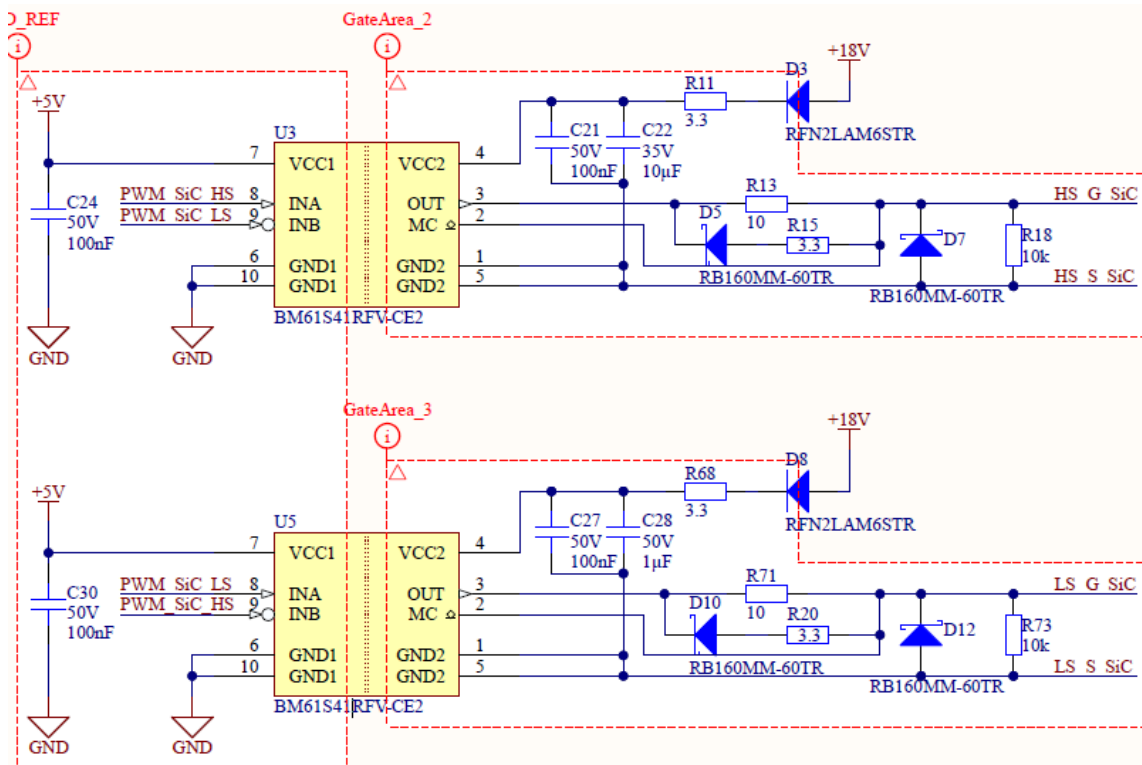

Figure 12: SiC MOSFET gate driver circuit

The SJ MOSFETs in the slow leg are driven by ROHM's BM61M41RFV-CE2 gate driver which has a lower UVLO threshold (7.8V -typ.) compared to the UVLO of the SiC MOSFET gate driver. Except for this small difference, the two gate drivers are identical in all other features.
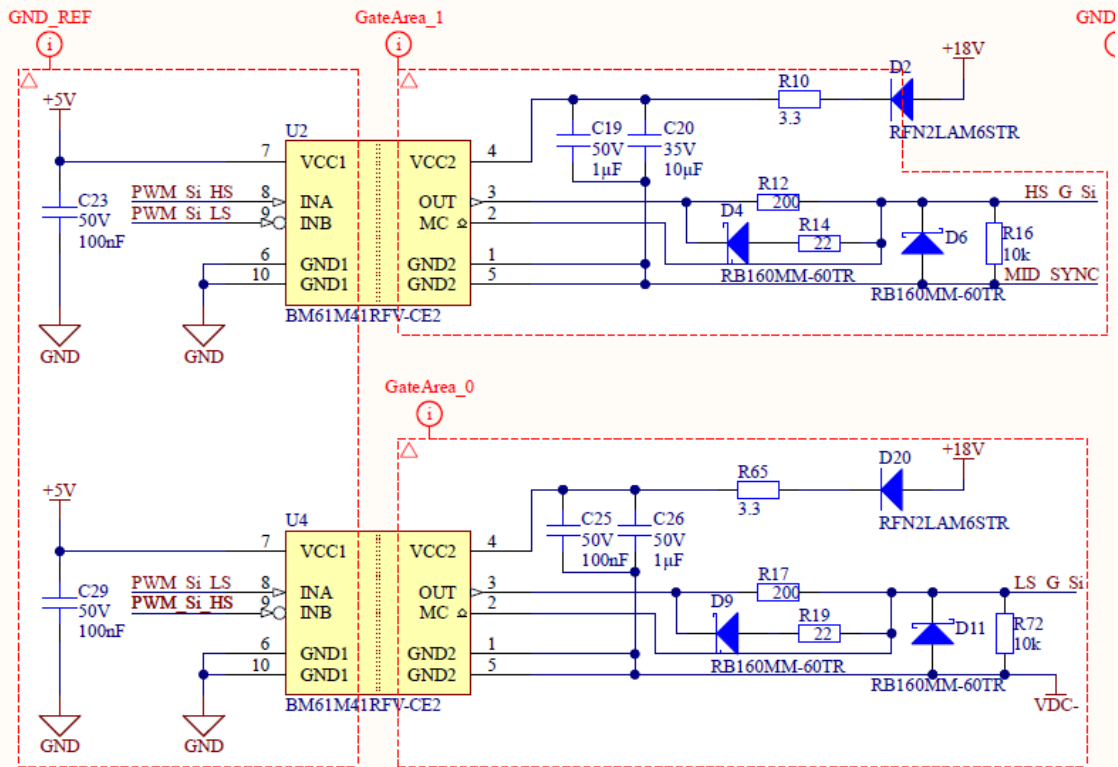
Figure 13: SJ MOSFET gate driver circuit

3.5. Auxiliary Power Supply board (Aux PS)

The Aux PS daughter board (PCB3052) generates the necessary supply voltages for the functioning of the main board (PCB3051).
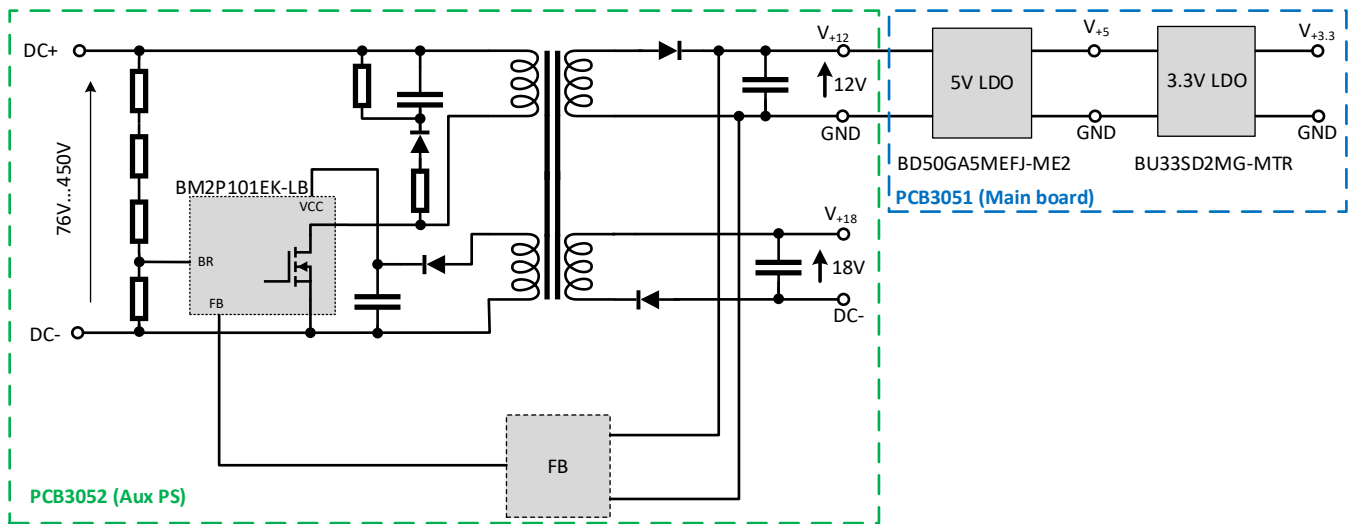Figure 14 shows the circuit diagram of the Aux PS board.

Figure 14: Aux PS circuit diagram

At power up, the bulk capacitors connected to the DC bus undergo a gradual charging process by means of the precharge circuit.
As the DC bus voltage is directly applied to the IC, the voltage at the BR pin of the flyback controller (BM2P101EK-LB) becomes
higher than its UVLO threshold (Typ=0.7V). The buildup of VCC voltage continues until it exceeds its UVLO1 threshold
(Typ=15.5V). The IC then starts to operate, and the switching begins until full regulation of the +12V and +18V outputs is reached.
On the main PFC board, a pair of Low Dropout Regulators (LDOs) have been incorporated to generate the necessary 5V and
3.3V supply voltages.

4. Totem Pole PFC FirmWare (FW) design

4.1. Control block diagram and description of main control blocks

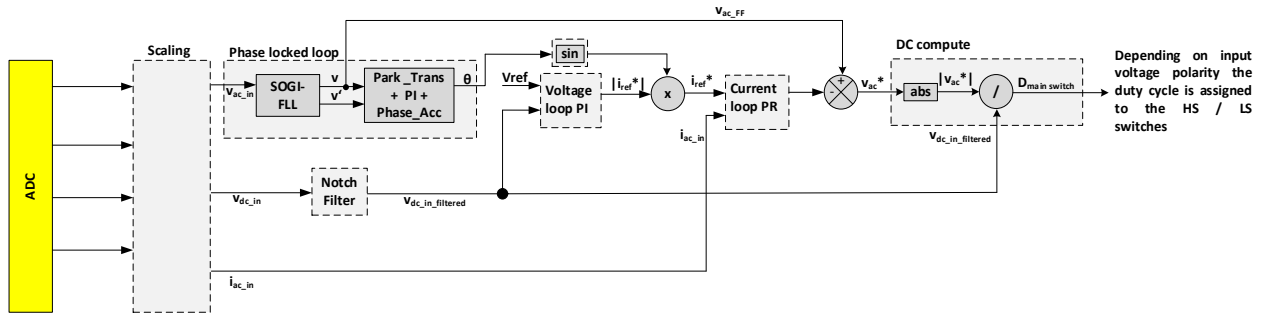Figure 15 shows the block diagram of the totem pole PFC digital controller.

Figure 15: TP PFC EVK digital control block diagram

In a totem pole PFC application, an accurate detection of the phase angle of the AC input voltage and the AC zero crossing is very critical. This is why a Phase-Locked-Loop (PLL) is used in this EVK to enable digital and accurate detection of the phase angle and zero crossing of the input voltage. An important building block of the PLL is the Second Order Generalized Integrator with Frequency-Locked-Loop (SOGI-FLL). Unlike the conventional SOGI method that generates in-phase and quadrature-phase signals from the input voltage with accurate tracking at AC frequencies of 50Hz or 60Hz, the implemented SOGI-FLL incorporates an added frequency feedback loop and DC offset compensation. This enhancement enables the system to maintain precise tracking of input voltage, even in scenarios involving distorted grids with DC offset and frequency drift.

The control algorithm is made of an outer voltage loop and an inner current loop. The current loop is executed at one third of the 100kHz switching frequency (ca. 33.3kHz), ten times faster, than the voltage loop which is executed at 3.33kHz.

4.1.1. Current loop controller

The inner loop forces the inductor current to match the current reference. The magnitude of this reference is determined by taking the absolute value of the output from the voltage loop. Meanwhile, the phase angle is computed using the PLL block. Since the current reference is generated from the voltage loop, the bandwidth of the current loop should be higher than the bandwidth of the voltage loop to ensure a proper tracking of the current reference and therefore a good THD under steady state operation.

The simple Proportional-Integral (PI) controller is the most used compensator for regulating DC components. It has a pole located at 0Hz, resulting in an infinite DC gain that effectively minimizes DC steady-state error to zero. In the totem pole PFC, the current reference is sinusoidal, therefore a simple PI controller will always show an error at the fundamental frequency and will not track the harmonic reference correctly. For this reason, the Proportional-Resonant (PR) controller is implemented in the current loop. The PI and PR controllers are very similar in the sense that they both have an infinite gain at a certain frequency. For the PI controller this frequency is 0Hz (DC) and for the PR controller, this frequency is the resonance frequency ω_0 (AC) of the resonator. Thanks to its infinite gain at the resonance frequency ω_0, the resonator can remove the steady state error at this frequency. Therefore, by setting ω_0 equal to the fundamental frequency of the AC input current (50Hz/ 60Hz) the steady state error can be reduced to zero at 50Hz/60Hz.

Since the grid voltage generally contains higher order harmonics, selective harmonic compensation is implemented in this design by cascading several resonant blocks. These resonators are respectively tuned to resonate at the third, fifth, seventh and ninth order harmonics. By doing this, the AC steady errors can be completely reduced to zero at those frequencies which helps achieve perfect sinusoidal AC current reference tracking.

While the resonant terms are only able to remove the error at their respective resonance frequencies, the PR controller also contains a proportional gain to stabilize the closed loop and remove the error at other frequencies.
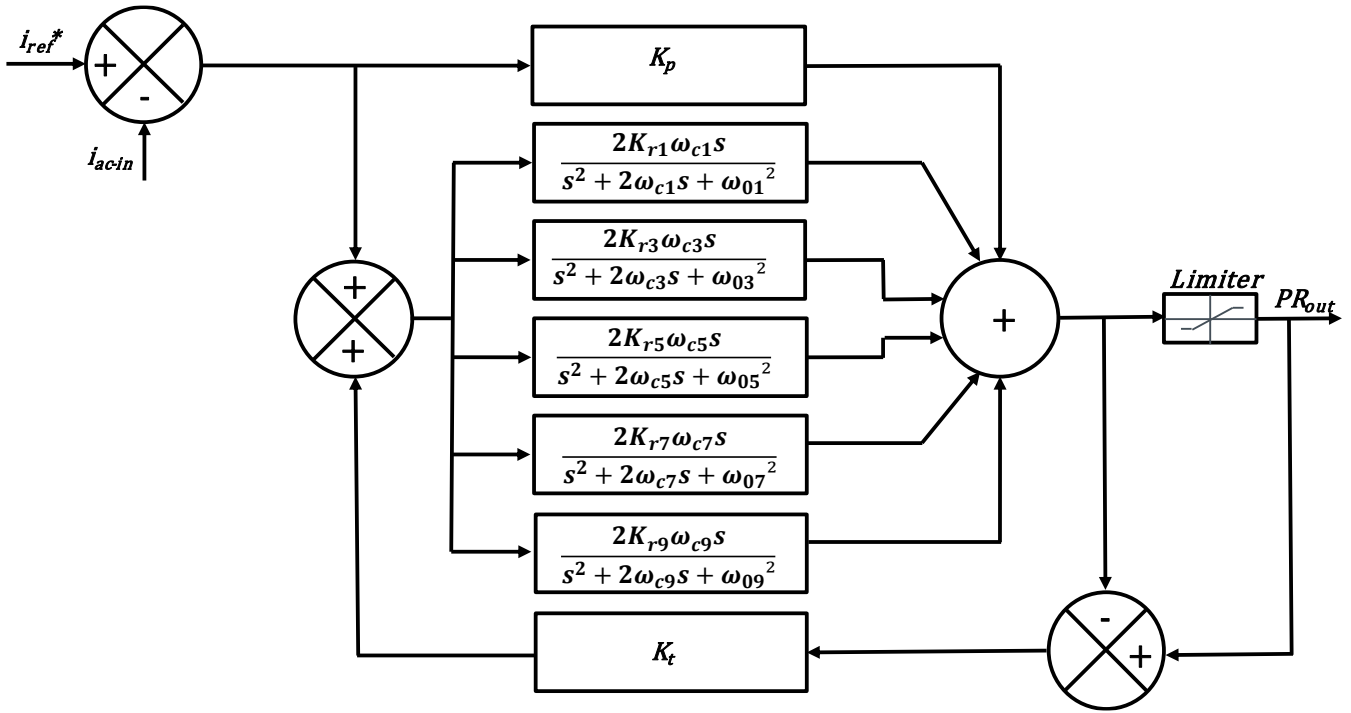
Figure 16: Proportional Resonant current loop controller with harmonics compensation and resonator anti-windup

Figure 16 shows the implemented PR controller with harmonics compensation up to the ninth order. Practically, the implementation of an infinite gain resonator in a digital controller is difficult, this is why a more practical way is to introduce some damping around the resonant frequency. By doing this, the gain at ω_0 becomes finite, but still high enough to achieve sufficiently small steady state error. The equations of the resonators are given in figure 16, where:

- Kp: Proportional gain of the PR current controller.

- $K_{r1}..K_{r9}$: Resonator gain of the fundamental and odd harmonics up to the ninth.

- $\omega_{01}..\omega_{09}$: Resonance frequency of the resonators up to the ninth harmonic.

- $\omega_{c1}..\omega_{c9}$: Resonant cut-off frequency which brings some dumping around ω_0 (i.e., width of the resonator)

- k_t: PR controller anti-windup gain.

As the output of the controller is physically limited by the fact that the duty cycle cannot exceed 100%, saturation of the controller occurs, and the feedback loop breaks. When this happens, the open loop should be stable as well, that's why an anti-windup mechanism with back calculation is implemented to prevent the resonators from winding-up as the controller output is saturated.

4.1.2. Voltage loop controller

In the outer voltage control loop, a Proportional-Integral (PI) controller is employed. Initially, the DC bus voltage is sensed and subsequently passed through a notch filter to eliminate the two-line frequency ripple. The filtered voltage is then compared with DC voltage reference to generate the control error. The magnitude of input reference current, $|i_{ref}{}^*|$, is obtained from the absolute value of PI controller. As the magnitude is constrained within physical limits, the controller can become saturated, resulting in a disruption of the feedback loop. Therefore, to prevent instability, an anti-windup mechanism is also implemented here to prevent the integrator from winding up when the output is saturated.
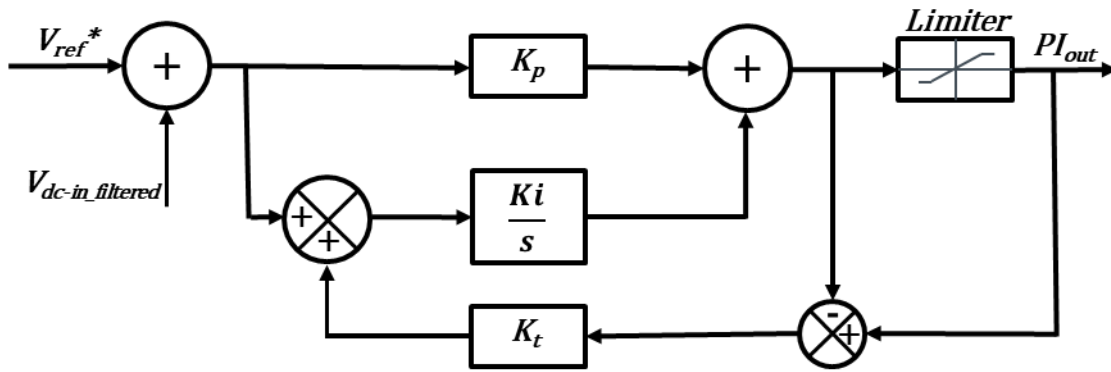
Figure 17: Proportional Integral voltage loop controller with anti-wind up

Figure 17, shows the block diagram of the implemented voltage loop PI controller where:

- k_p: PI controller proportional gain.

- k_i: PI controller integral gain.

- k_t: PR controller anti-windup gain.

Voltage loop controller: improvement features

Notch filter:

The DC bus of a single-phase totem pole PFC is not purely DC. In fact, it contains the typical two-line frequency voltage ripple (100Hz or 120Hz depending on the grid's frequency). The amplitude of this voltage ripple depends on the capacitance value of the DC capacitors connected to the bus. When sensing the DC bus voltage, this two-line frequency ripple propagates to the voltage controller output, which is undesirable since the current reference for the current loop is obtained from the voltage controller output as previously explained. The multiplication of voltage controller output and the sine of the calculated phase angle results in a current reference rich with third harmonic content and thus resulting in a high THD and low power factor.

A common solution to prevent this from happening is to remove the two-line frequency ripple by means of filtering. Different filters are used for this purpose including moving average filters, low pass filters and the use of a notch filter. In this design a notch filter tuned at the two-line frequency is implemented to remove the DC bus ripple from the sensed voltage as shown in figure 15. In addition, the notch filter was selected for its fast dynamic response and its low impact on the stability.
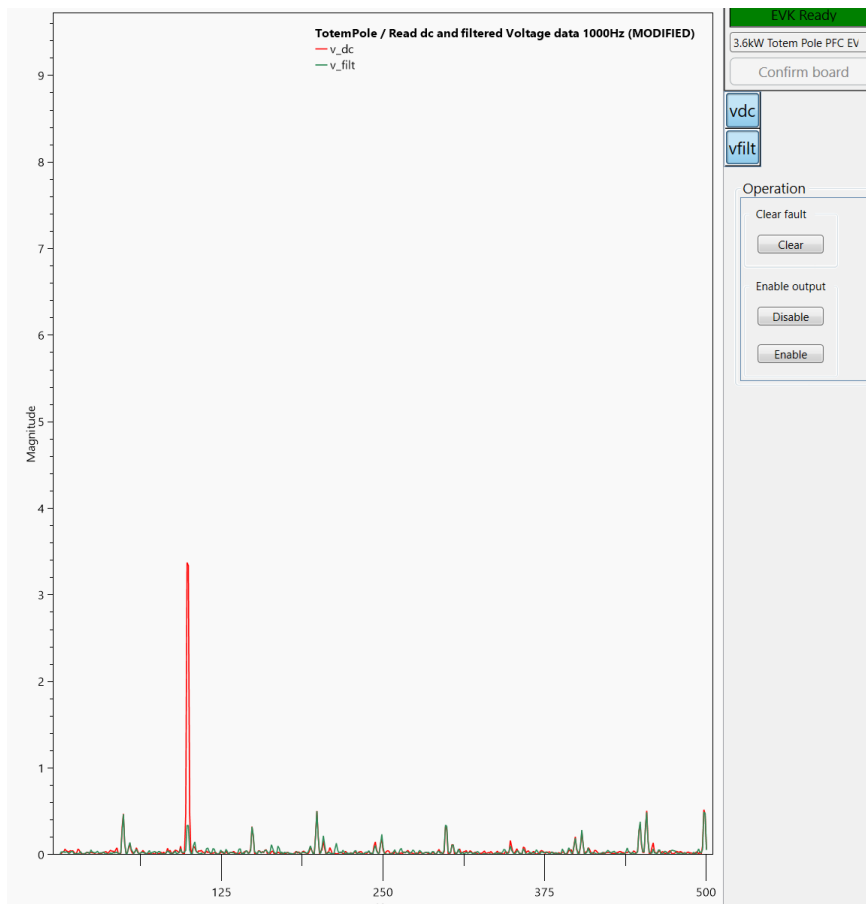
Figure 18: Effect of the notch filter on the two-line frequency voltage ripple

Figure 18 shows the FFT of the sensed DC voltage with and without the notch filter. The unfiltered DC voltage (red) has a high magnitude at 100Hz (second harmonic) whereas the second harmonic of the filtered DC voltage (green) was reduced to almost zero. This shows the effectiveness of the implemented notch filter in removing the two-line frequency voltage ripple from the measured DC voltage.

As previously mentioned, the implemented SOGI-FLL is capable of automatically detecting the grid's operational frequency as well as frequency variations. This enables the notch filter to dynamically adjust itself by modifying its "notch frequency" based on the estimated grid frequency obtained from the SOGI-FLL which in turn properly removes any two-line frequency voltage ripple.

Proportional gain hysteresis:

As previously discussed, the voltage loop should have a low bandwidth to reduce the effect on the current loop and thus THD and power factor. During load transients, particularly in scenarios involving substantial load dumps, the limited bandwidth of the voltage loop hinders rapid response for DC bus regulation. This can potentially result in significant overshooting, possibly exceeding the Over Voltage Protection threshold (OVP).

To improve the voltage controller's response to overshoots and undershoots during load transients, a hysteresis band is introduced in the voltage loop. The idea is to compare the absolute value of the voltage error at input of the PI controller (i.e., "$|PI_{Voltage-e}|$ = $|V_{ref}{}^*- V_{dc-in-filtered}|$") with two defined thresholds.

If the absolute value of the error is less than the lower threshold, the normal proportional gain is used in the PI controller. This basically means:

- The converter is running in the steady state.

- The DC bus voltage is within its nominal 400V ±5%.

- The voltage loop retains its originally designed low bandwidth.

When the absolute value of the error exceeds the upper threshold, the proportional gain of the PI controller is then increased to a higher value. This indicates:

- An occurrence of a load transient event leading to an undershoot or overshoot.

- The DC bus voltage falling either below or exceeding the nominal range of 400V ±5%.

- An enhanced bandwidth of the voltage loop that rapidly mitigates undershoots or overshoots on the DC bus, ensuring they remain within the permissible maximum voltage limits.

By introducing this hysteresis band into the voltage loop, the proportional gain is promptly reset to its normal value once the DC bus voltage returns within the nominal range.
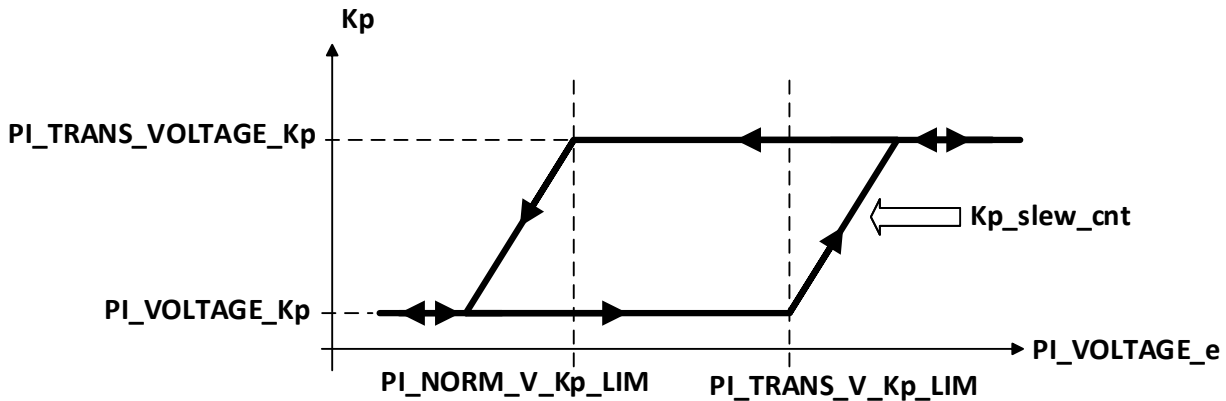

Figure 19: Proportional gain hysteresis in the voltage loop

Figure 19 depicts the implemented hysteresis band in the voltage loop. Where:

- **PI_NORM_V_Kp_LIM**: is the lower threshold of the hysteresis band. During steady state, the absolute value of the PI voltage error is less than this threshold.

- **PI_VOLTAGE_Kp**: is the PI controller proportional gain during steady state.

- **PI_TRANS_V_Kp_LIM**: is the upper threshold of the hysteresis band. During load transients, the absolute value of the PI voltage error is higher than this threshold.

- **PI_TRANS_VOLTAGE_Kp:** is the PI controller proportional gain during load transients.

Additionally, some important notes about the proportional gain hysteresis in the voltage loop are listed below:

- To avoid sudden changes in the dynamics of the controller and to ensure stability, the transition from the lower to the higher proportional gain is controlled by the factor "**Kp_slew_rate**".

- The use of the filtered DC bus sensing, by means of the notch filter, enables good calculation of the PI voltage error which is then compared against the thresholds of the hysteresis band.

- The thresholds of the hysteresis band were determined based on the DC voltage ripple at full load along with a margin for noise.

4.2. Soft start at AC zero crossing

The most common challenge that is inherent to the totem pole PFC topology is the occurrence of current spikes at the AC zero-crossing. These are mainly caused by the output parasitic capacitor "C_{OSS}" and the associated reverse recovery charge "Q_{rr}" of the line frequency switched MOSFETs, which are only changing state on the AC zero-crossing. A detailed analysis of the AC current spikes and waveforms in a TP-PFC topology is given in [2].

In this TP-PFC EVK a soft-start sequence is implemented after every AC zero crossing. This involves a ramping up of the duty cycles applied to the high frequency SiC MOSFETs (Q_3, Q_5) and fine control over the turn-on of the low frequency Si SJ MOSFETs (Q_4, Q_6). The implementation of this soft start achieved significantly reduced current spikes. The implemented MOSFET's switching sequence is shown in figure 20.
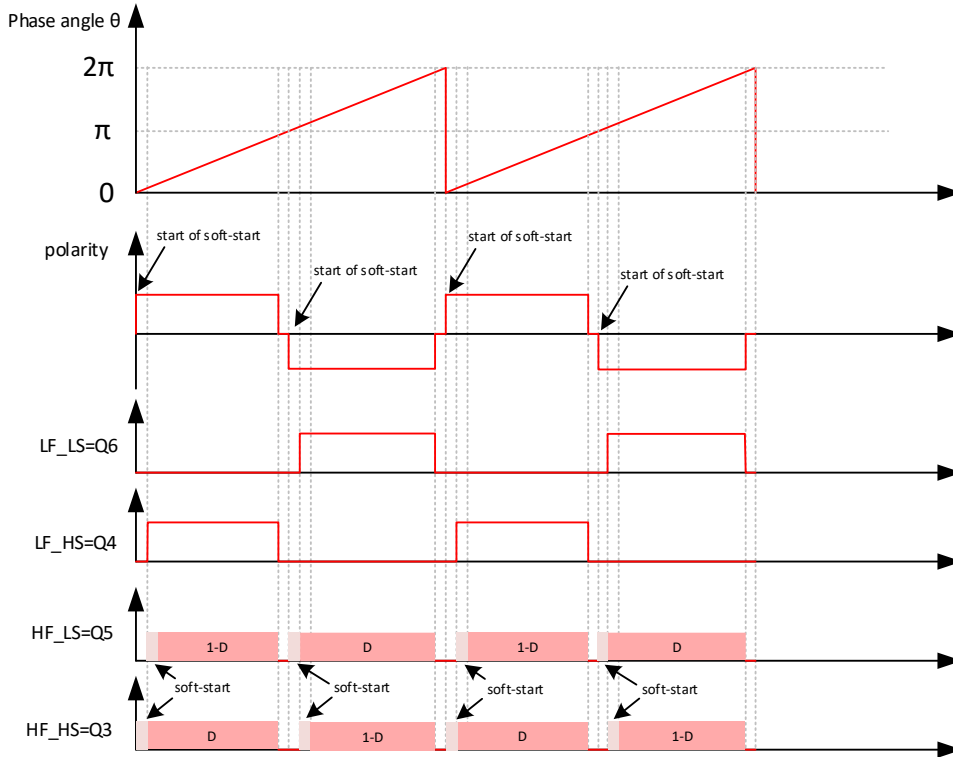

Figure 20: Soft start sequence at the AC zero crossing

Experiment results

Figure 21 shows the input current waveform at the AC zero-crossing with and without the soft start.

a) Without soft start at 233Vac rms, 400Vdc, 966W   b) With soft start at 233Vac rms, 400Vdc, 966W
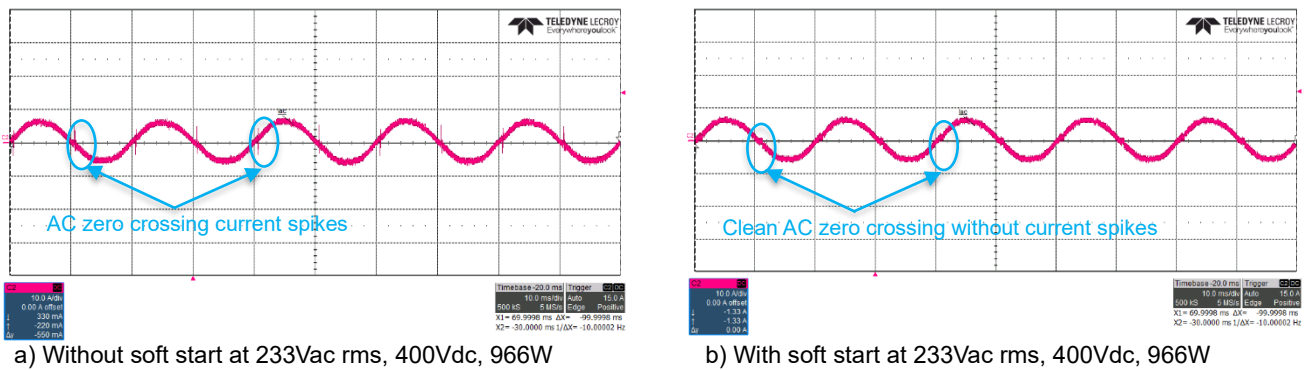
Figure 21: Input current spikes at AC zero crossing with and without soft start

The MOSFETs' control sequence explained in the previous section was implemented and tested on this EVK. With the PWM soft start at the AC zero crossing, the AC current waveform is much cleaner.

4.3. TP-PFC-EVK start-up: Inrush current mitigation

The TP-PFC EVK is equipped with a PTC resettable fuse which is connected in parallel with a bypass relay to mitigate the inrush current during the DC bus pre-charge time. At power-up, the relay is initially turned off and the bulk capacitors are pre-charged through the PTC. When the DC voltage exceeds the UVLO threshold, the bypass relay is turned on and shorts out the PTC. This prevents potential MOSFETs damage due to high inrush currents. The TP-PFC-EVK start-up was tested over the full universal input range [85Vac-265Vac].
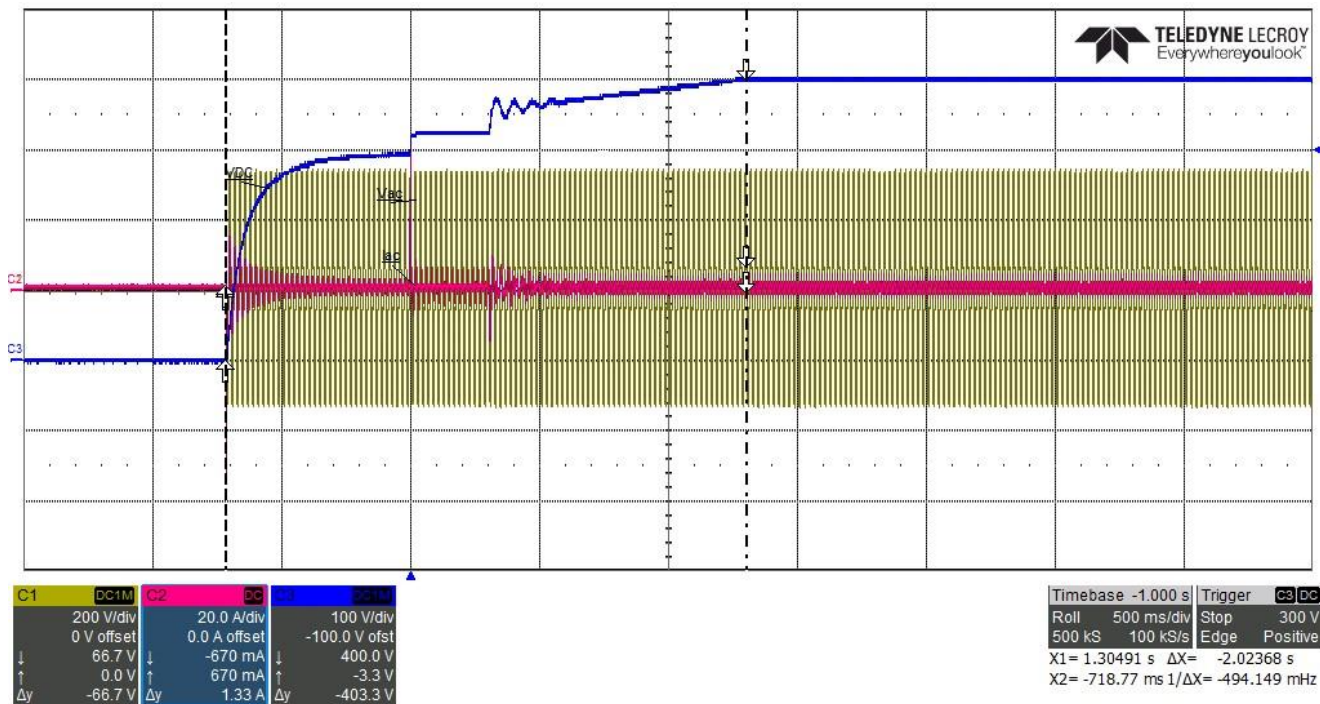

Figure 22: PFC start-up sequence at 235Vrms input AC voltage

4.4. FW state machine

The FW state machine of this 3.6 kW TP-PFC-EVK is depicted in figure 23. Where:

- ➢ **INIT**: During the INIT state, the FW is reading the ADC data, the PLL is locking its output data (grid's frequency, Omega, and phase) and the DC bus capacitors are precharged up to the Vac peak. In parallel with that, the Bluetooth communication is readily available for establishing a connection between the GUI and the microcontroller.

- ➢ **READY**: At the end of the INIT phase, when the DC bus is precharged and exceeds the UVLO threshold, the FW closes then AC relay to short-circuit the PTC resettable fuse and goes at the next AC zero crossing to the READY state. During the READY state, the FW either goes directly to the PRERUN state, if the "Automatic output enable" is selected by default or waits for the user to manually enable the output from the GUI. The FW will go back again to the READY state when the user manually disables the output from the GUI.

- ➢ **PRERUN**: During the PRERUN state, the FW waits an additional 330ms before ramping up the DC voltage to 400V.

- ➢ **RAMP_UP**: During this state, the PWMs are enabled, DC bus voltage is linearly ramped up to 400V.

- ➢ **RUN**: At the end of ramp-up time, the DC voltage is already at 400V, the FW goes to the RUN state where the converter can operate in its nominal conditions delivering power up to 3.6 kW.

- ➢ **FAULT**: After the INIT state, any detected fault will be reported in the GUI and will bring the FW to the FAULT state. The FW will transition again to the READY state when the fault cause is fixed, and the fault is cleared from the GUI.
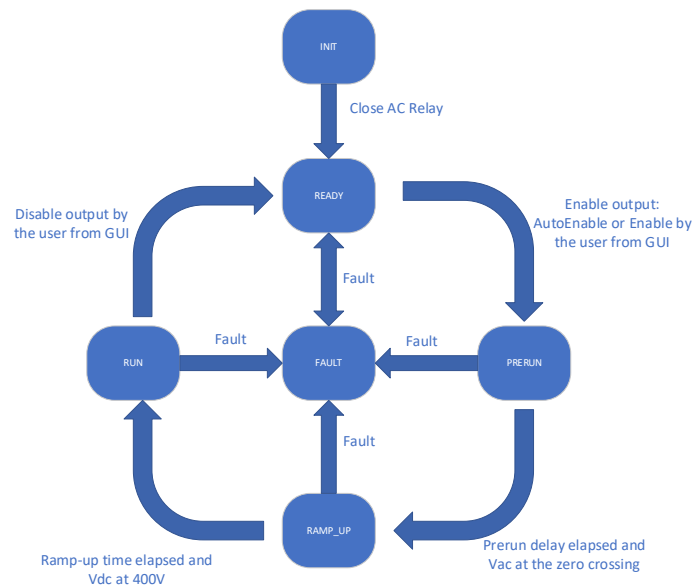

Figure 23 : TP-PFC-EVK FW state machine

5. Experimental results

5.1. Efficiency

The Totem Pole PFC efficiency test results are shown in figure 24. It's important to highlight that these results not only include the losses in the main power stage but also account for the losses occurring on the Aux PS daughter board. This auxiliary board supplies the essential power to the gate drivers, the cooling fan, and all other onboard power requirements.
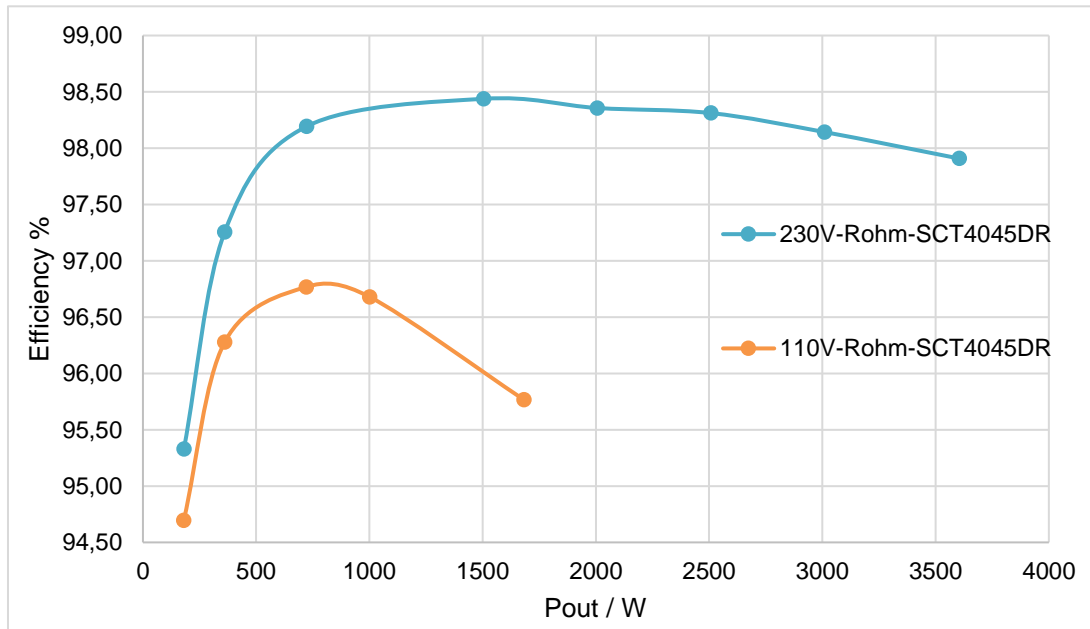

Figure 24:Efficiency measurement results including Aux PS, cooling fan, and all other onboard power consumption.
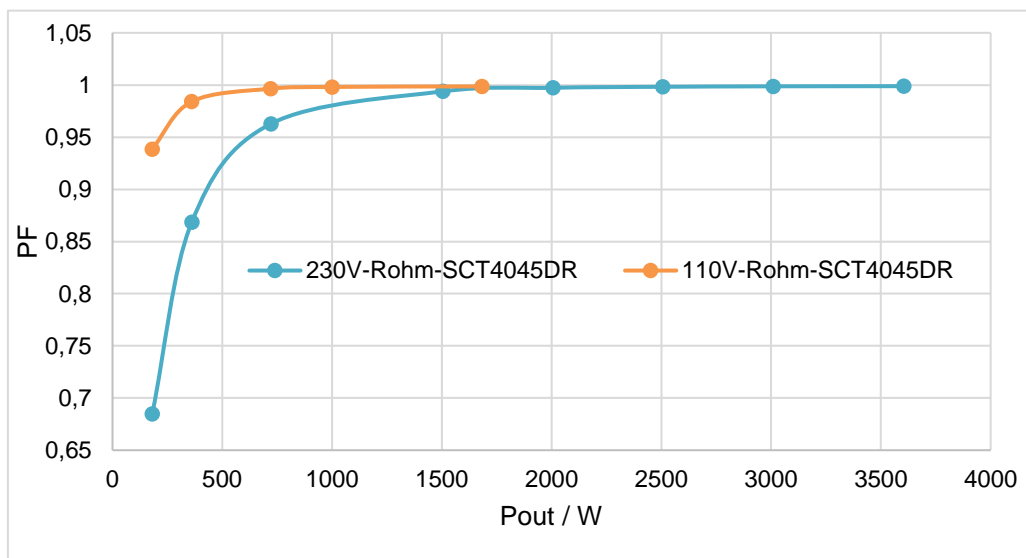
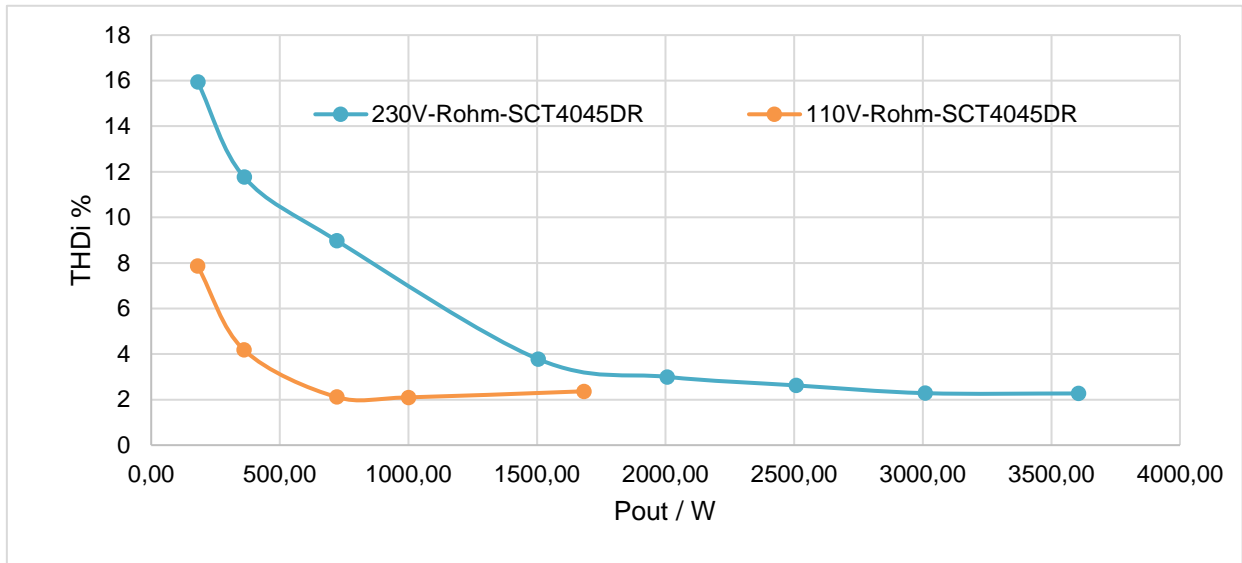## 5.2. Power factor

Figure 25: PF

5.3. THD

Figure 26: THD
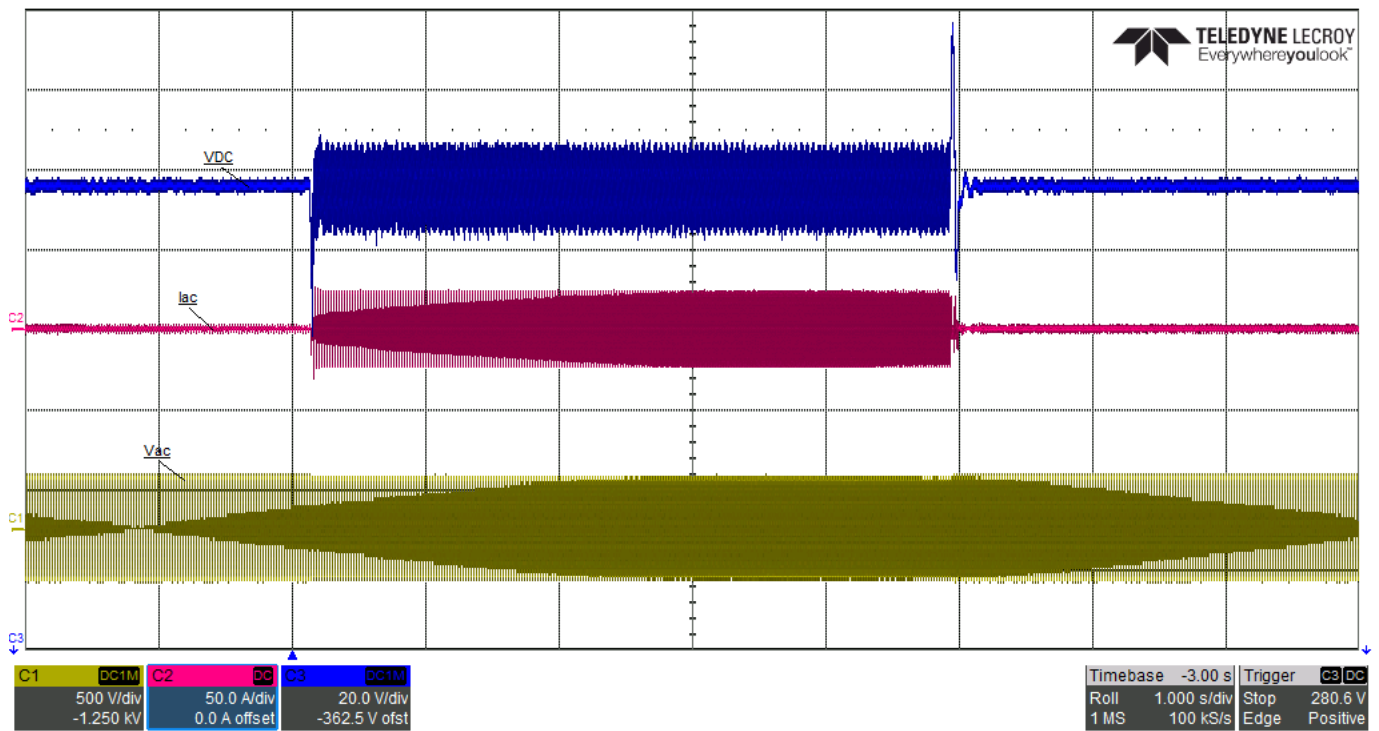
5.4. Load transients' response

Figure 27: Load transient response for a load step up and step down 160W ⬅➡ 3.6kW at input 230Vrms input AC voltage.

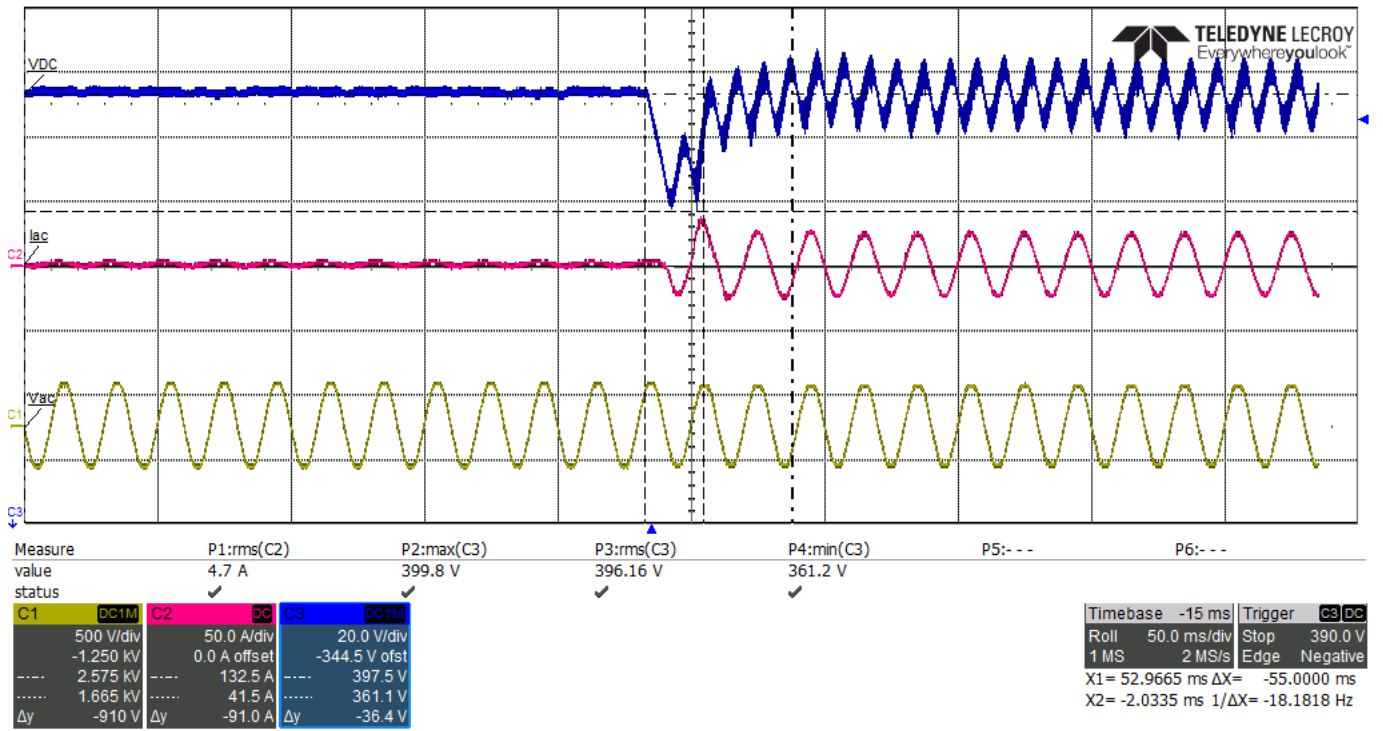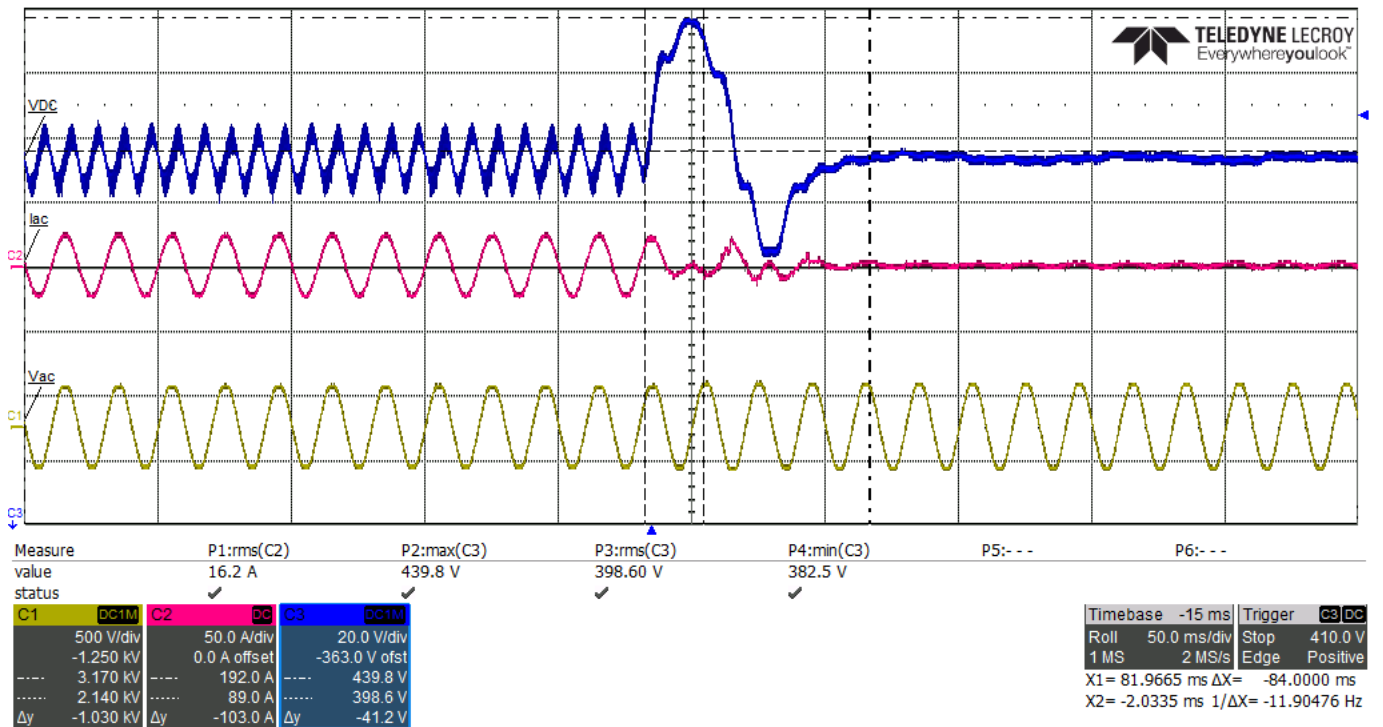Figure 28:Load transient response for a load step up 160W ➔ 3.6kW at input 230Vrms input AC voltage -zoomed-

Figure 29: Load transient response for a load step down 3.6kW ➔ 160W at 230Vrms input AC voltage -zoomed-
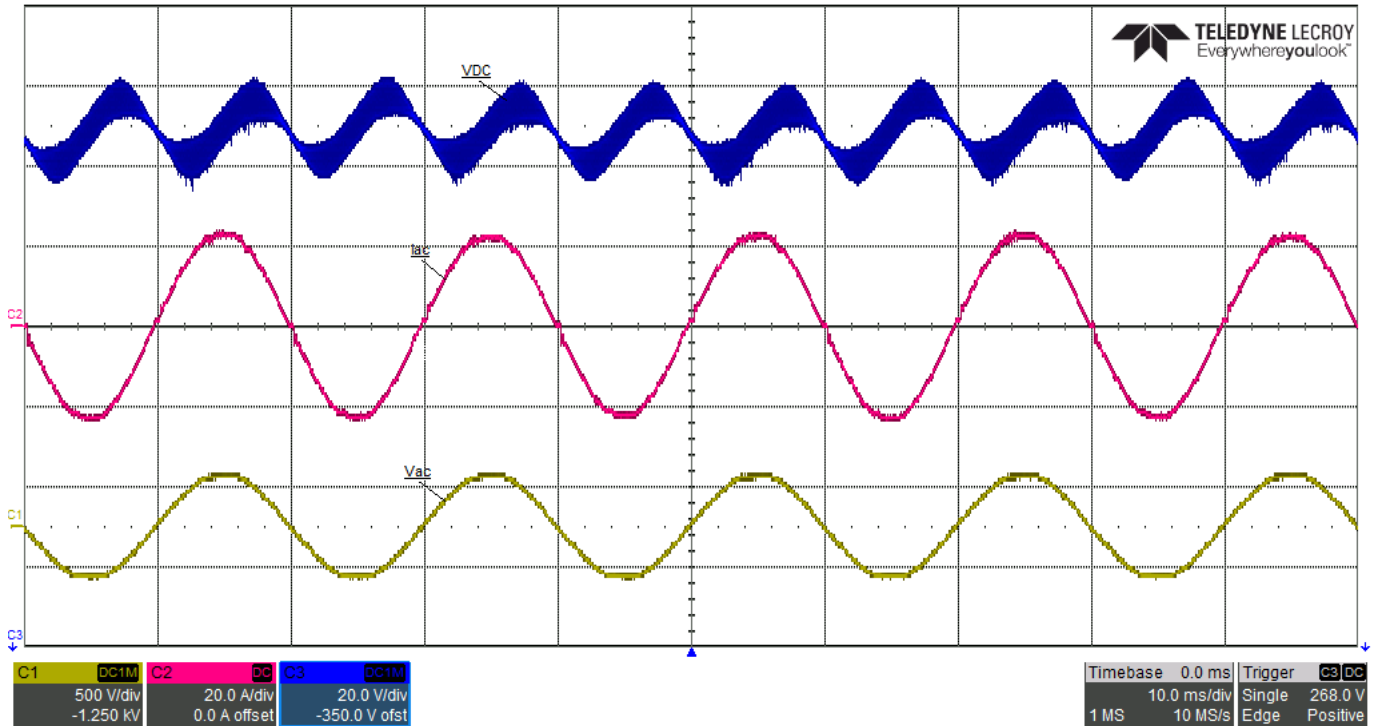
5.5. Steady state

Figure 30: PFC steady state at 230Vrms input AC voltage, 50 Hz and 3.6kW output power

5.6. DC bus discharge

As a safety precaution, during the power-down of the PFC, a rapid discharge of the DC bus voltage from 400V down to a safer voltage is automatically done. This discharge operation involves both the Aux PS board and an equivalent 1.02MΩ dummy load. This dummy load is specifically connected to the DC bus between the output connector terminals on the main PFC board. The discharge path is visually indicated in Figure 31 by the red dashed arrows when the load is completely disconnected.
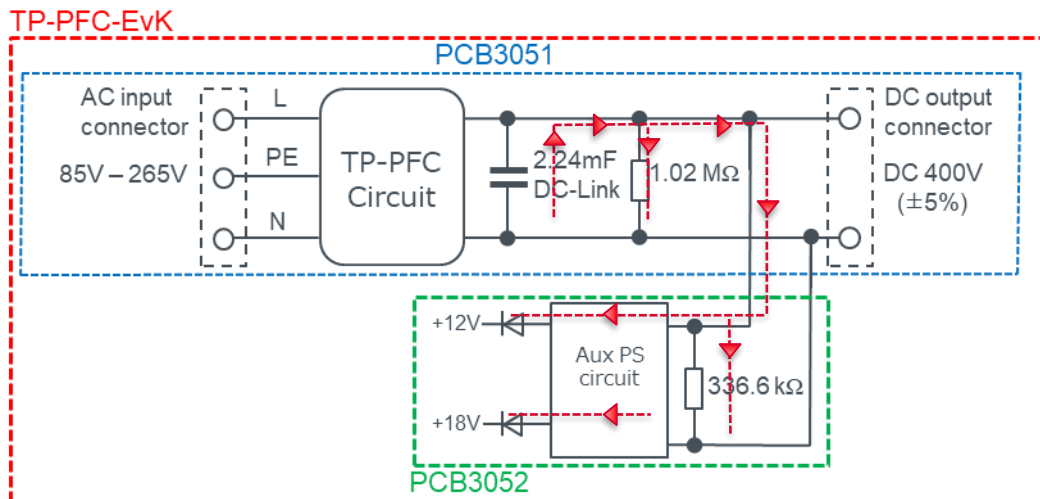
Figure 31: 400V DC bus discharge path on the TP-PFC-EVK

In this case, the DC voltage drops down to 10V in about 170 seconds (~3 minutes) as shown in the test results in figure 32.

Figure 32: DC bus discharge time from 400V to 10V with disconnected load

To achieve a faster discharge time, we suggest connecting a suitable 1 kΩ load to the DC output connector in parallel with the load utilized for the EVK evaluation. This configuration would result in the DC bus voltage rapidly declining from 400V to 0V within just 8 to 10 seconds.

Figure 33: Passive discharge time from 400V to 0V with a connected 1kΩ load

6. Totem Pole PFC protection features

6.1. Thermal shutdown

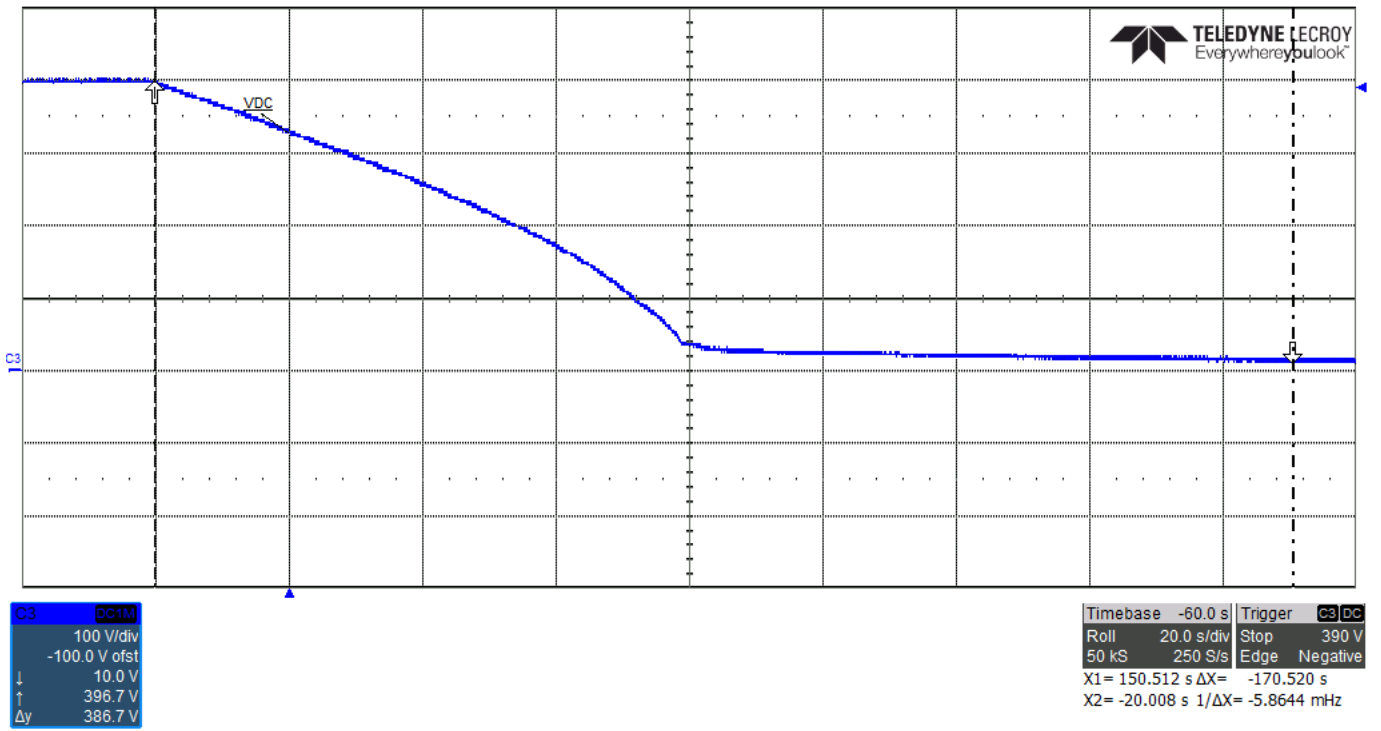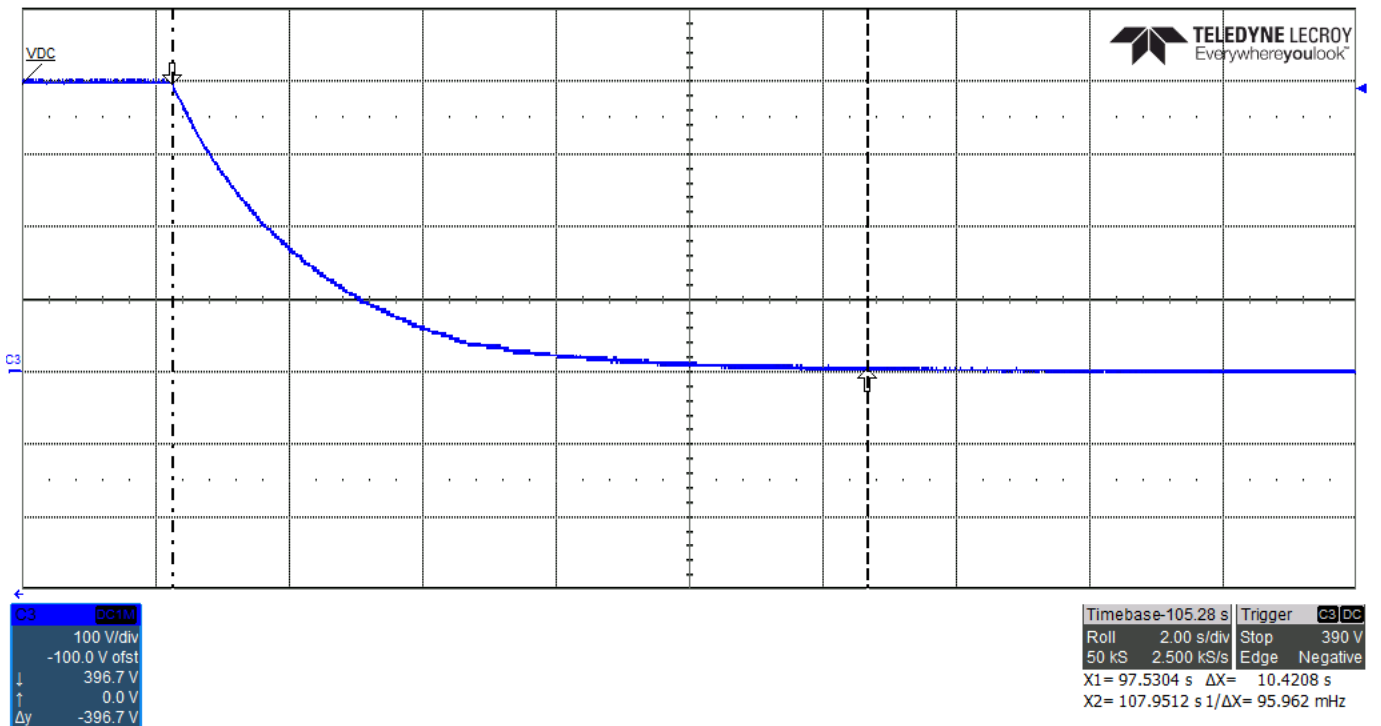As the PFC runs in steady state, the heatsink temperature increases. The MCU continuously reads this temperature to prevent MOSFETs damage due to excessive heat. The high temperature threshold is set to 92°C. This translates to a measured SiC MOSFET case temperature of ~122°C after 70~75 minutes of continuous operation at full power (3.6kW).

When this temperature limit is reached, the MCU first turns off the PWMs, the VDC drops to the rectified AC peak voltage. The PFC runs in passive rectification mode for a short time before an MCU command opens the AC relay as a second protection measure to protect the MOSFETs body diodes from large circulating current under heavy loads. To restart the board again, first turn off the AC power source, wait for the MOSFET's and the precharge PTC resettable fuse to cool down and then follow the start-up routine as described in the quick start guide [No. 66QS002E Rev.001] .
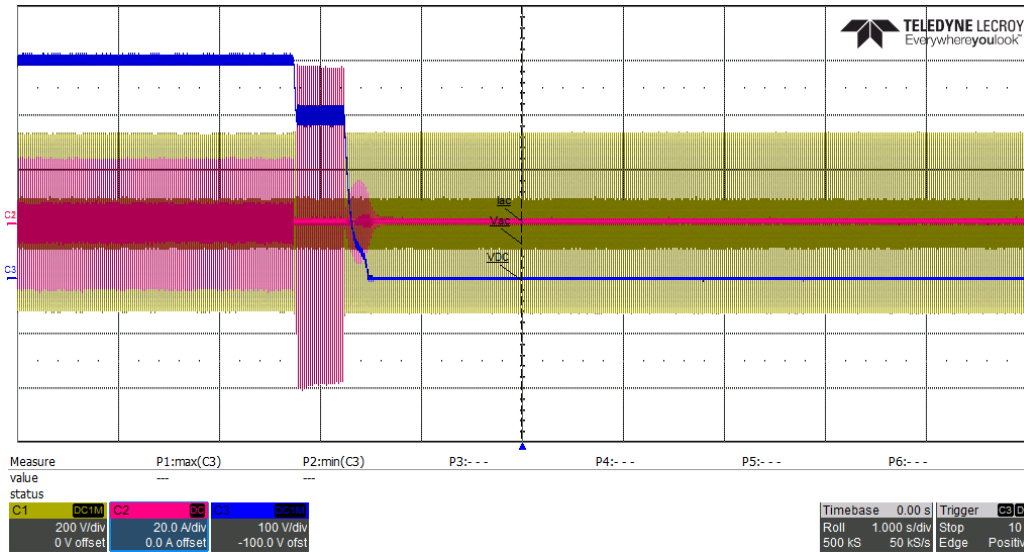

Figure 34: TPPFCSIC-EVK-301 thermal shutdown behavior

6.2. Output voltage UVL & OVP

The totem pole PFC EVK is designed to survive a full load dump from 100% output power to nearly zero Watt at high line. This means, the user should expect the voltage rise on the VDC during any load transient to be under the defined Over Voltage Protection (OVP) threshold which is set to 450V. Should the VDC rise over this limit for any other reason, the microcontroller will automatically shut down the PWMs for both fast leg and slow leg MOSFETs to protect the DC bus capacitors and other vulnerable parts of the circuit. Subsequently, the output will be disabled, the PFC will continue running in passive rectification mode and the OVP fault will be reported in the GUI.

Similarly, at high line, the EVK can survive a full load jump from nearly zero Watt to 100% output power **when the VDC is at its nominal voltage range**. In this case, the VDC undershoot will not hit the Under Voltage Lockout (UVL) threshold which is defined as the maximum between 93.5V and 110% of the AC input voltage RMS. If the VDC voltage drops below the UVL limit, the PFC controller will turn off the four MOSFETs. Subsequently, the output will be disabled, the PFC will continue running in passive rectification mode and the UVL fault will be reported in the GUI. This protection is implemented in the PFC side, but it would rather protect the downstream circuitry like a connected DC-DC stage.

6.3. Input AC current OCP

When the instantaneous input current is higher than 55A, which is set as the AC input peak current limit, the controller will report a fault and turn off the PWMs of the four switches. Setting the peak input current limit to 55A allows the PFC converter to operate normally under low line conditions while protecting the MOSFETs from high currents.

7.   Board schematic

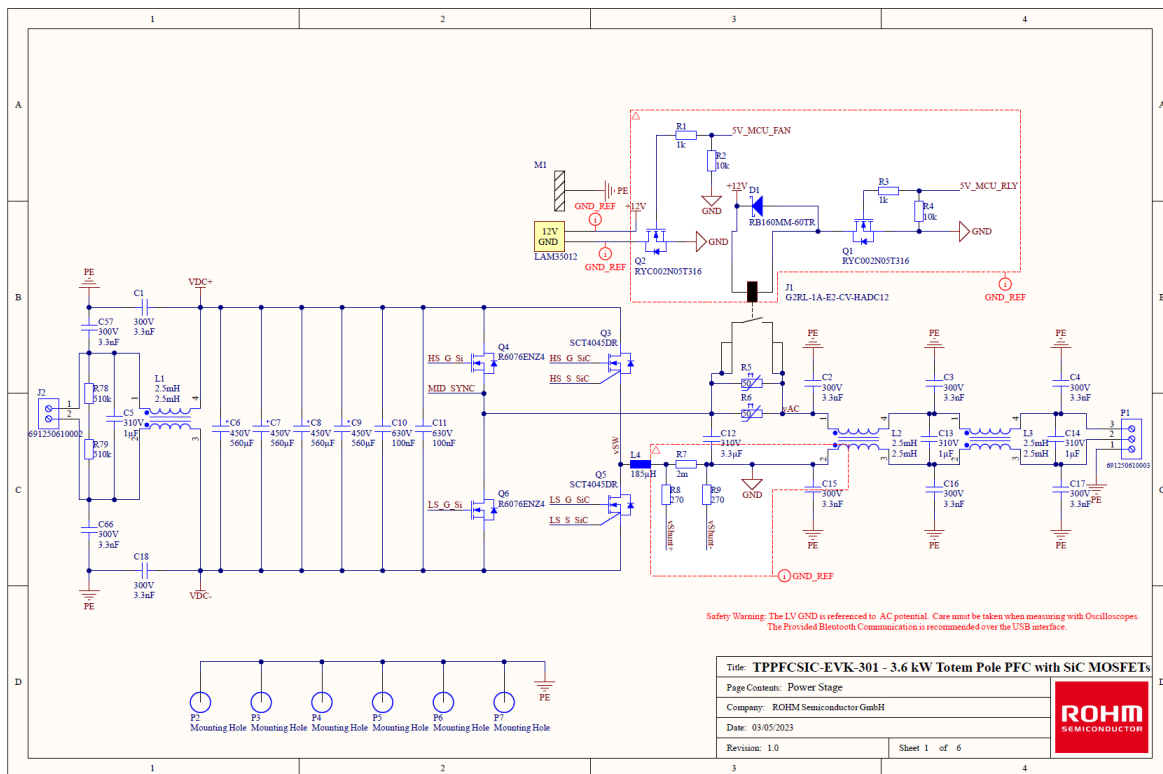## 7.1. PFC board schematic

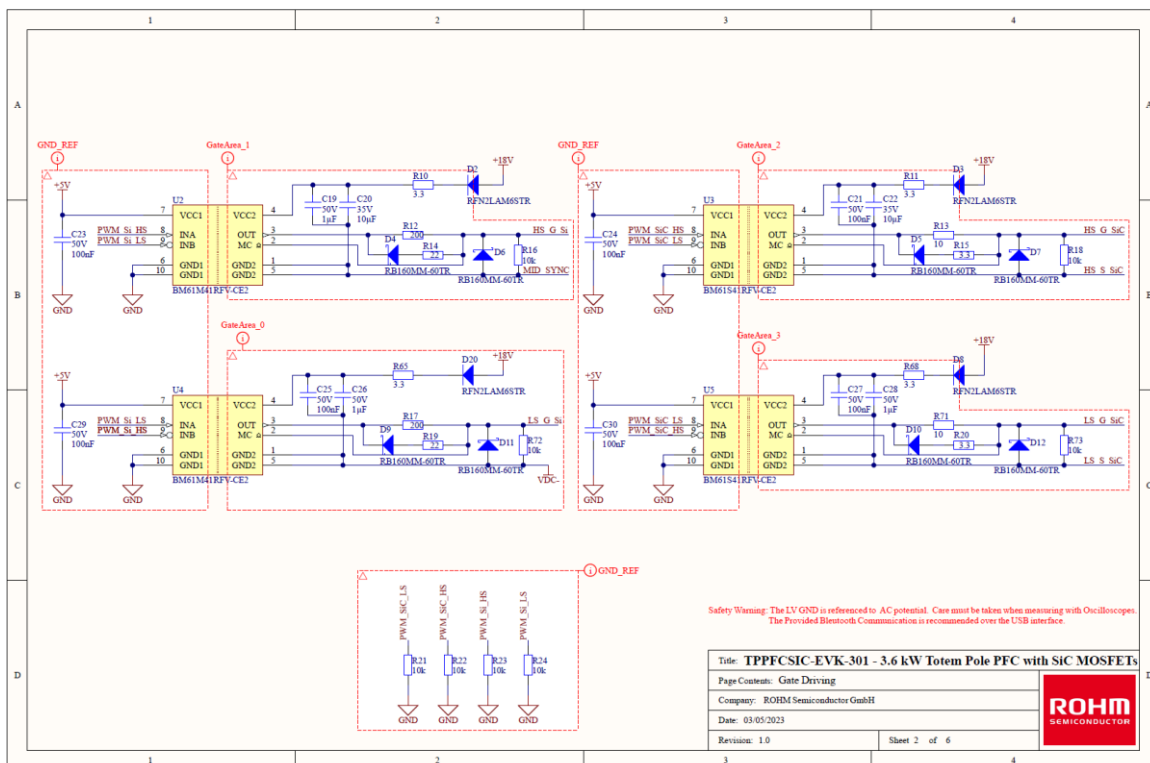Figure 35: PFC schematic (1 of 6)
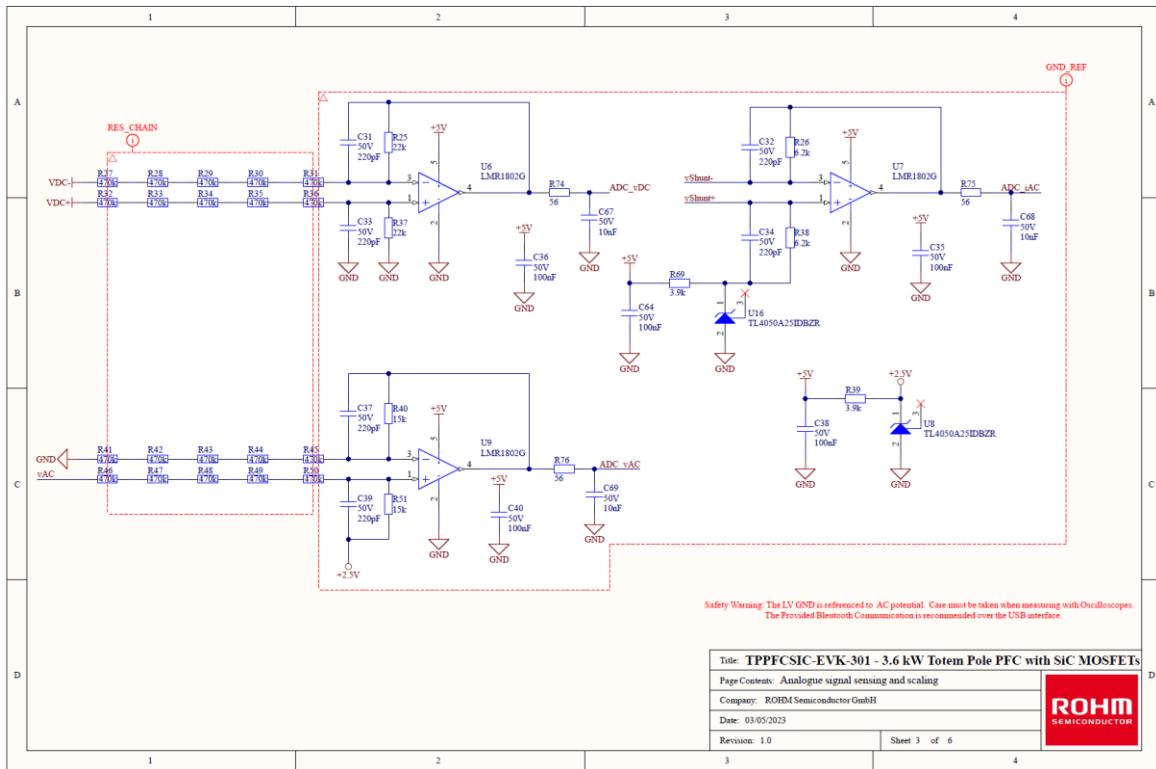

Figure 36: PFC schematic (2 of 6)
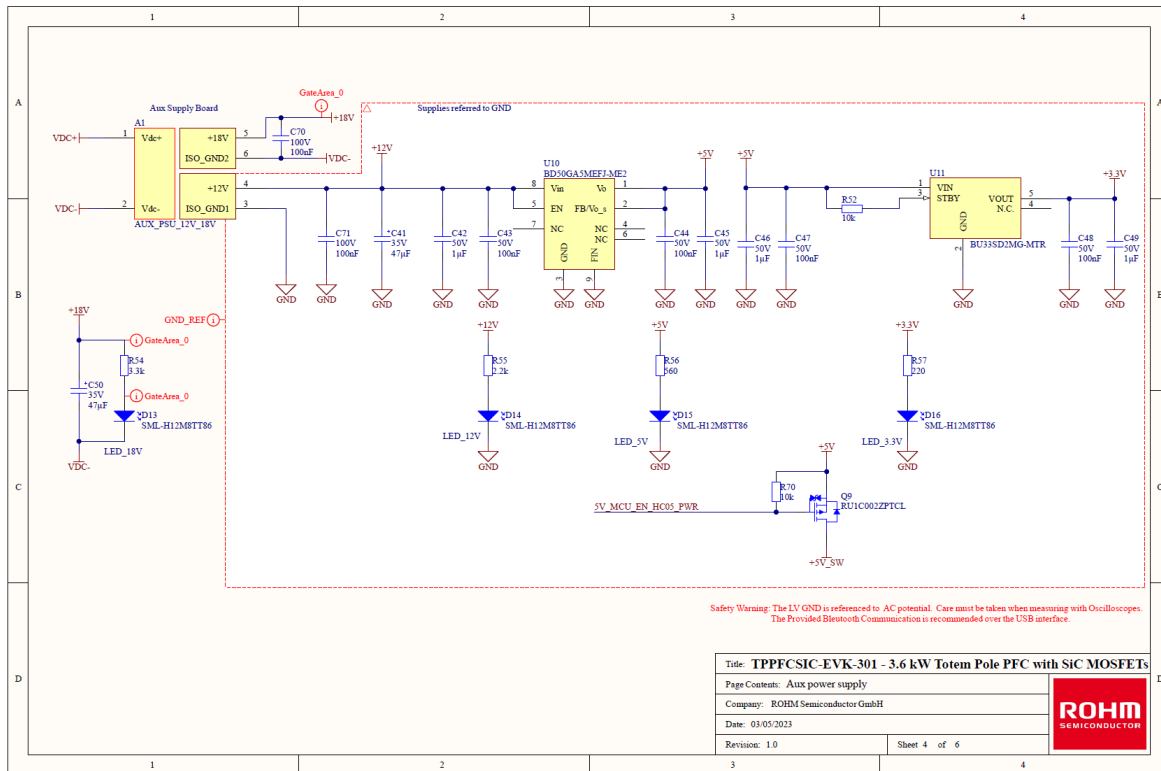
Figure 37: PFC schematic (3 of 6)

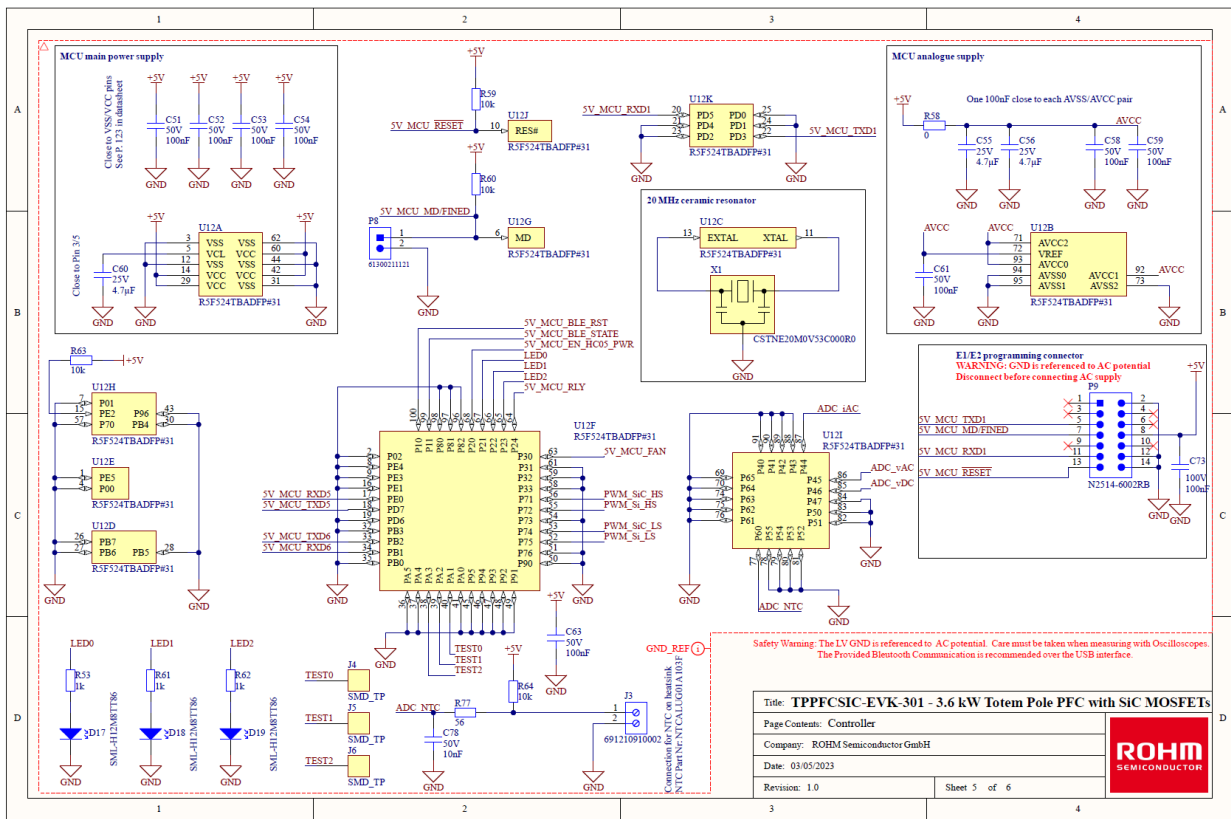Figure 38: PFC schematic (4 of 6)

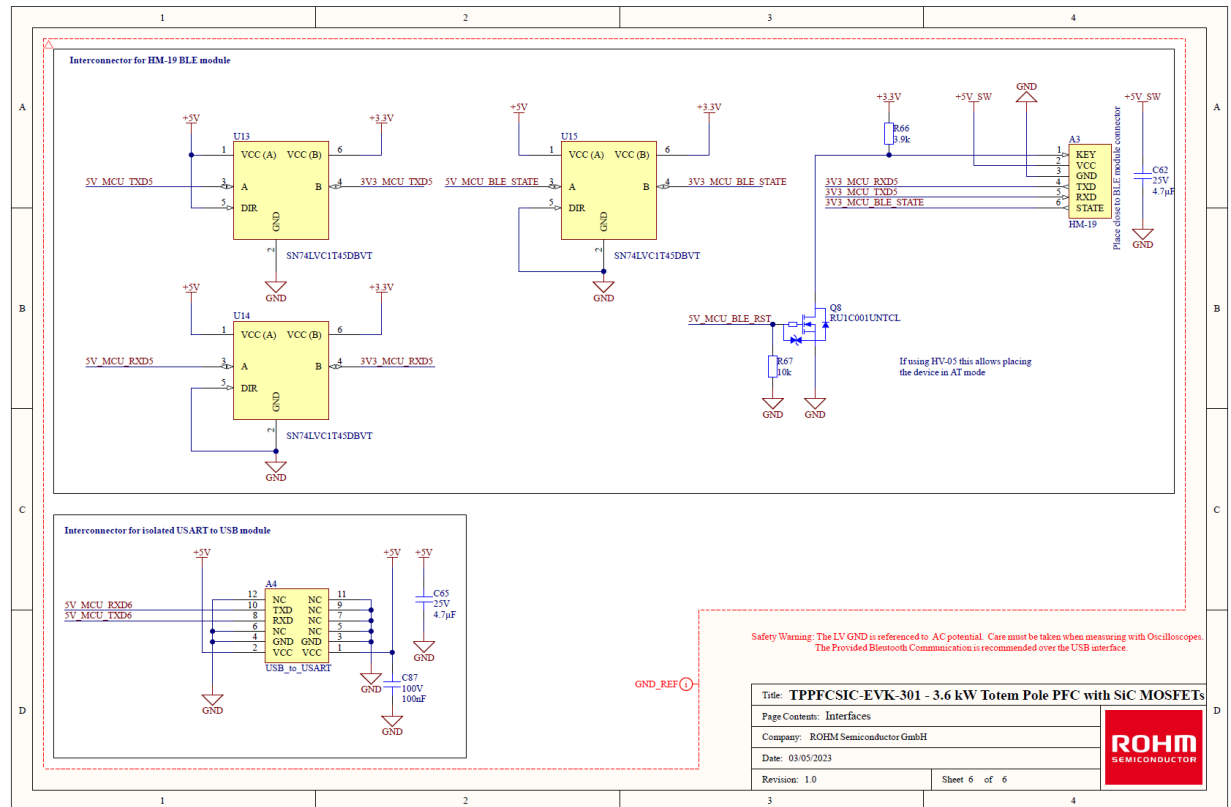Figure 39: PFC schematic (5 of 6)

Figure 40: PFC schematic (6 of 6)

7.2. Aux PS board schematic

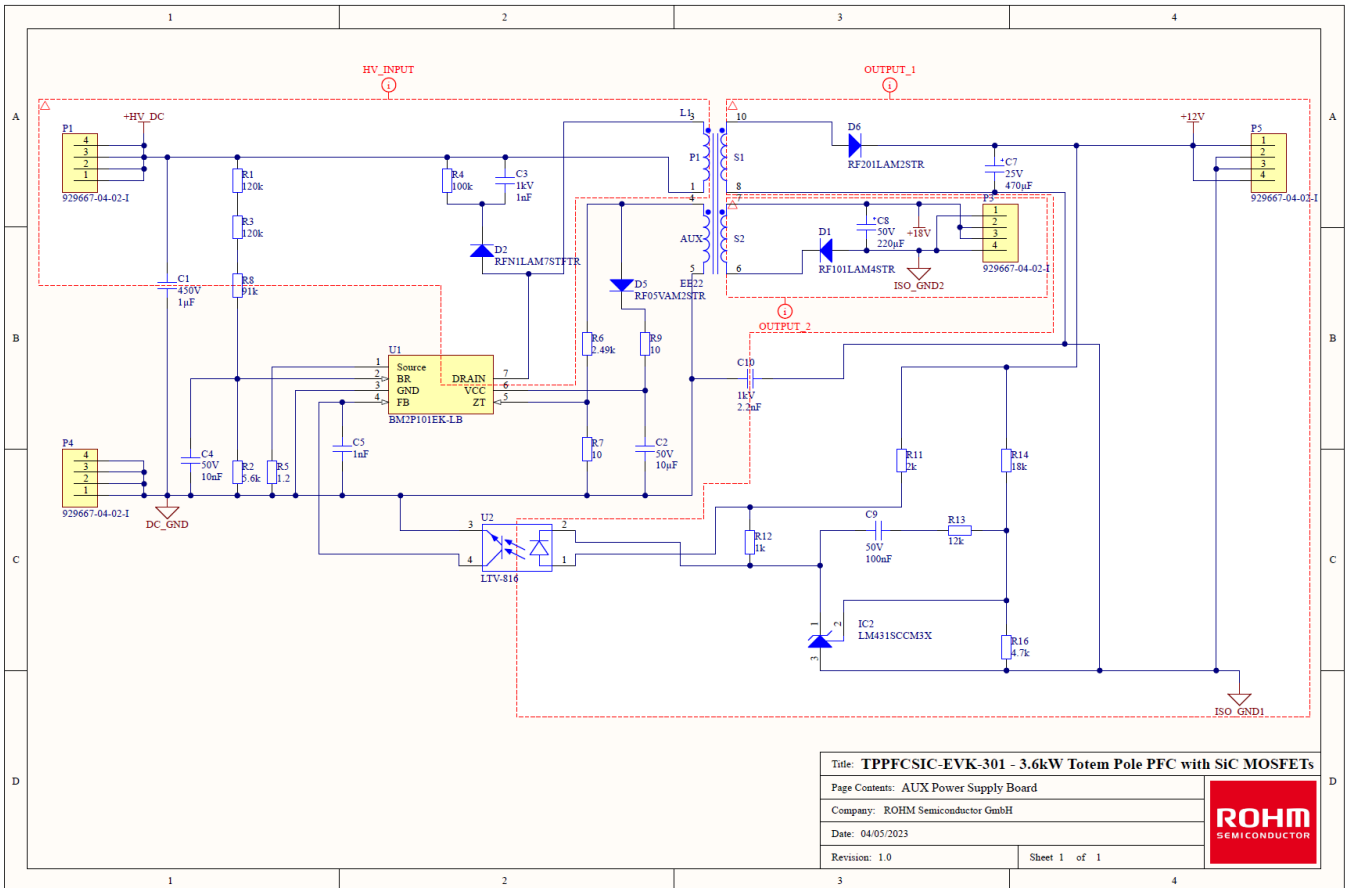Figure 41: Aux PS schematic

8. Bill of Materials

8.1. PFC BOM

Table 5 : PFC BoM

Ref.Desig-nator	Part Number	Manufacturer	Description	Quantity
A1	AUX_PSU_12V_18V	ROHM	Auxiliary Power Supply Daughter Board	1
A3	DSD -Tech HM-19	DSD -Tech	Bluetooth 5.0 Module	1
C1, C2, C3, C4, C15, C16, C17, C18, C57, C66	B32021A3332M000	EPCOS - TDK Electronics	Cap Film Suppression Y2 0.0033uF 300VAC PP 20% (13 X 4 X 9mm) Radial 10mm 110C Bulk	10
C5, C13, C14	890334026027	Würth Elektronik	Film Capacitor, Polypropyl-ene, 10% +Tol, 10% -Tol, 1uF, Through Hole Mount	3
C6, C7, C8, C9	B43647B5567M05#	EPCOS - TDK Electronics	CAP ALUM 560UF 20% 450V SNAP, 35×35mm	4
C10, C11	C2220C104KBRAC7800	KEMET	0.1 µF ±10% 630V Ceramic Capacitor X7R 2220	2
C12	890334027025	Würth Elektronik	CAP FILM 3.3UF 10% 310VAC RADIAL	1
C19, C26, C28, C42, C45, C46, C49	885012207103	Würth Elektronik	CAP CER 1UF 50V X7R 0805	7
C20, C22	CL31B106KLHNNNE	Samsung Electro-Mechanics	10 µF ±10% 35V Ceramic Capacitors X7R 1206	2
C21, C23, C24, C25, C27, C29, C30, C35, C36, C38, C40, C51, C52, C53, C54, C58, C59, C61, C63, C64	885012206095	Würth Elektronik	CAP CER 0.1UF 50V X7R 0603	20
C31, C32, C33, C34, C37, C39	885012006059	Würth Elektronik	CAP CER 220PF 50V C0G/NP0 0603	6
C41, C50	865060543005	Würth Elektronik	CAP ALUM 47UF 20% 35V SMD	2
C43, C44, C47, C48	885012207098	Würth Elektronik	CAP CER 0.1UF 50V X7R 0805	4
C55, C56, C60, C62, C65	885012107018	Würth Elektronik	CAP CER 4.7UF 25V X5R 0805	5
C67, C68, C69, C78	C1608X7R1H103K080AA	TDK Corporation	CAP CER 10000PF 50V X7R 0603	4
C70, C71, C73, C87	C0805C104K1REC7210	KEMET	CAP CER 0805 0.1UF 100V X7R	5
D1, D4, D5, D6, D7, D9, D10, D11, D12	RB160MM-60TR	Rohm Semiconductor	DIODE SCHOTTKY 60V 1A PMDU	9
D2, D3, D8, D20	RFN2LAM6STR	Rohm Semiconductor	DIODE GEN PURP 600V 1.5A PMDTM	4
D13, D14, D15, D16, D17, D18, D19	SML-H12M8TT86	Rohm Semiconductor	LED GREEN CLEAR 0805 SMD	7
J1	G2RL-1A-E2-CV-HADC12	Omron Electronics Inc-EMC Div	RELAY GEN PURPOSE SPST 23A 12V	1

J2	691250610002	Würth Elektronik	6.35 MM TERMINAL BLOCK, HORIZONT	1
J3	691210910002	Würth Elektronik	TERM BLOCK 2P HORIZON 2.54MM PCB	1
J4, J5, J6	5019	Keystone Electronics	PC TEST POINT MINIATURE	3
L1, L2, L3	7448052502	Würth Elektronik	CMC 2.5MH 25A 2LN TH	3
L4	750344728	Würth Elektronik	PFC Choke, 185µH, 26A, custom-made	1
M1	LAM35012	Fischer Elektronik	Universal rectangular aluminum heatsink, 1.3K/W, 50 x 30 x 30mm, PCB Mount	1
P1	691250610003	Würth Elektronik	6.35 MM TERMINAL BLOCK, HORIZONT	1
P8	61300211121	Würth Elektronik	CONN HEADER VERT 2POS 2.54MM	1
P9	N2514-6002RB	3M	CONN HEADER VERT 14POS 2.54MM	1
Q1, Q2	RYC002N05T316	Rohm Semiconductor	MOSFET N-CHANNEL 50V 200MA SST3	2
Q3, Q5	SCT4045DR	Rohm Semiconductor	SiC MOSFET, 750V, 45mOhm, TO-247-4L	2
Q4, Q6	R6076ENZ4	Rohm Semiconductor	MOSFET N-CH 600V 76A TO247	2
Q8	RU1C001UNTCL	Rohm Semiconductor	MOSFET N-CH 20V 100MA UMT3F	1
Q9	RU1C002ZPTCL	Rohm Semiconductor	MOSFET P-CH 20V 200MA UMT3F	1
R1, R3	ESR03EZPF1001	Rohm Semiconductor	RES Thick Film, 0.25W, 1000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	2
R2, R4, R16, R18, R21, R22, R23, R24, R52, R59, R60, R63, R67, R70, R72, R73	ESR03EZPF1002	Rohm Semiconductor	RES Thick Film, 0.25W, 10000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	16
R5, R6	B59751C0120A070	EPCOS - TDK Electronics	PTC RESET FUSE 440V 87MA RADIAL	2
R7	PMR18EZPFV2L00	Rohm Semiconductor	RES Thick Film, 0.002 ohm, PMR Series, 1206 [3216 Metric], 1 W, ± 1%	1
R8, R9	ESR03EZPF2700	Rohm Semiconductor	RES Thick Film, 0.25W, 270ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	2
R10, R11, R65, R68	ESR10EZPJ3R3	Rohm Semiconductor	RES Thick Film, 0.4W, 3.3ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0805	4
R12, R17	ESR10EZPF2000	Rohm Semiconductor	RES Thick Film, 0.4W, 200ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	2
R13, R71	ESR18EZPF10R0	Rohm Semiconductor	RES Thick Film, 0.5W, 10ohm, 200V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 1206	2
R14, R19	ESR10EZPF22R0	Rohm Semiconductor	RES Thick Film, 0.4W, 22ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	2
R15, R20	ESR18EZPF3R30	Rohm Semiconductor	RES Thick Film, 0.5W, 3.3ohm, 200V, 1% +/-Tol,	2

			100ppm/Cel, Surface Mount, 1206	
R25, R37	ESR03EZPF2202	Rohm Semiconductor	RES Thick Film, 0.25W, 22000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	2
R26, R38	ESR03EZPF6201	Rohm Semiconductor	RES Thick Film, 0.25W, 6200ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	2
R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50	ESR18EZPF4703	Rohm Semiconductor	RES Thick Film, 0.5W, 470000ohm, 200V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 1206	20
R39, R69	ESR03EZPF3901	Rohm Semiconductor	RES Thick Film, 0.25W, 3900ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	2
R40, R51	ESR03EZPF1502	Rohm Semiconductor	RES Thick Film, 0.25W, 15000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	2
R53, R61, R62	ESR10EZPF1001	Rohm Semiconductor	RES Thick Film, 0.4W, 1000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	3
R54	ESR18EZPF3301	Rohm Semiconductor	RES Thick Film, 0.5W, 3300ohm, 200V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 1206	1
R55	ESR10EZPJ222	Rohm Semiconductor	RES Thick Film, 0.4W, 2200ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0805	1
R56	ESR10EZPJ561	Rohm Semiconductor	RES Thick Film, 0.4W, 560ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0805	1
R57	ESR10EZPJ221	Rohm Semiconductor	RES Thick Film, 0.4W, 220ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0805	1
R58	SFR03EZPJ000	Rohm Semiconductor	Fixed Resistor, 0.1W, 0ohm, Surface Mount, 0603	1
R64	ESR10EZPF1002	Rohm Semiconductor	RES Thick Film, 0.4W, 10000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	1
R66	ESR03EZPJ392	Rohm Semiconductor	RES Thick Film, 0.25W, 3900ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0603	1
R74, R75, R76, R77	ESR03EZPF56R0	Rohm Semiconductor	RES Thick Film, 0.25W, 56ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	4
R78, R79	KTR18EZPF5103	Rohm Semiconductor	Fixed Resistor, 0.25W, 510000ohm, 500V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 1206	2

U2, U4	BM61M41RFV-CE2	Rohm Semiconductor	Single channel Isolated Gate driver with active Miller clamp	2
U3, U5	BM61S41RFV-CE2	Rohm Semiconductor	Single channel Isolated Gate driver with active Miller clamp	2
U6, U7, U9	LMR1802G	Rohm Semiconductor	Low Noise Low Input Offset Rail-to-Rail OpAmp	3
U8, U16	TL4050A25IDBZR	Texas Instruments	Shunt Voltage Reference IC Fixed 2.5V V ±0.1% 15 mA SOT-23-3	2
U10	BD50GA5MEFJ-ME2	Rohm Semiconductor	IC REG LINEAR 5V 500MA 8HTSOP	1
U11	BU33SD2MG-MTR	Rohm Semiconductor	IC REG LINEAR 3.3V 200MA 5SSOP	1
U12	R5F524TBADFP#31	Renesas Electronics America Inc	IC MCU 32BIT 256KB FLSH 100LFQFP	1
U13, U14, U15	SN74LVC1T45DBVT	Texas Instruments	Voltage level converter bidirectional 1 circuit 1 channel 420MBit/s SOT-23-6	3
X1	CSTNE20M0V53C000R0	Murata Electronics	CERAMIC RES 20.0000MHZ 15PF SMD	1
-	keratherm 86/60	Kerafol	Kerafol 86/60 heat conducting foil 0.25 mm 4.5 W/mK (L x W) 100 mm x 100 mm	1
-	NTCALUG01A103F800A	VISHAY	NTC LUG01A 10K 1% G24 80MM A	1

8.2. Aux PS BOM

Table 6 : Aux PS BoM

Designator	Part Number	Manufacturer	Description	Quantity
C1	ECW-F2W105JA	Panasonic Electronic Components	CAP FILM 1UF 5% 450VDC RADIAL	1
C2	UMJ325KB7106KMHP	Taiyo Yuden	CAP CER 10UF 50V X7R 1210	1
C3	885342208018	Würth Elektronik	WCAP-CSMH MID AND HIGH VOLTAGE M	1
C4	885012207092	Würth Elektronik	CAP CER 10000PF 50V X7R 0805	1
C5	885012007063	Würth Elektronik	CAP CER 1000PF 50V C0G/NP0 0805	1
C7	860160475022	Würth Elektronik	CAP ALUM 470UF 20% 25V RADIAL	1
C8	860020675020	Würth Elektronik	CAP ALUM 220UF 20% 50V RADIAL	1
C9	885012206095	Würth Elektronik	CAP CER 0.1UF 50V X7R 0603	1
C10	DE1E3KX222MB4BP01F	Murata Electronics	CAP CER 2200PF 300VAC RADIAL	1
D1	RF101LAM4STR	Rohm Semiconductor	DIODE GEN PURP 400V 1A PMDTM	1
D2	RFN1LAM7STFTR	Rohm Semiconductor	DIODE GEN PURP 700V 800MA PMDTM	1
D5	RF05VAM2STR	Rohm Semiconductor	DIODE GEN PURP 200V 500MA TUMD2S	1
D6	RF201LAM2STR	Rohm Semiconductor	DIODE GEN PURP 200V 2A PMDTM	1
IC2	LM431SCCM3X	Onsemi	V-Ref Adjustable 2.495V to 36V 100mA 3-Pin SOT-23 T/R	1
L1	750319172	Würth Elektronik	Transformer EE22 -Custom-Made	1
P1, P3, P4, P5	929667-04-02-I	3M	CONN HEADER R/A 4POS 2.54MM	4

R1, R3	ESR10EZPF1203	Rohm Semiconductor	RES Thick Film, 0.4W, 120000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	2
R2	ESR10EZPJ562	Rohm Semiconductor	RES Thick Film, 0.4W, 5600ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0805	1
R4	HV733ATTE1003F	KOA Speer Electronics, Inc.	Res Thick Film 2512 100K Ohm 1% 1W ±100ppm/C Pad SMD T/R	1
R5	ERJ1TRQF1R2U	Panasonic Electronic Components	RES Thick Film, 1W, 1.2ohm, 1.0954V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 2512	1
R6	RCS08052K49FKEA	Vishay Dale	RES SMD 2.49K OHM 1% 1/2W 0805	1
R7	ESR03EZPF10R0	Rohm Semiconductor	RES Thick Film, 0.25W, 10ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	1
R8	ESR10EZPF9102	Rohm Semiconductor	RES Thick Film, 0.4W, 91000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	1
R9	ESR10EZPF10R0	Rohm Semiconductor	RES Thick Film, 0.4W, 10ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	1
R11	ESR03EZPJ202	Rohm Semiconductor	RES Thick Film, 0.25W, 2000ohm, 150V, 5% +/-Tol, 200ppm/Cel, Surface Mount, 0603	1
R12	ESR10EZPF1001	Rohm Semiconductor	RES Thick Film, 0.4W, 1000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0805	1
R13	ESR03EZPF1202	Rohm Semiconductor	RES Thick Film, 0.25W, 12000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	1
R14	ESR03EZPF1802	Rohm Semiconductor	RES Thick Film, 0.25W, 18000ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	1
R16	ESR03EZPF4701	Rohm Semiconductor	RES Thick Film, 0.25W, 4700ohm, 150V, 1% +/-Tol, 100ppm/Cel, Surface Mount, 0603	1
U1	BM2P101EK-LB	Rohm Semiconductor	AC/DC converter DIP 7-PIN	1
U2	LTV-816	Lite-On	Optocoupler DC-IN 1-CH Transistor DC-OUT 4-Pin PDIP	1

9. Layout and assembly drawing

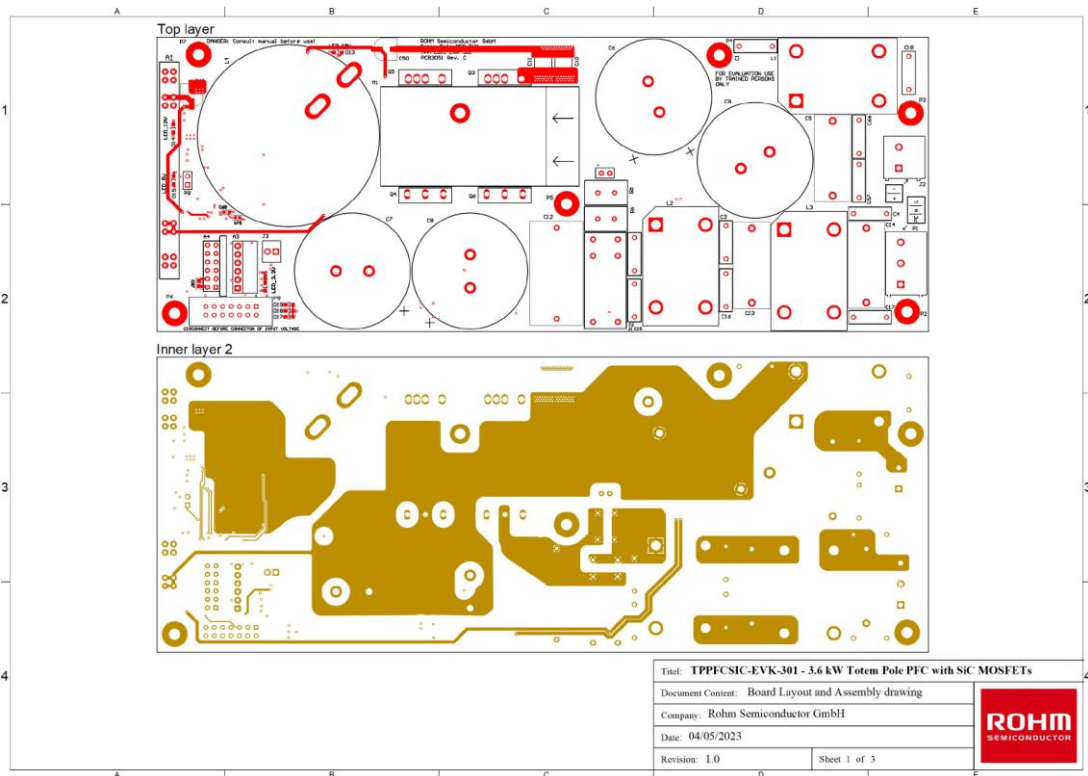## 9.1. PFC layout and assembly drawing

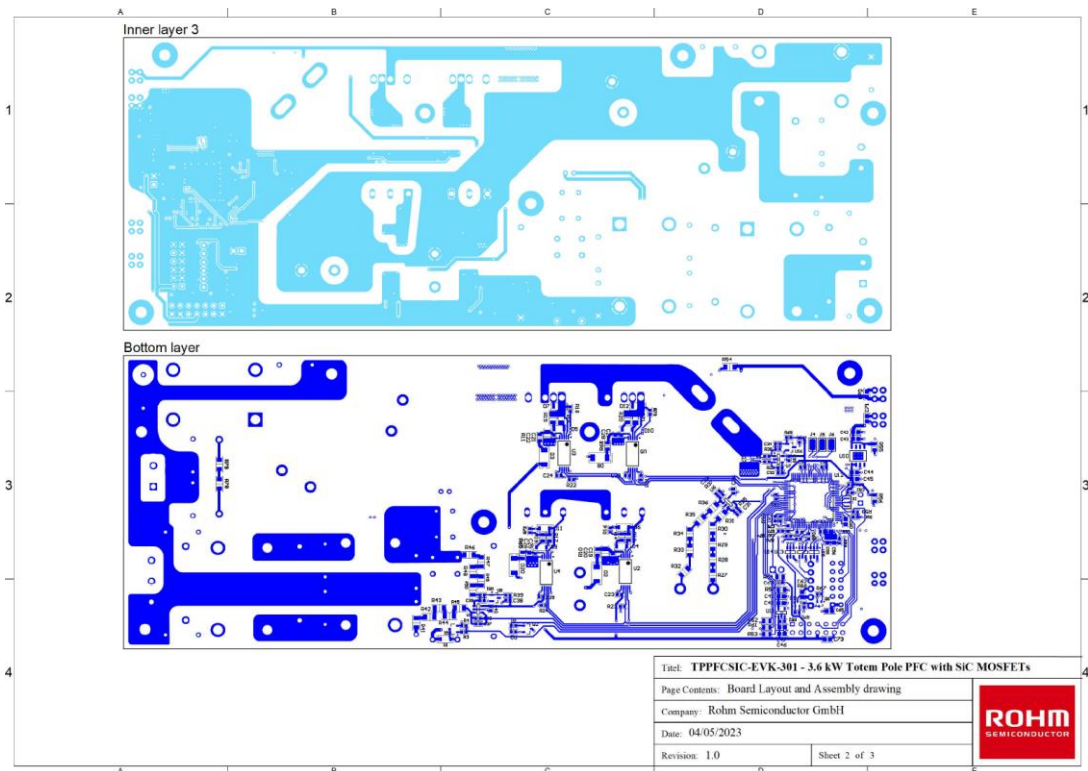Figure 42: PFC board layout and assembly drawing (1 of 3)

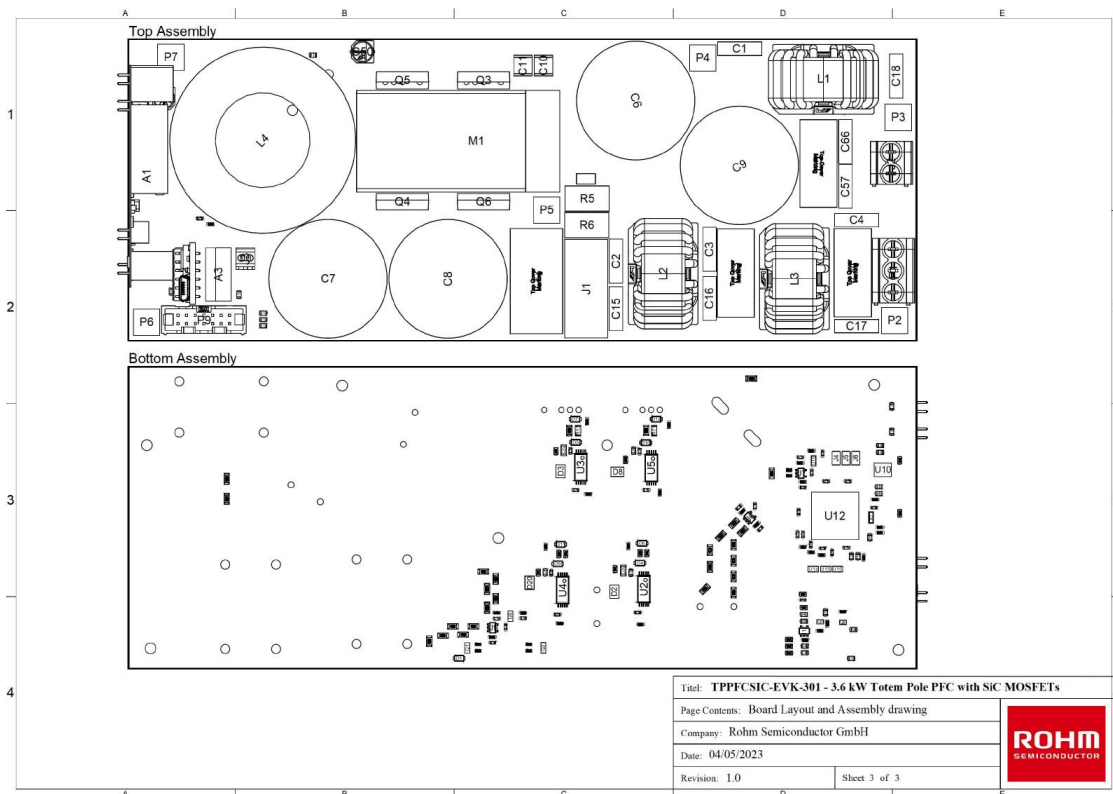Figure 43: PFC board layout and assembly drawing (2 of 3)

Figure 44: PFC board layout and assembly drawing (3 of 3)

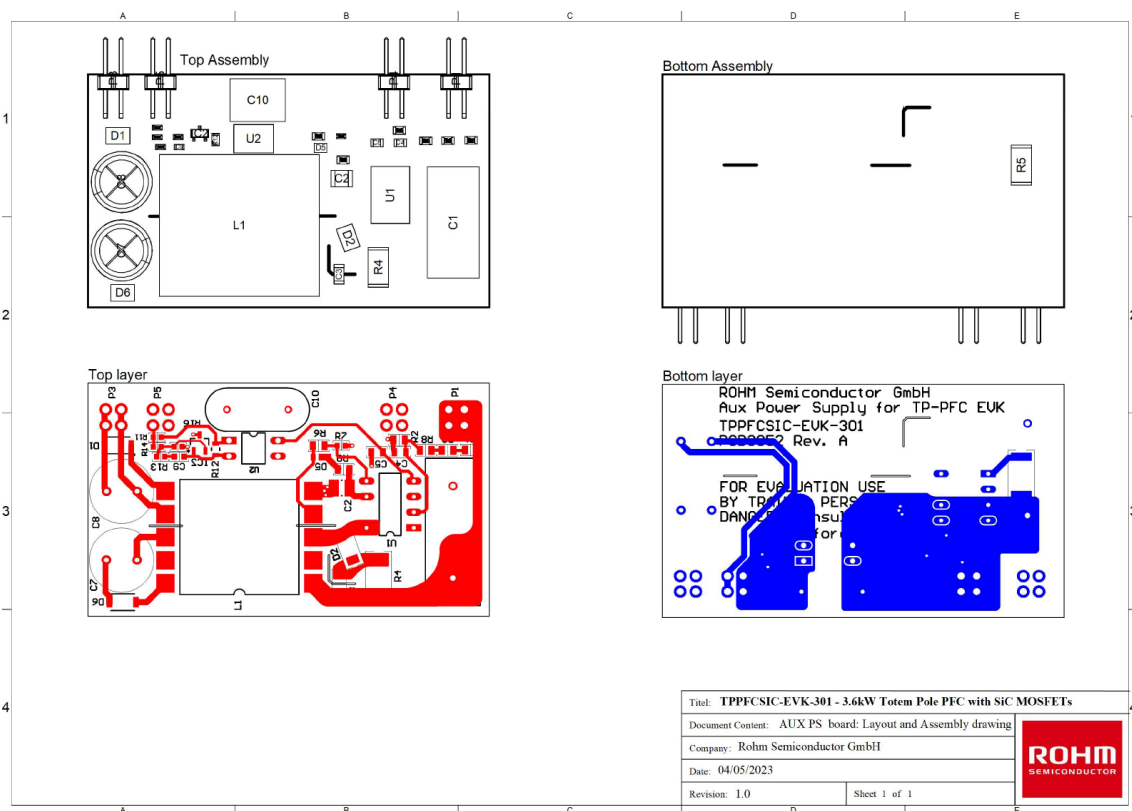## 9.2. Aux PS layout and assembly drawing

Figure 45: Aux PS board layout and assembly drawing

References:

[1] Abdelmouneim Charkaoui, Christian Felgemacher, Felipe Filsecker and Jochen Hüskens "4th Generation SiC MOSFET in Totem Pole PFC for High-Performance SMPS", Bodo's Power Systems, October 2022.

[2] Bosheng Sun, Analog Application Journal "How to reduce current spikes at AC zero-crossing for totem-pole PFC" Bosheng Sun, https://www.ti.com/lit/an/slyt650

[3] Magnetics, Inc "Inductor Cores: Material and Shape Choices": https://www.mag-inc.com/Design/Design-Guides/Inductor-Cores-Material-and-Shape-Choices

Revision History

Table 7 : Revision history

Revision	Date	Description of change
Rev.001	September 2023	Initial version

N o t e s

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