Automotive Power Management IC

BD86852MUF-C
PMIC for Automotive Camera

Introduction

This user's guide will provide the necessary steps to operate the ROHM's BD86852MUF-C. This includes the external parts, operating procedures and application data.

Description

BD86852MUF-C is a power management IC with primary buck converter (DC/DC1), secondary buck converters (DC/DC2 and DC/DC3), external linear regulator control block and the power-on reset function for CMOS sensor and image sensing power supply. Output voltage and sequence are selectable and applicable to various image sensor power supply. This device adopts small package VQFN24FV4040 which is optimal for camera module. In addition, this device has a pin that can be programmed to turn on/off the spread spectrum providing a lower noise regulated outputs.

Application

ADAS, Camera System (Automotive Camera and Security Camera) using CMOS Sensor

Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Conditions
VCC, PVCC(Note 1)	4.0 (Note 2)	6	18.0	V	-
VS2, VS3(Note 1)	3.2	-	4.0	V	VS2 and VS3 must be short to VO1
VO1 Output Current(Note 1)	-	-	2	A	-
VO2 Output Current(Note 1)	-	-	1	A	-
VO3 Output Current(Note 1)	-	-	1	A	-
VO1(3.3V) Maximum Efficiency	-	90.8	-	%	VCC = 5.0V, Io = 0.3A, Ta = 25°C
VO1(3.9V) Maximum Efficiency	-	92.1	-	%	VCC = 5.0V, Io = 0.3A, Ta = 25°C
VO2(1.2V) Maximum Efficiency	-	86.3	-	%	VS2 = 3.3V, Io = 0.32A, Ta = 25°C
VO2(1.1V) Maximum Efficiency	-	85.3	-	%	VS2 = 3.3V, Io = 0.32A, Ta = 25°C
VO3(1.8V) Maximum Efficiency	-	90.3	-	%	VS3 = 3.3V, Io = 0.32A, Ta = 25°C
FOSC1 (Note3)	2.0	2.2	2.4	MHz	RRT = 27kΩ, SSCG = GND short
FOSC2 (Note3)	1.8	2.1	FOSC1	MHz	RRT = 27kΩ, CSSC = 3300pF

(Note 1) Do not exceed the maximum junction temperature rating.

(Note 2) If differences between Power Supply Voltage of VCC and VO1 Output Voltage are small, VO1 Output Voltage may drop.

(Note 3) If the spread spectrum feature is not used, the SSCG pin must be shorted to GND. In this case, the internal DCDC converter1,2,3 switching frequency is FOSC1. If the spread spectrum feature is used, please connect a capacitor (CSSC) to SSCG pin. In this case, the internal DCDC converter1,2,3 switching frequency is FOSC2.

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Evaluation Board

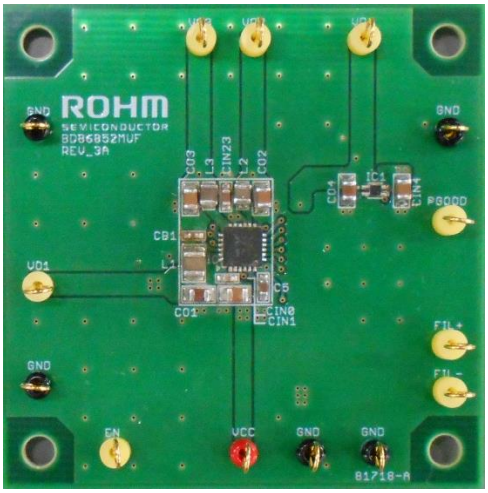

Figure 1. Evaluation Board Top View

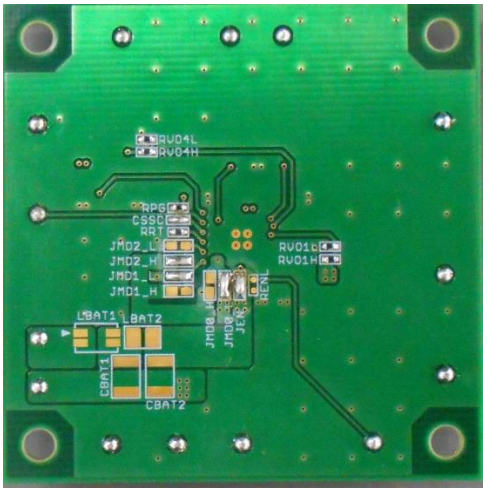

Figure 2. Evaluation Board Bottom View

Table 2. Main Parts Functional Description

Item	Note	Item	Note
IC1	External LDO	CSSC	Setting to spread spectrum ratio
RRT	Setting to switching frequency resistor	CIN1	VO1 input capacitor
RPG	PGOOD pull-up resistor	CO1	VO1 output capacitor
L1	VO1 output Inductor	CB1	VO1 boot strap capacitor
L2	VO2 output Inductor	CIN23	VO2 and VO3 input (VO1 output) capacitor
L3	VO3 output Inductor	CO2	VO2 output capacitor
CIN0	VCC input capacitor	CO3	VO3 output capacitor
C5	VREG output capacitor	CIN4	VO1 input capacitor of external LDO
LBAT1,2 and CBAT1,2	Input Noise Filter Parts	CO4	VO4 output capacitor of external LDO

Evaluation Board Schematic

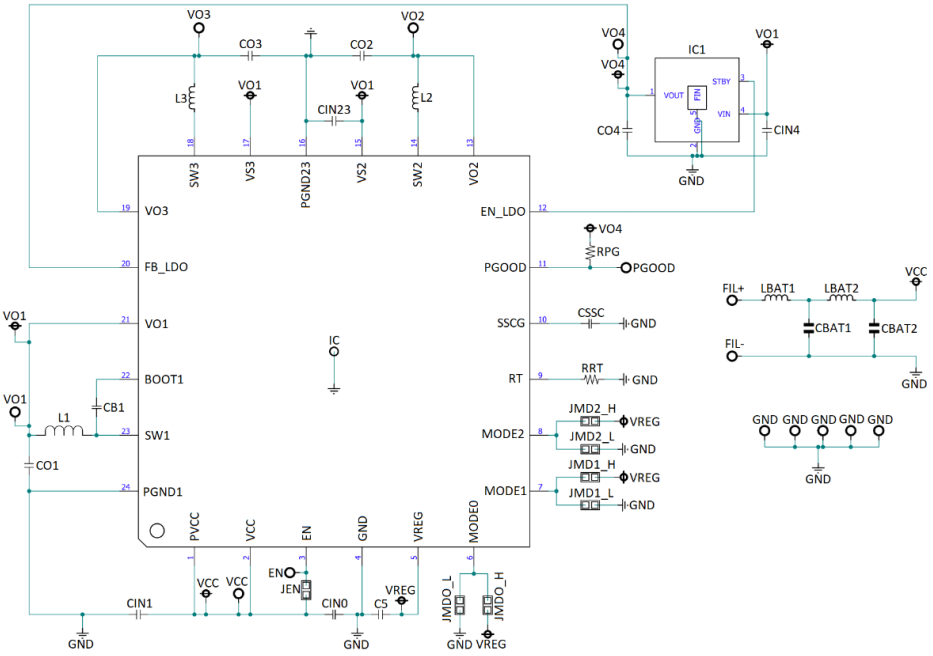

Figure 3.Circuit Diagram

Pin Configuration

(TOP VIEW)

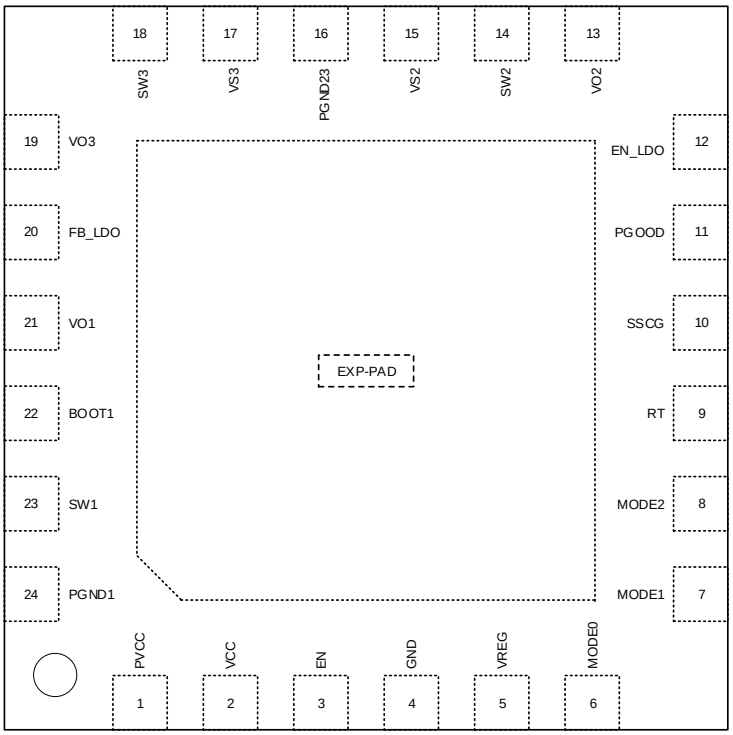

Figure 4. Pin Configuration

Pin Description

Table 3. Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	PVCC	Power supply for DC/DC1	13	VO2	DC/DC2 output voltage feedback
2	VCC	Power supply	14	SW2	DC/DC2 switching output
3	EN	Enable control input	15	VS2	Power supply for DC/DC2
4	GND	Ground	16	PGND23	Power ground for DC/DC2 and DC/DC3
5	VREG	Internal regulator output	17	VS3	Power supply for DC/DC3
6	MODE0	Mode select 0(Note 1)	18	SW3	DC/DC3 switching output
7	MODE1	Mode select 1(Note 1)	19	VO3	DC/DC3 output voltage feedback
8	MODE2	Mode select 2(Note 1)	20	FB_LDO	External LDO voltage feedback
9	RT	Adjust switching frequency	21	VO1	DC/DC1 output voltage feedback
10	SSCG	SSCG setting(Note 2)	22	BOOT1	DC/DC1 high side driver supply pin
11	PGOOD	Power Good (Note 3) (N-channel open-drain)	23	SW1	DC/DC1 switching output
12	EN_LDO	External LDO enable control output	24	PGND1	Power ground for DC/DC1
-	-		-	EXP-PAD	The EXP-PAD connect to GND, PGND1 and PGND23.

(Note 1) Connect to the GND pin or the VREG pin.

(Note 2) If not in use, connect to the GND pin

(Note 3) If not in use, open.

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Parts list

Component Coefficient (No.1)

Case1 (Light load model)		Output Current
V_{VCC}	4.0 V to 18 V	-
VO1	3.3 V	≤ 0.3 A (Note)
VO2	1.1 V or 1.2 V	≤ 0.25 A
VO3	1.8 V	≤ 0.25 A

(Note) Include VO2, VO3 and VO4 current.

Case2 (Light load model)		Output Current
V_{VCC}	5.0 V to 18 V	-
VO1	3.9 V	≤ 0.3 A (Note)
VO2	1.2 V	≤ 0.25 A
VO3	1.8 V	≤ 0.25 A

(Note) Include VO2, VO3 and VO4 current.

Component Coefficient (No.2)

Case3 (Middle load model)		Output Current
V_{VCC}	4.5 V to 18 V	-
VO1	3.3 V	≤ 1.0 A (Note)
VO2	1.1 V or 1.2 V	≤ 0.7 A
VO3	1.8 V	≤ 0.5 A

(Note) Include VO2, VO3 and VO4 current.

Case4 (Middle load model)		Output Current
V_{VCC}	5.5 V to 18 V	-
VO1	3.9 V	≤ 1.0 A (Note)
VO2	1.2 V	≤ 0.7 A
VO3	1.8 V	≤ 0.5 A

(Note) Include VO2, VO3 and VO4 current.

Case5 (Heavy load model)		Output Current
V_{VCC}	5.0 V to 18 V	-
VO1	3.3 V	≤ 2.0 A (Note)
VO2	1.1 V or 1.2 V	≤ 1.0 A
VO3	1.8 V	≤ 1.0 A

(Note) Include VO2, VO3 and VO4 current.

Case6 (Heavy load model)		Output Current
V_{VCC}	6.0 V to 18 V	-
VO1	3.9 V	≤ 2.0 A (Note)
VO2	1.2 V	≤ 1.0 A
VO3	1.8 V	≤ 1.0 A

(Note) Include VO2, VO3 and VO4 current.

Table 4. Parts List

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
RRT	1005	27kΩ	MCR01MZPF2702	Resistor	ROHM
RPG	1005	10kΩ	MCR01MZPF1002	Resistor	ROHM
CIN0	1005	0.1μF, 25V	CGA2B3X7R1E104K	Ceramic Capacitor	TDK
C5	1608	1μF, 16V	CGA3E1X7R1C105K	Ceramic Capacitor	TDK
CIN1	2012	4.7μF, 25V	CGA4J1X7R1E475K	Ceramic Capacitor	TDK
CSSC (Note3)	1005	3300pF (optional), 50V	CGA2B2X7R1H332K	Ceramic Capacitor	TDK
CO1 (Note 1)	2012	10μF, 10V	CGA4J3X7S1A106K	Ceramic Capacitor	TDK
CB1	1005	47nF, 16V	CGA2B2X7R1C473K	Ceramic Capacitor	TDK
CIN23 (Note 1)	2012	2.2μF, 16V	CGA4J3X7R1C225K	Ceramic Capacitor	TDK
CO2	2012	10μF, 6.3V	CGA4J1X7R0J106K	Ceramic Capacitor	TDK
CO3	2012	10μF, 6.3V	CGA4J1X7R0J106K	Ceramic Capacitor	TDK
L1 (Component Coefficient No.1)	2520	3.3μH, 2.0A	TFM252012ALMA3R3MTAA	Inductor	TDK
L1 (Component Coefficient No.2)	2016	3.3μH, 0.8A	MLD2016S3R3MTD25	Inductor	TDK
L2 (Note 2)	2016	1.5μH, 2.3A/20V	TFM201610ALMA1R5M	Inductor	TDK
L3 (Note 2)	2016	1.5μH, 2.3A/20V	TFM201610ALMA1R5M	Inductor	TDK
CIN4	2012	4.7μF, 25V	CGA4J1X7R1E475K	Ceramic Capacitor	TDK

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CO4	2012	10μF, 10V	CGA4J3X7S1A106K125AB	Ceramic Capacitor	TDK
IC1	SSON004R1010	-	BU29JA2MNVX-C	LDO	ROHM
IC	VQFN24FV4040	-	BD86852MUF-C	PMIC	ROHM
CBAT1	3225	10μF(optional), 25V	CGA6P3X7R1E226M250AB	Ceramic Capacitor	TDK
CBAT2	3225	10μF(optional), 25V	CGA6P3X7R1E226M250AB	Ceramic Capacitor	TDK
LBAT1	-	SHORT(optional)	-	-	-
LBAT2	2012	120Ω(optional)	BLM21PG121SH1	Ferrite bead	TDK
JEN	1608	0Ω	-	Jumper	-
JMD1_H	1608	0Ω	-	Jumper	-
JMD1_L	1608	-	-	Jumper	-
JMD2_H	1608	-	-	Jumper	-
JMD2_L	1608	0Ω	-	Jumper	-
JMDO_H	1608	0Ω	-	Jumper	-
JMDO_L	1608	-	-	Jumper	-

(Note 1) Total capacitance attached to VO1 node must not exceed 40 μF.

(Note 2)

Parts	Min value including tolerance, temperature characteristics and DC superposition characteristics
L1	2.0 μH
L2, L3	1.0 μH

(Note 3) If the spread spectrum feature is not used, the SSCG pin must be shorted to GND. In this case, the internal DCDC converter1,2,3 switching frequency is FOSC1. If the spread spectrum feature is used, please connect a capacitor (CSSC) to SSCG pin. In this case, the internal DCDC converter1,2,3 switching frequency is FOSC2.

Selection of External LDO

External LDO (IC_1) recommends BUxxJA2MNVX-C a miniature package. Please select external LDO by referring to "Mode Setting Description". If output current of VO4 exceed the following table value, adjust VO1 voltage to secure input/output voltage differences or selecting LDO with better drop out voltage characteristic is recommended.
Refer to Application circuit example (Using the VO1 resistance) for the method to adjust VO1 voltage.

Table 5. Selection of External LDO

External LDO	VO1 Voltage (typ.)	VO4 Voltage (typ.)	VO4 output current
BU28JA2MNVX-C	3.3 V	2.8 V	≤ 120 mA
BU29JA2MNVX-C	3.3 V	2.9 V	≤ 90 mA
BU33JA2MNVX-C	3.9 V	3.3 V	≤ 140 mA

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Board Layout

Evaluation Board PCB information

Number of Layers	Material	Board Size	Copper Thickness
4	FR-4	14.3 mm x 76.2 mm x 1.6 mm	4.2 mm x 74.2 mm (35 µm) / 74.2 mm x 74.2 mm (70 µm)

The layout of BD86852MUF-C is shown below.

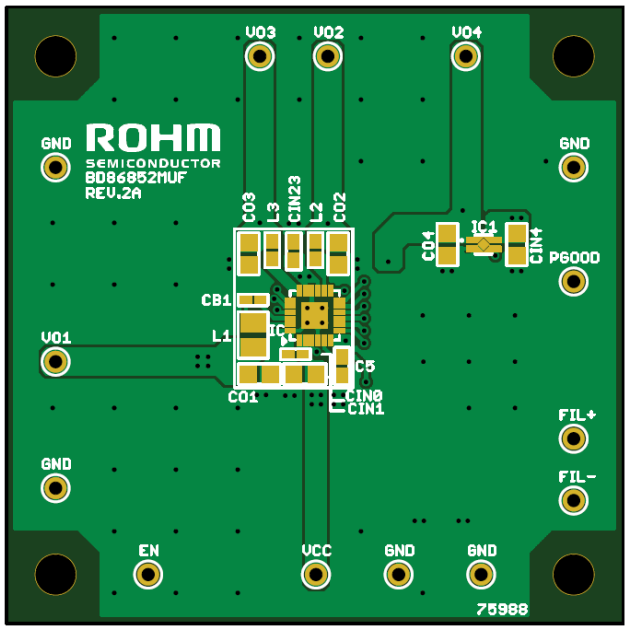

Figure 5. Top Layer Layout

(Top View)

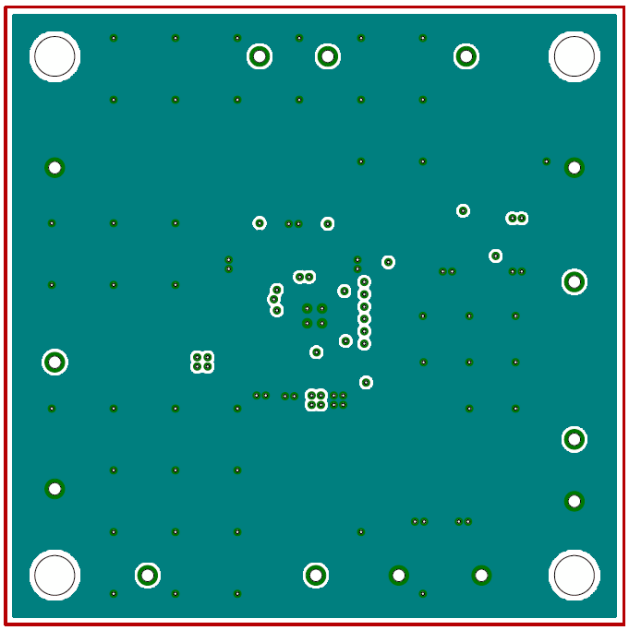

Figure 6. Middle1 Layer Layout

(Top View)

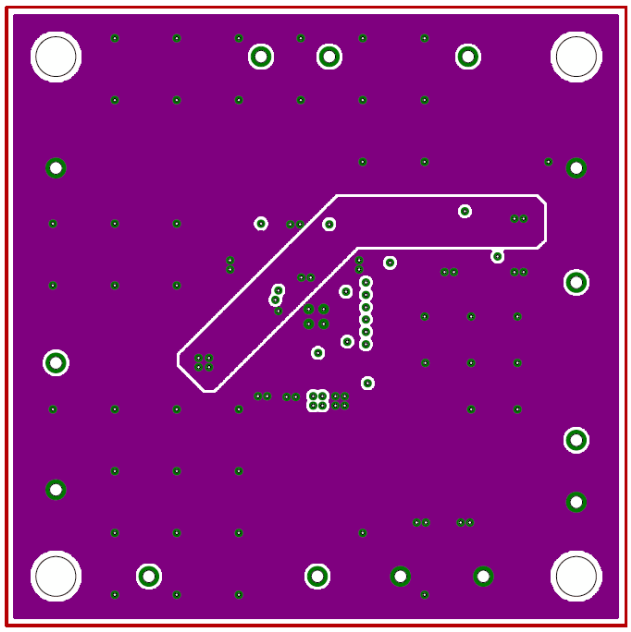

Figure 7. Middle2 Layer Layout

(Top View)

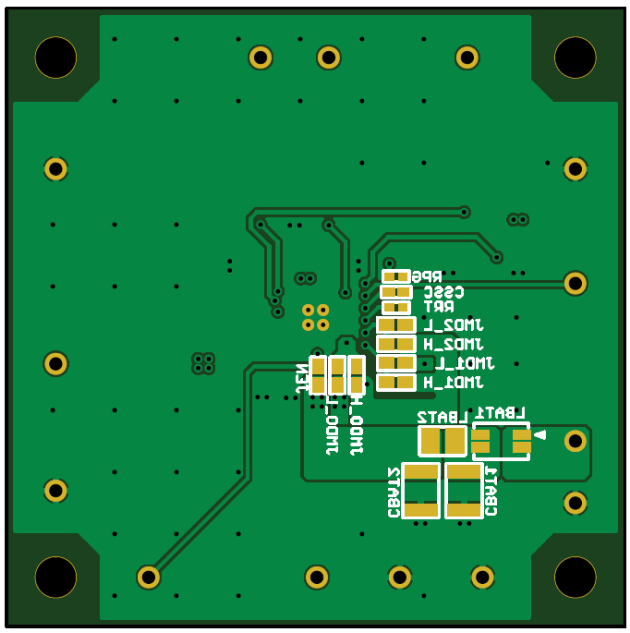

Figure 8.Bottom Layer Layout

(Top View)

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Mode Setting Description

CONTROL LOGIC Block

This block controls ON/OFF sequence, PGOOD and each protection.

When the EN Pin is high and UVLO_VCC and UVLO_VREG are released, CONTROL_LOGIC block is active.

When UVLO_VCC or UVLO_VREG is detected, CONTROL LOGIG Block will reset and initialize.

Output voltage and the sequence are decided by the combination of the MODE pins (MODE0, MODE1 and MODE2) logic.

It is necessary to connect the MODE pins to VREG or GND. The following table is details of output voltage and ON/OFF sequences.

Table 6. Mode Setting Description

Mode Name	MODE Pin (Note 1)			DCDC1 (VO1)	DCDC2 (VO2)	DCDC3 (VO3)	External LDO (VO4)	ON Sequence OFF Sequence	Protect
	2	1	0						
A-mode	L	L	L	3.3 V	1.2 V	1.8 V	2.7 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
B-mode	L	L	H	3.3 V	1.2 V	1.8 V	2.8 V	EN_LDO -> DCDC3 -> DCDC2 DCDC2 -> DCDC3 -> EN_LDO	Self-Restart
C-mode	L	H	L	3.3 V	1.2 V	1.8 V	2.9 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
D-mode	L	H	H	3.9 V	1.2 V	1.8 V	3.3 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
E-mode	H	L	L	3.3 V	1.1 V	1.8 V	2.9 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
F-mode	H	L	H	3.3 V	1.1 V	1.8 V	2.9 V	DCDC2 -> DCDC3 -> EN_LDO EN_LDO -> DCDC3 -> DCDC2	Self-Restart
G-mode	H	H	L	3.3 V	1.2 V	1.8 V	2.8 V	DCDC3 -> EN_LDO -> DCDC2 DCDC2 -> EN_LDO -> DCDC3	Self-Restart
H-mode	H	H	H	3.3 V	1.2 V	1.8 V	2.8 V	DCDC3 -> DCDC2 -> EN_LDO EN_LDO -> DCDC2 -> DCDC3	Self-Restart

(Note 1) L: GND short, H: VREG short

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Output Power Up and Power Down Sequence

Timing Chart of Start and Stop using EN (A, C, D, E, F-mode)

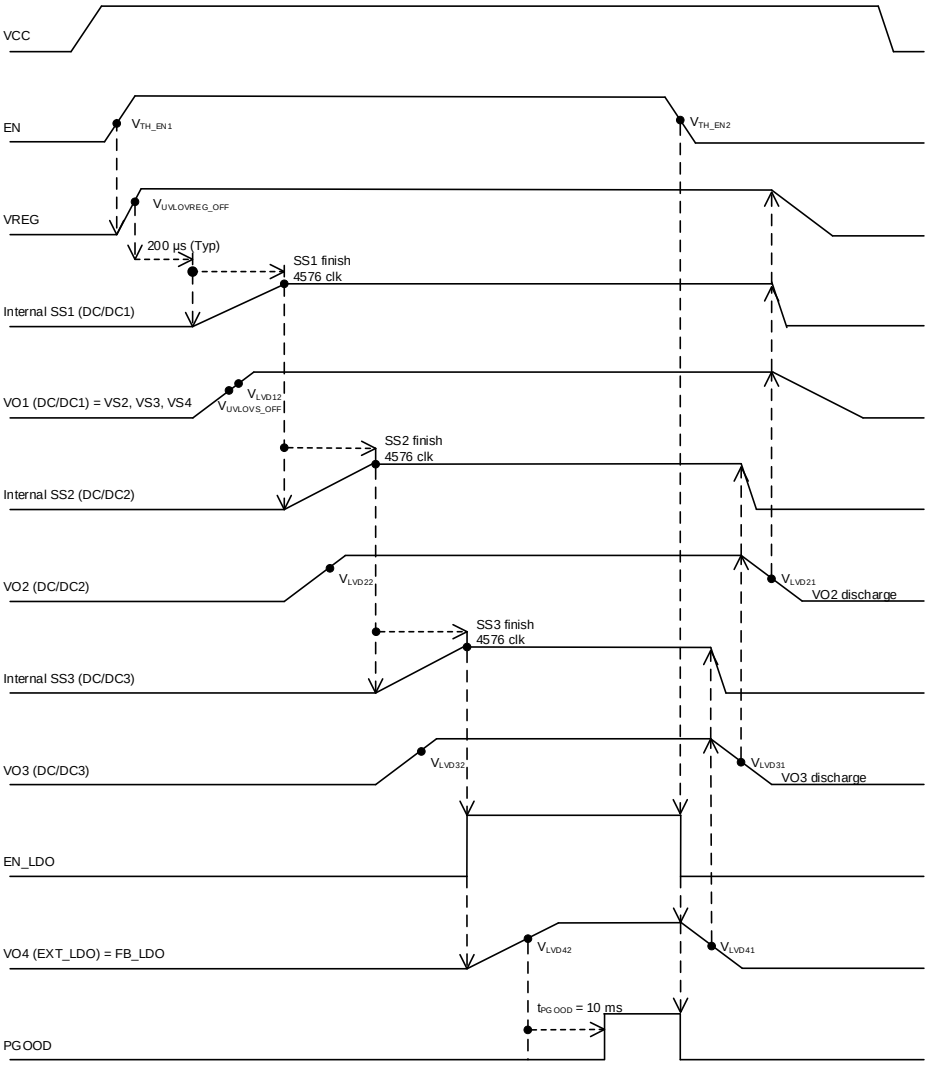

Figure 9.Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
4. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
5. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
6. Wait 10 ms (Typ) -> PGOOD is up (released). The "10 ms" time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low and EN_LDO low -> VO4 (External LDO) falls.
2. LVD4 power bad or 10 ms (Typ) after EN low input -> stop VO3 (DC/DC3) operation and start discharging VO3.
3. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> stop VO2 (DC/DC2) operation and start discharging VO2.
4. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The "10 ms" time depends on FOSC2.

(Note) Refer to the datasheet for the details about V_{LVDxx} and SSx.

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Timing Chart of Start and Stop using EN (B-mode)

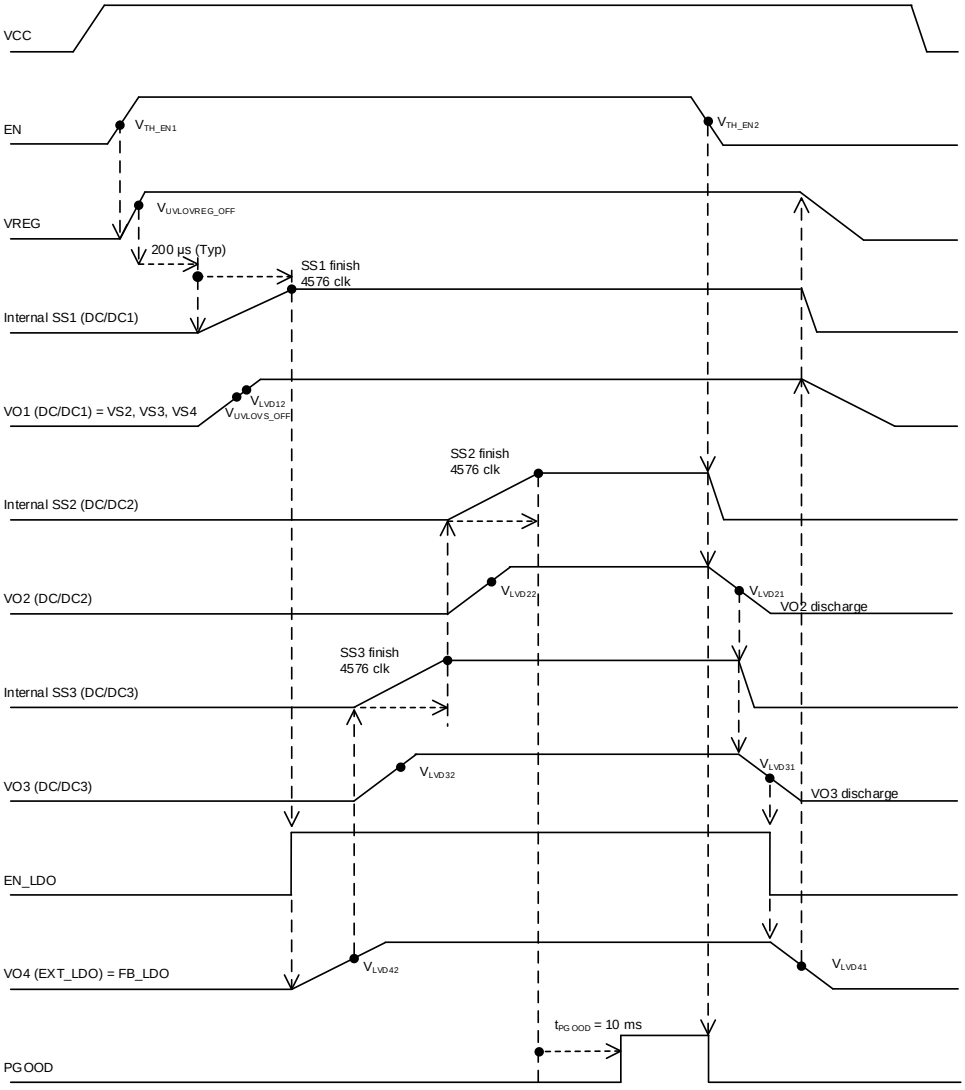

Figure 10.Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
4. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
5. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
6. Wait 10 ms (Typ) -> PGOOD is up (released). The "10 ms" time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low -> stop VO2 (DC/DC2) operation and discharging VO2.
2. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> stop VO3 (DC/DC3) operation and start discharging VO3.
3. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> VO4 (External LDO) falls.
4. LVD4 power bad or 10 ms (Typ) after EN_LDO low -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The "10 ms" time depends on FOSC2.

(Note) Refer to the datasheet for the details about V_{LVDxx} and SSx.

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Timing Chart of Start and Stop using EN (G-mode)

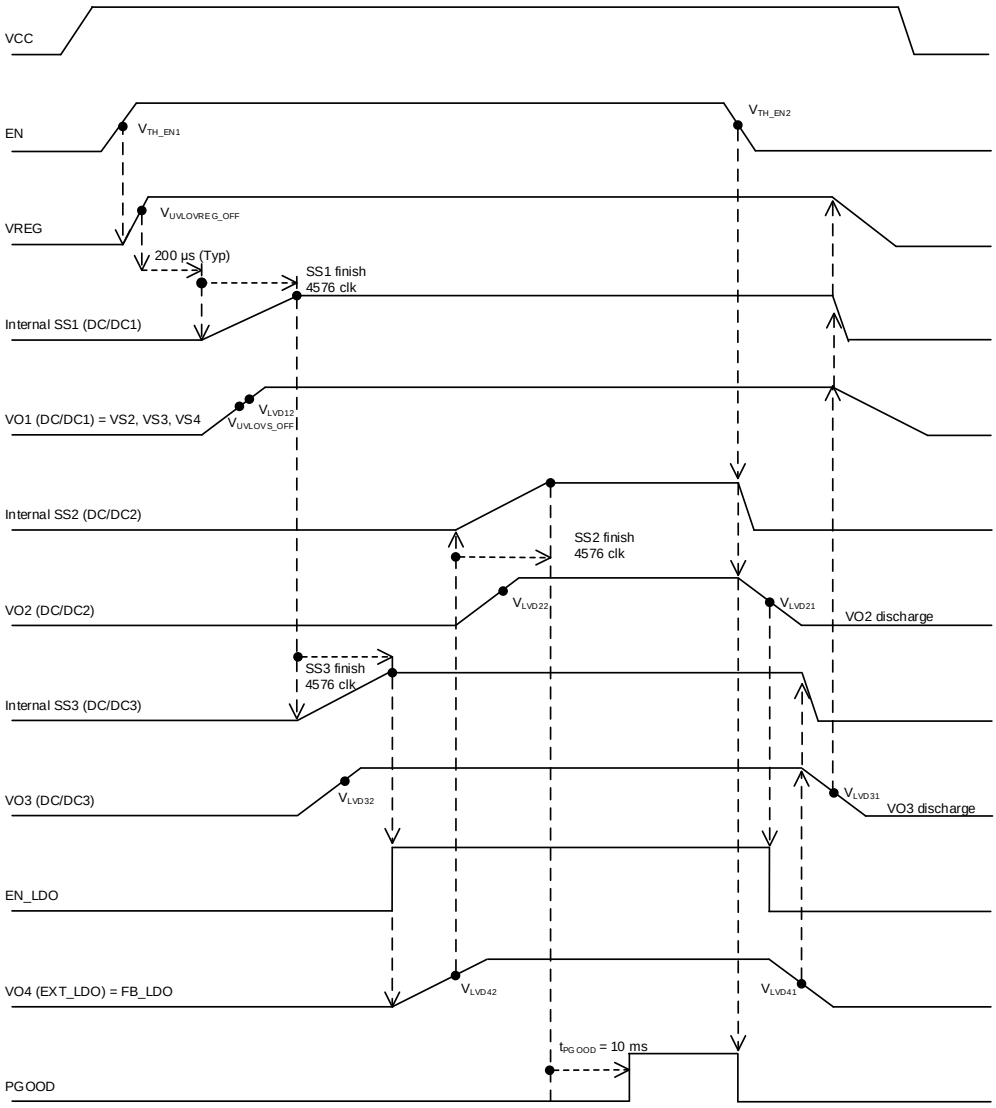

Figure 11. Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
4. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
5. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
6. Wait 10 ms (Typ) -> PGOOD is up (released). The "10 ms" time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low -> stop VO2 (DC/DC2) operation and discharging VO2.
2. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> VO4 (External LDO) falls.
3. LVD4 power bad or 10 ms (Typ) after EN_LDO low -> stop VO3 (DC/DC3) operation and start discharging VO3.
4. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The "10 ms" time depends on FOSC2.

(Note) Refer to the datasheet for the details about V_{LVDxx} and SSx.

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Timing Chart of Start and Stop using EN (H-mode)

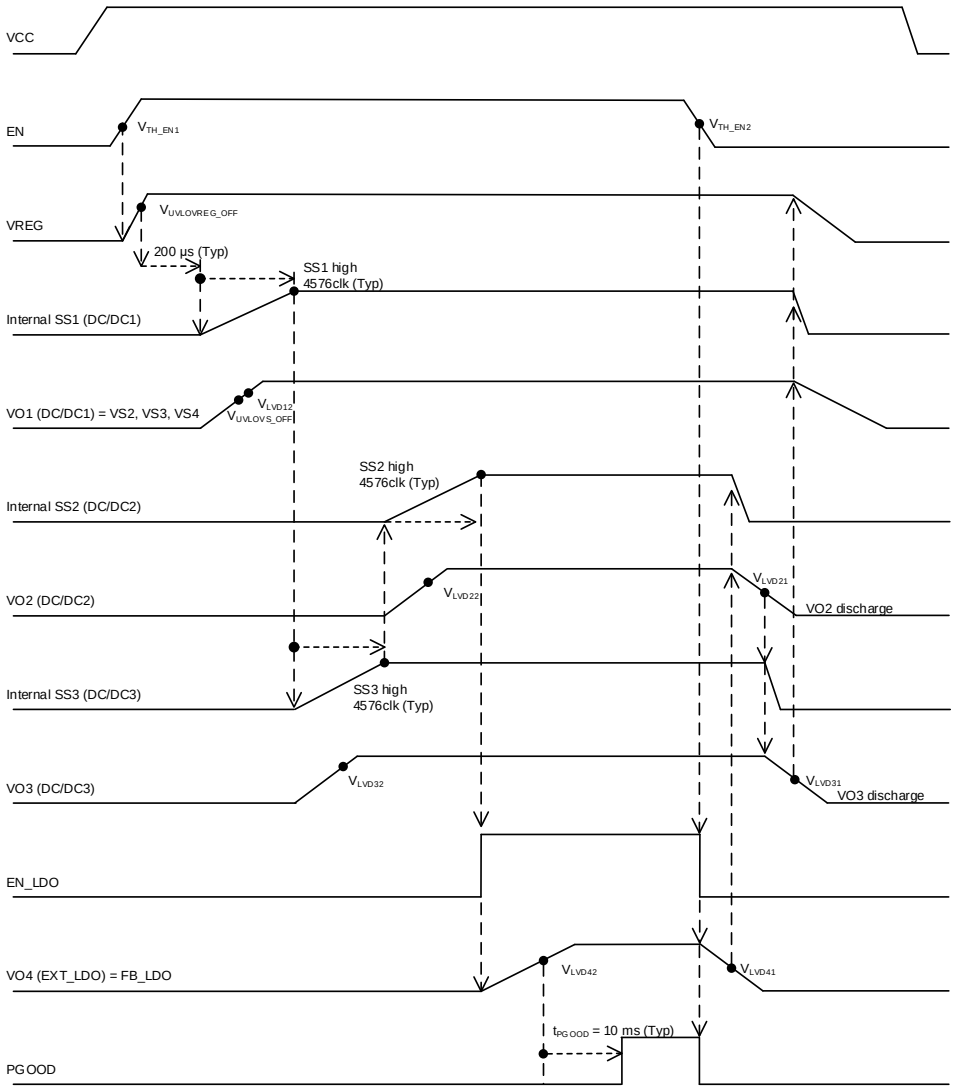

Figure 12. Output Timing Chart (EN Start-up and Stop)

Output power up sequence

1. EN high input -> Internal regulator (VREG) starts up -> VREG power good.
2. VO1 (DC/DC1) starts up -> VO1 power good (VO1 > V_{LVD12}), UVLO_VS is canceled and internal SS1 is up.
3. VO3 (DC/DC3) starts up -> VO3 power good (VO3 > V_{LVD32}), and internal SS3 is up.
4. VO2 (DC/DC2) starts up -> VO2 power good (VO2 > V_{LVD22}), and internal SS2 is up.
5. EN_LDO is up -> VO4 (External LDO) power good (VO4 > V_{LVD42}).
6. Wait 10 ms (Typ) -> PGOOD is up (released). The "10 ms" time depends on f_{OSC2}.

Output power down sequence

1. EN low input -> PGOOD low and EN_LDO low -> VO4 (External LDO) falls.
2. LVD4 power bad or 10 ms (Typ) after EN low input -> stop VO2 (DC/DC2) operation and start discharging VO2.
3. LVD2 power bad or 10 ms (Typ) after VO2 discharge start -> stop VO3 (DC/DC3) operation and start discharging VO3.
4. LVD3 power bad or 10 ms (Typ) after VO3 discharge start -> stop VO1 (DC/DC1) operation including the internal regulators (VREG).

PGOOD operation is dependent on LVD1 to 4 conditions. The "10 ms" time depends on FOSC2.

(Note) Refer to the datasheet for the details about V_{LVDxx} and SSx.

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Reference Application Data (BD86852MUF-C)

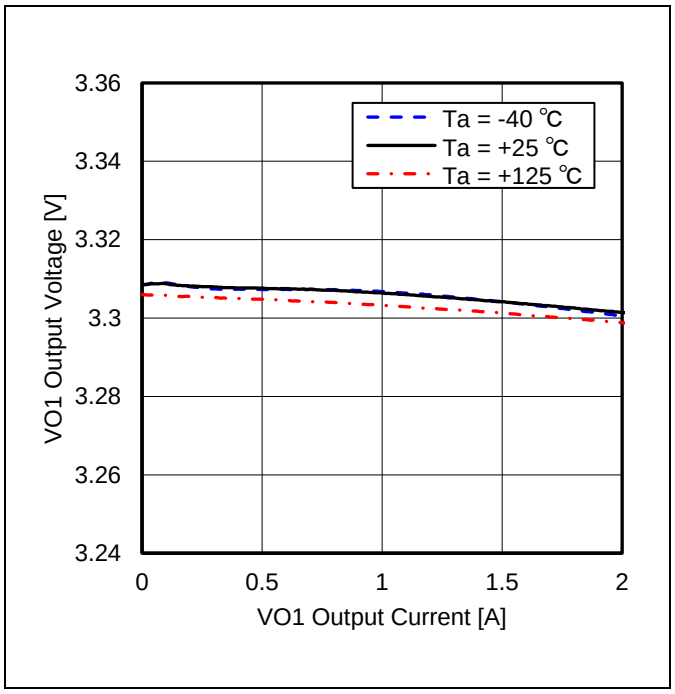

Figure 13. VO1 Output Voltage vs VO1 Output Current
(VO1 Load Regulation)

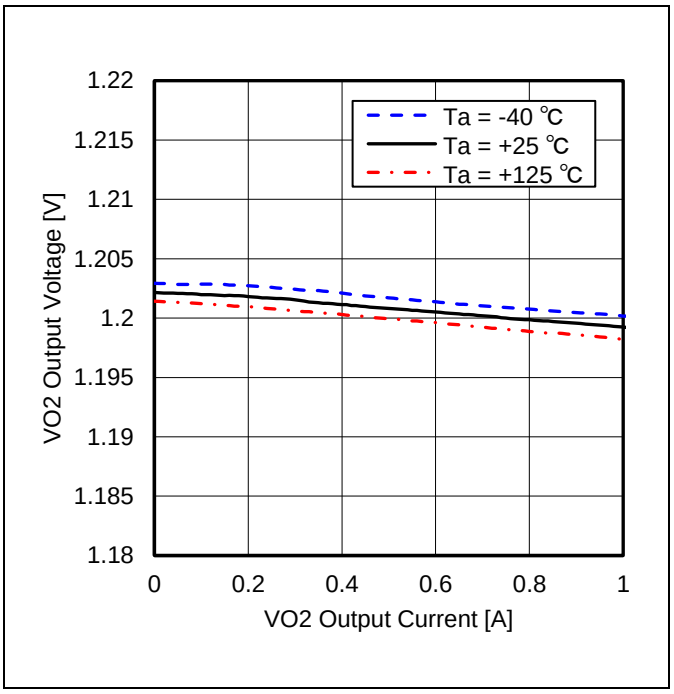

Figure 14. VO2 Output Voltage vs VO2 Output Current
(VO2 Load Regulation)

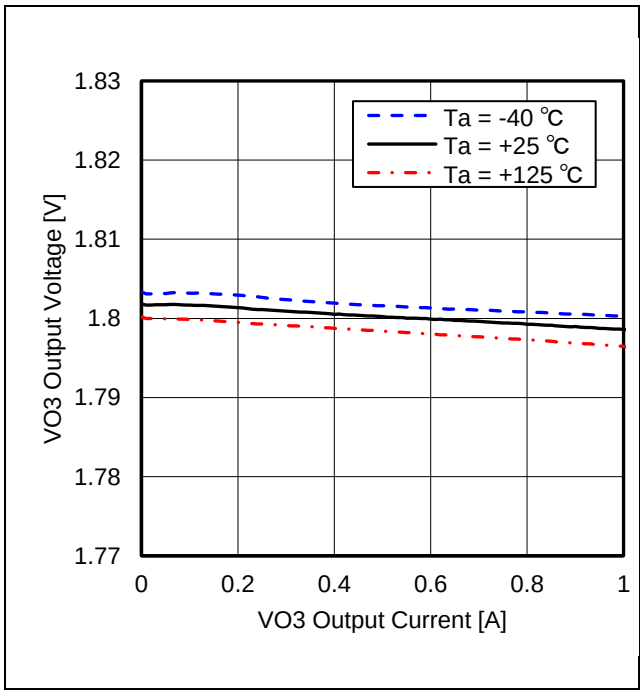

Figure 15. VO3 Output Voltage vs VO3 Output Current
(VO3 Load Regulation)

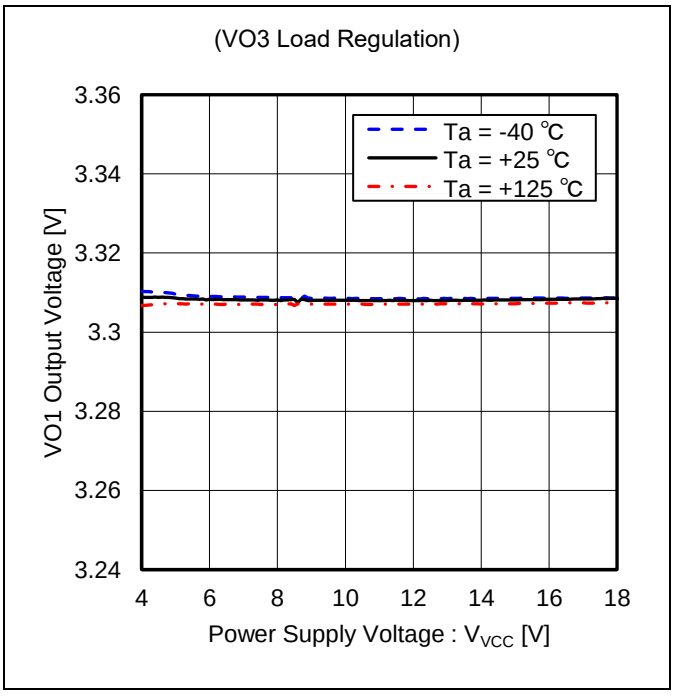

Figure 16. VO1 Output Voltage vs Power Supply Voltage
(VO1 Line Regulation)

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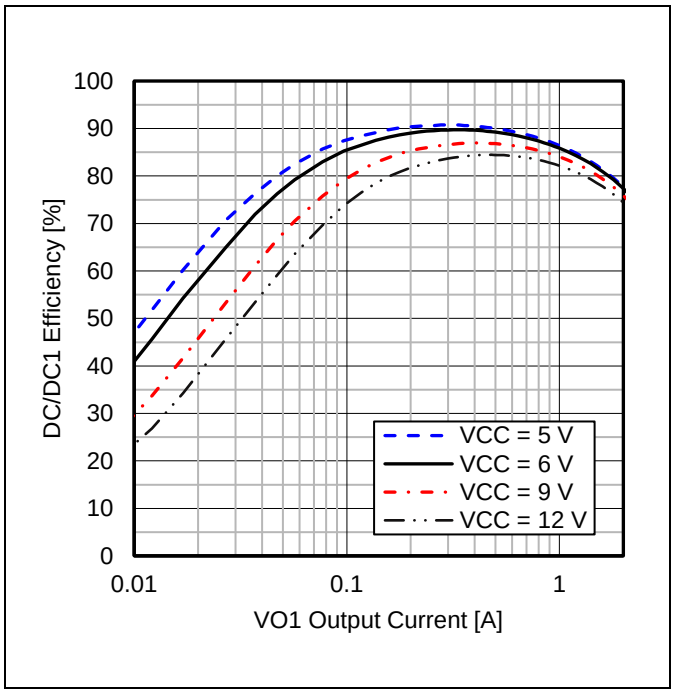

Figure 17. DC/DC1 Efficiency vs VO1 Output Current (VO1 = 3.3 V)

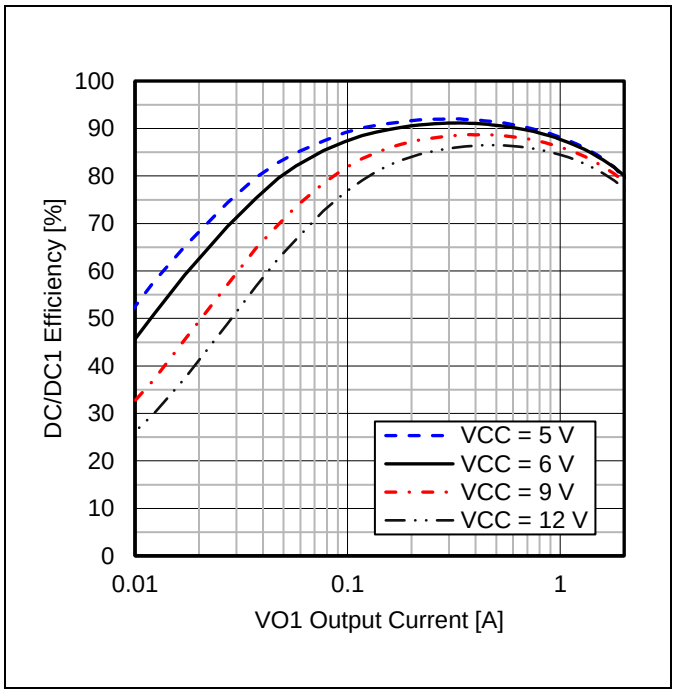

Figure 18. DC/DC1 Efficiency vs VO1 Output Current (VO1 = 3.9 V)

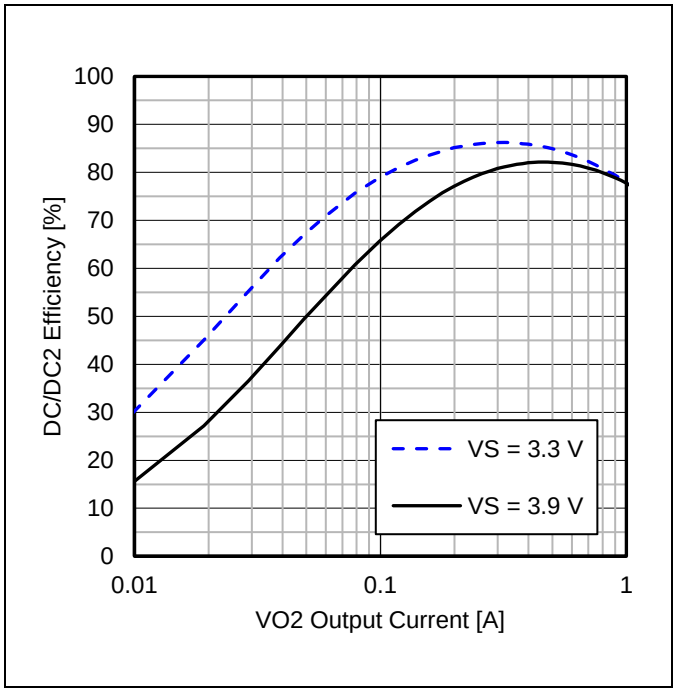

Figure 19. DC/DC2 Efficiency vs VO2 Output Current (VO2 = 1.2 V)

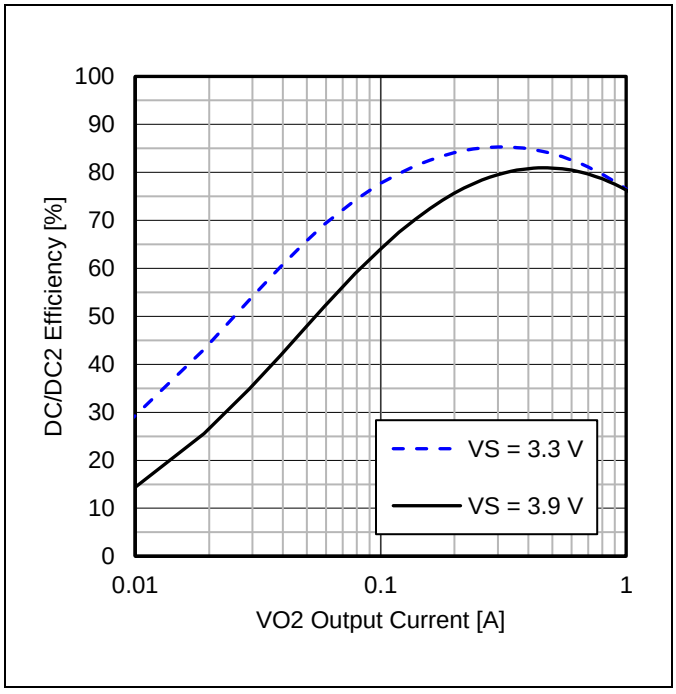

Figure 20. DC/DC2 Efficiency vs VO2 Output Current (VO2 = 1.1 V)

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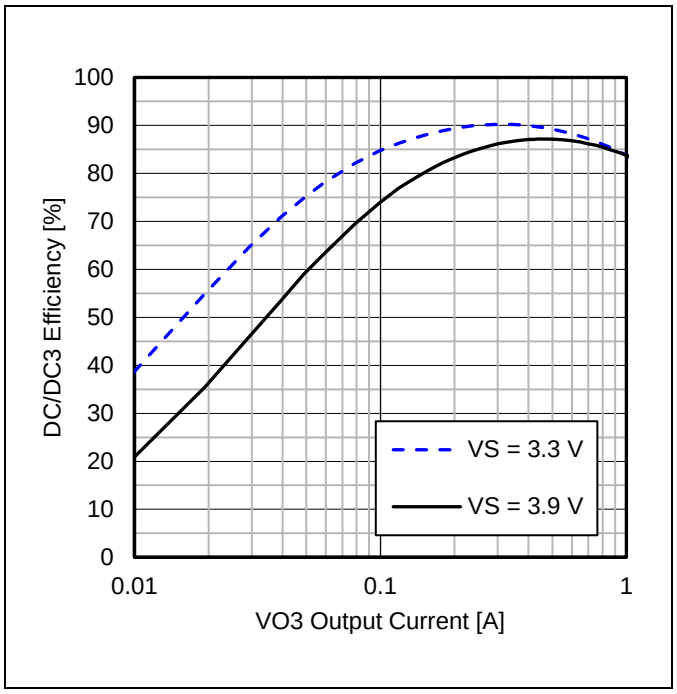

Figure 21. DC/DC3 Efficiency vs VO3 Output Current (VO3 = 1.8 V)

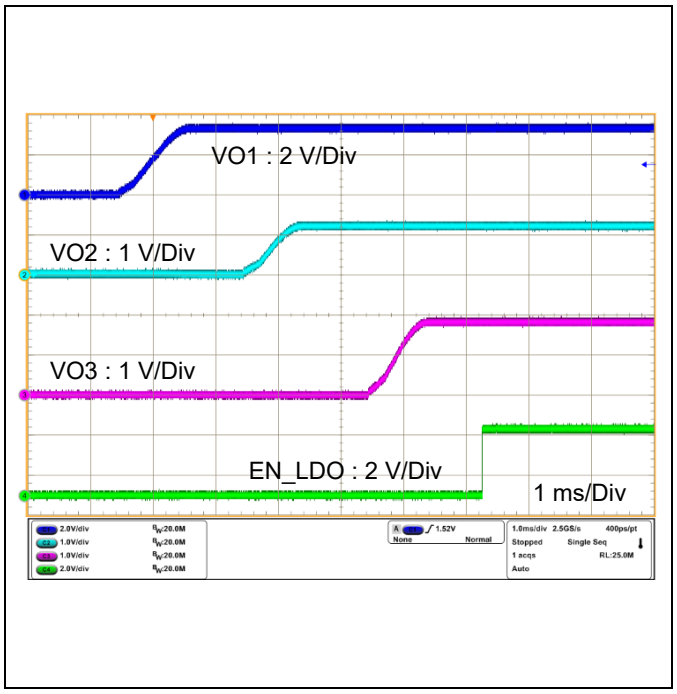

Figure 22. Start-up Waveform (A-MODE)

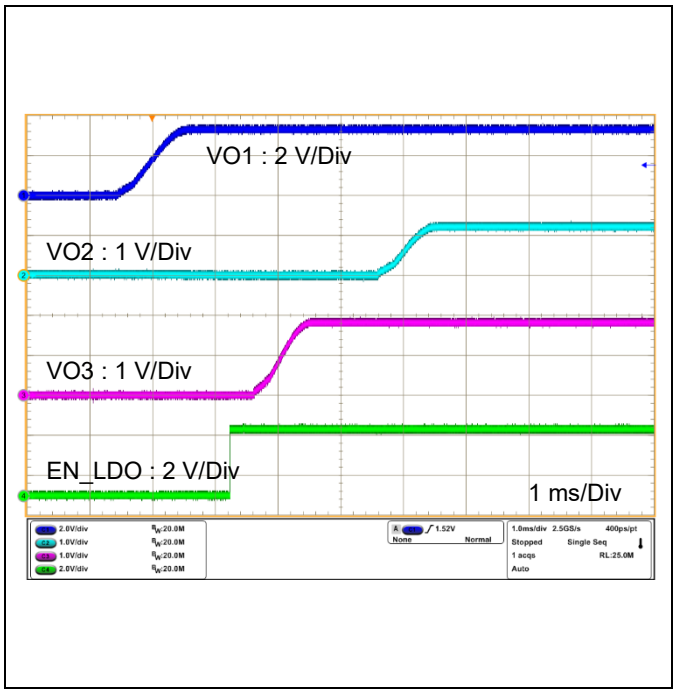

Figure 23. Start-up Waveform (B-MODE)

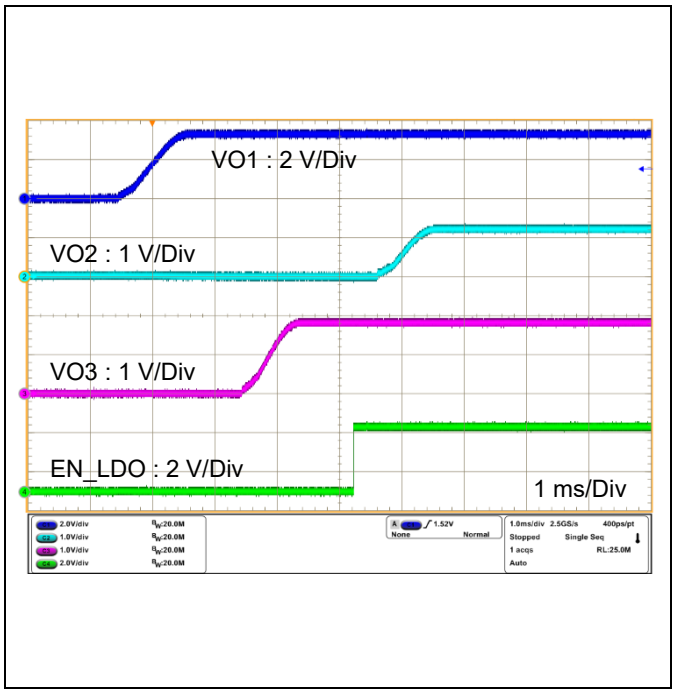

Figure 24. Start-up Waveform (G-MODE)

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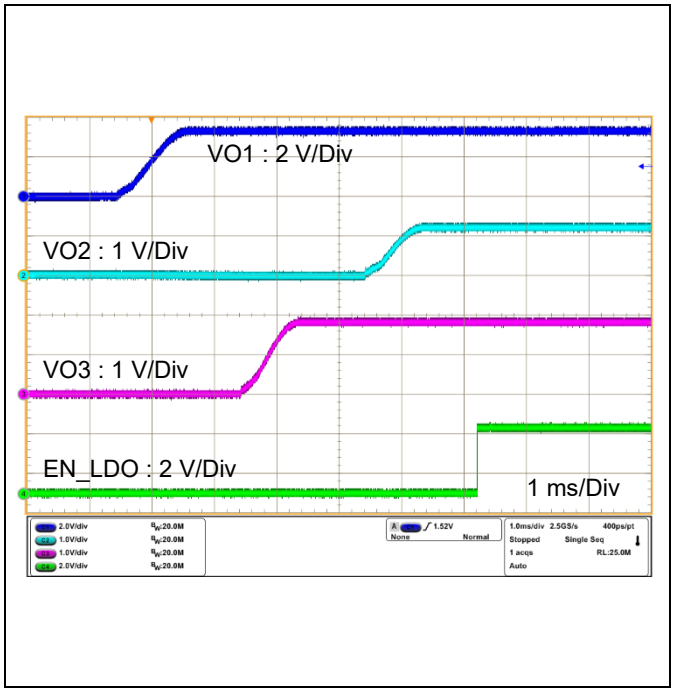

Figure 25. Start-up Waveform
(H-MODE)

Other application data refer to datasheet.

Revision History

Date	Revision Number	Description
17. Aug. 2021	001	Initial release

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Notes

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