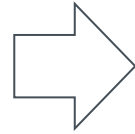
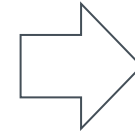


# How to add (change) a new component

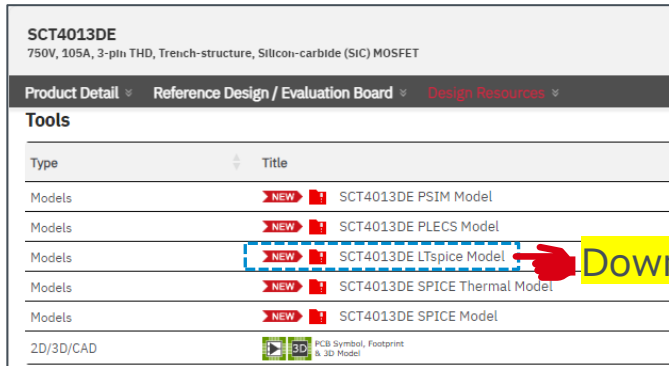
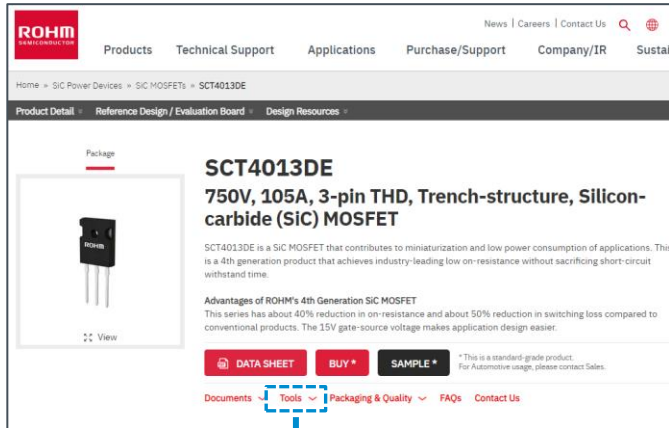
Download LTspice® model from ROHM website.



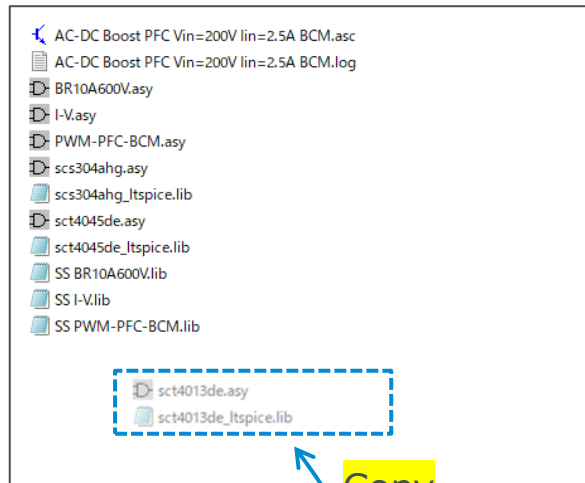
Save LTspice® model in the same folder as the schematic file.



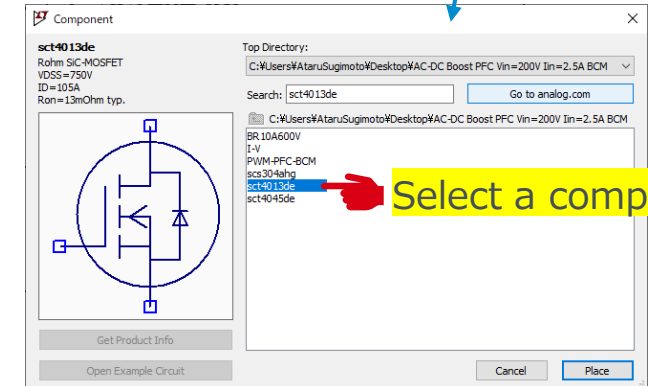
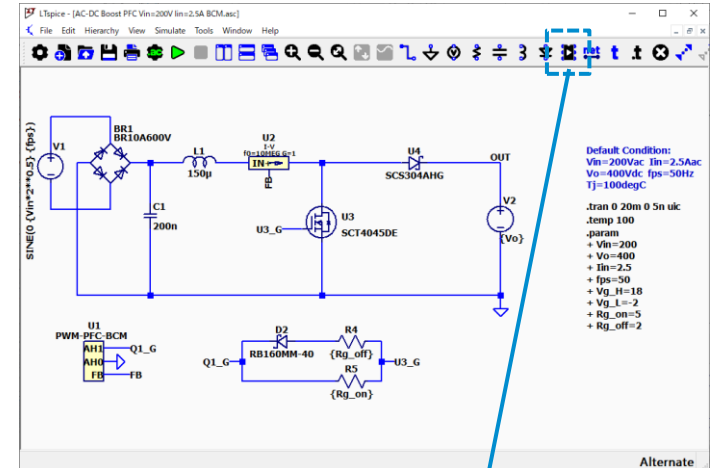
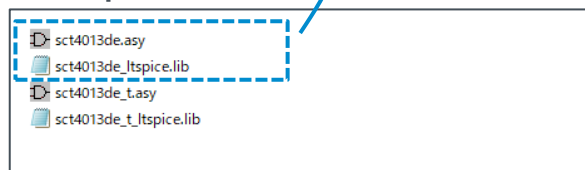
Click on the "Component" icon from the toolbar to add a new component to the schematic.



## LTspice® schematic file

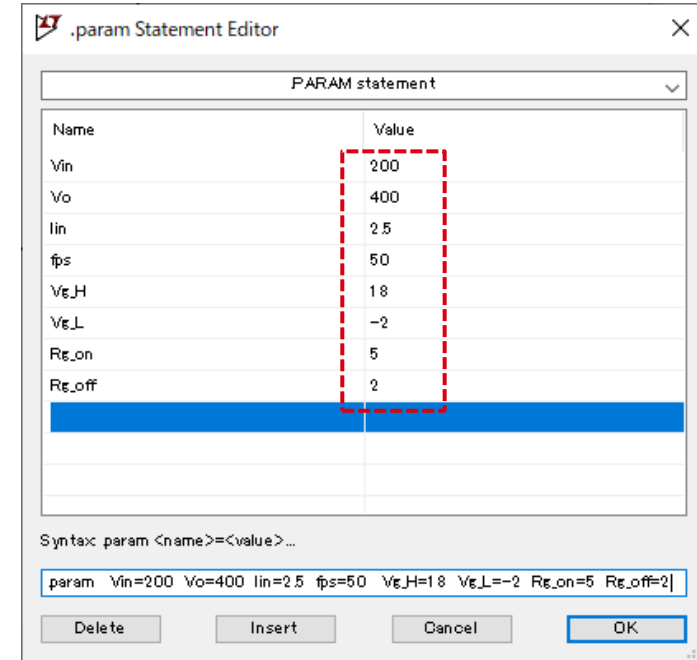
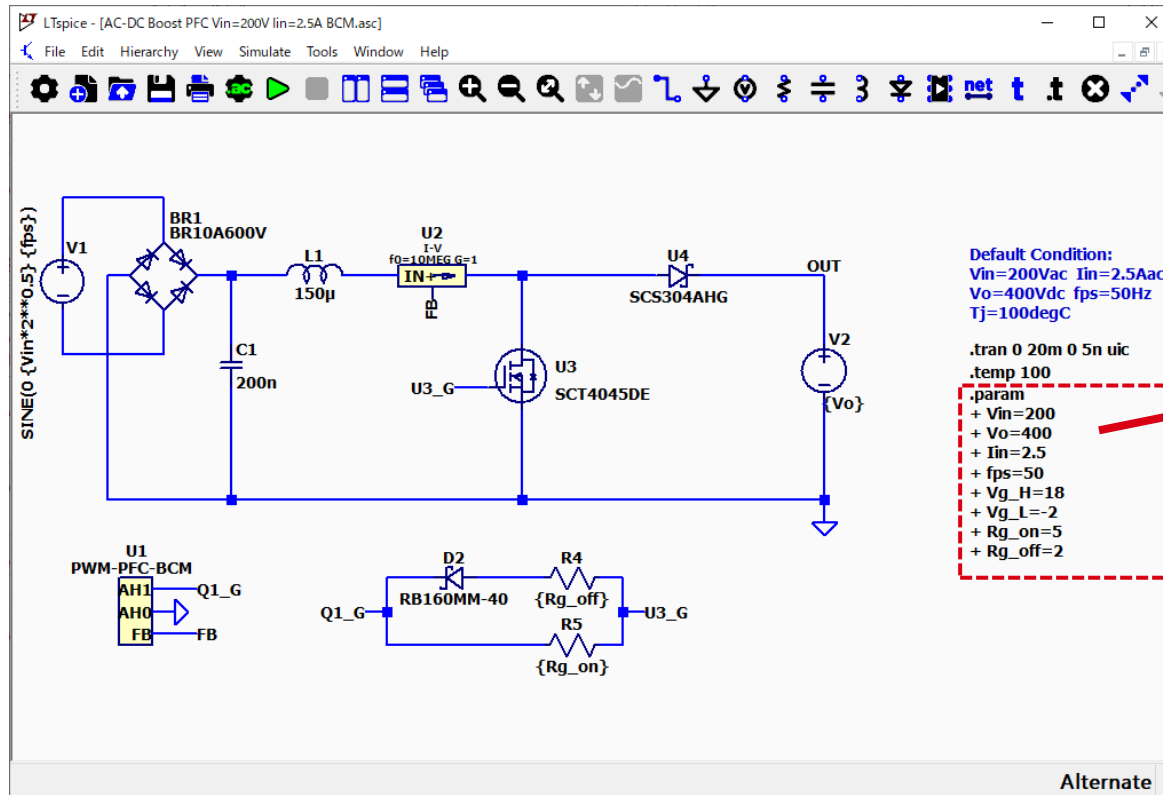


## LTspice® model

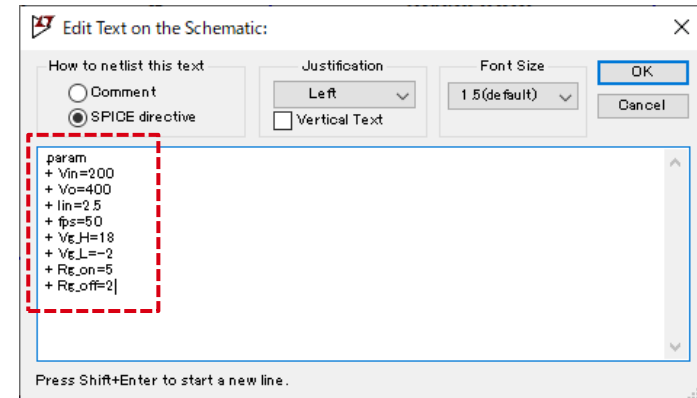


# How to change the Simulation Conditions

## Simulation Schematic



or



Right-click on the “.param” text on the schematic to launch the “.param Statement Editor” or “Text Editor. Change the parameters as necessary.

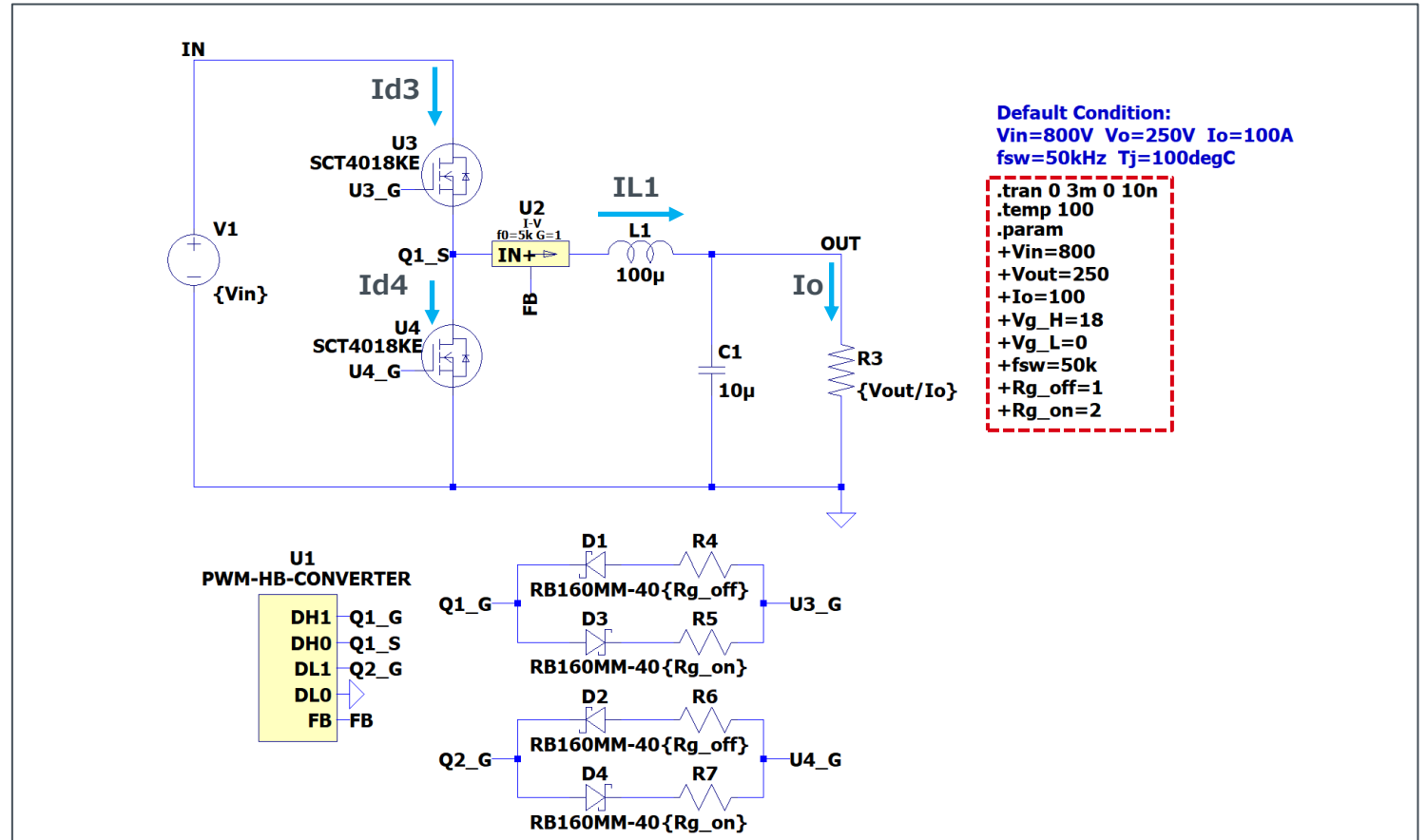
## Simulation Parameters

Param name	Unit	Description
Vin	V	Input Voltage
Vout	V	Output Voltage
Io	A	Output Current
fsw	Hz	Switching frequency
Vg_H	V	Gate Drive Voltage High
Vg_L	V	Gate Drive Voltage Low
Rg_on	$\Omega$	Gate Resistance ON
Rg_off	$\Omega$	Gate Resistance OFF

## Components

Instance name	Type	Default
U3,4	SiC MOSFET	SCT4018KE
D1,2	SBD	RB160MM-40

## Simulation Schematic



You can download and exchange other component models. See the link below for details.

[How to Use LTspice® Models](#)、[Design Simulation Models](#) : English version

[LTspice®モデルの使い方](#)、[デザインモデル](#) : 日本語版

# Simulation Result Waveform1

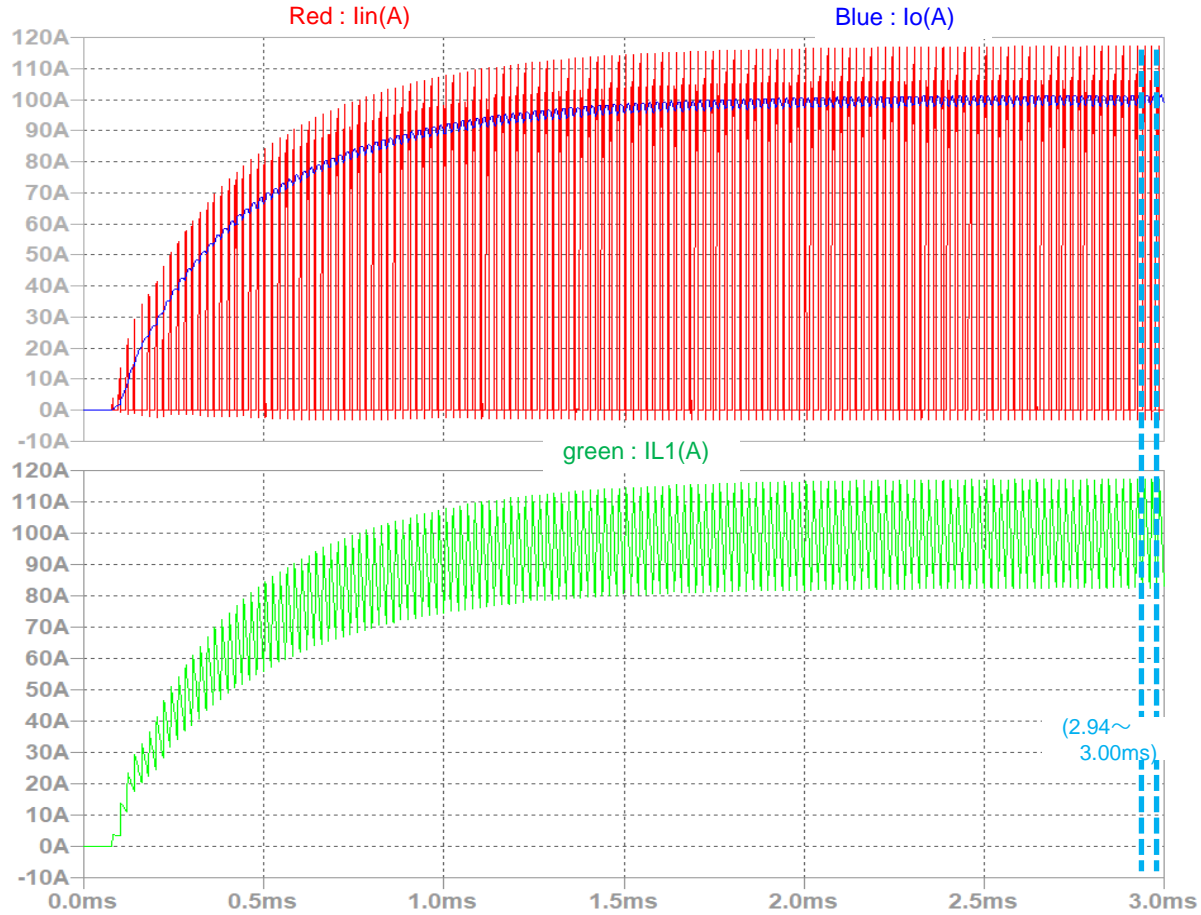
U3,4 : SiC MOSFET  
SCT4018KE

2025 Jan.

67UG117E Rev.002

IL1, lin ,Io

Vin=800V Io=100A  
Vout=250V Tj=100°C



Expansion (2.94~3.00ms)

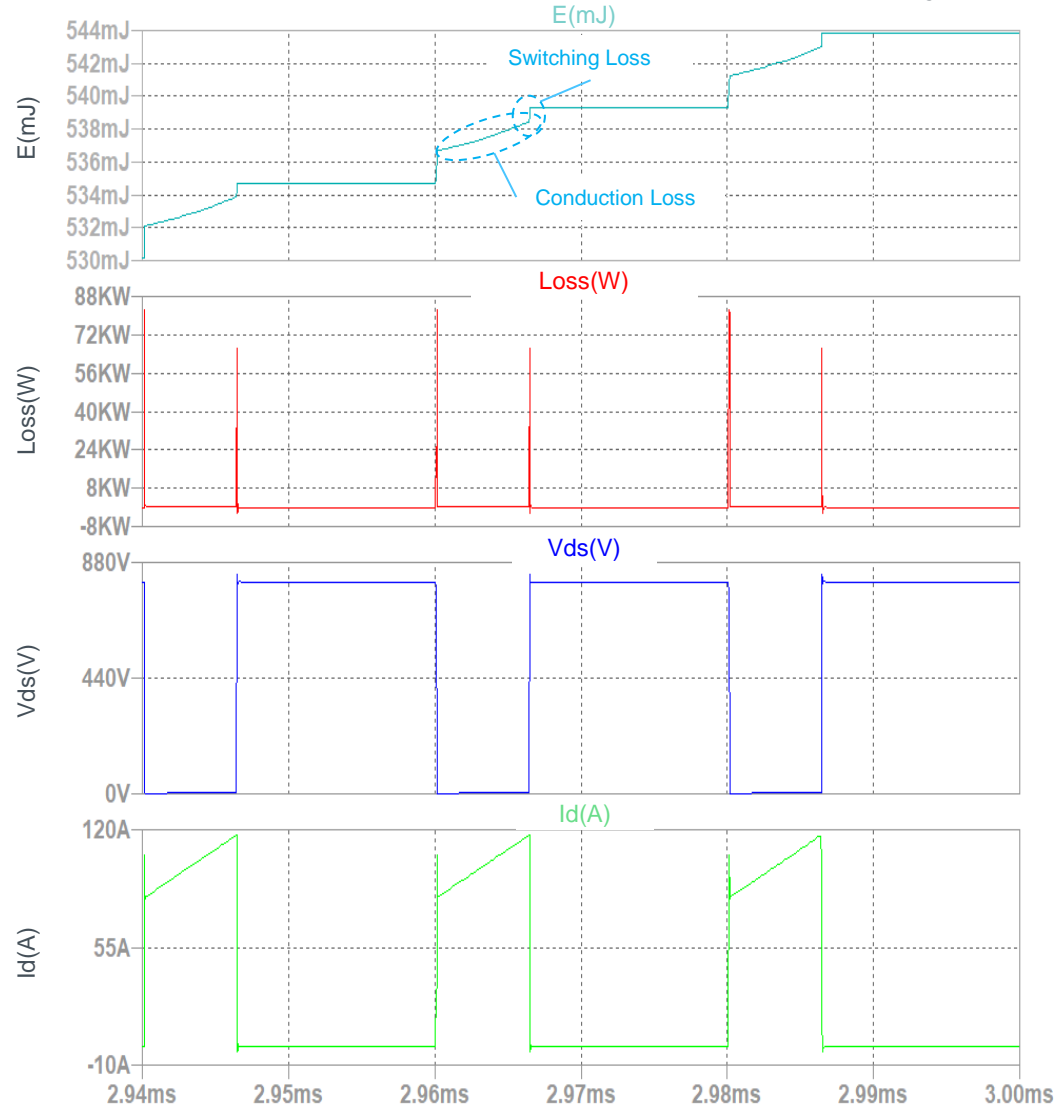


# Simulation Result Waveform2

U3,4 : SiC MOSFET  
SCT4018KE

### U3\_E, Loss, Vds, Id

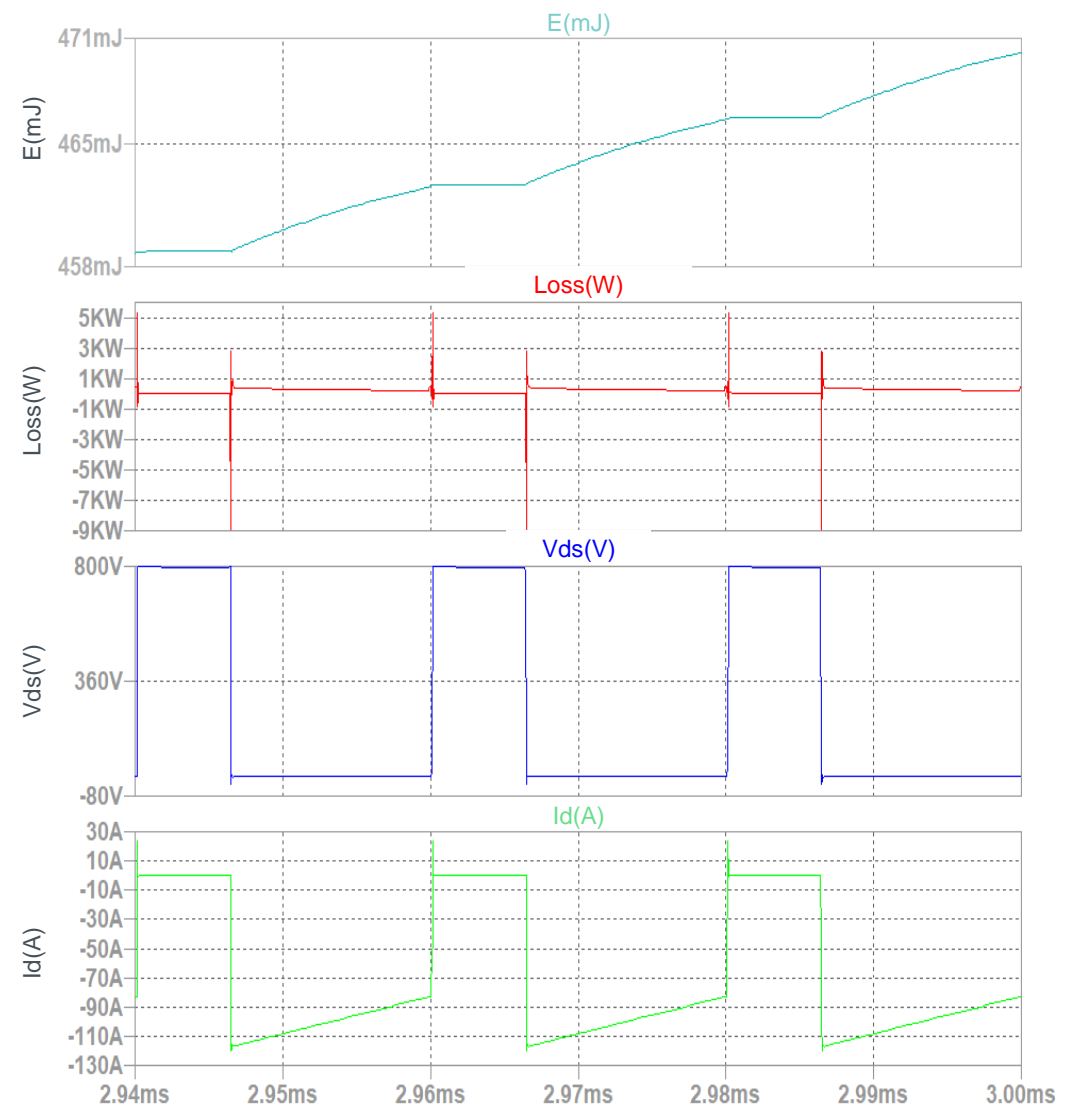
Vin=800V Io=100A  
Vout=250V Tj=100°C



### U4\_E, Loss, Vds, Id

Vin=800V Io=100A  
Vout=250V Tj=100°C

2025 Jan.  
67UG117E Rev.002



Settings

Netlist Options | Compression | Search Paths | Internet | Hacks

Operation | Schematic | Waveforms | **SPICE** | Save Defaults

Default Integration Method[\*]

trapezoidal  
 modified trap  
 Gear

Default DC solve strategy

Noopiter  
 Skip Gmin Stepping

Engine

Solver[\*]: Alternate ▾  
Max threads: 12 ▾  
Matrix Compiler: object code ▾  
Thread Priority[\*]: high ▾

Gmin: 1e-12  
Abstol: 1e-12  
Reltol: 0.001  
Chgtol: 1e-14  
Trtol[\*]: 3  
Volltol: 1e-06  
Sstol: 0.001  
MinDeltaGmin: 0.0001  
No Bypass[\*]

[\*] Setting remembered between program invocations.

Reset to Default Values

OK キャンセル ヘルプ

Configure Analysis

Transient | AC Analysis | DC sweep | Noise | DC Transfer | DC op pnt | Transient Frequency Response

Perform a non-linear, time-domain simulation.

Stop time: 3m  
Time to start saving data: 0  
Maximum Timestep: 10n

Start external DC supply voltages at 0V:   
Stop simulating if steady state is detected:   
Don't reset T=0 when steady state is detected:   
Step the load current source:   
Skip initial operating point solution:

Syntax: .tran <Tprint> <Tstop> [<Tstart> [<Tmaxstep>]] [<option> [<option>] ...]

.tran 0 3m 0 10n

Cancel and Edit Text Directly... OK Cancel

※LTspice version:24.1.3

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