Reliability Test Result

Product	Digital Transistor	Package	SOT-89 (MPT3)

1. TEST RESULT

TEST DESCRIPTION		TEST CONDITION	STANDARD	n [pcs]	Pn [pcs]
Soldering Heat Resistance	(1)	260±5℃ , 10sec. , Reflow Soldering , 2 times	JESD22-A111	22	0
	(2)	260±5℃ , 10sec. , Solder-Bath		22	0
	(3)	350±10℃ , 3sec. , Hand Soldering		22	0
Solderability	(1)	245±5℃ , 3sec. , Reflow Soldering	J-STD-002	22	0
	(2)	245±5℃ , 3sec. , Solder-Bath	JESD22-B102	22	0
Thermal Shock		0℃ ～ 100℃ , 100cycles	-	22	0
Temperature Cycle		-55±5℃←→150±5℃ , 200cycles	JESD22-A104	22	0
High Temp. High Humidity Reverse Bias		85±2℃, 85±5%RH, Specified Bias ,1000hours	JESD22-A101	22	0
Pressure Cooker Test		121±2℃ , 100%RH , 203kPa , 100hours	JESD22-A102	22	0
Load Life		25℃ , Pd=Pd max. , 1000hours	-	22	0
High Temperature Reverse Bias		Ta=Tstg max. , Specified Bias , 1000hours	JESD22-A108	22	0
High Temperature Storage		Tstg max. , 1000hours	-	22	0
Low Temperature Storage		Tstg min. , 1000hours	-	22	0
Lead strength (lead pull)		Sample body fixed, pulling lead axis direction, 5N , 10±1sec.	JEITA ED-4701/400 Test Method 401	22	0
Intermittent Operation Life		Ta=25℃±5℃ , ON 130sec /OFF 230sec, Pc max., 10,000 cycles	EIAJ ED-4701/100 Test Method 106	22	0

2. CRITERIA

ITEM	CONDITION	CRITERIA	
Output current : Io(off)	Per specification	Within two times of the standard value.	
DC current gain : GI	Per specification	Within two times of the standard value.	
Physical	Visual check	No outstanding change in physical.	
Solderability	Visual check	Reflow Soldering	Immersed surface, other than the end of pin as cut-surface, must be covered by solder.
		Solder-Bath	More than 95% of the electrode must be covered with solder.

3. JUDGEMENT

No failure is observed from each test item.

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4. TEST DESCRIPTION

TEST DESCRIPTION		TEST CONDITION	CRITERIA
1. Soldering Heat Resistance *4	(1)	1) Reflow Soldering, 260±5℃(peak) , 10 sec. , 2 times 2) After reflow soldering, leave at room temp. for more than 2h.	・Shall be no mechanical damage. ・See (*1) for criteria on electrical characteristics.
	(2) *3	1) Dip the leads once into solder bath til the point 1.5mm from the package body. 260±5℃, 10±1sec Solder : Sn-3Ag-0.5Cu（Lead free） 2) After dipping, leave at room temp. for more than 2h.	・Shall be no mechanical damage. ・See (*1) for criteria on electrical characteristics.
	(3)	1) Hand Soldering, 350±10℃ , 3sec. 2) After testing, leave at room temp. for more than 2h.	・Shall be no mechanical damage. ・See (*1) for criteria on electrical characteristics.
2. Solderability *5	(1)	1) Reflow Soldering, 245±5℃(peak) , 3sec. Solder : Sn-3Ag-0.5Cu（Lead free）	・ Immersed surface, other than the end of pin as cut-surface, must be covered by solder.
	(2) *3	Immerse the leads into flux once til the point 1.5mm from the package body for 10s, Then into solder bath of 245±5℃ til the point 1.5mm from the package body for 3±0.5s. Thereafter leave for natural dry at room temp. then wash off flux in 2-propanol. Solder : Sn-3Ag-0.5Cu（lead free） Flux : 2-propanol（IPA）(rosin 25wt%)	At least 95% of immersed surface, other than the end of pin as cut-surface, of must be covered by solder, which is observed through 10～20X magnifying glass.
3. Thermal Shock *6		1) Temp.&Time (Change within 10 sec,) 95～100℃ (Liquid) , 5min ←→ 0～5℃ (Liquid) , 5min 2) Freq. 100cycles. After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
4. Temperature Cycle *6		1) Temp.&Time (Change within 5 sec.) 55℃ (air) , 30min ←→ 150℃ (air) , 30min 2) Freq. 200cycles. After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
5. High Temp. High Humidity Reverse Bias *6		1) Ta=85±3℃, RH=75～90%、Time : 1000h 2) See (*2) for the THB bias. 3) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
6. Pressure Cooker Test *6		1) Ta=121℃, 100%RH, P=203KPa [2atm] 2) Time : 100h 3) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
7. Load Life *6		1) Ta=25±5℃, Pd/Pd(max), Time : 1000h 2) See (*2) for the THB bias. 3) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
8. High Temperature Reverse Bias *6		1) Ta=Tstg(max)±2℃, Time : 1000h 2) See (*2) for the THB bias. 3) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
9. High Temperature Storage		1) Ta=Tstg(max), Time : 1000h 2) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
10. Low Temperature Storage		1) Ta=Tstg(min), Time : 1000h 2) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.
11. Lead Strength (Lead Pull)		The sample body is fixed, and keep pulling the lead in lead axis direction with specified load for 10±1s.	Shall be no mechanical damage, detachment, extention between the lead and the package body.
12. Intermittent Operation Life		1) Ta=25±5℃, ON 130s/OFF 230s add Pc(max.). Time: 10,000 cycles, See (*2) for the LL bias. 3) After completion of test, leave at room temp. for more than 2h.	See (*1) for criteria on electrical characteristics.

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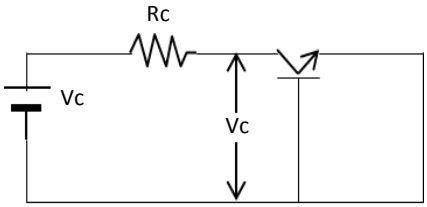
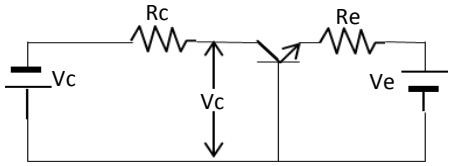
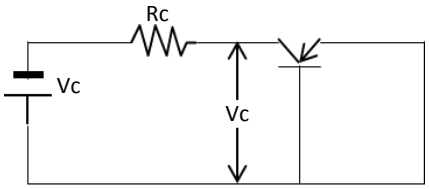
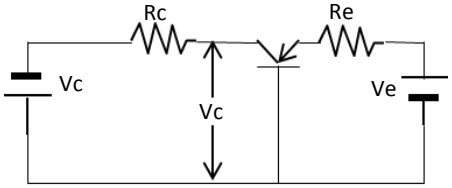
* REMARK

*1 Criteria for electrical characteristics.

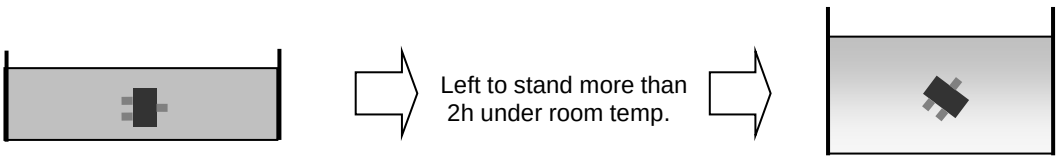
Digital Transistors
・Io(off) ＞Standard ×2
・$\frac{\triangle GI}{GI}$ > ±20%

*2 Bias Circuit

THB Bias Circuit	LL Bias Circuit
(NPN)  $V_C = BV_{CEO}$ (max.)	(NPN) 
(PNP)  $V_C = -BV_{CEO}$ (max.)	(PNP) 

Built-in resistor of digital transistors omitted

*3 Method of test 1, test 2



Immersed in solder bath

Wash off flux in 2-propanol

*4 Preconditioning : The test is carried out after it is left under the high temperature and the high humidity.(85℃,85%,168h)

*5 Preconditioning : Aging is done with the PCT device.（105℃,100%,1.22×10^5Pa,4h）

*6 Preconditioning : Soldering heat resistance(260℃,10s) is carried out. (Reflow Soldering)

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