

Product	Digital Transistor	Package	SOT-723(VMT3)
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1. TEST RESULT				
TEST ITEM	TEST CONDITION	STANDARD	n[pcs] (Sample QTY.)	Pn[pcs] (NG QTY.)
Soldering heat resistance	260±5°C , 30sec. , Reflow method 3times	JESD22-A111	22	0
	260±5°C , 10sec. , Solder-bath		22	0
	350±10°C , 3sec. , Hand soldering		22	0
Solderability	245±5°C , 3sec. , Reflow method	J-STD-002	22	0
	245±5°C , 3sec. , Solder-bath	JESD22-B102	22	0
Temperature cycle	-55±5°C ↔ 150±5°C 200cycles	JESD22-A104	22	0
High temp. high humidity reverse bias	85±2°C, 85±5%RH, specified bias ,1000hours	JESD22-A101	22	0
Pressure cooker test	121±2°C , 100%RH , 203kPa , 100hours	JESD22-A102	22	0
High temperature reverse bias	Tj max., specified bias , 1000hours	JESD22-A108	22	0
High temperature gate bias	Tj max, VGSS(max) , 1000hours	JESD22-A108	22	0
Intermittent Operation Life or Power and Temperature Cycle	Ta=25±5°C、 $\angle Tj \geq 100^\circ\text{C}$ 、 ON 120s/OFF 120s per cycle Duration: 15000cycles  Ta=-40(+0/-10)°C~+85(+10/-0)°C、 ON 300s/OFF 300s per cycle Duration: 6000cycles	MIL-STD-750 Method 1037  JESD22 A-105	22	0
Lead strength (lead pull)	Sample body fixed, pulling lead axis direction , 0.5N , 10±1sec.	JEITA ED-4701/400 Test Method 401	22	0

2. MEASUREMENT ITEM & CRITERIA			
ITEM	CONDITION	CRITERIA	
Output current : Io(off)	Per specification	According to the electrical characteristics specified by the specification	
DC current gain : GI	Per specification		
Physical	Visual check	No outstanding change in physical.	
Solderability	Visual check	Reflow Soldering	Immersed surface, other than the end of pin as cut-surface, must be covered by solder.
		Solder-bath	More than 95% of the electrode must be covered with solder.

3. JUDGEMENT
No failure is observed from each test item.

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