Automotive Motor Driver Series

Brushless DC 3-phase Gate Driver IC

BD16861MUF-C

General Description

BD16861MUF-C is a brushless DC 3-phase gate driver. IC for automotive use which drives 3 channels half bridges comprising 6 pcs of external Nch MOS-FET. It can output an electric current level flowing through each half bridge by monitoring voltage of shunt resistors and built-in amplifiers. To achieve ASIL-D level functional safety, various safety mechanisms are implemented, such as relay drivers to reduce the number of system components and Static Open/Short Detection to stably detect open/short external FET.

Features

- AEC-Q100 Qualified *(Note 1)*
- ISO 26262 Process Compliant to Support ASIL-D
- Built-in 2-stage Charge Pump Circuit
- 32bit Serial Peripheral Interface (SPI) (CRC check)
- High-Accuracy Current Sense Amplifiers (3ch)
- Integrated Relay Drivers (3ch) for Motor Lines
- Various Protections
  - Overvoltage and Undervoltage Protection
  - Open/Short Detection for External FET (Dynamic/ Static mode)
  - MCU/SPI Communication Error Detection (Q&A WDT, Interruption Detection, CRC)
  - Internal Clock Mutual Monitoring
  - Overtemperature Warning and Shutdown
- BIST for Checking Protection Functions

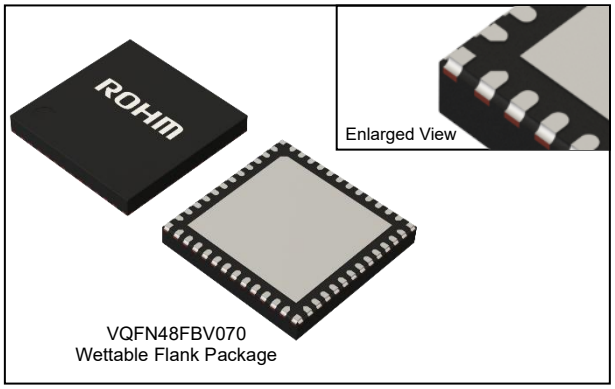
(Note 1) Grade 1

Key Specifications

- Operational Supply Voltage Range: VB: 4.5 V to 32 V
- Sleep Current: 10 µA (Max)
- Operational Temperature Range: -40 °C to +125 °C
- Gate Output Current: 75 mA to 1.2 A

Package

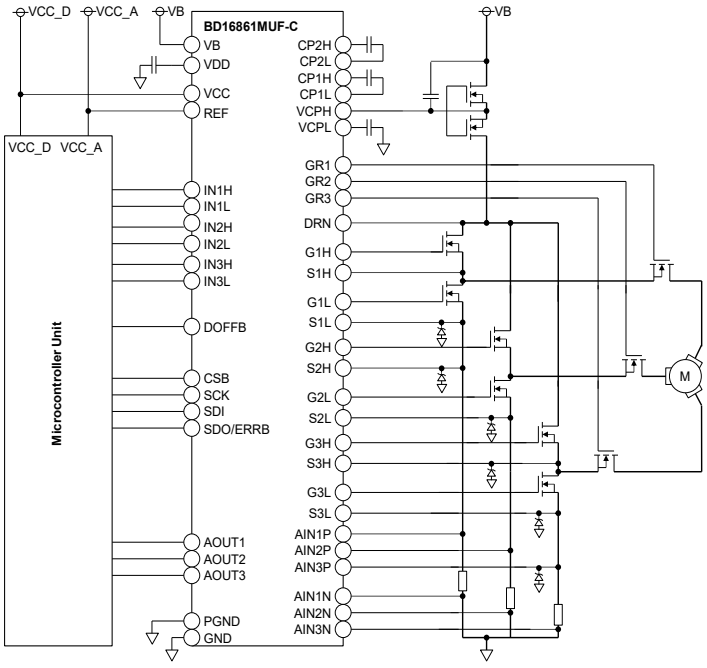
	W (Typ) x D (Typ) x H (Max)
VQFN48FBV070	7.00 mm x 7.00 mm x 1.00 mm



Applications

- EPS (Electric Power Steering)
- ISG (Integrated Starter Generator)
- EWP (Electric Water Pump) Electric OP (Oil Pump)
- BBW (Brake By Wire)
- SBW (Steer By Wire)
- PSD (Power Sliding Door)

Typical Application Circuit



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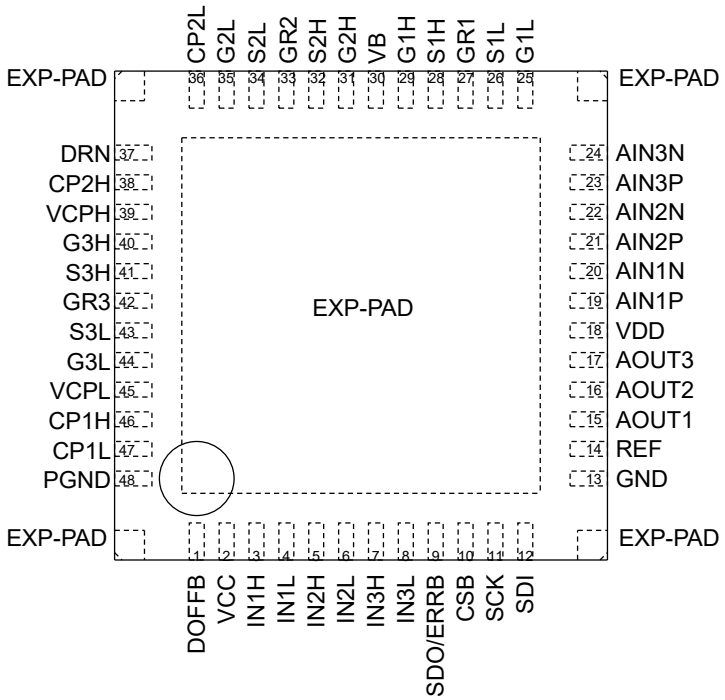
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Pin Configuration

(TOP VIEW)

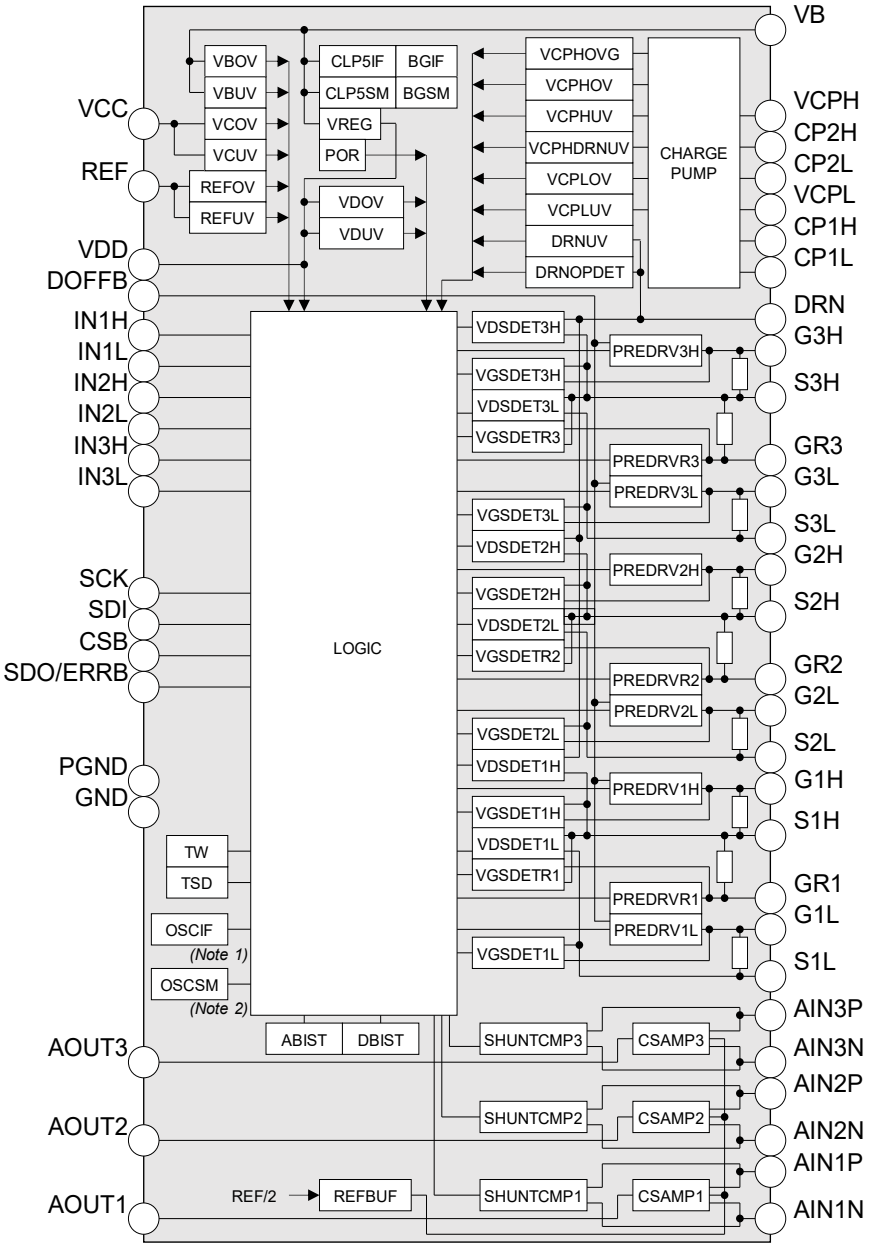


Pin Description

No.	Pin Name	Function	No.	Pin Name	Function
1	DOFFB	Gate drive outputs control	25	G1L	Connected to gate of low-side1
2	VCC	MCU supply voltage monitor and power supply for SDO/ERRB	26	S1L	Connected to source for low-side1
3	IN1H	Control input for output G1H	27	GR1	Connected to gate of Relay 1
4	IN1L	Control input for output G1L	28	S1H	Connected to source of high-side1
5	IN2H	Control input for output G2H	29	G1H	Connected to gate of high-side1
6	IN2L	Control input for output G2L	30	VB	Power supply (12 V)
7	IN3H	Control input for output G3H	31	G2H	Connected to gate of high-side2
8	IN3L	Control input for output G3L	32	S2H	Connected to source of high-side2
9	SDO/ERRB	SPI Data output / Error output	33	GR2	Connected to gate of Relay 2
10	CSB	SPI Chip select input	34	S2L	Connected to source of low-side2
11	SCK	SPI Clock input	35	G2L	Connected to gate of low-side2
12	SDI	SPI Data input	36	CP2L	Connected to Charge Pump capacitor 2
13	GND	Ground	37	DRN	Drain voltage of high-side
14	REF	Reference voltage input for CSAMP	38	CP2H	Connected to Charge Pump capacitor 2
15	AOUT1	Current sense output 1	39	VCPH	Charge Pump output 2
16	AOUT2	Current sense output 2	40	G3H	Connected to gate of high-side3
17	AOUT3	Current sense output 3	41	S3H	Connected to source of high-side3
18	VDD	LDO 5.3 V output for internal circuit	42	GR3	Connected to gate of Relay 3
19	AIN1P	Current sense input P 1	43	S3L	Connected to source of low-side3
20	AIN1N	Current sense input N 1	44	G3L	Connected to gate of low-side3
21	AIN2P	Current sense input P 2	45	VCPL	Charge Pump output 1
22	AIN2N	Current sense input N 2	46	CP1H	Connected to Charge Pump capacitor 1
23	AIN3P	Current sense input P 3	47	CP1L	Connected to Charge Pump capacitor 1
24	AIN3N	Current sense input N 3	48	PGND	Ground for the Charge Pump
EXP-PAD		The center EXP-PAD requires a short connection to the GND pin outside the IC. The center EXP-PAD and corner EXP-PADs are shorted inside the IC.			

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Block Diagram

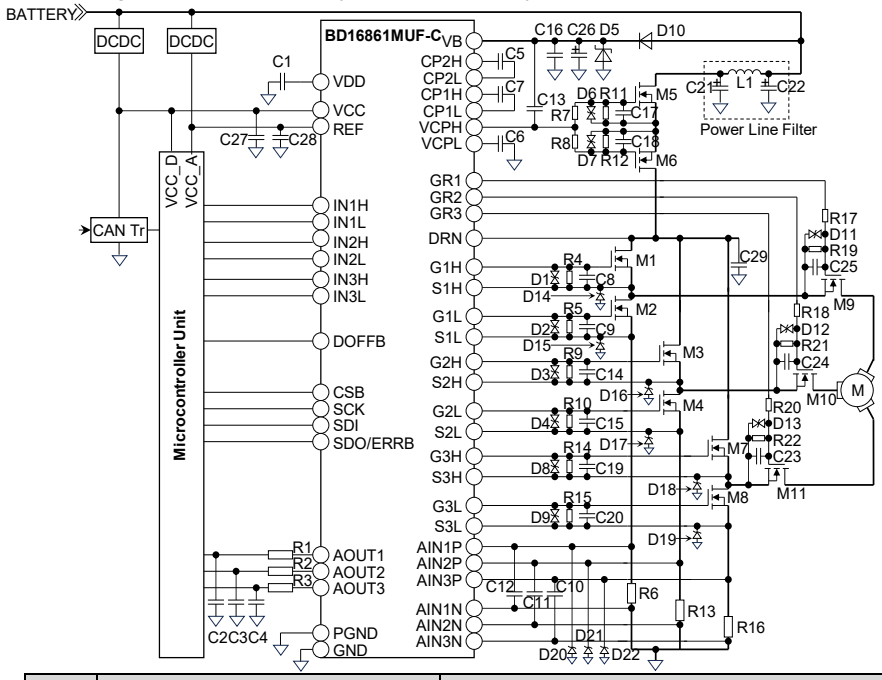


(Note 1) Generating clock is used as System CLK
(Note 2) Genarating clock is used for Monitor of System CLK

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Application Circuit and BOM List

When using external power relays and motor relays



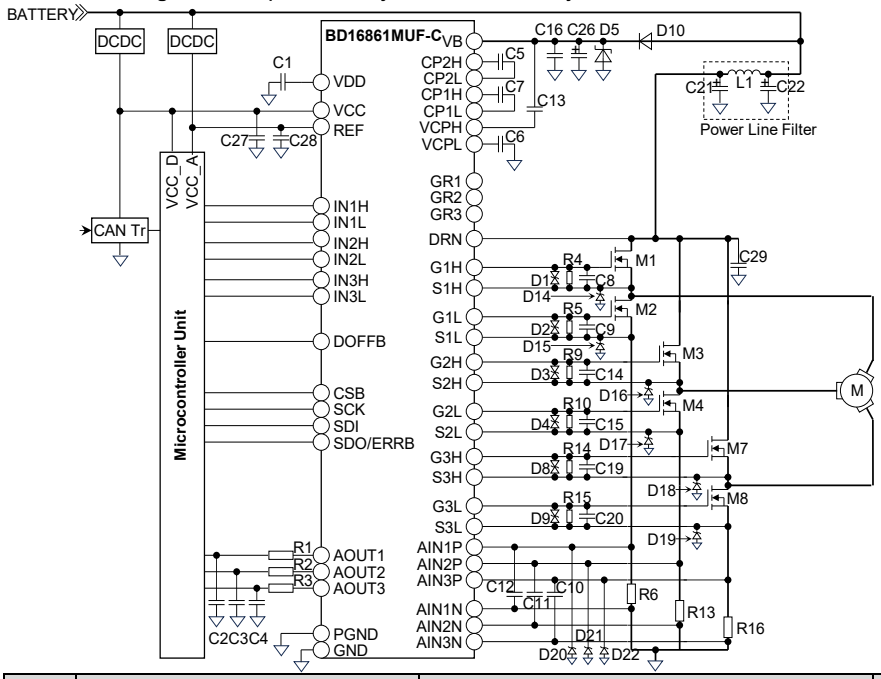
No	Item	Function	PCS	Reference Value (Typ)	Rated	Class *(Note 1)*
1	C1	Smoothing Capacitor for Internal Regulator	1	1.0 µF	10 V	A
2	C2/C3/C4	CSAMP Output filter capacitor	3	-	10 V	B
3	C5	Flying Capacitor for VCPH	1	0.47 µF	50 V	A
4	C6	Smoothing Capacitor for VCPL	1	4.7 µF	16 V	A
5	C7	Flying Capacitor for VCPL	1	0.47 µF	10 V	A
6	C8/C9/C14/C15/C17/C18/ C19/C20/C23/C24/C25	Gate-to-Source of MOSFET Protection Capacitor	11	-	-	B
7	C10/C11/C12	Capacitor for CSAMP Input	3	-	-	B
8	C13	Smoothing Capacitor for VCPH	1	1.0 µF	16 V	A
9	C16	Power-to-GND Bypass Capacitor	1	0.1 to 1 µF	50 V	A
10	C21	Noise Rejection Capacitor	1	-	-	B
11	C22	Noise Rejection Capacitor	1	-	-	B
12	C26	Power-to-GND Bypass Capacitor	1	10 µF or more	50 V	A
13	C27	Smoothing Capacitor for VCC	1	1 µF or more	10 V	A
14	C28	Smoothing Capacitor for REF	1	1 µF or more	10 V	A
15	C29	Smoothing Capacitor for DRN	1	0.1 to 1200 µF (*Note 2*)	50 V	B
16	R1/R2/R3	Resistor for CSAMP Output Filter	3	-	-	B
17	R4/R5/R9/R10/R11/R12/R14/ R15/R19/R21/R22	Gate-to-Source Pull-Down Resistor	11	-	-	B
18	R6/R13/R16	Shunt Resistor for Current Sense	3	-	-	B
19	R17/R18/R20	MOSFET Adjustment Resistor for Motor Relay	3	0.3 to 300 kΩ	-	A
20	R7/R8	MOSFET Adjustment Resistor for Power Relay	2	51 kΩ	-	A
21	D1/D2/D3/D4/D6/D7/D8/D9/ D11/D12/D13	Protection Diode for Gate-to-Source of MOSFET	11	-	-	B
22	D5	Protection Diode	1	-	-	B
23	D10	Diode for Reverse Current Protection	1	-	-	B
24	L1	Noise Rejection Inductor	1	-	-	B
25	M1/M2/M3/M4/M7/M8	MOSFET for Motor Drive	6	-	-	B
26	M5/M6	MOSFET for Power Relay	2	-	-	B
27	M9/M10/M11	MOSFET for Motor Relay	3	-	-	B
28	D14/D15/D16/D17/D18/D19	Diode for Source Protection	6	-	-	B
29	D20/D21/D22	CSAMP Input Protection Diode	3	-	-	B

(Note 1) Class A: Components required as pre-driver IC, Class B: Components required to be considered in the system.
(*Note 2)* Maximum value of C29 is 1200 µF.

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Application Circuit and BOM List – continued

When not using external power relays and motor relays



No	Item	Function	PC (S)	Reference Value (Typ)	Rated	Class (*Note 1*)
1	C1	Smoothing Capacitor for Internal Regulator	1	1.0 µF	10 V	A
2	C2/C3/C4	CSAMP Output filter capacitor	3	-	10 V	B
3	C5	Flying Capacitor for VCPH	1	0.47 µF	50 V	A
4	C6	Smoothing Capacitor for VCPL	1	4.7 µF	16 V	A
5	C7	Flying Capacitor for VCPL	1	0.47 µF	10 V	A
6	C8/C9/C14/C15/C17/C18/ C19/C20	Gate-to-Source of MOSFET Protection Capacitor	11	-	-	B
7	C10/C11/C12	Capacitor for CSAMP Input	3	-	-	B
8	C13	Smoothing Capacitor for VCPH	1	1.0 µF	16 V	A
9	C16	Power-to-GND Bypass Capacitor	1	0.1 to 1 µF	50 V	A
10	C21	Noise Rejection Capacitor	1	-	-	B
11	C22	Noise Rejection Capacitor	1	-	-	B
12	C26	Power-to-GND Bypass Capacitor	1	10 µF or more	50 V	A
13	C27	Smoothing Capacitor for VCC	1	1 µF or more	10 V	A
14	C28	Smoothing Capacitor for REF	1	1 µF or more	10 V	A
15	C29	Smoothing Capacitor for DRN	1	0.1 to 1200 µF (*Note 2*)	50 V	A
16	R1/R2/R3	Resistor for CSAMP Output Filter	3	-	-	B
17	R4/R5/R9/R10/R11/R12/R14/ R15	Gate-to-Source Pull-Down Resistor	11	-	-	B
18	R6/R13/R16	Shunt Resistor for Current Sense	3	-	-	B
21	D1/D2/D3/D4/D8/D9/D11	Protection Diode for Gate-to-Source of MOSFET	11	-	-	B
22	D5	Protection Diode	1	-	-	B
23	D10	Diode for Reverse Current Protection	1	-	-	B
24	L1	Noise Rejection Inductor	1	-	-	B
25	M1/M2/M3/M4/M7/M8	MOSFET for Motor Drive	6	-	-	B
28	D14/D15/D16/D17/D18/D19	Diode for Source Protection	6	-	-	B
29	D20/D21/D22	CSAMP Input Protection Diode	3	-	-	B

(Note 1) Class A: Components required as pre-driver IC, Class B: Components required to be considered in the system.
(*Note 2)* Maximum value of C29 is 1200 µF.

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1. IC State Description

1.1 State Transition Diagram

This IC has some states shown in the table below.

State	Description
Sleep	No operation in IC. Minimum current consumption in this state.
DBIST	Logic BIST is running. Therefore, logic block does not accept any operation from SPI until Logic BIST is finished. If clock is stopped, this IC stays in this state.
ABIST	Analog BIST is running. Logic block accepts some operation from SPI. Charge Pumps are booted. If Charge Pump cannot be booted, this IC stays in this state. When Analog BIST is finished, Charge Pump is stopped.
Stand-by	VDD for internal circuits is turned on. SPI is available. Protection functions for various power supplies are valid. Charge Pumps are not active and the protection circuit for them is invalid. Gate and relay drivers are fixed to Hi-Z.
CPON	Charge Pump are booted. If Charge Pump cannot be booted, this IC stays in this state.
Active	Charge Pump and the protection circuit are enabled. Gate driver, Relay driver and Current sense amplifiers are available. (If the current sense function is not required, MCU set Register CSEN to '0'. Power consumption can be reduced.)
FAIL	If DBIST fails, ABIST fails or Internal Error occurs, it transitions to this state. SPI and Error detection are available.

To read IC state status, MCU read register 05h by SPI access.
After reading register 05h in each state, the status is as shown below.

State	State (FAIL)	End (BIST)	End (OS)	State (ABIST)	State (CPON)	State (ACT)	State (STB)	State (ERRB)	Reg 05h
Sleep	Cannot read status from SPI								
DBIST									
ABIST	0	0	0	1	0	0	0	1	0011h
Stand-by	0	1	0	0	0	0	1	1	0043h
CPON	0	1	0	0	1	0	0	1	0049h
Active	0	1	0	0	0	1	0	1	0045h
FAIL	1	1	0	0	0	0	0	0	00C0h

End (OS) register is set to 1 when Static Open/Short Detection is finished.

IC functions for each state are as follows.

	Normal Function					Error Detection				
State	Logic OSC	BIST	SPI Access	Chage Pump	CSAMP Relay driver Gate driver	Internal	OSC Stop SPI REG	VB OV VDD OV VCC UV/OV REF UV/OV TW/TSD WDT SPI Stop	VB UV VDD UV OSC Freq	VCP UV/OV DRN UV VGS/VGSR VDS SNT Dynamic OS Static OS TDEAD
Sleep	S	S	S	S	S	S	S	S	S	S
DBIST	A	A				A				
ABIST			A	A		S	A	A	A	
Stand-by		S		S		A			S	
CPON				A					A	
Active					A				A	A
FAIL				S	S					S

S: Stopped/Disabled/Not active, A: Active

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1. IC State Description - Continued

State Transition Diagram is as follows.

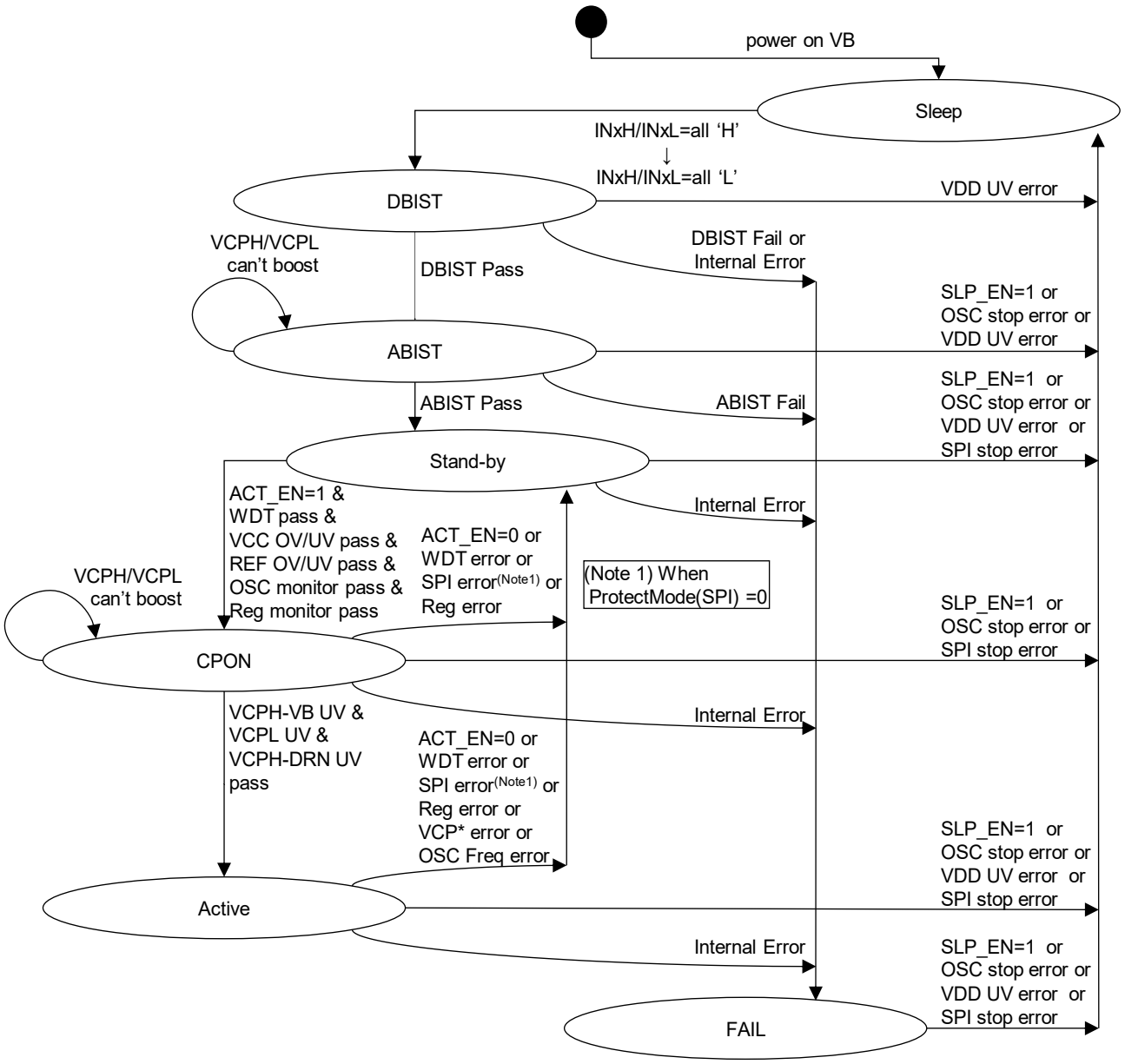


Figure 1. State machine

1.1.1 From Sleep to Stand-by state

To enter the Stand-by state from the sleep state, all INxH/INxL (x = 1,2,3) must be set to a high level and then to a low level. After that, IC turns on the internal power supply circuits and starts BIST to check each Safety Mechanism (SM). After DBIST state, SPI communication becomes available.
If DBIST and ABIST are passed, IC enter Stand-by state and End (BIST) set 1.
The period from applying low level to INxH/INxL (x = 1,2,3) to Stand-by state is maximum for 20ms.

End (BIST)	Function
1	DBIST and ABIST are finished.
0	DBIST and ABIST are not finished.

State (ABIST)	Function
1	State is ABIST state
0	State is others

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1. IC State Description - Continued

1.1.2 From Sleep to FAIL state

If either ABIST or DBIST is Fail, transition to FAIL state. And ERRB set L, Error (BIST) set 1.
If Internal Error occurs, transition to FAIL state. And ERRB set L, Error (Internal) set 1.
SPI communication becomes available, and IC cannot enter Active state.

State (FAIL)	Function
1	State is FAIL state
0	State is others

1.1.3 From Stand-by to Active state

Set register ACT_EN to '1' where the following 4 conditions are true to change the state from Stand-by through CPON to Active.

- OV/UV of VCC/REF detections are passed*(Note 1)*.
- WDT are passed. (Refer to 7.10 Watch Dog Timer (WDT) for detail.)
- OSC Error Detection does not detect errors.
- REG Monitor does not detect errors.

(Note 1) If set ErrorMaskUV(VCC) = '1' and ErrorMaskUV(REF) = '1' before set ACT_EN = '1', this condition becomes invalid.

If VCPH and VCPL turn on in CPON state, IC change state from CPON to Active.
This function does not depend on ErrorMaskUV(CP) setting.
When VCPH and VCPL can't turn on, IC continues to wait. Please check timeout in MCU.

ACT_EN	Function
1	Change state from Stand-by to Active
0	Change state from Active to Stand-by

State (CPON)	Function
1	State is CPON state
0	State is others

State (ACT)	Function
1	State is Active state
0	State is others

If set ACT_EN = '0', change state from Active to stand-by

1.1.4 From Some state to Sleep state

IC will change the state to sleep if any of following 4 conditions are met.

- 10 seconds have elapsed without SPI communication being performed correctly.
- VDD UV (under voltage) is detected.
- System CLK is stopped.
- MCU write SLP_EN = 1

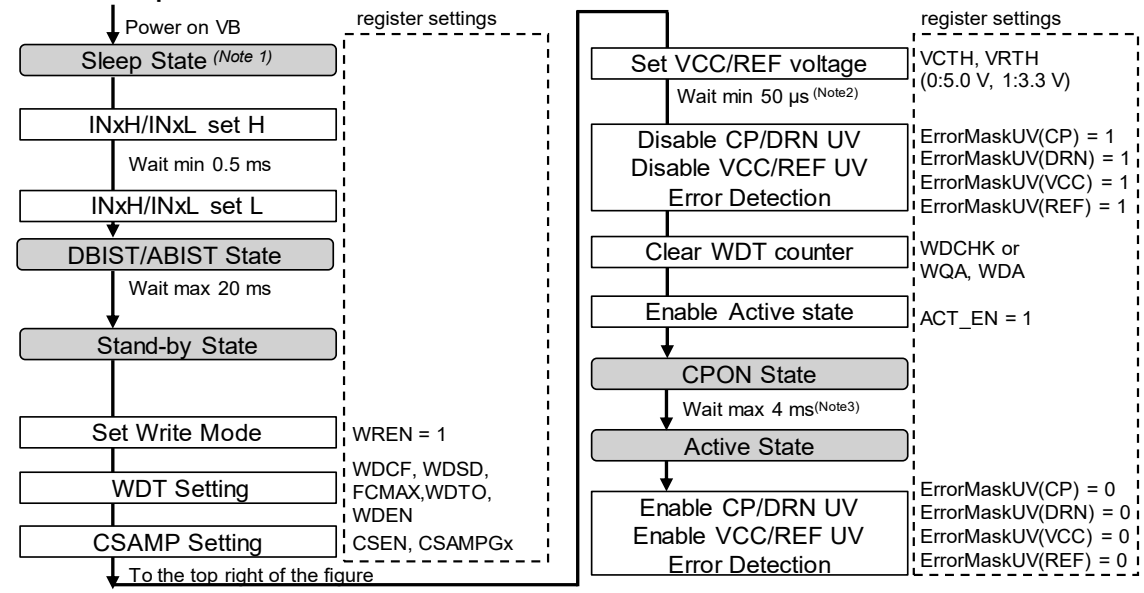
SLP_EN	Function
1	Change state to sleep.
0	Keep state

MCU cannot read error status in sleep state because IC is reset in the sleep state.
(Refer to 7.14 SPI Stop Detection and 7.3 Power Supply (VB/VDD/VCPH/VCPL) OV/UV and DRN UV Detection)

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1. IC State Description – Continued

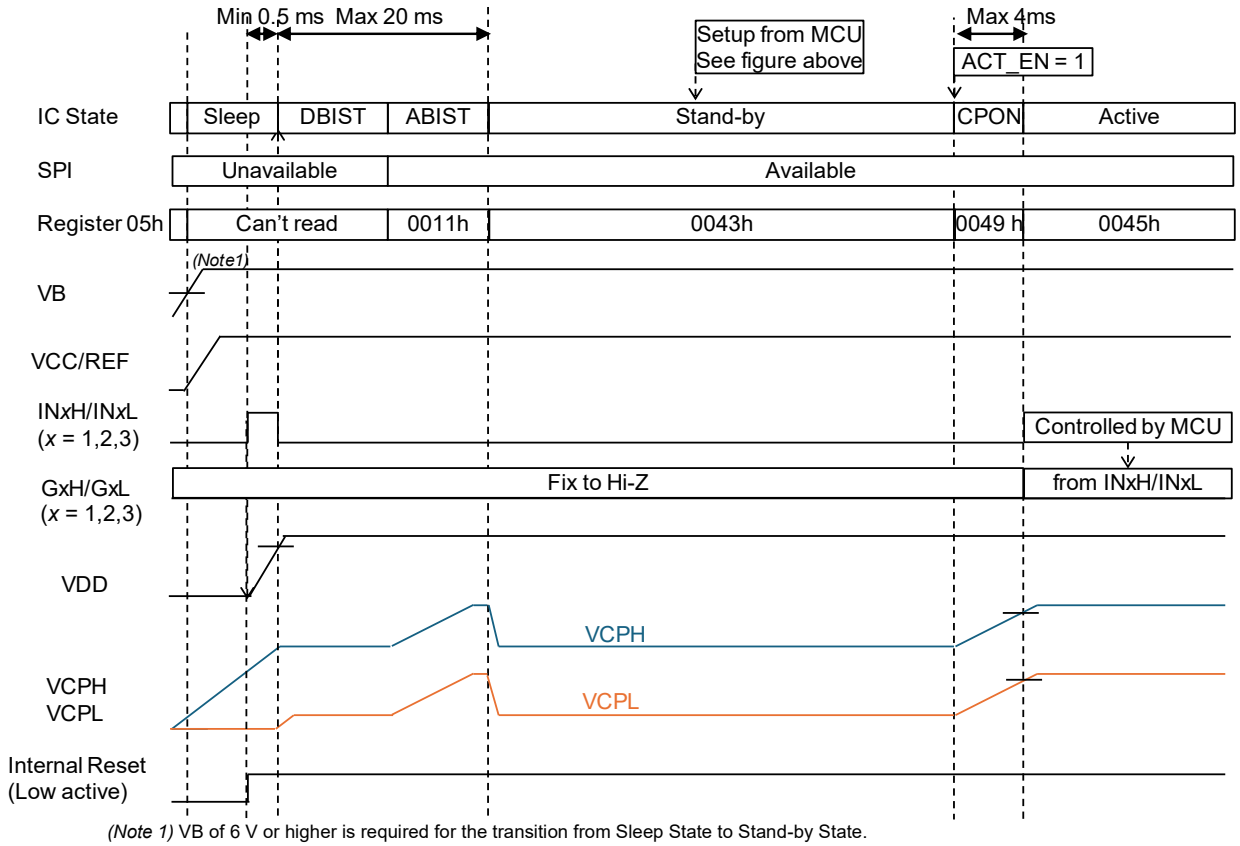
1.2 Power on sequence



(Note 1) VB of 6 V or higher is required for the transition from Sleep State to Stand-by State.
(Note 2) MCU must wait 50 µs for VCC/REF UV error detection to be enabled after setting VCC/REF voltage.
(Note 3) This time varies depending on the capacitance value used for VCPH/VCPL.

Figure 2. MCU action for power on sequence

Refer to 7.10 Watch Dog Timer (WDT) for WDT setting.
Refer to 5. Current Sense Amplifier (CSAMP) for CSAMP setting.



(Note 1) VB of 6 V or higher is required for the transition from Sleep State to Stand-by State.

Figure 3. Timing chart for power on sequence

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1. IC State Description – Continued

1.3 Power off sequence

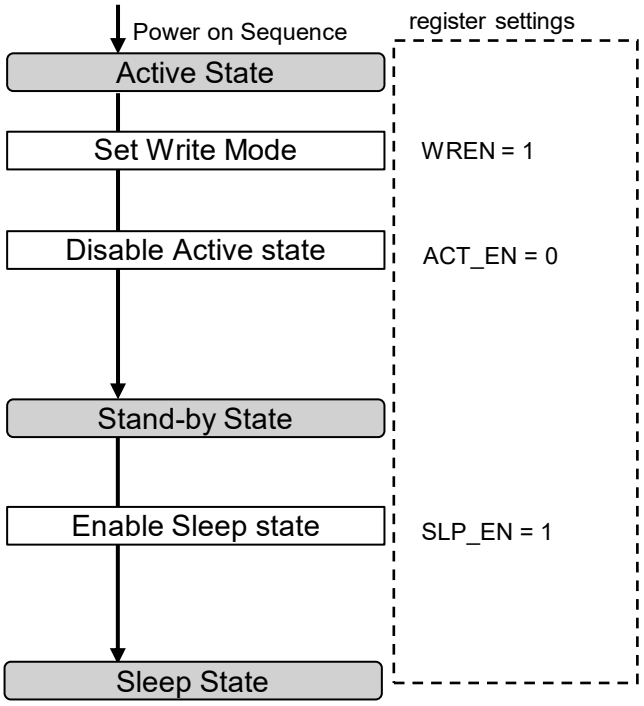


Figure 4. MCU action for power off sequence

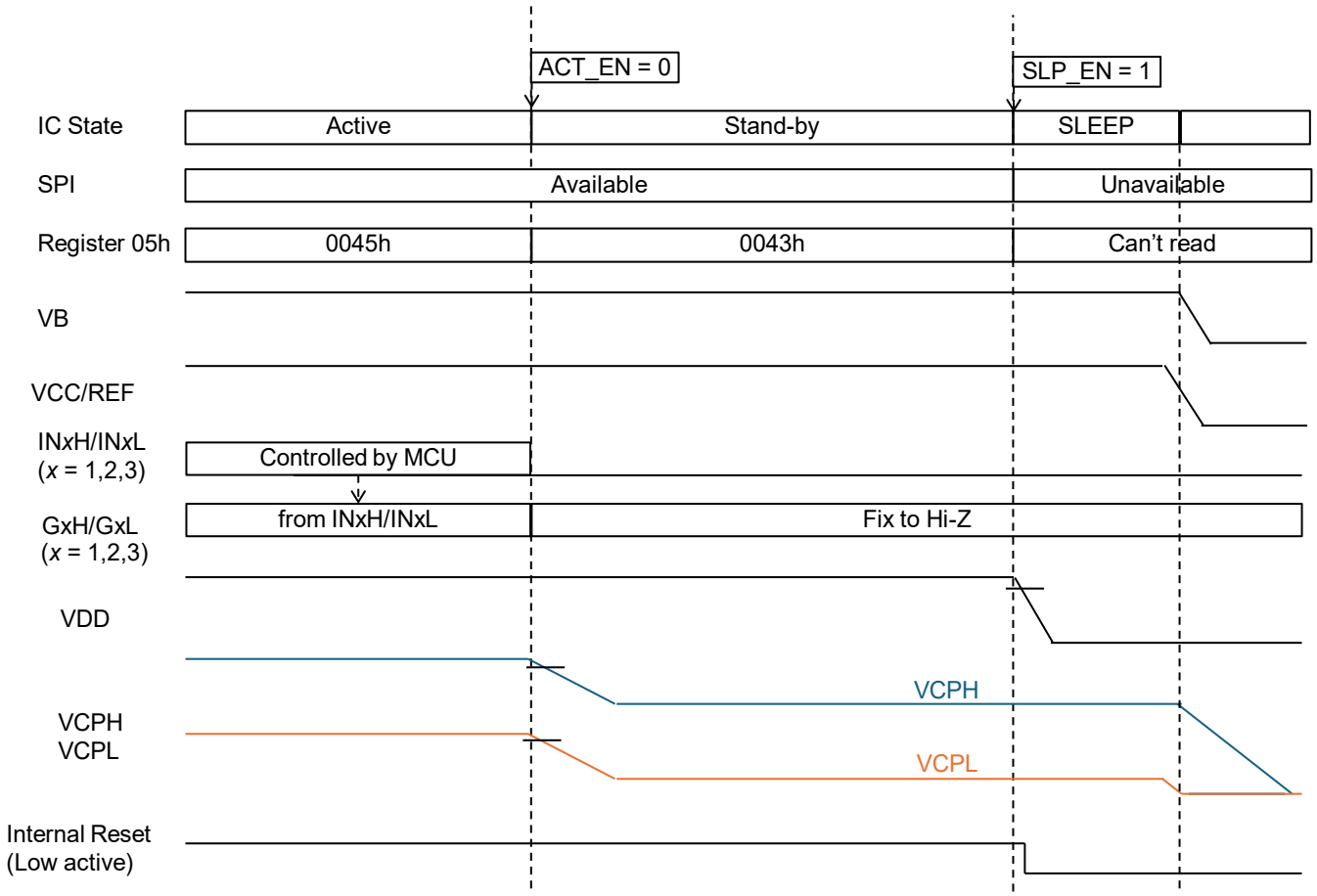


Figure 5. Timing Chart for Power Off Sequence

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2. MCU Interface

2.1 Serial Peripheral Interface (SPI) protocol

MCU can configure and control this IC, and it can read status of this IC via SPI. SPI access is available in ABIST, Stand-by, CPON, Active and FAIL state.

SPI consists of 4 signals: CSB, SCK, SDI and SDO/ERRB
CSB is a chip select. SCK is a serial clock. SDI is a serial data. SDO/ERRB is a data output and error status output. SPI communication is available only during CSB = Low. Data from SDI is latched to IC at the timing of rising edge of SCK. Data from SDO is output at the timing of falling edge of SCK.

SPI communication consists of 32bits per command. Each bit in SDI/SDO are defined below.

Data Type	Bit	Function
FC	2	Frame counter (FC). If FC value is equal to FC value in previous command, IC will ignore current command and assert SPI error. FC is reset by writing Register FCCLR = 1. Command after reset is accepted regardless of FC value.
ADR	5	Address for the register map (ADR).
WD	16	Data which is written to the register (WD).
RD	16	Data which is read from the register (RD).
CRC	8	In write access: MCU must calculate the CRC code using FC, ADR, and WD. And attach the CRC to the end of command. IC also executes the same calculation and compares the result with the CRC code generated by the MCU. If CRC codes are not equal, IC ignores this command and asserts SPI error. The register indicated by ADR is not updated. In read access: IC calculates the CRC code using FC, ADR and RD. And attach CRC at the bottom of command.
ERRB	1	Output error flag for error detections. L: Error, H: No Error.

SDO/ERRB signal can be changed by EREN register when CSB = H.
SDO/ERRB output control by EREN and CSB is shown in the table below.

EREN	CSB	
	Low period	High period
0	SPI communication	Hi-Z
1		ERRB (L: Error, H: No Error)

This IC has 3 kinds of registers by ADR. Access to them is controlled by WREN register.
Refer to 2.3 Register Map about assignment of kind by ADR.

Kind	Notation on Register map	WREN	
		0	1
Read only	R	Read access	
Write only	W	Write access	
Write or Read	W/R	Read access	Write access

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2. MCU Interface - Continued

Data format of SPI command is below.

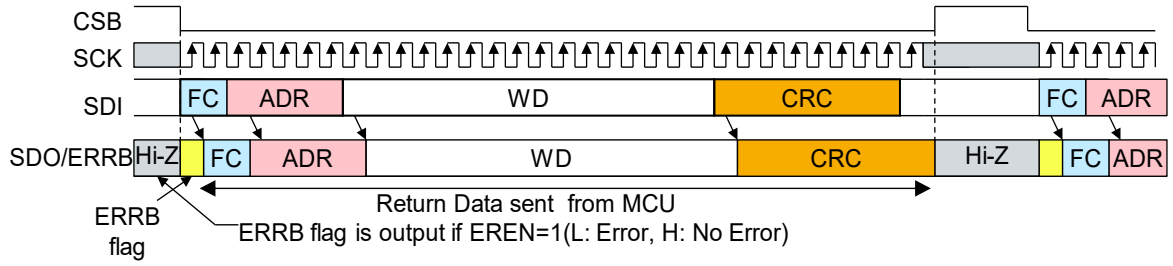


Figure 6. Data format for Write Access

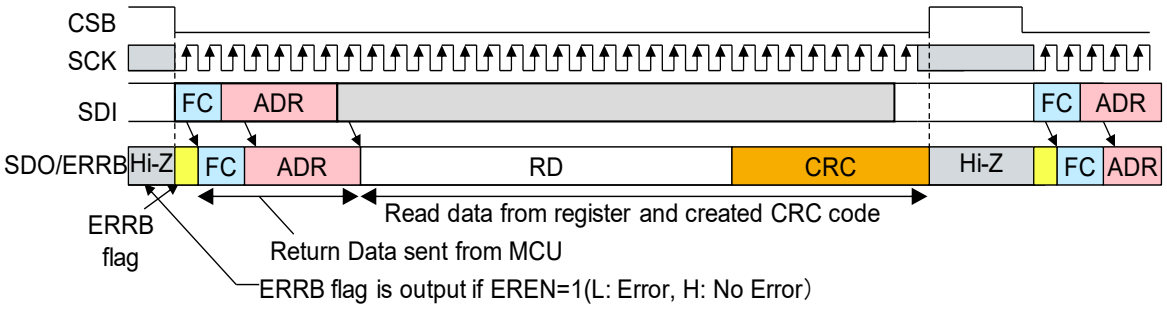


Figure 7. Data format for Read Access

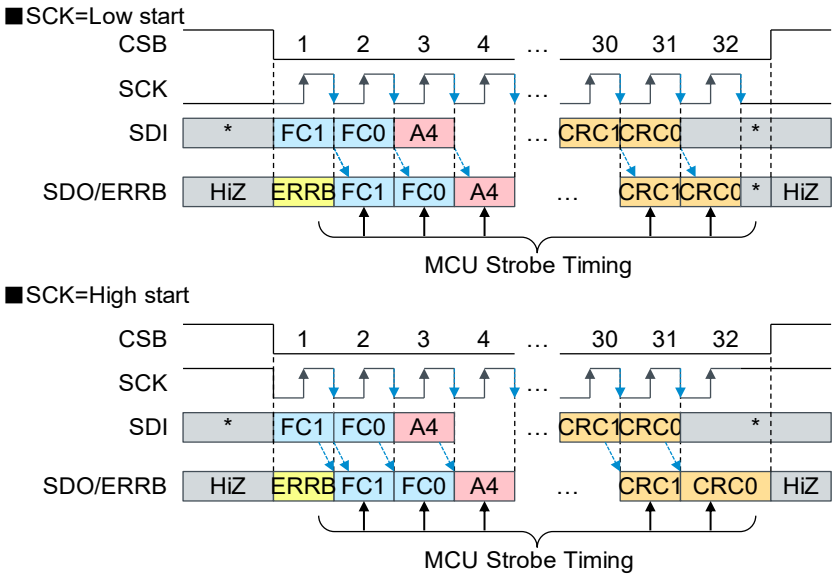


Figure 8. Support for SCK type in SPI communication

2.2 SPI CRC

The specifications of CRC used in SPI are as follows.

CRC Specification	
CRC result width	8bits
Polynomial	97h = $x^8 + x^7 + x^4 + x^2 + x^1 + 1$
Initial value	00h
Input data reflected	No
Result data reflected	No
XOR value	00h

Example:
When FC = 0, ADR = 01h, DATA = 0001h,
CRC result is F0h

When FC = 2, ADR = 0Ah, DATA = A865h,
CRC result is AAh

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2. MCU Interface - Continued

2.3 Register Map

The register map is shown in the table below.
Write 0 for Data in the gray area of the register map.
As for the W/R columns
R: Read only, W: Write only, W/R: Write and Read.

00h to 0Ch: Area 1

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	W/R / Default
00h	-				-				-				-			FCCLR	W / 0000h
01h	-				-				-				-			WREN	W / 0000h
02h	-				-				-				-			ACT_EN	W/R / 0000h
03h	-	-	OS_SEQ_MR1SH		OS_SEQ_PROP		OS_DETVTH		-				-			SLP_EN	W/R / 3B00h
04h	-			OSCHK					-				-			ER_CLR	W/R / 0000h
05h	-				-				Status FAIL	End BIST	End OS	Status ABIST	Status CPON	Status ACT	Status STB	Status ERRB	R / 0001h
06h	-				-			Error INTER	Error TSD	Error TW	Error WDT	Error SPI	Error REG	Error TDEAD	Error OSC	Error BIST	W/R / 0000h
07h	-	ErrorOV VB	ErrorOV VDD	ErrorOV VCC	ErrorOV REF	ErrorOV VCPH	ErrorOV VCPHG	ErrorOV VCPL	ErrorUV DRN	ErrorUV VB	-	ErrorUV VCC	ErrorUV REF	ErrorUV VCPH	ErrorUV VCPHD	ErrorUV VCPL	W/R / 0000h
08h	-	ErrorVDS 1H	ErrorVDS 2H	ErrorVDS 3H	ErrorVDS 1L	ErrorVDS 2L	ErrorVDS 3L	ErrorVGS 1R	ErrorVGS 2R	ErrorVGS 3R	ErrorVGS 1H	ErrorVGS 2H	ErrorVGS 3H	ErrorVGS 1L	ErrorVGS 2L	ErrorVGS 3L	W/R / 0000h
09h	-	ErrorShort MB	ErrorShort MG	ErrorShort PR	ErrorShort 1R	ErrorShort 2R	ErrorShort 3R	ErrorShort 1H	ErrorShort 2H	ErrorShort 3H	ErrorShort 1L	ErrorShort 2L	ErrorShort 3L	ErrorShort2 1L	ErrorShort2 2L	ErrorShort2 3L	W/R / 0000h
0Ah	ErrorSNT 1L	ErrorSNT 2L	ErrorSNT 3L	ErrorOpen PR	ErrorOpen 1R	ErrorOpen 2R	ErrorOpen 3R	ErrorOpen 1H	ErrorOpen 2H	ErrorOpen 3H	ErrorOpen 1L	ErrorOpen 2L	ErrorOpen 3L	ErrorOpen2 1L	ErrorOpen2 2L	ErrorOpen2 3L	W/R / 0000h
0Bh	-				-			WDTFC				WDQ					R / 0000h
0Ch	CRCR																R / 0000h

0Dh to 1Bh: Area 2

Addr.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	W/R / Default
0Dh	WDCF					WDSD					FCMAX		WDTO		WDEN		W/R / 0000h
0Eh	-				WDAS		-	WDCHK	WDA								W/R / 0000h
0Fh	-	ErrorMaskSNT 1L	ErrorMaskSNT 2L	ErrorMaskSNT 3L	ErrorMaskVDS 1HL	ErrorMaskVDS 2HL	ErrorMaskVDS 3HL	ErrorMaskVGS 1R	ErrorMaskVGS 2R	ErrorMaskVGS 3R	ErrorMaskVGS 1H	ErrorMaskVGS 2H	ErrorMaskVGS 3H	ErrorMaskVGS 1L	ErrorMaskVGS 2L	ErrorMaskVGS 3L	W/R / 0000h
10h	-				-				-		ErrorMaskShort 1H	ErrorMaskShort 2H	ErrorMaskShort 3H	ErrorMaskShort 1L	ErrorMaskShort 2L	ErrorMaskShort 3L	W/R / 0000h
11h	ErrorMask SPIST	ErrorMask OSC	-		-				-		ErrorMaskOpen 1H	ErrorMaskOpen 2H	ErrorMaskOpen 3H	ErrorMaskOpen 1L	ErrorMaskOpen 2L	ErrorMaskOpen 3L	W/R / 0000h
12h	ErrorMask TSD	ErrorMask TW	ErrorMask WDT	ErrorMask SPI	ErrorMask REG	ErrorMask TDEAD	ErrorMaskOV VB	ErrorMaskOV VDD	ErrorMaskOV VCC	ErrorMaskOV REF	ErrorMaskOV CP	ErrorMaskUV DRN	ErrorMaskUV VB	ErrorMaskUV VCC	ErrorMaskUV REF	ErrorMaskUV CP	W/R / 00C6h
13h	ErrorOutEn TSD	ErrorOutEn TW	ErrorOutEn WDT	ErrorOutEn SPI	ErrorOutEn REG	ErrorOutEn TDEAD	ErrorOutEnOV VB	ErrorOutEnOV VDD	ErrorOutEnOV VCC	ErrorOutEnOV REF	ErrorOutEnOV CP	ErrorOutEnUV DRN	ErrorOutEnUV VB	ErrorOutEnUV VCC	ErrorOutEnUV REF	ErrorOutEnUV CP	W/R / FFFFh
14h	ErrorOutEn Short	ErrorOutEn Open	ErrorOutEn VDS	ErrorOutEn SNT	ErrorOutEn VGS	ErrorOutEn VGSR	ProtectMode DRN	ProtectMode SPI	ProtectMode SNT	ProtectMode VDS	ProtectMode VGSR	ProtectMode VGS	ProtectMode VB	ProtectMode OS	EREN		W/R / FC10h
15h	ProtectKeep TSD	ProtectKeep Short	ProtectKeep Open	ProtectKeep VDS	ProtectKeep SNT	ProtectKeep VGS	ProtectKeep VGSR	ProtectKeepOV VB	ProtectKeepOV VDD	ProtectKeepOV VCC	ProtectKeepOV REF	ProtectKeepUV DRN	ProtectKeepUV VB	ProtectKeepUV VCC	ProtectKeepUV REF	-	W/R / 0000h
16h	-			DRN PD_EN	-		VRTH	VCTH	ROF HIZ	R1 OFF	R2 OFF	R3 OFF	GOF HIZ	G1 OFF	G2 OFF	G3 OFF	W/R / 0000h
17h	Reserved	-			TDEAD MD	TDEAD			CSAMPG3		CSAMPG2		CSAMPG1		-	CSEN	W/R / 0054h
18h	HSDRV_SRC				HSDRV_SNK				LSDRV_SRC				LSDRV_SNK				W/R / 8888h
19h	TVDS_FLT				TVDS_MSK				VDSL				VDSH				W/R / 41AAh
1Ah	TVGS_FLT			TVGS_MSK			TSNT_FLT			TSNT_MSK			VSNT				W/R / 860Ah
1Bh	CRCW																W/R / 0000h

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2. MCU Interface - Continued

2.4 Description of each bit in the register

The definition of each bit of the register is as follows.

00h: Write only registers

Symbol	Bit	Description
FCCLR	0	Frame Counter (FC) Reset. The frame counter is initialized by writing register FCCLR = 1. Command after reset is accepted regardless of FC value.

Refer to 2.1 Serial Peripheral Interface (SPI) protocol

01h: Write only registers

Symbol	Bit	Description
WREN	0	SPI Write enable. WREN influences W/R registers. 1: Write 0: Read

Refer to 2.1 Serial Peripheral Interface (SPI) protocol

02h: Write and Read registers

Symbol	Bit	Description
ACT_EN	0	Active Enable. 1: Transition from Stand-by state to Active state. 0: Transition from Active state to Stand-by state.

Refer to 1.1.3 From Stand-by to Active state

03h: Write and Read registers

Symbol	Bit	Description
OS_SEQ_MR1SH [1:0]	[13:12]	Period of Moter Relay Open/Short detection in Static OS Check.
OS_SEQ_PROP [1:0]	[11:10]	Period of Power Relay Open/Short detection in Static OS Check.
OS_DETVTH [1:0]	[9:8]	Thresh voltage between VB and DRN in Static OS Check.
SLP_EN	0	Sleep Enable. 1: Transition from Stand-by/Active state to Sleep state.

Refer to 7.8.1 Static OS Detection about OS_*
Refer to 1.1.4 From Some state to Sleep state about SLP_EN.

04h: Write and Read registers

Symbol	Bit	Description
OSCHK [4:0]	[12:8]	Static OS Check start register. If MCU read this register, this data is returned 0.
ERCLR	0	Error Clear. 1: Error detection registers can be cleared except Error (BIST) and Error (INTER). If MCU read this register, this data is returned 0.

Refer to 7.8.1 Static OS Detection about OSCHK.
Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification about ERCLR.

05h: Read only registers

Symbol	Bit	Description
State (FAIL)	7	State is in FAIL flag 1: FAIL state
End (BIST)	6	BIST complete flag 1: BIST is complete
End (OS)	5	Static Open / short check complete flag 1: Static OS check is complete. 0: No check static OS.
State (ABIST)	4	State is in ABIST flag 1: ABIST state
State (CPON)	3	State is in CPON flag 1: CPON state
State (ACT)	2	State is in Active flag 1: Active state
State (STB)	1	State is in Stand-by flag 1: Stand-by state
State (ERRB)	0	ERRB signal flag 1: No error, 0: Error has occurred.

Refer to 1.1 State Transition Diagram
Refer to 1.1.2 From Sleep to FAIL state about End (BIST).
Refer to 7.8.1 Static OS Detection about End (OS).

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2. MCU Interface – Continued

06h: Write and Read registers

Symbol	Bit	Description
Error (INTER)	8	Internal error 1: Error is detected. If MCU writes '1' in this bit, the status is not cleared to '0'.
Error (TSD)	7	TSD error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (TW)	6	TW error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (WDT)	5	WDT error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (SPI)	4	SPI error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (REG)	3	REG monitor error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (TDEAD)	2	Through-current prevention operation status: 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (OSC)	1	OSC error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
Error (BIST)	0	BIST error (common to ABIST error and DBIST error) 1: Error is detected. If MCU writes '1' in this bit, the status is not cleared to '0'.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

07h: Write and Read registers

Symbol	Bit	Description
ErrorOV (VB)	14	VB OV Error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOV (VDD)	13	VDD OV Error. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOV (VCC)	12	VCC OV Error. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOV (REF)	11	REF OV Error. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOV (VCPH)	10	VCPH-VB OV Error. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOV (VCPHG)	9	VCPH-GND OV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOV (VCPL)	8	VCPL-GND OV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (DRN)	7	DRN UV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (VB)	6	VB UV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (VCC)	4	VCC UV error. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (REF)	3	REF UV error. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (VCPH)	2	VCPH-VB UV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (VCPHD)	1	VCPH-DRN UV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorUV (VCPL)	0	VCPL-GND UV error 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification.

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2. MCU Interface - Continued

08h: Write and Read registers

Symbol	Bit	Description
ErrorVDS (1H)	14	VDS error in phase1 high-side drain-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVDS (2H)	13	VDS error in phase2 high-side drain-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVDS (3H)	12	VDS error in phase3 high-side drain-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVDS (1L)	11	VDS error in phase1 low-side drain-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVDS (2L)	10	VDS error in phase2 low-side drain-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVDS (3L)	9	VDS error in phase3 low-side drain-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (1R)	8	VGS error in phase1 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (2R)	7	VGS error in phase2 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (3R)	6	VGS error in phase3 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (1H)	5	VGS error in phase1 high-side gate-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (2H)	4	VGS error in phase2 high-side gate-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (3H)	3	VGS error in phase3 high-side gate-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (1L)	2	VGS error in phase1 low-side gate-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (2L)	1	VGS error in phase2 low-side gate-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorVGS (3L)	0	VGS error in phase3 low-side gate-source 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification.

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2. MCU Interface - Continued

09h: Write and Read registers

Symbol	Bit	Description
ErrorShort (MB)	14	Short Error between motor output and VB 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (MG)	13	Short Error between motor output and GND 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (PR)	12	Short Error in external FET for power relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (1R)	11	Short Error in external FET for phase1 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (2R)	10	Short Error in external FET for phase2 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (3R)	9	Short Error in external FET for phase3 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (1H)	8	Short Error in external FET for phase1 high-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (2H)	7	Short Error in external FET for phase2 high-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (3H)	6	Short Error in external FET for phase3 high-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (1L)	5	Short Error in external FET for phase1 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (2L)	4	Short Error in external FET for phase2 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort (3L)	3	Short Error in external FET for phase3 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort2 (1L)	2	Short Error in external FET for phase1 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort2 (2L)	1	Short Error in external FET for phase2 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorShort2 (3L)	0	Short Error in external FET for phase3 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification and 7.8 Open/Short (OS) Detection in External MOS-FET

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2. MCU Interface - Continued

0Ah: Write and Read registers

Symbol	Bit	Description
ErrorSNT (1L)	15	OV Error in external shunt register for phase1 circuit. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorSNT (2L)	14	OV Error in external shunt register for phase2 circuit. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorSNT (3L)	13	OV Error in external shunt register for phase3 circuit. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (PR)	12	Open Error in external FET for a power relay 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (1R)	11	Open Error in external FET for phase1 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (2R)	10	Open Error in external FET for phase2 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (3R)	9	Open Error in external FET for phase3 relay. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (1H)	8	Open Error in external FET for phase1 high-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (2H)	7	Open Error in external FET for phase2 high-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (3H)	6	Open Error in external FET for phase3 high-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (1L)	5	Open Error in external FET for phase1 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (2L)	4	Open Error in external FET for phase2 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen (3L)	3	Open Error in external FET for phase3 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen2 (1L)	2	Open Error in external FET for phase1 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen2 (2L)	1	Open Error in external FET for phase2 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.
ErrorOpen2 (3L)	0	Open Error in external FET for phase3 low-side gate. 1: Error is detected. If MCU writes '1' in this bit, the status is cleared to '0'.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification and 7.8 Open/Short (OS) Detection in External MOS-FET

0Bh: Read only registers

Symbol	Bit	Description
WDTFC [3:0]	[8:5]	WDT Fail Counter.
WDQ [4:0]	[4:0]	WDT Question Data.

Refer to 7.10 Watch Dog Timer (WDT).

0Ch: Read only registers

Symbol	Bit	Description
CRCR [15:0]	[15:0]	Register Monitor Internally calculated CRC

Refer to 7.11 Register (REG) Monitor

0Dh: Write and Read registers

Symbol	Bit	Description
WDCF [4:0]	[15:11]	WDT Config
WDSD [4:0]	[10:6]	WDT Timer Seed.
FCMAX [1:0]	[5:4]	WDT Fail Counter maximum value.
WDTO [1:0]	[3:2]	WDT detection period.
WDEN [1:0]	[1:0]	WDT function setting.

Refer to 7.10 Watch Dog Timer (WDT)

0Eh: Write and Read registers

Symbol	Bit	Description
WDAS [1:0]	[11:10]	WDT Answer setting.
WDCHK	8	WDT Check. WDT clear in Window mode and Time-Out mode. When "1" is written from MCU, WDT Counter is reset.
WDA [7:0]	[7:0]	WDT Answer. WDT clear in Q&A mode. When correct answer is written from MCU, WDT Counter is reset.

Refer to 7.10 Watch Dog Timer (WDT)

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2. MCU Interface - Continued

0Fh: Write and Read registers

Symbol	Bit	Description
ErrorMaskSNT (1L)	14	Mask SNT Error detection for phase1 circuit. 1: Disable detection. 0: Enable detection.
ErrorMaskSNT (2L)	13	Mask SNT Error detection for phase2 circuit. 1: Disable detection. 0: Enable detection.
ErrorMaskSNT (3L)	12	Mask SNT Error detection for phase3 circuit. 1: Disable detection. 0: Enable detection.
ErrorMaskVDS (1HL)	11	Mask VDS Error detection for phase1 gates. (Common to high and low-sides) 1: Disable detection. 0: Enable detection.
ErrorMaskVDS (2HL)	10	Mask VDS Error detection for phase2 gates. (Common to high and low-sides) 1: Disable detection. 0: Enable detection.
ErrorMaskVDS (3HL)	9	Mask VDS Error detection for phase3 gates. (Common to high and low-sides) 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (1R)	8	Mask VGS Error detection for phase1 relay. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (2R)	7	Mask VGS Error detection for phase2 relay. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (3R)	6	Mask VGS Error detection for phase3 relay. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (1H)	5	Mask VGS Error detection for phase1 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (2H)	4	Mask VGS Error detection for phase2 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (3H)	3	Mask VGS Error detection for phase3 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (1L)	2	Mask VGS Error detection for phase1 low-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (2L)	1	Mask VGS Error detection for phase2 low-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskVGS (3L)	0	Mask VGS Error detection for phase3 low-side gate. 1: Disable detection. 0: Enable detection.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

10h: Write and Read registers

Symbol	Bit	Description
ErrorMaskShort (1H)	5	Mask Short Error detection in external FET for phase1 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskShort (2H)	4	Mask Short Error detection in external FET for phase2 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskShort (3H)	3	Mask Short Error detection in external FET for phase3 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskShort (1L)	2	Mask Short Error detection in external FET for phase1 low-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskShort (2L)	1	Mask Short Error detection in external FET for phase2 low-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskShort (3L)	0	Mask Short Error detection in external FET for phase3 low-side gate. 1: Disable detection. 0: Enable detection.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

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2. MCU Interface - Continued

11h: Write and Read registers

Symbol	Bit	Description
ErrorMask (SPIST)	15	Mask SPI stop detection 1: Disable detection. 0: Enable detection.
ErrorMask (OSC)	14	Mask OSC Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskOpen (1H)	5	Mask Open Error in external FET for phase1 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskOpen (2H)	4	Mask Open Error in external FET for phase2 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskOpen (3H)	3	Mask Open Error in external FET for phase3 high-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskOpen (1L)	2	Mask Open Error in external FET for phase1 low-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskOpen (2L)	1	Mask Open Error in external FET for phase2 low-side gate. 1: Disable detection. 0: Enable detection.
ErrorMaskOpen (3L)	0	Mask Open Error in external FET for phase3 low-side gate. 1: Disable detection. 0: Enable detection.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

12h: Write and Read registers

Symbol	Bit	Description
ErrorMask (TSD)	15	Mask TSD Error detection. 1: Disable detection. 0: Enable detection.
ErrorMask (TW)	14	Mask TW Error detection. 1: Disable detection. 0: Enable detection.
ErrorMask (WDT)	13	Mask WDT Error detection. 1: Disable detection. 0: Enable detection.
ErrorMask (SPI)	12	Mask SPI Error detection. 1: Disable detection. 0: Enable detection.
ErrorMask (REG)	11	Mask REG monitor 1: Disable detection. 0: Enable detection.
ErrorMask (TDEAD)	10	Mask Shoot Through Error detection. 1: Disable detection. 0: Enable detection.
ErrorMaskOV (VB)	9	Mask VB OV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskOV (VDD)	8	Mask VDD OV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskOV (VCC)	7	Mask VCC OV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskOV (REF)	6	Mask REF OV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskOV (CP)	5	Mask Charge Pump OV Error detection. (Common to VCPH-VB OV, VCPH-GND OV and VCPL-GND OV Error) 1: Disable detection. 0: Enable detection.
ErrorMaskUV (DRN)	4	Mask DRN UV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskUV (VB)	3	Mask VB UV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskUV (VCC)	2	Mask VCC UV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskUV (REF)	1	Mask REF UV Error detection 1: Disable detection. 0: Enable detection.
ErrorMaskUV (CP)	0	Mask Charge Pump UV Error detection. (Common to VCPH-VB UV, VCPH-DRN UV and VCPL-GND UV Error) 1: Disable detection. 0: Enable detection.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

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2. MCU Interface - Continued

13h: Write and Read registers

Symbol	Bit	Description
ErrorOutEn (TSD)	15	Output TSD Error to SDO/ERRB. 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (TW)	14	Output TW Error to SDO/ERRB. 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (WDT)	13	Output WDT Error to SDO/ERRB. 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (SPI)	12	Output SPI Error to SDO/ERRB. 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (REG)	11	Output REG Monitor Error to SDO/ERRB. 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (TDEAD)	10	Output Short Through Prevention Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (VB)	9	Output VB OV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnOV (VDD)	8	Output VDD OV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnOV (VCC)	7	Output VCC OV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnOV (REF)	6	Output REF OV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnOV (CP)	5	Output Charge Pump OV Error to SDO/ERRB. (common to VCPH-VB OV, VCPH-GND OV and VCPL-GND OV Error) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnUV (DRN)	4	Output DRN UV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnUV (VB)	3	Output VB UV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnUV (VCC)	2	Output VCC UV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnUV (REF)	1	Output REF UV Error to SDO/ERRB 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEnUV (CP)	0	Output Charge Pump UV Error to SDO/ERRB. (common to VCPH-VB UV, VCPH-DRN UV and VCPL-GND UV Error) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

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2. MCU Interface - Continued

14h: Write and Read registers

Symbol	Bit	Description
ErrorOutEn (Short)	15	Output Short Error to SDO/ERRB. (common to all-phase & external FET) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (Open)	14	Output Open Error to SDO/ERRB. (common to all-phase & external FET) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (VDS)	13	Output VDS Error to SDO/ERRB. (common to all-phase & high/low-side) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (SNT)	12	Output SNT Error to SDO/ERRB. (common to all-phase) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (VGS)	11	Output VGS Error to SDO/ERRB. (common to all-phase & high/low-side) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ErrorOutEn (VGSR)	10	Output VGSR Error to SDO/ERRB. (common to all-phase) 1: output Error to SDO/ERRB. 0: stop Error to SDO/ERRB.
ProtectMode (DRN)	9	Disable Protection of DRN UV Error. 0: Enable protection. 1: Disable Protection.
ProtectMode (SPI)	8	Disable Protection of SPI Error. 0: Enable protection. 1: Disable Protection.
ProtectMode (SNT)	7	Disable Protection of SNT Error. (common to all-phase) 0: Enable protection. 1: Disable Protection.
ProtectMode (VDS)	6	Disable Protection of VDS Error. (common to all-phase & high/low-side) 0: Enable protection. 1: Disable Protection.
ProtectMode (VGSR)	5	Disable Protection of VGSR Error. (common to all-phase) 0: Enable protection. 1: Disable Protection.
ProtectMode (VGS) [1:0]	[4:3]	Protection Mode of VGS Error. (common to all-phase) 0: Enable protection. And Gate driver output to Low when VGS OV/UV error. 1: Enable protection. And Gate driver output to Hi-Z when VGS OV/UV error. 2: Enable protection. And Gate driver output to Low when VGS UV error. When VGS OV error at H-side, GxH is Hi-Z and GxL is Low. When VGS OV error at L-side, GxH is Low and GxL is Hi-Z. 3: Disable Protection.
ProtectMode (VB)	2	Protection Mode of VB Error. (common to OV/UV) 0: Enable protection. And Gate driver output to Short Brake. 1: Enable protection. And Gate driver output to signal selected by GOFHIZ.
ProtectMode (OS)	1	Disable Protection of OS Error in dynamic mode. (common to Short & Open) OS Error in static mode is not used protection. 0: Enable protection. 1: Disable Protection.
EREN	0	Enable ERRB in SDO 1: Enable ERRB. SDO/ERRB output “ERRB” during CSB = H. 0: Disable ERRB. SDO/ERRB output Hi-Z during CSB = H.

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification about ErrorOutEn(*)
Refer to 7.1 Protection After Error Detection about ProtectMode(*)
Refer to 2.1 Serial Peripheral Interface (SPI) protocol about EREN

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2. MCU Interface - Continued

15h: Write and Read registers

Symbol	Bit	Description
ProtectKeep (TSD)	15	Keep TSD Error 1: Keep on Error, 0: Output Error as it is
ProtectKeep (Short)	14	Keep Short Error (common to all-phase) 1: Keep on Error, 0: Output Error as it is
ProtectKeep (Open)	13	Keep Open Error (common to all-phase) 1: Keep on Error, 0: Output Error as it is
ProtectKeep (VDS)	12	Keep VDS Error (common to all-phase & high/low-side) 1: Keep on Error, 0: Output Error as it is
ProtectKeep (SNT)	11	Keep SNT Error (common to all-phase) 1: Keep on Error, 0: Output Error as it is
ProtectKeep (VGS)	10	Keep VGS Error (common to all-phase & high/low-side) 1: Keep on Error, 0: Output Error as it is
ProtectKeep (VGSR)	9	Keep VGSR Error (common to all-phase) 1: Keep on Error, 0: Output Error as it is
ProtectKeepOV (VB)	8	Keep VB OV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepOV (VDD)	7	Keep VDD OV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepOV (VCC)	6	Keep VCC OV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepOV (REF)	5	Keep REF OV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepUV (DRN)	4	Keep DRN UV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepUV (VB)	3	Keep VB UV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepUV (VCC)	2	Keep VCC UV Error 1: Keep on Error, 0: Output Error as it is
ProtectKeepUV (REF)	1	Keep REF UV Error 1: Keep on Error, 0: Output Error as it is

Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification

16h: Write and Read registers

Symbol	Bit	Description
DRN_PD_EN	12	Pull Down for DRN. 1: Enable, 0: Disable
VRTH	9	REF voltage detection threshold. 0: For 5.0 V, 1: For 3.3 V.
VCTH	8	VCC voltage detection threshold. 0: For 5.0 V, 1: For 3.3 V.
ROFHIZ	7	Relay driver output OFF state selection when RxOFF = ’1’ (x = 1,2,3). 0: Low, 1: Hi-Z
R1OFF	6	Relay driver GR1 ON/OFF 0: ON. Output to High. 1: OFF. Output to signal selected by ROFHIZ.
R2OFF	5	Relay driver GR2 ON/OFF. 0: ON. Output to High. 1: OFF. Output to signal selected by ROFHIZ.
R3OFF	4	Relay driver GR3 ON/OFF. 0: ON. Output to High. 1: OFF. Output to signal selected by ROFHIZ.
GOFHIZ	3	Gate drive output OFF state selection in occurring errors or GxOFF = ’1’ (x = 1,2,3). 0: Low, 1: Hi-Z
G1OFF	2	Gate driver G1H/G1L ON/OFF. 0: ON. Output to IN1H/IN1L, 1: OFF. Output to signal selected by GOFHIZ.
G2OFF	1	Gate driver G2H/G2L ON/OFF. 0: ON. Output to IN2H/IN2L, 1: OFF. Output to signal selected by GOFHIZ.
G3OFF	0	Gate driver G3H/G3L ON/OFF. 0: ON. Output to IN3H/IN3L, 1: OFF. Output to signal selected by GOFHIZ.

Refer to 7.8.1 Static OS Detection about DRN_PD_EN.
Refer to 7.4 Reference Voltage (VCC/REF) OV/UV Detection about VRTH and VCTH.
Refer to 6. Relay Driver about ROFHIZ and RxOFF.
Refer to 4.1 Gate ON/OFF Control about GOFHIZ and GxOFF.

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2. MCU Interface - Continued

17h: Write and Read registers

Symbol	Bit	Description
Reserved	15	Set '0'
TDEADMD	11	Dead time mode. 0: Using switching timing of INxH/INxL (x = 1,2,3) 1: Using Gate off level detection timing.
TDEAD [2:0]	[10:8]	Dead time period.
CSAMPG3 [1:0]	[7:6]	CSAMP Gain for phase3 circuit.
CSAMPG2 [1:0]	[5:4]	CSAMP Gain for phase2 circuit.
CSAMPG1 [1:0]	[3:2]	CSAMP Gain for phase1 circuit.
CSEN	0	CSAMP Enable 1: Enable, 0: Disable.

Refer to 4.2 Shoot Through Prevention and Detection (TDEAD) about TDEADMD and TDEAD.
Refer to 5. Current Sense Amplifier (CSAMP) about CSAMPGx and CSEN

18h: Write and Read registers

Symbol	Bit	Description
HSDRV_SRC [3:0]	[15:12]	Source current setting for gate drive of high-side FET.
HSDRV_SNK [3:0]	[11:8]	Sink current setting for gate drive of high-side FET.
LSDRV_SRC [3:0]	[7:4]	Source current setting for gate drive of low-side FET.
LSDRV_SNK [3:0]	[3:0]	Sink current setting for gate drive of low-side FET.

Refer to 4.3 Output Current Setting

19h: Write and Read registers

Symbol	Bit	Description
TVDS_FLT [3:0]	[15:12]	Filter period setting after VDS voltage abnormality detection.
TVDS_MSK [3:0]	[11:8]	Mask period setting for VDS voltage abnormality detection.
VDSL [3:0]	[7:4]	VDS voltage abnormality detection threshold setting for low-side FET
VDSH [3:0]	[3:0]	VDS voltage abnormality detection threshold setting for high-side FET

Refer to 7.6 Drain-Source voltage (VDS) Error Detection

1Ah: Write and Read registers

Symbol	Bit	Description
TVGS_FLT [2:0]	[15:13]	Filter period setting after VGS voltage abnormality detection.
TVGS_MSK [2:0]	[12:10]	Mask period setting for VGS voltage abnormality detection.
TSNT_FLT [2:0]	[9:7]	Filter period setting of shunt resistor voltage error detection._
TSNT_MSK [2:0]	[6:4]	Mask period setting for shunt resistor voltage error detection._
VSNT [3:0]	[3:0]	Shunt resistor voltage anomaly detection threshold setting.

Refer to 7.5 Gate-Source voltage (VGS) Error Detection about TVGS_ *
Refer to 7.7 Shunt Resister Voltage (SNT) Error Detection about TSNT_* and VSNT

1Bh: Write and Read registers

Symbol	Bit	Description
CRCW [15:0]	[15:0]	Register Monitor CRC from MPU

Refer to 7.11 Register (REG) Monitor

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3. LDO

A power supply circuit that generates VDD for internal circuits and VCPH and VCPL for gate control of external FETs from VB input is built in. The voltage relationship is shown in the figure below. (Voltage values are typical).

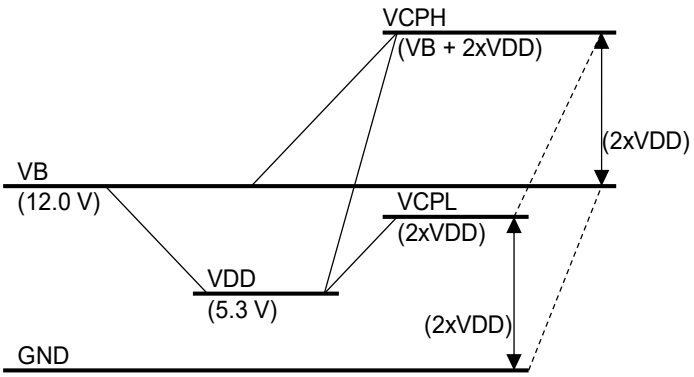


Figure 9. Voltage relationship

3.1 VDD: Power Supply for Internal Circuit

Power supply voltage for internal circuits is generated.
Connect a 1 µF to 4.7 µF capacitor between VDD and GND pins to stabilize the voltage.

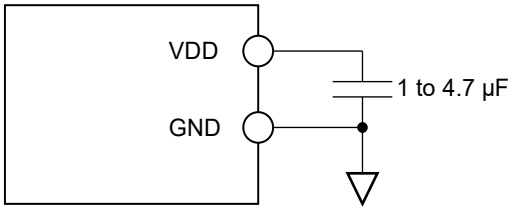


Figure 10. Capacitor for VDD

3.2 VCPH/VCPL: Power Supply for Gate Driving Circuit of External MOS-FET

VCPH is the ON-voltage level of the external high-side MOS-FET gate drive output (G1H/G2H/G3H) and VCPL is the ON-voltage level of the external low-side MOS-FET gate drive output (G1L/G2L/G3L).
Please attach 0.47 µF between CP1H-CP1L and between CP2H-CP2L. And please attach 1.0 µF /4.7 µF to VCPH/VCPL to stable output voltage.

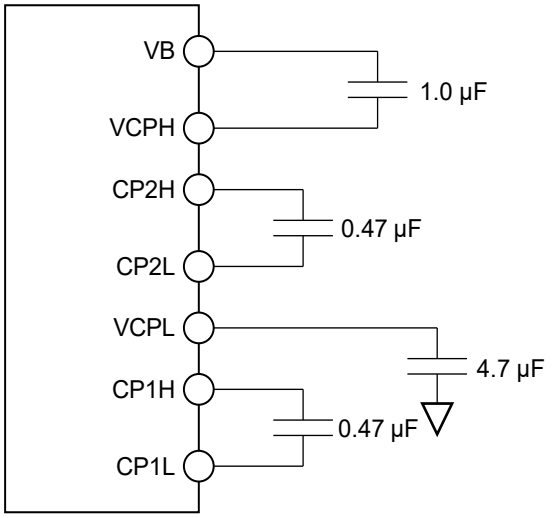


Figure 11. Capacitor for VCPH/VCPL

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4. Gate Driver

4.1 Gate ON/OFF Control

Gate driving output (G1H/G2H/G3H/G1L/G2L/G3L) is directly controlled by IN1H/IN1L/IN2H/IN2L/IN3H/IN3L input signals. IC provides dead-time control to prevent shoot-through at the half bridge caused by turning on both the high-side and low-side MOSFETs.

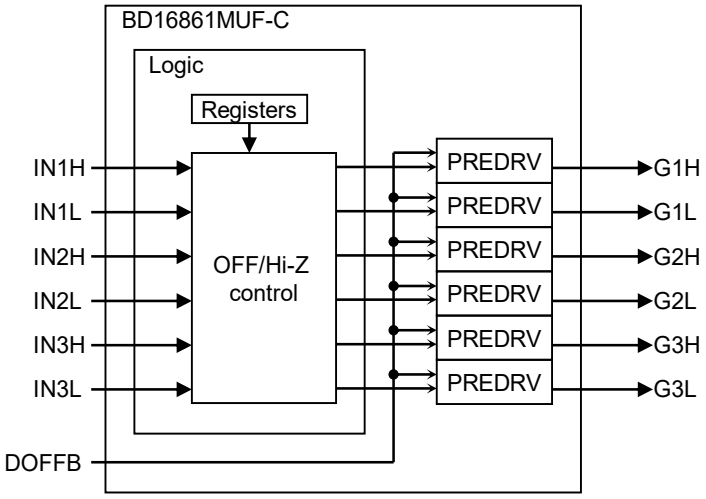


Figure 12. Block diagram

There are 4 output types in Gate Control state.

Output Type	Function
Normal	GxH is controlled by INxH and GxL is controlled by INxL.
LOW	GxH and GxL are low level. External high-side and low-side MOS-FET are OFF
Hi-Z	GxH are pulled down to SxH and GxL are pulled down to SxL.
Short Brake (SB)	GxH are low and GxL are high. External high-side MOS-FET are OFF, and low-side MOS-FET are ON

(x = 1,2,3)

There is another method to control Gate Driver by a pin DOFFB and GxOFF registers (x = 1,2,3).
When DOFFB is toggled from L to H, first set INxH / INxL input signals to L.
IC can fix the gate level of external MOS-FET to low or Hi-Z by GxOFF register. This fixing level can be selected by a register GOFHIZ. DOFFB directly controls the gate driver without internal control logic.

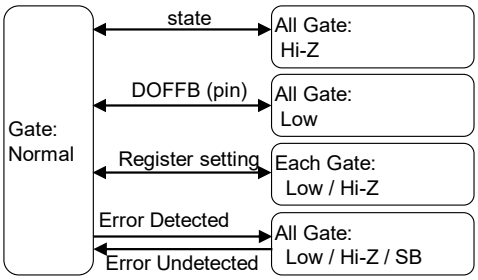


Figure 13. State in Gate Driver

State	Input	Register		Input		Output	
	DOFFB	GxOFF	GOFHIZ	INxH	INxL	GxH	GxL
Active	H	0	*	L	L	LOW	LOW
					H		HIGH
				H	L	HIGH	LOW
					H	LOW *(Note 1)*	LOW *(Note 1)*
		1	0	*	*	LOW	LOW
			1			Hi-Z	Hi-Z
	L	*	*			LOW	LOW
Others	*					Hi-Z	Hi-Z

(Note 1) If both INxH and INxL are high, force to low. (x = 1,2,3)

Refer to 7.1 Protection After Error Detection about gate control by Error detection.

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4. Gate Driver - Continued

4.2 Shoot Through Prevention and Detection (TDEAD)

This IC inserts a dead time to prevent shoot-through caused by the simultaneous turn-on of the high-side and low-side MOSFETs in each phase half bridge. Dead time is inserted as 'off period' when high-side and low-side gate control input are both high at the same time, or when 'off period' is shorter than a dead time which is set by TDEAD register.
In other case, 'off period' generated by INxH/INxL (x = 1,2,3) is used.
This function has 2 modes by TDEADMD register.

TDEADMD	Description
0	The dead time counter starts at the falling edge of INxH / INxL.
1	The dead time counter starts at the point where GxH / GxL falls and reaches the gate-off level defined by the VGS detection circuit.

Dead time can be selected by TDEAD register (f_{OSC} = 10.7 MHz (Typ))

TDEAD [2:0]	Dead time (t_{DEAD})	TDEAD [2:0]	Dead time (t_{DEAD})
0	0 ns	4	4 / f_{OSC}
1	1 / f_{OSC}	5	5 / f_{OSC}
2	2 / f_{OSC}	6	6 / f_{OSC}
3	3 / f_{OSC}	7	7 / f_{OSC}

This delay time is generated by re-timing internal clock. So, range of t_{DEAD} has 1 cycle of fluctuations.

If this function is inserted dead time, Error (TDEAD) set 1.

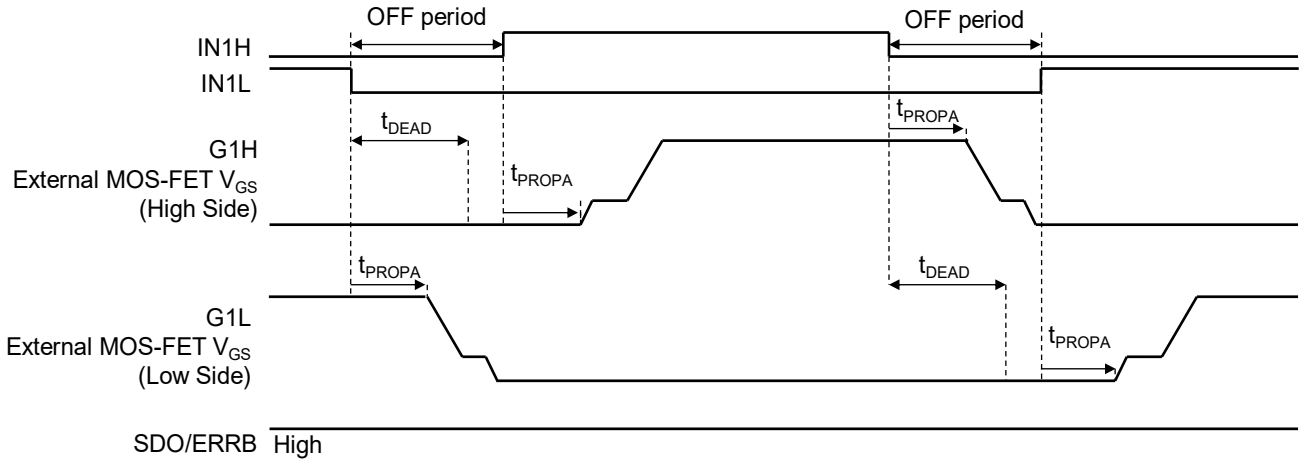
Error (TDEAD)	Function
0	Not insert dead time.
1	Insert dead time.

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4. Gate Driver - Continued

Timing Chart in TDEADMD = 0

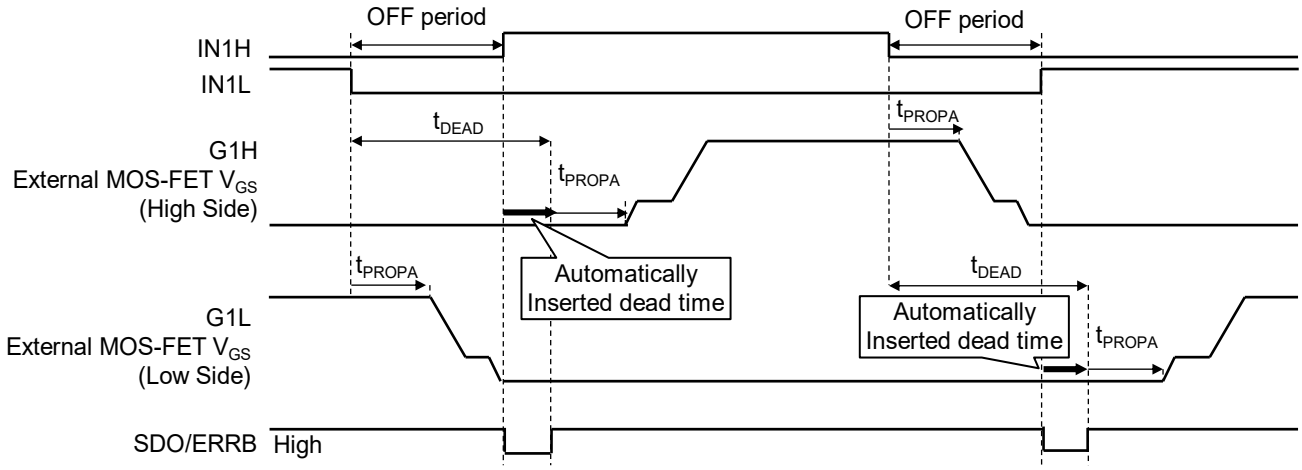
(A) OFF period >= t_{DEAD}



When "OFF period" is longer than t_{DEAD}, ERROR(TDEAD)='0',
Gate turns on as the input changes low to high

Figure 14. Timing Chart in TDEADMD = 0 and case (A)

(B) OFF period < t_{DEAD}



When "OFF period" is shorter than t_{DEAD}, ERROR(TDEAD)='1',
Automatically insert t^{DEAD} as shown in the figure.

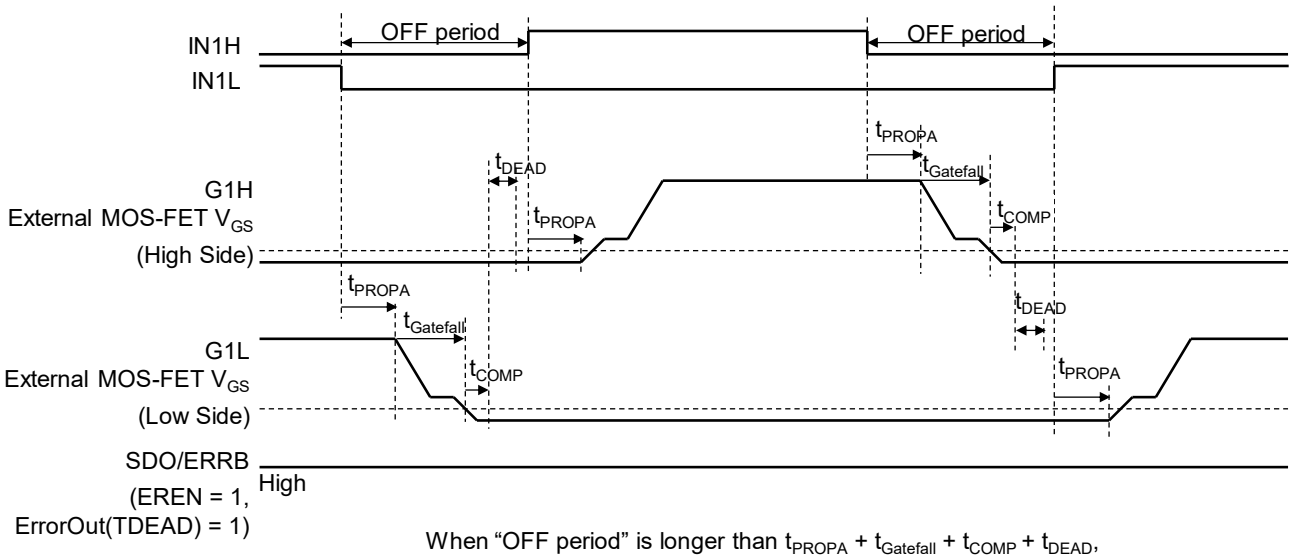
Figure 15. Timing Chart in TDEADMD = 0 and case (B)

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4. Gate Driver - Continued

Timing Chart in TDEADMD = 1

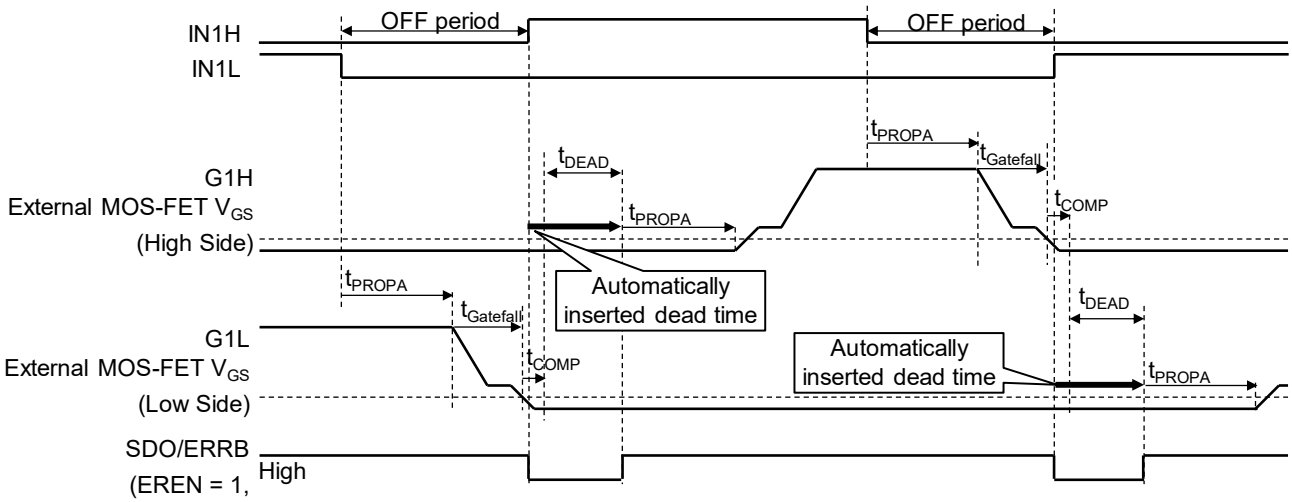
(A) OFF period >= t_{PROPA} + $t_{Gatefall}$ + t_{COMP} + t_{DEAD}



When "OFF period" is longer than t_{PROPA} + $t_{Gatefall}$ + t_{COMP} + t_{DEAD},
ERROR(TDEAD) = '0', Gate turns on as the input changes low to high.

Figure 16. Timing Chart in TDEADMD = 1 and case (A)

(B) OFF period < t_{PROPA} + $t_{Gatefall}$ + t_{COMP} + t_{DEAD}



When "OFF period" is shorter than t_{PROPA} + $t_{Gatefall}$ + t_{COMP} + t_{DEAD},
ERROR(TDEAD) = '1', t_{DEAD} is automatically inserted as shown in the figure.

Figure 17. Timing Chart in TDEADMD = 1 and case (B)

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4. Gate Driver - Continued

4.3 Output Current Setting

MCU can select Source current and Sink current of gate driving for external MOS-FET (G1H/G2H/G3H and G1L/G2L/G3L) via SPI. The setting is common in all three phases.

Source current setting for Gate driving
- HSDRV_SRC [3:0]: High-side MOS-FET
- LSDRV_SRC [3:0]: Low-side MOS-FET

HSDRV_SRC [3:0] LSDRV_SRC [3:0]	Source current (mA)
0h	75
1h	100
2h	125
3h	150
4h	175
5h	200
6h	300
7h	400
8h	500
9h	600
Ah	700
Bh	800
Ch	900
Dh	1000
Eh	1100
Fh	1200

Sink current setting for Gate driving
- HSDRV_SNK [3:0]: High-side MOS-FET
- LSDRV_SNK [3:0]: Low-side MOS-FET

HSDRV_SNK [3:0] LSDRV_SNK [3:0]	Sink current (mA)
0h	75
1h	100
2h	125
3h	150
4h	175
5h	200
6h	300
7h	400
8h	500
9h	600
Ah	700
Bh	800
Ch	900
Dh	1000
Eh	1100
Fh	1200

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5. Current Sense Amplifier (CSAMP)

A current sensing amplifier is built in to detect the current through the shunt resistor.
The gain can be set by registers. The reference voltage can be set by the input voltage from the REF pin.
The output voltage of the current detection amplifier is expressed by the following equation.

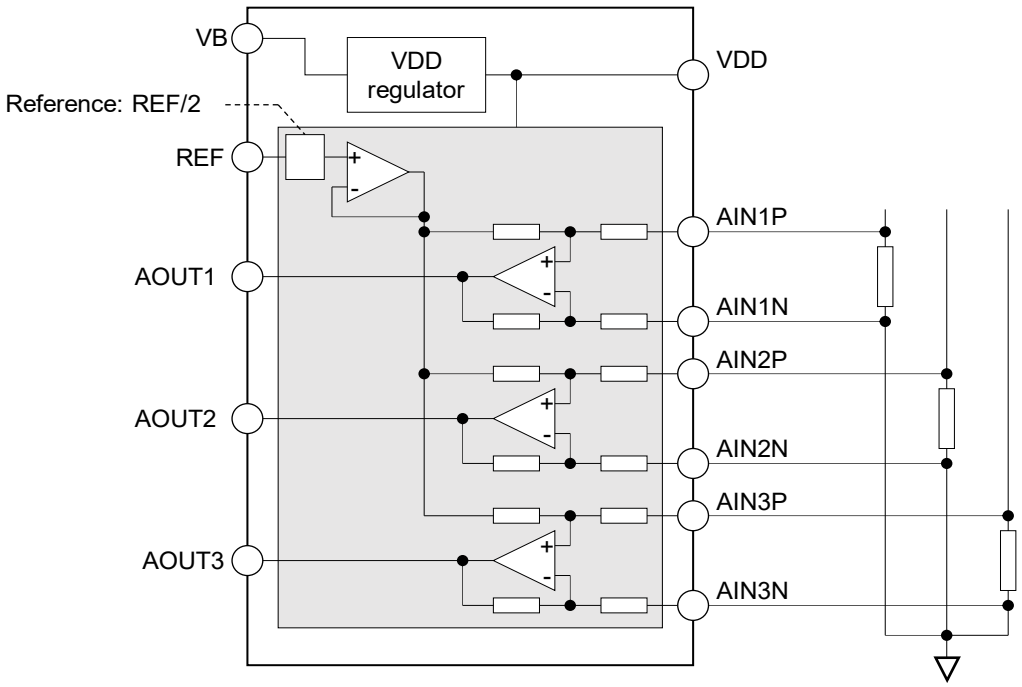


Figure 18. Block diagram in CSAMP

5.1 Current Sense Amplifier Setting

A register CSEN is an enabling register of CSAMP. If MCU sets CSEN to '0', power consumption can be reduced.
Registers CSAMPGx (x = 1,2,3) are to set gain of each AMP.

CSAMPGx [1:0]	AOUTx gain setting GAIN
0	12
1	16
2	24
3	32

Output AOUTx (x = 1,2,3) in Status and CSEN is below.

State	Register	CSAMP
	CSEN	AOUTx
Active	1	(AINxP – AINxN) * GAIN + REF/2
	0	Hi-Z
Others	*	

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6. Relay Driver

This IC has relay drivers (GRx (x = 1,2,3)) to control external MOS-FETs for motor relay.

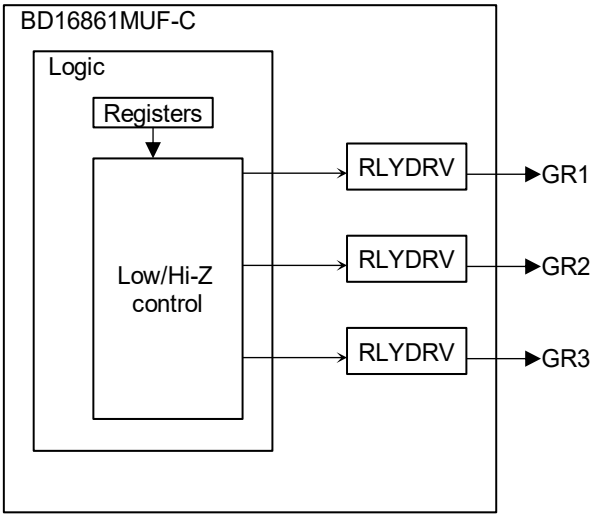


Figure 19. Block diagram

There are 3 output types in Relay Control state.

Output Type	Function
HIGH	GRx are high level.
LOW	GRx are low level.
Hi-Z	GRx are Hi-Z.

They can be turned on / off by R1OFF/R2OFF/R3OFF registers.
And the off state (LOW or Hi-Z) can be selected ROFHIZ register.

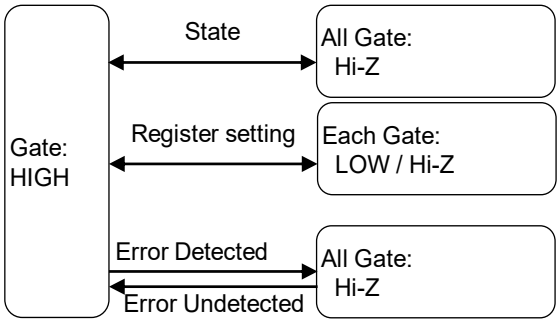


Figure 20. State in Relay Driver

State	Register		Output
	RxOFF	ROFHIZ	GRx
Active	0	*	HIGH
	1	0	LOW
		1	Hi-Z
Others	*	*	

Refer to 7.1 Protection After Error Detection about relay control by Error detection.

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7. Protection Function

This IC has various error detections such as an over / Undervoltage error for externally applied power supply (VB, VCC, REF) and internally generated power supply (VDD, VCPL, VCPH), and open / short detection for external FETs. And it also has protection functions to prevent it from a system destruction. When these errors are detected, IC notifies MCU by SDO/ERRB at the same time of the protection process. The detected error information is stored registers in IC and MCU can read it via SPI.

OV: Overvoltage, UV: Undervoltage

Error Detection Function			Detected Errors	Detection Threshold / Range (Typ)
Voltage Error	VB	OV	Overvoltage in power supply (12 V)	38.0 V
		UV	Undervoltage in power supply (12 V)	4.0 V
	VCC	OV	Overvoltage in voltage for SDO/ERRB (5.0 V / 3.3 V)	5.40 V / 3.55 V
		UV	Undervoltage in voltage for SDO/ERRB (5.0 V / 3.3 V)	4.60 V / 3.05 V
	REF	OV	Overvoltage in reference voltage for CSAMP (5.0 V / 3.3 V)	5.40 V / 3.55 V
		UV	Undervoltage in reference voltage for CSAMP (5.0 V / 3.3 V)	4.60 V / 3.05 V
	VDD	OV	Overvoltage in LDO voltage for internal circuit. (5.3 V)	6.0 V
		UV	Undervoltage in LDO voltage for internal circuit. (5.3 V)	2.9 V
	VCPL	OV	Overvoltage in the 1st step in Charge Pump.	14.1 V
		UV	Undervoltage in the 1st step in Charge Pump.	5.5 V
	VCPH	OV	Overvoltage in the 2nd step in Charge Pump (VB reference)	14.1 V
		UV	Undervoltage in the 2nd step in Charge Pump (VB reference)	5.5 V
	VCPHD	UV	Undervoltage in the 2nd step in Charge Pump (DRN reference)	5.5 V
	VCPHG	OV	Overvoltage in the 2nd step in Charge Pump (GND reference)	55.0 V
	DRN	UV	Undervoltage in DRN voltage.	3.7 V
FET Driver Error	VGS	H-side	Gate-Source voltage error in External MOS-FET for Motor Drive (ON-Level / OFF-level)	VCPH-2 V / SxH+1 V
		L-side	Same as above	VCPL-2 V / SxL+1 V
	VGSR		Gate-Source voltage error in External MOS-FET for Motor Relay (ON-Level / OFF-level)	VCPH-2 V / 1.0 V
	VDS	H-side	Drain-Source voltage error in External MOS-FET for Motor Drive	-200 to +3000 mV (16 steps)
		L-side	Same as above	
	SNT		Shunt Resistors voltage error	-200 to +1000 mV (16 steps)
	Dynamic OS		Open / short check in External MOS-FET (dynamic mode)	-
	Static OS		Open / short check in External MOS-FET (static mode)	-
Thermal Error	TW		Over temperature for Thermal Warning threshold	135 °C
	TSD		Over temperature for Thermal Shutdown threshold	175 °C
Oscillation Error	OSC Freq		Over and under 20 % frequency in OSC_IF/SM	-
	OSC Stop		Stop Oscillator in OSC_IF/SM	25 µs
MCU Error	WDT		Watch dog timeout. MCU communication error via SPI	6 to 96 ms (4 steps)
	SPI Stop		SPI long term stop.	10 s
	SPI		4 kinds of errors. 1. Mismatch CRC on write access. 2. Mismatch Frame counter on write/read access. 3. Over 32 clock pulse in SCK on write/read access. 4. Under 32 clock pulse in SCK on write/read access.	-
IC Error	REG		Unintended change in registers	-
	BIST		BIST is failed in DBIST or ABIST state.	-
	Internal		Internal Error in IC	-
Gate control	TDEAD		Simultaneous on period error between INxH and INxL.	0 to 654 ns (8 steps)

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7. Protection Function – Continued

7.1 Protection After Error Detection

The following table shows operations of Protection of Gate Driver and next IC state after each error detection in Active state. Each error detection can be masked by register setting. Refer to 7.2 Register Setting for Error Detection, Protection and Error Notification.
'-' in table indicates that it is not affected by this protection.

Their Error detections are protected by changing IC state.

Error Detection			Protection	
			Change IC State	GxH/GxL
Voltage Error	VB	OV	-	Protection (Refer to next page)
		UV		
	VCC	OV		
		UV		
	REF	OV		
		UV		
	VDD	OV		
		UV	Sleep	Hi-Z/Hi-Z *(Note 1)*
	VCPL	OV	Stand-by	
		UV		
	VCPH	OV		
		UV		
	VCPHD	UV		
	VCPHG	OV		
	DRN	UV	-	Protection (Refer to next page)
FET Driver Error	VGS	H-side		
		L-side		
	VGSR			
	VDS	H-side		
		L-side		
	SNT			
	Dynamic OS			
	Static OS			-
Thermal Error	TW			
	TSD			Protection (Refer to next page)
Oscillation Error	OSC Freq		Stand-by	Hi-Z/Hi-Z *(Note 1)*
	OSC Stop		Sleep	
MCU Error	WDT		Stand-by	
	SPI Stop		Sleep	
	SPI *(Note 2)*		Stand-by	
IC Error	REG			
	BIST		FAIL	
	Internal			
Gate control	TDEAD		-	Insert Deadtime *(Note 3)*

(Note 1) If state is changed Active to other state, gate driver and relay driver is forced to set Hi-Z. And Charge Pump is turned off.
(Note 2) Protection by SPI Error is changed by ProtectMode (SPI). If ProtectMode (SPI) is set 0, It is shown in the table. If ProtectMode (SPI) is set 1, protection by SPI Error is disabled.
(Note 3) GxH and GxL are inserted dead time for each phase. Refer to 4.2 Shoot Through Prevention and Detection (TDEAD)

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7. Protection Function - Continued

Each error and register assignment is shown in the table below.

Error Detection	ProtectMode (*)
VB UV VCC OV / UV REF OV / UV VDD OV TSD	No ProtectMode
DRN UV	ProtectMode (DRN)
VGSR	ProtectMode (VGSR)
VDS	ProtectMode (VDS)
SNT	ProtectMode (SNT)
Dynamic OS	ProtectMode (OS)
VB OV	ProtectMode (VB)
VGS	ProtectMode (VGS)

Their error detections are protected by gate control. This protection is selected by GOFHIZ.

Error Detection	Register	Protection	
	GOFHIZ	GxH	GxL
VB UV VCC OV / UV REF OV / UV VDD OV TSD	0	LOW	
	1	Hi-Z	

Their error detections are protected by gate control. This protection is selected by ProtectMode (*) & GOFHIZ.

Error Detection	Register		Protection	
	ProtectMode (*)	GOFHIZ	GxH	GxL
DRN UV VGSR VDS SNT Dynamic OS	0	0	LOW	
		1	Hi-Z	
	1	*	No protection	

VB OV error detection is protected below. If ProtectMode (VB) = 0, GxH and GxL are set Short Brake.

Error Detection	Register		Protection	
	ProtectMode (VB)	GOFHIZ	GxH	GxL
VB OV	0	*	LOW	HIGH
	1	0	LOW	
		1	Hi-Z	

VGS error detections are protected below.

Error Detection	Register	Error Location		Protection	
	ProtectMode (VGS) [1:0]	ON-level / OFF-level	High-side / Low-side	GxH	GxL
VGS	0	*	*	LOW	
	1			Hi-Z	
	2	ON-level		LOW	
		OFF-level	High-side	Hi-Z	LOW
			Low-side	LOW	Hi-Z
	3	*	*		

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7. Protection Function - Continued

7.1.1 Protection and ERRB timing after Error Detection

Each error detection can be classified into 4 types, depending on the protection and ERRB output pattern.

<table>
<tr><th>Error Detection</th><th>Error Type</th><th>Description</th></tr>
<tr><td>VB OV / UV
VDD OV
VCC OV / UV
REF OV / UV
VGSR
TW
TSD
OSC Freq
SPI
REG
TDEAD</td><td>A</td><td>Output Error in Basic.
If Error is detected, ERRB and protection are active.</td></tr>
<tr><td>VCPL OV / UV
VCPH OV / UV
VCPHD UV
VCPHG OV
DRN UV
VGS
VDS
SNT
Dynamic OS
Static OS</td><td>B</td><td>Output Error with the function of holding protection for a period of time (t_{PRO}) when ProtectMode(*) = 0.
<table>
<tr><th>Error Detection</th><th>t_{PRO} [µs]</th></tr>
<tr><td>VCPL OV / UV
VCPH OV / UV
VCPHD UV
VCPHG OV
DRN UV
Static OS</td><td>1</td></tr>
<tr><td>VGS
VDS
SNT
Dynamic OS</td><td>128</td></tr>
</table></td></tr>
<tr><td>BIST
Internal</td><td>C</td><td>Output Error with the function of keeping error conditions forever.</td></tr>
<tr><td>VDD UV
OSC Stop
SPI Stop</td><td>D</td><td>No output error and IC is sleep.</td></tr>
</table>

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7. Protection Function - Continued

The timing charts for each type are shown in the figure below.

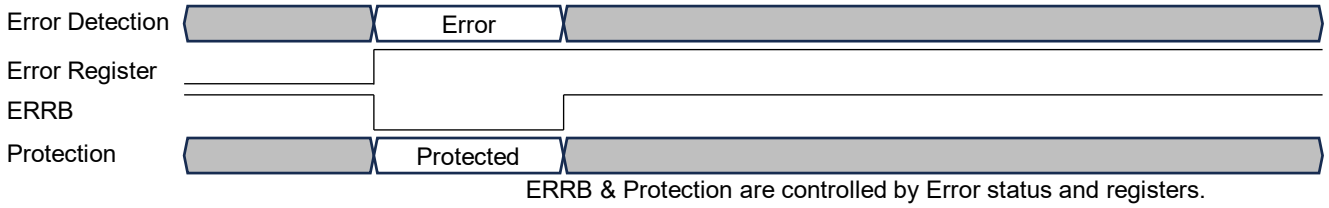


Figure 21. Behavior of ERRTYPE-A

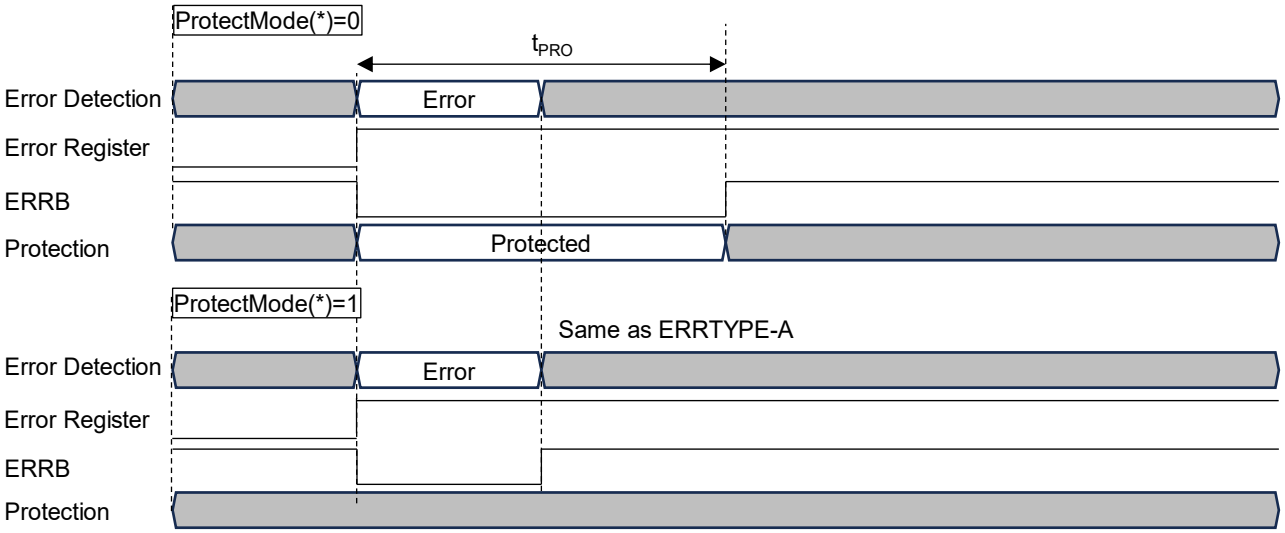


Figure 22. Behavior of ERRTYPE-B

VCP OV/UV Error detections are protected by changing state to Stand-by state. So, protection does not maintain 1µs.

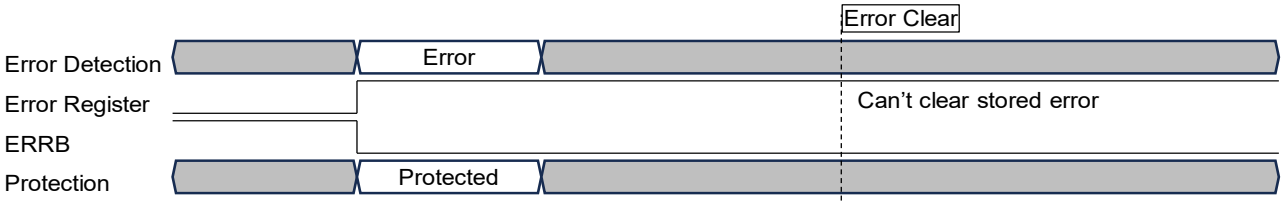


Figure 23. Behavior of ERRTYPE-C

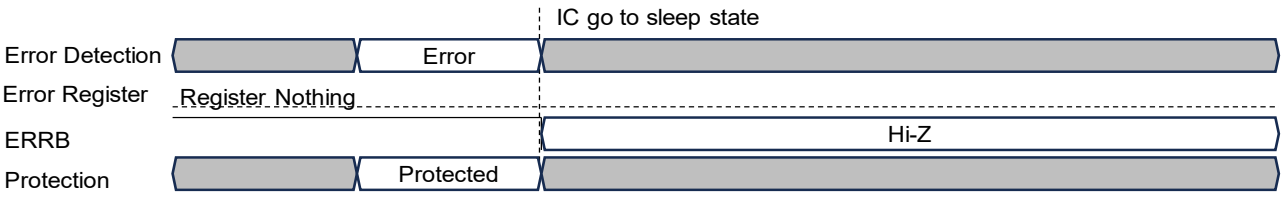


Figure 24. Behavior of ERRTYPE-D

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7. Protection Function - Continued

7.2 Register Setting for Error Detection, Protection and Error Notification

Detected error status are stored to Error registers. MCU can monitor the result by reading registers via SPI.

Item	Read Value	Error Clear method
Error Register	0: No error 1: Error	Writing ‘1’ to ERCLR register. But all stored errors are cleared. Writing ‘1’ to a register of Error Register. Writing ‘1’ to a register of Detection Mask

MCU can set following items for each detection / protection function.

Item	Function
ERRB output	Setting to output ERRB 0: Errors don’t output to ERRB 1: Errors output to ERRB
Detection Mask	Error detection is disabled. Protection operation after the detection is not executed if disabled. 0: Each error detection is enabled 1: Each error detection is disabled If error detection mask register is set to ‘1’ after the error was detected, the error register is cleared.
Keep Protection	Setting to keep the protection operation after each error status is cleared. 0: Recovering from protection state to normal state after each error is cleared 1: Keeping protection state even after each error is cleared. IC can recover from protection state by setting a register ProtectKeep (*) to ‘0’.

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7. Protection Function - Continued

The function assignments for each register and error detection are as follows. x represents each phase (x = 1,2,3)

Error Detection		Error Register	ERRB output	Detection Mask	Keep Protection
VB	OV	ErrorOV (VB)	ErrorOutEnOV (VB)	ErrorMaskOV (VB)	ProtectKeepOV (VB)
	UV	ErrorUV (VB)	ErrorOutEnUV (VB)	ErrorMaskUV (VB)	ProtectKeepUV (VB)
VCC	OV	ErrorOV (VCC)	ErrorOutEnOV (VCC)	ErrorMaskOV (VCC)	ProtectKeepOV (VCC)
	UV	ErrorUV (VCC)	ErrorOutEnUV (VCC)	ErrorMaskUV (VCC)	ProtectKeepUV (VCC)
REF	OV	ErrorOV (REF)	ErrorOutEnOV (REF)	ErrorMaskOV (REF)	ProtectKeepOV (REF)
	UV	ErrorUV (REF)	ErrorOutEnUV (REF)	ErrorMaskUV (REF)	ProtectKeepUV (REF)
VDD	OV	ErrorOV (VDD)	ErrorOutEnOV (VDD)	ErrorMaskOV (VDD)	ProtectKeepOV (VDD)
	UV	(No error info)	(No error info)	(Always enabled)	(No keep protection)
VCPL	OV	ErrorOV (VCPL)	ErrorOutEnOV (CP)	ErrorMaskOV (CP)	
	UV	ErrorUV (VCPL)	ErrorOutEnUV (CP)	ErrorMaskUV (CP)	
VCPH	OV	ErrorOV (VCPH)	ErrorOutEnOV (CP)	ErrorMaskOV (CP)	
	UV	ErrorUV (VCPH)	ErrorOutEnUV (CP)	ErrorMaskUV (CP)	
VCPHD	UV	ErrorUV (VCPHD)			
VCPHG	OV	ErrorOV (VCPHG)	ErrorOutEnOV (CP)	ErrorMaskOV (CP)	
DRN	UV	ErrorUV (DRN)	ErrorOutEnUV (DRN)	ErrorMaskUV (DRN)	ProtectKeepUV (DRN)
VGS	H-side	ErrorVGS (xH)	ErrorOutEn (VGS)	ErrorMaskVGS (xH)	ProtectKeep (VGS)
	L-side	ErrorVGS (xL)		ErrorMaskVGS (xL)	
VGSR		ErrorVGS (xR)	ErrorOutEn (VGSR)	ErrorMaskVGS (xR)	ProtectKeep (VGSR)
VDS	H-side	ErrorVDS (xH)	ErrorOutEn (VDS)	ErrorMaskVDS (xHL)	ProtectKeep (VDS)
	L-side	ErrorVDS (xL)			
SNT		ErrorSNT (xL)	ErrorOutEn (SNT)	ErrorMaskSNT (xL)	ProtectKeep (SNT)
Dynamic OS					
Open	H-side	ErrorOpen (xH)	ErrorOutEn (Open)	ErrorMaskOpen (xH)	ProtectKeep (Open)
	L-side	ErrorOpen (xL) ErrorOpen2 (xL)		ErrorMaskOpen (xL)	
Short	H-side	ErrorShort (xH)	ErrorOutEn (Short)	ErrorMaskShort (xH)	ProtectKeep (Short)
	L-side	ErrorShort (xL) ErrorShort2 (xL)		ErrorMaskShort (1L)	
Static OS					
Open	H-side	ErrorOpen (xH)	ErrorOutEn (Open)	(Always enabled)	(No keep protection)
	L-side	ErrorOpen (xL)			
	Motor Relay	ErrorOpen (xR)			
	Power Relay	ErrorOpen (PR)			
Short	H-side	ErrorShort (xH)	ErrorOutEn (Short)		
	L-side	ErrorShort (xL)			
	Motor Relay	ErrorShort (xR)			
	Power Relay	ErrorShort (PR)			
	Motor to VB	ErrorShort (MB)			
	Motor to GND	ErrorShort (MG)			
TW		Error (TW)	ErrorOutEn (TW)	ErrorMask (TW)	(No keep protection)
TSD		Error (TSD)	ErrorOutEn (TSD)	ErrorMask (TSD)	ProtectKeep (TSD)
OSC Freq	OSCIF	Error (OSC)	(Always enabled)	ErrorMask (OSC)	(No keep protection)
	OSCSM				
OSC Stop	OSCIF	(No error info)	(No error info)	(Always enabled)	
	OSCSM			ErrorMask (OSC)	
WDT		Error (WDT)	ErrorOutEn (WDT)	ErrorMask (WDT)	
SPI Stop		(No error info)	(No error info)	ErrorMask (SPIST)	
SPI		Error (SPI)	ErrorOutEn (SPI)	ErrorMask (SPI)	
REG		Error (REG)	ErrorOutEn (REG)	ErrorMask (REG)	
BIST		Error (BIST)	(Always enabled)	(Always enabled)	
Internal		Error (INTER)			
TDEAD		Error (TDEAD)	ErrorOutEn (TDEAD)	ErrorMask (TDEAD)	

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7. Protection Function - Continued

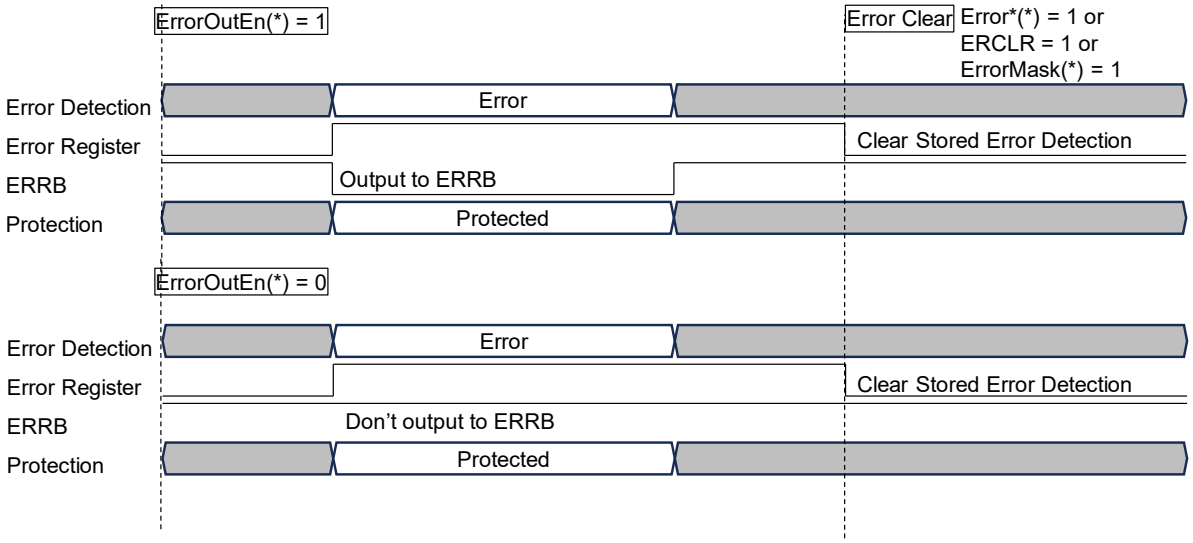


Figure 25. Behavior of ERRB output and Error Clear

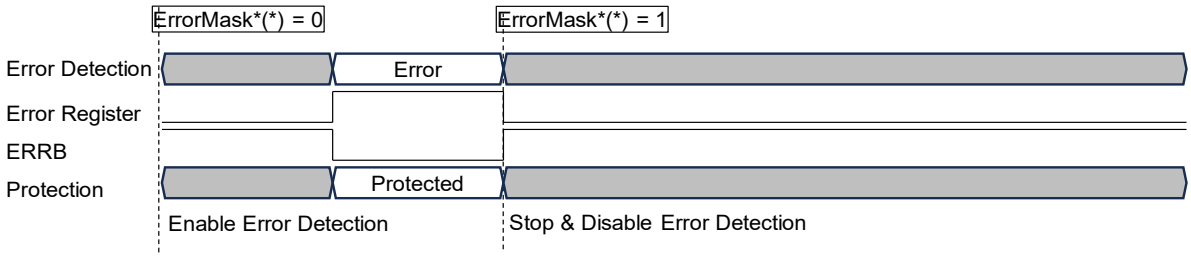


Figure 26. Behavior of Detection Mask

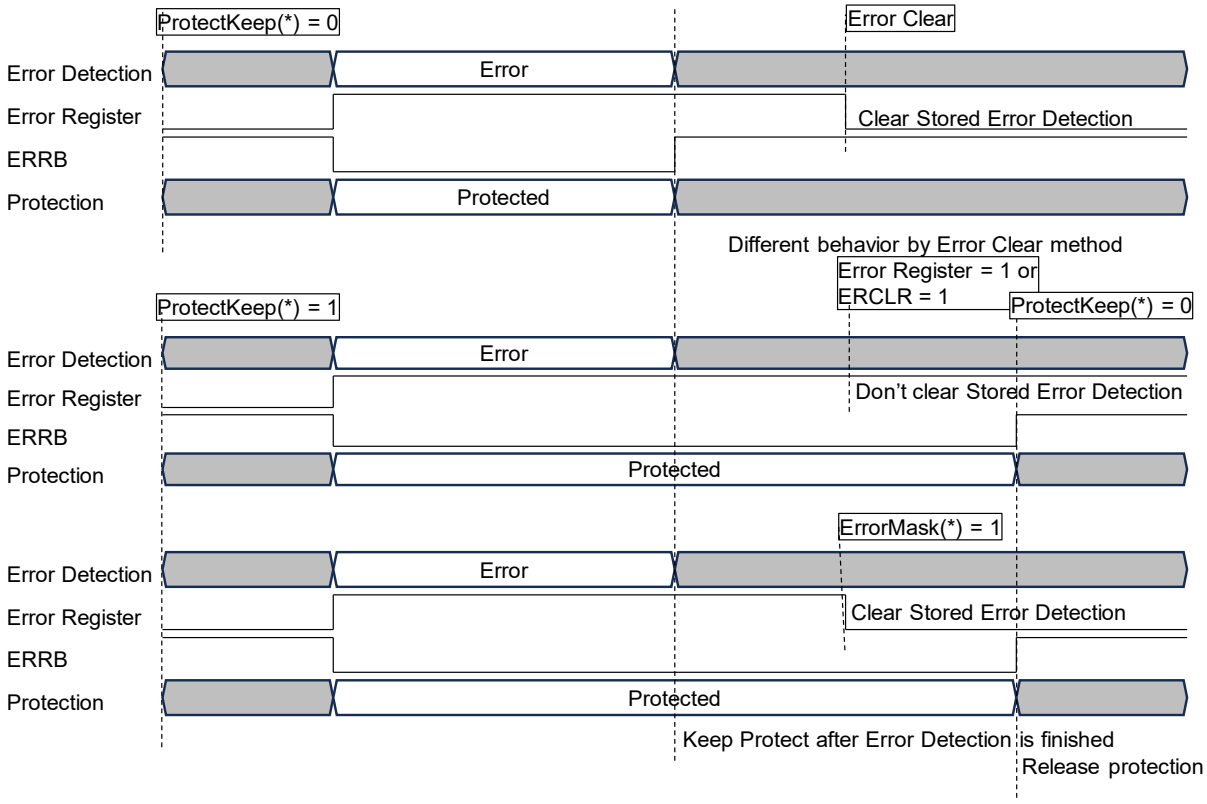


Figure 27. Behavior of Keep Protection

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7. Protection Function - Continued

7.3 Power Supply (VB/VDD/VCPH/VCPL) OV/UV and DRN UV Detection

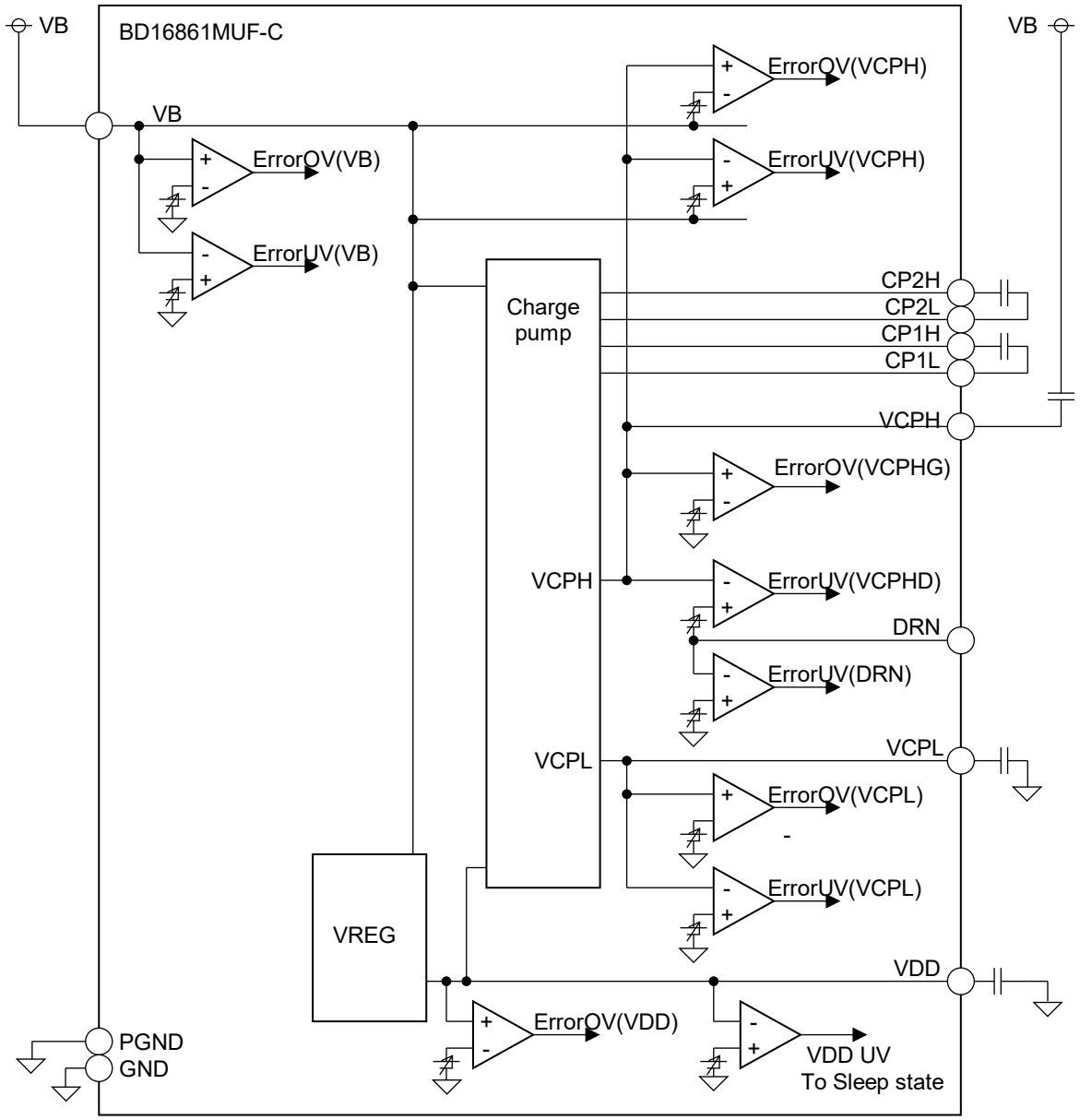


Figure 28. Block Diagram for Power Supply

Low voltage and high voltage of Power supply (VB/VDD/VCPH/VCPL) can be detected.

Behaviors of protection for Gate driver can be selected in Overvoltage detection in VB.
When VDD UV is detected, IC enters Sleep state.

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7. Protection Function - Continued

7.4 Reference Voltage (VCC/REF) OV/UV Detection

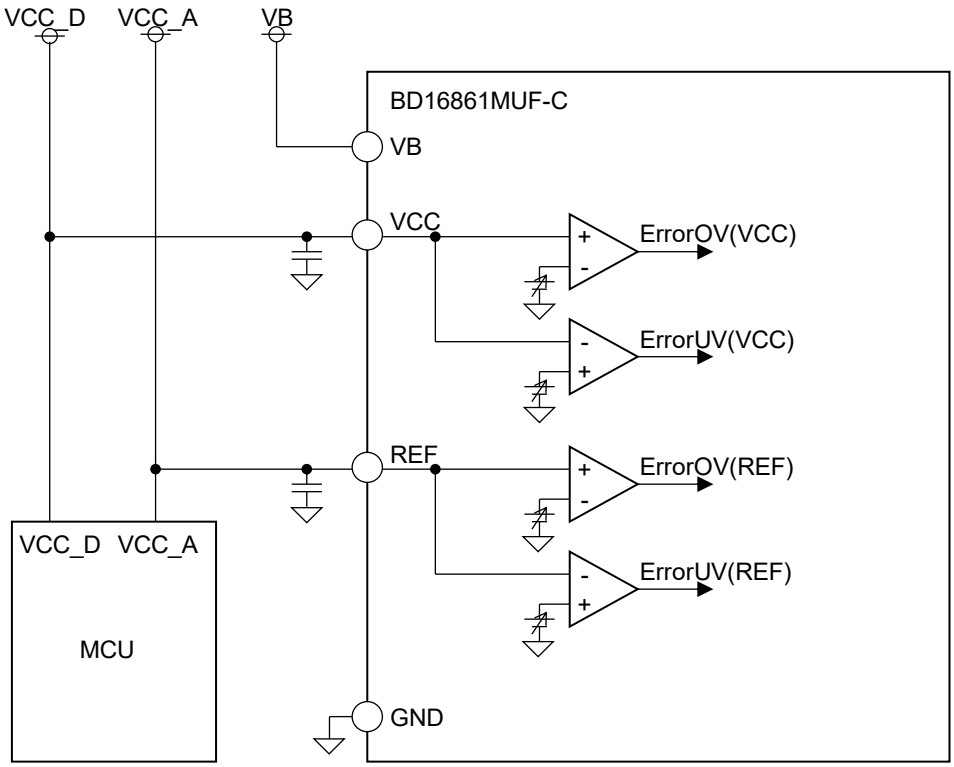


Figure 29. Block diagram for Reference Voltage

Overvoltage / Undervoltage of input pin (VCC/REF) can be detected. Each threshold can be set by registers VCTH, VRTH and state.

VCTH	V_{VCUV} (V)	V_{VCOV} (V)
0	4.60	5.40
1	3.05	3.55

VRTH	V_{REFUV} (V)	V_{REFOV} (V)
0	4.60	5.40
1	3.05	3.55

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7. Protection Function - Continued

7.5 Gate-Source voltage (VGS) Error Detection

7.5.1 VGS Error Detection in External MOS-FET for Motor Drive

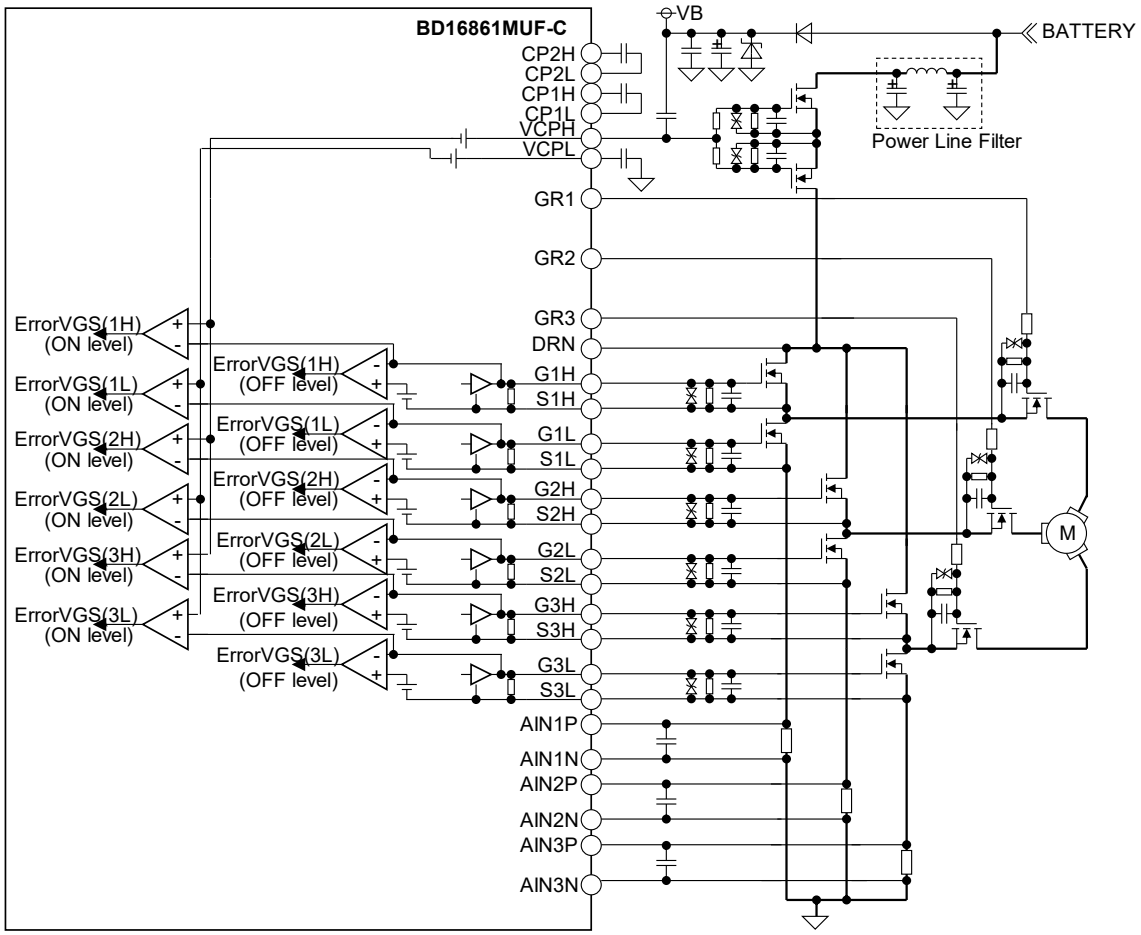


Figure 30. Circuit diagram for VGS Error Detection in GxH/GxL

This function detects 4 conditions in each phase.
1. When INxH = H, GxH is lower than ON level threshold (VCPH-2.0 V).
2. When INxH = L, GxH is higher than OFF level threshold (SxH+1.0 V).
3. When INxL = H, GxL is lower than ON level threshold (VCPL-2.0 V).
4. When INxL = L, GxL is higher than OFF level threshold (SxL+1.0 V).

VGS errors for GxH/GxL (x = 1,2,3) will be detected even if gate outputs are turned off by DOFFB = L or GxOFF = 1.

In VGS error detections for GxH/GxL, there are a detection mask period t_{VGS_MSK} after the gate drive output change and a filter period t_{VGS_FLT} after detection mask period, which can be set in the registers TVGS_MSK and TVGS_FLT, respectively. The mask and filter period are also applied when GxH/GxL are turned off by protection after error detection.
VGS errors for GxH/GxL will be detected if GOFHIZ = 1 because the settling time to low level will become longer than the masking period based on the gate capacitance of FET.

TVGS_MSK [2:0]	Mask Period (t_{VGS_MSK})	TVGS_FLT [2:0]	Filter Period (t_{VGS_FLT})
0	4 / f_{OSC}	0	0
1	8 / f_{OSC}	1	1 / f_{OSC}
2	12 / f_{OSC}	2	2 / f_{OSC}
3	16 / f_{OSC}	3	4 / f_{OSC}
4	24 / f_{OSC}	4	8 / f_{OSC}
5	32 / f_{OSC}	5	16 / f_{OSC}
6	48 / f_{OSC}	6	32 / f_{OSC}
7	64 / f_{OSC}	7	64 / f_{OSC}

1 / f_{OSC} = 93.7ns (Typ)

The timing chart below shows when an error occurs and when it does not.

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7. Protection Function - Continued

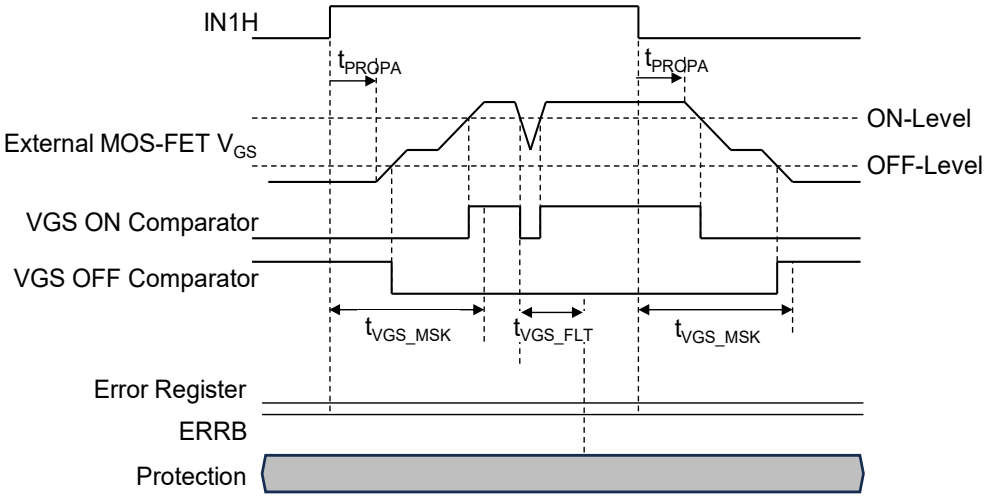


Figure 31. No-error Pattern Timing Chart for High-side in VGS.

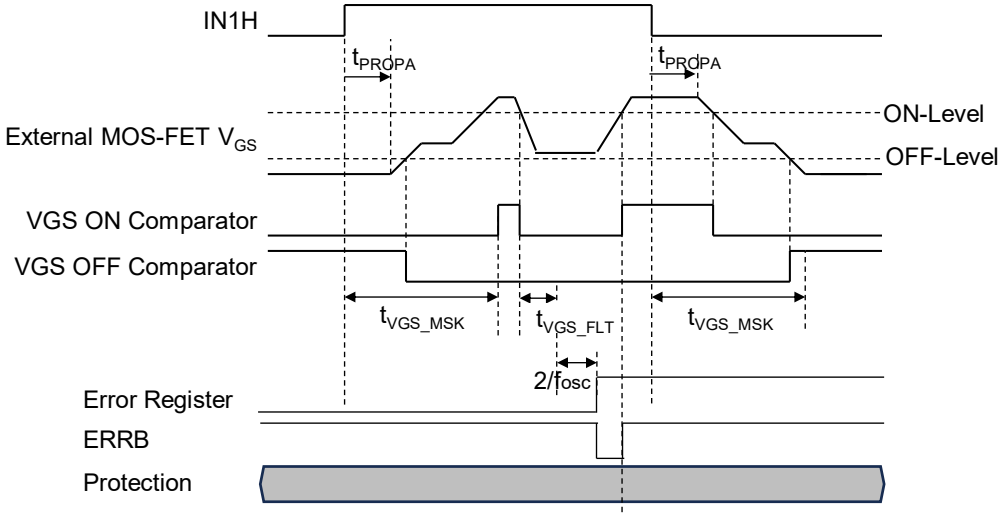


Figure 32. Error Pattern Timing Chart for High-side in VGS when ProtectMode(VGS) = 1

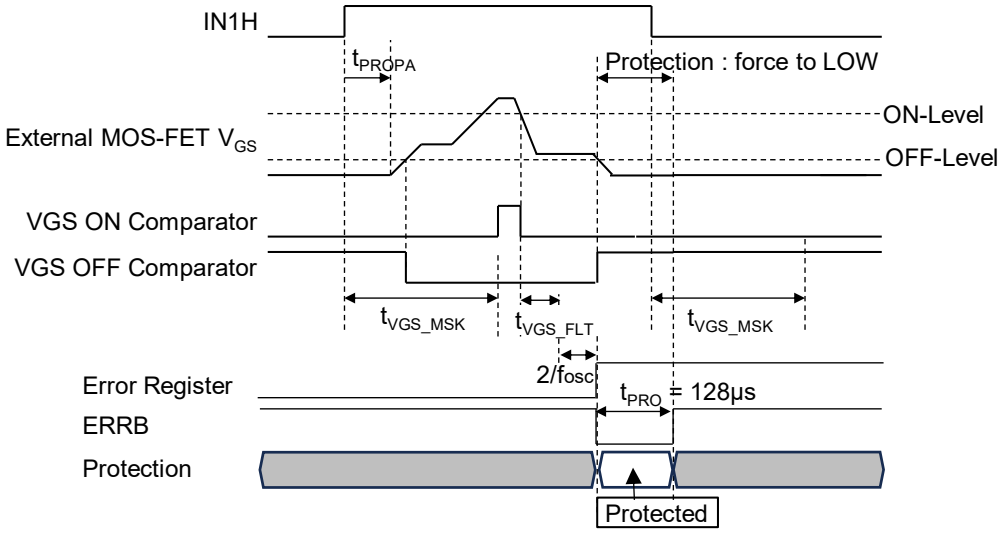


Figure 33. Error Pattern Timing Chart for High-side in VGS when ProtectMode(VGS) = 0

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7. Protection Function - Continued

7.5.2 VGS Error Detection in External MOS-FET for Motor Relay

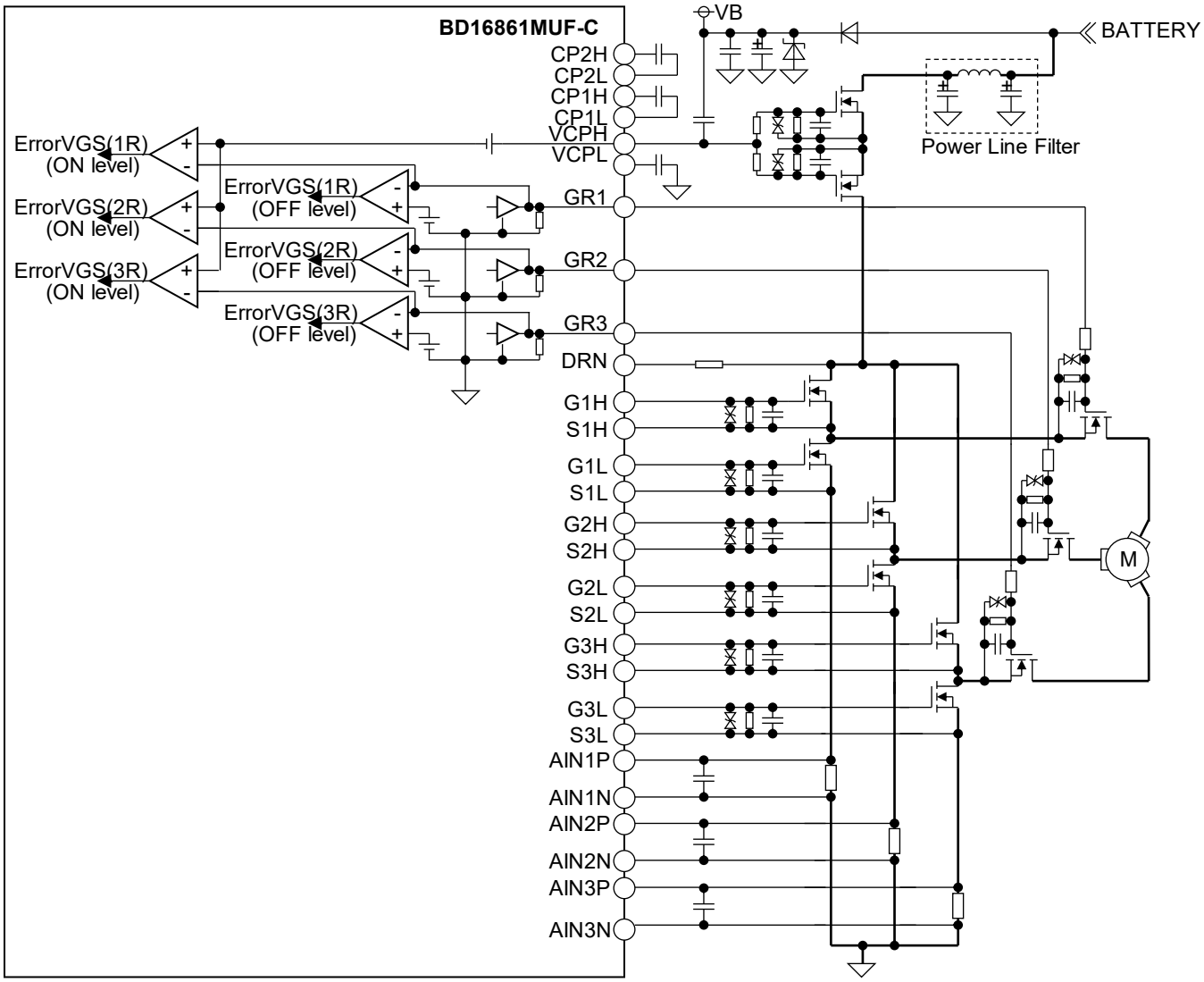


Figure 34. Circuit diagram for VGS Error Detection in GRx

This function detects 2 conditions in each phase.
1. When RxOFF = 0, GRx is lower than ON level threshold.
2. When RxOFF = 1, GRx is higher than OFF level threshold.

VGS errors for GRx (x = 1,2,3) will be detected even if relay outputs are turned off by RxOFF = 1.

In VGS error detections for GRx, there are a detection mask period t_{VGS_MSK} = 64 / f_{OSC} and a filter period t_{VGS_FLT} = 64 / f_{OSC}.
About timing chart, refer to 7.5.1 VGS Error Detection in External MOS-FET for Motor Drive.

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7. Protection Function - Continued

7.6 Drain-Source voltage (VDS) Error Detection

VDS error state can be detected by monitoring drain-source voltage of external MOS-FET.

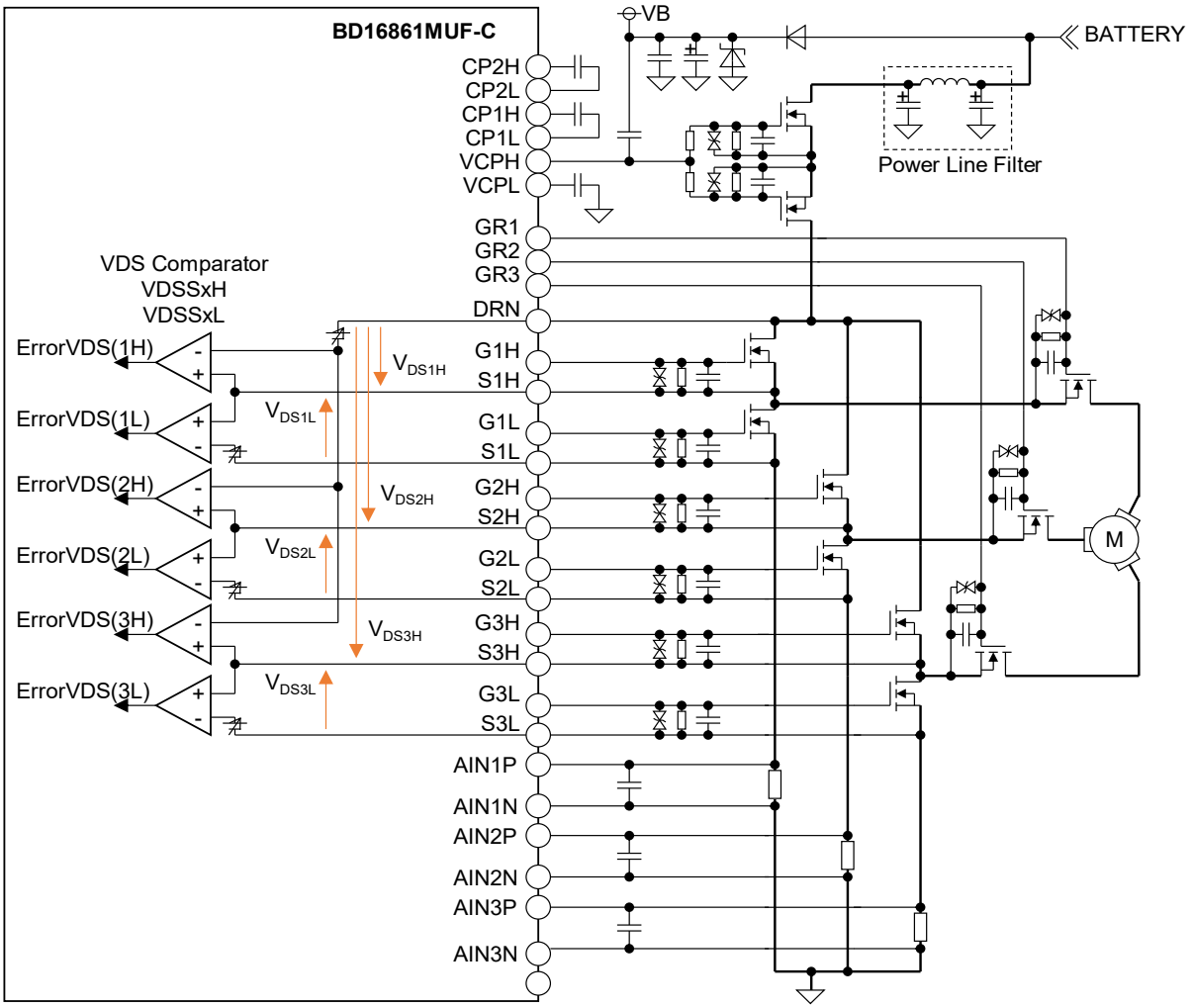


Figure 35. Circuit Diagram for VDS Error Detection

This function detects 2 conditions in each phase.

1. When INxH = H, VDS of High-side MOS-FET is higher than threshold.
2. When INxL = H, VDS of Low-side MOS-FET is higher than threshold.

VDS errors will be detected even if gate outputs are turned off by DOFFB = L or GxOFF = 1.

When VDS is over the selected voltage level, IC detects an error.
The threshold voltage level for error detection of VDS can be set for each of high-side / low-side FET by registers VDSH and VDSL.
(Note 1) : These setting are forbidden in the condition of VB = 4.5 to 5.5V.

VDSH [3:0] VDSL [3:0]	V_{DS} Abnormal Detection Threshold Voltage [mV]
0h	-200
1h	+50
2h	+100
3h	+200
4h	+300
5h	+400
6h	+500
7h	+600
8h	+700
9h	+800
Ah	+900
Bh	+1000
Ch	+1500
Dh	+2000
Eh *(Note 1)*	+2500
Fh *(Note 1)*	+3000

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7. Protection Function - Continued

Immediately after the gate drive output changes, the drain-source voltage becomes unstable. Spike noise may also occur immediately after VDS error detection. To prevent false detection due to these, there is a detection mask period t_{VDS_MSK} after the gate drive output change and a filter period t_{VDS_FLT} after detection mask period, which can be set in the registers TVDS_MSK and TVDS_FLT, respectively.

TVDS_MSK [3:0]	Mask Period t_{VDS_MSK}	TVDS_FLT [3:0]	Filter Period t_{VDS_FLT}
0h	4 / f_{OSC}	0h	0 ns
1h	8 / f_{OSC}	1h	1 / f_{OSC}
2h	12 / f_{OSC}	2h	2 / f_{OSC}
3h	16 / f_{OSC}	3h	4 / f_{OSC}
4h	24 / f_{OSC}	4h	8 / f_{OSC}
5h	32 / f_{OSC}	5h	16 / f_{OSC}
6h	48 / f_{OSC}	6h	32 / f_{OSC}
7h	64 / f_{OSC}	7h	64 / f_{OSC}
8h	80 / f_{OSC}	8h	80 / f_{OSC}
9h	160 / f_{OSC}	9h	160 / f_{OSC}
Ah	240 / f_{OSC}	Ah	240 / f_{OSC}
Bh	320 / f_{OSC}	Bh	320 / f_{OSC}
Ch	400 / f_{OSC}	Ch	400 / f_{OSC}
Dh	480 / f_{OSC}	Dh	480 / f_{OSC}
Eh	560 / f_{OSC}	Eh	560 / f_{OSC}
Fh	640 / f_{OSC}	Fh	640 / f_{OSC}

1 / f_{OSC} = 93.7ns (Typ)

The timing chart below shows when an error occurs and when it does not.

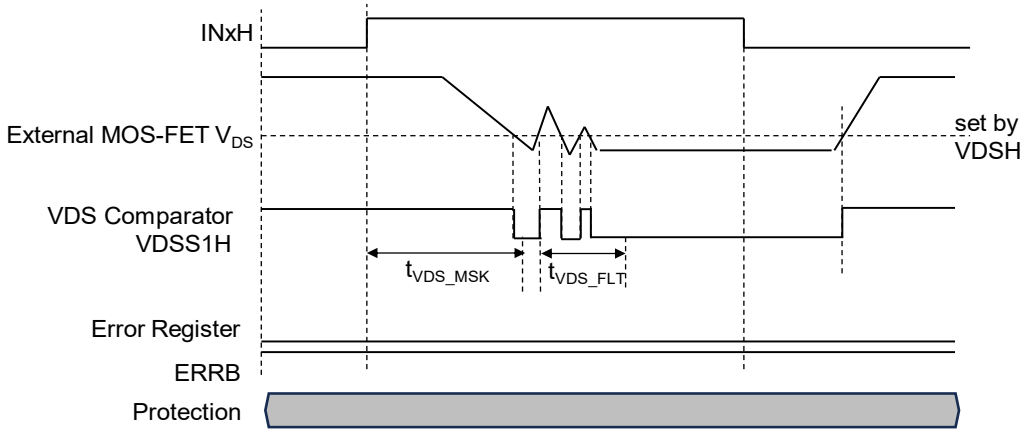


Figure 36. No-error pattern Timing Chart for VDS

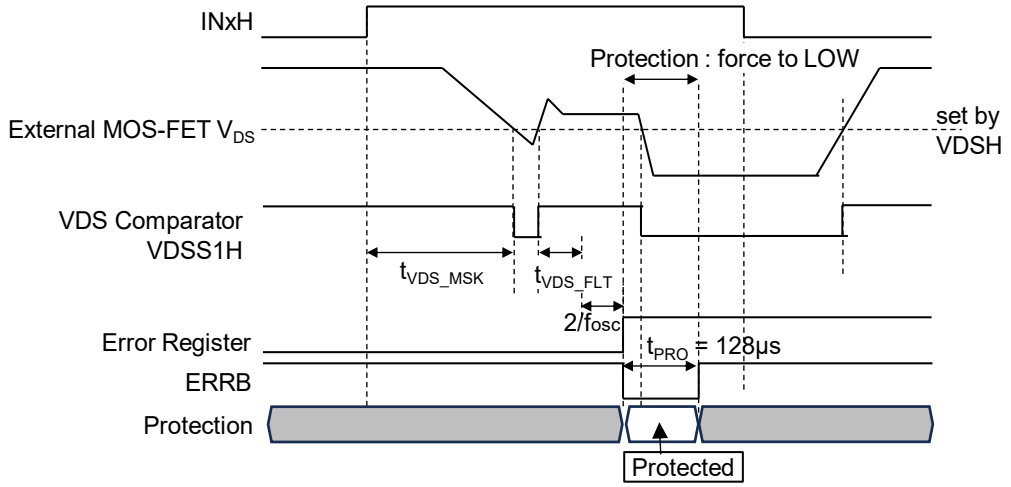


Figure 37. Error pattern Timing Chart for VDS

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7. Protection Function - Continued

7.7 Shunt Resister Voltage (SNT) Error Detection

The shunt resistor voltage abnormality detection function monitors abnormal voltage at both ends of the external shunt resistor.

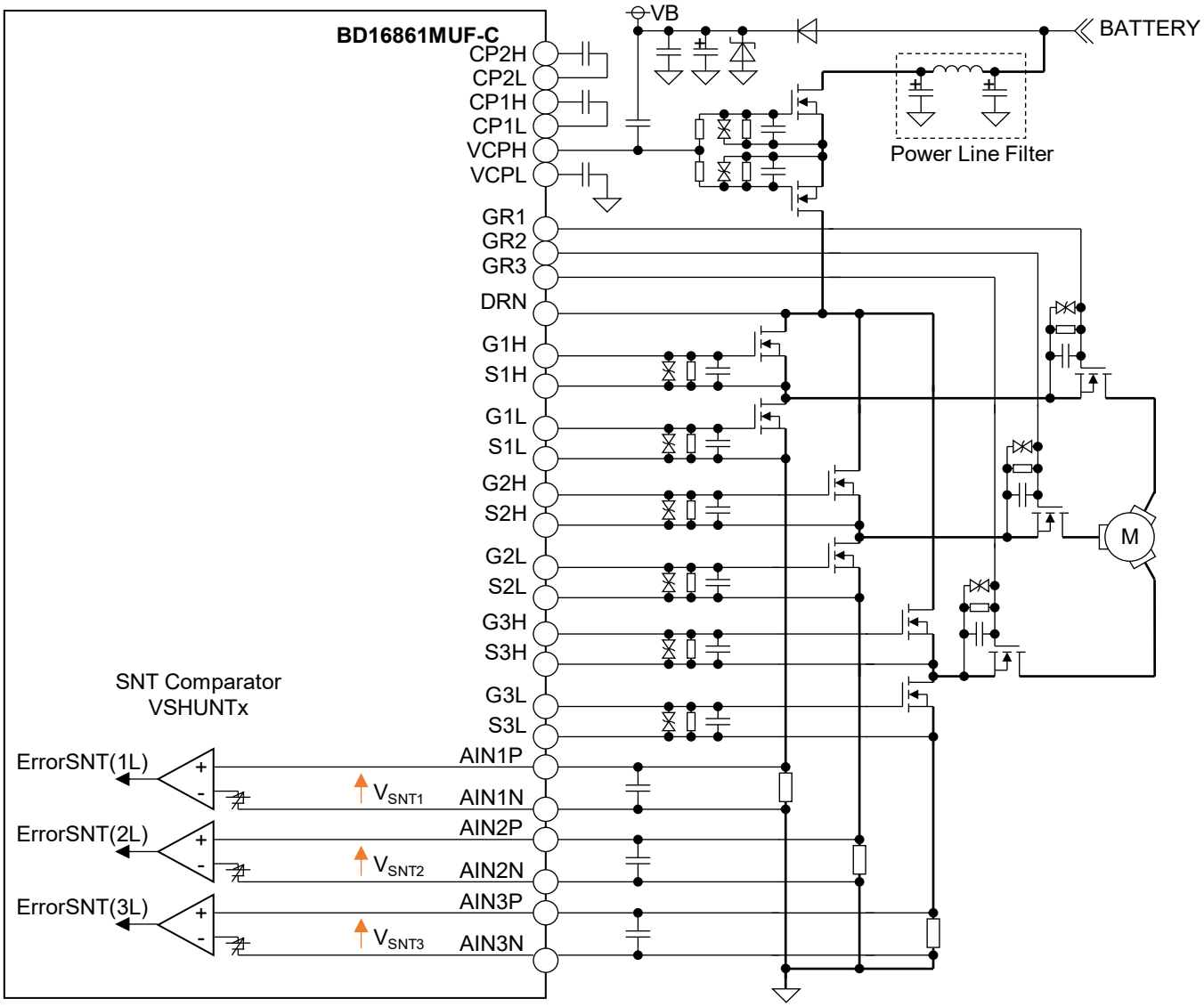


Figure 38. Circuit Diagram for SNT Error Detection

This function detects V_{SNTx} is higher than threshold when INxH = H or INxL= H. The threshold voltage for SNT error detection can be set with register VSNT.

VSNT [3:0]	Threshold Voltage [mV]
0h	-200
1h	+33
2h	+100
3h	+150
4h	+200
5h	+250
6h	+300
7h	+350
8h	+400
9h	+450
Ah	+500
Bh	+600
Ch	+700
Dh	+800
Eh	+900
Fh	+1000

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7. Protection Function - Continued

Immediately after the gate drive output changes, the voltage between AINxP and AINxN becomes unstable. Spike noise may also occur immediately after shunt resistor voltage error detection. To prevent false detection due to these factors, there is a detection mask period t_{SNT_MSK} after the gate drive output changes and a filter period t_{SNT_FLT} after detection mask period, which can be set with the registers TSNT_MSK and TSNT_FLT, respectively.

TSNT_MSK [2:0]	Mask Period t_{SNT_MSK}	TSNT_FLT [2:0]	Filter period t_{SNT_FLT}
0	0	0	0
1	1 / f_{OSC}	1	1 / f_{OSC}
2	2 / f_{OSC}	2	2 / f_{OSC}
3	4 / f_{OSC}	3	4 / f_{OSC}
4	8 / f_{OSC}	4	8 / f_{OSC}
5	16 / f_{OSC}	5	16 / f_{OSC}
6	32 / f_{OSC}	6	32 / f_{OSC}
7	64 / f_{OSC}	7	64 / f_{OSC}

1 / f_{OSC} = 93.7ns (Typ)

The timing chart below shows when an error occurs and when it does not.

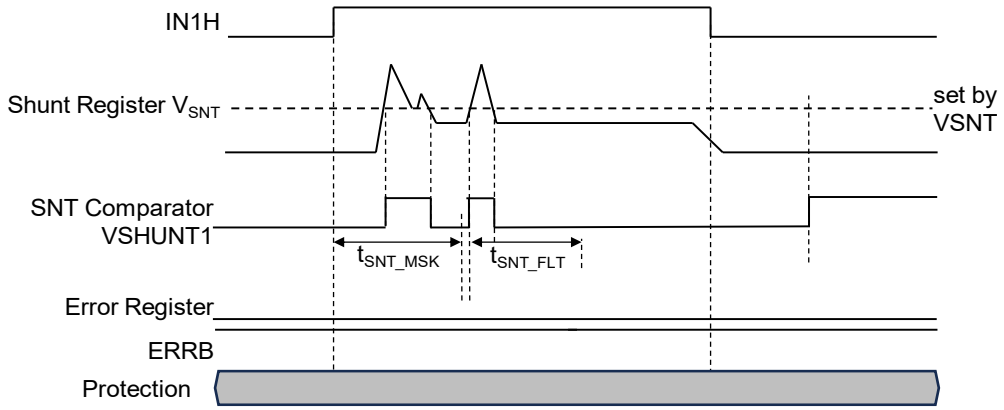


Figure 39. No-error pattern Timing Chart for SNT

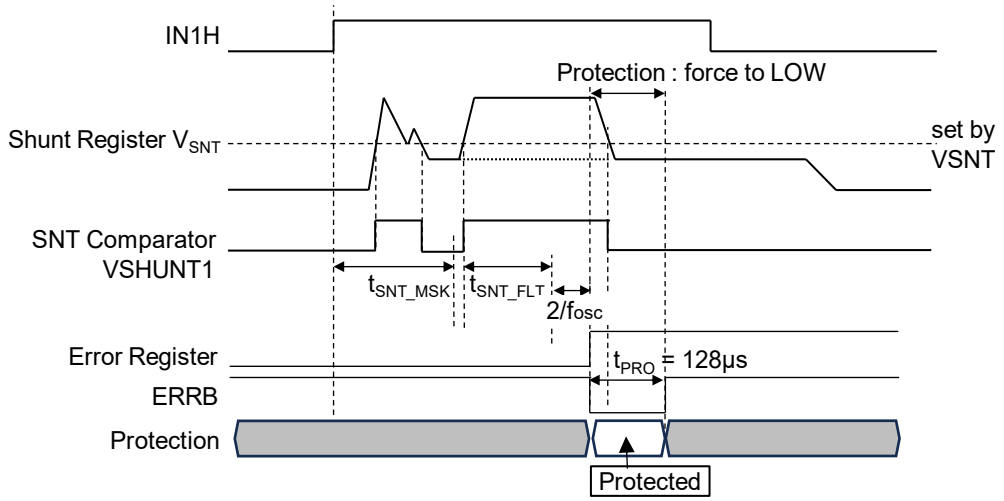


Figure 40. Error pattern Timing Chart for SNT

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7. Protection Function - Continued

7.8 Open/Short (OS) Detection in External MOS-FET

This IC has 2 modes of open / short detection in external MOS-FET. One is a static OS detection, and another is a dynamic OS detection. If IC runs static OS detection and dynamic OS detection at the same time, only static detection will take precedence.

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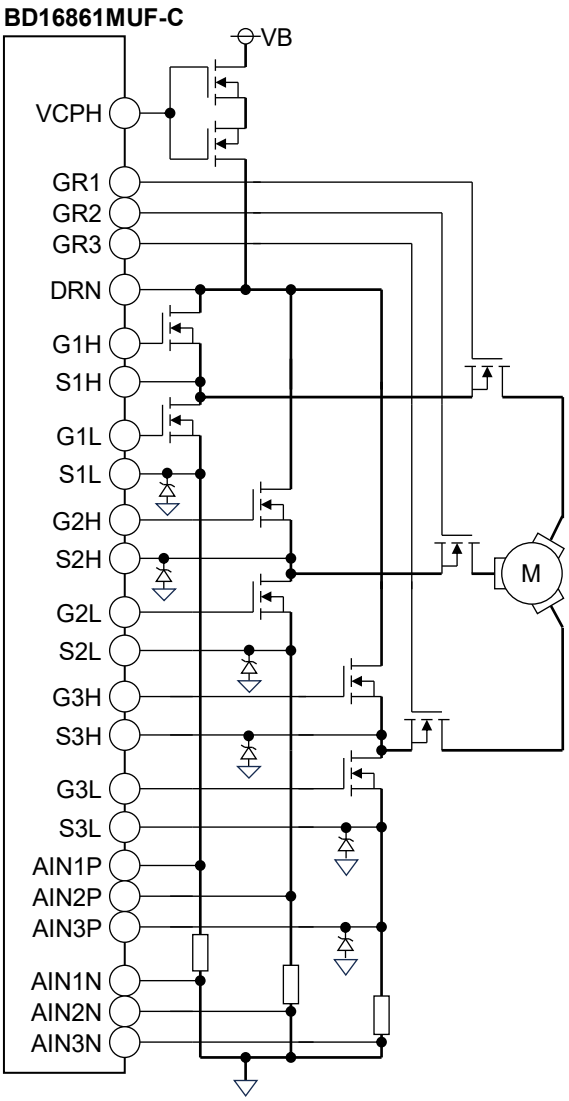
7. Protection Function - Continued

7.8.1 Static OS Detection

Static OS detection is available in Active state and it is executed during stopping motor rotation. It starts by writing value to the register OSCHK.

Support application circuit in the figure below.

Circuit A



Circuit B

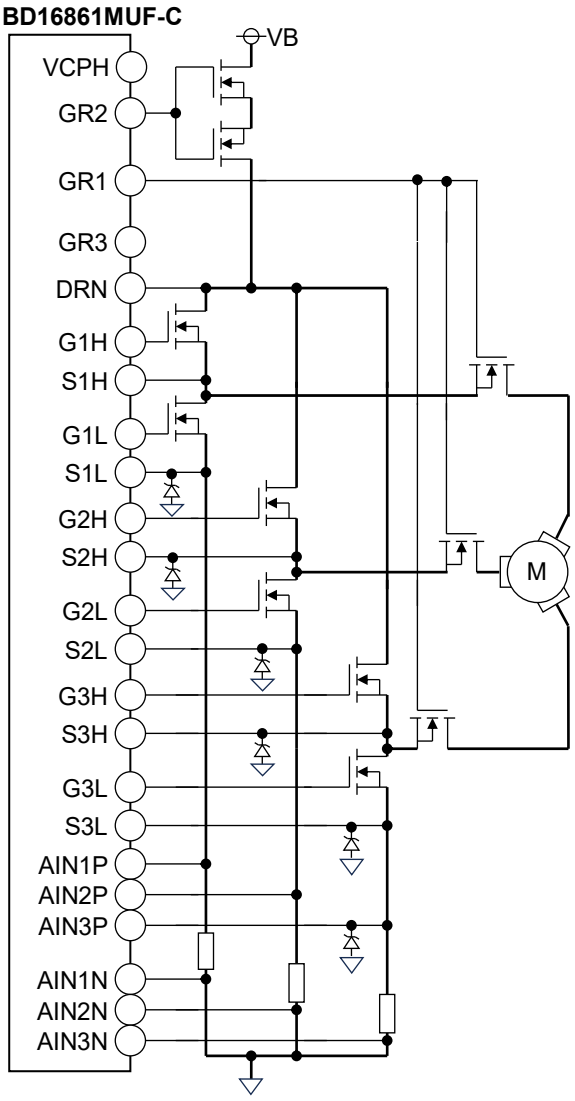


Figure 41. Support Circuit in Static OS Detection

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7. Protection Function - Continued

OSCHK [4:0]	Check item for Circuit A	OSCHK [4:0]	Check item for Circuit B
00h	(NOP)	10h	(NOP)
01h	(A1)→(A2)→(C)	11h	(A1)→(A2)→(B)→(C)
02h	(A1)→(A2)→(C)→(D)	12h	(A1)→(A2)→(B)→(C)→(D)
03h	(A1)→(A2)→(C)→(E)	13h	(A1)→(A2)→(B)→(C)→(E)
04h	(A1)→(A2)→(C)→(F)	14h	(A1)→(A2)→(B)→(C)→(F)
05h	(A1)→(A2)→(C)→(G)	15h	(A1)→(A2)→(B)→(C)→(G)
06h	(A1)→(A2)→(C)→(D)→(E)→(F)→(G)	16h	(A1)→(A2)→(B)→(C)→(D)→(E)→(F)→(G)
07h	(C)→(D)	17h	(C)→(D)
08h	(C)→(D)→(E)→(F)→(G)	18h	(C)→(D)→(E)→(F)→(G)
09h	(A1)→(A2)	19h	(A1)→(A2)→(B)
0Ah	(C)	1Ah	(C)
0Bh	(D)	1Bh	(D)
0Ch	(E)	1Ch	(E)
0Dh	(F)	1Dh	(F)
0Eh	(G)	1Eh	(G)
0Fh	(B) *(Note 1)*	1Fh	(NOP)

(Note 1) During short check of power relay, application circuit must be in the figure below.

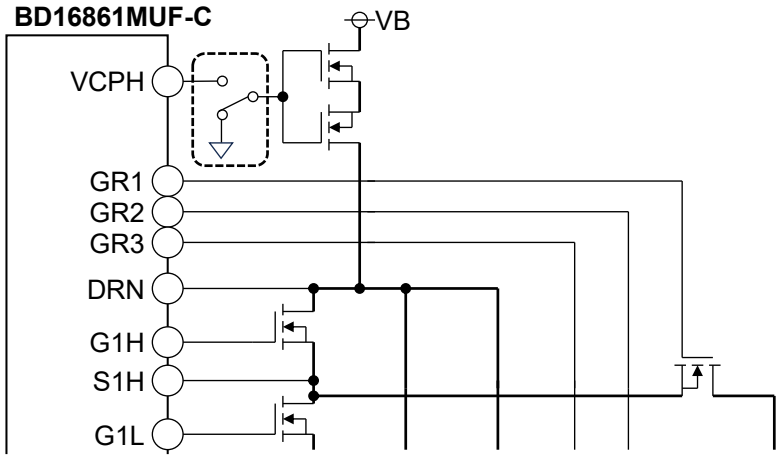


Figure 42. How to check Power Relay in Circuit A

Overview and period of each sequence.

Sequence	Overview	Period [ms]
Wait	-	0.1
A1	Power Relay Open check1	0.1
A2	Power Relay Open check2	0.1 / 1.0 / 10.0 / 20.0 (Select by OS_SEQ_PROP)
B	Power Relay Short check	
C	High/Low-side FET Short check	0.4
D	High/Low-side FET Open check	0.6
E	Motor output to VB check	0.5
F	Motor Relay Short check	0.5 / 0.6 / 0.9 / 1.4 (Select by OS_SEQ_MR1SH)
G	Motor Relay Open check	0.3 / 0.4 / 0.7 / 1.2 (Select by OS_SEQ_MR1SH)

DRNOPDET

DRNOPDET monitors DRN voltage during power relay check.
When power relay is checked open/short, DRN is pulled down, and the voltage between VB-DRN is compared with the threshold voltage for judgment.

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7. Protection Function - Continued

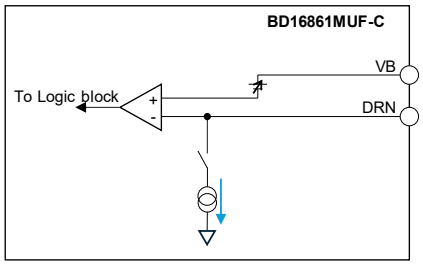


Figure 43. Circuit Diagram when DRNOPDET = 1

(A1) Power Relay Open check1
Open failure of the power relay is detected by turning on power relay and monitoring the voltage between VB-DRN.
If DRN voltage is greater than 0.5 V (Typ) with respect to VB voltage, it is judged as Open failure of power relay.

(A2) Power Relay Open check2
Open failure of the power relay is detected by turning on power relay and monitoring the voltage between VB-DRN.
DRN is pulled down in the interval set by OS_SEQ_PROP. If VB-DRN voltage exceeds the threshold set by OS_DETVTH within that interval, it is judged as Open failure of power relay.

(B) Power Relay Short check
Short failure of power relay is detected by turning off power relay and monitoring the voltage between VB-DRN.
DRN is pulled down in the interval set by OS_SEQ_PROP. DRN is pulled down may cause ErrorUV (DRN), ErrorUV (VCC) and ErrorUV (REF) errors, but don't worry. MCU needs to change OS_SEQ_PROP depending on the capacity of C29 (smoothing capacitor for DRN). If there is not enough time, short failure of power relay will be falsely determined.
If VB-DRN voltage doesn't exceed the threshold set by OS_DETVTH within that interval, it is judged as short failure of power relay.
This check is only available for applications where power relay can be turned off.

Static Open check detection period of Sequence (A2 and B) is set by register (OS_SEQ_PROP [1:0])

OS_SEQ_PROP [1:0]	(A2) Power Relay Open check (B) Power Relay Short check [ms]
0	0.1
1	1.0
2	10.0
3	20.0

Static Open/Short check detection threshold voltage between VB-DRN is set by register (OS_DETVTH [1:0])

OS_DETVTH [1:0]	Detection Threshold Voltage Between VB-DRN [V]
0	0.5
1	1.0
2	1.5
3	2.0

(C) High/Low-side FET Short check
Short failure of high-side / low-side FET is detected by turning all FET into OFF state and monitoring VDS voltage. IC can change VDS thresh by VDSL register.
Short check of high-side / low-side FET, and check for Motor short-to-ground faults are performed by the following two sequences.

1. SxH is pulled down, and if the voltage between DRN-SxH doesn't exceed 0.5V (Typ), it is judged as Open failure of high-side FET.
2. SxH is pulled up, and if the voltage between SxH-SxL doesn't exceed 0.5 V (Typ), it is judged as short failure of low-side FET.
   If low-side FET of all three phases are judged as short failure, it is judged as Motor short-to-ground fault.

(D) High/Low-side FET Open check
Open failure of high-side / low-side FET is detected by turning sequentially each FET into ON state and monitoring VDS voltage.
open check of high-side / low-side FET is performed by the following two sequences.

1. SxH is pulled down when high-side FET is turned ON, and if the voltage between DRN-SxH exceeds 0.5 V (Typ), it is judged as Open failure of high-side FET
2. SxH is pulled up when low-side FET is turned ON, and if the voltage between SxH-SxL exceeds 0.5 V (Typ), it is judged as Open failure of low-side FET.

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7. Protection Function - Continued

(E) Motor output to VB check

Moror short-to-VB fault is detected by turning motor relay and monitoring VDS voltage.
SxH is pulled down, and if the voltage between DRN-SxH for all three phases doesn't exceed 0.5V (Typ), it is judged as Motor short-to-VB fault.

(F) Motor Relay Short check

Short failure of motor relay is detected by turning motor relay into OFF state and monitoring VDS voltage.
SxH is pulled down, and if the voltage between DRN-SxH doesn't exceed 1.5 V (Typ), it is judged as short failure of motor relay.
The period of Sequence (F) can be set by OS_SEQ_MR1SH.
Static Short Check detection period of Sequence (F) is set by register (OS_SEQ_MR1SH [1:0])

(G) Motor Relay Open check

Open failure of motor relay is detected by turning motor relay into ON state and monitoring VDS voltage.
SxH is pulled down, and if the voltage between DRN-SxH exceeds 0.5 V (Typ), it is judged as Open failure of motor relay.
The period of Sequence (G) can be set by OS_SEQ_MR1SH.

OS_SEQ_MR1SH [1:0]	(F) Motor Relay Short check [ms]	(G) Motor Relay Open check [ms]
0	0.5	0.3
1	0.6	0.4
2	0.9	0.7
3	1.4	1.2

Note that shorted FET of high-side and low-side cannot be identified in case of no motor relay in the circuit.
Note that in circuit B, DRN_UV and VCPH_DRN_UV detection should be masked when power relay is off (R2OFF = '1' in register) because DRN level will be Hi-Z.

The register End (OS) becomes '1' after end of the static detection.

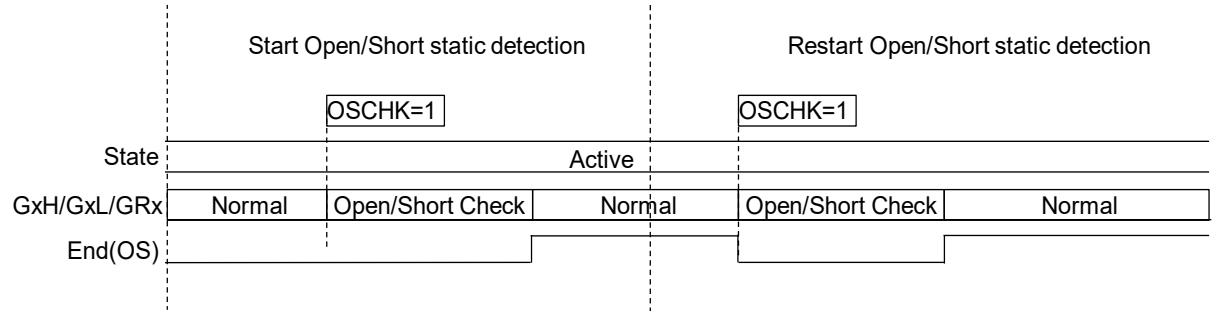


Figure 44. Behavior of End (OS)

During Static OS detection, Some Error Detections are masked or protection is disabled. Refer to the table below.

Error Detection		
VB OV VCC OV REF OV VDD OV / UV VCP OV Static OS TW/TSD OSC Freq OSC Stop WDT SPI Stop SPI REG Internal	VB UV VCC UV REF UV VCP UV DRN UV VGS/VGSR VDS SNT	Dynamic OS TDEAD
Error detection and protection are same as active state	Error detection is same as active state Protection is disabled	Error detection and protection are disabled.

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7. Protection Function - Continued

7.8.2 Dynamic OS Detection

Dynamic OS detection always monitoring open / short state of external MOS-FET during motor rotation. But this detection cannot detect Short / Open in Motor / Power Relay.
This detection is used VDS and SNT detection circuit and VDS and SNT comparator (VDSSxH, VDSSxL, VSHUNTx (x = 1,2,3). If MCU wants to execute Dynamic OS Detection, MCU needs to set the following settings.

ErrorMask (VDS) = 0
ErrorMask (SNT) = 0
ProtectMode (VDS) = 1
ProtectMode (SNT) = 1

The detection conditions for Open and Short are shown in the table below. If VDSSxH or VDSSxL is H, it is affected by t_{VDS_MSK} and t_{VDS_FLT}. If VSHUNTx is H, it is affected by t_{SNT_MSK} and t_{SNT_FLT}.

INxH	INxL	VDSSxH	VDSSxL	VSHUNTx	Register
H	L	H	L	L	ErrorOpen(xH) = 1
L	H	L	H	L	ErrorOpen(xL) = 1
L	H	L	*	H	ErrorOpen2(xL) = 1
L	H	H	H	H	ErrorShort(xH) = 1
H	L	H	H	H	ErrorShort(xL) = 1
H	L	H	H	L	ErrorShort2(xL) = 1

Dynamic OS detection will be detected even if gate outputs are turned off by DOFFB = L.
Short error can be detected in case of the short resistance ≤ 150mΩ (where VB = 12 V, FET's Ron = 0.65mΩ, Shunt resistor = 0.50 mΩ, VDS Abnormal Detection Threshold Voltage = 50 mV and Shunt Resistor Abnormal Detection Threshold Voltage = 33.3 mV. VB current is 80 A)

The timing chart below shows when an error occurs and when it does not.

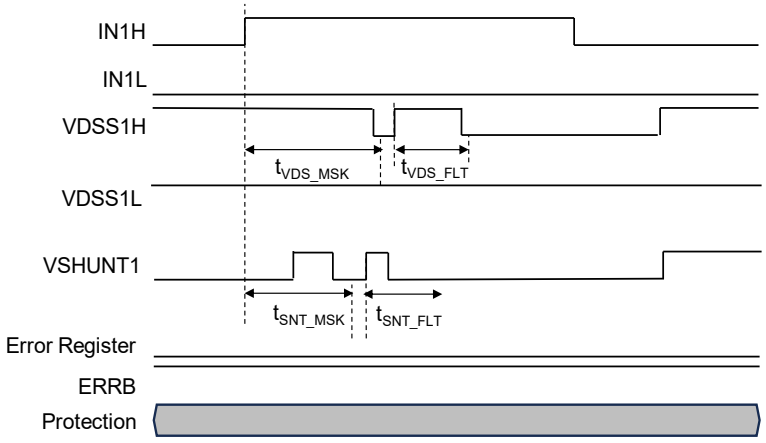


Figure 45. No-error pattern Timing Chart for Dynamic OS

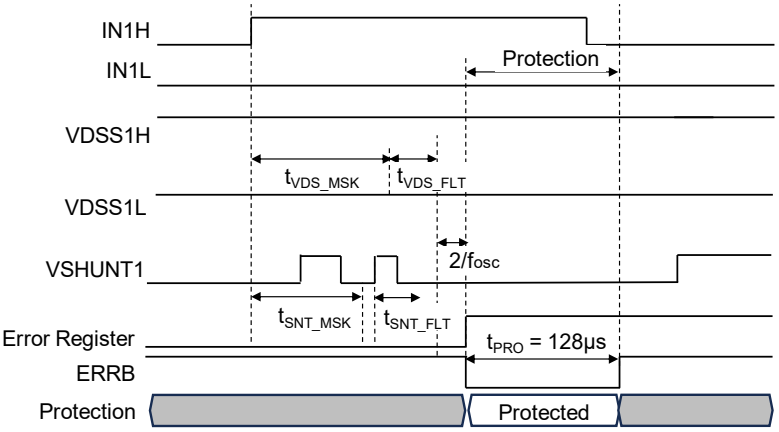


Figure 46. Error pattern Timing Chart for Dynamic OS

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7. Protection Function - Continued

7.9 Thermal Shutdown (TSD) / Thermal Warning (TW)

When the junction temperature exceeds 135 °C (Typ), a thermal warning (TW) is detected (Error (TW) = '1'). In this state, the IC itself raises an error flag, but continues normal operation.

And the temperature rises further and the junction temperature reaches 175 °C (Typ), the thermal shutdown function TSD operates, TSD error is detected (Error (TSD) = ’1’) and all gate output turns off. When the junction temperature falls below 150 °C (Typ), the gate output resumes operation when ProtectKeep (TSD) = '0'

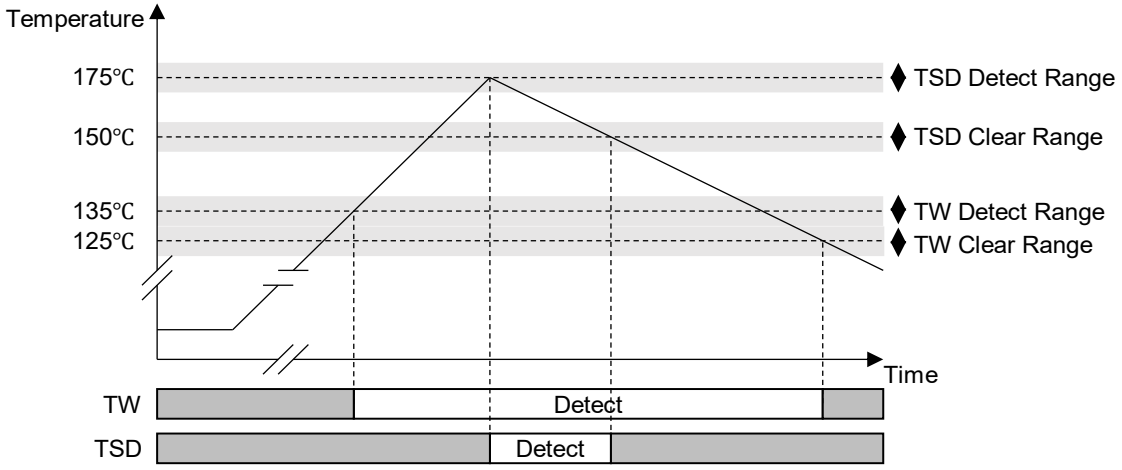


Figure 47. Graph of temperature for TSD / TW

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7. Protection Function - Continued

7.10 Watch Dog Timer (WDT)

The purpose of WDT is to monitor the abnormal condition of MCU. IC monitors SPI communication status with MCU. IC supports three modes of WDT: Time-out mode, Window mode, Q&A mode. MCU can select the mode by WDEN register. In any mode, WDT counter can be cleared by sending a specific command from MCU. Specific command is selected by WEDN. If timeout period (t_{WDTMAX}) is exceeded without clearing WDT counter, WDT is judged to be FAIL. The specified period selected by WDTO register. In Window mode and Q&A mode, WDT sets the minimum period during which specific command can be received (t_{WDTMIN}).

WDEN [1:0]	WD mode
0	WDT is stopped.
1	WDT is started in Timeout mode. If MCU write WDCHK = 1, WDT counter is cleared. If t_{WDTMAX} is exceeded without clearing WDT counter, WDT is judged as FAIL.
2	WDT is started in Window mode. If MCU write WDCHK = 1 in the period t_{WDTMIN} to t_{WDTMAX}, WDT counter is cleared. If it is outside the period, WDT is judged as FAIL.
3	WDT is started in Q&A mode. MCU read a question from WDQ register, write an answer to WDA register in the period t_{WDTMIN} to t_{WDTMAX}. If the answer from MCU is correct, WDT counter is cleared. If it is incorrect or outside the period, WDT is judged as FAIL. The solution to the question is described in 7.10.3 QA mode (WDEN = 3)

If WDT is judged as FAIL, Fail Counter is incremented by 2. If WDT counter is cleared, Fail Counter is decremented by 1. Fail Counter can be read from WDTFC register.

When Fail Counter reaches Max of Fail Counter selected by FCMAX, Error (WDT) is set 1 and ERRB becomes low.

Set a register WDTO for detection period of WDT following table below.

WDTO [1:0]	minimum period (t_{WDTMIN}) [ms]	timeout period (t_{WDTMAX}) [ms]
0	2	6
1	4	12
2	15	45
3	32	96

Set register FCMAX for max of fail counter following table below.

FCMAX [1:0]	Max of Fail Counter
0	2
1	6
2	10
3	14

7.10.1 Timeout mode (WDEN=1)

MCU must write WDCHK = 1 by t_{WDTMAX}.
The timing charts for correct and wrong patterns are as follows.

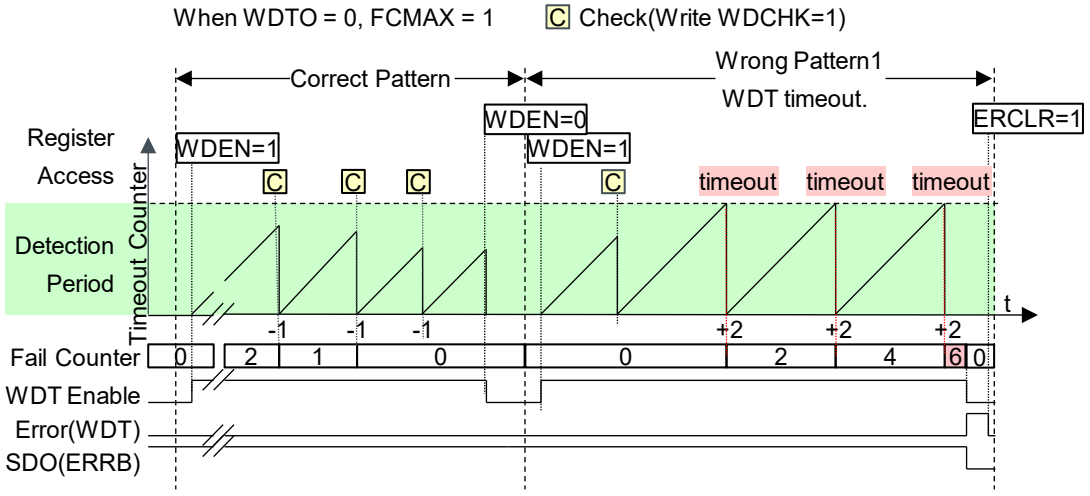


Figure 48. Timing Chart for WDT in Timeout mode

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7. Protection Function - Continued

7.10.2 Window mode (WDEN = 2)

MCU must write WDCHK = 1 from t_{WDTMIN} to t_{WDTMAX}.
The timing charts for correct and wrong patterns are as follows.

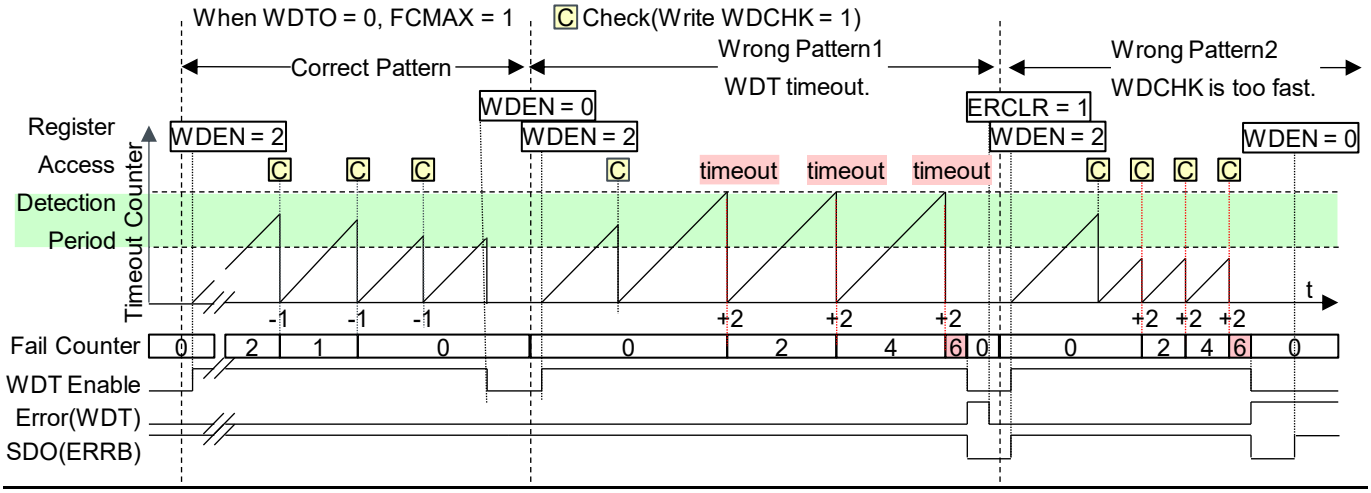


Figure 49. Timing Chart for WDT in Window mode

7.10.3 QA mode (WDEN = 3)

MCU must write correct answer to WDA from t_{WDTMIN} to t_{WDTMAX}.

Flow of Question-and-answer Generation in IC:
1. WDQ_pre is generated based on Seed register (WDSD) in Linear Feedback Shift Register (LFSR).
2. The question (WDQ) is calculated by exclusive OR of the WDQ_pre and WDCF register.
3. The answer can be generated based on WDQ. MCU can select a conversion method from 4 mode by WDAS register.
4. If MCU writes the answer of WDQ (WDA), IC compares WDA and answer generated in IC. If it is equal, WDT counter is cleared and WDQ_pre is regenerated. If it isn't equal, WDT is judged as FAIL.

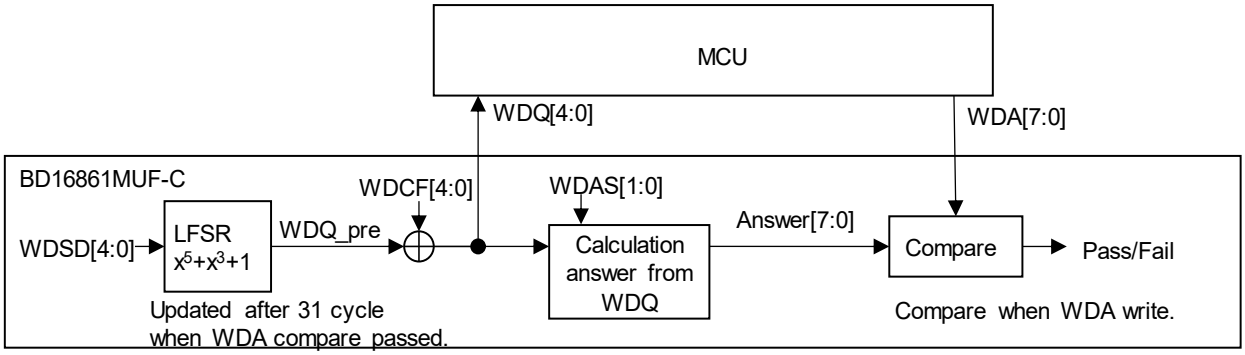


Figure 50. WDQ and WDA calculation flow

Calculation Answer [7:0] from WDQ by WDAS (~: Invert)

WDAS [2:0]	Answer [7:0]							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	~WDQ[4]	~WDQ[3]	~WDQ[2]	~WDQ[1]	~WDQ[0]	~WDQ[4]	~WDQ[3]	~WDQ[2]
1	~WDQ[0]	~WDQ[1]	~WDQ[2]	~WDQ[3]	~WDQ[4]	~WDQ[0]	~WDQ[1]	~WDQ[2]
2	1	1	1	~WDQ[4]	~WDQ[3]	~WDQ[2]	~WDQ[1]	~WDQ[0]
3	0	0	0	WDQ[4]	WDQ[3]	WDQ[2]	WDQ[1]	WDQ[0]

The timing charts for correct and wrong patterns are as follows.

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7. Protection Function - Continued

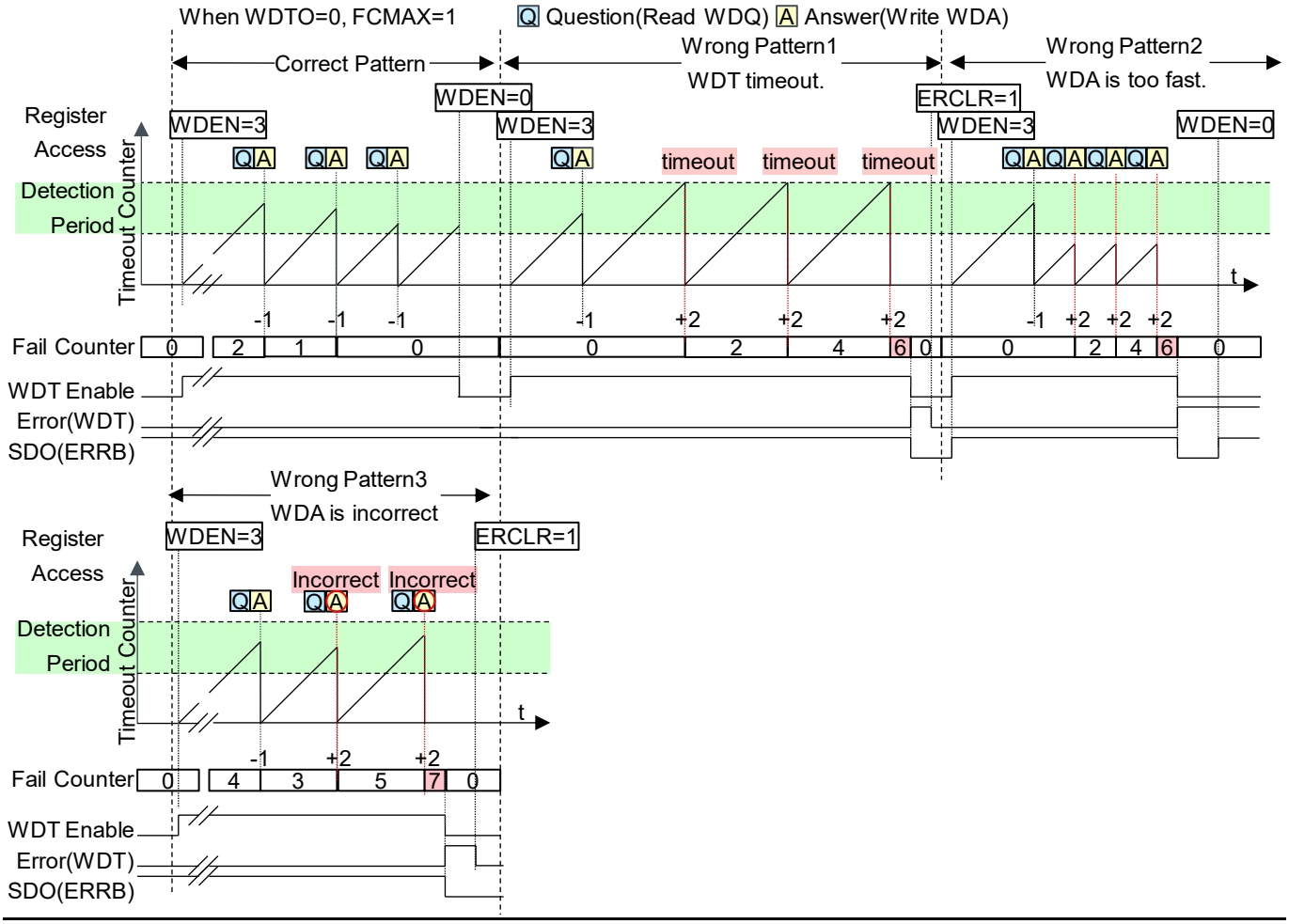


Figure 51. Timing Chart for WDT in Q&A mode

7.10.4 WDT on Startup sequence

When transitioning from Stand-by to CPON state, WDT counter must be cleared at least once.
The conditions depend on WDEN and ErrorMask (WDT) registers. Refer to the figure below.

ErrorMask (WDT)	WDEN	WDT Conditions of CPON state
1	*	Do nothing
0	0	
	1	Write WDCHK = 1 before timeout period (until t_{WDTMAX})
	2	Write WDCHK = 1 in the period minimum to timeout. (t_{WDTMIN} to t_{WDTMAX})
	3	Write correct WDA in the period minimum to timeout. (t_{WDTMIN} to t_{WDTMAX})

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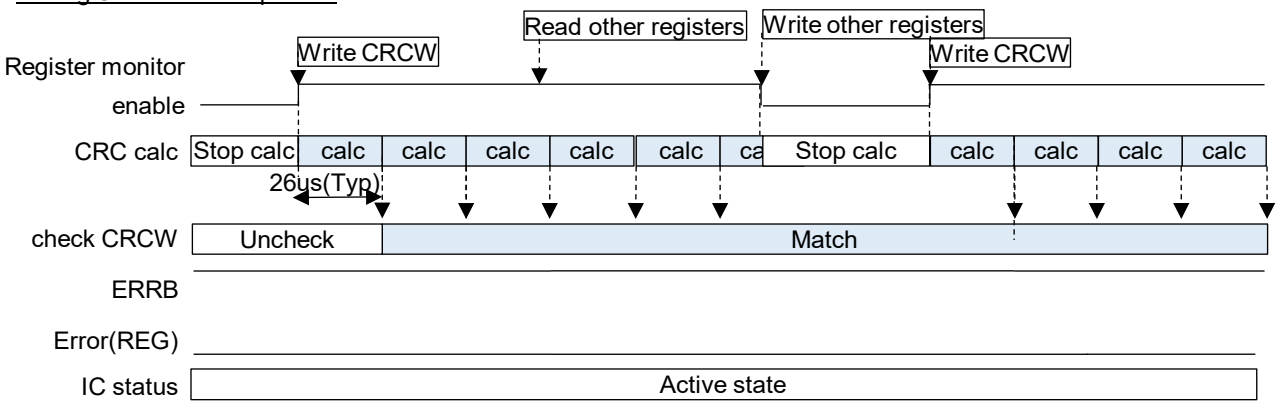
7. Protection Function - Continued

7.11 Register (REG) Monitor

This IC has a register monitor function to detect unintended changes caused by electric noise. This IC calculates CRC of writable registers regularly (CRCR) and compares CRCR with CRCW register written by MCU. When CRCW and CRCR are not equal, Error(REG) = 1 is set. The register monitor operates from the time CRCW is written until write access of other registers.

Register	Function
CRCW [15:0]	Expected CRC code written by the MCU
CRCR [15:0]	CRC code calculated by the IC, read-only resister

Timing Chart : Normal pattern



Timing Chart : Error pattern

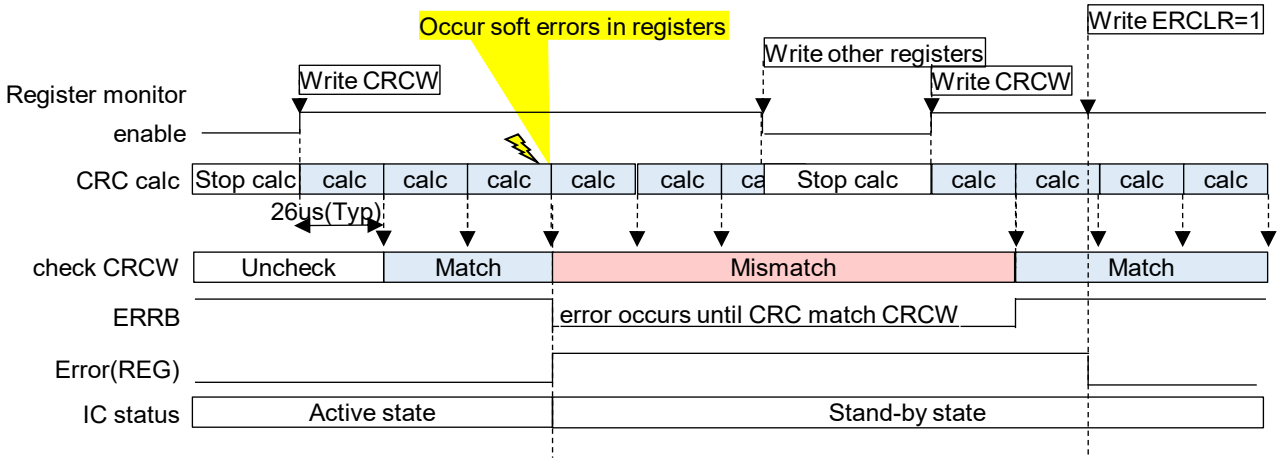


Figure 52. Timing Chart for Register Monitor

The registers that are protected by Register Monitor are as follows.

Register Monitor	
Protected Register's address	01h, 02h, 0Dh to 1Ah
CRC Calculate Data	256bits = 16bit x 16regs

The assignment of CRC calculation data and registers is as follows.

CRC Calculate Data Bits	Address of Target registers	CRC Calculate Data Bits	Address of Target registers
[255:240]	01h	[127:112]	13h
[239:224]	02h	[111:96]	14h
[223:208]	0Dh	[95:80]	15h
[207:192]	0Eh	[79:64]	16h
[191:176]	0Fh	[63:48]	17h
[175:160]	10h	[47:32]	18h
[159:144]	11h	[31:16]	19h
[143:128]	12h	[15:0]	1Ah

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7. Protection Function - Continued

The specifications of CRC used in Register Monitor are as follows.

CRC Specification	
CRC result width	16bits
Polynomial	8005h = $x^{16} + x^{15} + x^2 + 1$
Initial value	0000h
Input data reflected	No
Result data reflected	No
XOR value	0000h

Example:
Register on Addr. 01h = 0001h,
Register on Addr. 02h = 0001h,
Other registers = default value
CRC-result = CRCW value = 44a2h

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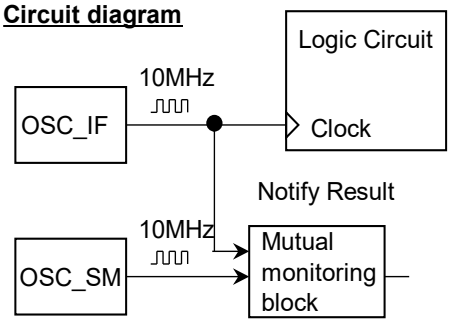
7. Protection Function - Continued

7.12 Oscillation (OSC) Error Detection

7.12.1 OSC Frequency Error Detection

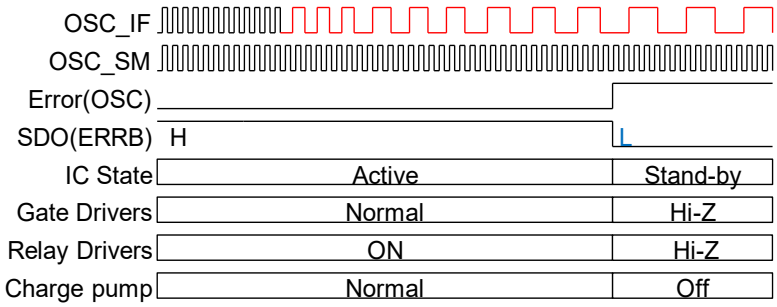
This is a function that oscillators for logic control monitor mutually and they detect an error when the frequency is out of range (-20 % to +20 %). Two oscillators are implemented, and they can inform detected errors after the detection.
This function is disabled when ErrorMask (OSC) = “1”

Circuit diagram



OSC error detects
when clock frequency faster
20% or slower 20% than
another clock frequency.

OSC_IF has failure



OSC_SM has failure

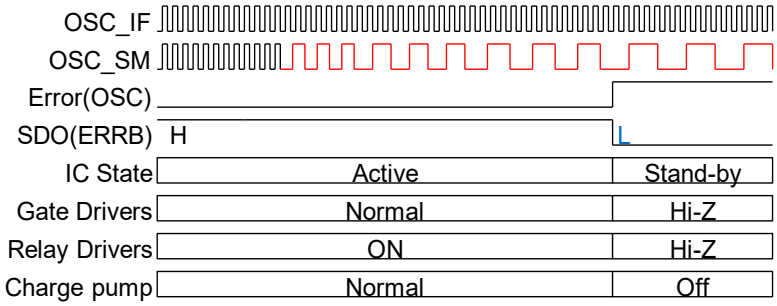


Figure 53. Circuit diagram and Timing chart for OSC Frequency Error

7.12.2 OSC Stop Detection

This is a function that oscillators for logic control monitor mutually and they detect an error when oscillation continue to stop over 25µs. This IC change to Sleep when Oscillation stop is detected. OSC stop detection is enable in all states except SLEEP and DBIST state.
OSC (Main) stop can be detected at ErrorMask (OSC) = 1.
OSC (Sub) stop can’t be detected at ErrorMask (OSC) = 1.
Describes the relationship between Error (OSC) and ErrorMask (OSC).

OSC Condition		ErrorMask (OSC) = 0		ErrorMask (OSC) = 1	
OSC_IF	OSC_SM	Error (OSC)	State	Error (OSC)	State
Normal freq.	Normal freq.	0	Unchanged	0	Unchanged
	Abnormal freq.	1	Go to Stand-by		
	Clock Stop		Go to Sleep		
Abnormal freq.	Normal freq.		Go to Stand-by		
Clock Stop			Go to Sleep		Go to Sleep

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7. Protection Function - Continued

7.13 SPI Error Detection

SPI Error is detected in the following cases
- CRC error
- Frame counter error
- SCK over 32 pulses error
- SCK under 32 pulses error

IC will not receive data to the registers if the command has any of 4 errors.
And it will notify the error to MCU via ERRB and a read register Error (SPI).
IC status after these error detections can be selected by ProtectMode (SPI) register.
(Refer to 7.1 Protection After Error Detection)

These SPI errors can be masked by ErrorMask (SPI) register.
When ErrorMask (SPI) = 1, if SPI command is less than SCK 32 clock cycles, this command is ignored.
However, protection after SPI Error is masked, and Error (SPI) is not triggered.

Cases	ErrorMask (SPI) = 0	ErrorMask (SPI) = 1
SPI CRC error is detected	Ignore command	Accept command
Frame counter error is detected		
SCK over 32 error is detected		
SCK under 32 error is detected		Ignore command

7.13.1 CRC error detection

If CRC of the command sent from MCU does not match, an error is detected.

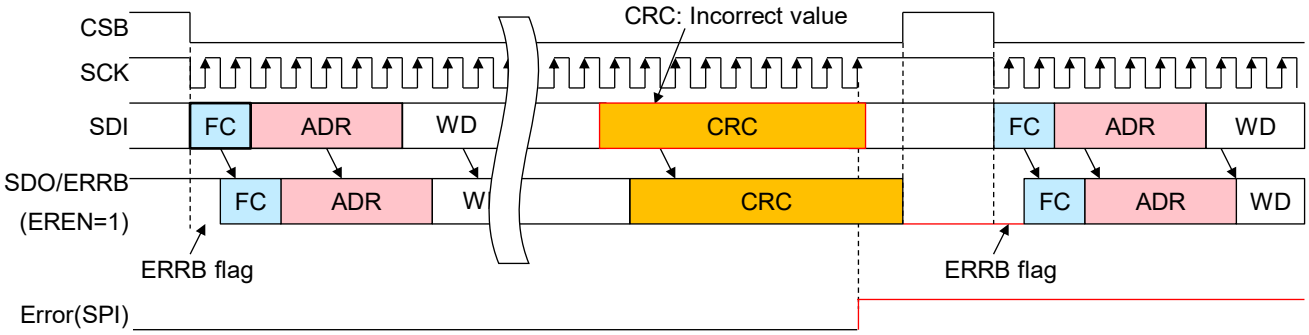


Figure 54. Timing chart for CRC error

SPI command from MCU				SCK Cycle	SPI receive in IC		Error detection			Output
FC	ADR	WD	CRC	NUM	SPI access	FC	CRC	FC	SCK	ERRB
0	01h	0001h	F0h	32	Write	-	Pass	Pass	Pass	H
1	0Dh	0513h	07h	32	Write	0	Pass	Pass	Pass	H
0	01h	0000h	67h	32	Write	1	Pass	Pass	Pass	H
3	08h	xxxxh	xxh	32	Read	0	Uncheck	Pass	Pass	H
0	01h	0001h	F0h	32	Write	3	Pass	Pass	Pass	H
1	16h	0000h	E9h	32	Ignore	0	Error	Pass	Pass	H
2	12h	00C6h	FDh	32	Write	1	Pass	Pass	Pass	L
3	0Eh	0034h	87h	32	Write	2	Pass	Pass	Pass	H
0	02h	0001h	59h	32	Write	3	Pass	Pass	Pass	H
1	01h	0000h	3Fh	32	Write	0	Pass	Pass	Pass	H
2	04h	xxxxh	xxh	32	Read	1	Uncheck	Pass	Pass	H

Figure 55. SPI command samples when CRC error

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7. Protection Function - Continued

7.13.2 FC error detection

If FC value is equal to FC value in previous command, an error is detected.

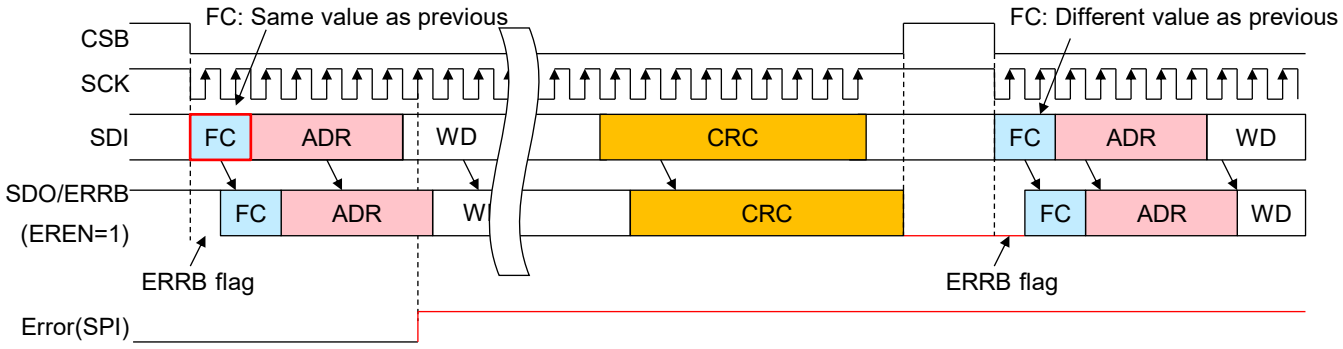


Figure 56. Timing chart for FC error

SPI command from MCU				SCK Cycle	SPI receive in IC		Error detection			Output
FC	ADR	WD	CRC	NUM	SPI access	FC	CRC	FC	SCK	ERRB
0	01h	0001h	F0h	32	Write	-	Pass	Pass	Pass	H
1	0Dh	0513h	07h	32	Write	0	Pass	Pass	Pass	H
0	01h	0000h	67h	32	Write	1	Pass	Pass	Pass	H
3	08h	xxxxh	xxh	32	Read	0	Uncheck	Pass	Pass	H
0	01h	0001h	F0h	32	Write	3	Pass	Pass	Pass	H
0	16h	0000h	E9h	32	Ignore	0	Pass	Error	Pass	H
2	12h	00C6h	FDh	32	Write	0	Pass	Pass	Pass	L
3	0Eh	0034h	87h	32	Write	2	Pass	Pass	Pass	H
0	02h	0001h	59h	32	Write	3	Pass	Pass	Pass	H
1	01h	0000h	3Fh	32	Write	0	Pass	Pass	Pass	H
2	04h	xxxxh	xxh	32	Read	1	Uncheck	Pass	Pass	H

Figure 57. SPI command samples when FC error

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7. Protection Function - Continued

7.13.3 SCK over 32 error detection

If the number of SCK cycles per command exceeds 32, an error is detected.

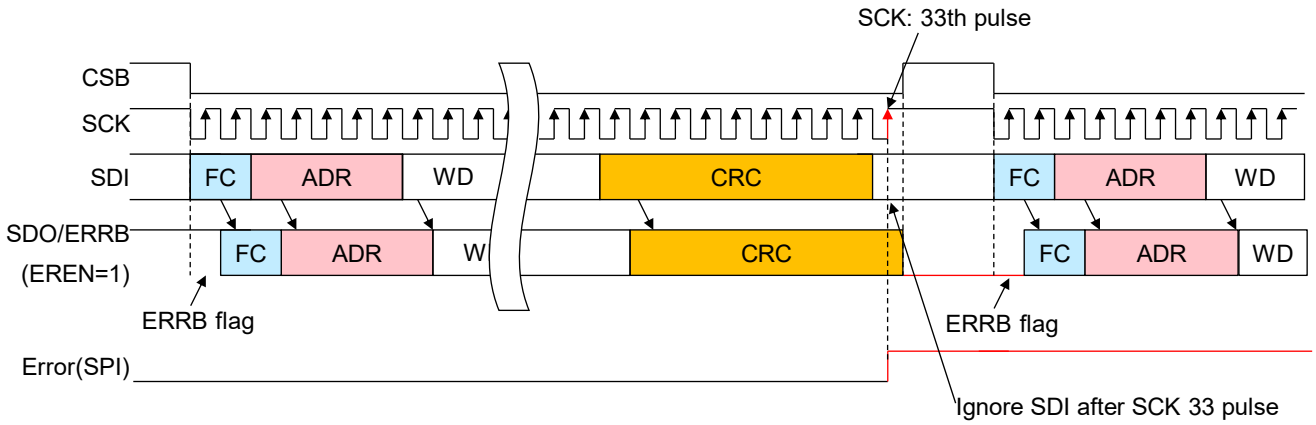


Figure 58. Timing chart for SCK over 32 error

SPI command from MCU				SCK Cycle	SPI receive in IC		Error detection			Output
FC	ADR	WD	CRC	NUM	SPI access	FC	CRC	FC	SCK	ERRB
0	01h	0001h	F0h	32	Write	-	Pass	Pass	Pass	H
1	0Dh	0513h	07h	32	Write	0	Pass	Pass	Pass	H
0	01h	0000h	67h	32	Write	1	Pass	Pass	Pass	H
3	08h	xxxxh	xxh	32	Read	0	Uncheck	Pass	Pass	H
0	01h	0001h	F0h	32	Write	3	Pass	Pass	Pass	H
1	16h	0000h	B1h	33	Ignore	0	Pass	Pass	Error	H
2	12h	00C6h	FDh	32	Write	1	Pass	Pass	Pass	L
3	0Eh	0034h	87h	32	Write	2	Pass	Pass	Pass	H
0	02h	0001h	59h	32	Write	3	Pass	Pass	Pass	H
1	01h	0000h	3Fh	32	Write	0	Pass	Pass	Pass	H
2	04h	xxxxh	xxh	32	Read	1	Uncheck	Pass	Pass	H

Figure 59. SPI command samples when SCK over 32 error

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7. Protection Function - Continued

7.13.4 SCK under 32 error detection

If the number of SCK cycles per command is less than 32, and error is detected. However, when it is 0 cycles, error is not detected.

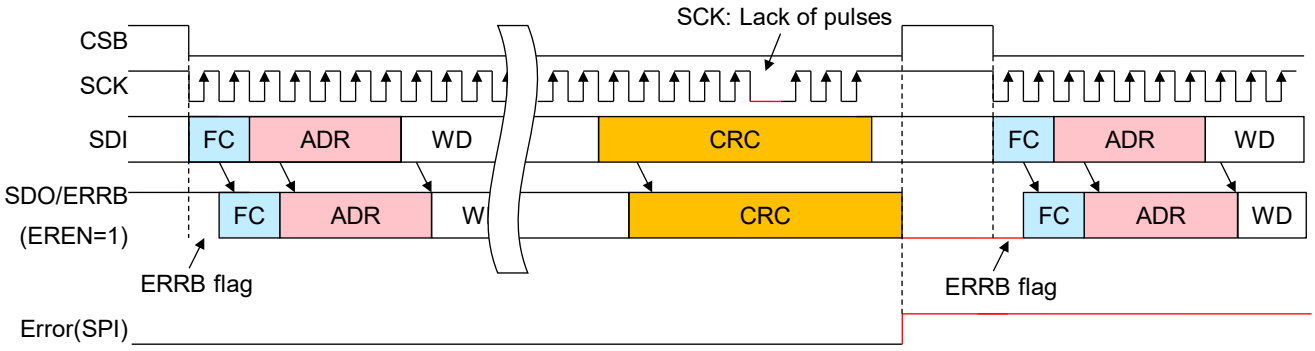


Figure 60. Timing chart for SCK under 32 error

SPI command from MCU				SCK Cycle	SPI receive in IC		Error detection			Output
FC	ADR	WD	CRC	NUM	SPI access	FC	CRC	FC	SCK	ERRB
0	01h	0001h	F0h	32	Write	-	Pass	Pass	Pass	H
1	0Dh	0513h	07h	32	Write	0	Pass	Pass	Pass	H
0	01h	0000h	67h	32	Write	1	Pass	Pass	Pass	H
3	08h	xxxxh	xxh	32	Read	0	Uncheck	Pass	Pass	H
0	01h	0001h	F0h	32	Write	3	Pass	Pass	Pass	H
1	16h	0000h	B1h	31	Ignore	0	Pass	Pass	Error	H
2	12h	00C6h	FDh	32	Write	0	Pass	Pass	Pass	L
3	0Eh	0034h	87h	32	Write	2	Pass	Pass	Pass	H
0	02h	0001h	59h	32	Write	3	Pass	Pass	Pass	H
1	01h	0000h	3Fh	32	Write	0	Pass	Pass	Pass	H
2	04h	xxxxh	xxh	32	Read	1	Uncheck	Pass	Pass	H

Figure 61. SPI command samples when SCK under 32 error

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7. Protection Function - Continued

7.14 SPI Stop Detection

IC automatically change the state to sleep state when SPI stops over 10s if there are any SPI errors. This error is not notified to MCU. If there is a good SPI communication (No SPI errors), internal timer for counting 10s is reset.

When WDT is used at the same time, this detection starts after WDT error detected. After WDT error detection and SPI error state keeps 10s, IC enters sleep state.

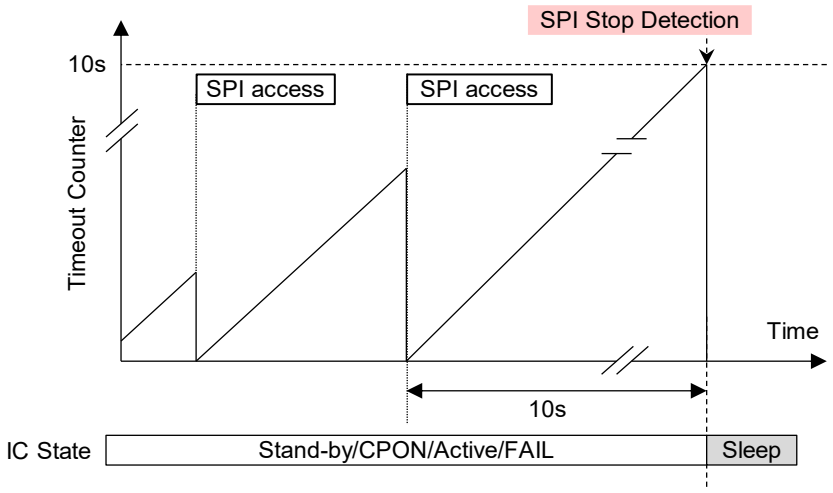


Figure 62. Timing Chart for SPI Stop

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8. Absolute Maximum Ratings

Item		Symbol	Rated Value			Unit
Supply Voltage	VB	V_{VB}	-0.3	to	+60	V
	VCC	V_{VCC}	-0.3	to	+60	V
Input Voltage	IN1H, IN1L, IN2H, IN2L, IN3H, IN3L, DOFFB	V_{IN1H}, V_{IN1L}, V_{IN2H}, V_{IN2L}, V_{IN3H}, V_{IN3L}, V_{DOFFB}	-0.3	to	+60	V
	SCK, SDI, CSB	V_{SCK}, V_{SDI}, V_{CSB}				
	AIN1P, AIN2P, AIN3P	V_{AIN1P}, V_{AIN2P}, V_{AIN3P}	-5.0	to	+7.0	V
	AIN1N, AIN2N, AIN3N	V_{AIN1N}, V_{AIN2N}, V_{AIN3N}				
	REF	V_{REF}	-0.3	to	+60	V
	DRN	V_{DRN}	-0.3	to	+60	V
Output Voltage	VDD	V_{VDD}	-0.3	to	+7.0	V
	SDO	V_{SDO}	-0.3	to	+60	V
	AOUT1, AOUT2, AOUT3	V_{AOUT1}, V_{AOUT2}, V_{AOUT3}	-0.3	to	+7.0	V
	VCPH, CP2H	V_{VCPH}, V_{CP2H}	-0.3	to	+60	V
	VCPH-VB	-	-0.3	to	+15.5	V
	VCPH-CP2H	-	-0.3	to	+22	V
	VCPL	V_{VCPL}	-0.3	to	+14	V
	VCPL-VDD	-	-0.3	to	+7.0	V
	G1H, G2H, G3H	V_{G1H}, V_{G2H}, V_{G3H}	-5.0	to	+60	V
	S1H, S2H, S3H	V_{S1H}, V_{S2H}, V_{S3H}	-5.0	to	+60	V
	G1H-S1H, G2H-S2H, G3H-S3H	-	-0.3	to	+20	V
	G1L, G2L, G3L	V_{G1L}, V_{G2L}, V_{G3L}	-5.0	to	+14	V
	S1L, S2L, S3L	V_{S1L}, V_{S2L}, V_{S3L}	-5.0	to	+5.0	V
	G1L-S1L, G2L-S2L, G3L-S3L	-	-0.3	to	+20	V
	GR1, GR2, GR3	V_{GR1}, V_{GR2}, V_{GR3}	-0.3	to	+60	V
	CP2L, CP1H	V_{CP2L}, V_{CP1H}	-0.3	to	+14	V
	CP1L	V_{CP1L}	-0.3	to	+7.0	V
Output Current	VCPH, VCPL	I_{VCPH}, I_{VCPL}	0	to	30	mA
	VDD	I_{VDD}	0	to	40	mA
	SDO	I_{SDO}	0	to	5	mA
	AOUT1, AOUT2, AOUT3	I_{AOUT1}, I_{AOUT2}, I_{AOUT3}	0	to	10	mA
Maximum Slew Rate of SxH (x = 1, 2, 3)		T_{SR}	-300	to	+300	V/us
Storage Temperature Range		Tstg	-55	to	+150	°C
Maximum Junction Temperature		Tjmax	150			°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

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9. Thermal Resistance

Based on JESD51-2A (Still-Air).

Parameter	Symbol	Terminal Resistance (Typ)		Unit
		1s (Note2)	4s (Note3)	
VQFN48FBV070				
Junction to Ambient	θ_{JA}	67.8	24.6	°C/W
Junction to Top Characterization Parameter (Note 1)	Ψ_{JT}	8	6	°C/W

(Note 1) Thermal characteristic parameters from junction to package top center (mold).
(Note 2) Using based on JESD51-3.
(Note 3) Using based on JESD51-5,7.

Number of layers in Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Number of layers in Measurement Board	Material	Board Size	Thermal Via (Note4)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm^2 (Square)	35 µm	74.2 mm^2 (Square)	70 µm

(Note 4) This thermal via connects with 1st, 2nd and 4th layer copper patterns.

10. Recommended Operating Conditions

Parameter	Symbol	Spec			Unit
		Min	Typ	Max	
Power Supply	V_{VB}	6.0 (Note 1)	12.0	32.0	V
		4.5 (Note 2)	12.0	32.0	V
	V_{VCC}	3.0	5.0	5.5	V
Input Pin	V_{REF}	3.0	5.0	5.5	V
Operating Temperature	Topr	-40	+25	+125	°C

(Note 1) VB of 6.0 V or higher is required for the transition from Sleep State to Stand-by State.
(Note 2) VB of 4.5V or higher is required for the transition after Stand-by State.

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11. Electrical Characteristics

11.1 Electrical Characteristics (Circuit Current, Input Pin)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND *(Note 1)*)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[All]						
VB Sleep Current	I_{VBSLP}	-	0	10	µA	Sleep state
VB STBY Current Including VDD internal power supply current	I_{VBSTB}	-	16	28	mA	Stand-by state VB = 12 V
VB Operating Circuit Current	I_{VBACT}	-	40	55	mA	Active state VB = 12 V SPI Communication Stopped
VCC Sleep Current	I_{VCCSLP}	-	3	8	µA	Sleep state
VCC STBY Current	I_{VCCSTB}	-	300	650	µA	Stand-by state VB = 12 V When SDO output L
VCC Operating Circuit Current	I_{VCCACT}	-	0.8	2.0	mA	Active state VB = 12 V SPI Communication Stopped
[Half Bridge Gate PWM Input Pin IN1H / IN1L / IN2H / IN2L / IN3H / IN3L Characteristic]						
Input Voltage L Level	V_{INxL}	0	-	Vvcc x 0.2	V	
Input Voltage H Level	V_{INxH}	Vvcc x 0.8	-	Vvcc	V	
Input Current L Level	I_{INxL_SLP}	-10	0	+10	µA	V_{INxH} = V_{INxL} = 0 V (x = 1,2,3)
Input Current H Level	I_{INxH_SLP}	-	10	40	µA	V_{INxH} = V_{INxL} = 5V (x = 1,2,3) Sleep Mode
	I_{INxH_STB}	-	20	100	µA	V_{INxH} = V_{INxL} = 5V (x = 1,2,3) Stand-by state
[Gate Drive ON/OFF Pin DOFFB Characteristic]						
Input Voltage L Level	V_{DOFFBL}	0	-	Vvcc x 0.2	V	
Input Voltage H Level	V_{DOFFBH}	Vvcc x 0.8	-	Vvcc	V	
Input Current L Level	I_{DOFFBL}	-10	0	+10	µA	V_{DOFFB} = 0.0 V
Input Current H Level	I_{DOFFBH}	-	15	50	µA	V_{DOFFB} = 5.0 V
[Serial Input Pin CSB, SCK, SDI Characteristic]						
Input Voltage L Level	V_{CSBL}, V_{SCKL}, V_{SDIL}	0	-	Vvcc x 0.2	V	
Input Voltage H Level	V_{CSBH}, V_{SCKH}, V_{SDIH}	Vvcc x 0.8	-	Vvcc	V	
Input Current L Level	I_{SCKL}, I_{SDIL}	-10	0	+10	µA	V_{SCK} = V_{SDI} = 0 V
	I_{CSBL_SLP}	-10	0	+10	µA	V_{CSB} = 0 V, Sleep state
	I_{CSBL_STB}	-50	-15	-	µA	V_{CSB} = 0 V, Stand-by/Active state
Input Current H Level	I_{SCKH_SLP}, I_{SDIH_SLP}	-10	0	+10	µA	V_{SCK} = V_{SDI} = 5 V, Sleep state
	I_{SCKH_STB}, I_{SDIH_STB}	-	15	50	µA	V_{SCK} = V_{SDI} = 5 V, Stand-by/Active state
	I_{CSBH}	-10	0	+10	µA	V_{CSB} = 5 V
[Serial Output Pin SDO Characteristic]						
Output Voltage Low Level	V_{SDOL}	-	-	0.6	V	I_{SDO} = 1.0 mA
Output Voltage High Level	V_{SDOH}	V_{VCC} -0.6	-	Vvcc	V	I_{SDO} = -1.0 mA

Regarding current items, + notation is for current inflow to IC, -notation is for current outflow from IC.

(Note 1) This condition is only for measurement purposes, in normal use it will be connected to 1/2/3 phases of motor.

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11. Electrical Characteristics - Continued

11.2 Electrical Characteristics (Internal Power Supply)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[Oscillator]						
Oscillation Frequency	f_{OSC}	9.0	10.7	12.3	MHz	V_{VB} = 4.5V to 5.5V
		9.3	10.7	12.0	MHz	V_{VB} = 5.5 V to 32 V
[Boosted Voltage] *(Note 1)*						
VCPH Boosted Voltage VCPL Boosted Voltage	V_{VCPH1}	V_{VB}+6.0	-	-	V	V_{VB} =4.5 V to 6.0 V, I_{VCPH} = -5 mA, I_{VCPL} = -5 mA
		V_{VB}+9.0	V_{VB}+10.6	V_{VB}+12.0	V	V_{VB} = 6.0 V to 32 V, I_{VCPH} = -5 mA, I_{VCPL} = -5 mA
	V_{VCPL1}	7.0	-	-	V	V_{VB} = 4.5 V to 6.0 V, I_{VCPH} = -5 mA, I_{VCPL} = -5 mA
		9.0	10.6	12.0	V	V_{VB} = 6.0 V to 32 V, I_{VCPH} = -5 mA, I_{VCPL} = -5 mA
	V_{VCPH2}	V_{VB}+6.0	-	-	V	V_{VB} = 4.5 V to 7.0 V, I_{VCPH} = -10mA, I_{VCPL} = -10 mA
		V_{VB}+9.0	V_{VB}+10.6	V_{VB}+12.0	V	V_{VB} = 7.0 V to 32 V, I_{VCPH} = -10mA, I_{VCPL} = -10 mA
	V_{VCPL2}	7.0	-	-	V	V_{VB} = 4.5 V to 7.0 V, I_{VCPH} = -10mA, I_{VCPL} = -10 mA
		9.0	10.6	12.0	V	V_{VB} = 7.0 V to 32 V, I_{VCPH} = -10mA, I_{VCPL} = -10 mA
[Regulator Output Characteristics]						
VDD Regulator Output Voltage	V_{VDD}	V_{VB}-0.5	-	V_{VB}	V	V_{VB} = 4.5 V to 5.5 V
		5.2	5.3	5.4	V	V_{VB} = 5.5 V to 32 V, I_{VDD} = -5 mA
VDD Load Regulation *(Note2)*	V_{LINVD}	-	-	500	mV	V_{VB} = 4.5 V to 6.0 V, I_{VDD} = -15 mA to -50 mA
		-	-	150	mV	V_{VB} = 6.0 V to 32 V, I_{VDD} = -15 mA to -50 mA

(Note 1) These values are subject to change.
(Note 2) These values are design values and are not tested at the time of shipment.

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11. Electrical Characteristics - Continued

11.3 Electrical Characteristics (Shunt Current Sense Amplifier)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND, CSAMPGx = 01h)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[Shunt Current Sense Amplifier]						
Input Offset Voltage (Absolute Error)	$V_{OFAMPABS}$	-5.0	-	+5.0	mV	V_{VB} = 4.5 V to 5.5 V, VINP = VINN = 0 V, Tj = 25 °C
		-1.0	-	+1.0	mV	V_{VB} = 5.5 V to 32 V, VINP = VINN = 0 V, Tj = 25 °C
Input Offset Voltage (Relative Error)	$V_{OFAMPREL}$	-3.0	-	+3.0	mV	V_{VB} = 4.5 V to 5.5 V, VINP = VINN = 0 V, Tj = 25 °C
		-1.0	-	+1.0	mV	V_{VB} = 5.5 V to 32 V, VINP = VINN = 0 V, Tj = 25 °C
Input Offset Drift *(Note1)*	$V_{OFDRIFT}$	-	40	-	µV/°C	V_{VB} = 4.5 V to 5.5 V
		-	6	-	µV/°C	V_{VB} = 5.5 V to 32 V
Input Common Mode Voltage Range	V_{INAMP}	-0.5	-	+1.5	V	V_{VB} = 4.5 V to 5.5 V
		-0.5	-	+2.0	V	V_{VB} = 5.5 V to 32 V
Gain Configuration	G_{AMPG1}	-	12	-	V/V	CSAMPGx = 0h, G_{AMPG1} = V_{AOUTx}/ (V_{AINxP}-V_{AINxN}+$V_{OFAMPABS}$)
	G_{AMPG2}	-	16	-	V/V	CSAMPGx = 1h, G_{AMPG2} = V_{AOUTx}/ (V_{AINxP}-V_{AINxN}+$V_{OFAMPABS}$)
	G_{AMPG3}	-	24	-	V/V	CSAMPGx = 2h, G_{AMPG3} = V_{AOUTx}/ (V_{AINxP}-V_{AINxN}+$V_{OFAMPABS}$)
	G_{AMPG4}	-	32	-	V/V	CSAMPGx = 3h, G_{AMPG4} = V_{AOUTx}/ (V_{AINxP}-V_{AINxN}+$V_{OFAMPABS}$)
Gain Configuration Error	G_{ERR1}	-1.2	0	+1.2	%	
Common Mode Rejection Ratio *(Note 1)*	$CMRR_{DC}$	60	-	-	dB	V_{VB} = 4.5 V to 6.0 V, Common mode ripple < 100 Hz
		70	-	-	dB	V_{VB} = 6.0 V to 32 V, Common mode ripple < 100 Hz
	$CMRR_{20K}$	50	-	-	dB	V_{VB} = 4.5 V to 6.0 V, Common mode ripple = 20 kHz
		65	-	-	dB	V_{VB} = 6.0 V to 32 V, Common mode ripple = 20 kHz
Power Supply Rejection Ratio *(Note 1)*	$PSRR_{DC}$	60	-	-	dB	V_{VB} = 4.5 V to 6.0 V, Power supply ripple < 100 Hz
		80	-	-	dB	V_{VB} = 6.0 V to 32 V, Power supply ripple < 100 Hz
	$PSRR_{20K}$	50	-	-	dB	V_{VB} = 4.5 V to 6.0 V, Power supply ripple = 20 kHz
		70	-	-	dB	V_{VB} = 6.0 V to 32 V, Power supply ripple = 20 kHz
Rise Time Delay *(Note1)*	$t_{AMPRISE}$	-	-	3.0	µs	V_{AINxP} = -156 mV→+156 mV, V_{AINxN} = 0 V, V_{VB} = 4.5 V to 5.5 V, CSAMPGx = 1h, Cout = 25 pF
		-	-	0.8	µs	V_{AINxP} = -156 mV→+156 mV, V_{AINxN} = 0 V, V_{VB} = 5.5 V to 32 V, CSAMPGx = 1h, Cout = 25 pF
Fall Time Delay *(Note1)*	$t_{AMPFALL}$	-	-	3.0	µs	V_{AINxP} = +156 mV→-156 mV, V_{AINxN} = 0 V, V_{VB} = 4.5 V to 5.5 V, CSAMPGx = 1h, Cout = 25 pF
		-	-	0.8	µs	V_{AINxP} = +156 mV→-156 mV, V_{AINxN} = 0 V, V_{VB} = 5.5 V to 32 V, CSAMPGx = 1h, Cout = 25 pF

(Note 1) These values are design values and are not tested at the time of shipment.

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11. Electrical Characteristics - Continued

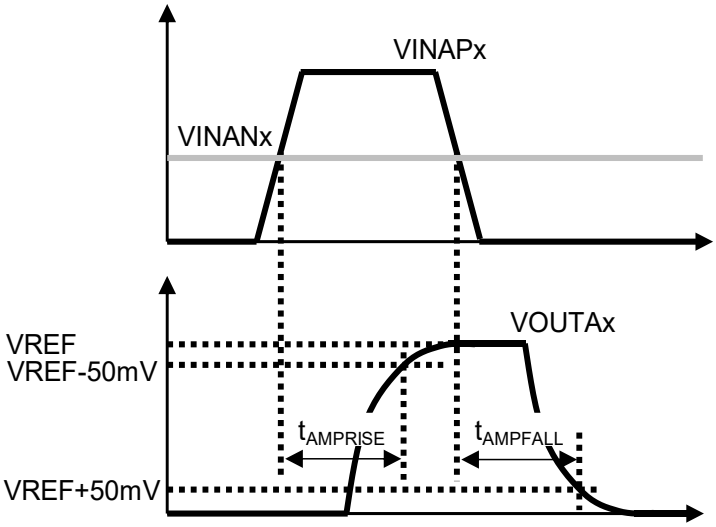


Figure 63. $t_{AMPRISE}/t_{AMPFALL}$

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11. Electrical Characteristics - Continued

11.4 Electrical Characteristics (Gate Driver Output)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[Gate Driver Output]						
High-side Gate Output V_{GS} Voltage	V_{HSGS1}	6.0	-	-	V	V_{VB} = 4.5 V to 6.0 V, I_{DRVHS} ≤ -5 mA *(Note2)*
		9.0	10.6	12.0	V	V_{VB} = 6.0 V to 32 V, I_{DRVHS} ≤ -5 mA *(Note2)*
	V_{HSGSH}	6.0	-	-	V	V_{VB} = 4.5 V to 7.0 V, I_{DRVHS} = -10mA *(Note2)*
		9.0	10.6	12.0	V	V_{VB} = 7.0 V to 32 V, I_{DRVHS} = -10 mA *(Note2)*
	V_{HSGSL}	0	-	0.2	V	V_{VB} = 4.5V to 32V I_{DRVHS} = 10 mA *(Note2)*
Low-side Gate Output V_{GS} Voltage	V_{LSGS1}	6.0	-	-	V	V_{VB} = 4.5 V to 6.0 V, I_{DRVLS} ≤ -5 mA *(Note2)*
		9.0	10.6	12.0	V	V_{VB} = 6.0 V to 32 V, I_{DRVLS} ≤ -5 mA *(Note2)*
	V_{LSGSH}	6.0	-	-	V	V_{VB} = 4.5 V to 7.0 V, I_{DRVLS} = -10mA *(Note2)*
		9.0	10.6	12.0	V	V_{VB} = 7.0 V to 32 V, I_{DRVLS} = -10 mA *(Note2)*
	V_{LSGSL}	0	-	0.2	V	V_{VB} = 4.5 V to 32 V I_{DRVLS} = 10 mA *(Note2)*
Gate Driver Current Accuracy *(Note1)*	I_{AC_DRVHS} I_{AC_DRVLS}	-65	-	+65	%	V_{VB} = 4.5V to 5.5 V HSDRV_SRC [3:0] = 0h to 2h, HSDRV_SNK [3:0] = 0h to 2h, LSDRV_SRC [3:0] = 0h to 2h, LSDRV_SNK [3:0] = 0h to 2h
		-50	-	+50	%	V_{VB} = 4.5 V to 5.5 V HSDRV_SRC [3:0] = 3h to 4h, HSDRV_SNK [3:0] = 3h to 4h, LSDRV_SRC [3:0] = 3h to 4h, LSDRV_SNK [3:0] = 3h to 4h
		-45	-	+45	%	V_{VB} = 4.5 V to 5.5 V HSDRV_SRC [3:0] = 5h to Fh, HSDRV_SNK [3:0] = 5h to Fh, LSDRV_SRC [3:0] = 5h to Fh, LSDRV_SNK [3:0] = 5h to Fh
		-60	-	+60	%	V_{VB} = 5.5 V to 32 V HSDRV_SRC [3:0] = 0h to 2h, HSDRV_SNK [3:0] = 0h to 2h, LSDRV_SRC [3:0] = 0h to 2h, LSDRV_SNK [3:0] = 0h to 2h
		-45	-	+45	%	V_{VB} = 5.5 V to 32 V HSDRV_SRC [3:0] = 3h to 4h, HSDRV_SNK [3:0] = 3h to 4h, LSDRV_SRC [3:0] = 3h to 4h, LSDRV_SNK [3:0] = 3h to 4h
		-30	-	+30	%	V_{VB} = 5.5 V to 32 V HSDRV_SRC [3:0] = 5h to Fh, HSDRV_SNK [3:0] = 5h to Fh, LSDRV_SRC [3:0] = 5h to Fh, LSDRV_SNK [3:0] = 5h to Fh

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11. Electrical Characteristics - Continued

Input/Output Propagation Delay	t_{PROPA}	-	-	2.0	µs	V_{VB} = 4.5 V to 5.5 V HSDRV_SRC [3:0] = Fh, HSDRV_SNK [3:0] = Fh, LSDRV_SRC [3:0] = Fh, LSDRV_SNK [3:0] = Fh, Rise Prop: INxH/INxL rising edge to VGS = 1 V, Fall Prop: INxH/INxL falling edge to VGS = VCPH/VCPL-1 V
		-	-	0.3	µs	V_{VB} = 5.5 V to 32 V HSDRV_SRC [3:0] = Fh, HSDRV_SNK [3:0] = Fh, LSDRV_SRC [3:0] = Fh, LSDRV_SNK [3:0] = Fh, Rise Prop: INxH/INxL rising edge to VGS = 1 V, Fall Prop: INxH/INxL falling edge to VGS = VCPH/VCPL-1V
Delta Input/Output Propagation Delay1 *(Note 1)*	$t_{propadelta1}$	-	-	50	ns	| Lside Fall Prop Delay -Hside Rise Prop Delay |
Delta Input/Output Propagation Delay2 *(Note 1)*	$t_{propadelta2}$	-	-	50	ns	| Hside Fall Prop Delay -Lside Rise Prop Delay |

(Note 1) These values are design values and are not tested at the time of shipment.
(Note 2) IDRVHS is the total gate output current of the High-side 1/2/3 phase, IDRVLS is the total gate output current of Low-side 1/2/3 phase.

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11. Electrical Characteristics - Continued

11.5 Electrical Characteristics (Gate Driver Output / Relay Driver Output)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[Gate Driver Output Pin]						
Dead Time Accuracy	t_{COMP}	-	-	350	ns	V_{VB} = 4.5 V to 5.5 V
		-	-	300	ns	V_{VB} = 5.5 V to 32 V
	t_{DEAD}	Setting Time - 1/f_{OSC}	Setting Time	Setting Time +1/f_{OSC}	ns	
High-side H Level VGS Detection Voltage	$V_{HTHDETH}$	V_{VCPH} -3.5	V_{VCPH} -2.0	V_{VCPH} -0.5	V	
Low-side H Level VGS Detection Voltage	$V_{LTHDETH}$	V_{VCPL} -3.5	V_{VCPL} -2.0	V_{VCPL} -0.5	V	
High-side L Level VGS Detection Voltage	$V_{HTHDETL}$	SxH +0.5	SxH +1.0	SxH +1.4	V	
Low-side L Level VGS Detection Voltage	$V_{LTHDETL}$	SxL +0.5	SxL +1.0	SxL +1.4	V	
GxH-SxH Pull Down Resistance Voltage	V_{ORESH}	0.3	2.2	4.5	V	I_{OH} = 5 µA
GxL-SxL Pull Down Resistance Voltage	V_{ORESL}	0.3	2.2	4.5	V	I_{OL} = 5 µA
SxH Outflow Current	I_{SH}	0.30	0.40	0.75	mA	
[Relay Driver Output Pin]						
Gate Output Voltage	V_{RGH}	V_{VB}+6.0	-	-	V	V_{VB} = 4.5 V to 6.0 V, I_{RDRV} = -5 mA
		V_{VB} +9.0	V_{VB} +10.6	V_{VB} +12.0	V	V_{VB} = 6.0 V to 32 V, I_{RDRV} = -5 mA
	V_{RGL}	0	-	0.3	V	V_{VB} = 4.5 V to 32 V, I_{RDRV} = 5 mA
Input/Output Propagation Delay	t_{PROPAR}	-	-	2.0	µs	V_{VB} = 4.5 V to 5.5 V
		-	-	1.0	µs	V_{VB} = 5.5 V to 32 V
H Level Relay Output Detection Voltage	V_{THDETH}	V_{VCPH} -3.5	V_{VCPH} -2.0	V_{VCPH} -0.5	V	
L Level Relay Output Detection Voltage	V_{THDETL}	0.5	1.0	1.4	V	

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11. Electrical Characteristics - Continued

11.6 Electrical Characteristics (Abnormal Detection 1)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[VB, VCC, REF, VDD Overvoltage Protection]						
VB Overvoltage Detection	V_{VBOVH}	36.0	38.0	40.0	V	
VB Overvoltage Release	V_{VBOVL}	33.5	35.5	37.5	V	
VCC Overvoltage Detection	V_{VCOVH}	3.45	3.55	3.65	V	V_{VCC} = 3.3 V
		5.25	5.40	5.55	V	V_{VCC} = 5.0 V
VCC Overvoltage Release	V_{VCOVL}	3.35	3.45	3.55	V	V_{VCC} = 3.3 V
		5.10	5.25	5.40	V	V_{VCC} = 5.0 V
REF Overvoltage Detection	V_{REFOVH}	3.45	3.55	3.65	V	V_{REF} = 3.3 V
		5.25	5.40	5.55	V	V_{REF} = 5.0 V
REF Overvoltage Release	V_{REFOVL}	3.35	3.45	3.55	V	V_{REF} = 3.3 V
		5.10	5.25	5.40	V	V_{REF} = 5.0 V
VDD Overvoltage Detection	V_{VDOVH}	5.80	6.00	6.20	V	
VDD Overvoltage Release	V_{VDOVL}	5.45	5.65	5.85	V	
[VB, VCC, REF, VDD, DRN Undervoltage Protection]						
VB Undervoltage Detection	V_{VBUVL}	3.80	4.00	4.20	V	
VB Undervoltage Release	V_{VBUVH}	4.00	4.20	4.40	V	
VCC Undervoltage Detection	V_{VCUVL}	2.95	3.05	3.15	V	V_{VCC} = 3.3 V
		4.45	4.60	4.75	V	V_{VCC} = 5.0 V
VCC Undervoltage Release	V_{VCUVH}	3.05	3.15	3.25	V	V_{VCC} = 3.3 V
		4.60	4.75	4.90	V	V_{VCC} = 5.0 V
REF Undervoltage Detection	V_{REFUVL}	2.95	3.05	3.15	V	V_{REF} = 3.3 V
		4.45	4.60	4.75	V	V_{REF} = 5.0 V
REF Undervoltage Release	V_{REFUVH}	3.05	3.15	3.25	V	V_{REF} = 3.3 V
		4.60	4.75	4.90	V	V_{REF} = 5.0 V
VDD Undervoltage Detection	V_{VDUVL}	2.70	2.90	3.10	V	
DRN Undervoltage Detection	V_{DRNVL}	3.50	3.70	3.90	V	
DRN Undervoltage Release	V_{DRNVH}	3.60	3.80	4.00	V	
[Charge Pump Overvoltage]						
VCPH Overvoltage Detection	$V_{VCPHOVH}$	12.5	14.1	15.7	V	V_{VCPH} - V_{VB}
VCPL Overvoltage Detection	$V_{VCPLOVH}$	12.4	13.2	14.0	V	
VCPH Overvoltage Detection (GND Reference)	$V_{VCPHOVH_ABS}$	50	55	60	V	V_{VCPH} - GND
[Charge Pump Undervoltage]						
VCPH Undervoltage Detection	$V_{VCPHUVL}$	4.5	5.5	6.5	V	V_{VCPH} - V_{VB}
VCPL Undervoltage Detection	$V_{VCPLUVL}$	4.5	5.5	6.5	V	
VCPH-DRN Undervoltage Detection	V_{DRNUVL}	4.5	5.5	6.5	V	V_{VCPH} - V_{DRN}

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11. Electrical Characteristics - Continued

11.7 Electrical Characteristics (Abnormal Detection 2)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec Min	Spec Typ	Spec Max	Unit	Condition
[High / Low-side MOS-FET Drain-Source Voltage, SHUNT Voltage Abnormal Protection]						
Accuracy of Detection Voltage between DRN and SxH 1	V_{DSSH_SET1}	-800	-200	-20	mV	V_{VB} = 4.5 V to 32 V, VDSH [3:0] = 0h
Accuracy of Detection Voltage between DRN and SxH 2	V_{DSSH_SET2}	Setting Voltage -40	Setting Voltage	Setting Voltage +40	mV	V_{VB} = 4.5 V to 5.5 V, VDSH [3:0] = 1h
		Setting Voltage -30	Setting Voltage	Setting Voltage +30	mV	V_{VB} = 5.5 V to 32 V, VDSH [3:0] = 1h
Accuracy of Detection Voltage between DRN and SxH 3	V_{DSSH_SET3}	-50	0	+50	%	V_{VB} = 4.5 V to 5.5 V, VDSH [3:0] = 2h to 5h
		-25	0	+25	%	V_{VB} = 5.5 V to 32 V, VDSH [3:0] = 2h to 5h
Accuracy of Detection Voltage between DRN and SxH 4	V_{DSSH_SET4}	-50	0	+50	%	V_{VB} = 4.5 V to 5.5 V, VDSH [3:0] = 6h to Dh
		-10	0	+10	%	V_{VB} = 5.5 V to 32 V, VDSH [3:0] = 6h to Fh
Accuracy of Detection Voltage between SxH and SxL 1	V_{DSSL_SET1}	-800	-200	-20	mV	V_{VB} = 4.5 V to 32 V, VDSL [3:0] = 0h
Accuracy of Detection Voltage between SxH and SxL 2	V_{DSSL_SET2}	Setting Voltage -40	Setting Voltage	Setting Voltage +40	mV	V_{VB} = 4.5V to 5.5V, VDSL [3:0] = 1h
		Setting Voltage -30	Setting Voltage	Setting Voltage +30	mV	V_{VB} = 5.5 V to 32 V, VDSL [3:0] = 1h
Accuracy of Detection Voltage between SxH and SxL 3	V_{DSSL_SET3}	-50	0	+50	%	V_{VB} = 4.5V to 5.5V, VDSL [3:0] = 2h to 5h
		-25	0	+25	%	V_{VB} = 5.5 V to 32 V, VDSL [3:0] = 2h to 5h
Accuracy of Detection Voltage between SxH and SxL 4	V_{DSSL_SET4}	-50	0	+50	%	V_{VB} = 4.5V to 5.5 V, VDSL [3:0] =0h to Dh
		-10	0	+10	%	V_{VB} = 5.5 V to 32 V, VDSL [3:0] =6h to Fh
SHUNT Resistor-to-Resistor Detection Voltage Accuracy 1	V_{SHUNT_SET1}	-800	-200	-20	mV	V_{VB} = 4.5 V to 32 V, VSNT [3:0] =0h
SHUNT Resistor-to-Resistor Detection Voltage Accuracy 2	V_{SHUNT_SET2}	Setting Voltage -30	Setting Voltage	Setting Voltage +30	mV	V_{VB} = 4.5 V to 5.5 V, VSNT [3:0] = 1h
		Setting Voltage -20	Setting Voltage	Setting Voltage +20	mV	V_{VB} = 5.5 V to 32 V, VSNT [3:0] = 1h
SHUNT Resistor-to-Resistor Detection Voltage Accuracy 3	V_{SHUNT_SET3}	-50	0	+50	%	V_{VB} = 4.5 V to 5.5 V, VSNT [3:0] = 2h to Ah
		-25	0	+25	%	V_{VB} = 5.5 V to 32 V, VSNT [3:0] = 2h to Ah
SHUNT Resistor-to-Resistor Detection Voltage Accuracy 4	V_{SHUNT_SET4}	-50	0	+50	%	V_{VB} = 4.5 V to 5.5 V, VSNT [3:0] = Bh to Fh
		-10	0	+10	%	V_{VB} = 5.5 V to 32 V, VSNT [3:0] = Bh to Fh

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11. Electrical Characteristics - Continued

11.8 Electrical Characteristics (Abnormal Detection 3)

(Unless otherwise specified V_{VB} = 4.5 V to 32 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
[High / Low-side MOS-FET Drain-Source Voltage, SHUNT Voltage Abnormal Protection]						
Detect Delay Time	$t_{VDSSHMTON}$, $t_{VDSSLMTON}$, $t_{SHTMTON}$	-	1.5	10.0	µs	TVDS_MSK [3:0] = 0h TVDS_FLT [3:0] = 0h
Release Delay Time	$t_{VDSSHMTOFF}$, $t_{VDSSLMTOFF}$, $t_{SHTMTOFF}$	-	1.5	10.0	µs	TVDS_MSK [3:0] = 0h TVDS_FLT [3:0] = 0h
Mask/Filter Time Variation	t_{VDS_MSK} t_{VDS_FLT}	Setting Time - 1/f_{OSC}	Setting Time	Setting Time +1/f_{OSC}	ns	TVDS_MSK [3:0] = 0h to Fh TVDS_FLT [3:0] = 0h to Fh

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11. Electrical Characteristics - Continued

11.9 Electrical Characteristics (SPI AC)

(Unless otherwise specified V_{VB} = 4.5V to 32 V, VCC = 3.0 V to 5.5 V, Tj = -40 °C to +150 °C, 0.47 µF between CP1L -CP1H, 0.47 µF between CP2L -CP2H. 1 µF between VCPH -VB, 4.7 µF between VCPL -GND, V_{S1H} /V_{S2H} /V_{S3H} = VB, V_{S1L} /V_{S2L} /V_{S3L} = GND)

Parameter	Symbol	Spec			Unit	Condition
		Min	Typ	Max		
SCK Frequency	f_{SCK}	-	-	5	MHz	
SCK Cycle Period	t_{CYC}	200	-	-	ns	
SCK High Pulse Width	t_{CKWH}	90	-	-	ns	
SCK Low Pulse Width	t_{CKWL}	90	-	-	ns	
SCK Setup Time	t_{CKS}	50	-	-	ns	
SCK Hold Time	t_{CKH}	150	-	-	ns	
CSB Setup Time	t_{CSS}	50	-	-	ns	
CSB Hold Time	t_{CSH}	50	-	-	ns	
CSB High Pulse Width	t_{CSWH}	400	-	-	ns	
SDI Setup Time	t_{DS}	20	-	-	ns	
SDI Hold Time	t_{DH}	30	-	-	ns	
SDO Output Delay *(Note 1) (Note 2)*	t_{OD}	-	-	90	ns	C_L = 20 pF
SDO Output On *(Note 1) (Note 2)*	t_{OON}	-	-	90	ns	C_L = 20 pF
SDO Output Off *(Note 1) (Note 2)*	t_{OOF}	-	-	90	ns	C_L = 20 pF
SDO Output Off (Hi-Z) *(Note 1) (Note 3)*	t_{OOFZ}	-	-	90	ns	

(Note 1) These values are design values and are not tested at the time of shipment.
(Note 2) The reference level is defined as 20 % and 80 % of VCC.
(Note 3) The reference level is defined as 0% and 100% of VCC.

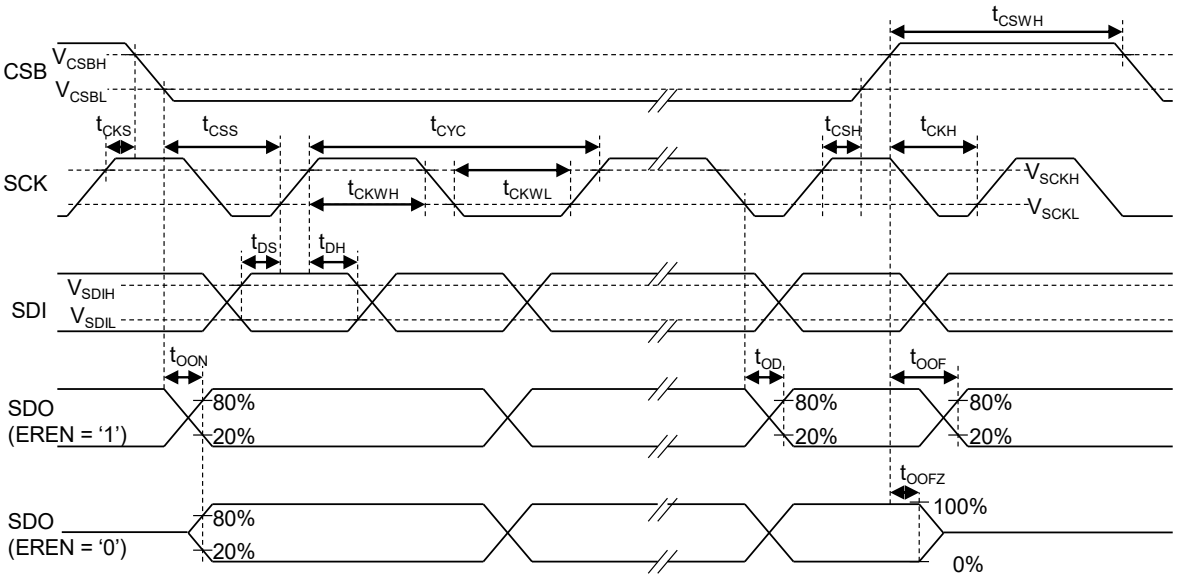


Figure 64. SPI Timing

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12. Typical Performance Curves

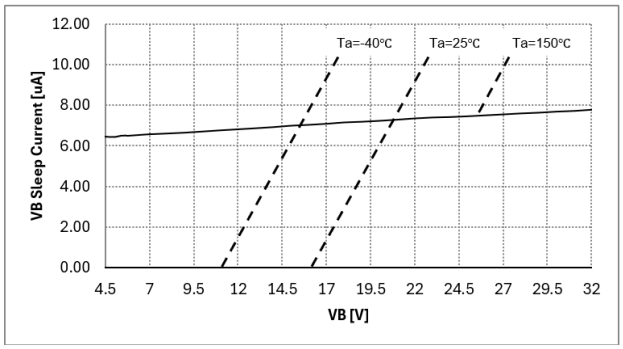


Figure 65. VB Sleep Current vs VB

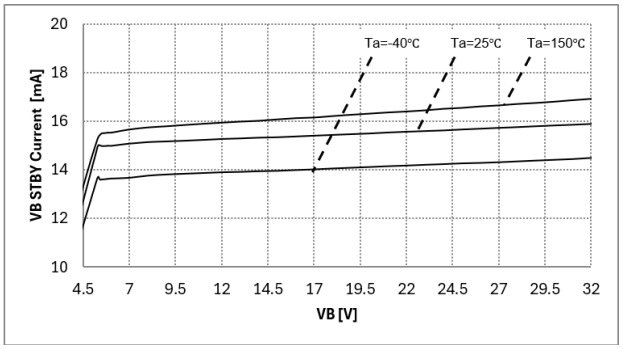


Figure 66. VB STBY Current vs VB

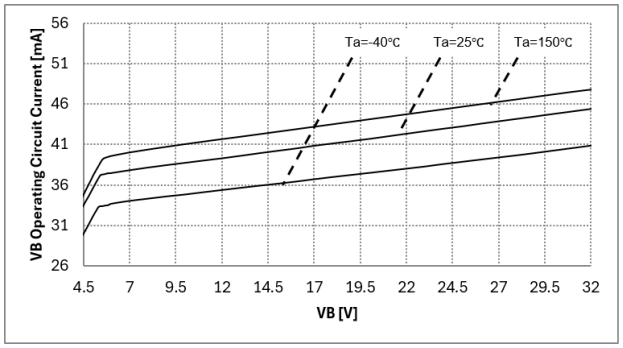


Figure 67. VB Operating Circuit Current vs VB

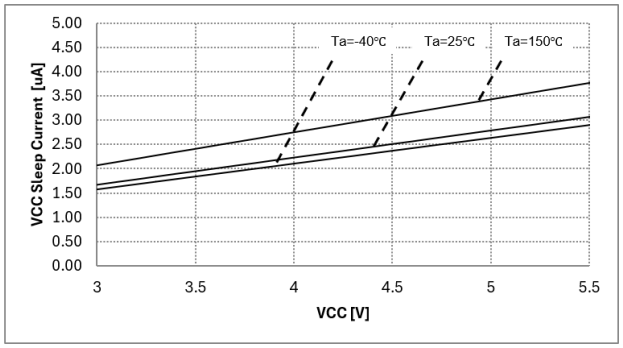


Figure 68. VCC Sleep Current vs VCC

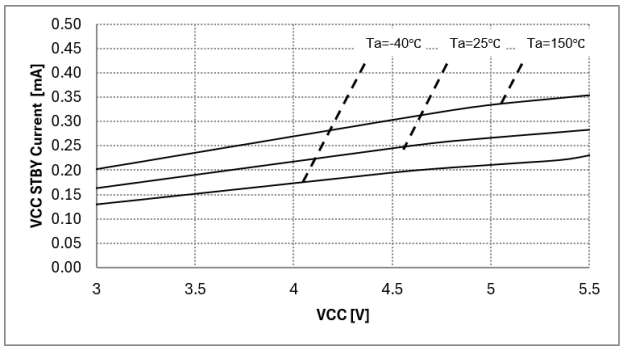


Figure 69. VCC STBY Current vs VCC

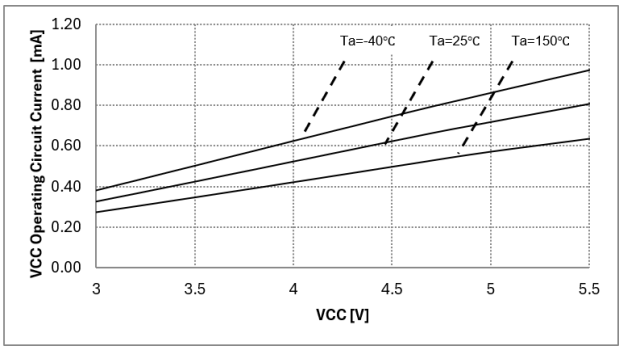
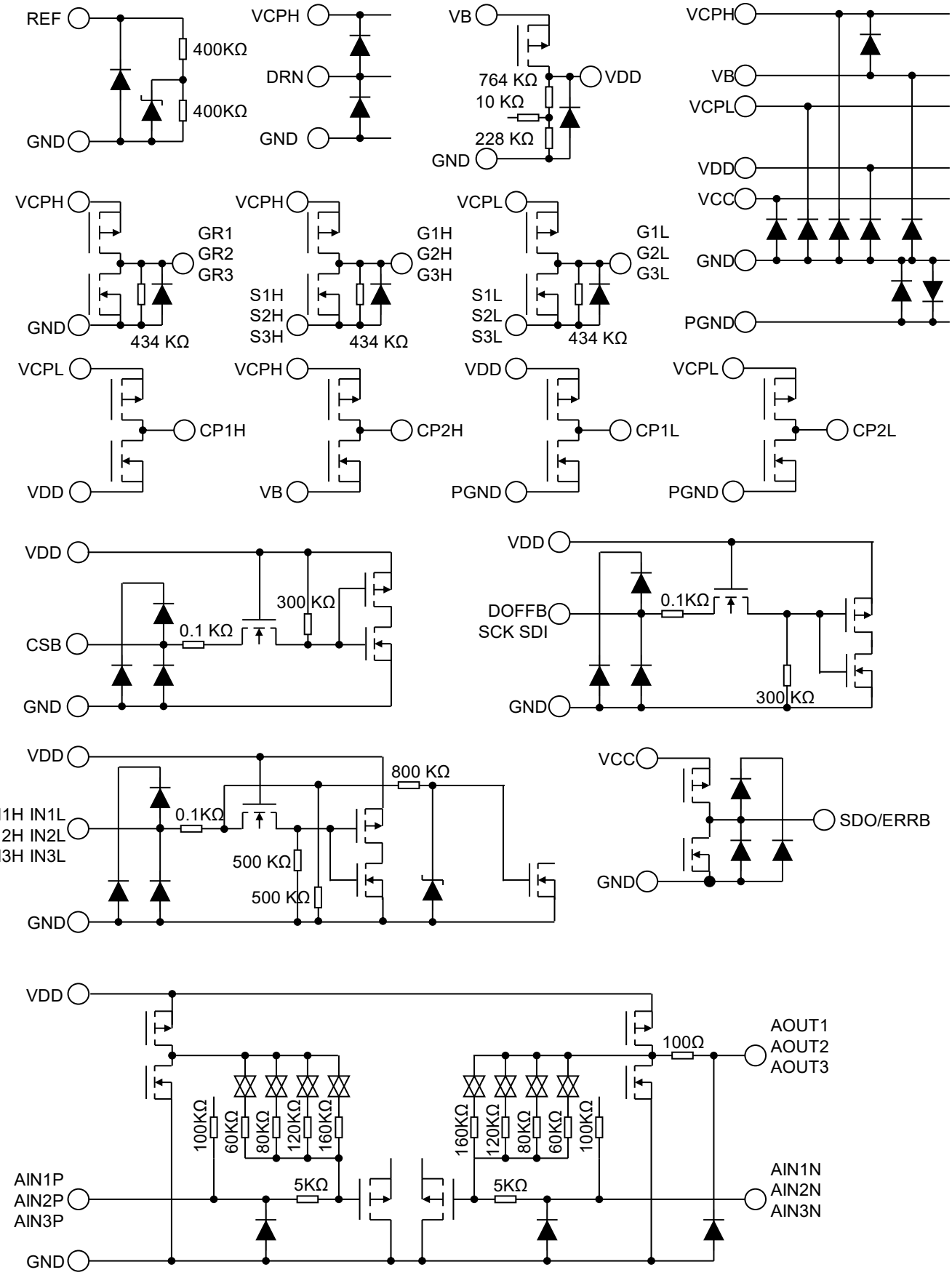


Figure 70. VCC Operating Circuit Current vs VCC

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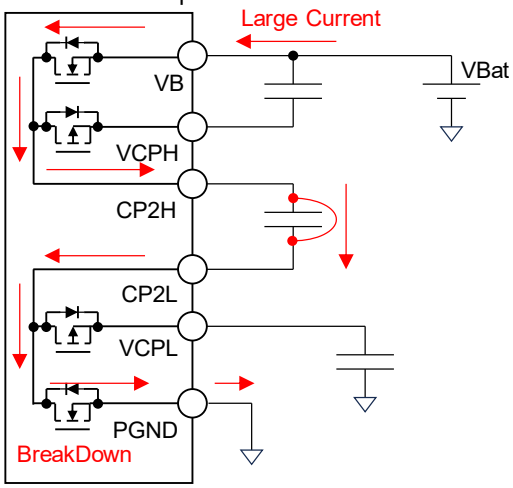
13. I/O Equivalence Circuit



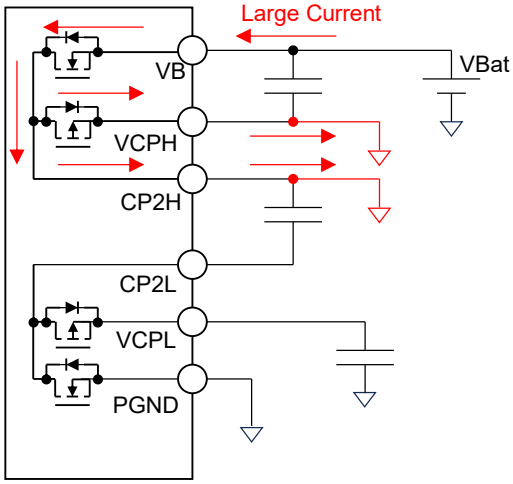
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14. Note in Application Circuit

(1) CP2H - CP2L short circuit
Large current will occur if CP2H-CP2L are short-circuited.
Duplication of the capacitor is recommended to avoid this case.



(2) VCPH – ground / CP2H – ground short circuit
Large current will occur if VCPH – ground or CP2H – ground is short-circuited.
Insert fuse or switch on VB line if this case should be avoided.



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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – Continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

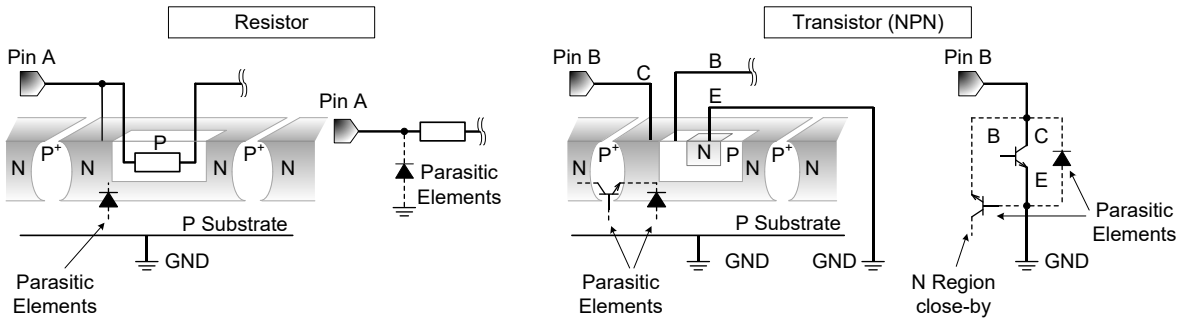


Figure 71. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

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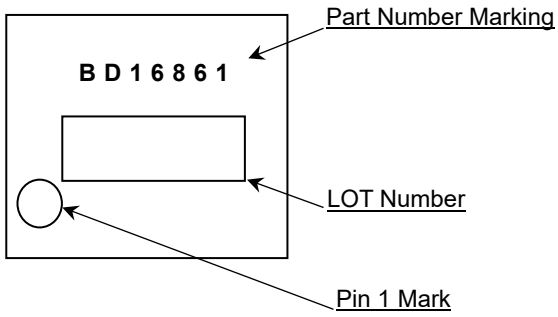
Ordering Information

B D 1 6 8 6 1 M U F	-	CE2

- Part Number
- Package
  MUF: VQFN48FBV070
- Packaging and forming specification
  C: for Automotive
  E2: Embossed tape and reel

Marking Diagram

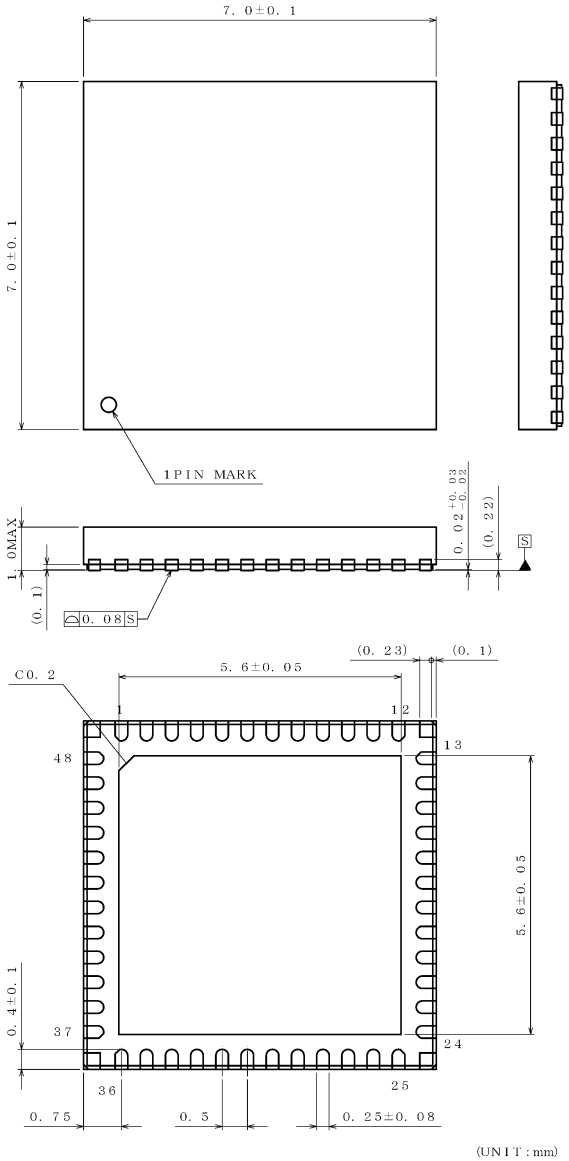
VQFN48FBV070 (TOP VIEW)



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Physical Dimension and Packing Information

Package Name	VQFN48FBV070



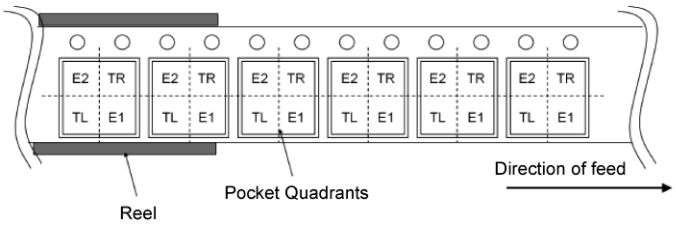
(UNIT : mm)

NOTE : Dimensions in ( ) for reference only.

PKG : VQFN48FBV070
Drawing No. EX414-5001-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
14.Sep.2026	001	New Release

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Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application examples, their constants, software, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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