Datasheet

Accelerometer Series

Kionix$^{\text{TM}}$ Technology
Accelerometer IC

KX134ACR-LBZ

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

KX134ACR-LBZ is a MEMS capacitive 3-axis accelerometer using Kionix$^{\text{TM}}$ Technology.*(Note 1)* Acceleration ranges of ±8 g, ±16 g, ±32 g and ±64 g are supported. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element which further utilize common mode cancellation to decrease errors from process variation, temperature, and environmental stress.

(Note 1) Kionix™ Technology is defined by the proprietary plasma micromachining process and the technology to hermetically seal at a wafer level by bonding the silicon lid wafer to the device wafer.

Features

- Kionix$^{\text{TM}}$ Technology*(Note 1)*
- Selectable Acceleration Range and Output Data Rate
- Selectable Low Power or High Resolution Mode
- Digital High-pass Filter Outputs
- Embedded FIFO Buffer
- Configurable Low Power Mode for Noise and Power
- User-configurable Wake-up / Back-to-sleep Function
- Digital I^{2}C up to 400 kHz
- Digital SPI up to 10 MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

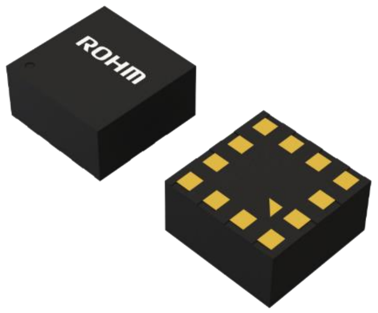
Applications

- Factory Automation Equipment
- Industrial Motor, Pump
- Robotic Machine, Arm
- Motion Data Logger

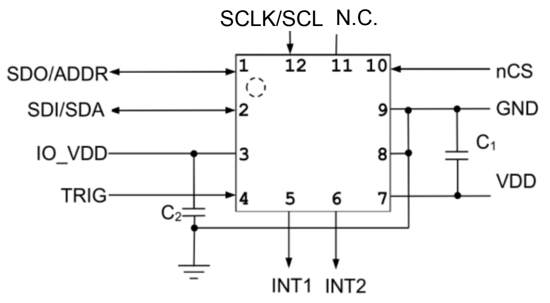
Key Specifications

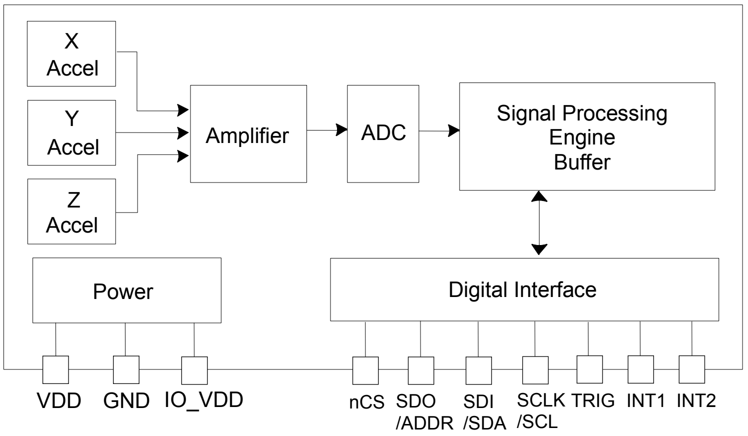
■ Acceleration Range:	±8 g, ±16 g, ±32 g or ±64 g
■ Wake-up and Back-to-sleep Engine Threshold Resolution:	15.6 mg/counts
■ Output Data Rate:	0.781 Hz to 25600 Hz
■ Embedded Buffer:	43 or 86 Stored Samples
■ Operating Temperature Range:	-40 °C to +105 °C

Package	**W (Typ) x D (Typ) x H (Max)**
VLGA012AV02A	2.0 mm x 2.0 mm x 1.0 mm



Typical Application Circuit and Block Diagram



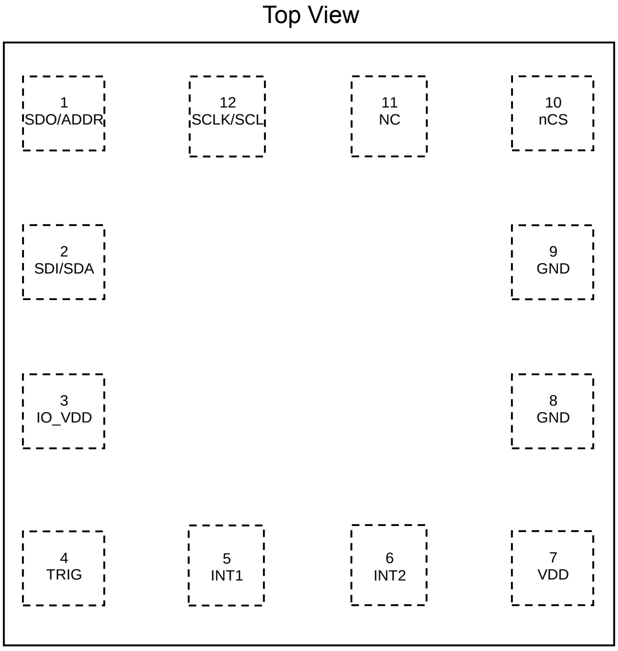


Kionix$^{\text{TM}}$ is a trademark or a registered trademark of ROHM Co., Ltd.

○Product structure: Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	SDO/ADDR	Serial Data Out pin during 4-wire SPI communication and the LSB(Least Significant Bit) setting pin of the Target address during I^2C communication. Do not leave floating when using I^2C communication. Pull-up or pull-down when using 4-wire or 3-wire SPI communication.
2	SDI/SDA	SPI Data input / I^2C Serial Data pin*(Note 1)*. Do not leave floating.
3	IO_VDD	Power voltage pin*(Note 2)*.
4	TRIG	Trigger pin for FIFO buffer control. Connect to GND when not using external trigger option.
5	INT1	Physical Interrupt. The pin is in High-impedance state during Power-on sequence and is driven following Power-on sequence. Leave floating if not used.
6	INT2	Physical Interrupt. The pin is in High-impedance state during Power-on sequence and is driven following Power-on sequence. Leave floating if not used.
7	VDD	Power voltage pin*(Note 2)*.
8	GND	Ground
9	GND	Ground
10	nCS	Chip Select (active LOW) for SPI communication. Connect to IO_VDD for I^2C communication. Do not leave floating.
11	N.C.	Not internally connected. Can be connected to VDD, IO_VDD, GND.
12	SCLK/SCL	SPI and I^2C Serial Clock pin*(Note 1)*. Do not leave floating.

(Note 1) When there is other device which is connected to SDA, SCL or INT pins and its signal falls sharply, that might generate undershoot and the pin voltage might go below ground. When such undershoot occurs, a measure like disposing a capacitor near the pins of the device must be taken.

(Note 2) Place a bypass capacitor (0.1 μF) as close as possible to the IC.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (VDD, IO_VDD)	V_{MAX}	4.5	V
Input/Output Voltage(Note 1)	V_{INOUT}	-0.3 to +4.5	V
Storage Temperature Range	Tstg	-40 to +125	°C
Maximum Junction Temperature	Tjmax	150	°C
Mech. Shock (Powered and Unpowered)	S_{OVR}	5000 g for 0.5 ms 10000 g for 0.2 ms	g

(Note 1) Except VDD pin, IO_VDD pin

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
VLGA012AV02A				
Junction to Ambient	θ_{JA}	195.7	131.0	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	8	6	°C/W

(Note 2) Based on JESD51-2A(Still-Air)

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{VDD}	1.7	2.5	3.6	V
I/O Pads Supply Voltage (IO_VDD)	V_{IO_VDD}	1.7	2.5	V_{VDD}	V
Input Voltage	V_{IN}	0.0	-	3.6	V
I^2C Communication Rate	f_{SCL_I2C}	-	-	0.4	MHz
SPI Communication Rate	f_{SCL_SPI}	-	-	10	MHz
I^2C Target Address(Note 6)	-	1Eh or 1Fh			-
WHO_AM_I register value	-	CCh			-
Output Data Rate(Note 7)	-	0.781	50	25600	Hz
Output Signal Bandwidth(Note 8)	-	ODR/9 or ODR/2			-
Operating Temperature	Topr	-40	+25	+105	°C

(Note 6) Determined by ADDR pin assignment: GND for 1Eh, IO_VDD for 1Fh.

(Note 7) Typical values. ODR is user-selectable via I^2C or SPI. See ODCNTL register for details.

(Note 8) Refers to accelerometer's raw output data.

Electrical Characteristics

(Unless otherwise specified V_{VDD} = 2.5 V, V_{IO_VDD} = 2.5 V, Ta = 25 °C, Acceleration Range = ±8 g)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current Consumption						
Operating(High Resolution Mode)	I_{dd_HR}	-	220	-	µA	ODR = 400 Hz
Operating(Low Power Mode)	I_{dd_LP}	-	10	-	µA	ODR = 50 Hz*(Note 1)*
Standby Mode	I_{ss}	-	0.9	-	µA	
Logic						
L Input Voltage	V_{IL}	-	-	0.2x V_{IO_VDD}	V	
H Input Voltage	V_{IH}	0.8x V_{IO_VDD}	-	-	V	
L Output Voltage1*(Note 2)*	V_{OL1}	-	-	0.2x V_{IO_VDD}	V	IO_VDD < 2 V
L Output Voltage2*(Note 2)*	V_{OL2}	-	-	0.4	V	IO_VDD ≥ 2 V
H Output Voltage	V_{OH}	0.8x V_{IO_VDD}	-	-	V	
Boot characteristics						
Start Up Time*(Note 3)*	T_{SU}	-	0.9+ 1000 / ODR	-	ms	
Power Up Time*(Note 4)*	T_{PU}	-	20	50	ms	
Accelerometer characteristics						
Zero-g Offset	-	-	±75	±175	mg	
Zero-g Offset Variation from RT over Temperature	-	-	±0.5	-	mg/°C	
Sensitivity1*(Note 5)*	-	3768	4096	4424	counts/g	GSEL[1:0] = 0 (±8 g)
Sensitivity2*(Note 5)*	-	1884	2048	2212	counts/g	GSEL[1:0] = 1 (±16 g)
Sensitivity3*(Note 5)*	-	942	1024	1106	counts/g	GSEL[1:0] = 2 (±32 g)
Sensitivity4*(Note 5)*	-	471	512	553	counts/g	GSEL[1:0] = 3 (±64 g)
Sensitivity Variation from RT over Temperature	-	-	±0.01	-	%/°C	X,Y-axis
	-	-	±0.03	-	%/°C	Z-axis
Positive Self-test Output Change on Activation	-	-	0.5	-	g	
Mechanical Signal Bandwidth (-3dB) *(Note 6)*	-	-	8.2	-	kHz	X-axis
	-	-	8.5	-	kHz	Y-axis
	-	-	5.6	-	kHz	Z-axis
Non-Linearity	-	-	±0.6	-	% of FS	
Cross Axis Sensitivity	-	-	2	-	%	
RMS Noise*(Note 7)*	-	-	1.6	-	mg	High Resolution Mode

(Note 1) Current varies with Output Data Rate (ODR) as shown, types and number of enabled digital engines, the average filter control settings, and VDD. Measured with OWUF[2:0] = 0, OSA[3:0] = 6, AVC[2:0] = 2.

(Note 2) For I^2C communication, this assumes a minimum 1.5 kΩ pull-up resistor between SCL/SDA pins and IO_VDD pin.

(Note 3) Start up time is from PC1 set to valid outputs. Time varies with ODR and Power Mode bit setting.

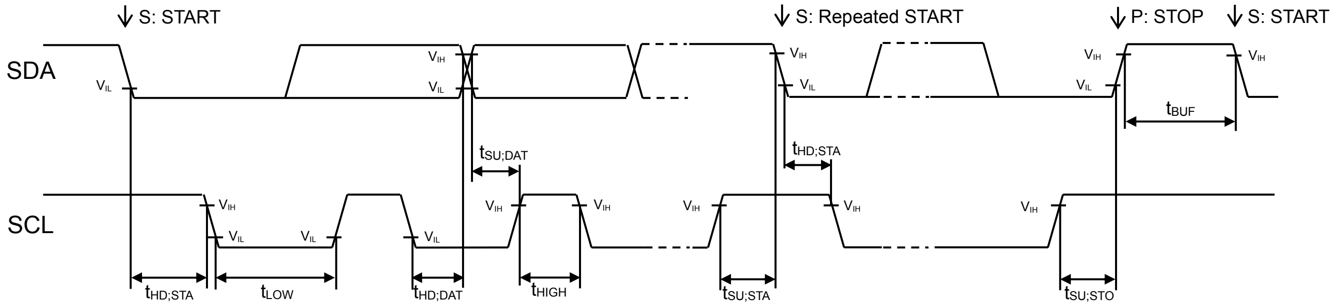
(Note 4) Power up time is from VDD valid to device boot completion.

(Note 5) Resolution and acceleration ranges are user selectable via I^2C or SPI. Tolerance specified at ±1 g stimulus.

(Note 6) Signal bandwidth varies with Output Data Rate (ODR), and Low-pass filter setting. Measured with ODR = 25600 Hz, LPRO = 1 settings.

(Note 7) Noise varies with ODR, power mode, and Low-pass filter settings. Measured with RES = 1, ODR = 50 Hz, LPRO = 1 settings.

I²C Bus Timing Characteristics

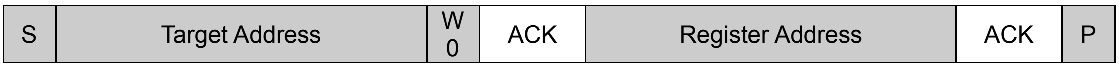


(Unless otherwise specified V_{VDD} = 2.5 V, V_{IO_VDD} = 2.5 V, Ta = 25 °C)

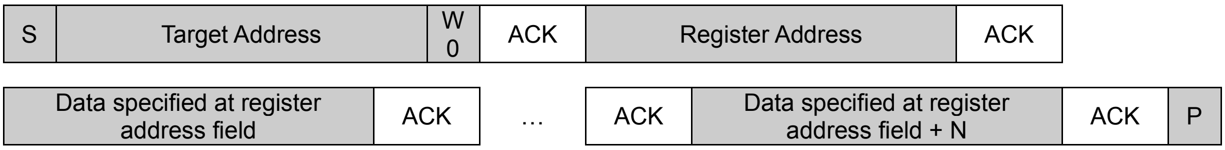
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCL Clock frequency	f_{SCL}	0	-	400	kHz	
‘L’ Period of SCL Clock	t_{LOW}	1.3	-	-	μs	
‘H’ Period of SCL Clock	t_{HIGH}	0.6	-	-	μs	
Setup Time for Repeated START	$t_{SU;STA}$	0.6	-	-	μs	
Hold Time for START	$t_{HD;STA}$	0.6	-	-	μs	
Data Setup Time	$t_{SU;DAT}$	100	-	-	ns	
Data Hold Time	$t_{HD;DAT}$	0	-	-	μs	
Setup Time for STOP	$t_{SU;STO}$	0.6	-	-	μs	
Bus Free Time between STOP and START	t_{BUF}	1.3	-	-	μs	

I²C Bus Communication

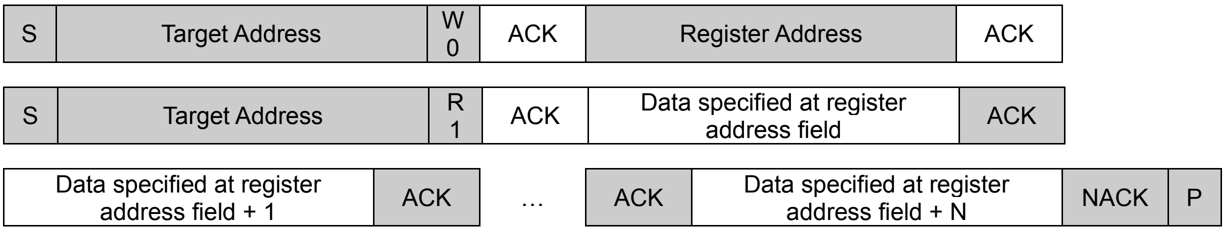
1. Write Format
   (1) Indicate register address



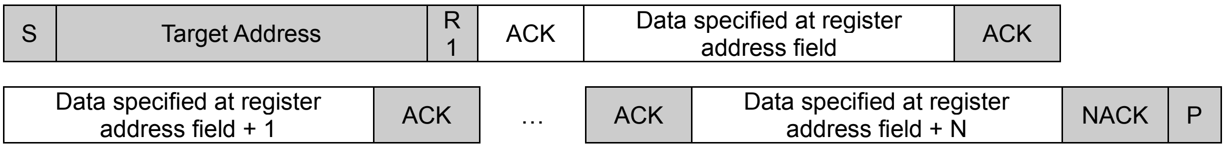
   (2) Write data after indicating register address



2. Read Format
   (1) Read data after indicating register address



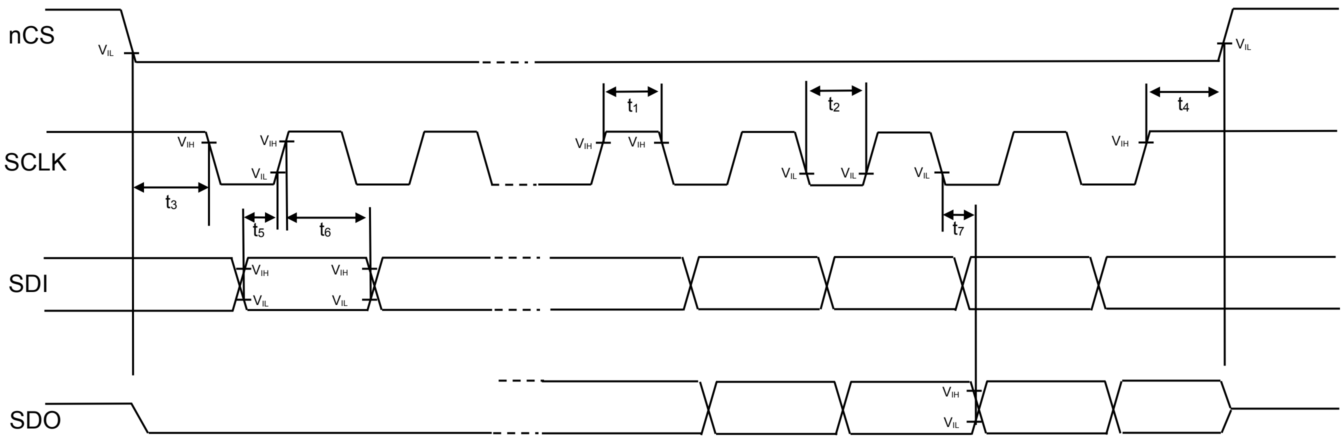
   (2) Read data from the specified register



▨ from Controller to Target   ☐ from Target to Controller

4-Wire SPI Bus Timing Characteristics

Timings are with 1 kΩ pull-up resistor and maximum 20 pF load capacitor on SDO. SCLK keeps HIGH when nCS is HIGH (no transmission). The MSB (Most Significant Bit) of the register address byte will indicate ‘0’ when writing to the register and ‘1’ when reading from the register. All commands are sent MSB first. The host must return nCS HIGH for at least one clock cycle(1/f_{SCLK}) before the next data request.

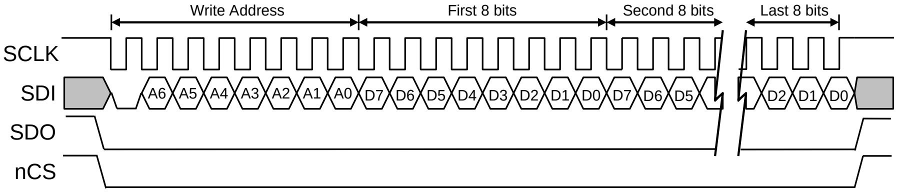


(Unless otherwise specified V_{VDD} = 2.5 V, V_{IO_VDD} = 2.5 V, Ta = 25 °C)

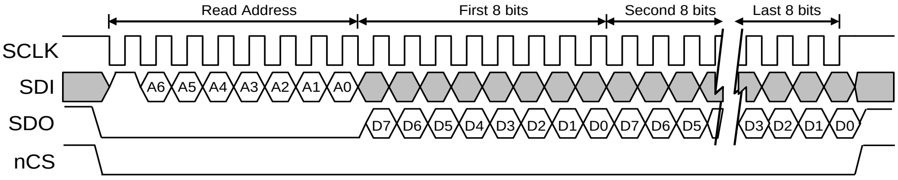
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCLK Clock frequency	f_{SCLK}	-	-	10	MHz	
‘H’ Period of SCLK Clock	t_1	45	-	-	ns	
‘L’ Period of SCLK Clock	t_2	45	-	-	ns	
nCS LOW to first SCLK falling edge	t_3	20	-	-	ns	
nCS LOW after the final SCLK rising edge to nCS rising edge	t_4	20	-	-	ns	
SDI input valid to SCLK rising edge	t_5	10	-	-	ns	
SCLK rising edge to SDI input invalid	t_6	10	-	-	ns	
SCLK falling edge to SDO output becomes valid *(Note 1)*	t_7	-	35	50	ns	

(Note 1) Only present during reads.

1. Write Format

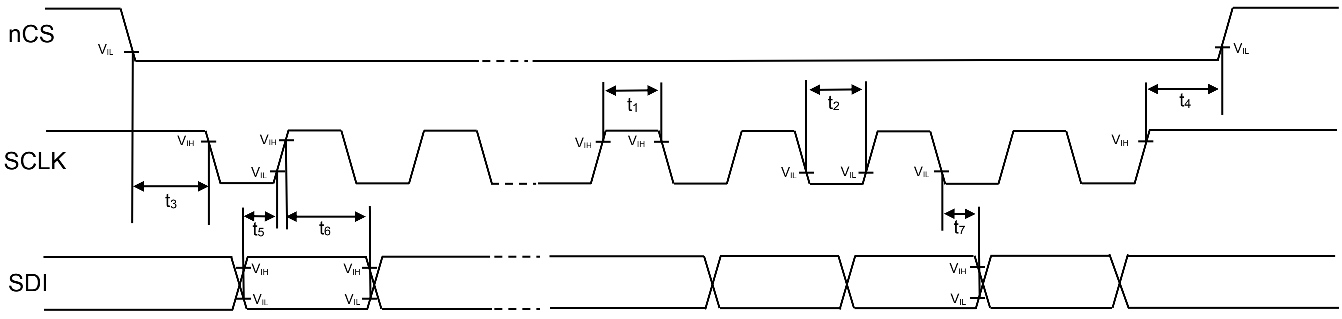


2. Read Format



3-Wire SPI Bus Timing Characteristics

Timings are with 1 kΩ pull-up resistor and maximum 20 pF load capacitor on SDI. SCLK keeps HIGH when nCS is HIGH (no transmission). The MSB (Most Significant Bit) of the register address byte will indicate ‘0’ when writing to the register and ‘1’ when reading from the register. All commands are sent MSB first. The host must return nCS HIGH for at least one clock cycle($1/f_{SCLK}$) before the next data request.
SDO/ADDR pin is configured in a high-impedance input-state, and must be externally tied to GND or IO_VDD.

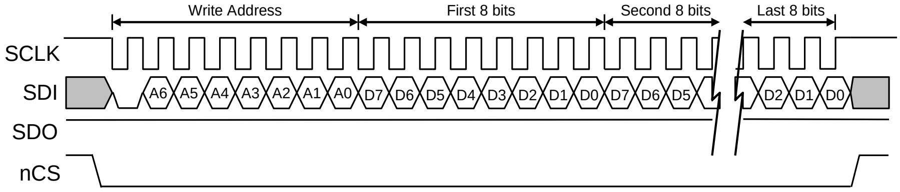


(Unless otherwise specified V_{VDD} = 2.5 V, V_{IO_VDD} = 2.5 V, Ta = 25 °C)

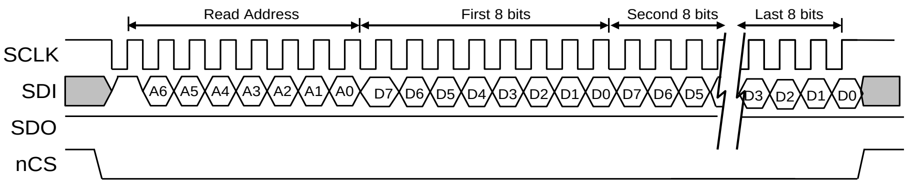
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCLK Clock frequency	f_{SCLK}	-	-	10	MHz	
‘H’ Period of SCLK Clock	t_1	45	-	-	ns	
‘L’ Period of SCLK Clock	t_2	45	-	-	ns	
nCS LOW to first SCLK falling edge	t_3	20	-	-	ns	
nCS LOW after the final SCLK falling edge to nCS rising edge	t_4	20	-	-	ns	
SDI input valid to SCLK rising edge	t_5	10	-	-	ns	
SCLK rising edge to SDI input invalid	t_6	10	-	-	ns	
SCLK falling edge to SDI output becomes valid*(Note 1)*	t_7	-	35	50	ns	

(Note 1) Only present during reads.

1. Write Format



2. Read Format



Register Map*(Note 1)*

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	XHPL	R	XHP [7:0]							
01h	XHPH	R	XHP [15:8]							
02h	YHPL	R	YHP [7:0]							
03h	YHPH	R	YHP [15:8]							
04h	ZHPL	R	ZHP [7:0]							
05h	ZHPH	R	ZHP [15:8]							
06h	XOUTL	R	XOUT [7:0]							
07h	XOUTH	R	XOUT [15:8]							
08h	YOUTL	R	YOUT [7:0]							
09h	YOUTH	R	YOUT [15:8]							
0Ah	ZOUTL	R	ZOUT [7:0]							
0Bh	ZOUTH	R	ZOUT [15:8]							
0Ch	COTR	R	COTR [7:0]							
0Fh	WHO_AM_I	R/W	WAI [7:0]							
13h	INS2	R	BTS	BFI	WMI	DRDY	0	0	WUFS	0
14h	INS3	R	0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU
15h	STATUS_REG	R	PC1_ STAT	RES_ STAT	CRC_F	INT	POR_ STAT	STAT_ REG	Reserved	WAKE
17h	INT_REL	R	INT_REL							
18h	CNTL1	R/W	PC1	RES	DRDYE	GSEL [1:0]		0	WUFE	0
19h	CNTL2	R/W	SRST	COTC	1	1	1	1	1	1
1Ah	CNTL3	R/W	1	0	1	0	1	OWUF [2:0]		
1Bh	ODCNTL	R/W	0	LPRO	Reserved		OSA [3:0]			
1Ch	INC1	R/W	PW1 [1:0]		IEN1	IEA1	IEL1	0	STPOL	SPI3E
1Dh	INC2	R/W	0	AOI	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE
1Fh	INC4	R/W	0	BFI1	WMI1	DRDYI1	BTSI1	0	WUFI1	0

(Note 1) Do not write any commands to other addresses except above. Do not write ‘1’ to the fields in which value is ‘0’ in above table. Do not write ‘0’ to the fields in which value is ‘1’ in above table.

Register Map(Note 1) – continued

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
20h	INC5	R/W	PW2[1:0]		IEN2	IEA2	IEL2	ACLR2	ACLR1	0
21h	INC6	R/W	0	BFI2	WMI2	DRDYI2	BTSI2	0	WUFI2	0
23h	WUFC	R/W	WUFC [7:0]							
2Ch	MAN_WAKE	W	0	0	0	0	0	0	MAN_WAKE	MAN_SLEEP
2Dh	BTS_CNTL	R/W	BTSE	0	0	0	0	OBTS [2:0]		
2Eh	BTSC	R/W	BTSC [7:0]							
2Fh	BTS_TH	R/W	BTSTH [7:0]							
30h	WUF_TH	R/W	WUFTH [7:0]							
31h	BTS_WUF_TH	R/W	0	BTSTH [10:8]			0	WUFTH [10:8]		
35h	LP_CNTL	R/W	1	AVC [2:0]			1	0	1	1
3Ah	BUF_CNTL1	R/W	Reserved	SMP [6:0]						
3Bh	BUF_CNTL2	R/W	BUFE	BRES	BFIE	Reserved			BM [1:0]	
3Ch	BUF_STATUS_1	R	SMP_LV [7:0]							
3Dh	BUF_STATUS_2	R	BUF_TRIG	0	0	0	0	0	0	0
3Eh	BUF_CLEAR	W	BUF_CLEAR [7:0]							
3Fh	BUF_READ	R	BUF_READ [7:0]							
46h	BTS_WUF_CNTL	R/W	0	TH_MODE	C_MODE_BTS	C_MODE_WUF	0	0	0	1
60h	SELFTEST	W	SELFTEST [7:0] (activation key = CAh)							

(Note 1) Do not write any commands to other addresses except above. Do not write ‘1’ to the fields in which value is ‘0’ in above table. Do not write ‘0’ to the fields in which value is ‘1’ in above table.

Register Map – continued

(00h-05h) XHPL, XHPH, YHPL, YHPH, ZHPL, ZHPH

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	XHPL	R	XHP [7:0]							
01h	XHPH	R	XHP [15:8]							
02h	YHPL	R	YHP [7:0]							
03h	YHPH	R	YHP [15:8]							
04h	ZHPL	R	ZHP [7:0]							
05h	ZHPH	R	ZHP [15:8]							

Fields	Function
XHP [15:0] YHP [15:0] ZHP [15:0]	High-pass filter accelerometer output. Data is updated at the ODR frequency determined by either OWUF in CNTL3 or OBTS in BTS_CNTL.

(06h-0Bh) XOUTL, XOUTH, YOUTL, YOUTH, ZOUTL, ZOUTH

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
06h	XOUTL	R	XOUT [7:0]							
07h	XOUTH	R	XOUT [15:8]							
08h	YOUTL	R	YOUT [7:0]							
09h	YOUTH	R	YOUT [15:8]							
0Ah	ZOUTL	R	ZOUT [7:0]							
0Bh	ZOUTH	R	ZOUT [15:8]							

Fields	Function
XOUT [15:0] YOUT [15:0] ZOUT [15:0]	When accelerometer is enabled (the PC1 bit is set to 1 in CNTL1 register), the 16-bits of valid acceleration data for each axis is routed to registers. The output data is available in 2's complement data format.

Register Map – continued

Data Format:

16-bit Register Data (2’s complement)	Equivalent Counts in decimal	Acceleration Range = ±8 g	Acceleration Range = ±16 g	Acceleration Range = ±32 g	Acceleration Range = ±64 g
0111 1111 1111 1111	+32767	+7.99976 g	+15.99951 g	+31.99902 g	+63.99805 g
0111 1111 1111 1110	+32766	+7.99951 g	+15.99902 g	+31.99805 g	+63.99609 g
…	…	…	…	…	…
0000 0000 0000 0001	+1	+0.00024 g	+0.00049 g	+0.00098 g	+0.00195 g
0000 0000 0000 0000	0	0.00000 g	0.00000 g	0.00000 g	0.00000 g
1111 1111 1111 1111	-1	-0.00024 g	-0.00049 g	-0.00098 g	-0.00195 g
…	…	…	…	…	…
1000 0000 0000 0001	-32767	-7.99976 g	-15.99951 g	-31.99902 g	-63.99805 g
1000 0000 0000 0000	-32768	-8.00000 g	-16.00000 g	-32.00000 g	-64.00000 g

8-bit Register Data (2’s complement)	Equivalent Counts in decimal	Acceleration Range = ±8 g	Acceleration Range = ±16 g	Acceleration Range = ±32 g	Acceleration Range = ±64 g
0111 1111	+127	+7.93750 g	+15.87500 g	+31.75000 g	+63.50000 g
0111 1110	+126	+7.87500 g	+15.75000 g	+31.50000 g	+63.00000 g
…	…	…	…	…	…
0000 0001	+1	+0.06250 g	+0.12500 g	+0.25000 g	+0.50000 g
0000 0000	0	0.00000 g	0.00000 g	0.00000 g	0.00000 g
1111 1111	-1	-0.06250 g	-0.12500 g	-0.25000 g	-0.50000 g
…	…	…	…	…	…
1000 0001	-127	-7.93750 g	-15.87500 g	-31.75000 g	-63.50000 g
1000 0000	-128	-8.00000 g	-16.00000 g	-32.00000 g	-64.00000 g

(0Ch) COTR

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	COTR	R	COTR [7:0]							

default value 55h

Fields	Function
COTR [7:0]	The COTR is used for command test response which verifies proper integrated circuit functionality. The value of this register will change from a default value of 55h to AAh when COTC bit in CNTL2 register is set. After reading AAh from this register, the value returns to the default value of 55h and COTC bit in CNTL2 register is self-cleared.

Register Map – continued

(0Fh) WHO_AM_I

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	WHO_AM_I	R/W	WAI [7:0]							

default value CCh

Fields	Function
WAI [7:0]	This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is CCh.

(13h) INS2

This register tells which function caused an interrupt.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
13h	INS2	R	BTS	BFI	WMI	DRDY	0	0	WUFS	0

Fields	Function
BTS	Reports the Back-to-sleep interrupt status. This bit is cleared when the interrupt latch release register INT_REL is read. BTS = 1 - Back-to-sleep event is detected. BTS = 0 - No Back-to-sleep event is detected.
BFI	Buffer Full interrupt bit indicates that buffer has been filled. This bit is automatically cleared when at least one sample from the buffer is read. BFI = 0 - Buffer is not full. BFI = 1 - Buffer is full.
WMI	Watermark interrupt bit indicates that user-defined buffer’s sample threshold, has been exceeded when in FIFO or Stream modes. Not used in Trigger mode. This bit is automatically cleared when buffer is read, and the content is below the watermark threshold as defined by SMP [6:0] in BUF_CNTL1 register. WMI = 0 - Buffer watermark has not been exceeded. WMI = 1 - Buffer watermark has been exceeded.
DRDY	Reports that new acceleration data is available. This bit is cleared when acceleration data is read or the interrupt release register INT_REL is read. DRDY = 0 - New acceleration data is not available. DRDY = 1 - New acceleration data is available.
WUFS	Reports the Wake-up interrupt status. This bit is cleared when the interrupt latch release register INT_REL is read. WUFS = 1 - Wake-up event is detected. WUFS = 0 - No Wake-up event is detected.

Register Map – continued

(14h) INS3

Motion Engine Interrupt Status register reports the axis and direction of detected motion that triggered the Wake-up and Back-to-sleep interrupt.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
14h	INS3	R	0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU

Fields	Function
XNWU	X Negative (X-) Reported
XPWU	X Positive (X+) Reported
YNWU	Y Negative (Y-) Reported
YPWU	Y Positive (Y+) Reported
ZNWU	Z Negative (Z-) Reported
ZPWU	Z Positive (Z+) Reported

(15h) STATUS_REG

This register reports the status of the KX134ACR-LBZ.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
15h	STATUS_REG	R	PC1_STAT	RES_STAT	CRC_F	INT	POR_STAT	STAT_REG	Reserved	WAKE

Fields	Function
PC1_STAT	Reports if the PC1 bit in CNTL1 register is set. PC1_STAT = 0 - PC1 bit in CNTL1 register is not set. PC1_STAT = 1 - PC1 bit in CNTL1 register is set.
RES_STAT	Reports if the RES bit in CNTL1 register is set. RES_STAT = 0 - RES bit in CNTL1 register is not set. RES_STAT = 1 - RES bit in CNTL1 register is set.
CRC_F	Reports One Time Programmable (OTP) memory load failure. CRC_F = 0 - OTP load was successful. CRC_F = 1 - OTP load has failed. Perform Software Reset or Power Cycle the device.
INT	Reports the combined (OR) interrupt information according to interrupt setting. INT = 0 - No interrupt events were detected. INT = 1 - Interrupt event was detected.
POR_STAT	Reports the POR status of KX134ACR-LBZ. POR_STAT = 0 - No POR events. POR_STAT = 1 - POR event has occurred. Reading STATUS_REG automatically clears the POR_STAT bit.
STAT_REG	Reports whether KX134ACR-LBZ is running and sensing motion is OK. STAT_REG = 0 - The accelerometer is either in Standby Mode or has detected that supplied VDD is below the minimum required, in which case the output data may not be valid. STAT_REG = 1 - The accelerometer is running and sensing motion.
WAKE	Reports the wake/back to sleep state. WAKE = 0 - KX134ACR-LBZ is in the Sleep state. WAKE = 1 - KX134ACR-LBZ is in the Wake state. Note that the WAKE bit just indicates the motion detection status, no KX134ACR-LBZ power mode changes. The Sleep state is the default after power-up.

Register Map – continued

(17h) INT_REL

Latched interrupt source information is cleared, and physical interrupt latched pin is changed to its inactive state when this register is read. Read value is dummy.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
17h	INT_REL	R	INT_REL							

(18h) CNTL1

Read/write control register that provides more feature set control. Note that to change the value of this bit, the PC1 bit must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
18h	CNTL1	R/W	PC1	RES	DRDYE	GSEL [1:0]		0	WUFE	0

default value 00h

Fields	Function
PC1	Controls the operating mode of the KX134ACR-LBZ. When in RES = 0, allow 1.2/ODR delay time when transitioning from standby PC1 = 0 to operating mode PC1 = 0 - KX134ACR-LBZ is in the Standby Mode. PC1 = 1 - KX134ACR-LBZ is in the either Low Power Mode or High Resolution Mode. <table><tr><th>PC1</th><th>RES</th><th>Power Mode</th></tr><tr><td>0</td><td>Don’t care</td><td>Standby</td></tr><tr><td>1</td><td>0</td><td>Low Power</td></tr><tr><td>1</td><td>1</td><td>High Resolution</td></tr></table>
RES	Determines the power mode of the KX134ACR-LBZ. The noise varies with ODR, RES and different LP_CNTL settings possibly reducing the effective resolution. RES = 0 - Low Power Mode if PC1 = 1 RES = 1 - High Resolution Mode if PC1 = 1
DRDYE	Enables the reporting of the availability of new acceleration data as an interrupt. DRDYE = 0 - Availability of new acceleration data is not reflected as an interrupt. DRDYE = 1 - Availability of new acceleration data is reflected as an interrupt.
GSEL [1:0]	Selects the Acceleration Range of the KX134ACR-LBZ outputs. GSEL [1:0] = 0 - Acceleration range is ±8 g GSEL [1:0] = 1 - Acceleration range is ±16 g GSEL [1:0] = 2 - Acceleration range is ±32 g GSEL [1:0] = 3 - Acceleration range is ±64 g
WUFE	Enables the Wake-up function. WUFE = 0 - Wake-up function is disabled. WUFE = 1 - Wake-up function is enabled.

Register Map – continued

(19h) CNTL2

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
19h	CNTL2	R/W	SRST	COTC	1	1	1	1	1	1

default value 3Fh

Fields	Function
SRST	Initiates Software Reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished with SPI reading. The KX134ACR-LBZ returns NACK with I^{2}C reading during the reboot routine. SRST = 0 - No action SRST = 1 - KX134ACR-LBZ starts the RAM reboot routine.
COTC	Command test control bit. COTC = 0 - No action COTC = 1 - COTR register is set to AAh. COTC bit is self-cleared after the COTR reading. (COTR is also returns to 55h)

(1Ah) CNTL3

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Ah	CNTL3	R/W	1	0	1	0	1	OWUF [2:0]		

default value A8h

Fields	Function
OWUF [2:0]	Sets the output data rate for the Wake-up function and the High-pass filter outputs. The default ODR is 0.781 Hz.

OWUF [2]	**OWUF [1]**	**OWUF [0]**	**Output Data Rate**
0	0	0	0.781 Hz
0	0	1	1.563 Hz
0	1	0	3.125 Hz
0	1	1	6.25 Hz
1	0	0	12.5 Hz
1	0	1	25 Hz
1	1	0	50 Hz
1	1	1	100 Hz

Register Map – continued

(1Bh) ODCNTL

This register is responsible for configuring ODR (output data rate) and filter settings. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Bh	ODCNTL	R/W	0	LPRO	Reserved		OSA [3:0]			

default value 06h

Fields	Function
LPRO	The Low-pass filter roll off control LPRO = 0 - The corner frequency of the Low-pass filter is set to ODR/9. LPRO = 1 - The corner frequency of the Low-pass filter is set to ODR/2.
OSA [3:0]	Acceleration output data rate. The default ODR is 50 Hz for both High Resolution and Low Power Mode. This ODR setting must be equal to or higher than enabled engine ODR setting.

OSA [3]	**OSA [2]**	**OSA [1]**	**OSA [0]**	**Output Data Rate**
0	0	0	0	0.781 Hz*(Note 1)*
0	0	0	1	1.563 Hz*(Note 1)*
0	0	1	0	3.125 Hz*(Note 1)*
0	0	1	1	6.25 Hz*(Note 1)*
0	1	0	0	12.5 Hz*(Note 1)*
0	1	0	1	25 Hz*(Note 1)*
0	1	1	0	50 Hz*(Note 1)*
0	1	1	1	100 Hz*(Note 1)*
1	0	0	0	200 Hz*(Note 1)*
1	0	0	1	400 Hz*(Note 1)*
1	0	1	0	800 Hz
1	0	1	1	1600 Hz
1	1	0	0	3200 Hz
1	1	0	1	6400 Hz
1	1	1	0	12800 Hz
1	1	1	1	25600 Hz

(Note 1) Low Power Mode available.

Register Map – continued

(1Ch) INC1

This register controls the settings for the physical interrupt pin INT1 and the Self-test polarity and SPI interface mode. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	INC1	R/W	PW1 [1:0]		IEN1	IEA1	IEL1	0	STPOL	SPI3E

default value 10h

Fields	Function
PW1 [1:0]	Pulse interrupt width configuration of the physical interrupt pin INT1. PW1 = 0 - 50 μs PW1 = 1 - OSA period PW1 = 2 - 2xOSA period PW1 = 3 - Reserved
IEN1	Sets the enables/disables of the physical interrupt pin INT1. IEN1 = 0 - The physical interrupt pin is disabled. IEN1 = 1 - The physical interrupt pin is enabled.
IEA1	Sets the polarity of the physical interrupt pin INT1. IEA1 = 0 - The polarity of the physical interrupt pin is set to active LOW. IEA1 = 1 - The polarity of the physical interrupt pin is set to active HIGH.
IEL1	Sets the response of the physical interrupt pin INT1. IEL1 = 0 - The physical interrupt pin latches until it is cleared by reading INT_REL. IEL1 = 1 - The physical interrupt pin will transmit one pulse with a period of PW1.
STPOL	Sets the polarity of Self-test. STPOL = 1 - The Self-test polarity is inverted. STPOL = 0 - The Self-test polarity is nominal.
SPI3E	Sets 3-wire SPI Interface Enable. SPI3E = 0 - KX134ACR-LBZ is set to 4-wire SPI mode. SPI3E = 1 - KX134ACR-LBZ is set to 3-wire SPI mode.

Register Map – continued

(1Dh) INC2

This register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Dh	INC2	R/W	0	AOI	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE

default value 3Fh

Fields	Function
AOI	AND-OR configuration on motion detection AOI = 0 - OR combination between selected directions AOI = 1 - AND combination between selected axes Ex. If all directions are enabled, Active state in OR configuration = (XN || XP || YN || YP || ZN || ZP) Active state in AND configuration = (XN || XP) & (YN || YP) & (ZN || ZP)
XNWUE	XNWUE = 0 - X negative(XN) is disabled. XNWUE = 1 - X negative(XN) is enabled.
XPWUE	XPWUE = 0 - X positive(XP) is disabled. XPWUE = 1 - X positive(XP) is enabled.
YNWUE	YNWUE = 0 - Y negative(YN) is disabled. YNWUE = 1 - Y negative(YN) is enabled.
YPWUE	YPWUE = 0 - Y positive(YP) is disabled. YPWUE = 1 - Y positive(YP) is enabled.
ZNWUE	ZNWUE = 0 - Z negative(ZN) is disabled. ZNWUE = 1 - Z negative(ZN) is enabled.
ZPWUE	ZPWUE = 0 - Z positive(ZP) is disabled. ZPWUE = 1 - Z positive(ZP) is enabled.

Register Map – continued

(1Fh) INC4

This register controls routing of an interrupt reporting to physical interrupt pin INT1. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Fh	INC4	R/W	0	BFI1	WMI1	DRDYI1	BTSI1	0	WUFI1	0

default value 00h

Fields	Function
BFI1	BFI1 = 0 – Buffer full interrupt is not reported on physical interrupt pin INT1. BFI1 = 1 – Buffer full interrupt is reported on physical interrupt pin INT1.
WMI1	WMI1 = 0 – Watermark interrupt is not reported on physical interrupt pin INT1. WMI1 = 1 – Watermark interrupt is reported on physical interrupt pin INT1.
DRDYI1	DRDYI1 = 0 - Data ready interrupt is not reported on physical interrupt pin INT1. DRDYI1 = 1 - Data ready interrupt is reported on physical interrupt pin INT1.
BTSI1	BTSI1 = 0 - Back-to-sleep interrupt is not reported on physical interrupt pin INT1. BTSI1 = 1 - Back-to-sleep interrupt is reported on physical interrupt pin INT1
WUFI1	WUFI1 = 0 - Wake-up interrupt is not reported on physical interrupt pin INT1. WUFI1 = 1 - Wake-up interrupt is reported on physical interrupt pin INT1.

(20h) INC5

This register controls the settings for the physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
20h	INC5	R/W	PW2[1:0]		IEN2	IEA2	IEL2	ACLR2	ACLR1	0

default value 10h

Fields	Function
PW2 [1:0]	Pulse interrupt width configuration of the physical interrupt pin INT2. PW2 = 0 - 50 µs PW2 = 1 - OSA period PW2 = 2 - 2xOSA period PW2 = 3 - Reserved
IEN2	Enables/disables the physical interrupt pin INT2. IEN2 = 0 - The physical interrupt pin is disabled. IEN2 = 1 - The physical interrupt pin is enabled.
IEA2	Sets the polarity of the physical interrupt pin INT2. IEA2 = 0 - The polarity of the physical interrupt pin is set to active LOW. IEA2 = 1 - The polarity of the physical interrupt pin is set to active HIGH.
IEL2	Sets the response of the physical interrupt pin INT2. IEL2 = 0 - The physical interrupt pin latches until it is cleared by reading INT_REL. IEL2 = 1 - The physical interrupt pin will transmit one pulse with a period of PW2.
ACLR2	Enables/disables INT2 auto interrupt latch clear for WUF and BTS. ACLR2 = 0 - Latched interrupt is not automatically cleared. Until it is cleared by reading INT_REL, the pulse interrupt will not occur even if detected. ACLR2 = 1 - Latched interrupt is automatically cleared. The pulse interrupt will occur on each detection without reading INT_REL.
ACLR1	Enables/disables INT1 auto interrupt latch clear for WUF and BTS. ACLR1 = 0 - Latched interrupt is not automatically cleared. Until it is cleared by reading INT_REL, the pulse interrupt will not occur even if detected. ACLR1 = 1 - Latched interrupt is automatically cleared. The pulse interrupt will occur on each detection without reading INT_REL.

Register Map – continued

(21h) INC6

This register controls routing of interrupt reporting to physical interrupt pin INT2. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
21h	INC6	R/W	0	BFI2	WMI2	DRDYI2	BTSI2	0	WUFI2	0

default value 00h

Fields	Function
BFI2	BFI2 = 0 – Buffer full interrupt is not reported on physical interrupt pin INT2. BFI2 = 1 – Buffer full interrupt is reported on physical interrupt pin INT2.
WMI2	WMI2 = 0 – Watermark interrupt is not reported on physical interrupt pin INT2. WMI2 = 1 – Watermark interrupt is reported on physical interrupt pin INT2.
DRDYI2	DRDYI2 = 0 - Data ready interrupt is not reported on physical interrupt pin INT2. DRDYI2 = 1 - Data ready interrupt is reported on physical interrupt pin INT2.
BTSI2	BTSI2 = 0 - Back-to-sleep interrupt is not reported on physical interrupt pin INT2. BTSI2 = 1 - Back-to-sleep interrupt is reported on physical interrupt pin INT2.
WUFI2	WUFI2 = 0 - Wake-up interrupt is not reported on physical interrupt pin INT2. WUFI2 = 1 - Wake-up interrupt is reported on physical interrupt pin INT2.

(23h) WUFC

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
23h	WUFC	R/W	WUFC [7:0]							

default value 00h

Fields	Function
WUFC [7:0]	This register is the initial count register for the Wake-up detection timer. Every count is calculated as 1/ODR delay period, where the ODR is user-defined by OWUF bits in CNTL3 register. A new state must be valid as many measurement periods before the change is accepted.

(2Ch) MAN_WAKE

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Ch	MAN_WAKE	W	0	0	0	0	0	0	MAN_WAKE	MAN_SLEEP

default value 00h

Fields	Function
MAN_WAKE	Manual wake/sleep engine override MAN_WAKE = 0 - No action MAN_WAKE = 1 - The wake state is forced to WAKE state. (The MAN_WAKE bit is self-cleared)
MAN_SLEEP	Manual wake/sleep engine override MAN_SLEEP = 0 - No action MAN_SLEEP = 1 - The wake state is forced to SLEEP state. (The MAN_SLEEP bit is self-cleared)

Register Map – continued

(2Dh) BTS_CNTL

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	BTS_CNTL	R/W	BTSE	0	0	0	0	OBTS [2:0]		

default value 00h

Fields	Function
BTSE	Enables the Back-to-sleep function. Note that to change the value of this bit, the PC1 bit must first be set to ‘0’. BTSE = 0 - Back-to-sleep function is disabled. BTSE = 1 - Back-to-sleep function is enabled.
OBTS [2:0]	Sets the output data rate for the Back-to-sleep and the High-pass filter outputs. The default ODR is 0.781 Hz.

OBTS [2]	OBTS [1]	OBTS [0]	Output Data Rate
0	0	0	0.781 Hz
0	0	1	1.563 Hz
0	1	0	3.125 Hz
0	1	1	6.25 Hz
1	0	0	12.5 Hz
1	0	1	25 Hz
1	1	0	50 Hz
1	1	1	100 Hz

(2Eh) BTSC

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	BTSC	R/W	BTSC [7:0]							

default value 00h

Fields	Function
BTSC [7:0]	This register is the initial count register for the Back-to-sleep detection timer. Every count is calculated as 1/ODR delay period, where the ODR is user-defined by OBTS bits in BTS_CNTL register. A new state must be valid as many measurement periods before the change is accepted.

Register Map – continued

(2Fh-31h) BTS_TH, WUF_TH, BTS_WUF_TH

Note that to properly change the value of these register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	BTS_TH	R/W	BTSTH [7:0]							

default value 80h

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30h	WUF_TH	R/W	WUFTH [7:0]							

default value 80h

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31h	BTS_WUF_TH	R/W	0	BTSTH [10:8]			0	WUFTH [10:8]		

default value 00h

Fields	Function
BTSTH [10:0]	This register sets the threshold for the Back-to-sleep function. KX134ACR-LBZ will ship from the factory with this value set to correspond to a change in acceleration of 2.0 g.

Fields	Function
WUFTH [10:0]	This register sets the threshold for the Wake-up function. KX134ACR-LBZ will ship from the factory with this value set to correspond to a change in acceleration of 2.0 g.

(35h) LP_CNTL

Low Power Control sets the number of samples of accelerometer output to be averaged. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
35h	LP_CNTL	R/W	1	AVC [2:0]			1	0	1	1

default value CBh

Fields	Function
AVC [2:0]	Averaging Filter Control in Low Power Mode, the default setting is 16 samples averaged.

AVC [2]	**AVC [1]**	**AVC [0]**	**Number of Averaging**
0	0	0	Reserved
0	0	1	2 Samples Averaged
0	1	0	4 Samples Averaged
0	1	1	8 Samples Averaged
1	0	0	16 Samples Averaged
1	0	1	32 Samples Averaged
1	1	0	64 Samples Averaged
1	1	1	128 Samples Averaged

Register Map – continued

(3Ah) BUF_CNTL1

Read/write control register that controls the buffer sample threshold. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Ah	BUF_CNTL1	R/W	Reserved	SMP [6:0]						

default value 00h

Fields	Function
SMP [6:0]	Determines the number of samples that will trigger a watermark interrupt or will be saved prior to a trigger event. When BRES = 1, the maximum number of samples is 43; when BRES = 0, the maximum number of samples is 86. In the case of FIFO and Stream mode, SMP specifies how many buffer samples are needed to trigger a watermark interrupt. In the case of Trigger mode, SMP specifies how many buffer samples before the trigger event are retained in the buffer.

(3Bh) BUF_CNTL2

Read/write control register that controls sample buffer operation. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Bh	BUF_CNTL2	R/W	BUFE	BRES	BFIE	Reserved			BM [1:0]	

default value 00h

<table>
<tr><th>Fields</th><th>Function</th></tr>
<tr><td>BUFE</td><td>Controls activation of the sample buffer.
BUFE = 0 - The sample buffer is disabled.
BUFE = 1 - The sample buffer is enabled.</td></tr>
<tr><td>BRES</td><td>Determines the resolution of the acceleration data samples collected by the sample buffer.
BRES = 0 - 8-bits samples are accumulated in the buffer.
BRES = 1 - 16-bits samples are accumulated in the buffer.</td></tr>
<tr><td>BFIE</td><td>Buffer full interrupt enable.
BFIE = 0 - The buffer full interrupt is disabled.
BFIE = 1 - The buffer full interrupt is enabled.</td></tr>
<tr><td>BM [1:0]</td><td>Selects the operating mode of the sample buffer.
<table>
<tr><th>BM [1]</th><th>BM [0]</th><th>Mode</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>FIFO</td><td>The buffer collects 86 sets of 8-bit low resolution values or 43 sets of 16-bit high resolution values and then stops collecting data, collecting new data only when the buffer is not full.</td></tr>
<tr><td>0</td><td>1</td><td>Stream</td><td>The buffer holds the last 86 sets of 8-bit low resolution values or 43 sets of 16-bit high resolution values. Once the buffer is full, the oldest data is discarded to make room for newer data.</td></tr>
<tr><td>1</td><td>0</td><td>Trigger</td><td>When a trigger event occurs, the buffer holds the last data set of SMP [6:0] samples before the trigger event and then continues to collect data until full. New data is collected only when the buffer is not full.</td></tr>
</table></td></tr>
</table>

Register Map – continued

(3Ch) BUF_STATUS_1

This register reports the status of the sample buffer.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Ch	BUF_STATUS_1	R	SMP_LV [7:0]							

Fields	Function
SMP_LV [7:0]	Reports the number of data bytes that have been stored in the sample buffer. When BRES = 1, this count will increase by 6 for each 3-axis sample in the buffer; when BRES = 0, the count will increase by 3 for each 3-axis sample. If this register reads 0, no data has been stored in the buffer.

(3Dh) BUF_STATUS_2

This register reports the status of the sample buffer trigger function.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	BUF_STATUS_2	R	BUF_TRIG	0	0	0	0	0	0	0

Fields	Function
BUF_TRIG	Reports the status of the buffer’s trigger function if this mode has been selected. When using trigger mode, a buffer read should only be performed after a trigger event.

(3Eh) BUF_CLEAR

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Eh	BUF_CLEAR	W	BUF_CLEAR [7:0]							

default value 00h

Fields	Function
BUF_CLEAR [7:0]	Latched buffer status information and the entire sample buffer are cleared when any data is written to this register.

(3Fh) BUF_READ

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Fh	BUF_READ	R	BUF_READ [7:0]							

Fields	Function
BUF_READ [7:0]	Buffer output register. Note, new data is not being written to the buffer during the buffer read operation. Thus, care must be taken when reading from the buffer. If data loss is not desired, the buffer read operation should be completed within ODR cycle.

Register Map – continued

(46h) BTS_WUF_CNTL

This register controls Wake-up and Back-to-sleep engine mode. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to ‘0’.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
46h	BTS_WUF_CNTL	R/W	0	TH_MODE	C_MODE_BTS	C_MODE_WUF	0	0	0	1

default value 41h

Fields	Function
TH_MODE	Determines the threshold mode of Wake-up function/Back-to-sleep engine. TH_MODE = 0 - Engine is set to absolute threshold mode. TH_MODE = 1 - Engine is set to relative threshold mode.
C_MODE_BTS	Determines the Back-to-sleep debounce counter mode. C_MODE_BTS = 0 - The Back-to-sleep debounce counter is set to count up/reset. C_MODE_BTS = 1 - The Back-to-sleep debounce counter is set to count up/down.
C_MODE_WUF	Determines the Wake-up function debounce counter mode. C_MODE_WUF = 0 - The Wake-up function debounce counter is count up/reset. C_MODE_WUF = 1 - The Wake-up function debounce counter is count up/down.

(60h) SELFTEST

Self-test Enable register.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
60h	SELFTEST	W	SELFTEST [7:0] (activation key = CAh)							

Fields	Function
SELFTEST [7:0]	Writing activation key (CAh) causes the KX134ACR-LBZ into the Self-test mode.

To perform the Self-test, the following procedure is required:

(1) Set PC1 bit to ‘0’ in CNTL1 register to disable KX134ACR-LBZ.
(2) Write CAh to this register to enable the MEMS Self-test function.
(3) Set PC1 bit to ‘1’ in CNTL1 register to enable KX134ACR-LBZ.

Once the Self-test function is enabled, electrostatic actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Calculate the Self-test (ST) response.

ST [g] = | ((OUTPUT_ST_ON [counts]) - (OUTPUT_ST_OFF [counts])) | / Sensitivity [counts/g]

The Self-test response should be compared to the product specifications to determine if the MEMS response is within the specified range (see the Electrical Characteristic table). To disable the Self-test mode, any of the following methods can be used:

(1) Power Cycle KX134ACR-LBZ.
(2) Perform Software Reset by setting SRST bit to 1 in CNTL2 register.
(3) Set PC1 bit to 0 in CNTL1 register, then write 00h to this register.

Motion Interrupt

KX134ACR-LBZ features an advanced threshold interrupt by the internal Wake-up and Back-to-sleep digital engines. These engines allow the KX134ACR-LBZ to trigger interrupts when accelerometer activity falls below a defined threshold window (Back-to-sleep) or exceeds a threshold window (Wake-up event). Note that this function only generates an interrupt and doesn’t trigger any changes to the part configuration (e.g. power mode, ODR, etc.).

1. Enabling/Disabling

The Wake-up and Back-to-sleep detection can be enabled/disabled using WUFE bit in CNTL1 and BTSE bit in BTS_CNTL register and the direction of motion detection can be set for any axis in INC2 register.

2. Debounce Counter

The Wake-up and Back-to-sleep digital engines have an internal debounce counter to qualify motion status detection. The debounce counter function can be set using either C_MODE_BTS or C_MODE_WUF bit in BTS_WUF_CNTL register. The counter can be configured to either reset or decrement itself if accelerometer data has either fallen below or risen above the threshold for Wake-up or Back-to-sleep functionality respectively. Note that each Wake-up Function Counter (WUFC) count qualifies 1 (one) user-defined Wake-up Function ODR period as set by OWUF [2:0] bits in CNTL3 register. Similarly, each Back-to-sleep Counter (BTSC) count qualifies 1 (one) user-defined Back-to-sleep function ODR period as set by OBTS [2:0] bits in BTS_CNTL register. Following equation shows how to calculate the WUFC and BTSC register values for a desired Wake-up and Back-to-sleep delay times.

WUFC (counts) = Wake-up Delay Time (s) x Wake-up Function ODR (Hz)
BTSC (counts) = Back-to-sleep Delay Time (s) x Back-to-sleep Function ODR (Hz)

3. Threshold Resolution

The motion interrupt threshold values are set by WUFTH [10:0] and BTSTH [10:0] bits in BTS_TH, WUF_TH and BTS_WUF_TH registers. The values in these registers are compared to the top 11 bits of the accelerometer 32 g output regardless of GSEL [1:0] setting in CNTL1 register. This results in threshold resolution of 15.6 mg/counts.

2^{11} counts/32 g = 2048 counts/32 g = 64 counts/g or 15.6 mg/counts.

4. Threshold Calculation

To calculate the desired Wake-up Threshold (WUFTH) and Back-to-sleep Threshold (BTSTH). Note that the Wake-up engine function is independent of the user selected Acceleration Range.

WUFTH (counts) = Wake-up Threshold (g) x 64 (counts/g)
BTSTH (counts) = Back-to-sleep Threshold (g) x 64 (counts/g)

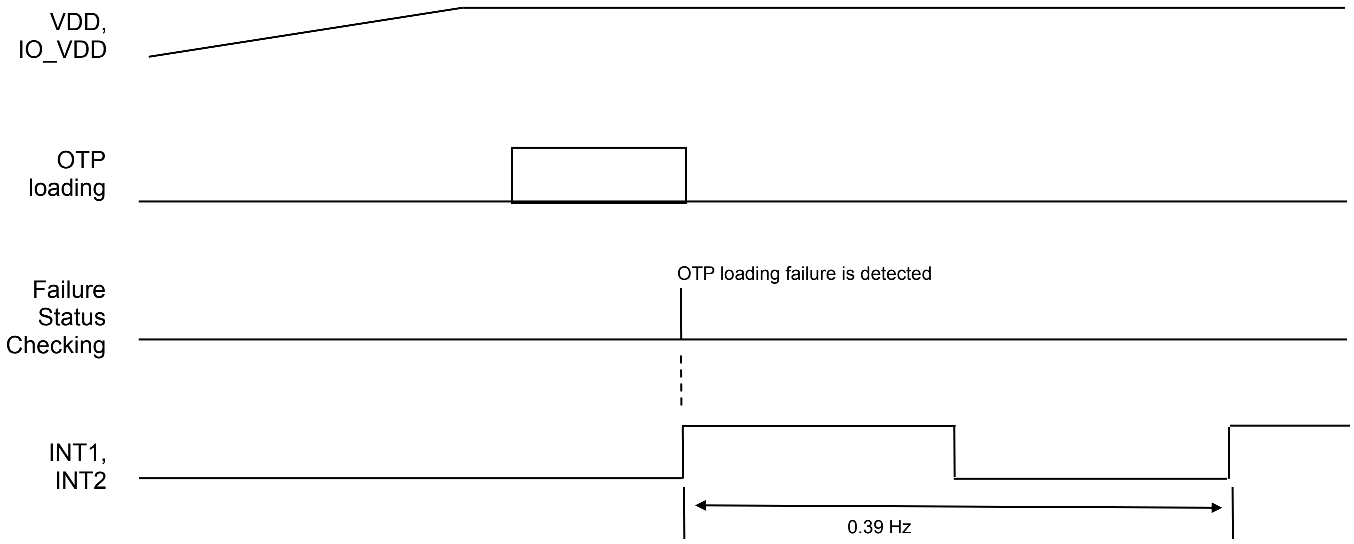
5. Relative/Absolute Threshold Modes Select

The type of threshold used for motion interrupt is controlled using the TH_MODE bit in BTS_WUF_CNTL register. The threshold can be set to either an absolute acceleration value or a relative acceleration value.

Failure Report Function

KX134ACR-LBZ has the OTP memory load failure report function which are routed on INT1 and INT2. Note that the failure report function is prioritized than interrupt function. INT1 and INT2 toggle even if the IEN1 and IEN2 are not set, and any interrupt is ignored.
The failures are also reported on the CRC_F bit in STATUS_REG register.

The CRC_F bit is set, and INT1 and INT2 pins toggle IO_VDD and GND levels when the failure is detected. Perform Software Reset or Power Cycle the device when the failure is detected. This report function is available with any power-mode.



Sample Buffer Feature Description

The sample buffer feature of the KX134ACR-LBZ accumulates and outputs acceleration data based on how it is configured. There are 3 buffer modes available, and samples can be accumulated at either low (8-bits) or high (16-bits) resolution. Acceleration data is collected at the ODR specified by OSA [3:0] in the ODCNTL register. Each buffer mode accumulates data, reports data, and interacts with status indicators in a slightly different way.

1. FIFO Mode

Data Accumulation

Sample collection stops when the buffer is full.

Data Reporting

Data is reported with the oldest byte of the oldest sample first (X_L or X, based on resolution).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples. (calculated with below Equation).

BRES=0:
SMPX = SMP_LV [7:0] / 3 - SMP [6:0]

BRES=1:
SMPX = SMP_LV [7:0] / 6 - SMP [6:0]

Equation 1. Samples Above Sample Threshold

2. Stream Mode

Data Accumulation

Sample collection continues when the buffer is full; older data is discarded to make room for newer data.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

A watermark interrupt occurs when the number of samples in the buffer reaches the Sample Threshold. The watermark interrupt stays active until the buffer contains less than this number of samples. This can be accomplished through clearing the buffer or explicitly reading greater than SMPX samples (calculated with Equation 1).

3. Trigger Mode

Data Accumulation

When a physical interrupt is caused by one of the digital engines, or when a logic HIGH signal occurs on TRIG pin, the trigger event is asserted and SMP [6:0] samples prior to the event are retained. Sample collection continues until the buffer is full.

Data Reporting

Data is reported with the oldest sample first (uses FIFO read pointer).

Status Indicators

When a physical interrupt occurs or when a logic HIGH signal occurs on the TRIG pin, and there are at least SMP [6:0] samples in the buffer, BUF_TRIG bit in BUF_STATUS_2 is asserted. This bit should be cleared by writing to BUF_CLEAR register to prevent Buffer Full interrupt from firing while TRIG pin remains de-asserted.

Buffer Operation

The following diagrams illustrate the operation of the buffer conceptually. Actual physical implementation has been abstracted to offer a simplified explanation of how the different buffer modes operate. Figure 1 represents a high-resolution 3-axis sample within the buffer. Figure1 – Figure9 represent a 10-sample version of the buffer (for simplicity), with Sample Threshold set to 8. Regardless of the selected mode, the buffer fills sequentially, one byte at a time. It is important to keep in mind that new data is not being written to the buffer during the buffer read operation. Thus, care must be taken when reading from the buffer.
If data loss is not desired, the buffer read operation should be completed within ODR cycle.

Figure 1 shows one 6-bytes data sample. Note the location of the FIFO read pointer.

	Index	**Byte**	
	0	X_L	← FIFO read pointer
	1	X_H	
	2	Y_L	
	3	Y_H	
	4	Z_L	
	5	Z_H	
Buffer write pointer →	6		

Figure 1. One Buffer Sample

Regardless of the selected mode, the buffer fills sequentially, one sample at a time. Note in Figure 2 the location of the FIFO read pointer. The buffer write pointer shows where the next sample will be written to the buffer.

	Index	**Sample**	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
Buffer write pointer →	3		
	4		
	5		
	6		
	7		← Sample Threshold
	8		
	9		

Figure 2. Buffer Filling

Buffer Operation – continued

The buffer continues to fill sequentially until the Sample Threshold is reached. Note in Figure 3 the location of the FIFO read pointer.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
Buffer write pointer →	7		← Sample Threshold
	8		
	9		

Figure 3. Buffer Approaching Sample Threshold

In FIFO and Stream modes, a watermark interrupt is issued when the number of samples in the buffer reaches the Sample Threshold. In trigger mode, this is the point where the oldest data in the buffer is discarded to make room for newer data.

	Index	Sample	
	0	Data0	← FIFO read pointer
	1	Data1	
	2	Data2	
	3	Data3	
	4	Data4	
	5	Data5	
	6	Data6	
	7	Data7	← Sample Threshold
Buffer write pointer →	8		
	9		

Figure 4. Buffer at Sample Threshold

Buffer Operation – continued

In trigger mode, data is accumulated in the buffer sequentially until the Sample Threshold is reached. Once the Sample Threshold is reached, the oldest samples are discarded when new samples are collected. Note in Figure 5 how Data0 was thrown out to make room for Data8.

	Index	Sample	
	0	Data1	← Trigger read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
Trigger write pointer →	7	Data8	← Sample Threshold
	8		
	9		

Figure 5. Additional Data Prior to Trigger Event

After a trigger event occurs, the buffer no longer discards the oldest samples, and instead begins accumulating samples sequentially until full. The buffer then stops collecting samples, as seen in Figure 6. This results in the buffer holding SMP [6:0] samples prior to the trigger event, and SMPX samples after the trigger event.

Index	Sample	
0	Data1	← Trigger read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	

Figure 6. Additional Data After Trigger Event

Buffer Operation – continued

In FIFO, Stream, and Trigger (after a trigger event has occurred) modes, the buffer continues filling sequentially after the Sample Threshold is reached. Sample accumulation after the buffer is full depends on the selected operation mode. FIFO and Trigger modes stop accumulating samples when the buffer is full, and Stream mode begin discarding the oldest data when new samples are accumulated.

Index	Sample	
0	Data0	← FIFO read pointer
1	Data1	
2	Data2	
3	Data3	
4	Data4	
5	Data5	
6	Data6	
7	Data7	← Sample Threshold
8	Data8	
9	Data9	

Figure 7. Buffer Full

After the buffer has been filled in Stream mode, the oldest samples are discarded when new samples are collected. Note in Figure 8 how Data0 was thrown out to make room for Data10.

Index	Sample	
0	Data1	← FIFO read pointer
1	Data2	
2	Data3	
3	Data4	
4	Data5	
5	Data6	
6	Data7	
7	Data8	← Sample Threshold
8	Data9	
9	Data10	

Figure 8. Buffer Full - Additional Sample Accumulation in Stream Mode

Buffer Operation – continued

In FIFO, Stream, or Trigger mode, reading one sample from the buffer will remove the oldest sample and effectively shift the entire buffer contents up, as seen in Figure 9.

	Index	Sample	
	0	Data1	← FIFO read pointer
	1	Data2	
	2	Data3	
	3	Data4	
	4	Data5	
	5	Data6	
	6	Data7	
	7	Data8	← Sample Threshold
	8	Data9	
Buffer write pointer →	9		

Figure 9. FIFO Read from Full Buffer

Typical Performance Curves

(Reference data)
(Unless otherwise specified V_{IO_VDD} = 2.5V, V_{VDD} = 2.5 V Ta = 25 °C)

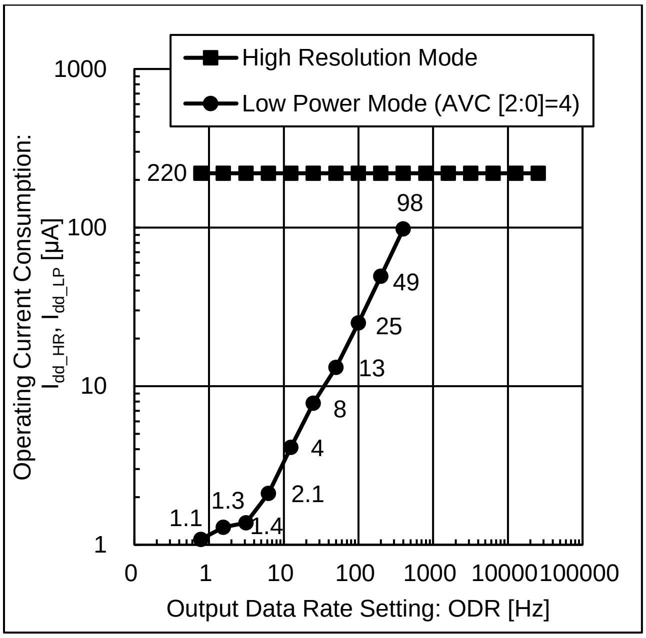


Figure 10. Operating Current Consumption vs ODR

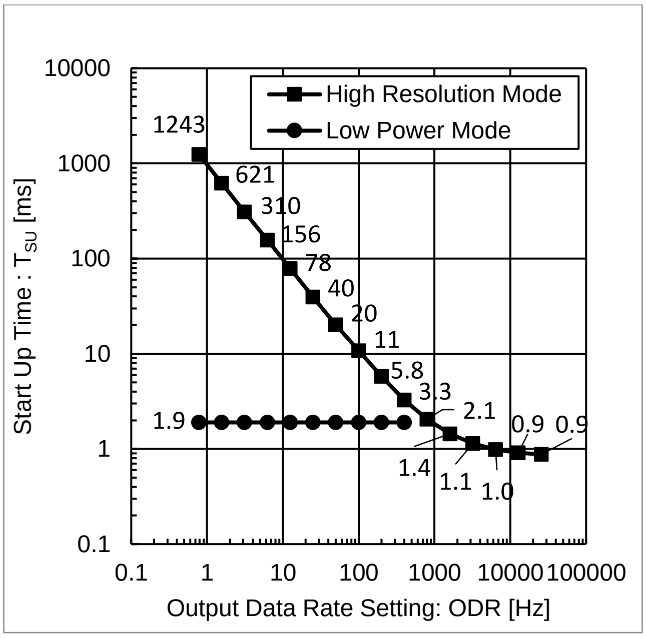
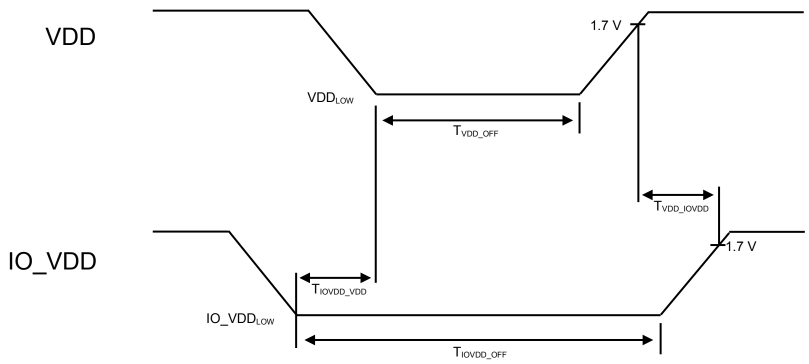


Figure 11. Start Up Time vs ODR

Power On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific VDD$_{LOW}$ and T$_{VDD\_OFF}$ profile of individual applications. It is recommended to minimize VDD$_{LOW}$ and maximize T$_{VDD\_OFF}$. It is also advised that the VDD ramp up time be monotonic. To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD$_{LOW}$, T$_{VDD\_OFF}$ and temperature as POR performance can vary depending on these parameters. Bench Testing has demonstrated POR performance regions for a proper POR trigger. To assure POR trigger properly executes, setting operational thresholds consistent with Table as follows.



(Unless otherwise specified V$_{VDD}$ = 2.5 V, V$_{IO\_VDD}$ = 2.5 V and Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD off time	T$_{VDD\_OFF}$	10	-	-	ms	
IO_VDD off time	T$_{IO\_VDD\_OFF}$	10	-	-	ms	
VDD low voltage	VDD$_{Low}$	-	-	250	mV	
IO_VDD low voltage	IO_VDD$_{Low}$	-	-	250	mV	
IO_VDD low to VDD low time	T$_{IOVDD\_VDD}$	0	-	-	ms	
VDD high to IO_VDD high time	T$_{VDD\_IOVDD}$	0	-	-	ms	

(Note) VDD and IO_VDD must always be monotonic ramps without ambiguous state.

The V$_{IO\_VDD}$ must remain ≤ V$_{VDD}$.

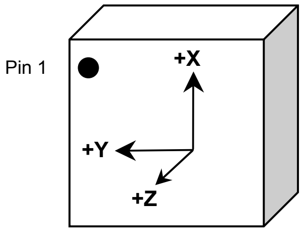
In order to prevent entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND (≤ 250 mV) for duration of time ≥ 10 ms.

The Power-up time is specified in the Electrical Characteristics table

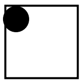
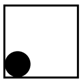
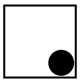
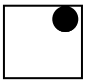
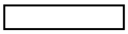
It is important the user determines the timing (T$_{VDD\_OFF}$) and threshold (VDD$_{LOW}$) levels by evaluating the performance in the specific system for which the device will be incorporated.

Orientation

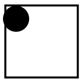
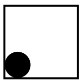
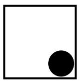
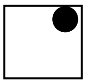
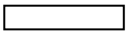
When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.



Static X/Y/Z Output Response versus Orientation to Earth’s surface with GSEL [1:0] = 0 (Acceleration Range: ±8 g)

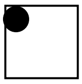
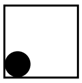
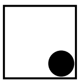
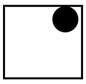
Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram	 Earth’s surface		 Earth’s surface		 Earth’s surface		 Earth’s surface		Top  Bottom Earth’s surface		Bottom  Top Earth’s surface	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+4096	+16	0	0	-4096	-16	0	0	0	0	0	0
Y (counts)	0	0	-4096	-16	0	0	+4096	+16	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+4096	+16	-4096	-16

Static X/Y/Z Output Response versus Orientation to Earth’s surface with GSEL [1:0] = 1 (Acceleration Range: ±16 g)

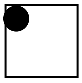
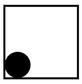
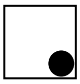
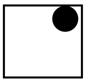
Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram	 Earth’s surface		 Earth’s surface		 Earth’s surface		 Earth’s surface		Top  Bottom Earth’s surface		Bottom  Top Earth’s surface	
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+2048	+8	0	0	-2048	-8	0	0	0	0	0	0
Y (counts)	0	0	-2048	-8	0	0	+2048	+8	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+2048	+8	-2048	-8

Orientation – continued

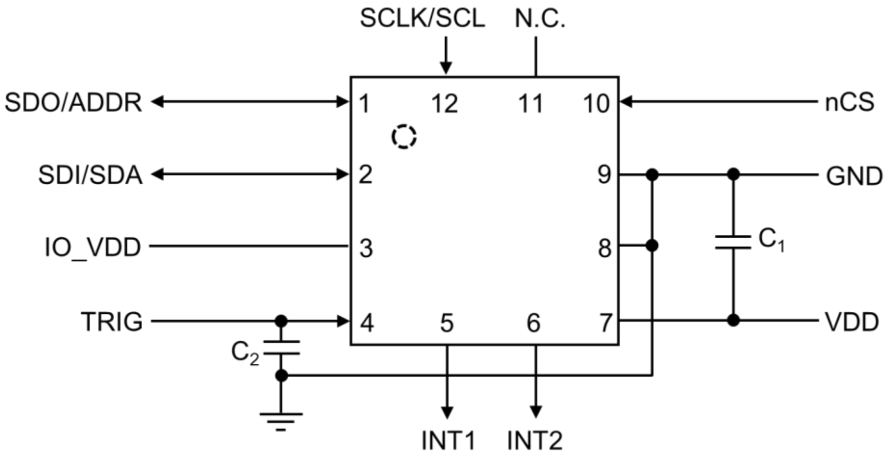
Static X/Y/Z Output Response versus Orientation to Earth’s surface with GSEL [1:0] =2 (Acceleration Range: ±32 g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram												
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+1024	+4	0	0	-1024	-4	0	0	0	0	0	0
Y (counts)	0	0	-1024	-4	0	0	+1024	+4	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+1024	+4	-1024	-4

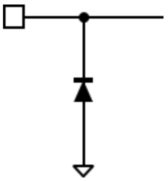
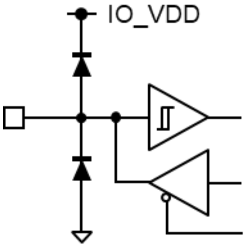
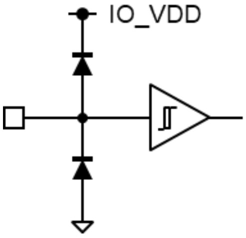
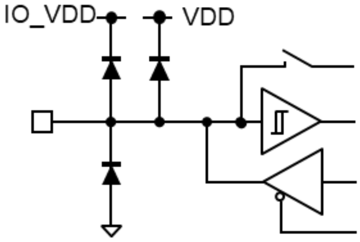
Static X/Y/Z Output Response versus Orientation to Earth’s surface with GSEL [1:0] =3 (Acceleration Range: ±64 g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram												
Resolution (bits)	16	8	16	8	16	8	16	8	16	8	16	8
X (counts)	+512	+2	0	0	-512	-2	0	0	0	0	0	0
Y (counts)	0	0	-512	-2	0	0	+512	+2	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+512	+2	-512	-2

Application Example



I/O Equivalence Circuits

Pin Name	Equivalence Circuit	Pin Name	Equivalence Circuit
VDD IO_VDD		SDI/SDA SDO/ADDR	
SCLK/SCL TRIG nCS		INT1 INT2	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. **Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

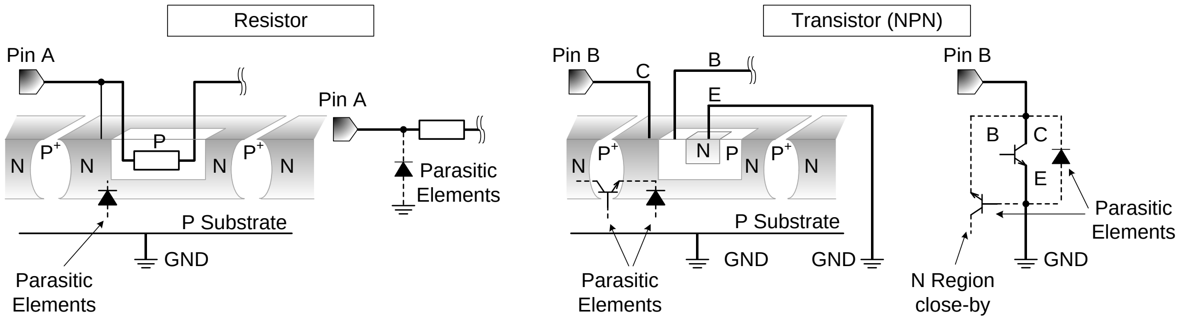
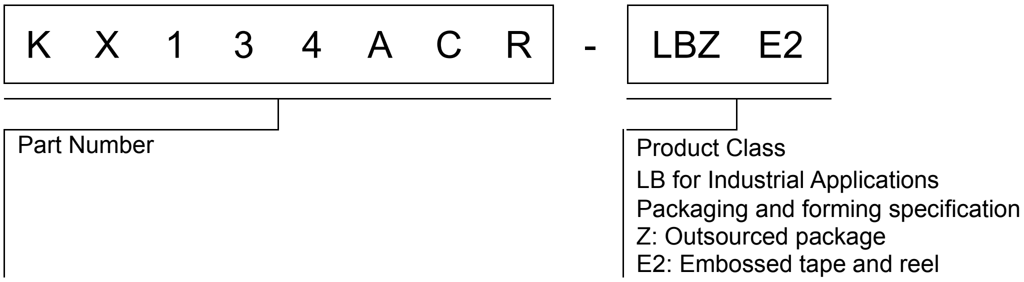


Figure 12. Example of Monolithic IC Structure

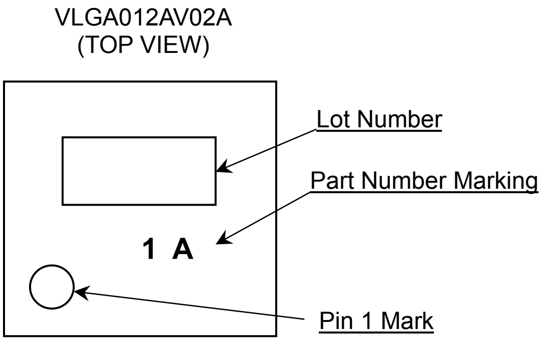
11. **Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

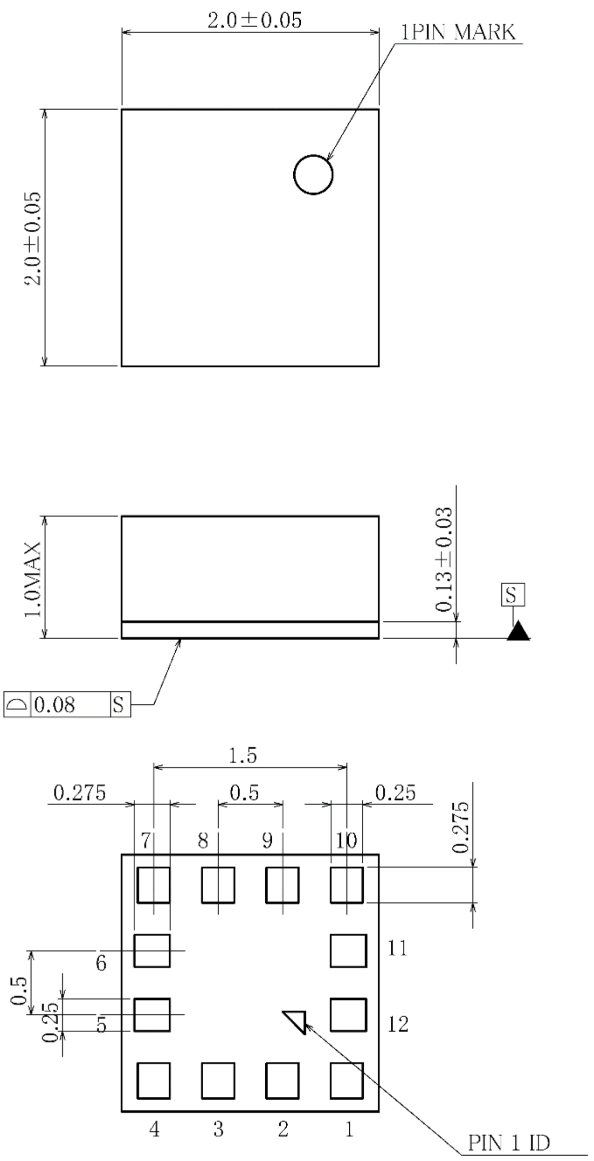


Marking Diagram



Physical Dimension and Packing Information

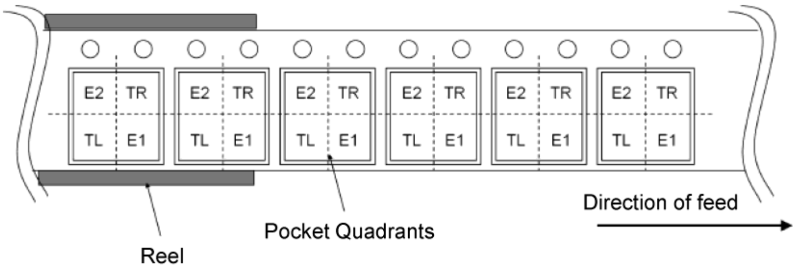
Package Name	VLGA012AV02A



(UNIT:mm)
PKG:VLGA012AV02A
Drawing No.EX001-0132

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	10000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
07.Jul.2023	001	New Release
12.Apr.2024	002	Add Kionix^{TM} logo. Fix typo in docs.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   - [a] Installation of protection circuits or other protective devices to improve system safety
   - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   - [f] Sealing or coating our Products with resin or other coating materials
   - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   - [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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