



Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,  
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"  
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than  
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.  
April 1, 2024

# **RB-D610Q306GD36**

## **User's Manual**

---

Issue Date: March 09, 2021

## Notes

- 1) The information contained herein is subject to change without notice.
- 2) When using LAPIS Technology Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.
- 3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.
- 4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.
- 5) The Products are intended for use in general electronic equipment (AV/OA devices, communication, consumer systems, gaming/entertainment sets, etc.) as well as the applications indicated in this document. For use of our Products in applications requiring a high degree of reliability (as exemplified below), please be sure to contact a LAPIS Technology representative and must obtain written agreement: transportation equipment (cars, ships, trains, etc.), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us. Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc.
- 6) The Products specified in this document are not designed to be radiation tolerant.
- 7) LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Technology does not warrant that such information is error-free and LAPIS Technology shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.
- 8) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.
- 9) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.
- 10) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.
- 11) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) "LAPIS Technology" as used in this document means LAPIS Technology Co., Ltd.

Copyright 2021 LAPIS Technology Co., Ltd.

---

## LAPIS Technology Co., Ltd.

2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan  
<https://www.lapis-tech.com/en/>

## Table of Contents

1.	Overview.....	1
2.	Operational notes.....	1
3.	Board Outline Drawing .....	1
4.	Specification .....	2
4.1.	Jumper pin (PWR/SPVDD/VREF) .....	2
4.2.	ADC.....	3
4.3.	LED .....	3
4.4.	Jack .....	3
4.5.	CN1 Connector .....	4
4.6.	CN2 Connector .....	4
4.7.	CNUE connector.....	4
5.	Appendix.....	5
5.1.	PCB layout.....	5
5.2.	BOM list, Schematic .....	6
6.	Revision History.....	8

## 1. Overview

This instruction manual is for the RB-D610Q306GD36 which is the reference board for ML610Q306 (hereinafter referred to as "MCU").

This board can be combined with on-chip debug tool EASE1000 V2 and software development environment(DUT8 and MWU16) to do the following:

- Development and debugging of the MCU control software.
- Programing control and sound code data to the MCU internal Flash-ROM.
- Voice playback by the MCU.

## 2. Operational notes

The following describes the precautions to follow when handling the RB-D610Q306GD36.

- Turn off the power when inserting and removing jumper socket from PWR/SPVDD/VREF Jumper pin on the RB-D610Q306GD36.
- Turn off the power when attaching and deattaching external board, device and cable from CN1/CN2/CNUE Connector on the RB-D610Q306GD36.
- Connect only monaural speakers to the jack.
- RB-D610Q306GD36 is a device used only by experts in R&D facilities for research and development purposes. RB-D610Q306GD36 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-D610Q306GD36 support. Replace only in case of initial failure.

## 3. Board Outline Drawing

Figure 1 shows an outline drawing of the RB-D610Q306GD36.

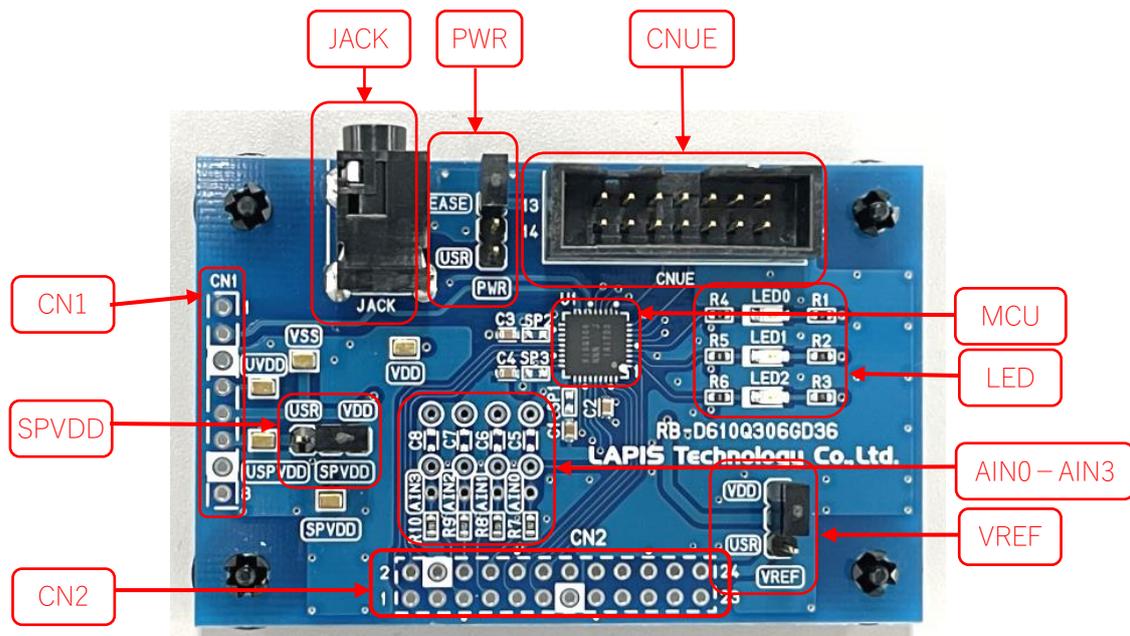


Figure 1 Board Outline Drawing

## 4. Specification

### 4.1. Jumper pin (PWR/SPVDD/VREF)

This board has three jumper pins named PWR/SPVDD/VREF. Each jumper pin specification is explained below.

•PWR jumper pin

PWR jumper pin can switch the supply source of VDD pin of MCU.

PWR	Contents
EASE	VDD pin is connected to 13pin of CNUE.
USR	VDD pin is connected to 4pin (UVDD) of CN1.

When attaching “EASE1000 V2” on the board, PWR jumper pin set to “EASE” if power supply from 13pin of CNUE connector.

PWR jumper pin set to “USR” if power supply from CN1 connector.

•SPVDD jumper pin

SPVDD jumper pin can switch the supply source of SPVDD pin of MCU.

SPVDD	Contents
VDD	SPVDD pin is connected to 2pin of PWR jumper pin.
USR	SPVDD pin is connected to 6pin (USPVDD) of CN1.

SPVDD jumper pin set to “VDD” if power supply from VDD as same as selecting PWR jumper pin.

SPVDD jumper pin set to “USR” if power supply from CN1 connector.

•VREF jumper pin

VREF jumper pin can switch the supply source of VREF pin of MCU.

VREF	Contents
VDD	VREF pin is connected to 2pin of PWR jumper pin.
USR	VREF pin is connected to 24pin (UVREF) of CN2.

VREF jumper pin set to “VDD” if power supply from VDD as same as selecting PWR jumper pin.

VREF jumper pin set to “USR” if power supply from CN2 connector.

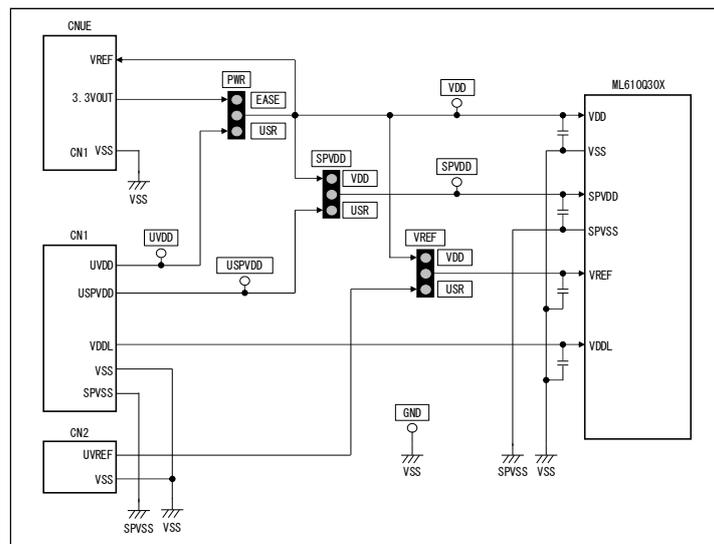


Figure 2 Jumper pin and Power circuit

### 4.2. ADC

Apply voltage to the AIN0-AIN3 pins of MCU from 5-8 pins of CN2 when using ADC function. Mount a noise reduction capacitor on board land indicated by “C5-C8” if necessary. Figure 3 shows the ADC circuit processing example.

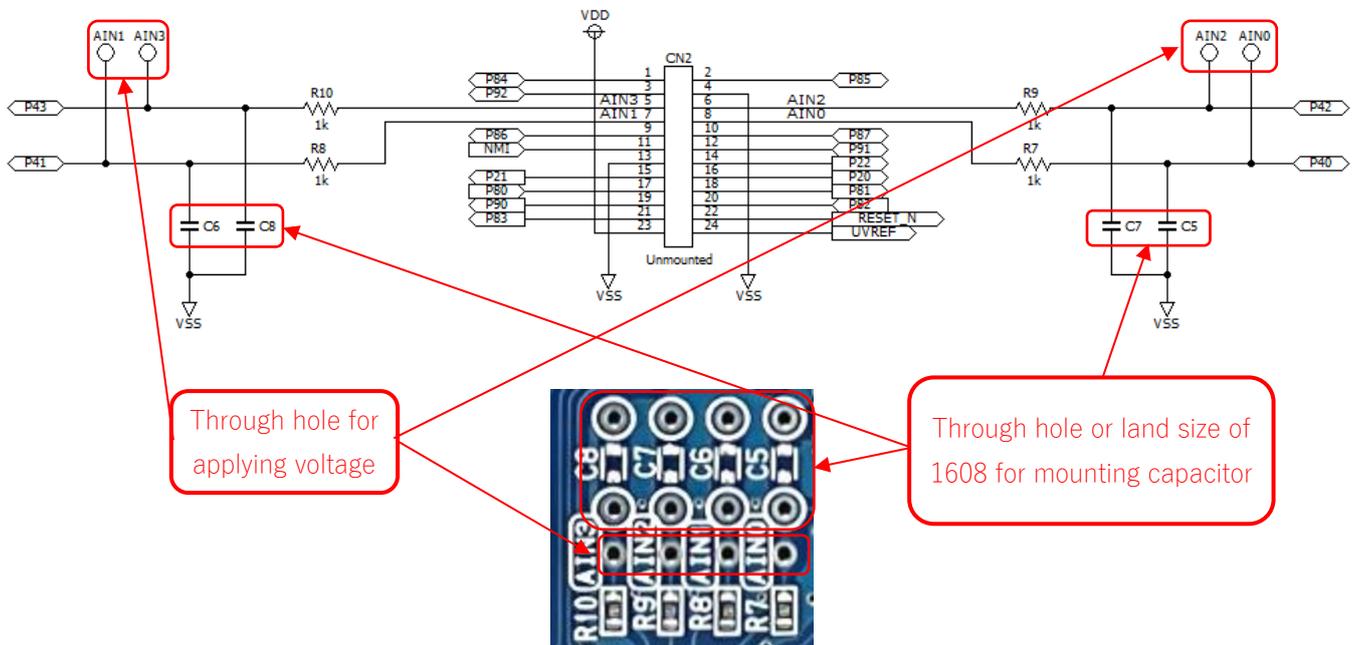


Figure 3 ADC circuit processing example

### 4.3. LED

P20-22 pins of MCU allow direct LEDs drive. Enable to use LEDs connecting these pins when the N-channel open drain output is selected. Unmount register on the board indicated by “R4-R6” when not using LEDs. Figure 4 shows the LED circuit processing example.

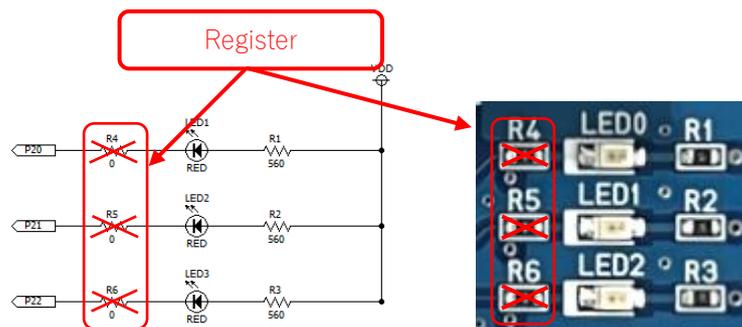


Figure 4 LED circuit processing example

### 4.4. Jack

Jack is connected to SPP/SPM pins of the MCU. Connect only monaural speakers to the jack.

#### 4.5. CN1 Connector

The through hole indicated by “CN1” is enable to mount connector that specification is single row, 8 position and 2.54mm(0.1mil) pich.

The table of CN1 connector pin related to the MCU is shown below.

Connector		MCU		Remarks
Symbol	Number	Pin number	Pin name	
CN1	1	13/14	SPP	
	2	15/16	SPM	
	3	3/23	VSS	
	4	25	VDD	
	5	17/18	SPVSS	
	6	19/20	SPVDD	
	7	3/23	VSS	
	8	24	VDDL	

#### 4.6. CN2 Connector

The through hole indicated by “CN2” is enable to mount connector that specification is Double row, 12 position and 2.54mm(0.1mil) pich.

The table of CN2 connector pin related to the MCU is shown below.

Connector		MCU		Remarks
Symbol	Pin number	Pin number	Pin name	
CN2	1	23	P84	
	2	24	P85	
	3	25	P92	
	4	4/26	VSS	
	5	29	P43/AIN3	
	6	30	P42/AIN2	
	7	31	P41/AIN1	
	8	32	P40/AIN0	
	9	34	P86	
	10	35	P87	
	11	36	NMI	
	12	1	P91	
	13	4/26	VSS	
	14	2	P22	
	15	3	P21	
	16	5	P20	
	17	6	P80	
	18	7	P81	
	19	9	P90	
	20	12	P82	
	21	13	P83	
	22	14	RESET_N	
	23	28	VDD	
	24	33	UVREF	

#### 4.7. CNUE connector

CNUE connector is used to connect the on-chip debug tool EASE1000 V2 manufactured by LAPIS Technology Co.,Ltd. Refer to the “EASE1000 V2 User's Manual” for details.

5. Appendix

5.1. PCB layout

Figure 5 shows the RB-D610Q306GD36 PCB layout.

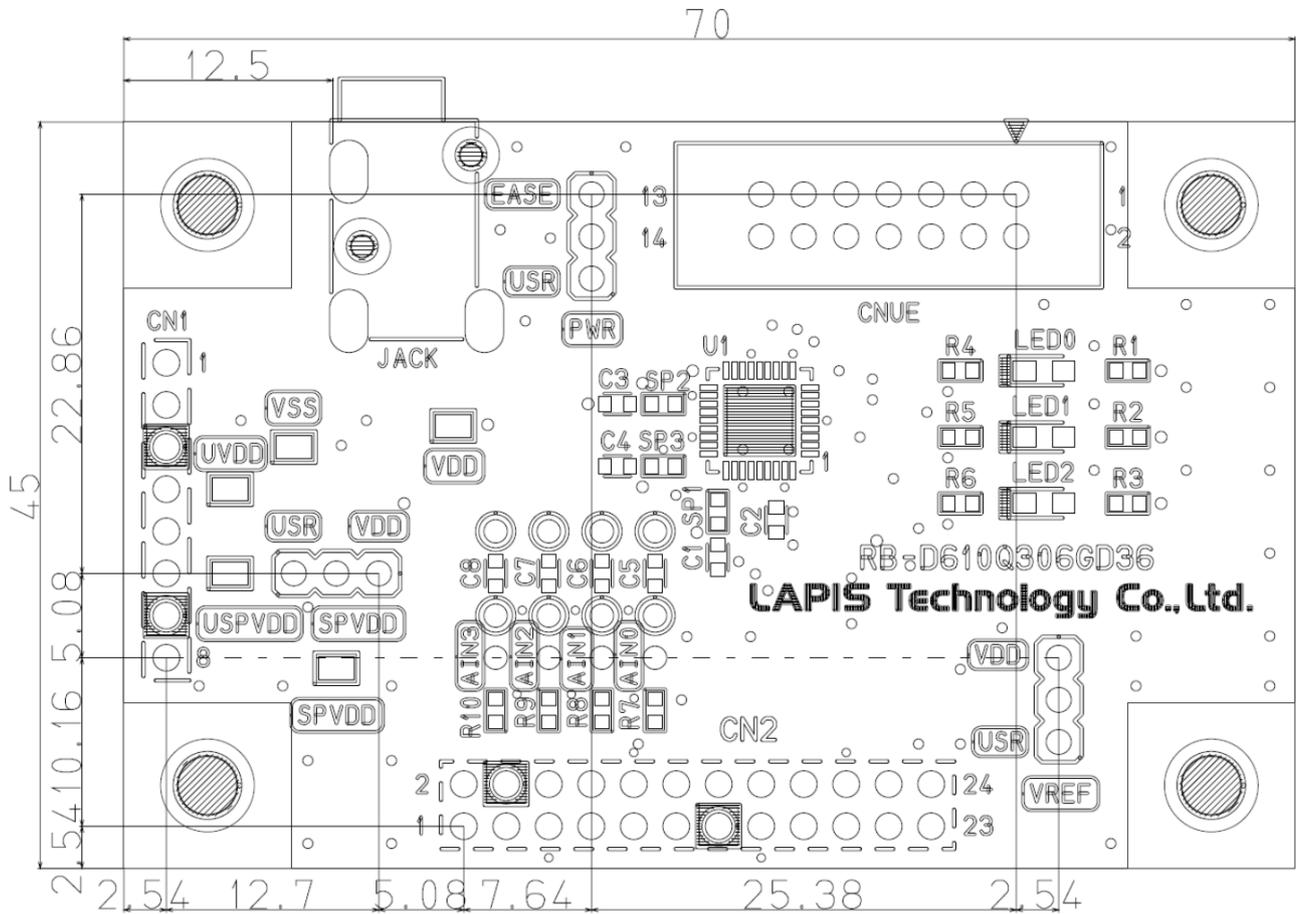
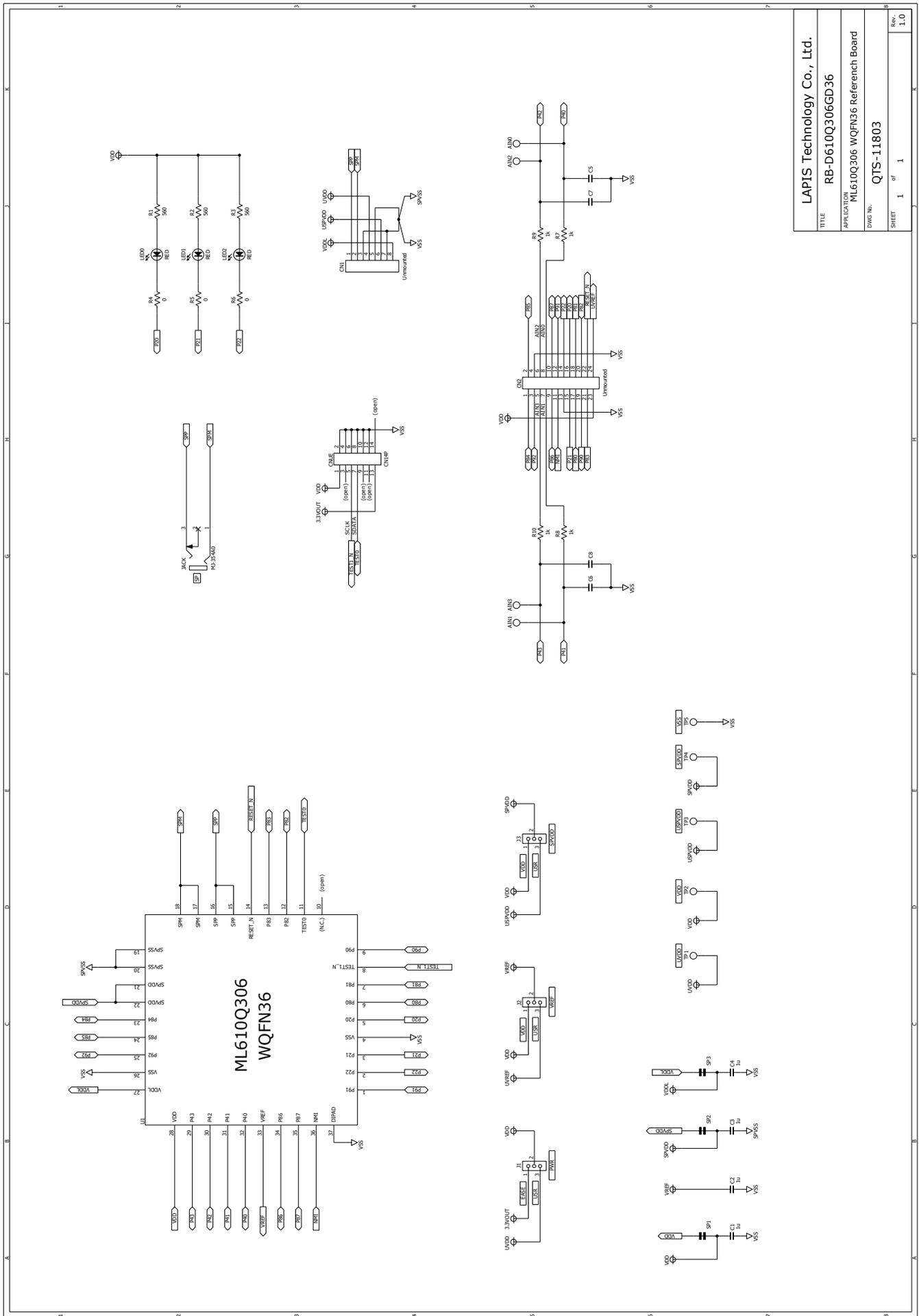


Figure 5 PCB layout

## 5.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11929	RB-D610Q306GD36	PWB	1	LAPIS Technology Co., Ltd.
2	C1608X7R1E105K	C1,C2,C3,C4	Ceramic Capacitor 1uF/25V X7R	4	TDK
3	-	C5,C6,C7,C8	Unmounted	4	-
4	TSW-108-07-F-S	CN1	Unmounted	1	Samtec
5	TSW-112-07-L-D	CN2	Unmounted	1	Samtec
6	HIF3FC-14PA-2.54DSA	CNUE	14pin Header	1	HIROSE
7	MJ-354A0	JACK	Monaural Speaker Jack	1	MARUSHIN
8	SML-M13UT	LED1,LED2,LED3	LED Red	3	ROHM
9	MCR03EZPJ561	R1,R2,R3	Resistor 560Ω ±5%	3	ROHM
10	MCR03EZRJ000	R4,R5,R6	Resistor 0Ω ±5%	3	ROHM
11	MCR03EZPJ102	R7,R8,R9,R10	Resistor 1kΩ ±5%	4	ROHM
12	XJ8B-0311	J1,J2,J3	3pin Header	3	OMRON
13	XJ8A-0214	-	Jumper Socket	3	OMRON
14	HK-3-G	TP1,TP2,TP3,TP4,TP5	Check pin	5	MAC8
15	Test Pad	AIN0,AIN1,AIN2,AIN3	Unmounted	4	-
16	ML610Q306-NNNGD	U1	MCU	1	LAPIS Technology Co., Ltd.
17	FF013-P3555-AR791	-	Rubber leg, Push rivet	4	KOYO FASTENER



TITLE	LAPIS Technology Co., Ltd.
APPLICATION	RB-D610Q306GD36
DWG. No.	ML610Q306 WQFN36 Reference Board
REV.	QTS-11803
SHEET	1 of 1
Rev.	1.0

6. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL610Q306RB-01	Mar 9, 2021	-	-	First edition.