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ROHM Co., Ltd.
April 1, 2024

ROHM GROUP
LAPIS TECHNOLOGY

FEUL630Q464-03

ML630Q464/Q466
User's Manual

Issue Date: Dec.15, 2023

ROHM SEMICONDUCTOR

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LAPIS Technology Co.,Ltd.
2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

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Notes for product usage

Notes on this page are applicable to the all LAPIS Technology microcontroller products.
For individual notes on each LAPIS Technology microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS
   Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON
   At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
   On LAPIS Technology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
   Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY
   If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCTS
   Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
   When replacing from other product to LAPIS Technology microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS Technology microcontroller products.

5. USE ENVIRONMENT
   When using LAPIS Technology microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

Preface

This manual describes the operation of the hardware of the 32-bit microcontroller ML630Q464/Q466.

Please ensure that you refer to the latest versions.

■ Cortex™-M0+ Technical Reference Manual (DDI0484C)
■ Cortex™-M0+ Generic User Guide (DUI0662B)

The documents above are published by ARM Limited. Please ensure that you refer to the latest versions.

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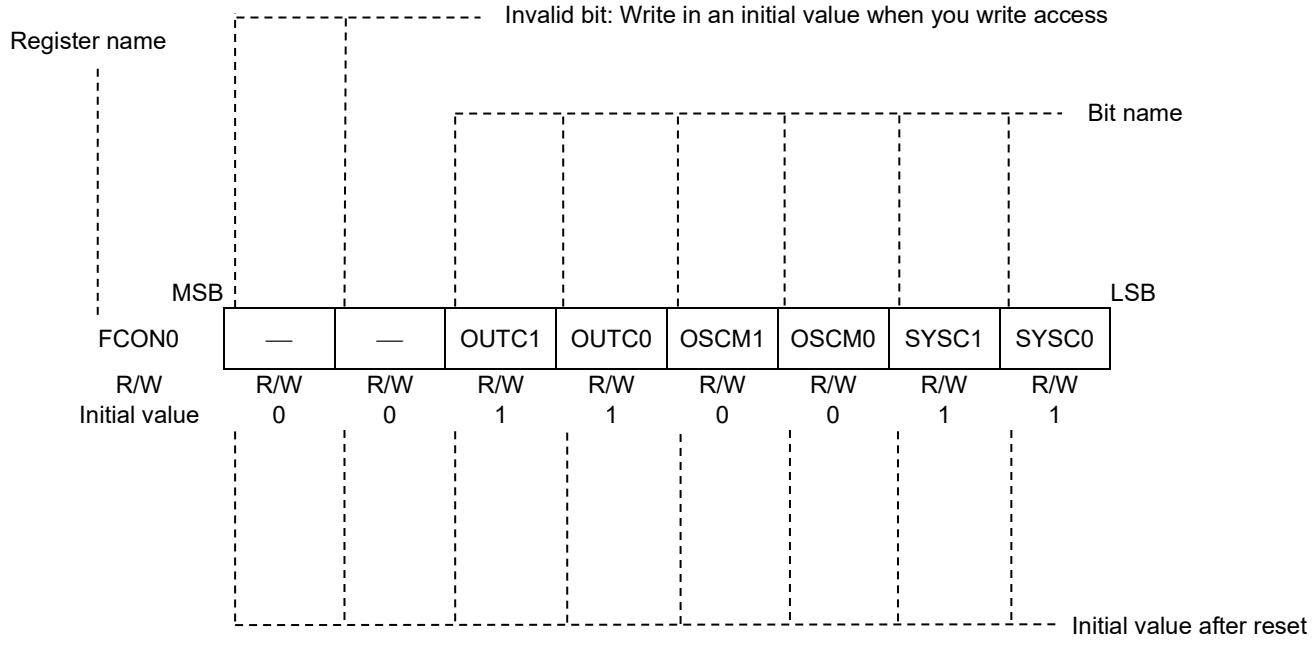
Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	0xnn, 0xnnnn_nnnn	Indicates a hexadecimal number.
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
	0bnn, 0bnnnn_nnnn	Indicates a binary number.
♦ Unit	word, W	1 word = 32 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.



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Chapter 1

Overview

1. Overview

This LSI is a high-performance low power 32-bit microcontroller. Equipped with a 32-bit CPU core ARM®Cortex®M0+, it implements a 128 KB flash memory* 16KB RAM, rich peripheral circuits, such as USB Full speed device, synchronous serial port, UART, I^2C bus interface, supply voltage level detect circuit, RC oscillation type A/D converter, successive approximation type A/D converter, and LCD driver. The Flash ROM* that is installed as program memory achieves low-voltage low-power consumption operation (read operation) is most suitable for battery-driven applications.

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc. SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

- Applications
  Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

  【NOTE】
  This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems.
  Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

1.1. Features

- CPU
  - 32-bit RISC CPU (CPU name: ARM®Cortex®M0+)
  - ARM®Thumb®/Thumb®-2 instruction supported
  - Serial Wire Debug Port
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    41.7ns (@24 MHz system clock)

- Internal memory
  - Re-writing the program memory area by software
  - Number of segments

Product name	Flash memory		SRAM
	Program area	Data area	
ML630Q464	64KB (16K × 32bit)	2KB (0.5K × 32bit)	8KB (2K × 32bit)
ML630Q466	128KB (32K × 32bit)	2KB (0.5K × 32bit)	16KB (4K × 32bit)

- Interrupt controller (NVIC)
  - 1 non-maskable interrupt sources (Internal source: 1)
  - 31 maskable interrupt sources (Internal sources: 30, External sources: 1)
  - Priority level (4-level) can be set for each interrupt

- DMA controller (DMAC)
  - 2 channels
  - Enable to allocate multiple DMA transfer request sources for each channel.
  - Channel priority: fixed mode/round robin mode
  - DMA transfer mode: cycle steal mode/burst mode
  - DMA request type: software requests/hardware requests
  - Maximum transfer count: 65,536
  - Data transfer size: 8 bits/16 bits/32 bits
  - Transfer request source: SSIOF, UART, UARTF, I2CF, RC-ADC, SA-ADC

- Time base counter (TBC)
  – Low-speed time base counter × 1 channel

- 1 kHz Timer
  – 10 Hz / 1 Hz interrupt function

- Timers (TMR)
  – 8 bit × 8 channels
    (Timer0-7: 16bit × 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
  – Selection of one shot timer mode is possible
  – External clock can be selected as timer clock.

- Function Timers (FTM)
  – 16bit × 4 channels
  – Equipped with the timer/capture/PWM functions using a 16bit counter
  – An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3ϕ)
  – 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input selectable as timer clock
  – Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Real Time Clock (RTC)
  – 1 channels (99 years calendar, alarm, revision of the clock)

- Watchdog timer (WDT)
  – Non-maskable interrupt and reset
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Synchronous serial port (SSIOF/ SSIO)
  – without FIFOs (SSIO) : 1 channel
  – with 16-byte transmits and receives FIFOs (SSIOF) : 1 channel
  – Master/slave are selectable
  – LSB first/MSB first are selectable
  – Clock polarity (data out at rising edge and data in at falling edge/data out at falling edge and data in at rising edge) selectable
  – 8bit length/16bit length are selectable
  – Initial clock level (High start/Low start) selectable
  – supports slave-select signal (only SSIOF)

- UART (UARTF/ UART)
  – without FIFOs (UART) : 1channel
  – with 16-byte transmits and receives FIFOs (UARTF): 1channel
  – Full duplex buffer system
  – Communication speed: Settable within the range of 2400bps to 115200bps.
  – Programmable interface (data length, parity, stop bits are selectable)

- I^2C bus interface (I^2CF/ I^2C)
  – without FIFOs(I^2C) :1 channel
  – with 16-byte transmits and receives FIFOs(I^2CF): 1 channel
  – Master/Slave function (only I^2CF)
  – Fast mode (400 kHz), standard mode (100 kHz)

- USB full-speed device
  - Compliant with Universal Serial Bus (USB)
  - Full speed (12 Mbps) 1 port.
  - End points: 5 or 6
  - Supports all data transfer types (control transfer, bulk transfer, interrupt transfer, isochronous transfer).
  - Built-in SOF generation and CRC5/16 generation functions
  - Access size to data transfer FIFOs: 8 bits/16 bits/32 bits

- General-purpose ports (PORT)
  - Input/output port × 38 channels (including secondary or tertiary or quaternary or quinary functions).
    (ML630Q464 and ML630Q466: including LCD com/seg ports (each 20 ports))

- RC oscillation type A/D converter (RC-ADC)
  - Time division × 2 channels
  - Starting by trigger of Timer/FTM function.
  - 24 bit counter

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2 channels
  - Common mode input voltage: 0.2V to V_{DD} - 0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection are selectable

- Voltage Level Supervisor (VLS)
  - Threshold voltages: One of 64 levels
  - Acuraccy: ±3%
  - Interrupt or Reset generation are selectable
  - Voltage measurement with voltage input pin or V_{DD} pin

- Low Level Detector(LLD)
  - Judgement Voltage: 1.8V±0.2V
  - Usable as low level detection reset

- LCD driver
  - Maximun 400 dots (50 segment x 8 common)
  - 1/1 to 1/8 duty
  - 1/2 or 1/3 bias(built-in bias generation circuit)
  - Frame frequency selectable
  - Bias voltage multiplying clock selectable(5 types)
  - Contrast adjustment(32steps)
  - 4 operating mode: LCD drive stop, LCD display, all LCDs on, all LCDs off
  - Programmable display allocation function

- Random number generator (RANDOM)
  - Generates 8-bit random numbers

- AES
  - 128-bit Common key
  - Supports key sizes of 128, 192, and 256 bits
  - Supports ECB, CBC, and CTR modes

- Reset
  - Reset by the RESET_N pin input
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by threshold detection in Voltage Level Supervisor(VLS)
  - Reset by low level detection in Low Level Detector(LLD)
  - Reset by the low-speed crystal oscillation stop detection
  - Reset by SYSRESETREQ of ARM®Cortex®M0+ (software reset)

- Clock
  - Low-speed clock:
    - Crystal oscillation (32.768 kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - PLL (24 MHz) generated from Crystal oscillation (32.768 kHz)
    - Built-in RC oscillation (16MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states.
  - ULTRA-DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states, at V_{DD}>2.5V.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature (ambient) : -40°C to +85°C
  - Operating voltage: V_{DD} = 1.8V to 3.6V

- Supply current (Typ)
  - High-speed operation (24 MHz) : 250uA/MHz
  - sleepdeep mode : 0.80uA

- Package and shipping form
  - 100-pin plastic TQFP
    - Tray
      ML630Q464-xxxTBZWAX
      ML630Q466-xxxTBZWAX

1.2. Configuration of Functional Blocks

1.2.1. Block Diagram of ML630Q464/Q466

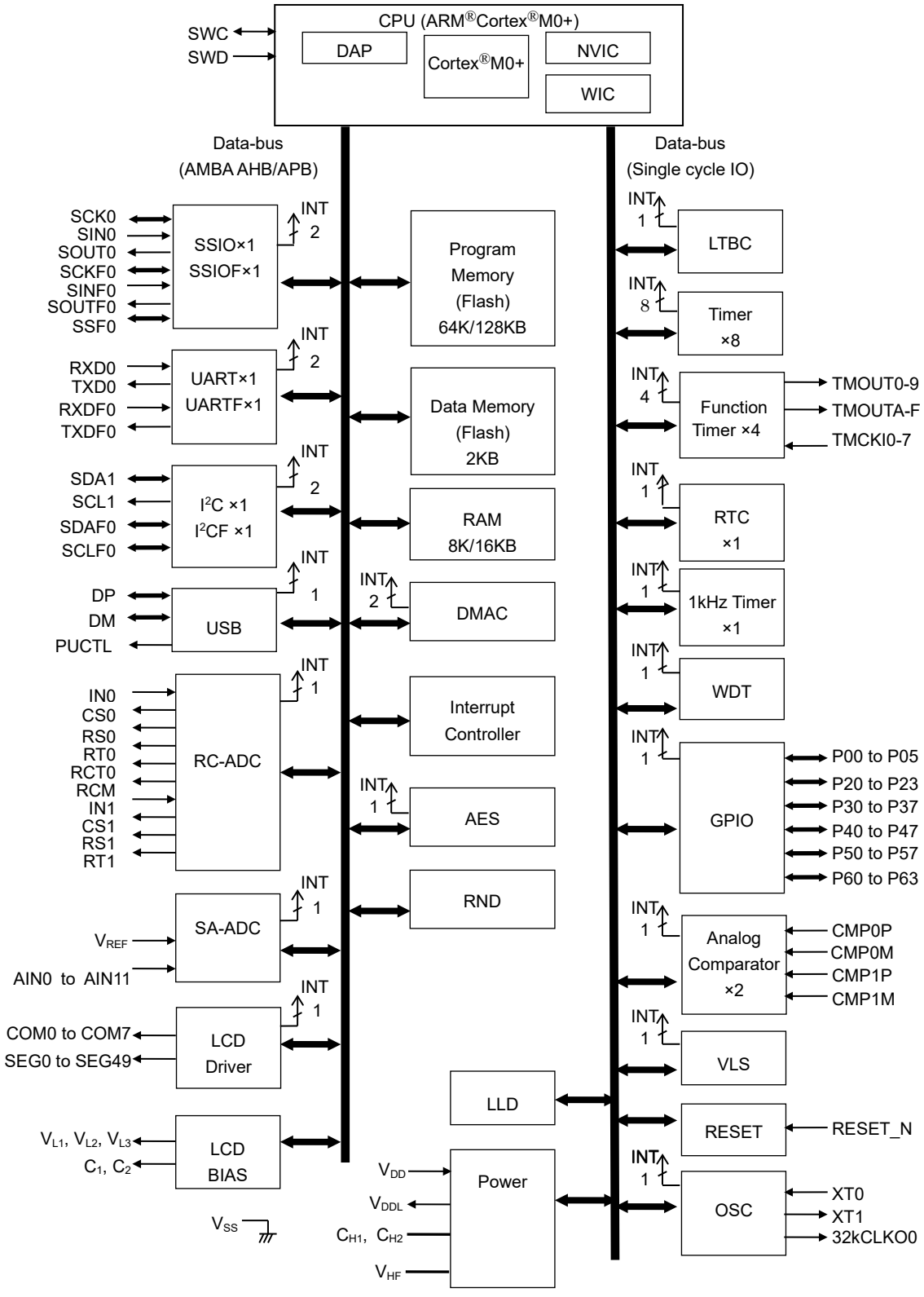


Figure 1-1 Block Diagram of ML630Q464/Q466

1.3. Pins

1.3.1. Pin Layout

1.3.1.1. Pin Layout of ML630Q464/Q466 TQFP Package

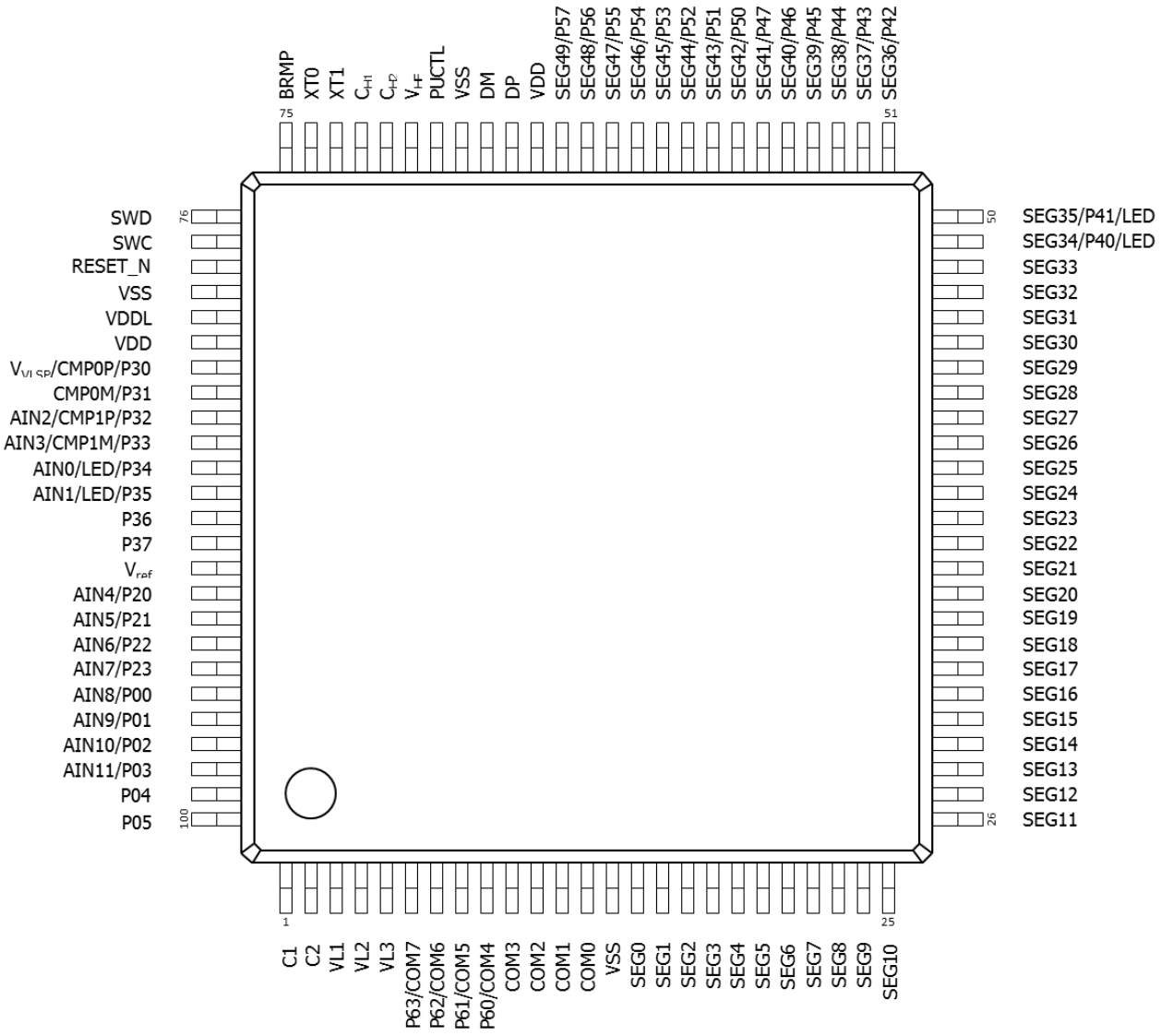


Figure 1-2 Pin Layout of ML630Q464/Q466

1.3.2. List of Pins

1.3.2.1. List of Pins of ML630Q464/Q466

PIN No.	.Reset State	Primary Function		Secondary Function		Tertiary Function		Quaternary Function		Quinary Function	
		Pin name	I/O	Pin name	I/O	pin name	I/O	pin name	I/O	pin name	I/O
14 68 79	–	V_{SS}	–	–	–	–	–	–	–	–	–
65 81	–	V_{DD}	–	–	–	–	–	–	–	–	–
80	–	V_{DDL}	–	–	–	–	–	–	–	–	–
70	–	V_{HF}	–	–	–	–	–	–	–	–	–
90	–	V_{REF}	–	–	–	–	–	–	–	–	–
74	–	XT0	–	–	–	–	–	–	–	–	–
73	–	XT1	–	–	–	–	–	–	–	–	–
78	Pull-up Input	RESET_N	I	–	–	–	–	–	–	–	–
77	Pull-up Input	SWC	I	–	–	–	–	–	–	–	–
76	Pull-up Input	SWD	I/O	–	–	–	–	–	–	–	–
75	Pull-down Input	BRMP	I	–	–	–	–	–	–	–	–
95	Hi-Z output	P00/ EXI00/ AIN8	I/O	IN0	I	SOUT0	O	RXDF0	I	–	–
96	Hi-Z output	P01/ EXI01/ AIN9	I/O	CS0	O	SIN0	I	TXDF0	O	–	–
97	Hi-Z output	P02/ EXI02/ AIN10	I/O	RCT0	O	SCK0	I/O	TMOUT0	O	–	–
98	Hi-Z output	P03/ EXI03/ AIN11	I/O	RS0	O	–	–	TMOUT1	O	–	–
99	Hi-Z output	P04/ EXI04	I/O	RT0	O	–	–	–	–	–	–
100	Hi-Z output	P05/ EXI05	I/O	RCM	O	–	–	–	–	–	–
91	Hi-Z output	P20/ EXI20/ AIN4	I/O	IN1	I	SOUTF0	O	–	–	–	–
92	Hi-Z output	P21/ EXI21/ AIN5	I/O	CS1	O	SINF0	I	–	–	–	–
93	Hi-Z output	P22/ EXI22/ AIN6	I/O	RS1	O	SCKF0	I/O	TMOUT2	O	–	–
94	Hi-Z output	P23/ EXI23/ AIN7	I/O	RT1	O	SSF0	I/O	TMOUT3	O	–	–
82	Hi-Z output	P30/ EXI30/ CMP0P V_{VLSP}	I/O	SDAF0	I/O	SOUT0	O	–	–	–	–
83	Hi-Z output	P31/ EXI31/ CMP0M	I/O	SCLF0	I/O	SIN0	I	–	–	–	–
84	Hi-Z output	P32/ EXI32/ CMP1P/ AIN2	I/O	RXDF0	I	SCK0	I/O	TMOUT4	O	–	–
85	Hi-Z output	P33/ EXI33/ CMP1M/ AIN3	I/O	TXDF0	O	32kCLKO	O	TMOUT5	O	–	–
86	Hi-Z output	P34/ EXI34/ AIN0 LED	I/O	SDA1	I/O	SOUTF0	O	–	–	–	–
87	Hi-Z output	P35/ EXI35/ AIN1 LED	I/O	SCL1	O	SINF0	I	–	–	–	–
88	Hi-Z output	P36/ EXI36/ TMCKI4	I/O	RXD0	I	SCKF0	I/O	TMOUT6	O	–	–
89	Hi-Z output	P37/ EXI37/ TMCKI5	I/O	TXD0	O	SSF0	I/O	TMOUT7	O	–	–
13 to 10	Low Level Output	COM0 to COM3	O	–	–	–	–	–	–	–	–
9	Hi-Z output	P60/ EXI60	I/O	COM4	O	–	–	–	–	–	–
8	Hi-Z output	P61/ EXI61	I/O	COM5	O	–	–	–	–	–	–

PIN No.	.Reset State	Primary Function		Secondary Function		Tertiary Function		Quaternary Function		Quinary Function	
		Pin name	I/O	Pin name	I/O	pin name	I/O	pin name	I/O	pin name	I/O
7	Hi-Z output	P62/ EXI62	I/O	COM6	O	–	–	–	–	–	–
6	Hi-Z output	P63/ EXI63	I/O	COM7	O	–	–	–	–	–	–
15 to 48	Low Level Output	SEG0 to SEG33	O	–	–	–	–	–	–	–	–
49	Hi-Z output	P40/ EXI40/ LED	I/O	SDAF0	I/O	SOUT0	O	–	–	SEG34	O
50	Hi-Z output	P41/ EXI41/ LED	I/O	SCLF0	I/O	SIN0	I	–	–	SEG35	O
51	Hi-Z output	P42/ EXI42/ TMCKI0	I/O	RXDF0	I	SCK0	I/O	TMOUT8	O	SEG36	O
52	Hi-Z output	P43/ EXI43/ TMCKI1	I/O	TXDF0	O	32kCLKO	O	TMOUT9	O	SEG37	O
53	Hi-Z output	P44/ EXI44	I/O	SDA1	I/O	SOUTF0	O	–	–	SEG38	O
54	Hi-Z output	P45/ EXI45	I/O	SCL1	O	SINF0	I	–	–	SEG39	O
55	Hi-Z output	P46/ EXI46/ TMCKI2	I/O	RXD0	I	SCKF0	I/O	TMOUTA	O	SEG40	O
56	Hi-Z output	P47/ EXI47/ TMCKI3	I/O	TXD0	O	SSF0	I/O	TMOUTB	O	SEG41	O
57	Hi-Z output	P50/ EXI50	I/O	SDAF0	I/O	SOUT0	O	–	–	SEG42	O
58	Hi-Z output	P51/ EXI51	I/O	SCLF0	I/O	SIN0	I	–	–	SEG43	O
59	Hi-Z output	P52/ EXI52	I/O	RXDF0	I	SCK0	I/O	TMOUTC	O	SEG44	O
60	Hi-Z output	P53/ EXI53	I/O	TXDF0	O	32kCLKO	O	TMOUTD	O	SEG45	O
61	Hi-Z output	P54/ EXI54	I/O	SDA1	I/O	SOUTF0	O	–	–	SEG46	O
62	Hi-Z output	P55/ EXI55	I/O	SCL1	O	SINF0	I	–	–	SEG47	O
63	Hi-Z output	P56/ EXI56/ TMCKI6	I/O	RXD0	I	SCKF0	I/O	TMOUTE	O	SEG48	O
64	Hi-Z output	P57/ EXI57/ TMCKI7	I/O	TXD0	O	SSF0	I/O	TMOUTF	O	SEG49	O
66	Hi-Z output	DP	I/O	–	–	–	–	–	–	–	–
67	Hi-Z output	DM	I/O	–	–	–	–	–	–	–	–
69	Low output	PUCTL	O	–	–	–	–	–	–	–	–
3	–	V_{L1}	–	–	–	–	–	–	–	–	–
4	–	V_{L2}	–	–	–	–	–	–	–	–	–
5	–	V_{L3}	–	–	–	–	–	–	–	–	–
1	–	C_1	–	–	–	–	–	–	–	–	–
2	–	C_2	–	–	–	–	–	–	–	–	–
71	–	C_{H1}	–	–	–	–	–	–	–	–	–
72	–	C_{H2}	–	–	–	–	–	–	–	–	–

1.3.3. Description of Pins

In the table below indicates the functional pin description.
The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.
(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quaternary function, 5th:quinary function)

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
System					
RESET_N	I	Reset input pin. When this pin is set to an "L" level, system reset mode is set and the internal section is initialized. When this pin is set to an "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	RESET_N	–	L
BRMP	I	Remapping control input (for firmware update) Based on the BRMP pin setting at the time of the reset release, Bank0 is remapped.	BRMP	–	H
XT0	I	Crystal connection pin for low-speed clock.	XT0	–	–
XT1	O	Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	XT1	–	–
32kCLKO	O	Low-speed clock output pin	P33,P43,P53	3rd	
General-purpose input/output port					
P00-P05	I/O	General-purpose input/output port.	P00-P05	1st	–
P20-P23	I/O	General-purpose input/output port.	P20-P23	1st	–
P30-P37	I/O	General-purpose input/output port.	P30-P37	1st	–
P40-P47	I/O	General-purpose input/output port.	P40-P47	1st	–
P50-P57	I/O	General-purpose input/output port.	P50-P57	1st	–
P60-P63	I/O	General-purpose input/output port.	P60-P63	1st	–
External interrupt					
EXI00-05 EXI20-23 EXI30-37 EXI40-47 EXI50-57 EXI60-63	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software.	P00-P05 P20-P23 P30-P37 P40-P47 P50-P57 P60-P63	1st	H/L
LED					
LED	O	N-channel open drain output pins to drive LED.	P34,P35,P40,P41	1st	–
UART					
TXD0	O	UART data output pin.	P37,P47,P57	2nd	–
RXD0	I	UART data input pin.	P36,P46,P56	2nd	–
TXDF0	O	UARTF with FIFO data output pin.	P01,P33,P43,P53	2nd	–
RXDF0	I	UARTF with FIFO data input pin.	P00,P32,P42,P52	2nd	–
I^2C bus interface					
SDA1	I/O	I2C1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P34,P44,P54	2nd	–
SCL1	O	I2C1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P35,P45,P55	2nd	–
SDAF0	I/O	I2CF0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P30,P40,P50	2nd	–
SCLF0	I/O	I2CF0 clock input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P31,P41,P51	2nd	–

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
Synchronous serial					
SCK0	I/O	Synchronous serial (SSIO) clock input/output pin.	P02,P32,P42,P52	3rd	–
SIN0	I	Synchronous serial (SSIO) data input pin.	P01,P31,P41,P51	3rd	–
SOUT0	O	Synchronous serial (SSIO) data output pin.	P00,P30,P40,P50	3rd	–
SCKF0	I/O	Synchronous serial with FIFO (SSIOF) clock input/output pin.	P22,P36,P46,P56	3rd	–
SINF0	I	Synchronous serial with FIFO (SSIOF) data input pin.	P21,P35,P45,P55	3rd	–
SOUTF0	O	Synchronous serial with FIFO (SSIOF) data output pin.	P20,P34,P44,P54	3rd	–
SSF0	I/O	Synchronous serial with FIFO (SSIOF) select input/output pin.	P23,P37,P47,P57	3rd	L
FTM					
TMOUT0-9 TMOUTA-F	O	FTM output pin.	P02,P03,P22,P23 P32,P33,P36,P37 P42,P43,P46,P47 P52,P53,P56,P57	4th	–
TMCKI0-7	I	External clock input pin for Timer	P42,P43,P46,P47 P36,P37,P56,P57	1st	–
RC oscillation type A/D converter					
IN0	I	Oscillation input pin of Channel 0.	P00	2nd	–
CS0	O	Reference capacitor connection pin of Channel 0.	P01	2nd	–
RS0	O	Reference resistor connection pin of Channel 0.	P03	2nd	–
RT0	O	Resistor sensor connection pin for measurement of Channel 0.	P04	2nd	–
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement.	P02	2nd	–
RCM	O	RC oscillation monitor pin.	P05	2nd	–
IN1	I	Oscillation input pin of Channel 1.	P20	2nd	–
CS1	O	Reference capacitor connection pin of Channel 1.	P21	2nd	–
RS1	O	Reference resistor connection pin of Channel 1.	P22	2nd	–
RT1	O	Resistor sensor connection pin for measurement of Channel 1.	P23	2nd	–
Successive approximation type A/D converter					
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	V_{REF}	–	–
AIN0-11	I	Analog input for successive approximation type A/D converter.	(AIN0-3) P32-35, (AIN4-7) P20-23, (AIN8-11) P00-03	1st	–
Analog comparator					
CMP0P	I	Comparator0 Non-inverted input pin.	P30	1st	–
CMP0M	I	Comparator0 Inverted input pin.	P31	1st	–
CMP1P	I	Comparator1 Non-inverted input pin.	P32	1st	–
CMP1M	I	Comparator1 Inverted input pin.	P33	1st	–
USB FS Device					
DP	I	USB Device D+ pin.	DP	–	–
DM	I	USB Device D- pin.	DM	–	–
PUCTL	O	USB Device pull up control pin	PUCTL	–	–

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
For testing					
SWC	I	Debugger clock input pin.	SWC	–	–
SWD	I/O	Debugger data input/output pin.	SWD	–	–
Power supply					
V_{SS}	–	Negative power supply pin.	V_{SS}	–	–
V_{DD}	–	Positive power supply pin.	V_{DD}	–	–
V_{DDL}	–	Positive power supply pin (internally generated) for internal logic. Capacitors $C_{L\ is}$ connected between this pin and V_{SS}.	V_{DDL}	–	–
V_{HF}	–	Positive power supply pin (internally generated) for built-in halver circuit. Capacitor C_{VH} is connected between this pin and V_{SS}.	V_{HF}	–	–
C_{H1} – C_{H2}	–	Capacitor pins of built-in halver circuit	C_{H1} – C_{H2}	–	–
LCD driver					
COM0 – COM3	–	Common pins of LCD driver	COM0 – COM3	1st	–
COM4 – COM7	–	Common pins of LCD driver	P60-P63	2nd	–
SEG0 – SEG33	–	Segment pins of LCD driver	SEG0 – SEG33	1st	–
SEG34 – SEG49	–	Segment pins of LCD driver	P40-P47 P50-P57	5th	–
C_1 – C_2	–	Capacitor pins of built-in generation bias circuit	C_1 – C_2	–	–
V_{L1} – V_{L3}	–	Reference voltage input pins of built-in bias generation circuit	V_{L1} – V_{L3}	–	–

1.3.4. Termination of Unused Pins

Table 1-3 shows methods of terminating the unused pins.

Table 1-3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	Connect to V_{DD}
BRMP	Connect to V_{SS}
SWC	Connect a pull-up resistor.
SWD	Connect a pull-up resistor.
V_{REF}	Connect to V_{DD}
P00 to P05	open
P20 to P23	open
P30 to P37	open
P40 to P47	open
P50 to P57	open
P60 to P63	open
COM0 to COM3	open
SEG0 to SEG33	open
DP, DM, PUCTL	open
V_{L1}, V_{L2}, V_{L3}	open
C_1, C_2	open

[Note]
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

Chapter 2

CPU

2. CPU

2.1. Overview

A RISC processor manufactured by ARM.
It is a 32-bit processor for small size and low power consumption applications and has a 3-stage pipeline configuration. It implements the ARMv6-M architecture, and operates with 16-bit Thumb® instructions and Thumb®-2 instructions.
For details, see " Cortex™-M0+ Technical Reference Manual".

2.1.1. Features

- Multiplier can process 32 bit × 32 bit in one cycle (holding the lower 32 bits of the operation result).
- Serial wire debug port
- Little-Endian
- Built-in debug component with four break points and two watch points
- Wakeup from any interrupt is possible.
- WFI (Wait for Interrupts) supported
- WFE (Wait for Events) supported
- SysTick not supported

2.2. Description of Registers

2.2.1. List of Registers

Address	Name	Symbol	R/W	Size [bits]	Initial value
0xE000_ED00	CPUID register	CPUID	R	32	0x410C_C200
0xE000_ED04	Interrupt control and state register	ICSR	R/W	32	0x0000_0000
0xE000_ED0C	Application interrupt and reset control register	AIRCR	R/W	32	0xFA05_0000
0xE000_ED10	System control register	SCR	R/W	32	0x0000_0000
0xE000_ED14	Configuration and control register	CCR	R	32	0x0000_0208
0xE000_ED1C	System handler priority register 2	SHPR2	R/W	32	0x0000_0000
0xE000_ED20	System handler priority register 3	SHPR3	R/W	32	0x0000_0000

For details of the register, see "ARMv6-M Architecture Reference Manual".

Chapter 3

Memory Space

3. Memory Space

3.1. General Description

In ML630Q464/Q466, various memories and registers are located in a 4 GB memory space, which is partitioned into 32 banks of 128 MB each.

3.2. Memory Map

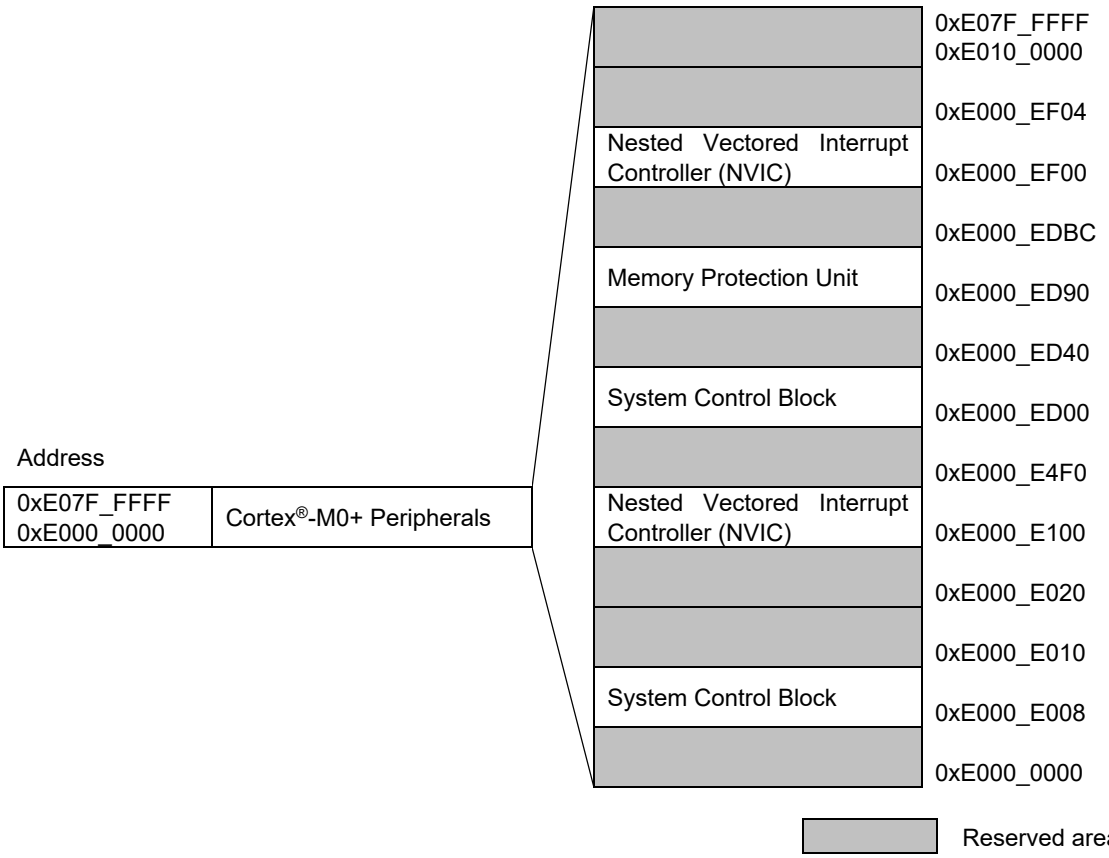
Figure 3-1 shows the memory map of ML630Q464/Q466.

Bank	4GB	Address	Memory space	
31		0xF800_0000		
30		0xF003_0000		
		0xF001_0000		
		0xF000_0000	ROM Table	
29		0xE800_0000		
28		0xE080_0000		
		0xE000_0000	Cortex™-M0+ Peripherals	See Figure 3-1 (2)
27		0xD800_0000		
26		0xD000_0000		
25		0xC800_0000		
24	3GB	0xC000_0000		
23		0xB800_0000		
22		0xB000_0000		
21		0xA800_0000		
20		0xA000_0000		
19		0x9800_0000		
18		0x9000_0000		
17		0x8800_0000		
16	2GB	0x8000_0000		
15		0x7800_0000		
14		0x7000_0000		
13		0x6800_0000		
12		0x6000_0000		
11		0x5C00_0000	Single-cycle I/O	See Figure 3-1 (3)
		0x5800_0000		
10		0x5000_0000		
9		0x4800_0000		
8	1GB	0x4000_0000	AHB/APB I/O	See Figure 3-1 (4)
7		0x3800_0000		
6		0x3000_0000		
5		0x2800_0000		
4		0x2000_4000		
		0x2000_2000	Work RAM (8KB) *2	
		0x2000_0000	Work RAM (8KB)	
3		0x1800_0800		
		0x1800_0000	Data Flash ROM(2KB)	
2		0x1002_0000		
		0x1001_0000	Program Flash ROM(64KB) *2	
		0x1000_0000	Program Flash ROM(64KB)	
1		0x0800_0000		
0	0GB	0x0000_0000	Remappable space	

: Reserved area*1

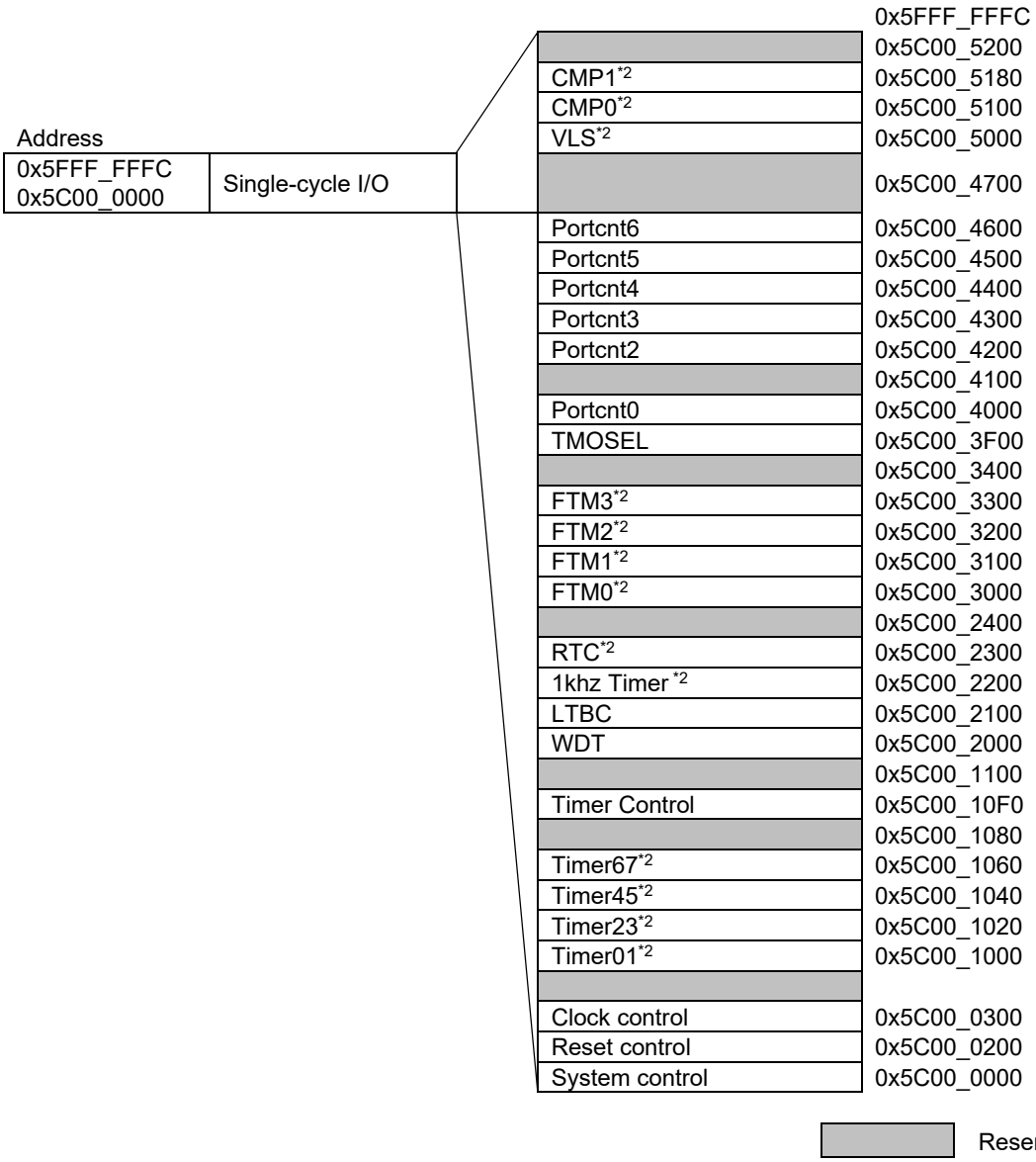
*1: Accessing any of reserved areas is prohibited. Proper operation cannot be guaranteed if accessed.
*2: Only ML630Q466.

Figure 3-1 (1) ML630Q464/Q466 Memory Map



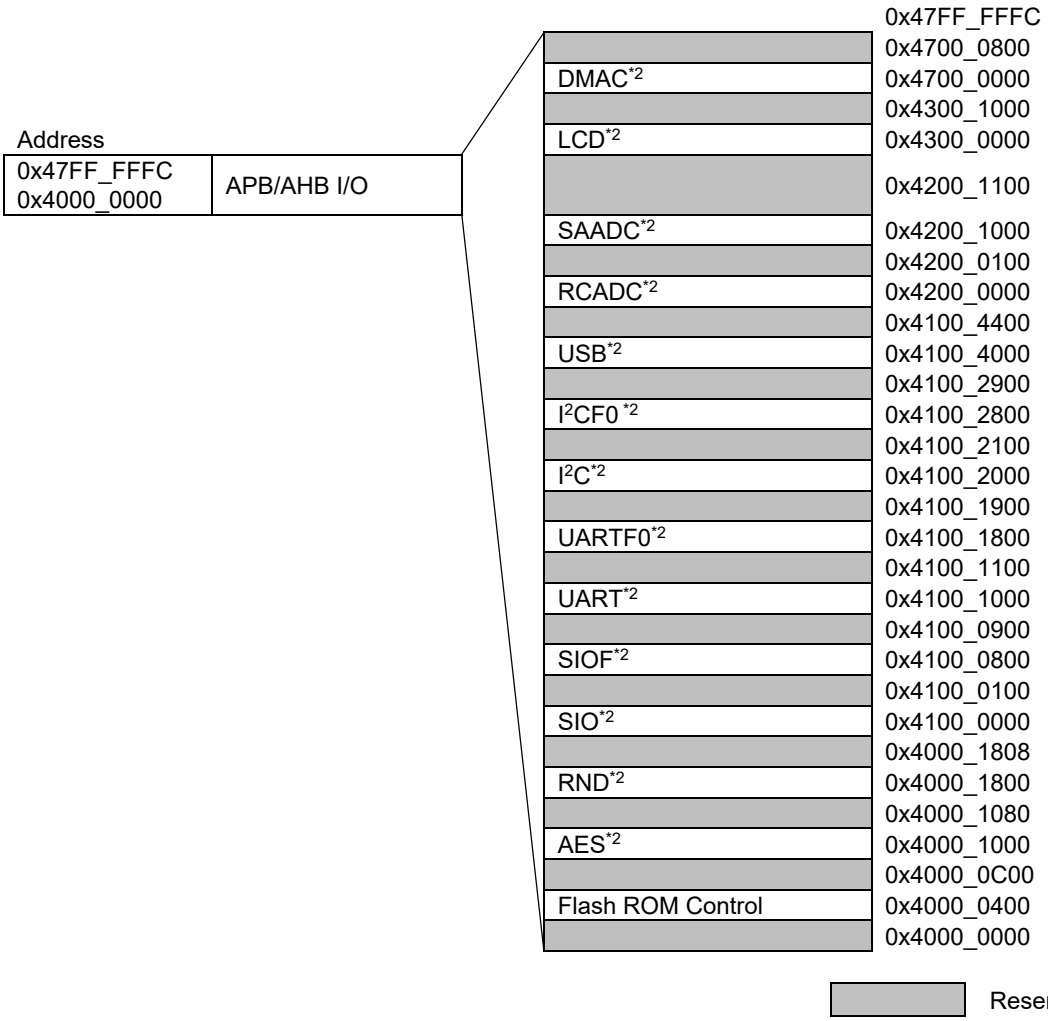
*1: Accessing any of reserved areas is prohibited. Proper operation cannot be guaranteed if accessed.

Figure 3-2 (2) Cortex®-M0+ Peripherals Area Memory Map



*1: Accessing any of reserved areas is prohibited. Proper operation cannot be guaranteed if accessed.
*2: During individual block stop state, write data is ignored and read data is undefined. For details of individual block stop state, see Chapter 5.

Figure 3-3 (3) Single Cycle I/O Area Memory Map



*1: Accessing any of reserved areas is prohibited. Proper operation cannot be guaranteed if accessed.
*2: During individual block stop state, write data is ignored and read data is undefined. For details of individual block stop state, see Chapter 5.

Figure 3-4 (4) APB/AHB I/O Area Memory Map

3.3. Internal Memory

3.3.1. Internal Flash ROM

Table 3-1 shows the address range of the Flash ROM of Bank2 and Bank3.

Table 3-1 Address Range of Bank2 and Bank3 Memory

Product	Program Area	Address range
ML630Q464	64 KB	0x1000_0000 to 0x1000_FFFF *1
ML630Q466	128 KB	0x1000_0000 to 0x1001_FFFF *1

Product	Data Area	Address range
ML630Q464/ Q466	2 KB	0x1800_0000 to 0x1800_07FF *1

*1: Accessing an address out of this address range in the same bank is prohibited. Proper operation cannot be guaranteed if accessed.

3.3.2. Work RAM

Table 3-2 shows the address range of the work RAM of Bank4.

Table 3-2 Bank4 Address Range

Product	Work RAM	Address range
ML630Q464	8 KB	0x2000_0000 to 0x2000_1FFF *1
ML630Q466	16 KB	0x2000_0000 to 0x2000_3FFF *1

*1: Accessing an address out of this address range in the same bank is prohibited. Proper operation cannot be guaranteed if accessed.

3.4. Memory Controller Function

3.4.1 List of Registers

Address	Name	Symbol	R/W	Size [bits]	Initial value
0x5C00_0010	Remapping control register	REMAPCON	R/W	32	0x0000_0000
0x5C00_0014	Remapping base address register	REMAPBASE	R/W	32	0x100x_F000

3.4.2 Remapping Control Register (REMAPCON)

Address: 0x5C00_0010
Access: R/W
Access size: 32 Bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	REMAP_EN	REMAP[3:0]			
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. "0" is read when reading. Write a "0" for write.

[Description of Register]
This is a special function register (SFR) used to set remapping.

[Description of Each Bit]
REMAP[3:0] (bits 0-3)
REMAP_EN (bit 4)

REMAP_EN	REMAP [3:0]	Description
0	xxxx	Based on the BRMP pin that is set after the reset release, the following area is remapped to Bank0. H: (Q464) The area of 0x1000_F000 of Flash ROM is remapped to Bank0. (Q466) The area of 0x1001_F000 of Flash ROM is remapped to Bank0. L: The area of address 0 of Flash ROM is remapped to Bank0.
1	0000	The Program Flash ROM is remapped to Bank0.
1	xxx1	The internal RAM is remapped to Bank0.
1	x100	The area starting at the address set by the REMAP_BASE register is remapped to Bank0.
1	Other than above	Setting prohibited

(x: Don't care)

[Notes on Setting]

1. Operation cannot be guaranteed if remapping is performed when the remapping processing program (instruction to set the remapping control register) is placed in Bank0. Be sure to place the remapping processing program in a Bank other than Bank0 when performing the remapping.

2. Remapping of Bank0 is performed as soon as this register is set.

3. This register is not initialized by software reset.

3.4.3 Remapping Base Address Register (REMAPBASE)

Address: 0x5C00_0014
Access: R/W
Access size: 32 Bits
Initial value: 0x1000_F000 (Q464), 0x1001_F000 (Q466)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	REMAP_BASE[29:16]													
Access	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0/1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	REMAP_BASE[15:12]				–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	R/W	R/W	R/W	R/W	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. "0" is read when reading. Write "0" when writing.

[Description of Register]
This is a special function register (SFR) used to set the base address of remapping. It is enabled only when REMAP_EN = 1 and REMAP[2:0] = ”100” are set in the remapping control register.

[Description of Each Bit]

REMAP_BASE[29:12]

The 4-KB area starting at the address set by this register is assigned starting from address 0.
The value of bit 16 is “0” in the case of ML630Q464.
The value of bit 16 is “1” in the case of ML630Q466.

The starting address must be an address in the memory space.

ML630Q464
Flash ROM: 0x1000_0000 - 0x1000_FFFF
Work RAM: 0x2000_0000 - 0x2000_1FFF

ML630Q466
Flash ROM: 0x1000_0000 - 0x1001_FFFF
Work RAM: 0x2000_0000 - 0x2000_3FFF

* Area assigned to the remapping area is only 4 KB at the remapping by the remapping base address. If the space exceeding 4 KB is needed for re-writing the program memory area by software, for example, the program needs to jump to the area where the entity such as Flash ROM is placed (0x10000000 and after for Flash ROM) to be executed, except for the minimum necessary codes such as exception vectors.

[Notes on Setting]

1. This register is not initialized by software reset.

3.4.4 Boot/Remapping Function

It is possible to allocate the following devices to Bank0 after booting by setting REMAP[3:0] of the remapping control register. Table 3-3 shows the allocations of Bank0 during booting and remapping.
Operation cannot be guaranteed if remapping is performed when the remapping processing program (instruction to set the remapping control register) is placed in Bank0. Be sure to place the remapping processing program in a Bank other than Bank0 when performing the remapping.

Table 3-3 Bank0 Allocations during Booting and Remapping

Boot/ Remapping	BRMP	REMAP _EN	REMAP [3:0]	Device	Remarks
Boot	0	0	xxxx	Program Flash ROM	Start address: 0x1000_0000
	1			Program Flash ROM	Start address: 0x1001_F000 (Q466) 0x1000_F000 (Q464)
Remapping	x	0	xxxx	Not remapped	
		1	0000	Program Flash ROM	
			xxx1	Work RAM	
			x100	Work RAM/ Program Flash ROM	The device placed at the address set by the remapping base address responds.
			Other than above	Setting prohibited	

x: Don't care the data.

3.5 Access Response for Memory Space

• An access made to a bank that has been set as not allocated returns an error response (*). For specifications of the space in a bank exceeding the allocated memory size, see Section 3.3.

*: Operation at error response
• If an error response is returned for access from CPU, a hard fault exception is generated.

Chapter 4

Reset Function

4. Reset Function

4.1. Overview

This LSI has the 8 reset functions shown below. If any of these resets occur, this LSI enters system reset mode.

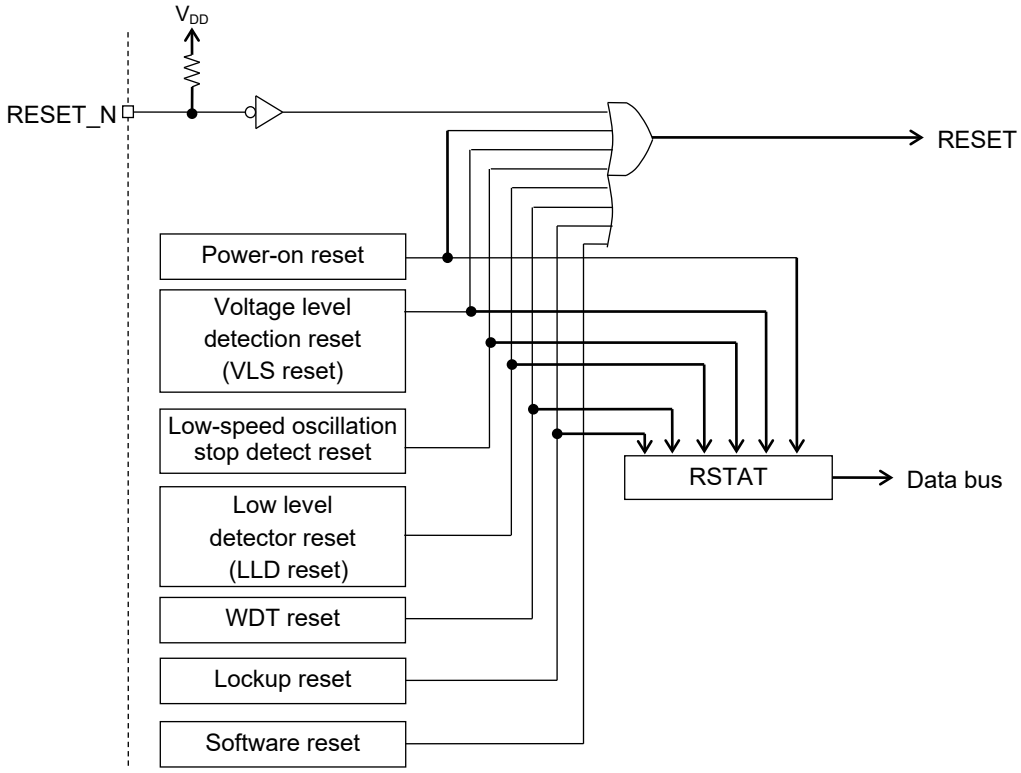
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd overflow of watchdog timer (WDT)
- Reset by Voltage Level Supervisor (VLS)
- Reset by Low Level Detector (LLD)
- Reset by the low-speed crystal oscillation stop detection
- Reset by Lockup of processor
- Software reset by the SYSRESETREQ bit

4.1.1. Features

- The RESET_N pin has an internal pull-up resistor
- 125 ms, 500ms, 2 sec, or 8 sec can be selected as the watchdog timer (WDT) overflow period when LSCLK=32.768 kHz)
- Built-in reset status register (RSTAT) indicating the reset generation causes

4.1.2. Configuration

Figure 4-1 shows the configuration of the reset generation circuit.



RSTAT:Reset status register

Figure 4-1 Configuration of Reset Generation Circuit

4.1.3. List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

4.2. Description of Registers

4.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_0200	Reset status register	RSTAT	R/W	32	Undefined
0x5C00_0204	LOCKUP reset setting register	LOCKUPEN	R/W	32	0x0000_0001

4.2.2. Reset Status Register (RSTAT)

Address: 0x5C000200
Access: R/W
Access size: 32 bit
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	LOCKUP	LLDR	VLSR	WDTR	XSTR	POR
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x

*) The initial value depends on the reset factor

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RSTAT is a special function register (SFR) that indicates the cause of a switch to the system reset mode.

At switch to the system reset mode, the bit for the reset cause is set to "1". RSTAT is not initialized during the system reset mode. When checking the reset cause using this function, clear each reset cause bit of RSTAT to "0" (not occurred) in advance.

[Description of Bits]

- **POR (bit 0)**
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not occurred
1	Power-on reset occurred

- **XSTR** (bit 1)
  The XSTR bit is a flag that indicates the occurrence of low-speed crystal oscillation stop detect reset. When low-speed crystal oscillation stops for the period specified by the low-speed crystal oscillation stop detection time (T_{STOP}) or more, this bit is set to "1". Also, the bit is undefined when the power is turned on.

XSTR	Description
0	Low-speed crystal oscillation stop detect reset not occurred
1	Low-speed crystal oscillation stop detect reset occurred

- **WDTR** (bit 2)
  The WDTR is a flag that indicates that the watchdog timer reset is occurred. This bit is set to "1" when the reset by overflow of the watchdog timer is generated. Also, the bit is undefined when the power is turned on.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

- **VLSR** (bit 3)
  The VLSR is a flag that indicates that the Voltage Level Supervisor reset is occurred. This bit is set to "1" when the reset by overflow of the Voltage Level Supervisor generated. Also, the bit is undefined when the power is turned on.

VLSR	Description
0	Voltage Level Supervisor reset not occurred
1	Voltage Level Supervisor reset occurred

- **LLDR** (bit 4)
  The LLDR is a flag that indicates that the Low Level Detector reset is occurred. This bit is set to "1" when the reset by overflow of the Low Level Detector is generated. Also, the bit is undefined when the power is turned on.

LLDR	Description
0	Low Level Detector reset not occurred
1	Low Level Detector reset occurred

- **LOCKUP** (bit 5)
  LOCKUP is a flag that a reset has occurred because the processor fell in the lockup state. This bit is set to "1" when a lockup reset occurs. This bit is set to "0" when the power is turned on. This register is enabled when the EN bit of the LOCKUPEN register is set to "1".

LOCKUP	Description
0	Lockup reset not occurred
1	Lockup reset occurred

[Note]
No flag is provided that indicates the occurrence of reset by the RESET_N pin or software reset.

4.2.3. LOCKUP reset setting register (LOCKUPEN)

Address: 0x5C000204
Access: R/W
Access size: 32 bit
Initial value: 0x00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
LOCKUPEN is a special function register (SFR) to enable/disable the LOCKUP reset.

[Description of Bits]
- **EN** (bit 0)
  Sets whether to enable/disable the LOCKUP reset. "1" enables the LOCKUP reset. This register is not initialized by a LOCKUP reset.

EN	Description
0	LOCKUP reset disabled
1	LOCKUP reset enabled (initial value)

4.3. Description of Operation

4.3.1. Cause of Reset

In addition to a reset by RESET_N pin and software reset by the reset control register, this LSI enters the system reset mode according to the state in the LSI.

- Reset by the RESET_N pin
  System reset occurs when "0" is input to RESET_N. The contents of reset status register(RSTAT) are not changed at system reset mode entered by the RESET_N pin.

- Reset by power-on detection
  System reset occurs when LSI is powered on. POR bit of reset status register(RSTAT) becomes "1" at system reset mode entered by Power-on detection.

- Reset by the overflow of watchdog timer (WDT)
  System reset occurs by the second WDT over flow.
  For the watchdog timer operation, see Chapter 14 "Watchdog Timer".
  WDTR bit of reset status register(RSTAT) is set to "1" at system reset occurred by WDT over flow.

- Reset by Voltage Level Supervisor (VLS)
  System reset occurs when power supply voltage falls under the specified voltage level.
  The reset by VLS is disabled initially. To enable it, set the VLSSEL0 bit of the voltage level supervisor mode register (VLSMOD) to "1".
  For operations of the VLS function, see Chapter 30 "Voltage Level Supervisor".
  VLSR bit of the reset status register(RSTAT) is set to "1" at system reset occurred by VLS.

- Reset by Low Level Detector (LLD)
  System reset occurs when the power supply voltage falls under the threshold(1.8V Typ) of Low Level Detector(LLD). The function of LLD function is disabled initially. To enable it, set the RLLD bit of the reset control register (RSTCON) to "0".
  LLDR bit of the reset status register(RSTAT) is set to "1" at system reset occurred by LLD.

- Reset by the low-speed crystal oscillation stop detection
  System reset occurs when the crystal oscillation stops for the period specified by the low-speed oscillation stop detection time (T_{STOP}) or longer. This function is disabled initially. This is also disabled when the low-speed crystal oscillation is not used. At the time of the shift to a system reset mode by the low-speed crystal oscillation stop detection, XSTR bit of the reset status register (RSTAT) is set to "1". For the reset function by low-speed crystal oscillation stop detection, refer to Chapter 6 "Clock Generation Circuit".

- Software reset by SYSRESETREQ
  System reset occurs by software.
  The contents of reset status register(RSTAT) are not changed at system reset mode entered by SYSRESETREQ.
  For details, refer to "Cortex™-M0+ Devices Generic User Guide".

- Reset by lockup of processor
  The reset occurs when the processor enters the lockup state. For details, refer to "Cortex™-M0+ Devices Generic User Guide"

4.3.2. Operation of System Reset Mode

System reset has the highest priority among all the processing and any other processing being executed up to then is cancelled.
In system reset mode, the following processing is performed.

(1) The power circuit is initialized.
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, SFRs of RTC are not initialized by except for the reset by RESET_N pin. See Appendix A "Registers" for the initial values of the SFRs.
(3) CPU is initialized.
- All the registers in CPU are initialized.

[Note]
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.

The following table shows the causes of switch to the system reset mode and the initialization state in the LSI.

Module \ Reset causes	RESET_N	POR	SYSRESETREQ	LOCKUP	LLD	VLS	WDT	XTSTOP
SFR	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized
CPU	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized	Initialized
Data memory	Not initialized	Not initialized	Not initialized	Not initialized	Not initialized	Not initialized	Not initialized	Not initialized
RTC	Initialized	Initialized	Not initialized	Not initialized	Not initialized	Not initialized	Not initialized	Not initialized
VLS enable*1	Initialized	Initialized	Initialized	Initialized	Initialized	Not initialized	Initialized	Initialized
LLD enable*2	Initialized	Initialized	Initialized	Initialized	Not initialized	Initialized	Initialized	Initialized

*1 See below for the initialization state at power-up and VLS reset assert.

Signal	At power up	VLS reset	Other than VLS reset
VLS enable (ENVLS bit of the VLSCON register)	Disabled	State before the reset held	Disabled
VLS clock enable (CVLS bit of CLKCON register)	Clock disabled	State before the reset held	Clock disabled
VLS reset enable (RVLS bit of RSTCON register)	Reset enabled	State before the reset held	Reset enabled

*2 See below for the initialization state at power-up and LLD reset assert.

Signal	At power up	LLD reset	Other than LLD reset
LLD reset enable (RLLD bit of RSTCON register)	Reset enabled	State before the reset held	Reset enabled

The ENVLS bit of the VLSCON register, the CVLS bit of the CLKCON register, the RVLS bit of the RSTCON register, and the RLLD bit of the RSTCON register select enable/disable of the respective function.
They are disabled at power-up, and hold the state before the reset only when a reset occurs by the respective cause.

Chapter 5

System Control Function

5. System Control Function

5.1. General Description

This LSI has five power management modes listed below to save the current consumption. These power management modes are set by the Cortex™-M0+ sleep mode and the standby control register (SBYCON).
It also has a block control function, which power downs unused peripheral functions (reset registers and stop clock supplies) to further reduce the current consumption.

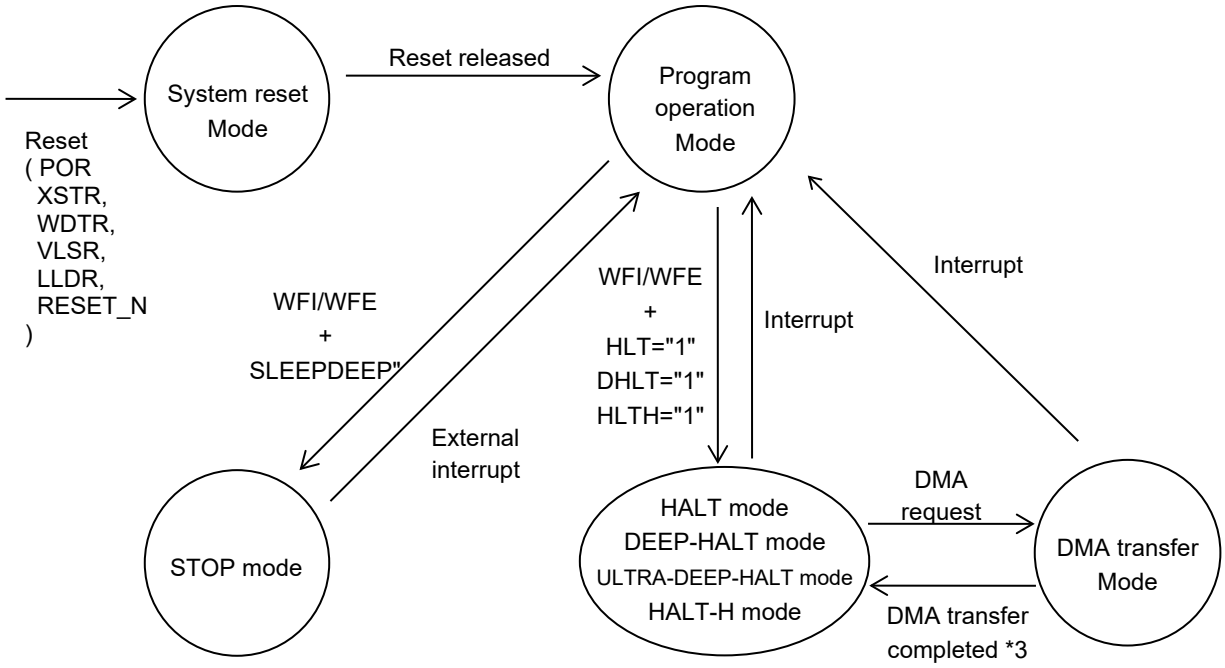
(1) HALT mode
(2) HALT-H mode
(3) DEEP-HALT mode
(4) ULTRA-DEEP-HALT mode
(5) STOP mode

5.1.1. Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- HALT-H mode, which stops the high-speed clock when the CPU operation using the high-speed clock
- DEEP-HALT mode, which is stopped the CPU operating and only LTBC, timers, LCD, VLS, and LLD can operate at lower power consumption
- ULTRA-DEEP-HALT mode, where the power consumption is even lower than the DEEP-HALT mode (only when VDD > 2.5 V)
- STOP mode, which both low-speed oscillation and high-speed oscillation stop.
- Block control function, which power downs the circuits of unused function blocks (reset registers and stop clock supplies)

5.1.2. Configuration

Figure 5-1 shows an operating state transition diagram.



*1: At reset, the LSI switches to the system reset mode from any mode.
*2: When switching to the DEEP-HALT/HALT-H mode with the internal PLL selected for the system clock, the LSI uses the low-speed clock at start-up in the DMA transfer mode.
*3: After DMA transfer, the LSI switches to the HALT/DEEP-HALT/ULTRA-DEEP-HALT/HALT-H mode after waiting for 8 cycles of the system clock.
*4: When switching from the DMA transfer mode, the interrupt has a priority over the DMA transfer completion.

Figure 5-1 Operating State Transition Diagram

5.2. Description of Registers

5.2.1. Register Configuration List

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_0000	Revision register	IDR	R	32	0x0630_46x0
0x5C00_0004	DMA request select register	DREQSEL	R/W	32	0x0000_0000
0x5C00_0008	BRMP control register	BRMPCON	R/W	32	0x0000_0001
0x5C00_0044	Standby control register	SBYCON	R/W	32	0x0000_0000
0x5C00_0048	Power management control register	PMCON	R/W	32	0x0000_0000
0x5C00_004C	Clock control register	CLKCON	R/W	32	0x0000_0000
0x5C00_0050	Reset control register	RSTCON	R/W	32	0xFFFF_EFFF

5.2.2. Revision Register (IDR)

Address: 0x5C00_0000
Access: R
Access size: 32 bit
Initial value: 0x0630_46xx

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	PID[27:12]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	PID[11:0]												PRV[3:0]			
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	1	0	0	0	1	1	0	0	1	x	0	x	x	x	x

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
IDR holds the 28-bit product ID and 4-bit revision.

[Description of Bits]

- **PRV[3:0]** (bit 3 to 0)
  PRV[3:0] is indicated the revision of this LSI.

- **PID[27:0]** (bit 31 to 4)
  PID[27:0] is indicated the product ID of this LSI.
  ML630Q464 : 0x0630_4640
  ML630Q466 : 0x0630_4660

5.2.3. DMA Request Select register (DREQSEL)

Address: 0x5C00_0004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	DREQ1SEL[3:0]				–*	–*	–*	–*	DREQ0SEL[3:0]			
Access	–	–	–	–	R/W	R/W	R/W	R/W	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
The DREQSEL is a register used to select the external request of DMAC.

[Description of Bits]

- **DREQ0SEL[3:0]** (bit 3 to 0)
  The DREQ0SEL bit is used to select the peripheral which uses ch0 at transferring external requests of DMAC. The following peripherals are selected by the DREQ0SEL setting:

DREQ0SEL[3:0]	Selected peripheral
0001	SSIOF (RX)
0010	SSIOF (TX)
0101	UART (RX)
0110	UART (TX)
0111	UARTF (RX)
1000	UARTF (TX)
1001	I2CF (RX)
1010	I2CF (TX)
1100	SA-ADC
1101	RC-ADC
Others	Not selected

- **DREQ1SEL[3:0]** (bit 11 to 8)
  The DREQ1SEL bit is used to select the peripheral which uses ch1 at transferring external requests of DMAC. The following peripherals are selected by the DREQ1SEL setting:

DREQ1SEL[3:0]	Selected peripheral
0001	SSIOF (RX)
0010	SSIOF (TX)
0101	UART (RX)
0110	UART (TX)
0111	UARTF (RX)
1000	UARTF (TX)
1001	I2CF (RX)
1010	I2CF (TX)
1100	SA-ADC
1101	RC-ADC
Others	Not selected

5.2.4. BRMP Control Register (BRMPCON)

Address: 0x5C00_0008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	PDEN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
The BRMPCON register is used to control the pull-down resistor of the BRMP pin.

[Description of Bits]

- **PDEN** (bit 0)
  The PDEN bit is used to set the pull-down resistor of the BRMP pin.

PDEN	Selected peripheral
0	Pull-down resistance disabled
1	Pull-down resistance enabled (initial value)

5.2.5. Standby Control Register (SBYCON)

Address: 0x5C00_0044
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	HLTH	DHLT	–*	HLT
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SBYCON is a special function register (SFR) to control the operation mode of MCU.

[Description of Bits]

- **HLT** (bit 0)
  The HLT bit is used for setting the HALT mode. When the HLT bit is set to "1", and the WFI/WFE instruction is executed, the LSI switches to the HALT mode.

- **DHLT** (bit 2)
  The DHLT bit is used for setting the DEEP-HALT mode. When the DHLT bit is set to "1", and the WFI/WFE instruction is executed, the LSI switches to the DEEP-HALT mode.
  When the LSI switches to the DEEP-HALT mode with the UDHON and UDHEN bits of the PMCON register set to "1", it switches to the ULTRA-DEEP-HALT mode with even lower current consumption.

- **HLTH** (bit 3)
  The HLTH bit is used for setting the HALT-H mode. When the HLTH bit is set to "1", and the WFI/WFE instruction is executed, the LSI switches to the HALT-H mode. Also, the high-speed clock automatically stops.
  It does not switch to the HALT-H mode when "1" is written to the HLTH bit at the low-speed system clock.

[Note]

- These plural bit should not be set to “1” at the same time.
- When switching to the DEEP-HALT or ULTRA-DEEP-HALT mode while using the crystal oscillation with the low-speed clock, confirm that the LOSCS bit of the frequency status register (FSTAT) is set to "0".
- It can switch to the STOP, HALT, HALT-H, DEEP-HALT, or ULTRA-DEEP-HALT mode if a valid interrupt occurs. It returns from such a mode when another interrupt occurs which has a higher interrupt level than the valid interrupt.
- When this register is 0x0000_0000, and the CPU is operated the instuction of WFI/WFE, only the CPU is shifted sleep mode.

5.2.6. Power Management Control Register (PMCON)

Address: 0x5C00_0048
Access: R/W
Access size: 32bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	LXTHVN	UDHON	UDHEN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
PMCON is a special function register (SFR) to control the power management of this LSI.

[Description of Bits]

- **UDHEN, UDHON** (bit 0, 1)
  If the DHLT bit of the SBYCON register is set to "1" by setting UDHEN and UDHON to "1" in the predetermined sequence when V_{DD} is 2.5 V or higher, the LSI switches to the ULTRA-DEEP-HALT mode. For the switch sequence, refer to 5.3.3.

- **LXTHVN** (bit 2)
  If LXTHVN is set to "1" in the predetermined sequence when VDD is 2.5 V or higher, the 32k crystal oscillation can be operated with the lower current consumption.
  For the switch sequence, refer to 5.3.3.

[Note]
Prohibition to set "1" in LXTHVN bit when VDD is less than 2.5V, or sets "1" in UDHEN and UDHON bit without or keeping a predetermined sequenc.

5.2.7. Clock Control Register (CLKCON)

Address: 0x5C00_004C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	CCMP1	CCMP0	CDMAC	–*	CVLS	CRTC	CLCD	CUSB	CRND	CAES	CI2CF0	CI2C1	CUAF0*	CUA0	CSIOF0	CSIO0
Access	R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	CTM1K	CRAD	CSAD	–*	CFTM3	CFTM2	CFTM1	CFTM0	CTM7	CTM6	CTM5	CTM4	CTM3	CTM2	CTM1	CTM0
Access	R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
CLKCON is a special function register (SFR) used to control the clock of each peripherals.

[Description of Bits]

- **CTM7-0** (bit 7 to 0)

The CTM7 to CTM0 bits are used to control the 8-bit timer 0 to 7 clocks.

CTM0	Description
0	Timer 0 clock stop (initial value)
1	Timer 0 clock supply

CTM1	Description
0	Timer 1 clock stop (initial value)
1	Timer 1 clock supply

CTM2	Description
0	Timer 2 clock stop (initial value)
1	Timer 2 clock supply

CTM3	Description
0	Timer 3 clock stop (initial value)
1	Timer 3 clock supply

CTM4	Description
0	Timer 4 clock stop (initial value)
1	Timer 4 clock supply

CTM5	Description
0	Timer 5 clock stop (initial value)
1	Timer 5 clock supply

CTM6	Description
0	Timer 6 clock stop (initial value)
1	Timer 6 clock supply

CTM7	Description
0	Timer 7 clock stop (initial value)
1	Timer 7 clock supply

[Note]
Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, or Timers 6 and 7 is shared the high-speed source oscillation clock (OSCLK) and the system clock (SYSCLK). If one clock of each combination is stopped, the high-speed source oscillation clock and the system clock are stopped for both timers. The low-speed clock (LSCLK) can be stopped separately.

- **CFTM3-0** (bit 11 to 8)

The CFTM3, CFTM2, CFTM1, and CFTM0 bits are used to control the clock of the function timer (FTM).

CFTM0	Description
0	Function timer 0 clock stop (initial value)
1	Function timer 0 clock supply

CFTM1	Description
0	Function timer 1 clock stop (initial value)
1	Function timer 1 clock supply

CFTM2	Description
0	Function timer 2 clock stop (initial value)
1	Function timer 2 clock supply

CFTM3	Description
0	Function timer 3 clock stop (initial value)
1	Function timer 3 clock supply

- **CSAD** (bit 13)

The CSAD bit is used to control the successive approximation type (SA type) A/D converter clock.

CSAD	Description
0	SA type A/D converter clock stop (initial value)
1	Successive approximation type A/D converter supply

- **CRAD** (bit 14)

The CRAD bit is used to control the RC oscillation type A/D converter clock.

CRAD	Description
0	RC oscillation type A/D converter clock stop (initial value)
1	RC oscillation type A/D converter supply

- **CTM1K** (bit 15)

The CTM1K bit is used to control 1 kHz timer clock.

CTM1K	Description
0	1 kHz timer clock stop (initial value)
1	1 kHz timer clock supply

- **CSIO0** (bit 16)

The CSIO0 bit is used to control the clock of the synchronous serial port.

CSIO0	Description
0	Synchronous serial port 0 clock stop (initial value)
1	Synchronous serial port 0 clock supply

- **CSIOF0** (bit 17)

The CSIOF0 bit is used to control the clock of the synchronous serial port with FIFO.

CSIOF0	Description
0	Synchronous serial port 0 with FIFO clock stop (initial value)
1	Synchronous serial port 0 with FIFO clock supply

- **CUA0** (bit 18)

The CUA0 bit is used to control the UART0 clock.

CUA0	Description
0	UART0 clock stop (initial value)
1	UART0 clock supply

- **CUAF0** (bit 19)

The CUAF0 bit is used to control the clock of UART with FIFO.

CUAF0	Description
0	UART with FIFO clock stop (initial value)
1	UART with FIFO clock supply

- **CI2C1** (bit 20)

The CI2C1 bit is used to control the clock of the I2C bus interface 1

CI2C1	Description
0	I2C bus interface 1 clock stop (initial value)
1	I2C bus interface 1 clock supply

- **CI2CF0** (bit 21)

The CI2CF0 bit is used to control the clock of the I2C bus interface 0 with FIFO.

CI2CF0	Description
0	I2C bus interface 0 with FIFO clock stop (initial value)
1	I2C bus interface 0 with FIFO clock supply

- **CAES** (bit 22)

The CAES bit is used to control the clock of AES.

CAES	Description
0	AES clock stop (initial value)
1	AES clock supply

- **CRNG** (bit 23)

The CRNG bit is used to control the clock of the random number generator.

CRNG	Description
0	Random number generator clock stop (initial value)
1	Random number generator clock supply

- **CUSB** (bit 24)

The CUSB bit is used to control the clock of the USB bus interface.

CUSB	Description
0	USB bus interface clock stop (initial value)
1	USB bus interface clock supply

- **CLCD** (bit 25)

The CLCD bit is used to control the clock of LCD driver.

CLCD	Description
0	LCD driver clock stop (initial value)
1	LCD driver clock supply

- **CRTC** (bit 26)

The CRTC bit is used to control the clock of the real time clock. This bit is initialized with the power-on reset or the reset by the RESET_N pin. It is not initialized with the other reset causes.

CRTC	Description
0	Real time clock stop (initial value)
1	Real time clock supply

- **CVLS** (bit 27)

The CVLS bit is used to control the clock of the power supply voltage detection circuit (VLS). This bit is not initialized by a VLS reset.

CVLS	Description
0	VLS clock stop (initial value)
1	VLS clock supply

- **CDMAC** (bit 29)

The CDMAC bit is used to control the clock of DMAC.

CDMAC	Description
0	DMAC clock stop (initial value)
1	DMAC clock supply

- **CCMP0** (bit 30)

The CCMP0 bit is used to control the clock of the analogue comparator 0.

CCMP0	Description
0	Analogue comparator 0 clock stop (initial value)
1	Analogue comparator 0 clock supply

- **CCMP1** (bit 31)

The CCMP1 bit is used to control the clock of the analogue comparator 1.

CCMP1	Description
0	Analogue comparator 1 clock stop (initial value)
1	Analogue comparator 1 clock supply

[Note]

- Setting any flag to "0" (disable operation) stops the clock supply of the applicable block. When the flag is set to "0", writing to the registers on the block is disabled.
  To use the function of the block, follow the procedure below:
  (1) Reset the applicable flag of the clock control register to "1" (clock supply).
  (2) Reset the applicable flag of the reset control register to "0" (reset disabled).

  To stop the function of the block, follow the procedure below:
  (1) Set the applicable flag of the reset control register to "1" (reset enabled).
  (2) Set the applicable flag of the clock control register to "0" (clock stop).

5.2.8. Reset Control Register (RSTCON)

Address: 0x5C00_0050
Access: R/W
Access size: 32 bit
Initial value: 0xFFFF_EFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	RCMP1	RCMP0	RDMAC	RLLD	RVLS	RRTC	RLCD	RUSB	RRND	RAES	RI2CF0	RI2C1	RUAF0	RUA0	RSIOF0	RSIO0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	RTM1K	RRAD	RSAD	–*	RFTM3	RFTM2	RFTM1	RFTM0	RTM7	RTM6	RTM5	RTM4	RTM3	RTM2	RTM1	RTM0
Access	R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RSTCON is a special function register (SFR) used to control the reset of each block.

[Description of Bits]

- **RTM7-0** (bits 7-0)
  The RTM7 to RTM0 bits are used to control the reset of the 8-bit timer.

RTM0	Description
0	Timer 0 reset disabled
1	Timer 0 reset enabled (initial value)

RTM1	Description
0	Timer 1 reset disabled
1	Timer 1 reset enabled (initial value)

RTM2	Description
0	Timer 2 reset disabled
1	Timer 2 reset enabled (initial value)

RTM3	Description
0	Timer 3 reset disabled
1	Timer 3 reset enabled (initial value)

RTM4	Description
0	Timer 4 reset disabled
1	Timer 4 reset enabled (initial value)

RTM5	Description
0	Timer 5 reset disabled
1	Timer 5 reset enabled (initial value)

RTM6	Description
0	Timer 6 reset disabled
1	Timer 6 reset enabled (initial value)

RTM7	Description
0	Timer 7 reset disabled
1	Timer 7 reset enabled (initial value)

[Note]
Timers 0 and 1, Timers 2 and 3, Timers 4 and 5, or Timers 6 and 7 can be reset separately.

- **RFTM3-0** (bits 11-8)
The RFTM3, RFTM2, RFTM1, and RFTM0 bits are used to control the reset of the function timer (FTM).

RFTM0	Description
0	Function timer 0 reset disabled
1	Function timer 0 reset enabled (initial value)

RFTM1	Description
0	Function timer 1 reset disabled
1	Function timer 1 reset enabled (initial value)

RFTM2	Description
0	Function timer 2 reset disabled
1	Function timer 2 reset enabled (initial value)

RFTM3	Description
0	Function timer 3 reset disabled
1	Function timer 3 reset enabled (initial value)

- **RSAD** (bit 13)
The RSAD bit is used to control the reset of the successive approximation type (SA type) A/D converter.

RSAD	Description
0	SA type A/D converter reset disabled
1	SA type A/D converter reset enabled (initial value)

- **RRAD** (bit 14)
The RRAD bit is used to control the reset of the RC oscillation type A/D converter.

RRAD	Description
0	RC oscillation type A/D converter reset disabled
1	RC oscillation type A/D converter reset enabled (initial value)

- **RTM1K** (bit 15)
  The RTM1K bit is used to control 1 kHz timer reset.

RTM1K	Description
0	1 kHz timer reset disabled
1	1 kHz timer reset enabled (initial value)

- **RSIO0** (bit 16)
  The RSIO0 bit is used to control the reset of the synchronous serial port.

RSIO0	Description
0	Synchronous serial port 0 reset disabled
1	Synchronous serial port 0 reset enabled (initial value)

- **RSIOF0** (bit 17)
  The RSIOF0 bit is used to control the reset of the synchronous serial port with FIFO.

RSIOF0	Description
0	Synchronous serial port 0 with FIFO reset disabled
1	Synchronous serial port 0 with FIFO reset enabled (initial value)

- **RUA0** (bit 18)
  The RUA0 bit is used to reset the UART0 operation.

RUA0	Description
0	UART0 reset disabled
1	UART0 reset enabled (initial value)

- **RUAF0** (bit 19)
  The RUAF0 bit is used to control the reset of UART with FIFO.

RUAF0	Description
0	UART with FIFO reset disabled
1	UART with FIFO reset enabled (initial value)

- **RI2C1** (bit 20)
  The RI2C1 bit is used to control the reset of the I2C bus interface 0.

RI2C1	Description
0	I2C bus interface 1 reset disabled
1	I2C bus interface 1 reset enabled (initial value)

- **RI2CF0** (bit 21)
  The RI2CF0 bit is used to control the reset of the I2C bus interface 0 with FIFO.

RI2CF0	Description
0	I2C bus interface 0 with FIFO reset disabled
1	I2C bus interface 0 with FIFO reset enabled (initial value)

- **RAES** (bit 22)
  The RAES bit is used to control the reset of AES.

RAES	Description
0	AES reset disabled
1	AES reset enabled (initial value)

- **RRND** (bit 23)
  The RRND bit is used to control the reset of the random number generator.

RRND	Description
0	Random number generator reset disabled
1	Random number generator reset enabled (initial value)

- **RUSB** (bit 24)
  The RUSB bit is used to control the reset of the USB bus interface.

RUSB	Description
0	USB bus interface reset disabled
1	USB bus interface reset enabled (initial value)

- **RLCD** (bit 25)
  The RLCD bit is used to control the reset of LCD driver.

RLCD	Description
0	LCD driver reset disabled
1	LCD driver reset enabled (initial value)

- **RRTC** (bit 26)
  The RRTC bit is used to control the reset of the real time clock. This bit is initialized with the power-on reset or the reset by the RESET_N pin. It is not initialized with the other reset causes.

RRTC	Description
0	Real time clock reset disabled
1	Real time clock reset enabled (initial value)

- **RVLS** (bit 27)
  The RVLS bit is used to control the reset of the power supply voltage detection circuit (VLS). This bit is not initialized by a VLS reset.

RVLS	Description
0	VLS reset disabled
1	VLS reset enabled (initial value)

- **RLLD** (bit 28)
  The RLLD bit is used to control the reset of the power supply voltage dropping detection circuit (LLD). This bit is not initialized by a LLD reset.

RLLD	Description
0	LLD reset disabled
1	LLD reset enabled (initial value)

- **RDMAC** (bit 29)
  The RDMAC bit is used to control the reset of DMAC.

RDMAC	Description
0	DMAC reset disabled
1	DMAC reset enabled (initial value)

- **RCMP0** (bit 30)
  The RCMP0 bit is used to control the reset of the analogue comparator 0.

RCMP0	Description
0	Analogue comparator 0 reset disabled
1	Analogue comparator 0 reset enabled (initial value)

- **RCMP1** (bit 31)
  The RCMP1 bit is used to control the reset of the analogue comparator 1.

RCMP1	Description
0	Analogue comparator 1 reset disabled
1	Analogue comparator 1 reset enabled (initial value)

[Note]

- Setting any flag to "1" (disable operation) enables the reset of the applicable block. When the flag is set to "1", writing to the registers on the block is disabled.
  To use the function of the block, follow the procedure below:
  (1) Reset the applicable flag of the clock control register to "1" (clock supply).
  (2) Reset the applicable flag of the reset control register to "0" (reset disabled).

  To stop the function of the block, follow the procedure below:
  (1) Set the applicable flag of the reset control register to "1" (reset enabled).
  (2) Set the applicable flag of the clock control register to "0" (clock stop).

5.3. Description of Operation

5.3.1. HALT Mode

During the HALT mode, the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", and the WFI/WFE instruction is executed, the LSI switches to the HALT mode.
When a WDT interrupt request, a valid interrupt is occurred, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK), the HALT mode is released, returning to the program run mode.
When a DMA request to DMAC is occurred, the HALT mode is released, switching to the DMA mode. The LSI switches to the HALT mode after DMA transfer is finished.
Figure 5-2 and Figure 5-3 show the operation waveforms in the HALT mode.

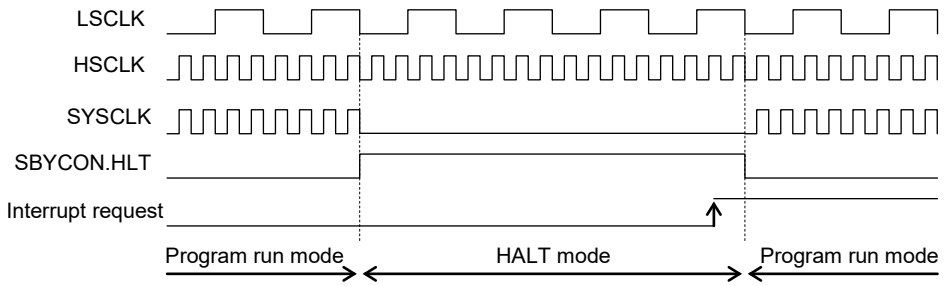


Figure 5-2(1) Operation Waveforms in HALT Mode (FCON1.SYSCLK=1, FCON1.ENOSC=1)

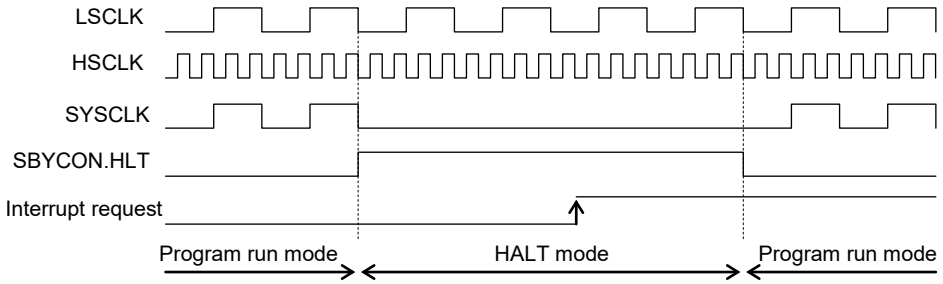


Figure 5-2(2) Operation Waveforms in HALT Mode (FCON1.SYSCLK=0, FCON1.ENOSC=1)

5.3.2. DEEP-HALT Mode

During the DEEP-HALT mode, the high-speed clock is stopped, the CPU interrupts execution of instructions, and the entire circuit stops operating except for some peripheral blocks such as watchdog timer and LTBC.
When the DHLT bit of the standby control register (SBYCON) is set to "1", and the WFI/WFE instruction is executed, the LSI switches to the DEEP-HALT mode.
When a WDT interrupt request, a valid interrupt is occurred, the DHLT bit is set to "0" on the falling edge of the next system clock (SYSCLK), the DEEP-HALT mode is released, returning to the program run mode.
When a DMA request to DMAC is occurred, the DEEP-HALT mode is released, switching to the DMA mode. The LSI switches to the DEEP-HALT mode after DMA transfer is finished.

When the DHLT bit is set to “1” during operation with the high-speed built-in RC clock, the mode returns to the program run mode with the high-speed built-in RC clock.
When low-speed clock counts 23, after the interrupt request is generated, high-speed built-in RC oscillation starts oscillation. And the counts256, as OSCLK clock supply. After two count of OSCLK, system clock is a high-speed clock, it returns to program operational mode.
When the DHLT bit is set to “1” during operation with the high-speed PLL clock, the mode returns to the program run mode with the low-speed Crystal oscillation clock. When low-speed clock counts 23, after the interrupt request is generated, system clock is a low-speed clock, it returns to program operational mode.

Figure 5-4 and Figure 5-5 show the operation waveforms in the DEEP-HALT mode when the internal RC oscillation and the PLL oscillation are used for the high-speed clock, respectively.

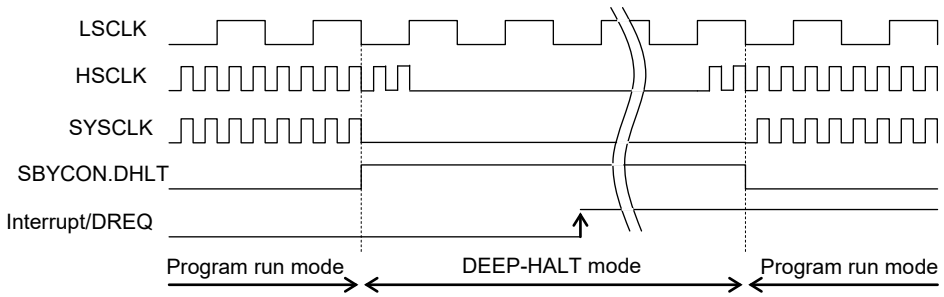


Figure 5-2 Operation Waveforms in DEEP-HALT Mode
(When Internal RC Oscillation Is Used for High-speed Clock)

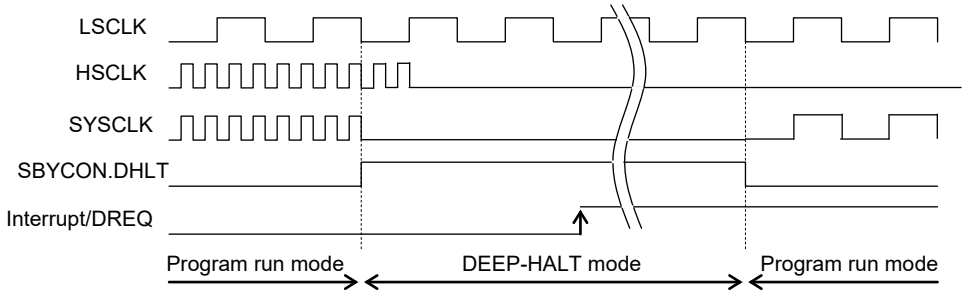


Figure 5-3 Operation Waveforms in DEEP-HALT Mode (When PLL Oscillation Is Used for High-speed Clock)

[Note]

- When switching to the DEEP-HALT mode while using the low-speed crystal oscillation, check that the LOSCS bit of the frequency status register (FSTAT) is set to "0".
  After the DEEP-HALT mode is released, a valid interrupt processing or a DMA transfer is started.

5.3.3. ULTRA-DEEP-HALT Mode

During the ULTRA-DEEP-HALT mode, the CPU interrupts execution of instructions, and the entire circuit stops operating except for some peripheral blocks such as watchdog timer and LTBC.
In the program run mode, when the UDHEN and UDHON bits of the power management register (PMCON) are set to "1" in the predetermined sequence, the DHLT bit of the standby control register (SBYCON) is set "1", and then the WFI/WFE instruction is executed, the LSI switches to the ULTRA-DEEP-HALT mode.
When a WDT interrupt request, a valid interrupt is occurred, the DHLT bit is set to "0" on the falling edge of the next system clock (SYSCLK), the ULTRA-DEEP-HALT mode is released, returning to the program run mode.
When a DMA request to DMAC is occurred, the ULTRA-DEEP-HALT mode is released, switching to the DMA mode. The LSI switches to the ULTRA-DEEP-HALT mode after DMA transfer is finished.

When the DHLT bit is set to “1” during operation with the high-speed built-in RC clock, the mode returns to the program run mode with the high-speed built-in RC clock.

When the DHLT bit is set to “1” during operation with the high-speed built-in RC clock, the mode returns to the program run mode with the high-speed built-in RC clock.
When low-speed clock counts 23, after the interrupt request is generated, high-speed built-in RC oscillation starts oscillation. And the counts256, as OSCLK clock supply. After two count of OSCLK, system clock is a high-speed clock, it returns to program operational mode.
When the DHLT bit is set to “1” during operation with the high-speed PLL clock, the mode returns to the program run mode with the low-speed Crystal oscillation clock. When low-speed clock counts 23, after the interrupt request is generated, system clock is a low-speed clock, it returns to program operational mode.

Figure 5-6 shows the operation waveforms in the ULTRA-DEEP-HALT mode when the internal RC oscillation is used for the high-speed clock.

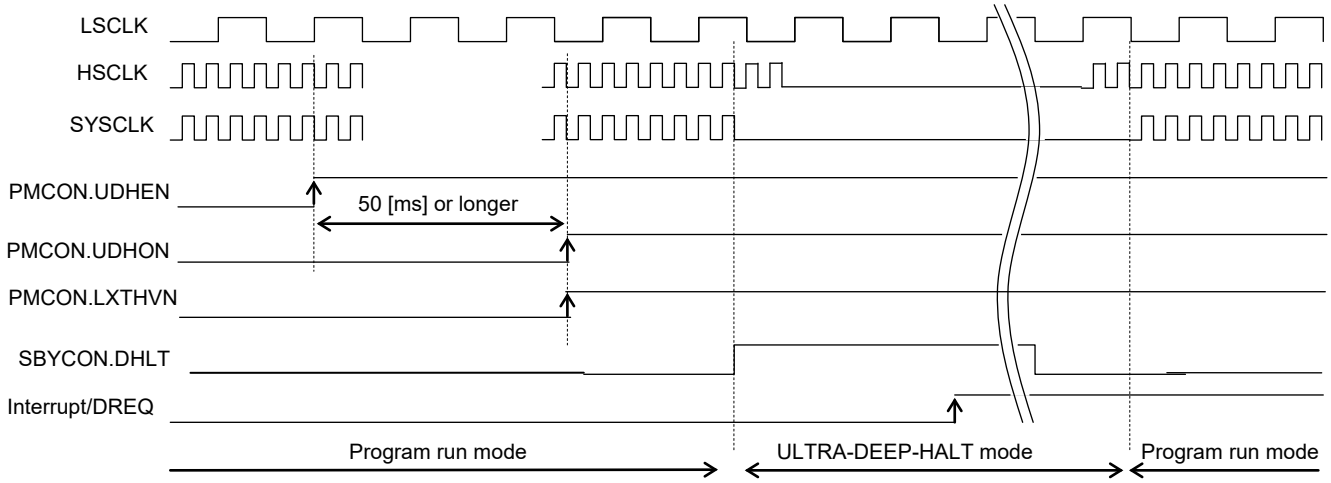


Figure 5-4 Operation Waveforms in ULTRA-DEEP-HALT Mode

[Note]

- When switching to the ULTRA-DEEP-HALT mode while using the low-speed crystal oscillation, check that the LOSCS bit of the frequency status register (FSTAT) is set to "0".
- After the ULTRA-DEEP-HALT mode is released, a valid interrupt processing or a DMA transfer is started.

5.3.4. HALT-H Mode

During the HALT-H mode, the CPU interrupts execution of instructions, the high-speed clock is stopped, and only the peripheral circuits operate that can operate with the low-speed clock.
When the HLTH bit of the standby control register (SBYCON) is set to "1", and the WFI/WFE instruction is executed, the high-speed clock stops, and the LSI switches to the HALT-H mode.
When a WDT interrupt request, a valid interrupt is occurred, the HLTH bit is set to "0" on the falling edge of the next system clock (SYSCLK), the HALT-H mode is released, returning to the program run mode.
When a DMA request to DMAC is occurred, the HALT-H mode is released, switching to the DMA mode. The LSI switches to the HALT-H mode after DMA transfer is finished.

When the LSI switches to the HALT-H mode with the system clock in the high-speed RC oscillation mode, it returns to the program run mode with the system clock in high-speed RC oscillation mode.
When the LSI switches to the HALT-H mode with the system clock in the PLL oscillation mode, it returns to the program run mode with the system clock in low-speed Crystal oscillation mode.
The LSI returns to the program run mode in up to 200[us] after an interrupt request occurs, which is faster than from DEEP-HALT mode.

Figure 5-7 shows the operation waveforms after switching to the HALT-H mode with the system clock in the high-speed RC oscillation mode.
Figure 5-8 shows the operation waveforms after switching to the HALT-H mode with the system clock in the PLL oscillation mode.

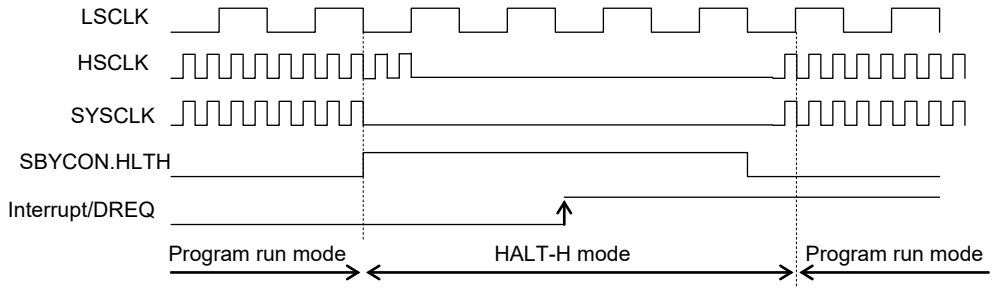


Figure 5-5 Operation Waveforms in HALT-H Mode
(When High-speed RC Oscillation Is Used for System Clock)

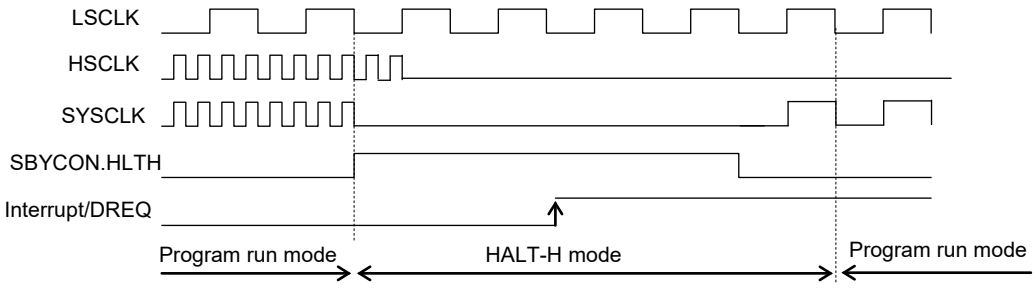


Figure 5-6 Operation Waveforms in HALT-H Mode
(When PLL Oscillation Is Used for System Clock)

[Note]
- After the HALT-H mode is released, a valid interrupt processing or a DMA transfer is started.

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5.3.5. STOP Mode

In the STOP mode, the low-speed oscillation and high-speed oscillation stop, and the CPU and peripheral circuits stop the operation.
When the SLEEPDEEP bit of the SCR register is set to "1", and the WFI/WFE instruction is executed, the LSI switches to the STOP mode. When a valid external pin interrupt request is generated, the STOP mode is released, returning to the program run mode.

[Note]
After the STOP mode is released, a valid interrupt processing is started.

5.3.5.1. Oscillation Stop and Restart Timing of Low-Speed Clock

When the LSI switches to the STOP mode, the low-speed and high-speed oscillations stop. When a valid external pin interrupt request is generated in the STOP mode, it is released, restarting the low-speed oscillation. If the high-speed clock was oscillating before switching to the STOP mode, the high-speed oscillation restarts. If the high-speed clock was not oscillating before switching the STOP mode, it does not start.
Regardless of the clock mode, the low-speed internal RC oscillation starts after an interrupt request is generated, and it starts supplying the low-speed internal RC clock to LSCLK after 24 counts. In case of the low-speed system clock, the LSI returns to the program run mode in the low-speed internal RC mode after 19 counts since the LSCLK output is started.
In the case of low-speed crystal oscillation mode, oscillation is started after low-speed oscillation start time (T_{XTL}) by interrupt request occurs. And, LSCLK changes from RC oscillation into crystal oscillation by the automatic operation in after counts 8192 by the crystal oscillation. For the low-speed oscillation start time (T_{XTL}), see Appendix C “Electrical Characteristics”.
Figure 5-9 shows the operation waveforms in the STOP mode when CPU operates with the low-speed clock.

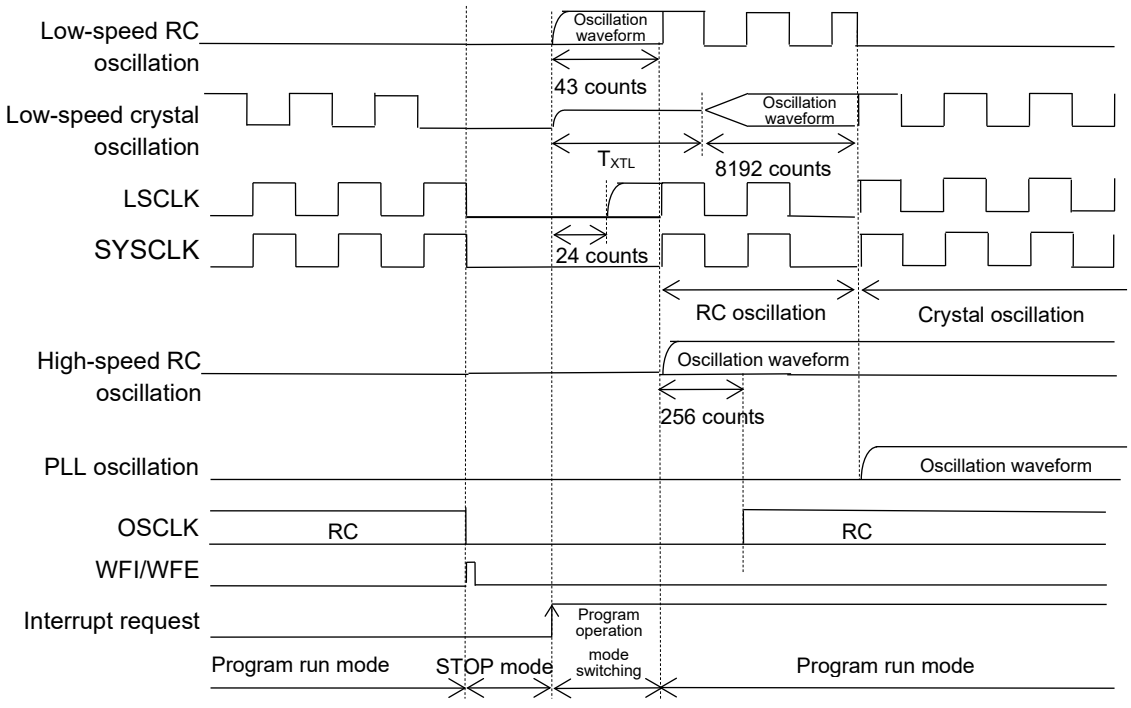


Figure 5-7 Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

5.3.5.2. Oscillation Stop and Restart Timing of High-Speed Clock

When the LSI switches to the STOP mode, the low-speed and high-speed oscillations stop. When a valid external pin interrupt request is generated in the STOP mode, it is released, restarting the high-speed and low-speed oscillations.
Regardless of the clock mode, the low-speed internal RC oscillation starts after an interrupt request is generated, and it starts supplying the low-speed internal RC clock to LSCLK after 24 counts. After 19 counts since the LSCLK output is started, the high-speed internal RC starts oscillating.
When the LSI switches to the STOP mode with the system clock in the high-speed RC oscillation mode, it returns to the program run mode with the system clock in high-speed RC oscillation mode once the high-speed internal RC counts to 256.
When the LSI switches to the STOP mode with the system clock in the PLL oscillation mode, it returns to the program run mode in the low-speed internal RC mode after 19 counts since the LSCLK output is started.
OSCLK outputs the PLL clock after LSCLK switches to the crystal oscillation. To use the system clock in the PLL oscillation mode after returning to the STOP mode, wait for LPLL bit =”1”, then switch to the mode from software.
For the low-speed oscillation start time (T_{XTL}), see Appendix C "Electrical Characteristics".
Figure 5-10 and Figure 5-11 show the operation waveforms in the STOP mode with the high-speed RC oscillation and the PLL oscillation, respectively.

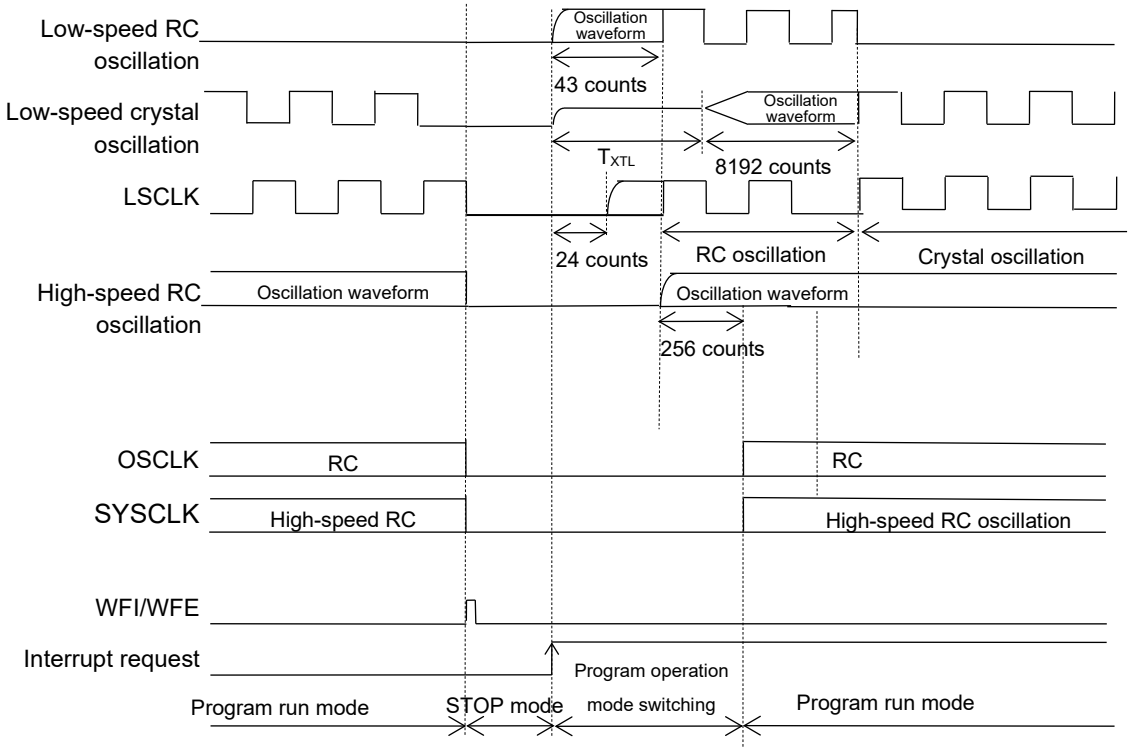


Figure 5-8 Operation Waveforms in STOP Mode with High-speed RC Oscillation

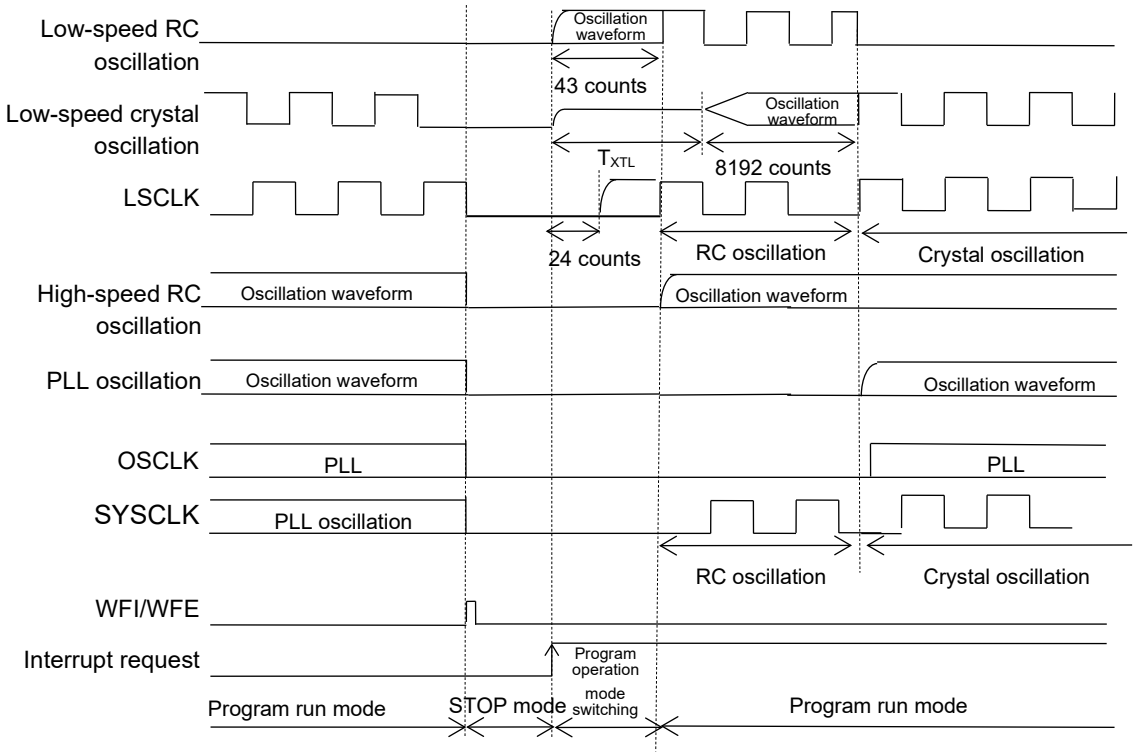


Figure 5-9 Operation Waveforms in STOP Mode With PLL Oscillation

5.3.6. Operation of Functions in STOP/HALT/DEEP-HALT/ULTRA-DEEP-HALT/HALT-H Mode

Table 5-1 shows the states of the functions in each of the STOP, HALT, DEEP-HALT, ULTRA-DEEP-HALT, and HALT-H modes.

Table 5-1 State of Functions in STOP/HALT/DEEP-HALT/ULTRA-DEEP-HALT/HALT-H Modes

Function	HALT	HALT-H*2	DEEP-HALT*2 ULTRA-DEEP-HALT*2	STOP
CPU	Not operable	Not operable	Not operable	Not operable
RAM	Retain	Retain	Retain	Retain
Watchdog timer	Operation	Operation	Operable	Not operable
External interrupt	Acceptable	Acceptable	Acceptable	Acceptable
DMAC	Operable	Operable	Operable	Not operable
LTBC	Operation	Operation	Operation	Not operable
Timer	Operable	Operable	Operable	Not operable
Function timer	Operable	Operable	Operable	Not operable
RTC	Operable	Operable	Operable	Not operable
1 kHz Timer	Operable	Operable	Operable	Not operable
UART	Operable	Operable	Not operable	Not operable
UART with FIFO	Operable*1	Not operable	Not operable	Not operable
SSIO	Operable	Operable	Not operable	Not operable
SSIO with FIFO	Operable*1	Not operable	Not operable	Not operable
I^2C	Operable*1	Not operable	Not operable	Not operable
I^2C with FIFO	Operable*1	Not operable	Not operable	Not operable
RC-ADC	Operable	Operable	Not operable	Not operable
SA-ADC	Operable	Operable	Not operable	Not operable
LCD	Operable	Operable	Operable	Not operable
USB	Operable*3	Not operable	Not operable	Not operable
Comparator	Operable	Operable	Operable	Operable
VLS	Operable	Operable	Operable	Operable
LLD	Operable	Operable	Operable	Operable

*1: Can operate only when the high-speed CLK is ON
*2: HALT-H, DEEP-HALT, or ULTRA-DEEP-HALT mode can operate only with the low-speed CLK
*3: Can operate only with the PLL oscillation

5.3.7. Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing current consumption.
For clock control register, the initial value of each flag is "0", meaning the clock of each block is stopped. The initial value of the reset control register is "1", meaning the reset of each block is enabled.

To use the function of the block, follow the procedure below:
(1) Set the applicable flag of the clock control register to "1" (clock supply).
(2) Reset the applicable flag of the reset control register to "0" (reset disabled).

To stop the function of the block, follow the procedure below:
(1) Set the applicable flag of the reset control register to "1" (reset enabled).
(2) Set the applicable flag of the clock control register to "0" (clock stop).

Chapter 6

Clock Generation Circuit

6. Clock Generation Circuit

6.1. General Description

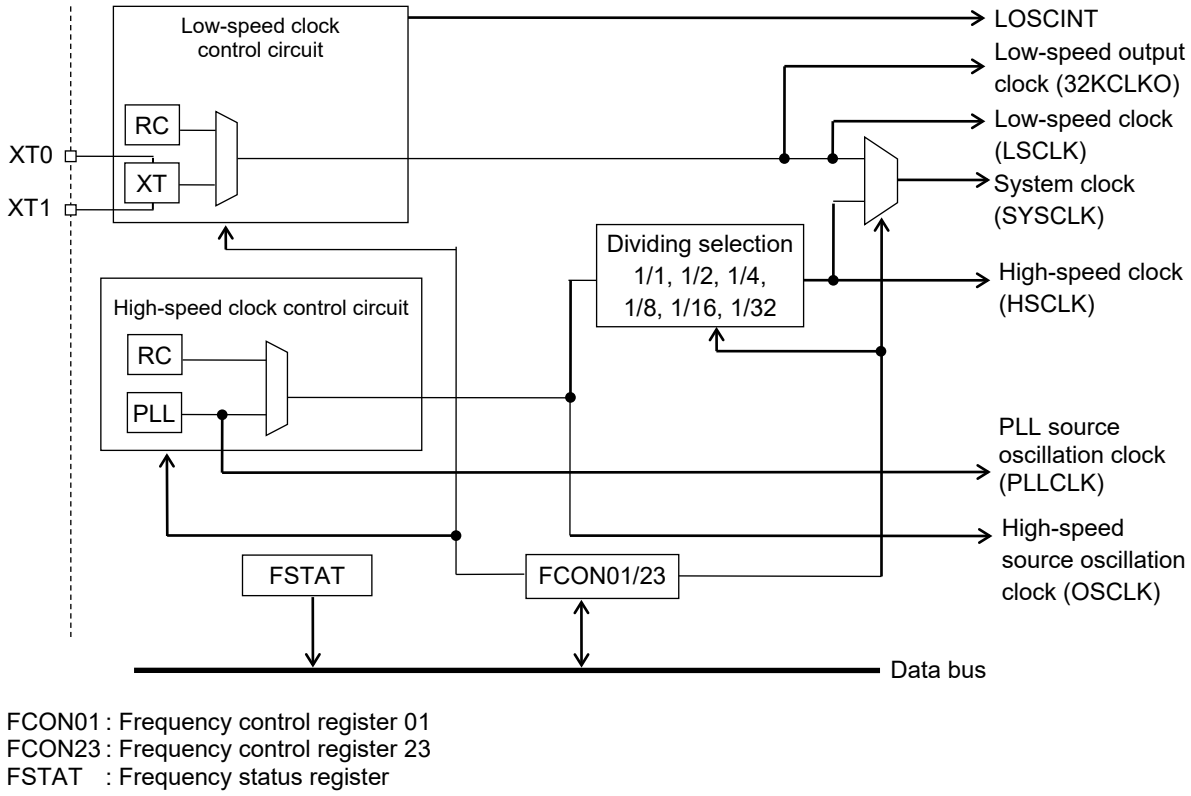
The clock generation circuit generates and provides the low-speed clock (LSCLK), the high-speed clock (HSCLK), the system clock (SYSCLK), and the low-speed output clock (32KCLKO). LSCLK and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and 32KCLKO is a clock that is output from a port.
For the 32KCLKO output port, see Chapter 22 "Port".
For the STOP mode described in this chapter, see Chapter 5, "System Control Function".

6.1.1. Features

- Low-speed clock generation circuit:
  - Crystal oscillation mode
  - Built-in RC oscillation mode
  - Interrupt generation at low-speed clock mode shift
- High-speed clock generation circuit:
  - Built-in RC oscillation mode
  - Built-in PLL Oscillation mode

6.1.2. Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON01 : Frequency control register 01
FCON23 : Frequency control register 23
FSTAT : Frequency status register

Figure 6-1 Configuration of Clock Generation Circuit

[Note]
After power-on or system reset, the operation starts by the clock supplied from the built-in RC high-speed clock generation circuit. At initialization by software, set the FCON01 and FCON23 register to switch to the required clock.

6.1.3. List of Pins

Pin Name	I/O	Function
XT0	I	Pin for connecting a crystal for low-speed clock.
XT1	I/O	Pin for connecting a crystal for low-speed clock.

6.1.4. Clock Configuration Diagram

Figure 6-2 shows the clock system diagram.

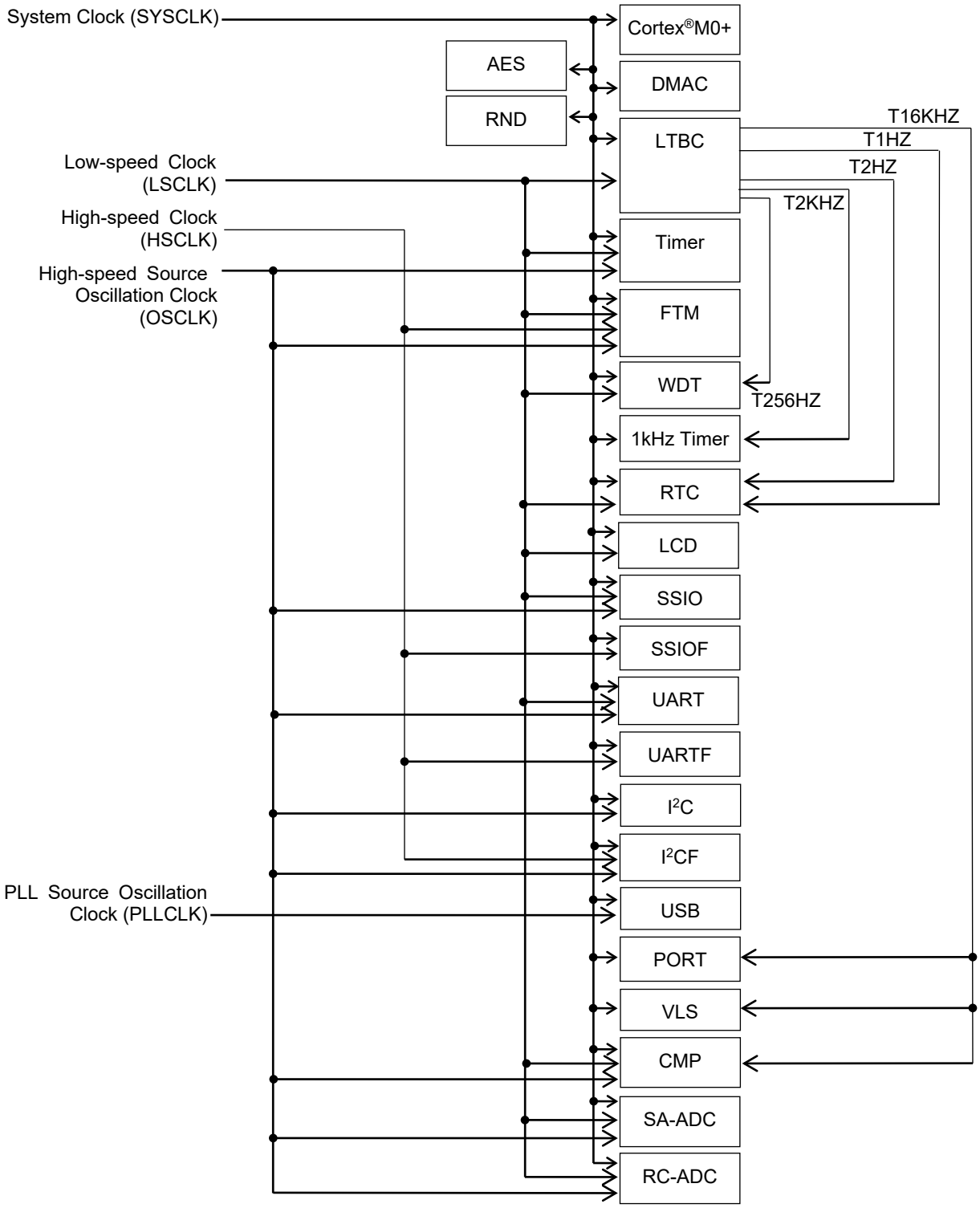


Figure 6-2 Clock System Diagram

6.2. Description of Registers

6.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_0300	Frequency control register 01	FCON01	R/W	32	0x0000_0313
0x5C00_0304	Frequency control register 23	FCON23	R/W	32	0x0000_0002
0x5C00_0308	Frequency status register	FSTAT	R	32	0x0000_0004

6.2.2. Frequency Control Register 01 (FCON01)

Address: 0x5C00_0300
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0313

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	LPLL	LOSST	–*	XSPEN	–*	ENPLL	ENOSC	SYSCLK	–*	–*	–*	OSCM[1:0]		SYSC[2:0]		
Access	R	R	–	R/W	–	R/W	R/W	R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FCON01 is a special function register (SFR) used to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

- **SYSC[2:0]** (bit 2 to 0)
  The SYSC[2:0] bit are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuits. OSCLK, 1/2OSCLK, 1/4OSCLK, 1/8OSCLK, 1/16OSCLK, or 1/32OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

SYSC[2]	SYSC[1]	SYSC[0]	Description
0	0	0	OSCLK
0	0	1	1/2OSCLK
0	1	0	1/4OSCLK
0	1	1	1/8OSCLK (initial value)
1	0	0	1/16OSCLK
1	0	1	1/32OSCLK
1	1	0	Setting prohibited (1/32OSCLK)
1	1	1	Setting prohibited (1/32OSCLK)

- **OSCM[1:0]** (bit 4 to 3)
  The OSCM[1:0] bits are used to select the high-speed clock mode. Built-in PLL oscillation mode or built-in RC oscillation mode can be selected. At system reset, the built-in RC oscillation mode is selected.
  OSCM[1:0] can be rewritten only when high-speed oscillation is being stopped (ENPLL and ENOSC bits of FCON01 are both "0").
  When switching the high-speed clock mode, at first, stop high-speed oscillation (set the ENPLL bit and the ENOSC bit of FCON01 register to “0”). Then switch the system clock to the low-speed clock (set SYSCLK bit of the FCON1 register to "0"). Finally, update the OSCM[1:0] bit then start high-speed oscillation (set the ENPLL bit or the ENOSC bit of FCON01 register to “1”).

OSCM[1]	OSCM[0]	Description
0	0	Setting prohibited (the setting is ignored and the previous value is held)
0	1	Built-in PLL oscillation mode
1	0	Built-in RC oscillation mode (initial value)
1	1	Setting prohibited (the setting is ignored and the previous value is held)

- **SYSCLK** (bit 8)
  The SYSCLK bit is used to select the system clock. The system clock can be selected from low-speed clock (LSCLK) or the HSCLK (1/nOSCLK: n = 1, 2, 4, 8, 16, 32) selected by SYSC[2:0].
  When the oscillation of high-speed clock stops (When OSCM[1:0] bits=”10”, setting ENOSC bit = "0" or When OSCM[1:0] bits=”01”, setting ENPLL bit= “0”), the SYSCLK bit is automatically cleared (“0”) and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK
1	HSCLK (initial value)

- **ENOSC** (bit 9)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed RC oscillator circuit.

ENOSC	Description
0	Disables high-speed RC oscillation
1	Enables high-speed RC oscillation (initial value)

- **ENPLL** (bit 10)
  The ENPLL bit is used to select enable/disable of the oscillation of the high-speed PLL oscillator circuit. This bit should be set with the low-speed crystal oscillation running.
  The status of the oscillation of the high-speed PLL oscillator circuit is confirmed the LPLL bit.

ENPLL	Description
0	Disables high-speed PLL oscillation (initial value)
1	Enables high-speed PLL oscillation

[Note]
When the high-speed clock mode is selected the built-in PLL oscillation mode (OSCM[1:0] = “01”) and the power-down mode which is stopped the high-speed clock (STOP mode, Deep HALT/ULTRA Deep HALT mode, HALT-H mode) is entered, ENPLL bit is automatically cleared (ENPLL=”0”). The system clock is selected the low-speed clock after returning to the power-down mode which is stopped the high-speed clock. If the built-in PLL oscillation is used, setting ENPLL bit to “1” again.

- **XSPEN** (bit 12)
  The XSPEN bit is used to control the reset function of the low-speed crystal oscillation stop detection. When the XSPEN is set to "1" and the low-speed crystal oscillation is used, the system reset is asserted after detection of the low-speed crystal oscillation stop.

XSPEN	Description
0	Disables the low-speed crystal oscillation stop detection reset function (initial value)
1	Enables the low-speed crystal oscillation stop detection reset function

- **LOSST** (bit 14)
  LOSST is the flag used to indicate the oscillation state of the low-speed crystal oscillator circuit.

LOSST	Description
0	The low-speed crystal oscillation has stopped, or the low-speed crystal oscillation stabilization time is being counted (initial value)
1	The low-speed crystal oscillation is in the stable state

- **LPLL** (bit 15)
  The LPLL is the flag used to indicate the oscillation state of the PLL oscillator circuit.

LPLL	Description
0	The PLL oscillator is not ready (initial value)
1	The PLL oscillator is ready

6.2.3. Frequency Control Register 23(FCON23)

Address: 0x5C00_0304
Access: R/W
Access size: 32bit
Initial Value: 0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	CR16 ENC	CR16 DC	–*	–*	–*	LFLT SEL	OUT LC	–*	XTM[1:0]	
Access	–	–	–	–	–	–	R/W	R/W	–	–	–	R/W	R/W	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FCON23 is a special function register (SFR) used to select the clock for the low-speed clock generation circuit.

[Description of Bits]

- **XTM[1:0]** (bit 1 to 0)
  The XTM[1:0] bits are used to select the low-speed clock mode. The low-speed crystal oscillation mode or the low-speed built-in RC oscillation mode can be selected. At system reset, the built-in low-speed RC oscillation mode is selected.

XTM[1]	XTM[0]	Description
0	0	Setting prohibited (the setting is ignored and the previous value is held)
0	1	Low-speed Crystal oscillation mode
1	0	Low-speed Built-in RC oscillation mode (initial value)
1	1	Setting prohibited (the setting is ignored and the previous value is held)

- **OUTLC** (bit 3)
  The OUTLC bit is used to select enable/disable of the low-speed clock output. Low-speed clock is output from the port by setting port tertiary function after OUTLC bit is set to “1”.

OUTLC	Description
0	Low speed clock output is disable (initial value)
1	Low speed clock output is enable

- **LFLTSEL** (bit 4)
  The LFLTSEL bit is used to select noise filter on/off at low-speed crystal oscillation mode.

LFLTSEL	Description
0	Low speed clock noise filter is off (initial value)
1	Low speed clock noise filter is on

- CR16DC (bit 8)
  The CR16DC bit is used to control the calibration of the high-speed RC oscillation circuit. If this calibration is on, the frequency error rate can be reduced and also the power consumption can be increased. And it is necessary for the calibration to run the low-speed crystal oscillation circuit.

CR16DC	Description
0	The calibration of the high-speed RC oscillation is off. (initial value)
1	The calibration of the high-speed RC oscillation is on.

- CR16ENC (bit 9)
  The CR16ENC bit is used to select enable/disable of the calibration of the high-speed RC oscillator circuit. This bit should be set with the low-speed crystal oscillation running.

CR16ENC	Description
0	Disables calibration of high-speed RC oscillation (initial value)
1	Enables calibration of high-speed RC oscillation

6.2.4. Frequency Status Register (FSTAT)

Address: 0x5C00_0308
Access: R
Access size: 32 bit
Initial value: 0x0000_0004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	C16MBS	C16MCDO	–*	–*	–*	LOSCS	–*	–*
Access	–	–	–	–	–	–	–	–	R	R	–	–	–	R	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FSTAT is a special function register (SFR) used to show the clock generation circuit state.

[Description of Bits]

- **LOSCS** (bit 2)
  LOSCS indicates the oscillation mode of the low-speed oscillator circuit. LOSCS changes when the low-speed oscillation mode switches. LOSCS is always "1" if the low-speed built-in RC oscillation mode is selected by the XTM[1:0] bit of the FCON23 register. Regardless of the low-speed oscillation mode, this becomes "1" when the mode enters the STOP mode.

LOSCS	Description
0	The low-speed crystal oscillation is stable.
1	The low-speed built-in RC oscillation is stable. The low-speed crystal oscillation is not stable or stops. (initial value)

- **C16MCDO** (bit 6)
  The C16MCDO bit indicates that calibration of high-speed RC oscillator has been completed. This bit is cleared by writing “0” by software.

C16MCDO	Description
0	Before calibration start or during calibration. (initial value)
1	Calibration is completed.

- **C16MBS** (bit 7)
  The C16MBS bit indicates during the high-speed RC oscillator calibration or not.

C16MBS	Description
0	The high-speed RC oscillator is not in the calibration. (initial value)
1	The high-speed RC oscillator is in the calibration.

6.3. Description of Operation

6.3.1. Low-Speed Clock

6.3.1.1. Low-Speed Built-In RC Oscillation Mode

Figure 6-3 shows the low-speed clock generation circuit configuration in the low-speed built-in RC oscillation mode.
When the RC oscillation clock is counted to 128, the low-speed oscillation clock (LSCLK) starts to be supplied.

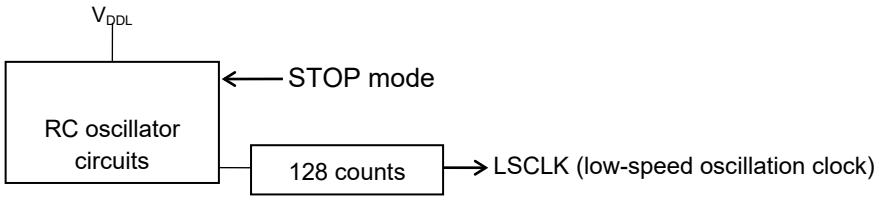


Figure 6-3 Circuit Configuration in the low-speed Built-in RC Oscillation Mode

6.3.1.2. Low-Speed Crystal Oscillation Mode

Figure 6-4 shows the low-speed clock generation circuit configuration in the crystal oscillation mode.
The low-speed clock generation circuit is provided with an external 32.768 kHz crystal. To match the oscillation frequency by using a trimmer capacitor, connect external capacitors (C_{GL} and C_{DL}) as required.

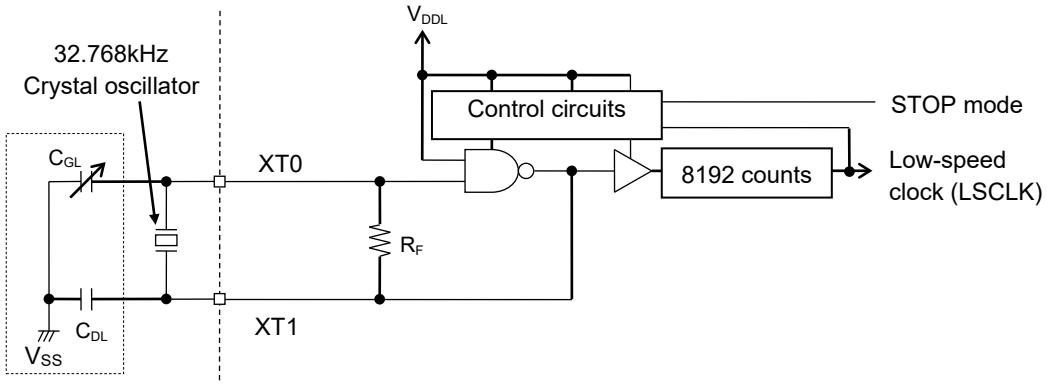


Figure 6-4 Circuit Configuration of the Crystal Oscillation Mode

[Note]
•Carefully design a board so that the crystal oscillator does not stop.
−Place the crystal oscillator near LSI as much as possible, and do not place a signal and power supply wiring that it becomes a noise source near the crystal oscillator and the wiring.
-The impedance between XT1 and XT0 might decrease by moisture uptake of circuit board in high moisture environment and condensation on the circuit board, and then the oscillation trouble may occur. Please make moisture measures such as coating the circuit board when used in such environments. The oscillation stop might be caused due to condensation.
Refer to the application note; “Precautions for MCU board design” for details.

6.3.1.3. Low-Speed Built-In RC Oscillation Mode Operation

The low-speed built-in RC oscillation mode starts by the occurrence of power ON reset.
After power-on, the built-in RC oscillation clock is counted to 128 as the low-speed clock, then the built-in RC oscillation clock (LSCLK) is supplied to the peripheral circuits.
The RC low-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. It restarts oscillation when the stop mode is released by an external interrupt. The built-in RC oscillation clock is counted to 46 as the low-speed clock, then the built-in RC oscillation clock (LSCLK) is supplied to the peripheral circuits. For STOP mode, see Chapter 5, "System Control Function".
Figure 6-5 shows the operation waveforms of the low-speed clock generation circuit in the built-in RC oscillation mode.

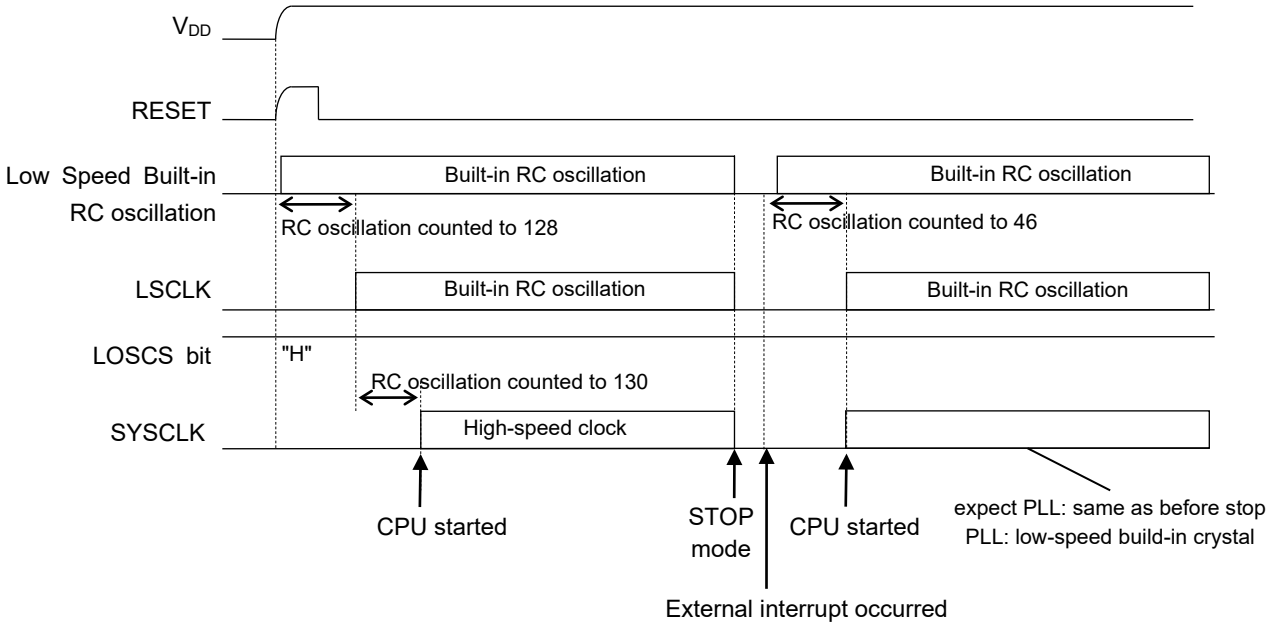


Figure 6-5 Low-Speed Clock Generation Circuit Operation (Low-speed Built-In RC Oscillation Mode)

6.3.1.4. Low-Speed Crystal Oscillation Mode Operation

For the low-speed crystal oscillation, the oscillation start/stop can be controlled by the frequency control register 01 (FCON01) or the frequency control register 23 (FCON23).
If it sets the XTM[1:0] bit of FCON23 to "01", Crystal oscillator circuit starts oscillation. After waiting for the low-speed crystal oscillation start time (T_{XTL}) and the low-speed crystal oscillation stabilization time (8192 counts), the low-speed clock (LSCLK) switches from the build-in RC oscillation clock to the low-speed crystal oscillation clock. In this time, the low-speed oscillation clock switch interrupt (LOSCINT) is generated.
Refer to Chapter 5 “System Control Function” for the operation at each power down mode.

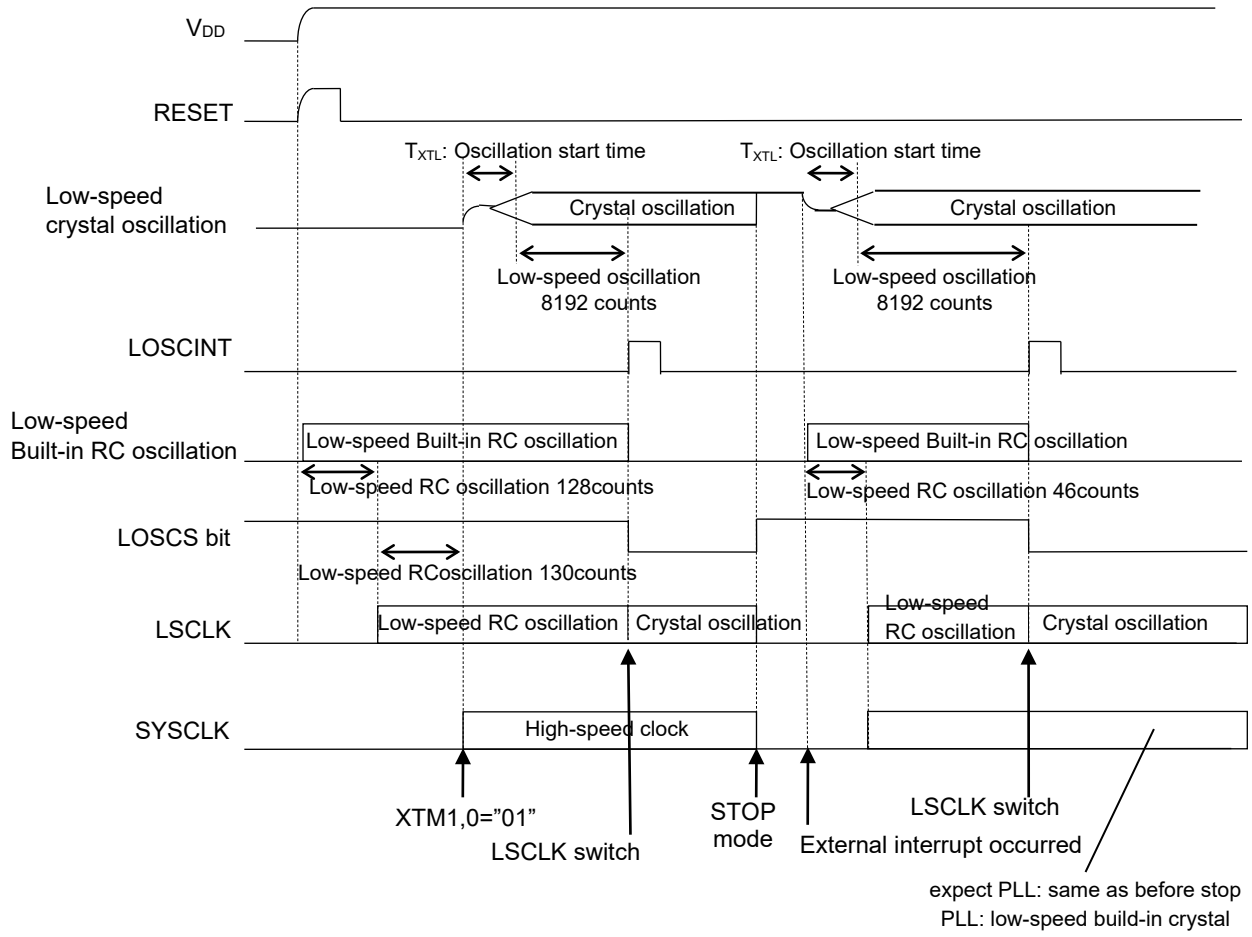


Figure 6-6 Low-Speed Clock Generation Circuit Operation (Crystal Oscillation Mode)

6.3.2. High-Speed Clock

For the high-speed clock generation circuit, the built-in RC oscillation mode or the built-in PLL oscillation mode can be selected.

6.3.2.1. Built-In RC Oscillation Mode

Figure 6-7 shows the high-speed clock generation circuit configuration in the built-in RC oscillation mode. When the RC oscillation clock is counted to 256, the high-speed oscillation clock (OSCLK) starts to be supplied.

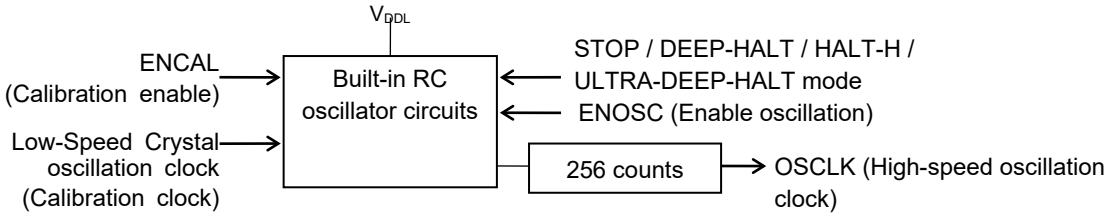


Figure 6-7 Circuit Configuration in the Built-in RC Oscillation Mode

6.3.2.2. Built-In PLL Oscillation Mode

Figure 6-8 shows the high-speed clock generation circuit configuration in the built-in PLL oscillation mode. Built-in PLL oscillation is stable and is in a condition to be able to supply it to high-speed oscillation clock (OSCLK) after setting to ENPLL= "1" and LPLL bit becomes "1".

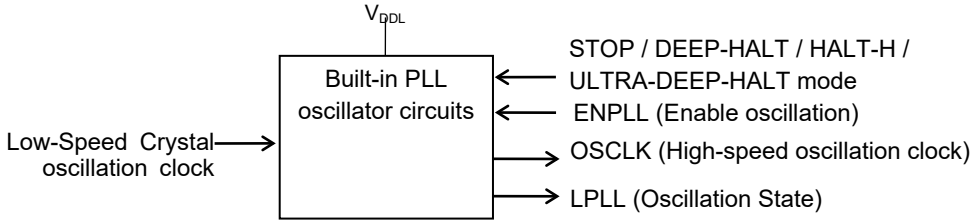


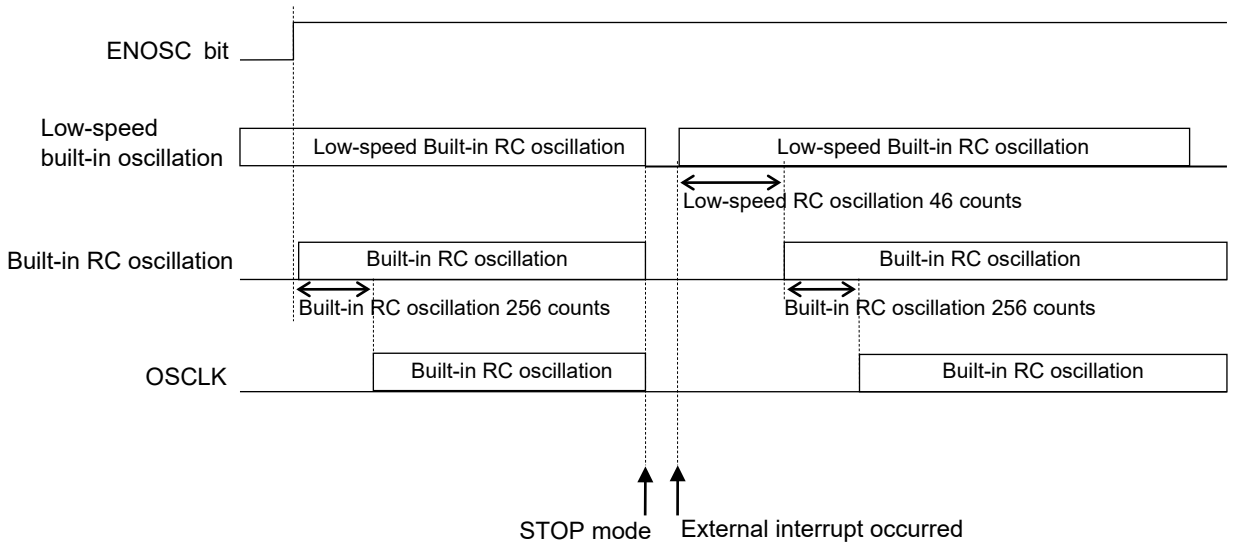
Figure 6-8 Circuit Configuration in the Built-In PLL Oscillation Mode

6.3.2.3. Built-In RC Oscillation Mode Operation

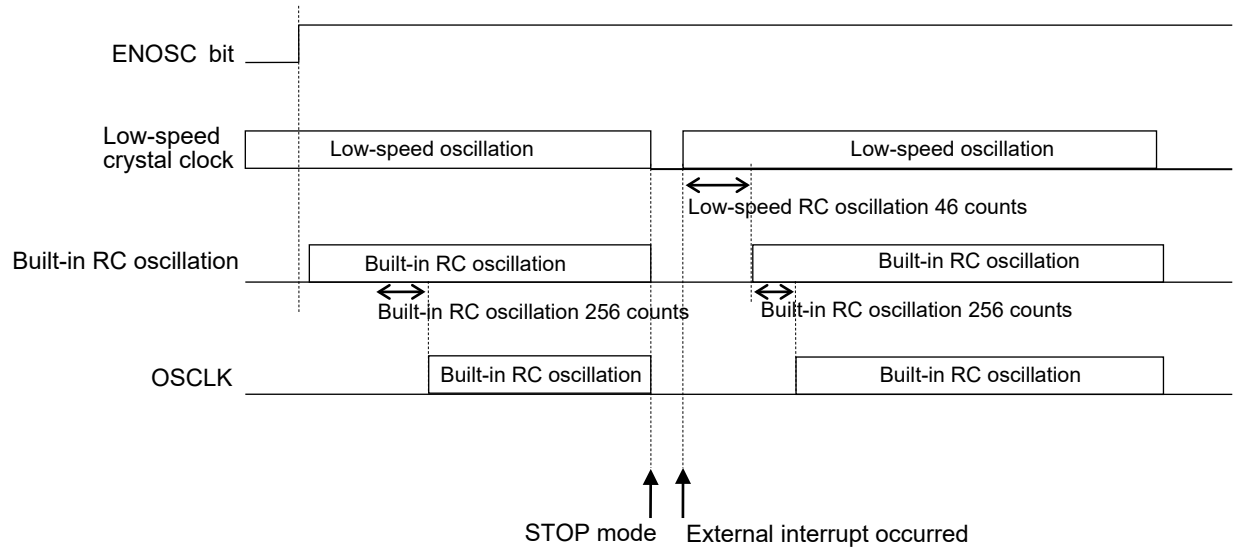
For the built-in RC oscillation, the oscillation start/stop can be controlled by the frequency control register 01 (FCON01).
Oscillation can be started by setting the ENOSC bit of FCON01 to "1". OSCLK starts to be supplied after the built-in RC oscillation clock is counted to 256 after the oscillation starts. In the low-speed crystal oscillation mode or external clock input mode, high-speed built-in oscillation starts after the low-speed clock is counted to 46.

The high-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. By releasing the stop mode by an external interrupt, the low-speed built-in RC oscillation clock is counted to 46 and then the high-speed built-in RC oscillation clock is counted to 256, then the built-in RC oscillation clock is supplied as OSCLK.
Refer to Chapter 5 “System Control Function” for the operation at each power down mode.

Figure 6-9 shows the operation waveforms of the high-speed clock generation circuit in the built-in RC oscillation mode.



(a) In the low-speed built-in RC oscillation mode



(b) In the low-speed crystal oscillation mode

Figure 6-9 High-Speed Clock Generation Circuit Operation (Built-In RC Oscillation Mode)

6.3.2.4. Built-In RC Oscillator Calibration Operation

The high-speed built-in RC oscillator can calibrate by itself by using the low-speed crystal oscillation and can keep the high frequency accuracy.
The calibration starts after setting the CR16DC bit and CR16ENC bit of FCON23 register to “1” in the low-speed crystal oscillation operation.
During calibration, C16MBS bit of frequency status register (FSTAT) becomes "1".
Can confirm a state of the calibration in C16MCDO bit.
CR16DC bit is a state of "1" and clock output is a state doing and continues calibration.
When finish calibration, make CR16DC bit "0". C16MBS bit becomes "0" after low-speed crystal oscillation 8 cycles(max), and the calibration is finished.

Figure 6-10 shows the movement wave pattern of the calibration.

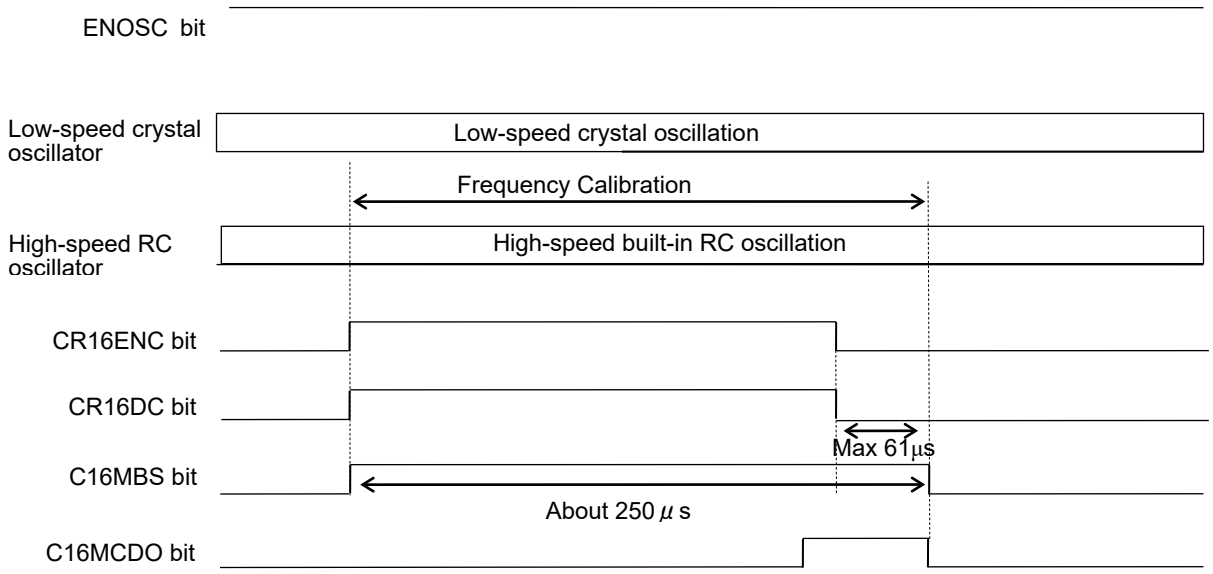


Figure 6-10 High-speed built-in RC oscillator calibration Operation

6.3.2.5. Operation of the Built-In PLL Oscillation mode

The high-speed clock (OSCLK) is switch from built-in RC oscillation clock by built-in PLL oscillation clock when make OSCM[1:0] bits of FCON01 "01".
After changing OSCM[1:0] bits, make ENPLL bit of FCON01 "1". And waiting for LPLL bit =“1”, available as a high-speed clock.
When the built-in PLL oscillation shifts to STOP mode by software, stop an oscillation.
When low-speed built-in RC oscillation clock 46 counts after the cancellation of the STOP mode by the external interrupt, and waiting for LPLL bit=”1” after low speed crystal clock after 8192 counts, Built-in PLL oscillation clock becomes available. Refer to Chapter 5 "System Control Function" for the movement in each power down mode.
Figure 6-11 shows the operation wave pattern of the high-speed clock generation circuit in the built-in PLL oscillation mode.

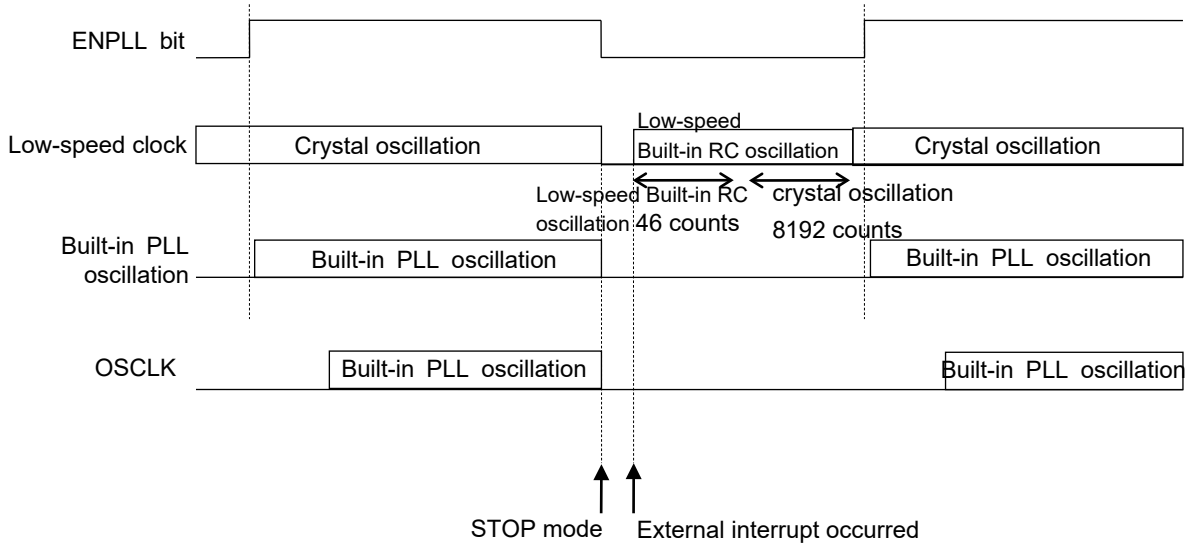


Figure 6-11 Operation of Built-in PLL Circuit (Low-speed crystal oscillation mode)

6.3.3. Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON01).
Figure 6-12 shows the flow chart of the system clock switching processing (HSCLK→LSCLK), and Figure 6-13 shows the flow chart of the system clock switching processing (LSCLK→HSCLK).

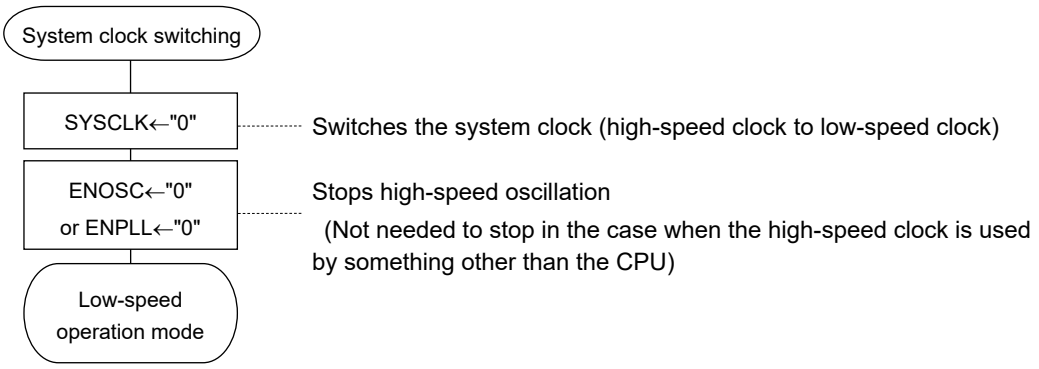


Figure 6-12 Flow Chart of System Clock Switching Processing (HSCLK to LSCLK)

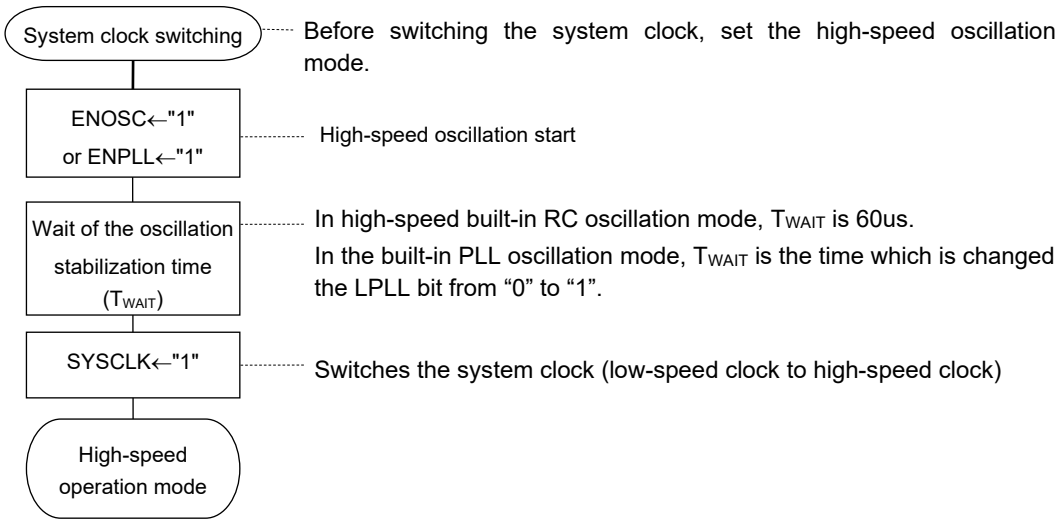


Figure 6-13 Flow Chart of System Clock Switching Processing (LSCLK to HSCLK)

6.3.4. Low-speed oscillation clock switch interrupt

The low-speed oscillation clock change interrupt occurs only when switching the mode from low-speed built-in RC oscillation mode to low-speed crystal oscillation mode. The interrupt does not occurs when switching the mode from low-speed crystal oscillation mode to low-speed build-in RC oscillation mode.

Chapter 7

Interrupts

7. Interrupts

7.1. General Description

This LSI has 32 interrupt sources (External interrupts: 1 sources, Internal interrupts: 31 sources) and a software interrupt (SVC).
For details of each interrupt, see the following chapters:

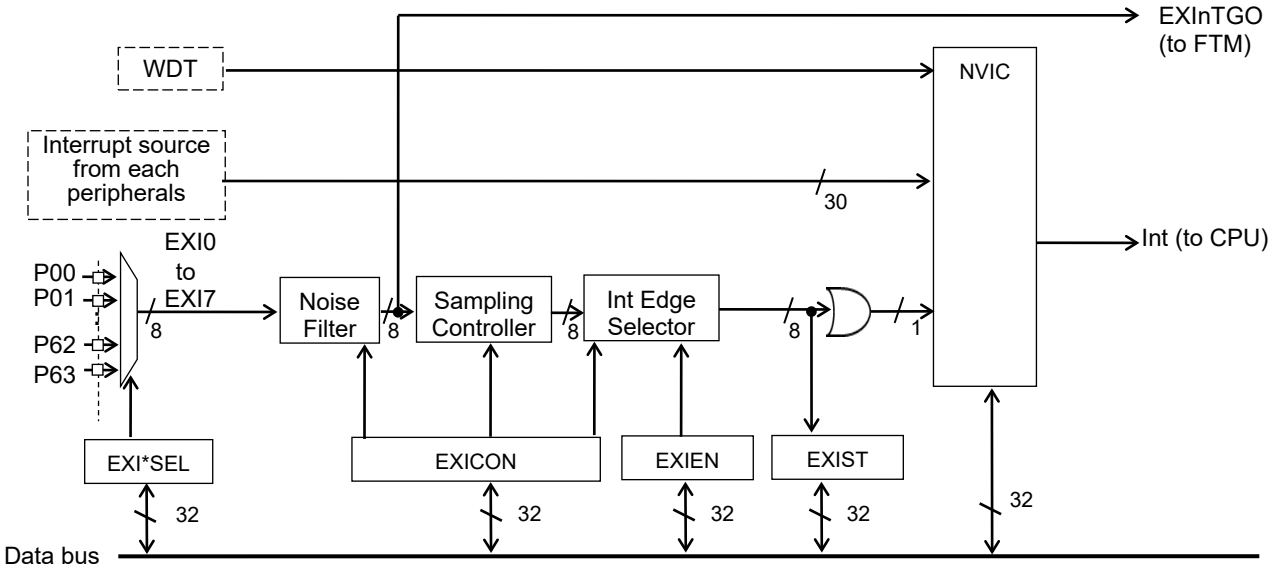
"Chapter 6 Clock Generation Circuit"
"Chapter 8 DMAC "
"Chapter 9 Time Base Counter "
"Chapter 10 Timers"
"Chapter 11 Function Timer(FTM)"
"Chapter 12 Real Time Clock(RTC)"
"Chapter 13 1kHz Timer "
"Chapter 14 Watchdog Timer"
"Chapter 15 Synchronous Serial Port(SSIO)"
"Chapter 16 Synchronous Serial Port with FIFO(SSIOF)"
"Chapter 17 UART"
"Chapter 18 UART with FIFO (UARTF)"
"Chapter 19 I^2C Bus Interface"
"Chapter 20 I^2C Bus Interface with FIFO(I2CF)"
"Chapter 21 USB Device"
"Chapter 22 Port"
"Chapter 23 AES"
"Chapter 25 RC Oscillation type A/D Converter(RC-ADC)"
"Chapter 26 Successive Approximation Type A/D Converter(SA-ADC)"
"Chapter 28 Analog Comparator"
"Chapter 30 Voltage Level Supervisor(VLS)"

7.1.1. Features

- Non-maskable interrupt source: 1 (WDT)
- Maskable interrupt sources: 31 (Internal sources: 30, External sources: 1)
- Software interrupt (SVC)
- External interrupts and comparator allow edge selection and sampling selection

7.1.2. Configuration

Figure 7-1 shows the circuit of the interrupt controller.



EXICON : External interrupt control register
EXIEN : External interrupt enable register
EXIST : External interrupt status register
EXI03/47SEL : External interrupt 03/47 select register
EXI0 to 7 : External interrupt

Figure 7-1 Configuration of Circuit

7.2. Description of Registers

7.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_0100	External interrupt enable register	EXIEN	R/W	32	0x0000_0000
0x5C00_0104	External Interrupt status register	EXIST	R/W	32	0x0000_0000
0x5C00_0108	External interrupt control register	EXICON	R/W	32	0x0000_0000
0x5C00_010C	External interrupt 03 selection register	EXI03SEL	R/W	32	0x0000_0000
0x5C00_0110	External interrupt 47 selection register	EXI47SEL	R/W	32	0x0000_0000
0xE000_E100	Interrupt set-enable register	NVIC_ISER	R/W	32	0x0000_0000
0xE000_E180	Interrupt clear-enable register	NVIC_ICER	R/W	32	0x0000_0000
0xE000_E200	Interrupt set-pending register	NVIC_ISPR	R/W	32	0x0000_0000
0xE000_E280	Interrupt clear-pending register	NVIC_ICPR	R/W	32	0x0000_0000
0xE000_E400	Interrupt priority register 0	NVIC_IPR0	R/W	32	0x0000_0000
0xE000_E404	Interrupt priority register 1	NVIC_IPR1	R/W	32	0x0000_0000
0xE000_E408	Interrupt priority register 2	NVIC_IPR2	R/W	32	0x0000_0000
0xE000_E40C	Interrupt priority register 3	NVIC_IPR3	R/W	32	0x0000_0000
0xE000_E410	Interrupt priority register 4	NVIC_IPR4	R/W	32	0x0000_0000
0xE000_E414	Interrupt priority register 5	NVIC_IPR5	R/W	32	0x0000_0000
0xE000_E418	Interrupt priority register 6	NVIC_IPR6	R/W	32	0x0000_0000
0xE000_E41C	Interrupt priority register 7	NVIC_IPR7	R/W	32	0x0000_0000

For details of the interrupt registers of NVIC (0xE000_E100 to 0xE000_E41C), see the section about NVIC of "Cortex™-M0+ Devices Generic User Guide".

7.2.2. External interrupt enable register (EXIEN)

Address: 0x5C00_0100
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	EEXI7	EEXI6	EEXI5	EEXI4	EEXI3	EEXI2	EEXI1	EEXI0
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
EXIEN is a special function register (SFR) used to control enable/disable for each interrupt request.

[Description of Bits]

- **EEXI0** (bit 0)
  EEXI0 is the enable flag for the external interrupt 0 (EXI0).

EEXI0	Description
0	Disabled (initial value)
1	Enabled

- **EEXI1** (bit 1)
  EEXI1 is the enable flag for the external interrupt 1 (EXI1).

EEXI1	Description
0	Disabled (initial value)
1	Enabled

- **EEXI2** (bit 2)
  EEXI2 is the enable flag for the external interrupt 2 (EXI2).

EEXI2	Description
0	Disabled (initial value)
1	Enabled

- **EEXI3** (bit 3)
  EEXI3 is the enable flag for the external interrupt 3 (EXI3).

EEXI3	Description
0	Disabled (initial value)
1	Enabled

- **EEXI4** (bit 4)
  EEXI4 is the enable flag for the external interrupt 4 (EXI4).

EEXI4	Description
0	Disabled (initial value)
1	Enabled

- **EEXI5** (bit 5)
  EEXI5 is the enable flag for the external interrupt 5 (EXI5).

EEXI5	Description
0	Disabled (initial value)
1	Enabled

- **EEXI6** (bit 6)
  EEXI6 is the enable flag for the external interrupt 6 (EXI6).

EEXI6	Description
0	Disabled (initial value)
1	Enabled

- **EEXI7** (bit 7)
  EEXI7 is the enable flag for the external interrupt 7 (EXI7).

EEXI7	Description
0	Disabled (initial value)
1	Enabled

7.2.3. Interrupt Request Register 01 (EXIST)

Address: 0x5C00_0104
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	QEXI7	QEXI6	QEXI5	QEXI4	QEXI3	QEXI2	QEXI1	QEXI0
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
EXIST is a special function register (SFR) used to hold the each interrupt request.
An interrupt is requested to the CPU when the related flag of the interrupt enable register (EXIEN) is set to "1" and the related bit is set to "1".
The bit which interrupt request is occurred can be clear by writing "1" to this bit.

[Description of Bits]

- **QEXI0** (bit 0)
  QEXI0 is the request flag for the external interrupt 0 (EXI0).

QEXI0	Description
0	No request (initial value)
1	Request

- **QEXI1** (bit 1)
  QEXI1 is the request flag for the external interrupt 1 (EXI1).

QEXI1	Description
0	No request (initial value)
1	Request

- **QEXI2** (bit 2)
  QEXI2 is the request flag for the external pin interrupt 2 (EXI2).

QEXI2	Description
0	No request (initial value)
1	Request

- **QEXI3** (bit 3)
  QEXI3 is the request flag for the external interrupt 3 (EXI3).

QEXI3	Description
0	No request (initial value)
1	Request

- **QEXI4** (bit 4)
  QEXI4 is the request flag for the external interrupt 4 (EXI4).

QEXI4	Description
0	No request (initial value)
1	Request

- **QEXI5** (bit 5)
  QEXI5 is the request flag for the external interrupt 5 (EXI5).

QEXI5	Description
0	No request (initial value)
1	Request

- **QEXI6** (bit 6)
  QEXI6 is the request flag for the external interrupt 6 (EXI6).

QEXI6	Description
0	No request (initial value)
1	Request

- **QEXI7** (bit 7)
  QEXI7 is the request flag for the external interrupt 7 (EXI7).

QEXI7	Description
0	No request (initial value)
1	Request

[Note]
When writing “1” to these bits, writing more than 2cycle later after writing to EXIEN register.

7.2.4. External Interrupt Control Register (EXICON)

Address: 0x5C00_0108
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	EXI7FL	EXI7SM	EXI7E[1:0]		EXI6FL	EXI6SM	EXI6E[1:0]		EXI5FL	EXI5SM	EXI5E[1:0]		EXI4FL	EXI4SM	EXI4E[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	EXI3FL	EXI3SM	EXI3E[1:0]		EXI2FL	EXI2SM	EXI2E[1:0]		EXI1FL	EXI1SM	EXI1E[1:0]		EXI0FL	EXI0SM	EXI0E[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
EXICON is a special function register (SFR) used to set the interrupt edge, filter, sampling of external interrupt.

[Description of Bits]

- **EXI7-0E[1:0]**(bit 1-0, 5-4, 9-8, 13-12, 17-16, 21-20, 25-24, 29-28)
  The EXI7-0E[1:0] bits are used to select the interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for EXI0 to 7, respectively.
  For the EXIn setting, the EXInE[1:0] bits determine the interrupt mode of the external interrupt (Example: When EXI0E[1:0] = "10", the external interrupt of EXI0 is in the rising-edge interrupt mode).

EXI7-0E1	EXI7-0E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt
1	0	Rising-edge interrupt
1	1	Both-edge interrupt

- **EXI7-0SM** (bit 2, 6, 10, 14, 18, 22, 26, 30)
  The EXI7-0SM bits are used to select detection of signal edge for an external interrupt with or without sampling. The sampling clock is T16KHz of the low-speed time base counter (LTBC).

EXI7-0SM	Description
0	Detects the input signal edge for an external interrupt without sampling (initial value).
1	Detects with sampling

[Note]
In STOP mode, since the sampling clock (T16KHZ) stops, no sampling is performed regardless of the values set in EXI7-0SM.

- **EXI7-0FL** (bit 3, 7, 11, 15, 19, 23, 27, 31)
  The EXI7-0FL bits are used to select detection of signal edge for an external interrupt with or without noise filter.

EXI7-0FL	Description
0	Detects without noise filter (initial value)
1	Detects with noise filter

7.2.5. External Interrupt 03 Selection Register (EXI03SEL)

Address: 0x5C00_010C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	EXI3S[7:0]								EXI2S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	EXI1S[7:0]								EXI0S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
EXI03SEL is a special function register (SFR) used to select the port used as EXI0 to EXI3.

[Description of Bits]

- **EXInS[7:0]** (bit 7-0, 15-8, 23-16, 31-24) (n=0 to 3)
  The EXInS[3:0] registers are used to select the bit of the port used as EXIn.
  The EXInS[7:4] registers are used to select the group of the port used as EXIn.
  (Example: When EXI0S[7:4] = "5" and EXI0S[3:0] = "1", Port 51 is used as EXI0).

EXInS[3:0] / EXInS[7:4]	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	–*	–*
1	–*	–*	–*	–*	–*	–*	–*	–*
2	P20	P21	P22	P23	–*	–*	–*	–*
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57
6	P60	P61	P62	P63	–*	–*	–*	–*

*: Setting is prohibited.

7.2.6. External Interrupt 47 Selection Register (EXI47SEL)

Address: 0x5C00_0110
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	EXI7S[7:0]								EXI6S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	EXI5S[7:0]								EXI4S[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
EXI47SEL is a special function register (SFR) used to select the port used as EXI4 to EXI7.

[Description of Bits]

- **EXInS[7:0]** (bit 7-0, 15-8, 23-16, 31-24) (n=4 to 7)
  The EXInS[3:0] registers are used to select the bit of the port used as EXIn.
  The EXInS[7:4] registers are used to select the group of the port used as EXIn.
  (Example: When EXI4S[7:4] = "5" and EXI4S[3:0] = "1", Port 51 is used as EXI4).

EXInS[3:0] / EXInS[7:4]	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	–*	–*
1	–*	–*	–*	–*	–*	–*	–*	–*
2	P20	P21	P22	P23	–*	–*	–*	–*
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57
6	P60	P61	P62	P63	–*	–*	–*	–*

*: Setting is prohibited.

7.3. Description of Operation

7.3.1. Interrupt Source

For 30 sources which do not include the watchdog timer interrupt (WDTINT), interrupt enable/disable is controlled by NVIC_ISER and NVIC_ICER. WDTINT is a non-maskable interrupt.
When the interrupt conditions are satisfied, the CPU reads the exception handler start address from the vector table address determined for each interrupt source and starts executing the exception handler.
Table 7-1 lists the interrupt sources.

Table 7-1 Interrupt Sources

Interrupt number	Interrupt source	Symbol	Vector table address
NMI	Watchdog timer interrupt	WDTINT	0x0000_0008
IRQ[0]	EXI interrupt	EXIINT	0x0000_0040
IRQ[1]	Timer 0 interrupt	TM0INT	0x0000_0044
IRQ[2]	Timer 1 interrupt	TM1INT	0x0000_0048
IRQ[3]	Function timer 0 interrupt	FTM0INT	0x0000_004C
IRQ[4]	DMAC ch0 interrupt	DMAC0INT	0x0000_0050
IRQ[5]	AES interrupt	AESINT	0x0000_0054
IRQ[6]	Synchronous serial port 0 interrupt	SIO0INT	0x0000_0058
IRQ[7]	I^2C bus 1 interrupt	I2C1INT	0x0000_005C
IRQ[8]	UART0 interrupt	UA0INT	0x0000_0060
IRQ[9]	Timer 2 interrupt	TM2INT	0x0000_0064
IRQ[10]	Timer 3 interrupt	TM3INT	0x0000_0068
IRQ[11]	Function timer 1 interrupt	FTM1INT	0x0000_006C
IRQ[12]	DMAC ch1 interrupt	DMAC1INT	0x0000_0070
IRQ[13]	Comparator interrupt	CMPINT	0x0000_0074
IRQ[14]	Synchronous serial port 0 with FIFO interrupt	SIOF0INT	0x0000_0078
IRQ[15]	I^2C with FIFO bus 0 interrupt	I2CF0INT	0x0000_007C
IRQ[16]	UART0 with FIFO interrupt	UAF0INT	0x0000_0080
IRQ[17]	Timer 4 interrupt	TM4INT	0x0000_0084
IRQ[18]	Timer 5 interrupt	TM5INT	0x0000_0088
IRQ[19]	Function timer 2 interrupt	FTM2INT	0x0000_008C
IRQ[20]	Low-speed oscillation clock switching interrupt	LOSCINT	0x0000_0090
IRQ[21]	VLS interrupt	VLSINT	0x0000_0094
IRQ[22]	Successive approximation type A/D converter interrupt	SADINT	0x0000_0098
IRQ[23]	RC oscillation type A/D converter interrupt	RADINT	0x0000_009C
IRQ[24]	USB interrupt	USBINT	0x0000_00A0
IRQ[25]	Timer 6 interrupt	TM6INT	0x0000_00A4
IRQ[26]	Timer 7 interrupt	TM7INT	0x0000_00A8
IRQ[27]	Function timer 3 interrupt	FTM3INT	0x0000_00AC
IRQ[28]	RTC interrupt	RTCINT	0x0000_00B0
IRQ[29]	Time base counter interrupt	LTBCINT	0x0000_00B4
IRQ[30]	1kHz timer interrupt	TM1KINT	0x0000_00B8

Interrupt number	Interrupt source	Symbol	Vector table address
IRQ[31]	-	-	0x0000_00BC

[Note]
- When multiple interrupts are generated concurrently, they are processed starting from the highest priority level, and the lower-priority interrupts are pending. If they have the same priority level, the interrupt with a smaller interrupt number has higher priority.
- Please define vector tables for all unused interrupts for fail safe.

7.3.2. External Interrupt

When an interrupt edge selected with the external interrupt control register (EXICON) occurs at one of external interrupts EXI0 to 7, any of the maskable EXI0 to EXI7 interrupts occurs.
It is possible to perform the filtering with noise filtering and/or sampling (2ϕ sampling with T16KHZ that is 2 dividing of LSCLK) for an external pin input.

But the signal for the trigger of FTM is filtered by noise filter/not sampling without relation for control of EXICON.

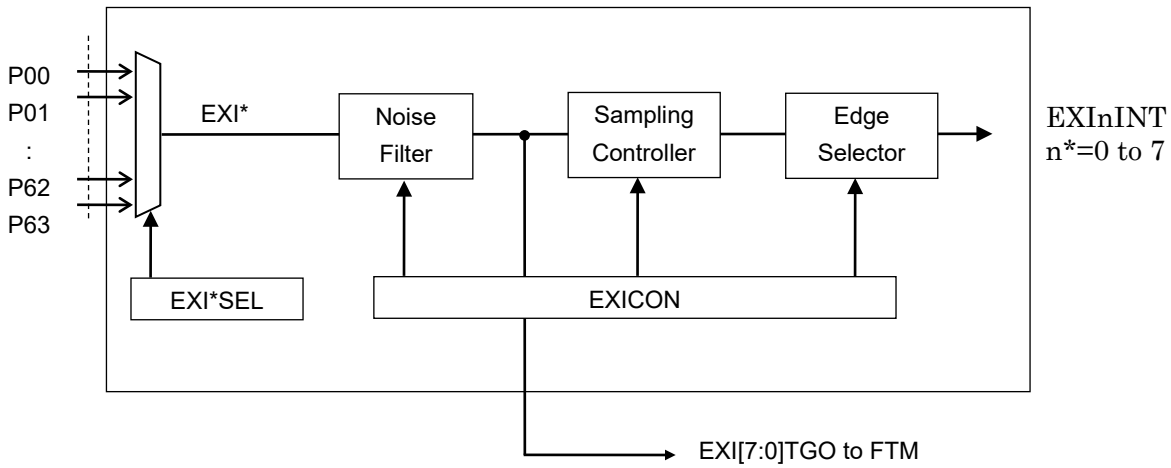
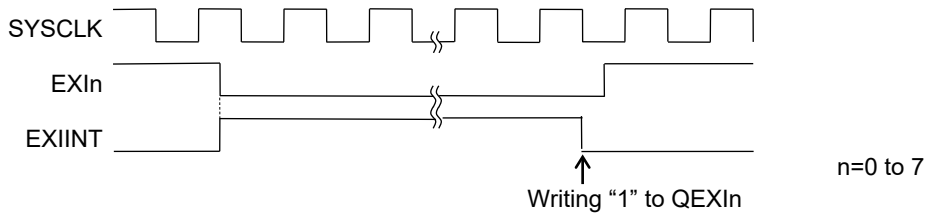
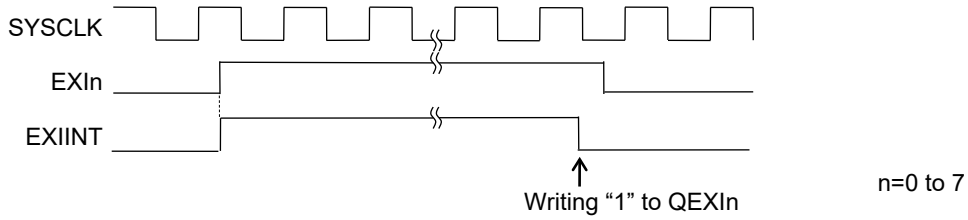


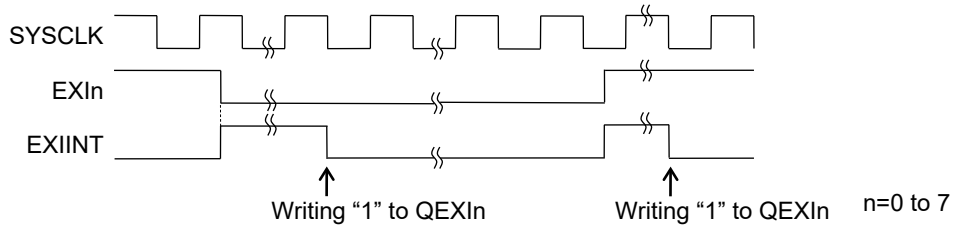
Figure 7-2 shows the interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling, and in rising-edge interrupt mode with sampling.



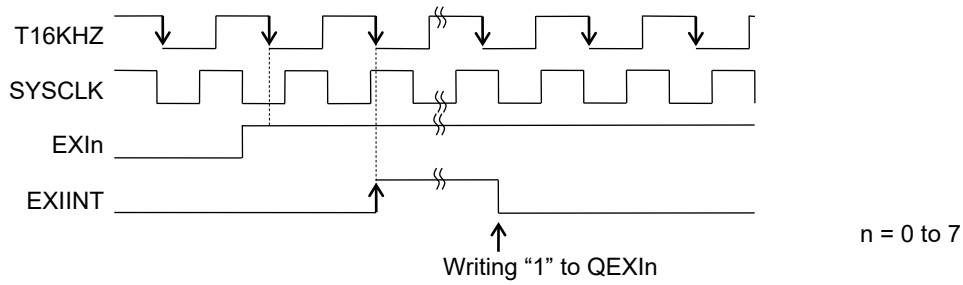
(a) When Falling-Edge Interrupt Mode without Sampling is Selected



(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 7-2 External Interrupt Generation Timing

Chapter 8

DMAC

8. DMAC

8.1. General Description

The DMAC (DMA controller) is a 2-channel direct memory access controller.
By incorporating the DMAC, data transfer between a memory unit and another memory unit, between I/O and memory unit, and between I/O and another I/O can be performed at high speed instead of using the CPU, reducing the burden on CPU operation as well as increasing the efficiency of LSI operation.
DMA transfer is supported for the various peripherals.

8.1.1. Features

- Channel count
  - 2 channels
- Channel priority
  - Fixed mode : Channel priority is always fixed. (Channel 0 > Channel 1).
  - Round robbing mode : The channel that has accepted a transfer request has the lowest priority.
- Maximum transfer count: 65536 (64K)
- Data transfer size
  - Byte (8 bits)/Half word (16 bits) /Word (32 bits)
- Dual address access
  - Data read from the transfer source and data write to the transfer destination are performed separately.
- Bus ownership request system
  - Cycle steal mode
    Bus ownership request signals are asserted for each DMA transfer.
  - Burst mode
    Bus ownership request signals are asserted until termination of the number of transfers specified.
    (Read→Write for a transfer unit is continuously performed up to the transfer count specified.)
- DMA transfer request system
  - Automatic request
    Transfer requests are automatically generated in the DMAC.
  - External requests
    Transfer requests are accepted by the request from the peripheral function block connected to the channel.
- Interrupt requests
  - An interrupt request is generated to the CPU after termination of the number of DMA transfers specified.
    Interrupt request signals are output to each channel individually.
    Interrupt request signals can be masked for each channel.

Note:
For selection of a peripheral that issues external requests, see Chapter 5, “System Control Function”, in the user’s manual.

8.1.2. Configuration

Figure 8-1 shows the configuration of the DMAC.

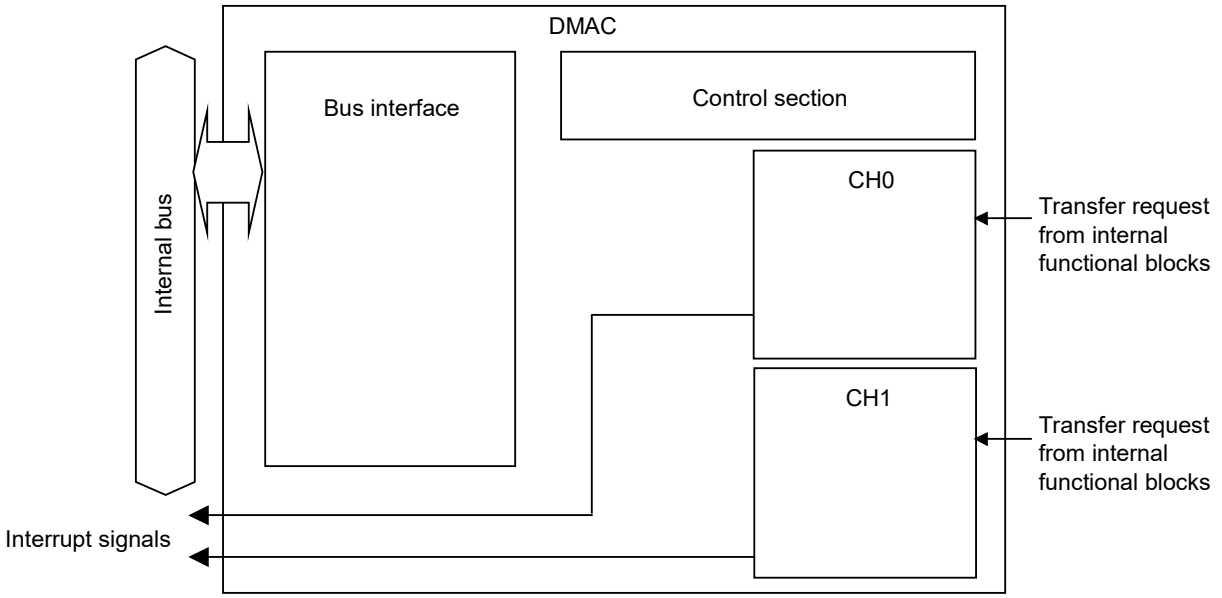


Figure 8-1 Configuration of DMAC

8.2. Description of Registers

8.2.1. List of Registers

CH	Address	Name	Symbol	R/W	Size	Initial value
Common	0x4700_0000	DMA mode register	DMAMOD	R/W	32	0x0000_0000
	0x4700_0004	DMA status register	DMASTA	R	32	0x0000_0000
	0x4700_0008	DMA end status register	DMAINT	R	32	0x0000_0000
CH0	0x4700_0100	DMA channel mask register	DMACMSK0	R/W	32	0x0000_0001
	0x4700_0104	DMA transfer mode register	DMACTMOD0	R/W	32	0x0000_0040
	0x4700_0108	DMA transfer source address register	DMACSAD0	R/W	32	0x0000_0000
	0x4700_010C	DMA transfer destination address register	DMACDAD0	R/W	32	0x0000_0000
	0x4700_0110	DMA transfer count register	DMACSIZ0	R/W	32	0x0000_0000
	0x4700_0114	DMA end status clear register	DMACCINT0	W	32	0x0000_0000
CH1	0x4700_0200	DMA channel mask register	DMACMSK1	R/W	32	0x0000_0001
	0x4700_0204	DMA transfer mode register	DMACTMOD1	R/W	32	0x0000_0040
	0x4700_0208	DMA transfer source address register	DMACSAD1	R/W	32	0x0000_0000
	0x4700_020C	DMA transfer destination address register	DMACDAD1	R/W	32	0x0000_0000
	0x4700_0210	DMA transfer count register	DMACSIZ1	R/W	32	0x0000_0000
	0x4700_0214	DMA end status clear register	DMACCINT1	W	32	0x0000_0000

8.2.2. DMA Mode Register (DMAMOD)

Address: 0x4700_0000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	PRI
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Register]
The DMAMOD register is a 32-bit readable/writable register that sets the priority (fixed/round robin) of each channel.

[Description of Bits]

- **PRI** (bit 0)
  Channel priority:
  In the case of the fixed mode, channel 0 has the highest channel priority and channel 1 has the lowest.
  In the case of the round robin mode, the channel that was used last among valid channels has the lowest channel priority.

PRI	Description
0	Fixed
1	Round robin

8.2.3. DMA Status Register (DMASTA)

Address: 0x4700_0004
Access: R/W
Access size: 32bit
Initial Value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	STA[1:0]	
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Register]
The DMASTA register is a 32-bit readable register that indicates the status of DMA transfer (whether untransferred data is present).
If a value other than "0" is set in the transfer count registers (DMACSIZ0, 1), "1" is set in the applicable channel bit. If a DMA transfer has been completed normally for the specified DMA transfer count or if it has been ended as an error during a DMA transfer, the applicable channel bit is cleared.

[Description of Bits]
- **STA[1:0]** (bits 0-1)
  These bits indicate the status of DMA transfer of channels 0 or 1 (whether untransferred data is present or not).

STA[0]	Description
0	ch0: No untransferred data present
1	ch0: Untransferred data present

STA[1]	Description
0	ch1: No untransferred data present
1	ch1: Untransferred data present

8.2.4. DMA Completion Status Register (DMAINT)

Address: 0x4700_0008
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	ISTP[1:0]	
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	ISTA[1:0]		–*	–*	–*	–*	–*	–*	IREQ[1:0]	
Access	–	–	–	–	–	–	R	R	–	–	–	–	–	–	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: To reference this register during interrupt processing, reference the ISTP bit when an abnormal end occurs.
At the time of normal end or forced abort, the ISTP bits retain the initial value.

[Description of Register]
The DMAINT register is a 32-bit readable register that indicates the interrupt request channel and its source (normal end/abnormal end) at the end of a DMA transfer, as well as the abnormal end cycle (read cycle (transfer source)/write cycle (transfer destination)).
When arbitrary data is written into the DMA completion status clear registers (DMACCINT0 or DMACCINT1) provided in each channel, the IREQ, ISTA and ISTP bits of the corresponding channel are cleared.

[Description of Bits]
- **IREQ[1:0]** (bits 0-1)
  These bits indicate whether an interrupt request for channels 0-1 exists or not.

IREQ[0]	Description
0	ch0: Does not generate interrupt request
1	ch0: Generates Interrupt request

IREQ[1]	Description
0	ch1: Does not generate interrupt request
1	ch1: Generates Interrupt request

- **ISTA[1:0]** (bits 8-9)
  These bits indicate the interrupt sources and normal end/abnormal end of channels 0-1.

ISTA[0]	Description
0	ch0: Normal end
1	ch0: Abnormal end

ISTA[1]	Description
0	ch1: Normal end
1	ch1: Abnormal end

- **ISTP[1:0]** (bits 16-17)
  These bits indicate the abnormal end cycles of channels 0-1.

ISTP[0]	Description
0	ch0: Abnormal end of read cycle
1	ch0: Abnormal end of write cycle

ISTP[1]	Description
0	ch1: Abnormal end of read cycle
1	ch1: Abnormal end of write cycle

8.2.5. DMA Channel Mask Registers (DMACMSK0-1)

Address: 0x4700_0100(CH0)
Address: 0x4700_0200(CH1)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	MSK
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Register]
The DMACMSK0-1 registers are 32-bit readable/writable registers that set the masks of channels. The DMAC does not perform transfer for masked channels.
Applicable channels are masked after a reset.

[Description of Bits]
- **MSK** (bit 0)
  This bit sets a channel mask.

MSK	Description
0	Releases channel mask
1	Channel mask

8.2.6. DMA Transfer Mode Registers (DMACTMOD0-1)

Address: 0x4700_0104(CH0)
Address: 0x4700_0204(CH1)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	IMK	BRQ	DDP	SDP	TSIZ[1:0]		ARQ
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Register]
The DMACTMOD0-1 registers are 32-bit readable/writable registers that set various DMA transfer modes (request/transfer size/device type/whether or not to generate an interrupt after transfer end).
If the IMK bit is set to "0", an interrupt can be generated when a DMA transfer ends (normal end/abnormal end). Be careful with the following items when setting these registers.

- Auto request is enabled (external request is disabled) when an auto request is specified for a transfer request with the ARQ bit and an external request signal is generated.
- The transfer size is restricted according to the device type and the bus width (See Section 8.4.).

[Description of Bits]

- **ARQ** (bit 0)
  This bit sets the DMA transfer request.

ARQ	Description
0	External transfer request
1	Auto request transfer request

- **TSIZ[1:0]** (bits 1-2)
  These bits set the transfer size.

TSIZ[1:0]	Description
00	Byte transfer
01	Half-word transfer
10	Word transfer
11	Prohibited

- **SDP** (bit 3)
  This bit sets the device type of the transfer source.

SDP	Description
0	Fixed address device
1	Increment address device

- **DDP** (bit 4)
  This bit sets the device type of the transfer destination.

DDP	Description
0	Fixed address device
1	Increment address device

- **BRQ** (bit 5)
  This bit sets the bus ownership request method.

BRQ	Description
0	Burst mode
1	Cycle steal mode

- **IMK** (bit 6)
  This bit sets the interrupt mask.

IMK	Description
0	Releases interrupt mask
1	Interrupt mask

8.2.7. DMA Transfer Source Address Registers (DMACSAD0-1)

Address: 0x4700_0108(CH0)
Address: 0x4700_0208(CH1)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	CSAD[31:16]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CSAD[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
This DMAC increments addresses according to the settings of the device type and transfer size. At that time, the lower bits of an address are ignored internally according to the settings; however, upon reading these registers, the lower bits output the values written.

[Description of Register]
The DMACSAD0-1 registers are 32-bit readable/writable registers that set the address of the DMA transfer source. A DMA transfer (read) is started based on the values set in these registers.
Also, if the transfer source is an increment address device, the address is incremented starting at the address set in this register according to the transfer size (byte/half-word/word), and if it is a fixed address device, fixed addresses are used as the DMAC accesses. Therefore note the following:

<In the Case of an Increment Address Device>
For word transfer : Set the lower two bits to “00”.
For half-word transfer : Set the lower one bit to “0”.
The address is updated when a read from the transfer source is completed normally.

8.2.8. DMA Transfer Destination Address Registers (DMACDAD0-1)

Address: 0x4700_010C(CH0)
Address: 0x4700_020C(CH1)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	CDAD[31:16]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CDAD[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
This DMAC increments addresses according to the settings of the device type and transfer size. At that time, the lower bits of an address are ignored internally according to the settings; however, upon reading these registers, the lower bits output the values written.

[Description of Register]
The DMACDAD0-1 registers are 32-bit readable/writable registers that set the address of the DMA transfer destination. A DMA transfer (write) is started based on the values set in these registers.
Also, if the transfer destination is an increment address device, the address is incremented starting at the address set in this register according to the transfer size (byte/half-word/word), and if it is a fixed address device, fixed addresses are used as the DMAC accesses. Therefore note the following:

<In the Case of an Increment Address Device>
For word transfer : Set the lower two bits to “00”.
For half-word transfer : Set the lower one bit to “0”.
The address is updated when a write to the transfer destination is completed normally.

8.2.9. DMA Transfer Count Registers (DMACSIZ0-1)

Address: 0x4700_0110(CH0)
Address: 0x4700_0210(CH1)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	CSIZ 16
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CSIZ[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Register]
The DMACSIZ0-1 registers are 32-bit readable/writable registers that set the DMA transfer count. When the transfer source (read) terminates properly, the values are decremented.
To perform DMA transfer n times, set this register to “n”.
Since the maximum setting value of these registers is “0001_0000H” (65536), the operation is not guaranteed if a value larger than the maximum setting value is specified.

8.2.10. DMA Completion Status Clear Registers (DMACCINT0-1)

Address: 0x4700_0114(CH0)
Address: 0x4700_0214(CH1)
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	CCINT[31:16]															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CCINT[15:0]															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
The DMACCINT0-1 registers are 32-bit writable registers that are used to clear the interrupt information of the applicable channel of the DMA completion status register (DMAINT).
When arbitrary data (32 bits) is written into these registers, the interrupt request bit (IREQ), interrupt source bit (ISTA) and abnormal end cycle bit (ISTP) of the corresponding channel of the DMAINT are cleared.

8.3. Description of Operation

8.3.1. Channel Priority

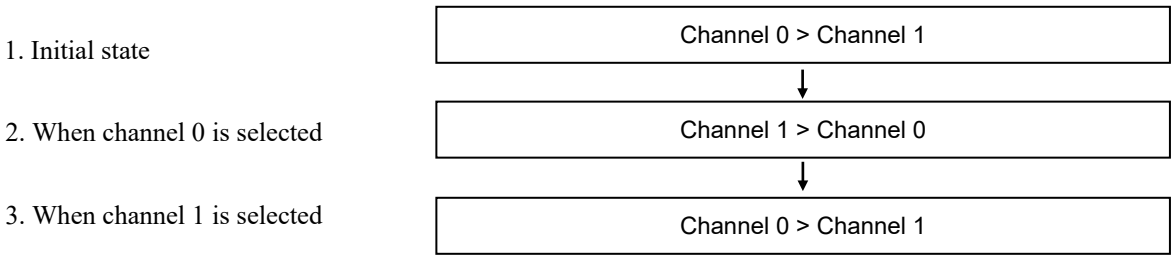
If a transfer request is issued to multiple channels at the same time, this DMAC performs transfers according to the predetermined priority order. The channel with the highest priority at that time can perform a DMA transfer in units of one transfer (byte, half-word, word, or one burst transfer).
The following methods are available to determine the priority order of channels, and either one can be selected by register setting.

8.3.1.1. Fixed Mode

In the fixed mode, the channel priority is channel 0 and channel 1 in this order.

8.3.1.2. Round Robin Mode

In the round robin mode, when a transfer in units of one transfer (byte, half-word, word, or one burst transfer) is completed in one channel, the priority order of that channel becomes the lowest, and the priority order is changed so that the channel with the second highest priority order becomes the highest. The channel priority after reset is channel 0 and channel 1 in this order.



8.3.2. Dual Address Access

In dual access, the DMAC accesses both the transfer source and the destination source via addresses, and performs DMA transfer using two bus cycles of a read cycle and a write cycle. The DMAC accesses the transfer source using a read cycle, and accesses the transfer destination using a write cycle, and then transfer data is temporarily stored in the register inside the DMAC.

8.3.3. Bus Ownership Request Method

If peripheral function blocks are selected by DMAC Control Register (DMARQCNT), use not Burst mode but Cycle steal mode. For the DMAC control register, see Chapter 5, “System Control Functions”.

8.3.3.1. Cycle Steal Mode

The DMAC deasserts the bus ownership request signal to the system bus for making accesses to the inside of the LSI every time 1 unit of transfer (1 byte, half-word or 1 word) is executed. Next, if there are any DMA transfers left that need to be executed, the DMAC asserts the bus ownership request signal, and executes 1 unit of transfer again after acquiring the bus ownership, and then deasserts the bus ownership request signal. This operation is repeated until the transfer end condition is satisfied.
If a transfer request is issued from a channel with a higher priority during a cycle steal transfer, the transfer of that channel is executed after one DMA transfer is finished.

8.3.3.2. Burst Mode

Once the DMAC obtains the bus ownership, it continuously asserts a bus ownership request signal until the specified number of transfers is complete. Therefore, in burst transfer, the bus ownership may not be passed to the CPU during the period of burst transfer; secure system performance by software processing.
If a transfer request is issued from a channel with a higher priority during a burst mode transfer, the transfer of that channel is not performed until the current burst transfer (for the specified number of transfers) is finished.

8.3.4. Termination of DMA Transfer

The following describes the DMA transfer termination and suspension conditions:

(a) Normal termination
If transfers are executed as many times as the value specified in the DMA transfer count register (DMACSIZ), the DMAC terminates the DMA transfer of the corresponding channel and can generate an interrupt.

(b) Abnormal termination
If the DMAC accesses a reserved area and receives an error response from the system bus, the DMAC immediately terminates DMA transfer and generates an interrupt.
Error information contains information about the channel in which the error occurred and about whether the error occurred in read cycle (occurred at the transfer source) or write cycle (occurred at the transfer destination). Error information can be acquired by referencing the values of IREQ, ISTA and ISTP of the DMA completion status register (DMAINT).
For the address areas causing error responses, see Chapter 3, "Memory Space".

(c) Forced suspension
When "1" is written (masked) in the mask channel bit of the DMA channel mask register (DMACMSK), the DMAC suspends transfer after the current transfer is terminated (a write to the transfer destination). In this case, an interrupt is not generated. Moreover, transfer can be resumed by canceling the mask.

Table 8-2 Register Values after DMA Transfer Terminates

Register		(a) After normal termination	(b) After abnormal termination	(c) After forced suspension
DMA status register (DMASTA)		"0" (No untransferred data)	"0" (No untransferred data)	"1" (Untransferred data present)
DMA completion status register (DMAINT)	IREQ	"1" (*1)	"1" (*1)	"0" (No change)
	ISTA	"0" (Normal termination)	"1" (Abnormal termination)	"0" (No change)
	ISTP	"0" (Initial status)	"0" (At transfer source error) "1" (At transfer destination error)	"0" (No change)
DMA transfer source/transfer destination address register (DMACSAD, DMACDAD)		Retains the address following the final transfer address	Retains the error address	Retains the address following the suspended transfer address
DMA transfer count register (DMACSIZ)		"0"	(*2)	Retains the number of remaining transfers

* 1: The IREQ bit is set to "1" regardless of the IMK (interrupt mask) bit setting of the DMA transfer mode register.
* 2: Note that the value varies depending on whether an error occurs at the transfer source or the transfer destination. The DMAC decrements the DMA transfer count register (DMACSIZ) when access to the transfer source is properly terminated.

8.3.5. DMA Transfer Request

There are two request modes for DMA transfer requests: the external request mode that uses the DMA transfer request signal from internal peripheral blocks, and the auto request mode that does not use such a signal. Either mode can be selected by register setting.

8.3.5.1. Auto Request Mode

The auto request mode is used to automatically generate transfer requests inside the DMAC. The CPU achieves this by setting the auto request bit to "1" inside the DMAC in the case of a transfer between memory and memory, or between a memory and a peripheral function block that cannot generate transfer requests.
In this case, once the auto request bit is set to "1", a DMA transfer is automatically performed every time the DMAC is started.

8.3.5.2. External Request Mode

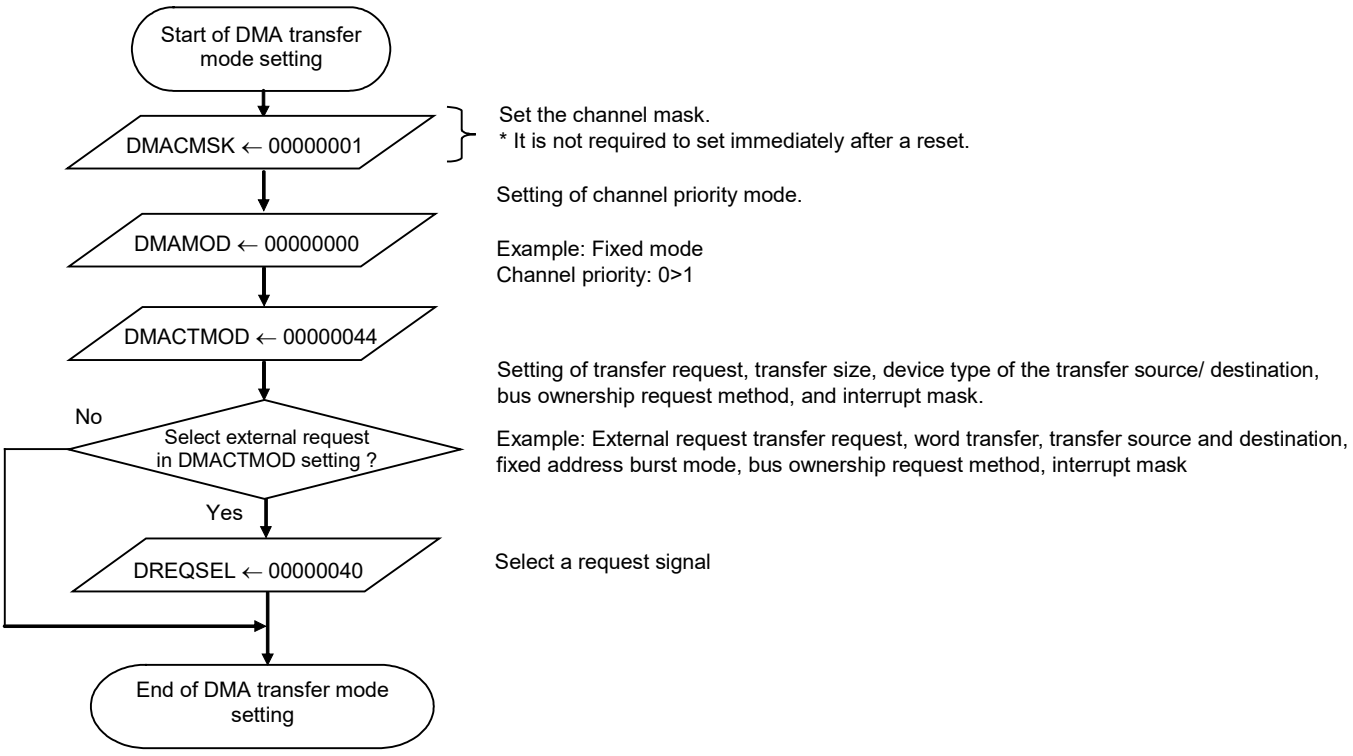
The external request mode is used to generate transfer requests by inputting a DMA transfer request signal from one of the peripheral function blocks. For the peripheral which is requested the external request, see Chapter 5, "System Control Function".

8.3.6. Procedure for setting DMA transfer mode

(1) Procedure for setting DMA transfer mode

1. Setting the DMA channel mask register (DMACMSK)
   - Channel mask
     (It is not necessary to set channel mask because channels are masked in the case of a transfer immediately after a reset.)
2. Setting the DMA mode register (DMAMOD)
   - Set the priority (fixed/round robin).
3. Setting the DMA channel transfer mode register (DMACTMOD) of the corresponding channel
   - Set the transfer request (auto request/external request).
   - Set the transfer size (byte/half-word/word).
   - Set the device type of the transfer source and destination (fixed address device/increment address device).
   - Set the bus ownership request method (set the cycle steal mode/burst mode).
   - Set whether to output or not to output an interrupt request.
4. Setting the DMAC Request Selection Register (DREQSEL)
   (In case of setting an external request in the DMACTMOD register)
   - Set the request signal.

The following figure shows an example of setting:

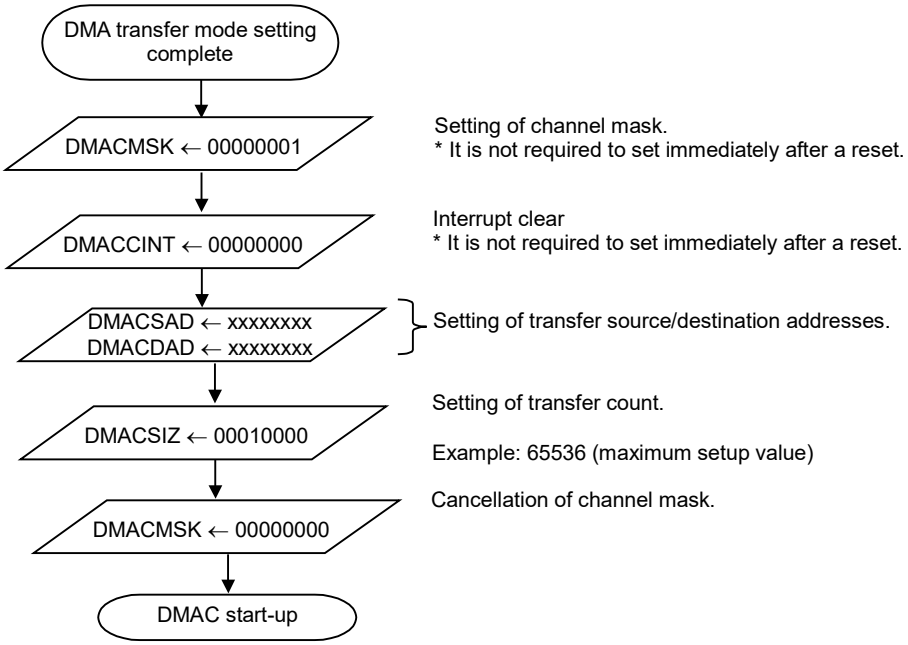


(2) Procedure for starting up DMAC

1. Setting the DMA channel mask register (DMACMSK) of the corresponding channel
   - Channel mask
     (It is not necessary to set this register in the case of a transfer immediately after a reset. For other cases, be sure to mask channels.)
2. Clearing an interrupt
   - Write arbitrary data into the DMA completion status clear register (DMACCINT).
     (It is not necessary to set this register in the case of a transfer immediately after a reset. For other cases, be sure to clear the interrupt.)
3. Setting the DMA channel start address registers (DMACSAD, DMACDAD) of the corresponding channel
   - Set the transfer source address register.
   - Set the transfer destination address register.
4. Setting the DMA channel transfer count register (DMACSIZ) of the corresponding channel
   - Set the transfer count.
5. Setting the DMA channel mask register (DMACMSK) of the corresponding channel
   - Start the DMAC by canceling the channel mask.

Note: If continuous DMA transfers are performed
In the case of an increment address device, the DMAC holds the next address in their respective registers (DMACSAD, DMACDAD) after the final transfer is terminated. Therefore, to transfer into successive address areas, the DMAC can be started by omitting the setting of the transfer source and destination addresses (step 3 above). In this case, be sure to perform interrupt clear processing (step 2 above). The DMAC does not perform transfer unless interrupt clear processing is performed.

The following figure shows an example of setting:



8.4. Notes

8.4.1. Notes at Transfer Size Setting

The DMAC cannot set the bus width of the transfer source and destination individually. Therefore, the data transfer size that can be used for DMA transfer may be limited according to the connecting device (transfer source/transfer destination). Determine the transfer size by giving consideration to the following items.

- Data bus width of transfer source and transfer destination devices
  8 bits, 16 bits or 32 bits
- Connection bus of transfer source and transfer destination devices
  Peripheral function block, or internal memory
- Device type of transfer source and transfer destination
  Increment address device or fixed address device

8.4.2. Notes at Accessing

It is prohibited to set the address of the register in the DMA to the source address and the destination address. If such an access is attempted, the operation cannot be guaranteed.

Chapter 9

Time Base Counter

9. Time Base Counter

9.1. Overview

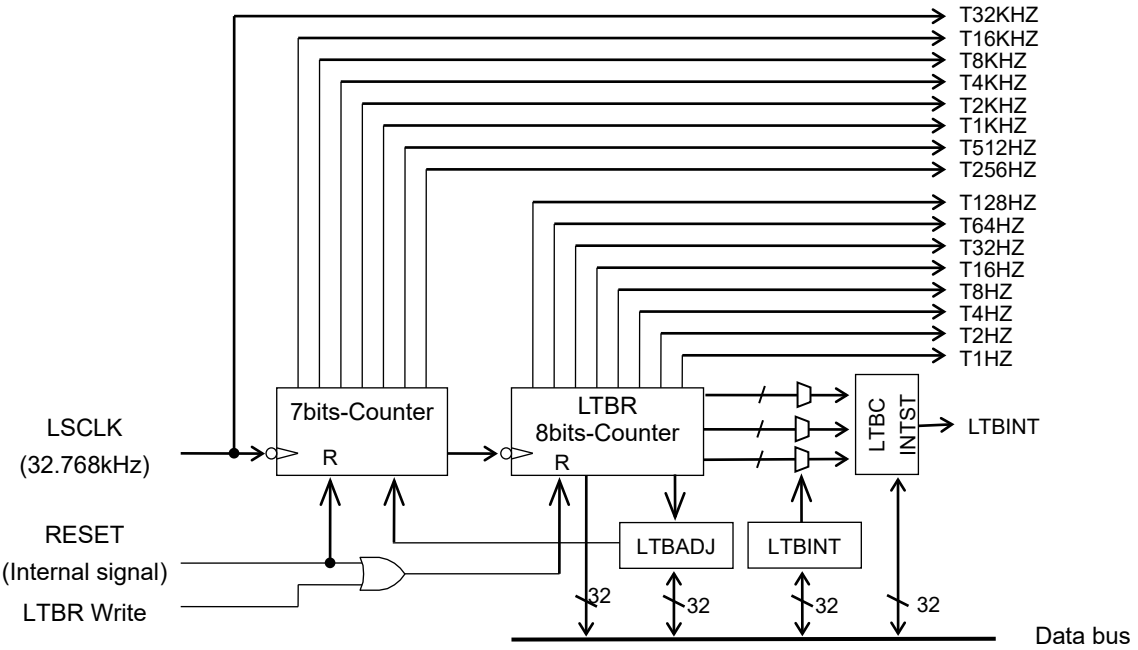
The time base counter generates base clocks for peripheral circuits, and generates interrupt periodically.

9.1.1. Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK).
- LTBC allows frequency adjustment (Adjustment range: Approx. -488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) by using the low-speed time base counter frequency adjustment registers (LTBADJ).
- 3clocks between 128Hz and 1Hz can be used as interrupt signal.

9.1.2. Configuration

Figure 9-1 show the configuration of a low-speed time base counter respectively.



LTBR : Low-speed time base counter register
LTBADJ : Low-speed time base counter frequency adjust register
LTBINT : Low-speed time base counter interrupt select register
LTBCINTST : Low-speed time base counter interrupt status register

Figure 9-1 Configuration of Low-Speed Time Base Counter (LTBC)

9.2. Description of Registers

9.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_2100	Low-speed time base counter register	LTBR	R/W	32	0x0000_0000
0x5C00_2104	Low-speed time base counter frequency adjustment register	LTBADJ	R/W	32	0x0000_0000
0x5C00_2108	Low-speed time base counter interrupt select resister	LTBINT	R/W	32	0x0000_0000
0x5C00_210C	Low-speed time base counter interrupt status register	LTBCINTST	R/W	32	0x0000_0000

9.2.2. Low-Speed Time Base Counter Register (LTBR)

Address: 0x5C00_2100
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter.
When write to LTBR, the content of LTBR becomes "0" regardless of the write data.

[Note]
LTBC interrupts may occur depending on the LTBR write timing (see 9.3.1 "Low-Speed Time Base Counter").

9.2.3. Low-Speed Time Base Counter Frequency Adjustment Register (LTBADJ)

Address: 0x5C00_2104
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	LADJ[10:0]										
Access	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
LTBADJ is a special function register (SFR) to set the frequency adjustment values of the low-speed time base clock.

[Description of Bits]
- **LADJ[10:0]** (bit 10 to 0)
  The LADJ[10:0] bits are used to adjust frequency.
  Adjustment range: Approx. –488ppm to +488ppm.
  Adjustment accuracy: Approx. 0.48ppm

  Frequency adjustment (Adjustment range: Approx. –488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) is possible for outputs of T8KHZ to T1HZ of LTBC by using the low-speed time base counter frequency adjust registers (LTBADJ).
  Table9-1 shows correspondence between the frequency adjustment values (LADJ) and adjustment ratio.

Table 9-1 Correspondence between Frequency Adjustment Values (LADJ) and Adjustment Ratio

LADJ10 to 0											Hexadecimal	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	–0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	–0.95
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	1	401H	–487.80
1	0	0	0	0	0	0	0	0	0	0	400H	–488.28

The adjustment values (LADJ[10:0]) to be set in LTBADJ can be obtained by using the following equations:

Adjustment value = Frequency adjustment ratio × 2097152 (decimal)
= Frequency adjustment ratio × 200000h (hexadecimal)

Example 1: When adjusting +15.0ppm (gaining time)
Adjustment value = +15.0ppm × 2097152 (decimal)
= $+15.0 \times 10^{-6} \times 2097152$
= +31.45728 (decimal)
≅ 01Fh (hexadecimal)

Example 2: When adjusting –25.5ppm (losing time)
Adjustment value = –25.5ppm × 2097152 (decimal)
= $-25.5 \times 10^{-6} \times 2097152$
= –53.477376 (decimal)
≅ 7CCh (hexadecimal)

[Note]
The low-speed clock (LSCLK) and the outputs of T32KHZ and T16KHZ of LTBC are not adjusted by the frequency adjust function.
The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the crystal oscillation (32.768kHz) due to temperature variations.

9.2.4. Low-Speed Time Base Counter Interrupt Select Register (LTBINT)

Address: 0x5C00_2108
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0888

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	LTI2S[3:0]				LTI1S[3:0]				LTI0S[3:0]			
Access	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
LTBINT is a special function register(SFR) which specify low speed time base clock which is used as an interrupt signal.

[Description of Bits]

- **LTI0S[3:0]** (bit 3 to 0)
  The bit specify an assignable clock to LTBINT0. Initial value is T128HZ.

- **LTI1S[3:0]** (bit 7 to 4)
  The bit specify an assignable clock to LTBINT1. Initial value is T16HZ.

- **LTI2S[3:0]** (bit 11 to 8)
  The bit specify an assignable clock to LTBINT2. Initical value is T2HZ.

LTInS[3]	LTInS[2]	LTInS[1]	LTInS[0]	Assignable clock
0	0	0	0	T128HZ
0	0	0	1	T64HZ
0	0	1	0	T32HZ
0	0	1	1	T16HZ
0	1	0	0	T8HZ
0	1	0	1	T4HZ
0	1	1	0	T2HZ
0	1	1	1	T1HZ
1	0	0	0	Not assigned
Other than above				Setting prohibited

* an interrupt may occur at setting.

9.2.5. Low-speed Time Base Counter Interrupt Status Register (LTBCINTST)

Address: 0x5C00_210C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	LTB INT2	LTB INT1	LTB INT0
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
LTBCINTST is a special function register(SFR) which indicates the cause of the interrupt.

[Description of Bits]

- **LTBCINT0** (bit 0)
  This bit is set to "1" when LTBINT0 interrupt request is generated. The LTBINT0 interrupt can be clear by writing "1" to this bit.

- **LTBCINT1** (bit 1)
  This bit is set to "1" when LTBINT1 interrupt request is generated. The LTBINT1 interrupt can be clear by writing "1" to this bit.

- **LTBCINT2** (bit 2)
  This bit is set to "1" when LTBINT2 interrupt request is generated. The LTBINT2 interrupt can be clear by writing "1" to this bit.

9.3. Description of Operation

9.3.1. Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
Three of LTBC interrupt are generated by falling edge of clock output which was assigned by the low-speed time base counter interrupt select register (LTBINT).
The T128HZ to T1HZ output of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 9-2 shows an example of program to read LTBR.

```
unsigned int ltbr_t;
do {
    ltbr_t = LTBR;              ; First read
}while(ltbr_t != LTBR);         ; Second read and compare
```

Figure 9-2 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". At this time, Interrupt occurs when clock is assigned to LTBC interrupt changing from "1" to "0". Therefore, when LTBR is reset, After prohibits each TBC interrupts of interrupt controller, LTBR is reset and the processing which clears LTBR interrupt request which occurred by reset is needed. Figure 9-3 shows the sequence to clear the LTBC interrupt request.

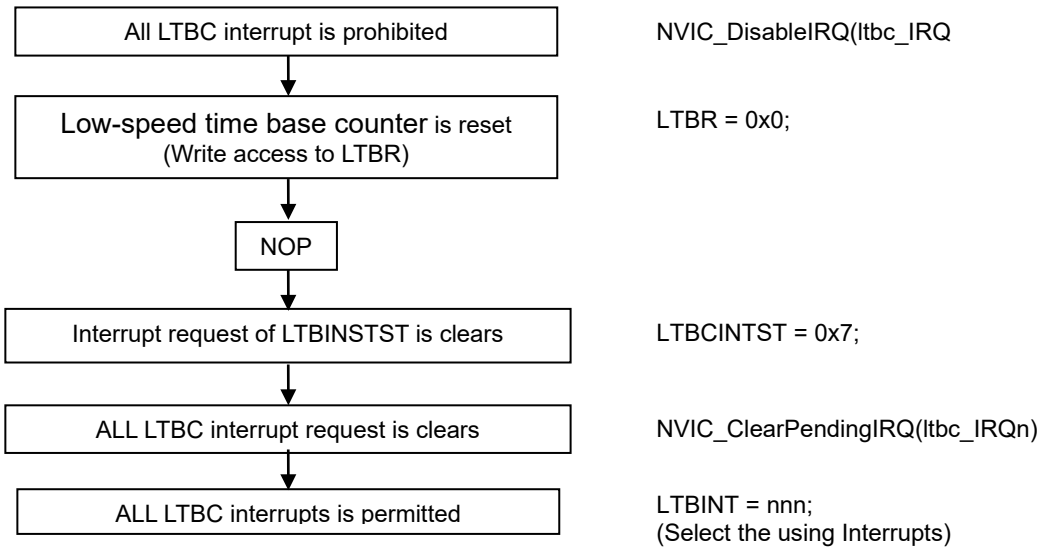


Figure 9-3 Sequence to Clear the LTBC Interrupt Request which Occurred by LTBR Reset

1CPU cycle is needed after LTBR interrupt occurs until LTBC interrupt request flag of interrupt controller is set. When LTBC interrupt request is cleared after the writing LTBR, Please do not put the order to clear request flag just after an order to write in LTBR at. Please clear request flag after placing NOP, and putting time.

Figure 9-4 shows interrupt generation timing of the time base counter output by writing to LTBR.

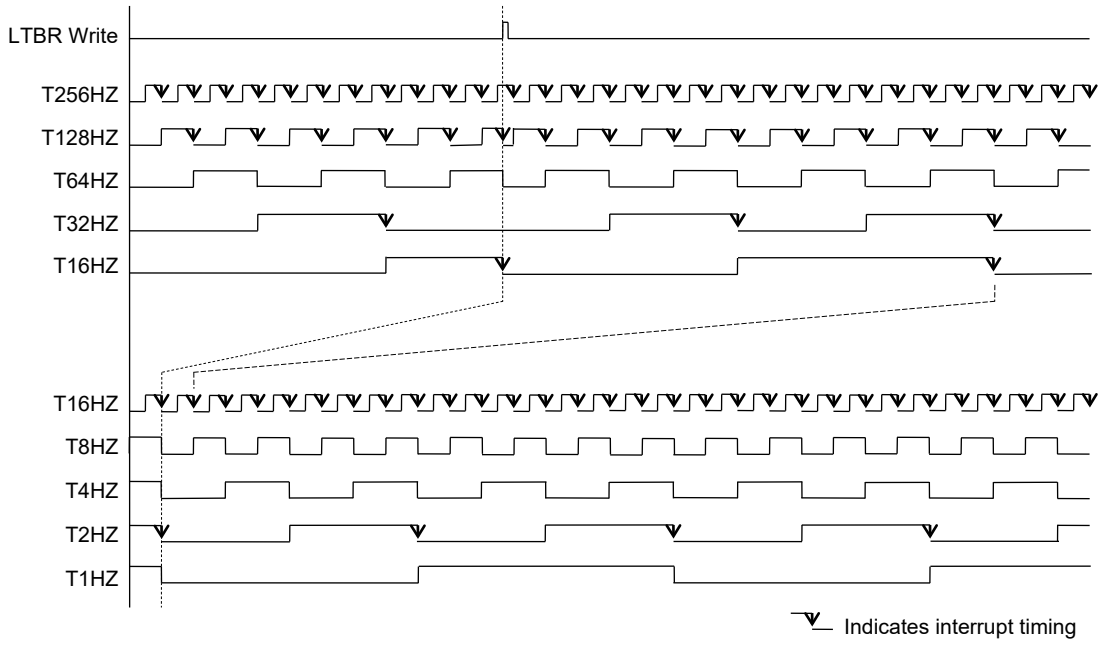


Figure 9-4 Interrupt Timing by Writing to LTBR

Chapter 10

Timers

10. Timers

10.1. Overview

This LSI includes 8 channels of 8 bit timers. A pair of 2 timers functions as 16 bit timer.

10.1.1. Features

- The timer interrupt (TMnINT, n=0 to 7) is generated when the values of timer counter register (TMnC, n=0 to7) and timer data register (TMnD, n=0 to 7) coincide.
- A timer configured by combining timer 0 and timer 1 or timer 2 and timer 3 or timer4 and timer 5 or timer 6 and timer 7 can be used as a 16 bit timer.
- Low-speed clock (LSCLK), high-speed clock (OSCLK), and external input(P36/P37/P56/P57) are selectable as timer clock(selectable clock is different every channel).
- Timer clock can be divided by 1, 2, 4, 8, 16, 32, and 64 by divider function.

10.1.2. Configuration

Figure 10-1 shows the configuration of the timers.

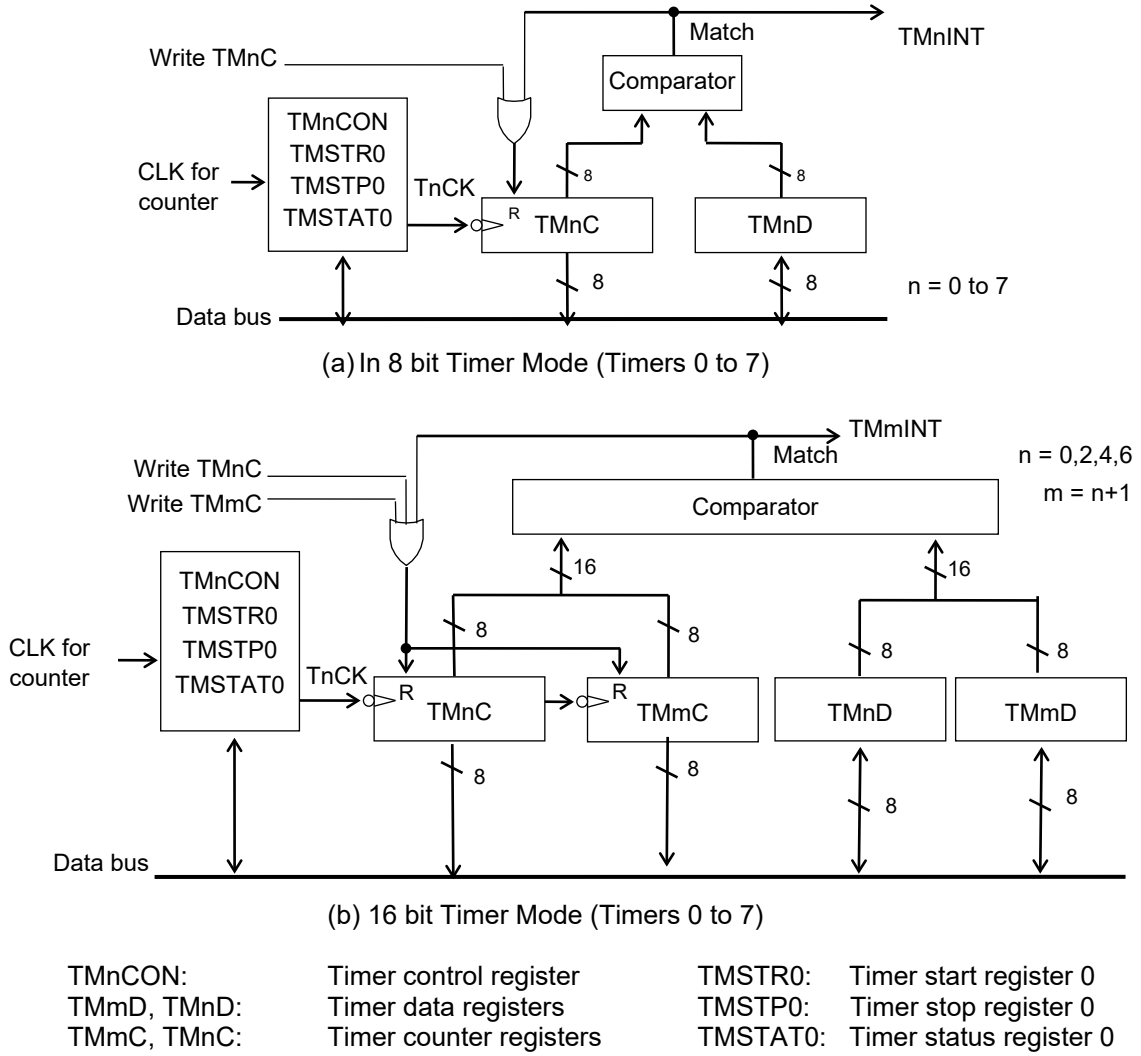


Figure 10-1 Configuration of Timers

Alternative counter clock of each channels are as below

8 bit timer mode

channel	Selectable clock
0	LSCLK/OSCLK
1	
2	LSCLK/OSCLK/external pin(P36)
3	LSCLK/OSCLK/external pin(P37)
4	LSCLK/OSCLK/external pin(P56)
5	LSCLK/OSCLK/external pin(P57)
6	LSCLK/OSCLK
7	

16 bit timer mode

channel	Selectable clock
0,1	LSCLK/OSCLK
2,3	LSCLK/OSCLK/external pin(P36)
4,5	LSCLK/OSCLK/external pin(P56)
6,7	LSCLK/OSCLK

10.2. Description of Registers

10.2.1. List of Registers

Ch	Address	Name	Symbol	R/W	Size	Initial value
0	0x5C00_1000	Timer 0 data register	TM0D	R/W	32	0x0000_00FF
	0x5C00_1004	Timer 0 counter register	TM0C	R/W	32	0x0000_0000
	0x5C00_1008	Timer 0 control register	TM0CON	R/W	32	0x0000_0000
1	0x5C00_1010	Timer 1 data register	TM1D	R/W	32	0x0000_00FF
	0x5C00_1014	Timer 1 counter register	TM1C	R/W	32	0x0000_0000
	0x5C00_1018	Timer 1 control register	TM1CON	R/W	32	0x0000_0000
2	0x5C00_1020	Timer 2 data register	TM2D	R/W	32	0x0000_00FF
	0x5C00_1024	Timer 2 counter register	TM2C	R/W	32	0x0000_0000
	0x5C00_1028	Timer 2 control register	TM2CON	R/W	32	0x0000_0000
3	0x5C00_1030	Timer 3 data register	TM3D	R/W	32	0x0000_00FF
	0x5C00_1034	Timer 3 counter register	TM3C	R/W	32	0x0000_0000
	0x5C00_1038	Timer 3 control register	TM3CON	R/W	32	0x0000_0000
4	0x5C00_1040	Timer 4 data register	TM4D	R/W	32	0x0000_00FF
	0x5C00_1044	Timer 4 counter register	TM4C	R/W	32	0x0000_0000
	0x5C00_1048	Timer 4 control register	TM4CON	R/W	32	0x0000_0000
5	0x5C00_1050	Timer 5 data register	TM5D	R/W	32	0x0000_00FF
	0x5C00_1054	Timer 5 counter register	TM5C	R/W	32	0x0000_0000
	0x5C00_1058	Timer 5 control register	TM5CON	R/W	32	0x0000_0000
6	0x5C00_1060	Timer 6 data register	TM6D	R/W	32	0x0000_00FF
	0x5C00_1064	Timer 6 counter register	TM6C	R/W	32	0x0000_0000
	0x5C00_1068	Timer 6 control register	TM6CON	R/W	32	0x0000_0000
7	0x5C00_1070	Timer 7 data register	TM7D	R/W	32	0x0000_00FF
	0x5C00_1074	Timer 7 counter register	TM7C	R/W	32	0x0000_0000
	0x5C00_1078	Timer 7 control register	TM7CON	R/W	32	0x0000_0000
0-7	0x5C00_10F0	Timer start register	TMSTR	W	32	0x0000_0000
	0x5C00_10F4	Timer stop register	TMSTP	W	32	0x0000_0000
	0x5C00_10F8	Timer status register	TMSTAT	R	32	0x0000_0000

10.2.2. Timer n Data Register (TMnD : n=0, 2, 4, 6)

Address: 0x5C00_1000 (TM0D), 0x5C00_1020 (TM2D)
0x5C00_1040 (TM4D), 0x5C00_1060 (TM6D)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	TnD[15:8]								TnD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMnD (n=0, 2, 4, 6) is a special function register (SFR) to set the value to be compared with the timer n counter register (TMnC) value.
The TMnD[7:0] is compared with the TMnC[7:0] in 8bit timer mode, and the TMnD[15:0] is compared with the TMnC[15:0] in 16bit timer mode.
In 16bit timer mode, TnD[15:8] is able to be accessed and the initial value is 0xFF.

[Note]
Set TMnD when the timer stops.
When "0x00" is written in TMnD, TMnD is set to "0x01" (8bit timer mode).
When "0x0000" is written in TMnD, TMnD is set to "0x0001" (16bit timer mode).

10.2.3. Timer m Data Register (TMmD : m=1, 3, 5, 7)

Address: 0x5C00_1010 (TM1D), 0x5C00_1030 (TM3D)
0x5C00_1050 (TM5D), 0x5C00_1070 (TM7D)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_00FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	TmD[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMmD (m=1, 3, 5, 7) is a special function register (SFR) to set the value to be compared with the timer m counter register (TMmC) value.
The TmD[7:0] is compared with the TmC[7:0] in 8bit timer mode. The value of TMmD[7:0] is displayed TnD[15:8] (n=0, 2, 4, 6).

[Note]
Set TMmD when the timer stops.
When "0x00" is written in TMmD, TMmD is set to "0x01" .

10.2.4. Timer n Counter Register (TMnC : n=0, 2, 4, 6)

Address: 0x5C00_1004(TM0C), 0x5C00_1024(TM2C),
0x5C00_1044(TM4C), 0x5C00_1064(TM6C)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	TnC[15:8]								TnC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMnC (n=0, 2, 4, 6) is a special function register (SFR) that functions as an 8/16 bit binary counter.
When some data is written to TMnC, TMnC is cleared to "0x00".
In 16 bit timer mode, even if write to either TMnC timer counter or TM(n+1)C timer counter, both timer counters are cleared to "0x00".

Table 10-1 shows whether a TMnC read during timer operation is enabled or disabled for each condition of the timer clock and system clock.

Table 10-1 TMnC Read Enable condition during Timer Operation

System clock SYSCLK	Timer clock TnCK
LSCLK	LSCLK and divided LSCLK
HSCLK	OSCLK and divided OSCLK However, when frequency of SYSCLK is more than TnCK

[Note]
When using the 16bit timer configured cascading two 8bit timers and also if you restart the timer after the timer is stopped by the software or automatically stopped in one shot timer mode, always reset the timer counter register(TMmC, TMnC) to "0000h" by making a write operation to the register with the equal to "0000h".

10.2.5. Timer m Counter Register (TMmC : n=1, 3, 5, 7)

Address: 0x5C00_1014(TM1C), 0x5C00_1034(TM3C),
0x5C00_1054(TM5C), 0x5C00_1074(TM7C)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	TmC[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMmC (m=1, 3, 5, 7) is a special function register (SFR) that functions as an 8 bit binary counter.
When some data is written to TMmC, TMmC is cleared to "0x00".
In 16 bit timer mode, even if write to either TMnC timer counter or TM(n+1)C timer counter, both timer counters are cleared to "0x00".

Table 10-2 shows whether a TMnC read during timer operation is enabled or disabled for each condition of the timer clock and system clock.

Table 10-2 TMnC Read Enable condition during Timer Operation

System clock SYSCLK	Timer clock TmCK
LSCLK	LSCLK and divided LSCLK
HSCLK	OSCLK and divided OSCLK However, when frequency of SYSCLK is more than TnCK

[Note]
When using the 16bit timer configured cascading two 8bit timers and also if you restart the timer after the timer is stopped by the software or automatically stopped in one shot timer mode, always reset the timer counter register(TMmC, TMnC) to "0000h" by making a write operation to the register with the equal to "0000h".

10.2.6. Timer n Control Register (TMnCON : n= 0, 2, 4, 6)

Address: 0x5C00_1008(TM0CON), 0x5C00_1028(TM2CON),
0x5C00_1048(TM4CON), 0x5C00_1068(TM6CON)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	TnmM16	–*	–*	–*	TnOST	–*	TnDIV[2:0]			–*	–*	TnCS[1:0]*1	
Access	–	–	–	R/W	–	–	–	R/W	–	R/W	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.
*1: T0CS[1] bit and T6CS[1] bit are fixed as "0".

[Description of Register]
Timer control register(TMnCON) is a special function register(SFR) to set timer modes.
Timer control register needs to be set while target timer is stop(TMSTAT register TnSTAT state is "0")

[Description of Bits]
- **TnCS[1:0]** (bit 1 to 0)
  TnCS[1:0] bits are used for selecting the operation clock of timer n(timer m). The clock assigned by TnCS[1:0] is used as the operation clock at 16bit timer mode.

TnCS[1: 0]		Description			
		Timer 6	Timer 4	Timer 2	Timer 0
0	0	LSCLK (initial value)			
0	1	OSCLK			
1	0	Prohibited	LSCLK		Prohibited
1	1	Prohibited	External clock (P56)	External clock (P36)	Prohibited

T0CS[1] bit and T6CS[1] bit are fixed as "0".

- **TnDIV[2:0]** (bit 6 to 4)
  TnDIV[2:0] bits are used for selecting dividing rate of operation clock .
  The dividing rate is assigned by TnDIV[2:0] at 16bit timer mode.

TnDIV[2]	TnDIV[1]	TnDIV[0]	Description
0	0	0	Clock assigned by TnCS[1:0] (initial value)
0	0	1	Clock assigned by TnCS[1:0] divide by 2
0	1	0	Clock assigned by TnCS[1:0] divide by 4
0	1	1	Clock assigned by TnCS[1:0] divide by 8
1	0	0	Clock assigned by TnCS[1:0] divide by 16
1	0	1	Clock assigned by TnCS[1:0] divide by 32
1	1	0	Clock assigned by TnCS[1:0] divide by 64
1	1	1	No use(Assigned clock by TnCS[1:0])

- **TnOST** (bit 8)
  The TnOST is used for selecting a normal timer mode or a one-shot timer mode.
  In 16bit timer mode, Timer function mode is selected by TnOST (n=0, 2, 4, 6).

TnOST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

- **TnmM16** (bit 12)
  The TnmM16 bit is used for selecting a 16 bit timer mode. When the TnmM16 is set to 1, two timers are connected and function as a 16 bit timer. When the TnmM16 bit is set to "0", two each timers function 8bit timer.

TnmM16	Description
0	8 bit timer mode (initial value)
1	16 bit timer mode

The below table shows the TnmM16 bit of each timer control register, connect timer, interrrupts which is used.

Timer control register	TnmM16 bit	Connect timer (H-L)	interrupt
TM0CON	T01M16	Timer1 – Timer0	Timer1
TM2CON	T23M16	Timer3 – Timer2	Timer3
TM4CON	T45M16	Timer5 – Timer4	Timer5
TM6CON	T67M16	Timer7 – Timer6	Timer7

10.2.7. Timer m Control Register (TMmCON : m= 1, 3, 5, 7)

Address: 0x5C00_1018(TM1CON), 0x5C00_1038(TM3CON),
0x5C00_1058(TM5CON), 0x5C00_1078(TM7CON)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	TmOST	–*	TmDIV[2:0]			–*	–*	TmCS[1:0]*1	
Access	–	–	–	–	–	–	–	R/W	–	R/W	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.
*1: T1CS[1] bit and T7CS[1] bit are fixed as "0".

[Description of Register]
Timer control register(TMmCON) is a special function register(SFR) to set timer modes.
Timer control register needs to be set while target timer is stop(TMSTAT register TmSTAT state is "0")

[Description of Bits]
- **TmCS[1:0]** (bit 1 to 0)
  TmCS[1:0] bits are used for selecting the operation clock of timer n(timer m). The clock assigned by TnCS[1:0] is used as the operation clock at 16bit timer mode.

TmCS[1: 0]		Description			
		Timer 6	Timer 4	Timer 2	Timer 0
0	0	LSCLK (initial value)			
0	1	OSCLK			
1	0	Prohibited	LSCLK		Prohibited
1	1	Prohibited	External clock (P57)	External clock (P37)	Prohibited

T1CS[1] bit and T7CS[1] bit are fixed as "0".

- **TmDIV[2:0]** (bit 6 to 4)
  TmDIV[2:0] bits are used for selecting dividing rate of operation clock .
  The dividing rate is assigned by TnDIV[2:0] at 16bit timer mode.

TmDIV[2]	TmDIV[1]	TmDIV[0]	Description
0	0	0	Clock assigned by TmCS[1:0] (initial value)
0	0	1	Clock assigned by TmCS[1:0] divide by 2
0	1	0	Clock assigned by TmCS[1:0] divide by 4
0	1	1	Clock assigned by TmCS[1:0] divide by 8
1	0	0	Clock assigned by TmCS[1:0] divide by 16
1	0	1	Clock assigned by TmCS[1:0] divide by 32
1	1	0	Clock assigned by TmCS[1:0] divide by 64
1	1	1	No use(Assigned clock by TmCS[1:0])

- **TmOST** (bit 8)
  The TmOST is used for selecting a normal timer mode or a one-shot timer mode.
  In 16bit timer mode, Timer function mode is selected by TnOST (n=0, 2, 4, 6).

TmOST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

10.2.8. Timer Start Register (TMSTR)

Address: 0x5C00_10F0
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	T7RUN	T6RUN	T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN
Access	–	–	–	–	–	–	–	–	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMSTR is a special function (SFR) to start the counter of timer 0 to timer 7.

[Description of Bits]
- **TnRUN** (bit n : n= 0 to 7)
  TnRUN is the control bit of Timer n count start.
  In initial state after power on, the counter is stopped.
  Timer n starts to count up by writing TnRUN bit to "1".
  Timer m and (m+1) start to count up at 16bit timer mode. (m = 0, 2, 4, 6)

TnRUN	Description
0	Keep current status (initial)
1	Start count

	8 bit timer mode	16 bit timer mode
T0RUN	For timer0	For timer0 and 1
T1RUN	For timer1	Setting prohibited
T2RUN	For timer2	For timer2 and 3
T3RUN	For timer3	Setting prohibited
T4RUN	For timer4	For timer4 and 5
T5RUN	For timer5	Setting prohibited
T6RUN	For timer6	For timer6 and 7
T7RUN	For timer7	Setting prohibited

10.2.9. Timer Stop Register (TMSTP)

Address: 0x5C00_10F4
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	T7 STP	T6 STP	T5 STP	T4 STP	T3 STP	T2 STP	T1 STP	T0 STP
Access	–	–	–	–	–	–	–	–	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMSTP is a special function (SFR) to stop the counter of a timer 0 to timer 7.

[Description of Bits]

- **TnSTP** (bit n : n = 0 to 7)
  TnSTP is the control bit of Timer n count stop.
  The counter is stopped at initial state after power on. "1" setting while count stop is invalid.
  Timer n stops counting up by setting TnSTP bit to "1".
  Timer m and (m+1) stop counting up at 16bit timer mode. (m = 0, 2, 4, 6)

TnSTP	Description
0	Keep current status (initial)
1	Stop count

	8 bit timer mode	16 bit timer mode
T0STP	For timer0	For timer0 and 1
T1STP	For timer1	Setting prohibited
T2STP	For timer2	For timer2 and 3
T3STP	For timer3	Setting prohibited
T4STP	For timer4	For timer4 and 5
T5STP	For timer5	Setting prohibited
T6STP	For timer6	For timer6 and 7
T7STP	For timer7	Setting prohibited

10.2.10. Timer Status Register (TMSTAT)

Address: 0x5C00_10F8
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	T7 STAT	T6 STAT	T5 STAT	T4 STAT	T3 STAT	T2 STAT	T1 STAT	T0 STAT
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
TMSTAT is a special function (SFR) to indicate the status of timer 0 to timer 7.

[Description of Bits]
- **TnSTAT** (bit n : n = 0 to 7)
  TnSTAT bit indicate timer n status(counting/stopping) .

TnSTAT	Description
0	Stopping(initial value)
1	counting

	8 bit timer mode	16 bit timer mode
T0STAT	For timer0	For timer0 and 1
T1STAT	For timer1	Not used (kept value "0".)
T2STAT	For timer2	For timer2 and 3
T3STAT	For timer3	Not used (kept value "0".)
T4STAT	For timer4	For timer4 and 5
T5STAT	For timer5	Not used (kept value "0".)
T6STAT	For timer6	For timer6 and 7
T7STAT	For timer7	Not used (kept value "0".)

10.3. Description of operation

10.3.1. Normal timer mode operation

When the TnRUN bit of timer n register (TMSTR) are set to 1, The timer counters(TMnC) is in operation state(TnSTAT ="1") by the first falling edge of the timer clock(TnCK) that are selected by the Timer control register(TMnCON), and start to count up by the second falling edge.
When the count value of TMnC coincide with the timer data register (TMnD), timer interrupt (TMnINT) occurs on the next falling edge of timer clock, at same time TMnC are reset to "0x00" and continues incremental count.

When the TnSTP bit are set to "1", TMnC stop a count after one fall count of the timer clock (TnCK) , and TnSTAT bit of timer status register (TMSTAT) becomes "0".

When the TnRUN bit are set to "1" again, TMn restart an incremental count from the previous values. To initialize TMnC to "0x00", perform write operation in TMnC.

The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n=0\text{-}7)$$

TMnD: Timer 0 to 7 data register (TMnD) setting value (0x01 to 0xFF)
TnCK: Clock frequency selected by the Timer n control register (TMnCON)

After TnRUN bit are set to "1", timer counter are synchronized by the timer clock and counting starts so that an error of a maximum of 1 clock period occurs until the first timer interrupt. The timer interrupt periods from the second time are constant.
Figure 10-2 shows the normal timer mode operation timing diagram of Timer 0 to 7

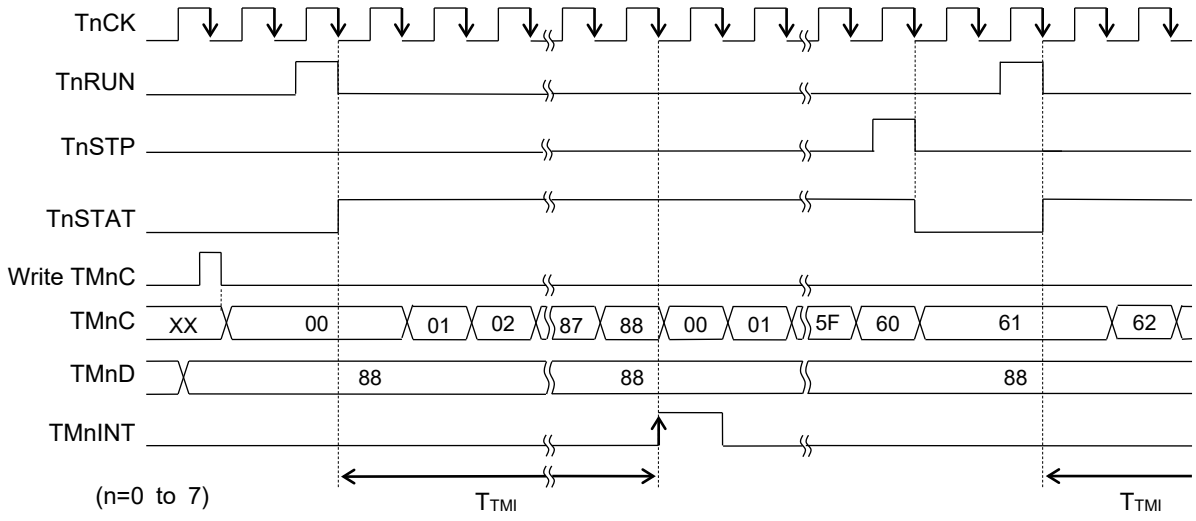


Figure 10-2 Normal Timer Mode Operation Timing Diagram of Timer 0 to 7

[Note]
Count stop and Timer interrupt may occour at same time because Counter stop operation is perfomed synclonizing with count operation.

10.3.2. One shot timer mode operation

When TMnCON register TnOST bit set to "1", Timer operate one-shot timer mode.
In one-shot timer mode, When the count value (TMnC) and the timer 0 to 7 data register (TMnD) coincide, TnRUN bit are cleared automatically .

Figure 10-3 shows the one-shot timer mode operation timing diagram

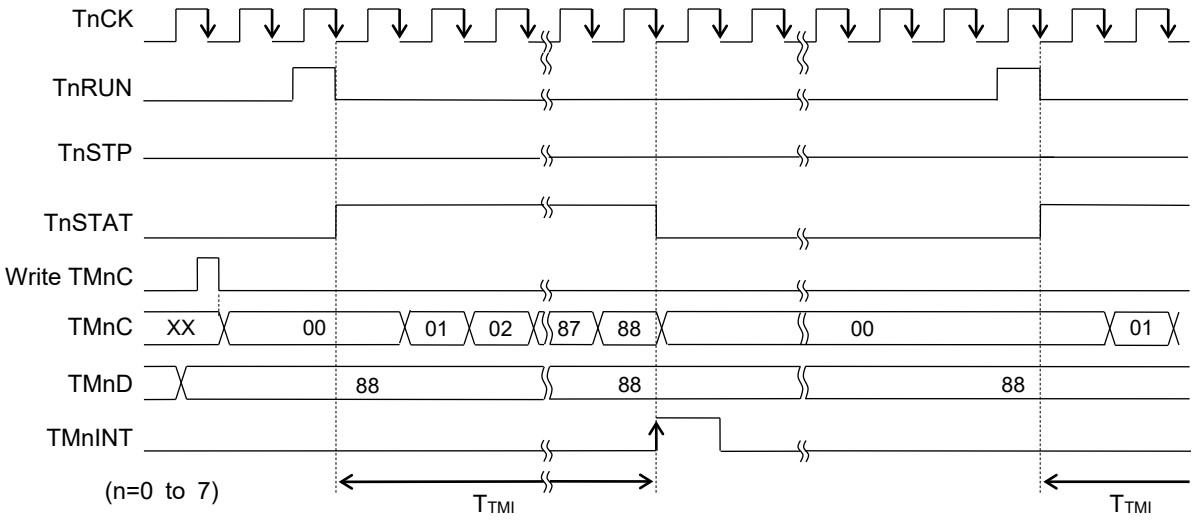


Figure 10-3 One-Shot Timer Mode Operation Timing Diagram

10.3.3. 16bit timer mode

Two of 8bit timer can be used as 16bit timer by TMnCON(N=0,2,4,6) register TnM16 bit.
The following shows a corresponding list of timer-channels and related registers.

Channel / Control	16bit timer 0,1	16bit timer 2,3	16bit timer 4,5	16bit timer 6,7
Data register	TM0D	TM2D	TM4D	TM6D
Counter register	TM0C	TM2C	TM4C	TM6C
Controll register	TM0CON	TM2CON	TM4CON	TM6CON
RUN bit	T0RUN	T2RUN	T4RUN	T6RUN
STOP bit	T0STP	T2STP	T4STP	T6STP
STAT bit	T0STAT	T2STAT	T4STAT	T6STAT
Interrupt	TM1INT	TM3INT	TM5INT	TM7INT

Chapter 11

Function Timer(FTM)

11. Function Timer (FTM)

11.1. General Description

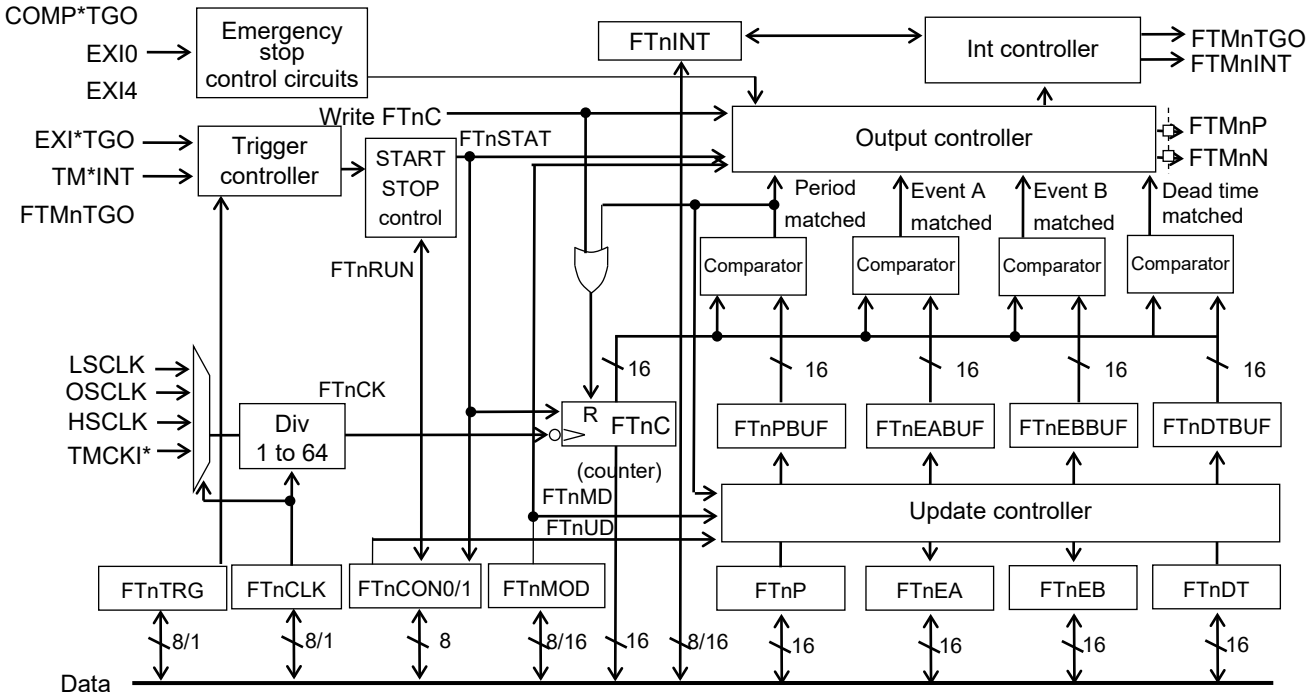
FTM is a 16 bit function timer with the capture and PWM functions in addition to the timer function. It can be started/stopped using an external input signal and a signal from another timer as a trigger.
The LSI includes four channels of the function timer.

11.1.1. Features

- Equipped with the timer/capture/PWM functions using a 16 bit counter
- 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input clock selectable as timer clock
- The timer output signal can be switched between the positive and negative logics
- Duty interrupt and coincident interrupt with the setting value as well as the cyclic interrupt generated
- Equipped with one-shot mode
- An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3ϕ)
- An external input can generate an emergency stop and emergency stop interrupt.
- Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output
- The capture function can measure the duty/cycle of the input signal
- Interrupt source to be notified can be set

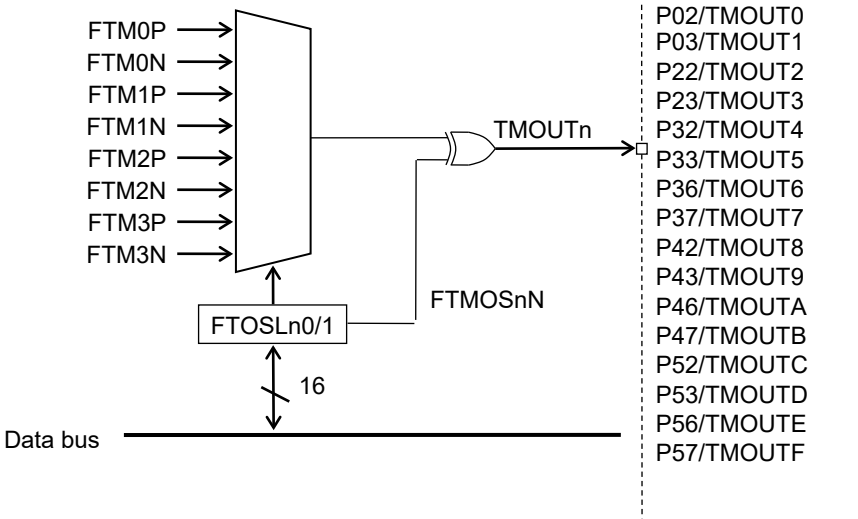
11.1.2. Configuration

Figure 11-1 shows the configuration of the FTM circuit.



FTnP	: FTMn period register	FTnPBUF	: FTMn period buffer
FTnEA/B	: FTMn event A/B register	FTnEA/BBUF	: FTMn event A/B buffer
FTnDT	: FTMn dead time register	FTnDTBUF	: FTMn dead time buffer
FTnC	: FTMn counter register	FTnMOD	: FTMn mode register
FTnCON0/1	: FTMn control register 0,1	FTnCLK	: FTMn clock register
FTnTRG	: FTMn trigger register		
FTnINTE/S/C	: FTMn interrupt enable/status/clear register		

Figure 11-1 (a) Configuration of Circuit



FTOSLn0/1 : FTM output selection register n0/1 (n = 0 to F)

Figure 11-1 (b) Configuration of FTM Output Selection Circuit

11.1.3. List of Pins

Pin Name	I/O	Function
TMCKI0-7	I	External clock input
TMOUT0-F	O	Timer output (selectable from FTM 0 to 3)

11.2. Description of Registers

11.2.1. List of Registers

Ch	Address	Name	Symbol	R/W	Size	Initial value
0	0x5C00_3000	FTM0 period register	FT0P	R/W	32	0x0000_FFFF
	0x5C00_3004	FTM0 event register A	FT0EA	R/W	32	0x0000_0000
	0x5C00_3008	FTM0 event register B	FT0EB	R/W	32	0x0000_0000
	0x5C00_300C	FTM0 dead time register	FT0DT	R/W	32	0x0000_0000
	0x5C00_3010	FTM0 counter register	FT0C	R/W	32	0x0000_0000
	0x5C00_3014	FTM0 control register 0	FT0CON0	R/W	32	0x0000_0000
	0x5C00_3018	FTM0 control register 1	FT0CON1	R/W	32	0x0000_0000
	0x5C00_301C	FTM0 mode register	FT0MOD	R/W	32	0x0000_0000
	0x5C00_3020	FTM0 clock register	FT0CLK	R/W	32	0x0000_0000
	0x5C00_3024	FTM0 trigger register	FT0TRG	R/W	32	0x0000_0000
	0x5C00_3030	FTM0 interrupt enable register	FT0INTE	R/W	32	0x0000_0000
	0x5C00_3034	FTM0 interrupt status register	FT0INTS	R	32	0x0000_0000
	0x5C00_3038	FTM0 interrupt clear register	FT0INTC	W	32	0x0000_0000
1	0x5C00_3100	FTM1 period register	FT1P	R/W	32	0x0000_FFFF
	0x5C00_3104	FTM1 event register A	FT1EA	R/W	32	0x0000_0000
	0x5C00_3108	FTM1 event register B	FT1EB	R/W	32	0x0000_0000
	0x5C00_310C	FTM1 dead time register	FT1DT	R/W	32	0x0000_0000
	0x5C00_3110	FTM1 counter register	FT1C	R/W	32	0x0000_0000
	0x5C00_3114	FTM1 control register 0	FT1CON0	R/W	32	0x0000_0000
	0x5C00_3118	FTM1 control register 1	FT1CON1	R/W	32	0x0000_0000
	0x5C00_311C	FTM1 mode register	FT1MOD	R/W	32	0x0000_0000
	0x5C00_3120	FTM1 clock register	FT1CLK	R/W	32	0x0000_0000
	0x5C00_3124	FTM1 trigger register	FT1TRG	R/W	32	0x0000_0000
	0x5C00_3130	FTM1 interrupt enable register	FT1INTE	R/W	32	0x0000_0000
	0x5C00_3134	FTM1 interrupt status register	FT1INTS	R	32	0x0000_0000
	0x5C00_3138	FTM1 interrupt clear register	FT1INTC	W	32	0x0000_0000
2	0x5C00_3200	FTM2 period register	FT2P	R/W	32	0x0000_FFFF
	0x5C00_3204	FTM2 event register A	FT2EA	R/W	32	0x0000_0000
	0x5C00_3208	FTM2 event register B	FT2EB	R/W	32	0x0000_0000
	0x5C00_320C	FTM2 dead time register	FT2DT	R/W	32	0x0000_0000
	0x5C00_3210	FTM2 counter register	FT2C	R/W	32	0x0000_0000
	0x5C00_3214	FTM2 control register 0	FT2CON0	R/W	32	0x0000_0000
	0x5C00_3218	FTM2 control register 1	FT2CON1	R/W	32	0x0000_0000
	0x5C00_321C	FTM2 mode register	FT2MOD	R/W	32	0x0000_0000
	0x5C00_3220	FTM2 clock register	FT2CLK	R/W	32	0x0000_0000
	0x5C00_3224	FTM2 trigger register	FT2TRG	R/W	32	0x0000_0000
	0x5C00_3230	FTM2 interrupt enable register	FT2INTE	R/W	32	0x0000_0000
	0x5C00_3234	FTM2 interrupt status register	FT2INTS	R	32	0x0000_0000
	0x5C00_3238	FTM2 interrupt clear register	FT2INTC	W	32	0x0000_0000
3	0x5C00_3300	FTM3 period register	FT3P	R/W	32	0x0000_FFFF
	0x5C00_3304	FTM3 event register A	FT3EA	R/W	32	0x0000_0000
	0x5C00_3308	FTM3 event register B	FT3EB	R/W	32	0x0000_0000
	0x5C00_330C	FTM3 dead time register	FT3DT	R/W	32	0x0000_0000
	0x5C00_3310	FTM3 counter register	FT3C	R/W	32	0x0000_0000
	0x5C00_3314	FTM3 control register 0	FT3CON0	R/W	32	0x0000_0000
	0x5C00_3318	FTM3 control register 1	FT3CON1	R/W	32	0x0000_0000
	0x5C00_331C	FTM3 mode register	FT3MOD	R/W	32	0x0000_0000

Ch	Address	Name	Symbol	R/W	Size	Initial value
	0x5C00_3320	FTM3 clock register	FT3CLK	R/W	32	0x0000_0000
	0x5C00_3324	FTM3 trigger register	FT3TRG	R/W	32	0x0000_0000
	0x5C00_3330	FTM3 interrupt enable register	FT3INTE	R/W	32	0x0000_0000
	0x5C00_3334	FTM3 interrupt status register	FT3INTS	R	32	0x0000_0000
	0x5C00_3338	FTM3 interrupt clear register	FT3INTC	W	32	0x0000_0000
0-3	0x5C00_3F00	FTM output select register 0	FTOSL0	R/W	32	0x0000_0000
	0x5C00_3F04	FTM output select register 4	FTOSL4	R/W	32	0x0000_0000
	0x5C00_3F08	FTM output select register 8	FTOSL8	R/W	32	0x0000_0000
	0x5C00_3F0C	FTM output select register C	FTOSLC	R/W	32	0x0000_0000

11.2.2. FTMn Period Register (FTnP : n=0,1,2,3)

Address: 0x5C00_3000(FT0P), 0x5C00_3100(FT1P), 0x5C00_3200(FT2P), 0x5C00_3300(FT3P)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FTnP[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnP is a special function register (SFR) used to set the cycle (clock count of one cycle) of FTMn.
The valid range is 0x0001 to 0xFFFF (clock count: 2 to 65536).
Set this register after setting the operation mode using FTnMD.

[Description of Bits]

- **FTnP[15:0]** (bit 15 to 0)

FTnMD	FTnP[15:0]	Description
TIMER CAPTURE PWM1 PWM2	0x0001-0xFFFF	Set one period to FTnP setting value + 1 clock.

[Note]
When 0x0000 is written to this register, one period is set to 2 clocks. The read value is 0000H.

11.2.3. FTMn Event Register A (FTnEA : n=0,1,2,3)

Address: 0x5C00_3004(FT0EA), 0x5C00_3104(FT1EA), 0x5C00_3204(FT2EA), 0x5C00_3304(FT3EA)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FTnEA[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnEA is a special function register (SFR) used to set the event timing of FTMn or indicate the captured data.
Set this register after setting the operation mode using FTnMD. In the CAPTURE mode, this is a read-only register. It cannot be written.

[Description of Bits]

- **FTnEA[15:0]** (bit 15 to 0)

FTnMD	FTnEA[15:0]	Description
TIMER	0x0000-0xFFFF	Set the count value to generate an interrupt. (interrupt timing is FTnEA setting value + 1) This value must be less than the period register FTnP.
CAPTURE	0x0000-0xFFFF	The captured count value is stored. When it is read, FTnFLGA/FTnISA is cleared. In the CAPTURE mode, writing to FTnEA is disabled.
PWM1	0x0000-0xFFFF	Set the duty of PWM output FTMnP of FTMn.
PWM2	0x0000-0xFFFF	Set the duty of PWM output FTMnP and FTMnN of FTMn.

11.2.4. FTMn Event Register B (FTnEB : n=0,1,2,3)

Address: 0x5C00_3008(FT0EB), 0x5C00_3108(FT1EB), 0x5C00_3208(FT2EB), 0x5C00_3308(FT3EB)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FTnEB[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnEB is a special function register (SFR) used to set the event timing of FTMn or indicate the captured data.
Set this register after setting the operation mode using FTnMD.
In the CAPTURE mode, this is a read-only register. It cannot be written.

[Description of Bits]

- **FTnEB[15:0]** (bit 15 to 0)

FTnMD	FTnEB[15:0]	Description
TIMER	0x0000-0xFFFF	Set the count value to generate an interrupt. (interrupt timing is FTnEB setting value + 1) This value must be less than the period register FTnP.
CAPTURE	0x0000-0xFFFF	The captured count value is stored. When it is read, FTnFLGB/FTnISB is cleared. In the CAPTURE mode, writing to FTnEB is disabled.
PWM1	0x0000-0xFFFF	Set the duty of PWM output FTMnN of FTMn.
PWM2	*	Set FTnIEB/FTnIOB to 0 in this mode.

11.2.5. FTMn Dead Time Register (FTnDT : n=0,1,2,3)

Address: 0x5C00_300C(FT0DT), 0x5C00_310C(FT1DT), 0x5C00_320C(FT2DT), 0x5C00_330C(FT3DT)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FTnDT[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnDT is a special function register (SFR) used to set the DeadTime of the timer output.
Set this register after setting the operation mode using FTnMD.

[Description of Bits]

- **FTnDT[15:0]** (bit 15 to 0)

FTnMD	FTnDT[15:0]	Description
TIMER PWM1/2	0x0000-0xFFFF	Set DeadTime of timer output (the dead-time width is FTnDT setting value + 1) This bit is enable when FTnDTEN bit of FTnMOD register is set to "1".
CAPTURE	*	This register is disabled

11.2.6. FTMn Counter Register (FTnC : n=0,1,2,3)

Address: 0x5C00_3010(FT0C), 0x5C00_3110(FT1C), 0x5C00_3210(FT2C), 0x5C00_3310(FT3C)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FTnC[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnC is a special function register (SFR) used to indicate the counter value of FTMn.
When writing to this register, the counter is cleared to "0x0000".
This register should be accessed while the counter is stopped.

11.2.7. FTMn Control Register 0 (FTnCON0 : n=0,1,2,3)

Address: 0x5C00_3014(FT0CON0), 0x5C00_3114(FT1CON0),
0x5C00_3214(FT2CON0), 0x5C00_3314(FT3CON0)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	FTnSDN	_*	_*	_*	FTnEMGEN	_*	_*	_*	FTnTGEN	_*	_*	_*	FTnRUN
Access	–	–	–	R/W	–	–	–	R/W	–	–	–	R/W	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnCON0 is a special function register (SFR) used to set the function of FTMn.

[Description of Bits]

- **FTnRUN** (bit 0)
  Stop/start counting of FTMn by the software.

FTnMD	FTnRUN	Description
TIMER CAPTURE PWM1/2	0	Stop counting (initial value)
	1	Start counting/during counting

- **FTnTGEN** (bit 4)
  Allow stopping/starting counting by a trigger event.

FTnMD	FTnGTEN	Description
TIMER CAPTURE PWM1/2	0	Trigger operation disabled (initial value)
	1	Trigger operation enabled

- **FTnEMGEN** (bit 8)
  Allow emergency stop of FTMn.

FTnMD	FTnEMGEN	Description
TIMER PWM1/2	0	Emergency stop disabled (initial value)
	1	Emergency stop enabled
CAPTURE	*	This bit is disabled.

- **FTnSDN** (bit 12)
  Mask the output of FTMn to L.

FTnMD	FTnSDN	Description
TIMER PWM1/2	0	Release the output mask (initial value)
	1	Set the output mask (fix output to L).
CAPTURE	*	This bit is disabled.

11.2.8. FTMn Control Register 1 (FTnCON1 : n=0,1,2,3)

Address: 0x5C00_3018(FT0CON1), 0x5C00_3118(FT1CON1),
0x5C00_3218(FT2CON1), 0x5C00_3318(FT3CON1)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	FTnSTAT	FTnFLGC	FTnFLGB	FTnFLGA	_*	_*	_*	FTnUD
Access	–	–	–	–	–	–	–	–	R	R	R	R	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnCON1 is a special function register (SFR) used to set the function of FTMn.

[Description of Bits]

- **FTnUD** (bit 0)
  This bit is used to update FTnP, FTnEA, FTnEB and FTnDT of FTMn during operation. To update FTnP, FTnEA, FTnEB and FTnDT, write "1" to this bit after setting these registers. Writing "1" transfers the setting values to the internal buffer of FTnP, FTnEA, FTnEB and FTnDT at the same time. When the transfer completes, this bit is cleared automatically.

FTnMD	FTnUD	Description
TIMER CAPTURE PWM1/2	0	Update completed (initial value)
	1	Requesting update

[Note]
To write "1" to this bit (to update register value), do so after reading this bit and confirm that the value is "0" (update is completed).

- **FTnFLGA** (bit 4)
  Indicates the state of event timing A of FTMn.

FTnMD	FTnFLGA	Description
TIMER PWM1/2	0	Counter value < Value of event register A (initial value)
	1	Counter value ≥ Value of event register A
CAPTURE	0	Capture data not available
	1	Capture data available. When FTnEA is read, it is cleared

- **FTnFLGB** (bit 5)
  Indicates the state of event timing B of FTMn.

FTnMD	FTnFLGB	Description
TIMER PWM1/2	0	Counter value < Value of event register B (initial value)
	1	Counter value ≥ Value of event register B
CAPTURE	0	Capture data not available
	1	Capture data available. When FTnEB is read, it is cleared

- **FTnFLGC** (bit 6)
  Indicates the control state by the CST bit of FTMn.
  When FTnC is read, it is cleared.

FTnMD	FTnFLGC	Description
TIMER PWM1/2 CAPTURE	0	Start enable state by event trigger (initial value)
	1	Start disable state by event trigger

- **FTnSTAT** (bit 7)
  Indicates the operation status of FTMn.

FTnMD	FTnSTAT	Description
TIMER CAPTURE PWM1/2	0	Counter stopped (initial value)
	1	Counter running

11.2.9. FTMn Mode Register (FTnMOD : n=0,1,2,3)

Address: 0x5C00_301C(FT0MOD), 0x5C00_311C(FT1MOD),
0x5C00_321C(FT2MOD), 0x5C00_331C(FT3MOD)
Access: R/W
Access size:32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	FTnSTPO	FTnOST	FTnDTEN	–*	–*	–*	–*	FTnMD[1:0]	
Access	–	–	–	–	–	–	–	R/W	R/W	R/W	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnMOD is a special function register (SFR) used to set the function of FTMn.

[Description of Bits]

- **FTnMD[1:0]** (bit 1 to 0)
  Sets the mode of FTMn.

FTnMD	FTnMD[1:0]	Description
-	0	TIMER mode (initial value)
	1	CAPTURE mode
	2	PWM1 mode
	3	PWM2 mode

- **FTnDTEN** (bit 6)
  Enables the dead time of FTMn.

FTnMD	FTnDTEN	Description
TIMER PWM1/2	0	Dead time disabled (initial value)
	1	Dead time enabled
CAPTURE	*	This bit is disabled.

- **FTnOST** (bit 7)
  Sets auto-reload/one-shot mode of FTMn.

FTnMD	FTnOST	Description
TIMER PWM1/2	0	Auto-reload mode (initial value)
	1	One-shot mode
CAPTURE	0	Auto mode Even if the capture is performed once, the data of EA and EB is overwritten (updated) when the next capture is performed. When the counter goes round, it restarts from 0.
	1	Single mode Once captured into EA or EB, the next capture is not performed before read. When the counter goes round, it stops.

[Note]
When using the One-shot mode / Single mode, set to “1” FTnIEP of FTnINTE register and confirm that FTnISP of FTnINTS register is “0”always.

- **FTnSTPO** (bit 8)
  Sets the output state when FTMn stops.

FTnMD	FTnSTPO	Description
TIMER PWM1/2	0	Set the output to "L" at stop. If restarted without clearing the counter, it is "L" until the next period. (initial value)
	1	The current output state is kept after stop. When restarted without clearing the counter, the output depends on the counter value.
CAPTURE	*	Setting disabled.

11.2.10. FTMn Clock Register (FTnCLK : n=0,1,2,3)

Address: 0x5C00_3020(FT0CLK), 0x5C00_3120(FT1CLK),
0x5C00_3220(FT2CLK), 0x5C00_3320(FT3CLK)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	FTnXCK [2:0]			–*	FTnCKD[2:0]			–*	–*	FTnCK[1:0]	
Access	–	–	–	–	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnCLK is a special function register (SFR) used to set the function of FTMn.

[Description of Bits]

- **FTnCK[1:0]** (bit 1 to 0)
  Selects the timer clock source of FTMn.

FTnMD	FTnCK	Description
TIMER CAPTURE PWM1/2	0	LSCLK (initial value)
	1	OSCLK
	2	HSCLK
	3	EXTCLK(Clock selected by FTnXCK[2:0])

- **FTnCKD[2:0]** (bit 6 to 4)
  Selects the dividing ratio of the timer clock source of FTMn.

FTnMD	FTnCKD	Description
TIMER CAPTURE PWM1/2	0	divide by 1 (initial value)
	1	divide by 2
	2	divide by 4
	3	divide by 8
	4	divide by 16
	5	divide by 32
	6	divide by 64
	7	Reserved

- **FTnXCK[2:0]** (bit 10 to 8)
  Selects the source when selecting EXTCLK as a timer clock source of FTMn.

FTnMD	FTnXCK	Description
TIMER CAPTURE PWM1/2	0	TMCKI0 (initial value)
	1	TMCKI1
	2	TMCKI2
	3	TMCKI3
	4	TMCKI4
	5	TMCKI5
	6	TMCKI6
	7	TMCKI7

11.2.11. FTMn Trigger Register (FTnTRG : n=0,1,2,3)

Address: 0x5C00_3024(FT0TRG), 0x5C00_3124(FT1TRG),
0x5C00_3224(FT2TRG), 0x5C00_3324(FT3TRG)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	FTnEST[1:0]		–*	–*	FTnTRM[1:0]	
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FTnSTSS	–*	–*	–*	FTnSTS3[3:0]				–*	–*	–*	–*	FTnCST	FTnEXCL	FTnST1	FTnST0
Access	R/W	–	–	–	R/W	R/W	R/W	R/W	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnTRG is a special function register (SFR) used to set the function of FTMn

[Description of Bits]

- **FTnST0** (bit 0)
  Selects whether a trigger event starts the counter.

FTnMD	FTnST0	Description
TIMER CAPTURE PWM1/2	0	Starting counter disabled (initial value)
	1	Starting counter enabled

- **FTnST1** (bit 1)
  Selects whether a trigger event stops the counter.

FTnMD	FTnST1	Description
TIMER CAPTURE PWM1/2	0	Stopping counter disabled (initial value)
	1	Stopping counter enabled

- **FTnEXCL** (bit 2)
  Selects whether the counter is cleared when a trigger event stops it. It is not cleared at emergency stop regardless of the this bit setting.

FTnMD	FTnEXCL	Description
TIMER CAPTURE PWM1/2	0	Clearing the counter disabled (initial value)
	1	Clearing the counter enabled

- **FTnCST** (bit 3)
  Selects the operation mode of starting the counter by trigger event.

FTnMD	FTnCST	Description
TIMER CAPTURE PWM1/2	0	A trigger event always starts the counter when it is stopped (except for emergency stop) (initial value)
	1	A trigger event does not start the counter before FTnC is read when it is stopped (except for emergency stop)

- **FTnSTSS, FTnSTS[3:0]** (bit 15, 11 to 8)
  Selects the source of the trigger event for FTMn. Do not select itself, for example, FTM0 for the FTM0 setting.

FTnMD	FTnSTS*					Description
	S	3	2	1	0	
TIMER CAPTURE PWM1/2	0	0	0	0	0	EXI0TGO (initial value)
	0	0	0	0	1	EXI1TGO
	0	0	0	1	0	EXI2TGO
	0	0	0	1	1	EXI3TGO
	0	0	1	0	0	EXI4TGO
	0	0	1	0	1	EXI5TGO
	0	0	1	1	0	EXI6TGO
	0	0	1	1	1	EXI7TGO
	1	0	0	0	0	TM0INT
	1	0	0	0	1	TM1INT
	1	0	0	1	0	TM2INT
	1	0	0	1	1	TM3INT
	1	0	1	0	0	TM4INT
	1	0	1	0	1	TM5INT
	1	0	1	1	0	TM6INT
	1	0	1	1	1	TM7INT
	1	1	0	0	0	FTM0TGO
	1	1	0	0	1	FTM1TGO
	1	1	0	1	0	FTM2TGO
	1	1	0	1	1	FTM3TGO
	others					Reserved

[Note]
EXInTGO is the trigger signal from external terminals.
The timer interrupt request (TMnINT) is an interrupt request signal independent of the interrupt enabled/disabled setting of the interrupt enable register.
FTM trigger output(FTMnTGO) is used only for event trigger.

- **FTnTRM[1:0]** (bit 17 to 16)
  Selects the edge of the trigger event for FTMn.
  It is enabled only when EXI0-7TGO is selected as the event trigger source. Otherwise, it is fixed to the rising edge.

FTnMD	FTnTRM[1:0]		Description	
			Counter start	Counter stop/clear
TIMER CAPTURE PWM1/2	0	0	Rising edge	Rising edge (initial value)
	0	1	Falling edge	Rising edge
	1	0	Rising edge	Falling edge
	1	1	Falling edge	Falling edge

- **FTnEST[1:0]** (bit 21 to 20)
  Selects the emergency stop trigger source of FTMn. This bit is effective only when FTnEMGEN is 1.

FTnMD	FTnEST	Description
TIMER CAPTURE PWM1/2	0	Rising edge of EXI0TGO (initial value)
	1	Rising edge of EXI4TGO
	2	Rising edge of CMP0TGO
	3	Rising edge of CMP1TGO

[Note]
EXInTGO is the trigger signal from external terminals.
CMP0TGO,CMP1TGO is signal for trigger of the comparator.

11.2.12. FTMn Interrupt Enable Register (FTnINTE: n = 0,1,2,3)

Address: 0x5C00_3030(FT0INTE), 0x5C00_3130(FT1INTE),
0x5C00_3230(FT2INTE), 0x5C00_3330(FT3INTE)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	FTnIOB	FTnIOA	FTnIOP	–*	–*	–*	FTnIETR	FTnIETS	FTnIEB	FTnIEA	FTnIEP
Access	–	–	–	–	–	R/W	R/W	R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnINTE is a special function register (SFR) used to control the interrupt of FTMn.
Setting a bit of FTnINTE to "1" makes the interrupt enabled and notifies the interrupt controller.

[Description of Bits]

- **FTnIEP** (bit 0)
  Sets the period interrupt enable of FTMn.

FTnMD	FTnIEP	Description
TIMER CAPTURE PWM1/2	0	Period interrupt disabled (initial value)
	1	Period interrupt enabled

- **FTnIEA** (bit 1)
  Sets the event timing A interrupt enable of FTMn.

FTnMD	FTnIEA	Description
TIMER PWM1/2	0	Event timing A interrupt disabled (initial value)
	1	Event timing A interrupt enabled
CAPTURE	0	Capture A interrupt disabled
	1	Capture A interrupt enabled

- **FTnIEB** (bit 2)
  Sets the event timing B interrupt enable of FTMn.

FTnMD	FTnIEB	Description
TIMER PWM1/2	0	Event timing B interrupt disabled (initial value)
	1	Event timing B interrupt enabled
PMW2	0	Set FTnIEB to 0 in this mode.
	1	Prohibited in this mode.
CAPTURE	0	Capture B interrupt disabled
	1	Capture B interrupt enabled

- **FTnIETS** (bit 3)
  Sets the trigger counter stop interrupt enable of FTMn.

FTnMD	FTnIETS	Description
TIMER CAPTURE PWM1/2	0	Trigger counter stop interrupt disabled (initial value)
	1	Trigger counter stop interrupt enabled

- **FTnIETR** (bit 4)
  Sets the trigger counter start interrupt enable of FTMn.

FTnMD	FTnIETR	Description
TIMER CAPTURE PWM1/2	0	Trigger counter start interrupt disabled (initial value)
	1	Trigger counter start interrupt enabled

- **FTnIOP** (bit 8)
  Outputs a period interrupt request of FTMn as the trigger for another peripheral.

FTnMD	FTnIOP	Description
TIMER CAPTURE PWM1/2	0	Period interrupt trigger disabled (initial value)
	1	Period interrupt trigger enabled

- **FTnIOA** (bit 9)
  Outputs an event timing A interrupt request of FTMn as the trigger for another peripheral.

FTnMD	FTnIOA	Description
TIMER CAPTURE PWM1/2	0	Event timing A interrupt trigger disabled (initial value)
	1	Event timing A interrupt trigger enabled

- **FTnIOB** (bit 10)
  Outputs an event timing B interrupt request of FTMn as the trigger for another peripheral.

FTnMD	FTnIOB	Description
TIMER CAPTURE PWM1	0	Event timing B interrupt trigger disabled (initial value)
	1	Event timing B interrupt trigger enabled
PWM2	0	Set FTnIOB to 0 in this mode.
	1	Prohibited in this mode.

11.2.13. FTMn Interrupt Status Register (FTnINTS : n=0,1,2,3)

Address: 0x5C00_3034(FT0INTS), 0x5C00_3134(FT1INTS),
0x5C00_3234(FT2INTS), 0x5C00_3334(FT3INTS)
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	FTnISES	FTnISTR	FTnISTS	FTnISB	FTnISA	FTnISP
Access	–	–	–	–	–	–	–	–	–	–	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnINTS is a special function register (SFR) used to indicate the interrupt status of FTMn.
FTnINTS is a read-only register. Writing to it has no effect.

[Description of Bits]

- **FTnISP** (bit 0)
  Indicates the period interrupt state of FTMn.

FTnMD	**FTnISP**	Description
TIMER CAPTURE PWM1/2	0	Period interrupt has not occurred (initial value)
	1	Period interrupt has occurred This bit is cleared when writing 1 to FTnICP

- **FTnISA** (bit 1)
  Indicates the state of event timing A interrupt of FTMn.
  Indicates that the captured data is stored to FTnEA in the CAPTURE mode.

FTnMD	**FTnISA**	Description
TIMER PWM1/2	0	Event timing A interrupt has not occurred (initial value)
	1	Event timing A interrupt has occurred This bit is cleared when writing 1 to FTnICA
CAPTURE	0	Capture A interrupt has not occurred
	1	Capture A interrupt has occurred This bit is cleared when writing 1 to FTnICA or reading FTnEA

- **FTnISB** (bit 2)
  Indicates the state of event timing B interrupt of FTMn.

FTnMD	FTnISB	Description
TIMER PWM1/2	0	Event timing B interrupt has not occurred (initial value)
	1	Event timing B interrupt has occurred This bit is cleared when writing 1 to FTnIB
CAPTURE	0	Capture B interrupt has not occurred
	1	Capture B interrupt has occurred Indicates that the captured data is stored to FTnEB. This bit is cleared when writing 1 to FTnICB or reading FTnEB

- **FTnISTS** (bit 3)
  Indicates the trigger counter stop interrupt state of FTMn.

FTnMD	FTnISTS	Description
TIMER CAPTURE PWM1/2	0	Trigger counter stop interrupt has not occurred (initial value)
	1	Trigger counter stop interrupt has occurred This bit is cleared when writing 1 to FTnICTS

- **FTnISTR** (bit 4)
  Indicates trigger counter start interrupt state of FTMn.

FTnMD	FTnISTR	Description
TIMER CAPTURE PWM1/2	0	Trigger counter start interrupt has not occurred (initial value)
	1	Trigger counter start interrupt has occurred This bit is cleared when writing 1 to FTnICTR

- **FTnISES** (bit 5)
  Indicates the emergency stop interrupt state of FTMn.

FTnMD	FTnISES	Description
TIMER CAPTURE PWM1/2	0	Emergency stop interrupt has not occurred (initial value)
	1	Emergency stop interrupt has occurred This bit is cleared when writing 1 to FTnICES

11.2.14. FTMn Interrupt Clear Register (FTnINTC : n=0,1,2,3)

Address: 0x5C00_3038(FT0INTC), 0x5C00_3138(FT1INTC),
0x5C00_3238(FT2INTC), 0x5C00_3338(FT3INTC)
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	FTnICES	FTnICTR	FTnICTS	FTnICB	FTnICA	FTnICP
Access	–	–	–	–	–	–	–	–	–	–	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTnINTC is a special function register (SFR) used to clear the interrupt status of FTMn.
When writing 1 to this bit, the target interrupt status is cleared.
When reading it, 0000H is always read.

[Description of Bits]

- **FTnICP** (bit 0)
  Clears the period interrupt of FTMn.

- **FTnICA** (bit 1)
  Clears the event timing A interrupt of FTMn.

- **FTnICB** (bit 2)
  Clears the event timing B interrupt of FTMn.

- **FTnICTS** (bit 3)
  Clears trigger counter stop interrupt of FTMn.

- **FTnICTR** (bit 4)
  Clears trigger counter start interrupt of FTMn.

- **FTnICES** (bit 5)
  Clears the emergency stop interrupt of FTMn.

11.2.15. FTM Output nm Select Register n (FTOSLn : n = 0, 4, 8, C)

Address: 0x5C00_3F00(FTOSL0), 0x5C00_3F04(FTOSL4),
0x5C00_3F08(FTOSL8), 0x5C00_3F0C(FTOSLC)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	FTOS N(n+3)	–*	FTOS(n+3) [2:0]			–*	–*	–*	FTOS N(n+2)	–*	FTOS(n+2) [2:0]		
Access	–	–	–	R/W	–	R/W	R/W	R/W	–	–	–	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	FTOS N(n+1)	–*	FTOS (n+1) [2:0]			–*	–*	–*	FTOS Nn	–*	FTOSn [2:0]		
Access	–	–	–	R/W	–	R/W	R/W	R/W	–	–	–	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FTOSLn is a special function register (SFR) used to control assignment and output polarity of output FTMnP/FTMnN of FTM to TMOUT0 - F.

The word symbol FTOSLn (n=0, 4, 8, C) corresponds to TMOUT0 - F as follows:

Pin name	Output signal	Symbol	FTOSNn	FTOSn [2:0]
P02	TMOUT0	FTOSL0	FTOSN0 (bit4)	FTOS0 [2:0] (bit2 to 0)
P03	TMOUT1		FTOSN1 (bit12)	FTOS1 [2:0] (bit10 to 8)
P22	TMOUT2		FTOSN2 (bit20)	FTOS2 [2:0] (bit18 to 16)
P23	TMOUT3		FTOSN3 (bit28)	FTOS3 [2:0] (bit26 to 24)
P32	TMOUT4	FTOSL4	FTOSN4 (bit4)	FTOS4 [2:0] (bit2 to 0)
P33	TMOUT5		FTOSN5 (bit12)	FTOS5 [2:0] (bit10 to 8)
P36	TMOUT6		FTOSN6 (bit20)	FTOS6 [2:0] (bit18 to 16)
P37	TMOUT7		FTOSN7 (bit28)	FTOS7 [2:0] (bit26 to 24)
P42	TMOUT8	FTOSL8	FTOSN8 (bit4)	FTOS8 [2:0] (bit2 to 0)
P43	TMOUT9		FTOSN9 (bit12)	FTOS9 [2:0] (bit10 to 8)
P46	TMOUTA		FTOSNA (bit20)	FTOSA [2:0] (bit18 to 16)
P47	TMOUTB		FTOSNB (bit28)	FTOSB [2:0] (bit26 to 24)
P52	TMOUTC	FTOSLC	FTOSNC (bit4)	FTOSC [2:0] (bit2 to 0)
P53	TMOUTD		FTOSND (bit12)	FTOSD [2:0] (bit10 to 8)
P56	TMOUTE		FTOSNE (bit20)	FTOSE [2:0] (bit18 to 16)
P57	TMOUTF		FTOSNF (bit28)	FTOSF [2:0] (bit26 to 24)

[Description of Bits]

- **FTOSn[2:0]** (bit 2 to 0), **FTOS(n+1)[2:0]** (bit 10 to 8), **FTOS(n+2)[2:0]** (bit 18 to 16), **FTOS(n+3)[2:0]** (bit 26 to 24)

These bit used to select the FTM output that is assigned TMOUTx(X=0-F) output signal.

FTOSn[2]	FTOSn[1]	FTOSn[0]	Description
0	0	0	FTM0P (Initial value)
0	0	1	FTM0N
0	1	0	FTM1P
0	1	1	FTM1N
1	0	0	FTM2P
1	0	1	FTM2N
1	1	0	FTM3P
1	1	1	FTM3N

- **FTOSNn** (bit 7), **FTOSN(n+1)** (bit 15), **FTOSN(n+2)** (bit 23), **FTOSN(n+3)** (bit 31)
  These bit invert the FTM output.

FTOSNn	Description
0	Does not invert the output. (Initial value)
1	Inverts the output.

11.3. Description of Operation

This operates as timer, capture, or PWM according to the mode set in FTnMD[1:0].
This section describes start/stop by software/event trigger, emergency stop, interrupt processing, and output control for each mode.
FTMn has four types of operation mode: TIMER, CAPTURE, PWM1, and PWM2.

TIMER mode:
It controls the interrupt generation and output signal using the counter overflow.

CAPTURE mode:
It stores the count value when the selected trigger event is generated to the FTMn event register A (FTnEA) and FTMn event register B (FTnEB).

PWM1 mode:
It can generate two types of PWM waveform with the same period and aligned start edges, using the FTMn event register A (FTnEA) as the DUTY value of the output signal FTMnP and the FTMn event register B (FTnEB) as the DUTY value of the output signal FTMnN.

PWM2 mode:
It can generate a complementary PWM waveform where the output signal FTMnN operates exclusively, using the FTMn event register A (FTnEA) as the DUTY value of the output signal FTMnP. Also, the dead time can be set using the FTMnDeadTimer register (FTMnDT).

11.3.1. Common Sequence

FTM starts the operation by FTnCON0 after setting 1-6 described below as needed.
Then it processes interrupts and updates cycle/event settings and so on.

1: Mode setting (FTnMOD)
Select the mode using the mode register (FTnMOD). Also, set the dead time to output waveform, and so on.

2: Clock setting (FTnCLK)
Select the counter clock. This sets the source clock and the dividing ratio.

3: Trigger setting (FTnTRG)
Use this setting when starting/stopping the counter by event trigger. Select the event trigger source and action , and the edge of the event trigger/emergency stop/capture for FTnTRG.

4: Interrupt setting (FTnINTE)
Set the interrupt source. Select from period/event (counter coincide, duty, capture) and trigger start/stop interrupt.
When using the One-shot mode / Single mode, set to “1” FTnIEP of FTnINTE register and confirm that FTnISP of FTnINTS register is “0” always.

5: Period/event setting (FTnP, FTnEA, FTnEB, FTnDT)
Set the period, data for counter coincide, duty and dead time.

	TIMER	CAPTURE	PWM1	PWM2
FTnP	Auto-reload period or timeout of one-shot			
FTnEA	Coincident interrupt setting value	(Capture data.)	FTMnP duty	Duty
FTnEB	Coincident interrupt setting value		FTMnN duty	(Unused)
FTnDT	Dead time for output	(Unused)	Dead time for output	Dead time for output

The period is calculated as follows:

$$T_{priod} = \frac{FTnP + 1}{FTnCK\ [Hz]} \quad (FTnP : 0001H \text{ to } FFFFH)$$

6: Output setting (FTOSL*, Each Port Setting)
Set which output to which port, and reverse.

7: Control start/stop (FTnCON0)
Allow the software start or event trigger reception. Also, set the emergency stop enable.
The counter operates at a falling edge of FTnCK. The software start/stop are synchronized by FTnCK. FTnSTAT is set to H after FTnCK1 cycle at start, and the counter starts operating after two cycles. At stop, the counter is stopped in FTnCK1 cycle, and FTnSTAT is set to L. The counter value is kept at this time. If started again, it restarts after one cycle. To clear the counter, use write access to FTnC.

8: Processing during operation (FTnCON0/1, FTnINTS/C)
The state during operation can be seen in FTnCON1 or FTnINTS. To change the waveform of PWM, etc., set the period/event and set FTnUD of FTnCON1. Then, it is updated in the next period. Also, setting FTnSDN of FTnCON0 forces the output to be masked to L.

11.3.2. Counter Operation

The internal counter of FTM operates in the same way in all the modes.
It counts up until the setting value of the FTMn period register (FTnP).
At overflow in auto-reload mode (FTnOST bit of the FTMn mode register (FTnMOD) is "0"), the counter is cleared and continues counting again. At overflow in one-shot mode (FTnOST bit of FTnMOD is "1" and FTnIPE bit of FTnINTE is “1”), the counter is cleared and stops counting.
The software or trigger event can start/stop counting.

11.3.2.1. Starting/Stopping Counting by Software

When FTnRUN bit of the FTMn control register 0 (FTnCON0) is set to "1", the counter starts.
In one-shot mode (FTnOST bit of the FTMn mode register (FTnMOD) is "1"), FTnRUN bit is automatically set to "0" when the counter stops due to overflow.

If the counter is operating (FTnSTAT bit of the FTMn control register 1 (FTnCON1) is "1"), the counter stops when FTnRUN is set to "0". At this time, the counter keeps the value when it stops. When FTnRUN bit is set to "1" again, the counter continues from the stopped value.
To clear the counter, write to the FTMn counter register (FTnC) when it is not operating. (This written data is meaningless.)

11.3.2.2. Starting/Stopping Counting by Trigger Event

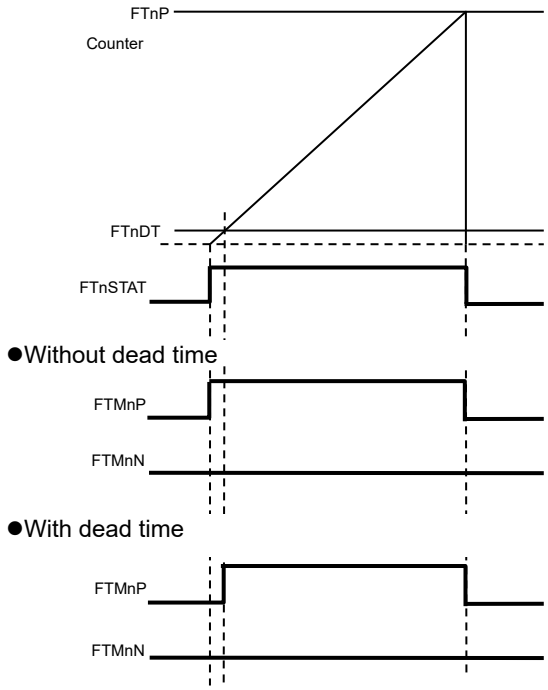
When FTnTGEN bit of the FTMn control register 0 (FTnCON0) is set to "1", the counter is made controllable by triggers.
Set the FTMn trigger setting register 0 and 1 (FTnTRG) to select a trigger and so on.
The trigger event source can be selected from the external interrupts, the timer interrupts, and another FTM triggers.
The counter start, counter stop, or counter start/ stop can be selected by selecting a trigger event.

11.3.3. TIMER Mode Operation

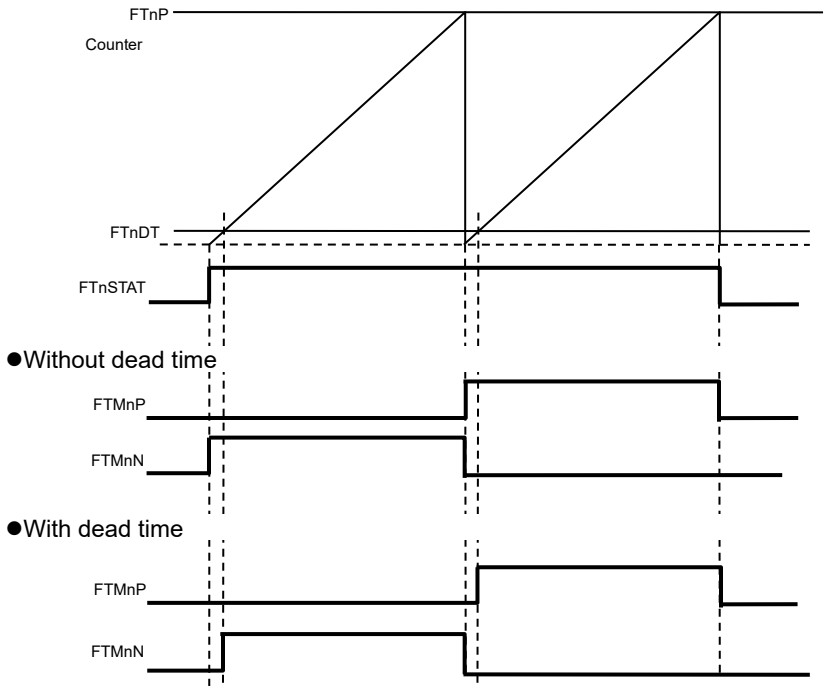
The TIMER mode controls the interrupt generation and output signal using the counter overflow.

11.3.3.1. Output Waveform in TIMER Mode

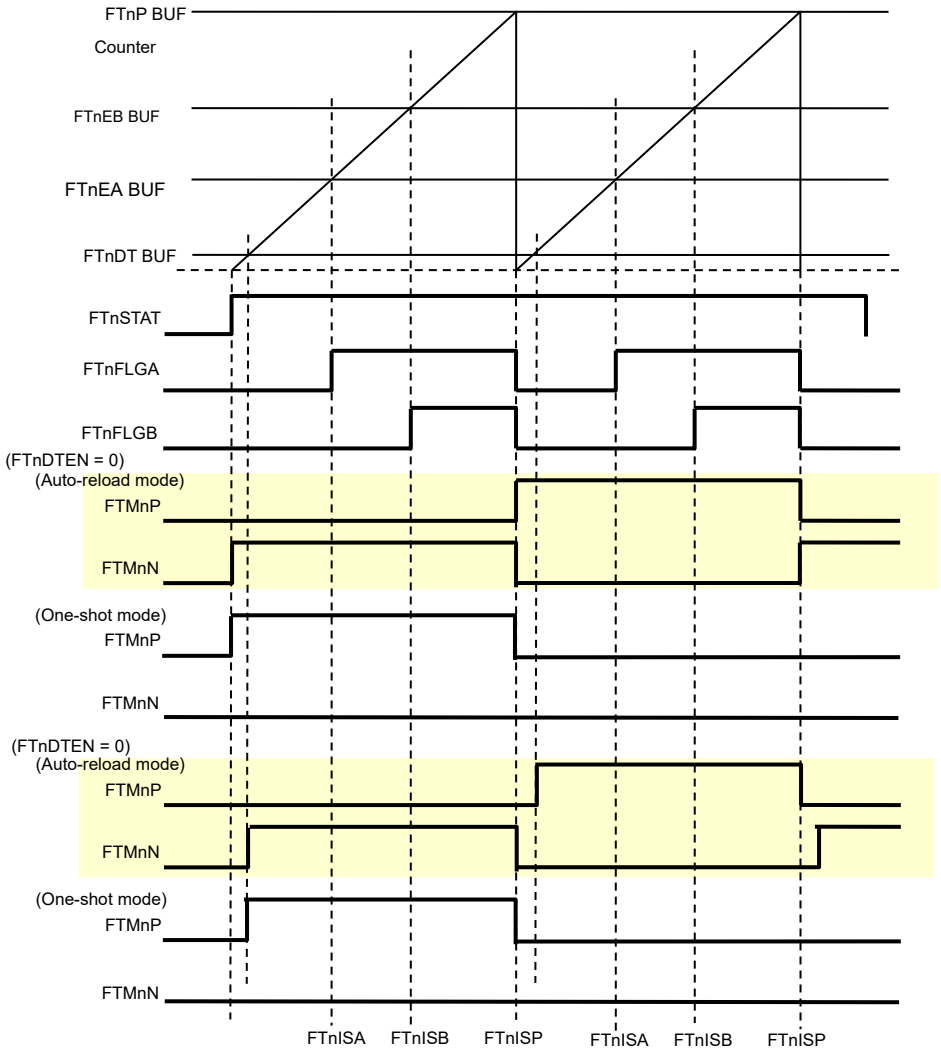
In the timer output auto-reload modem, the output is toggled for each period.
If the counter value is "0000H", FTMnP starts with L and FTMnN starts with H when FTnRUN bit of the FTMn control register 0 (FTnCON0) is set to "1".
In the one-shot mode, it stops after outputting H pulse of one period from FTMnP. FTMnN is fixed to L.
When the dead time is set using the FTMn DeadTime register (FTnDT), the output is L after starting the counter before passing the count set in FTnDT.



(a) TIMER mode output waveform (one-shot mode)



(b) TIMER mode output waveform (auto-reload mode)



(c) waveform and interrupt timing

$$T_{priod} = \frac{FTnP + 1}{FTnCK\ [Hz]} \quad (FTnP : 0x0001 \text{ to } 0xFFFF)$$

$$T_{eventA/B} = \frac{FTnEA(or\ FTnEB) + 1}{FTnCK\ [Hz]} \quad (FTnA/FTnB : 0x0000 \text{ to } 0xFFFE)$$

$$T_{deadtime} = \frac{FTnDT + 1}{FTnCK\ [Hz]} \quad (FTnDT : 0x0000 \text{ to } 0xFFFE)$$

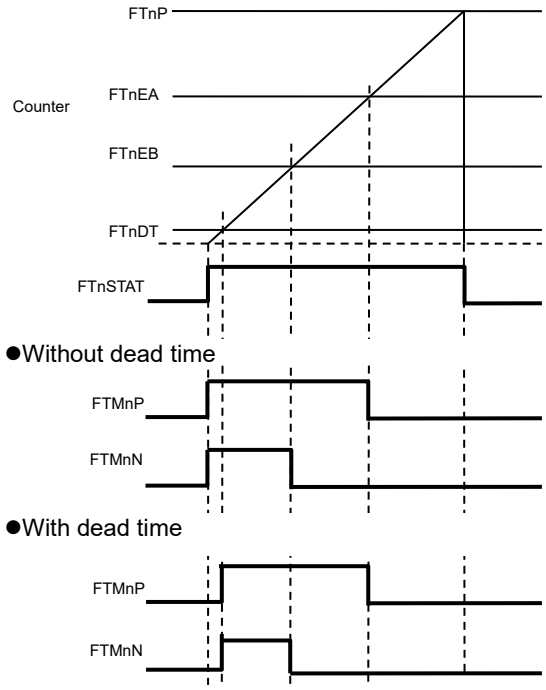
Figure 11-2 waveform in TIMER mode

11.3.4. PWM1 Mode Operation

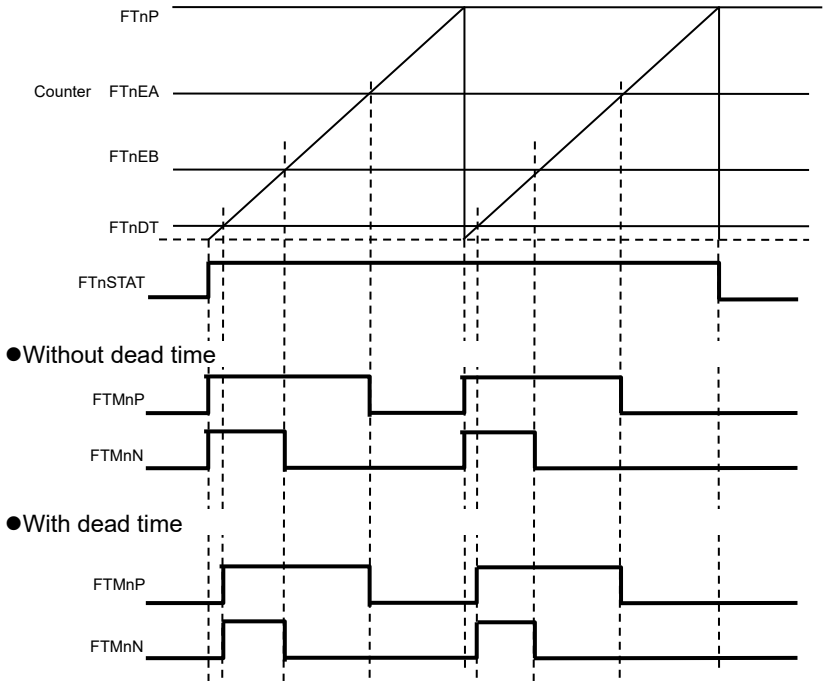
The PWM1 mode generates synchronization output pulses with the period set in FTnP. The duties of the output FTMnP and FTMnN are set in FTnEA and FTnEB respectively.

11.3.4.1. Output Waveform in PWM1 Mode

In the Auto-reload mode, the initial values of FTMnP and FTMnN are L, and they change to H at start. Each of them changes to L at the duty value. It changes to H in the next period. This is repeated until they stop. In the one-shot mode, they automatically stop and change to L after one period.
If the dead time is enabled, the FTMnP and FTMnN are L during the dead time from start of the counter.



(a) PWM1 mode output waveform (one-shot mode)



(b) PWM1 mode output waveform (auto-reload mode)

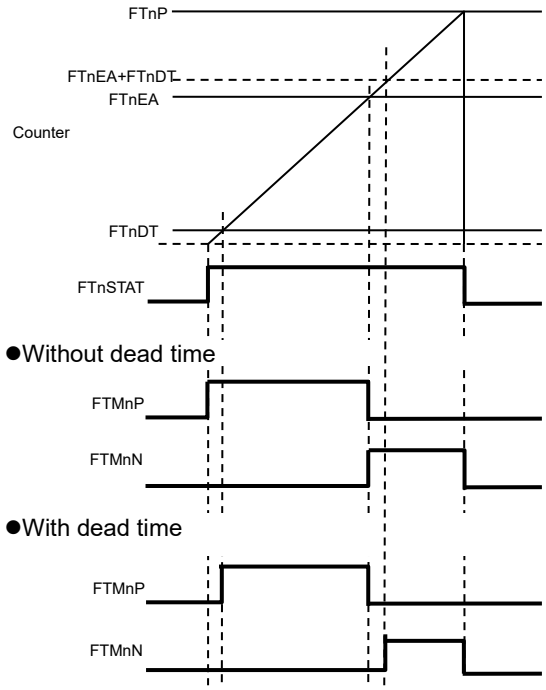
Figure 11-3 waveform in PWM1 mode

11.3.5. PWM2 Mode Operation

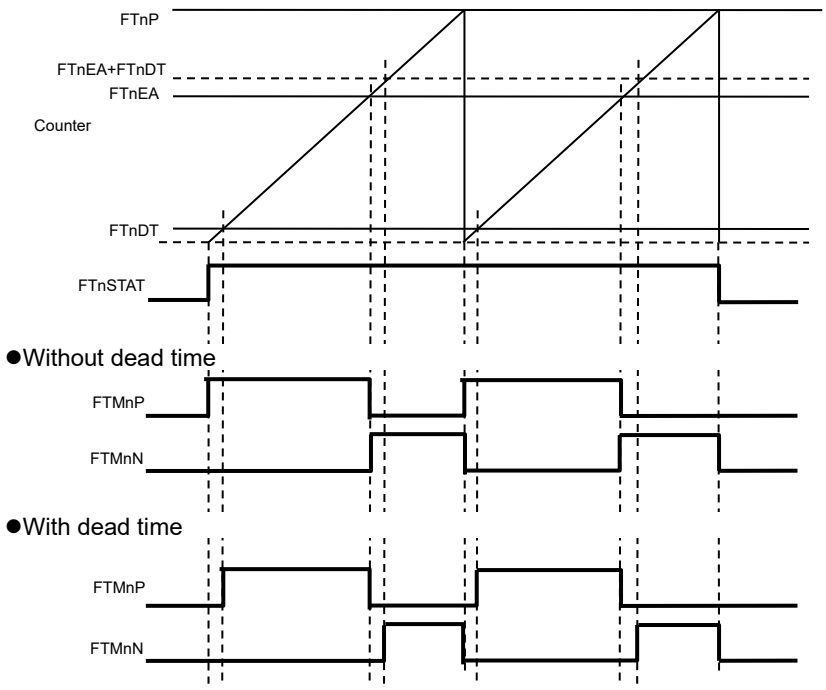
The PWM2 mode generates a complementary output pulse with the cycle set in FTnP. Set the duties of the output FTMnP/N in FTnEA. FTnEB is not used.

11.3.5.1. Output Waveform in PWM2 Mode

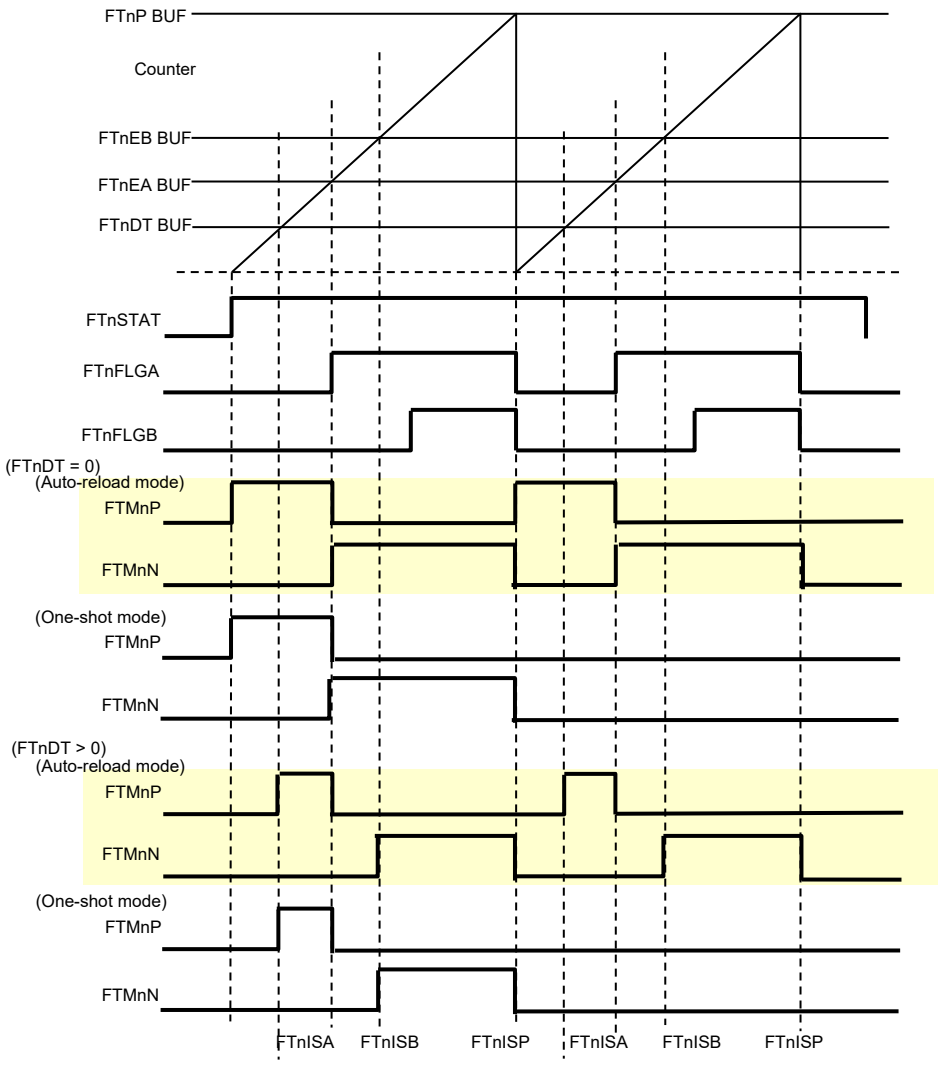
In the Auto-reload mode, the initial values of FTMnP and FTMnN are L, and FTMnP changes to H at start. FTMnP changes to L and FTMnN changes to H at the duty value. FTMnP changes to H and FTMnN changes to L in the next period. This is repeated until they stop. In the one-shot mode, they automatically stop and change to L after one period.
If the dead time is enabled, L is output during the dead time from start of the counter for FTMnP and from coincidence of duty for FTMnN.



(a) PWM2 mode output waveform (one-shot mode)



(b) PWM2 mode output waveform (auto-reload mode)



(c) waveform and interrupt timing

$$T_{priod} = \frac{FTnP + 1}{FTnCK\ [Hz]} \quad (FTnP : 0x0001 \text{ to } 0xFFFF)$$

$$T_{duty} = \frac{FTnEA + 1}{FTnCK\ [Hz]} \quad (FTnA/FTnB : 0x0000 \text{ to } 0xFFFE)$$

$$T_{deadtime1} = \frac{FTnDT + 1}{FTnCK\ [Hz]} \quad (FTnDT : 0x0000 \text{ to } 0xFFFE)$$

Figure 11-4 waveform in PWM2 mode

11.3.6. CAPTURE Mode Operation

The CAPTURE mode stores the count value at the time when an event trigger source is generated, to the FTnEA/FTnEB register. The event trigger source to be captured is common to that used at counter start/stop.

Stored data in FTnEA	Counter value at the time when an event trigger rising edge is generated
Stored data in FTnEB	Counter value at the time when an event trigger falling edge is generated

11.3.6.1. Measurement Example in the CAPTURE Mode

The following example shows the measurement of the period and duty of PWM input from EXI0 using CAPTURE mode and counter start/stop by trigger events.

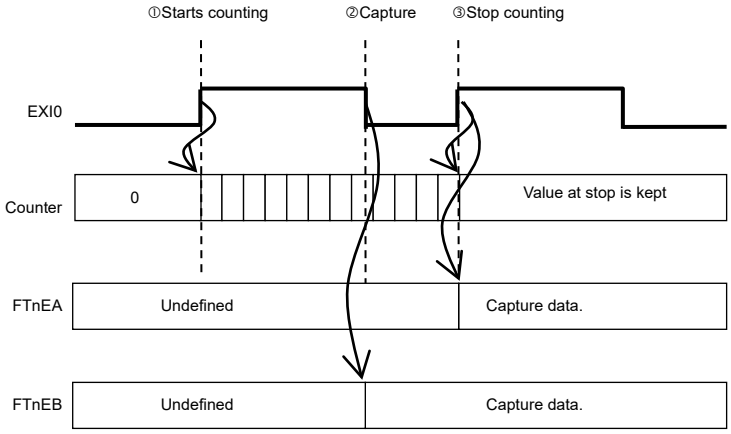


Figure 11-5 Measurement example in the CAPTURE mode

Set the FTnMOD register to the capture mode (FTnMD=01b).
Use the FTnINTE register (FTnIETS=1) to enable the trigger counter stop interrupt.
Use the FTnTRG register to set the trigger event source to EXI0TGO (FTnSTSS=0, FTnSTS=0x00), enable counter start (FTnST0=1), and enable counter stop (FTnST1=1).
Use the FTnTRG register to set counter start and stop to rising edge (FTnTRM=00b).
Use the FTnCON0 register to enable the trigger operation (FTnTGEN=1).

The counter starts at rising of EXI0. (①)
Then the counter value is stored to the FTnEB register at falling of EXI0. (②)
When the rising of EXI0 is detected again, the counter stops, and an interrupt occurs. (③)
And the counter value is stored to the FTnEA register at rising of EXI0.

At this time, the values of FTnEA and FTnEB correspond to the period and the duty of EXI0 respectively.

The operation after capture depends on the FTnOST bit of the FTnMOD register.

●When FTnOST=0 (auto mode)

After the counter restarts at the next rising of EXI0, the value of FTnEA is updated at falling of EXI0.

●When FTnOST=1 (single mode)

After the counter restarts at the next rising of EXI0, the value of FTnEA is not updated at falling of EXI0.

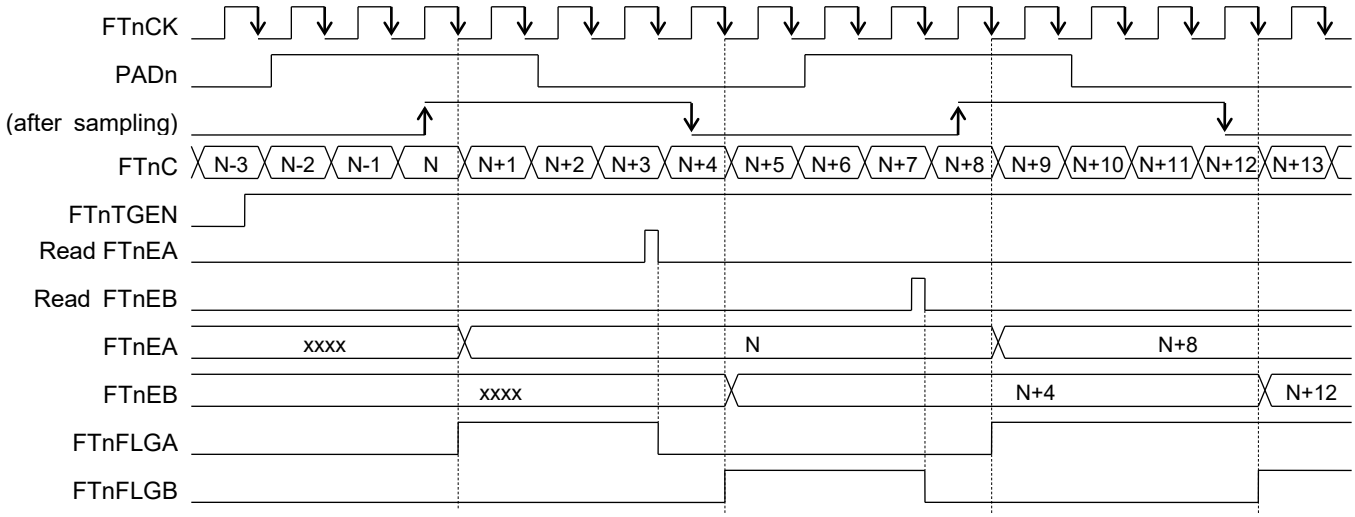


Figure 11-6 (a) FTnEA, FTnEB register read before next trigger (FTnOST=0,1)

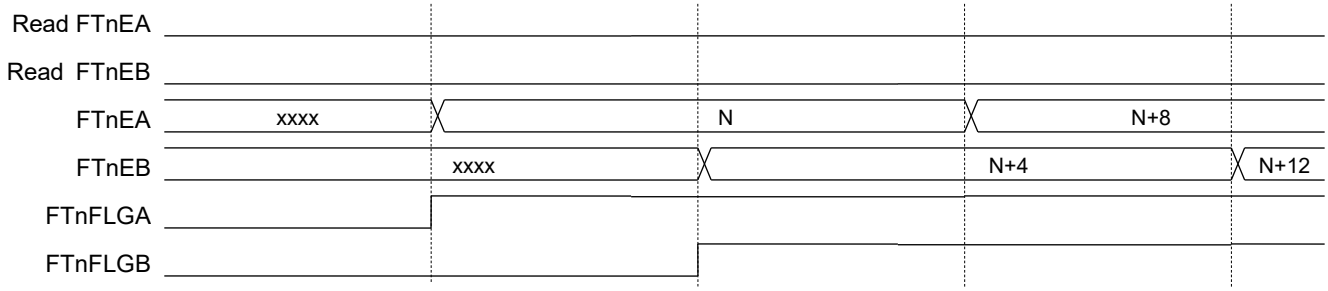


Figure 11-6 (b) Next trigger occurred without register read (FTnOST=0)

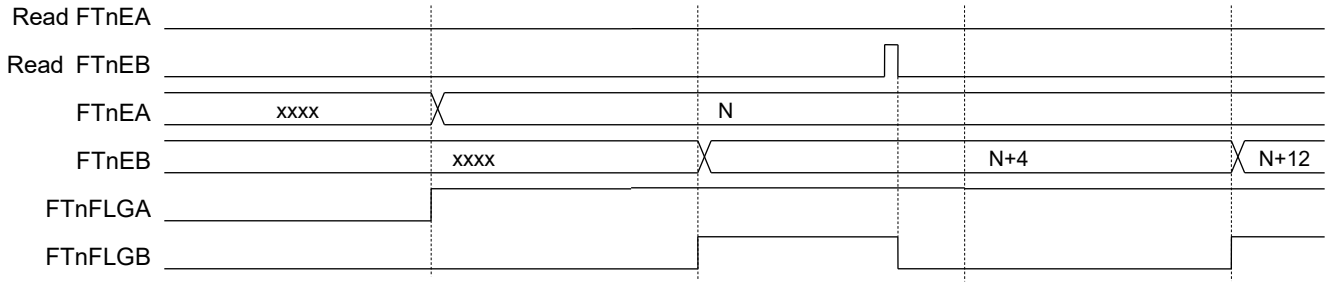


Figure 11-6 (c) Next trigger occurred without register read (FTnOST=1)

11.3.7. Event/Emergency Stop Trigger Control

11.3.7.1. Trigger Signal

FTMn can receive two types of trigger signal: event trigger and emergency stop trigger.
The event trigger is used as counter start/stop or trigger of capture. EXI0-7TGO (external interrupts), TIMER0-7 interrupts, or FTM0-3 triggers can be selected as the trigger source.
The emergency stop trigger is used to stop the timer operation. It stops the counter and sets output FTMnP/FTMnN to L. CMP0TGO/CMP1TGO interrupt, EXI0TGO, or EXI4TGO can be selected as the trigger source.

The analog filter output of the interrupt controller is connected to the EXI0-7TGO input. The analog filter can be enabled/disabled using the interrupt controller register.
The output of the sampling controller in the comparator is connected to the input from CMP0/1TGO.
The sampling can be selected using the comparator register.
The timer interrupt source and the FTM trigger source are set using the register of each timer.

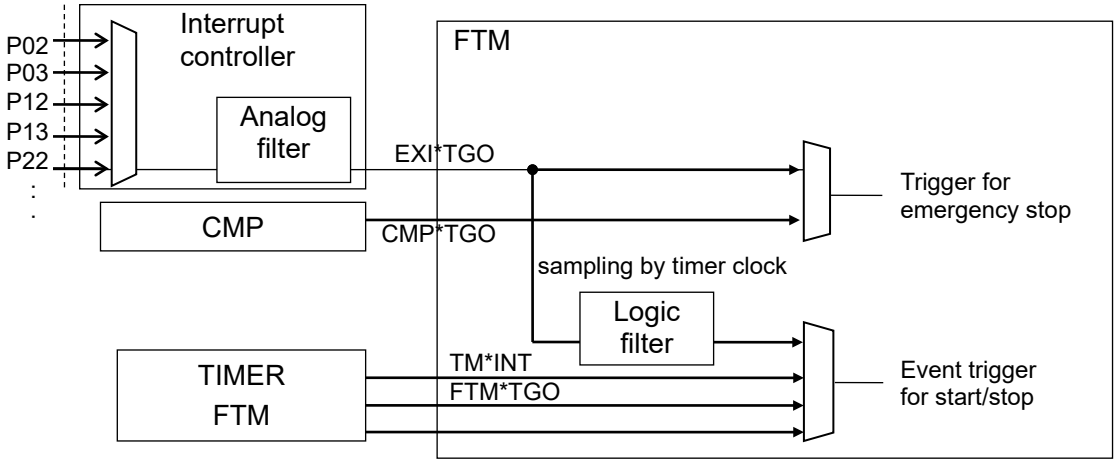


Figure 11-7 Input Path of Trigger Signal

11.3.7.2. Start/Stop Operationg by Event Trigger

Here is the setting used to control the counter by event triggers.

1) FTnTRG setting
   Enable/Disable counter start/stop by event triggers
   Set whether or not to clear the counter at stop by an event trigger
   Set whether or not to accept the next counter start after stop by an event trigger
   Set the event trigger source (EXI0-7TGO, TIMER0-7INT, FTM0-3TGO)
   Set the edge of the event trigger which generates counter start
   Set the edge of the event trigger which generates counter stop
3) Controlling FTnCON0
   Set FTnTGEN to "1" to enter the waiting state for event triggers.
   Then, set FTnRUN to "1" to start the counter by the software.
   Set FTnRUN to "0" during the counter operation to stop the counter by the software.

Because the trigger signal is sampled at FTnCK when the external input trigger (EXInTGO) is selected as counter control by event triggers, the input pulse width should be set to Analog filter 200ns and three or more sampling clocks. Pulses shorter than three sampling clock may be or may not be removed. Note that the sampling is not performed when the timer interrupt is selected as the event trigger.

Figure 11-8 shows the sampling timing of the external input.

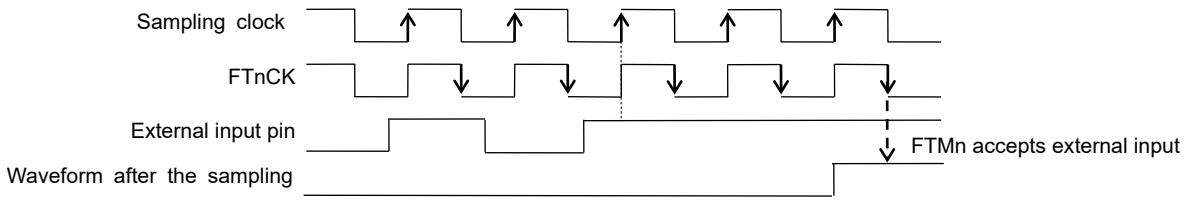
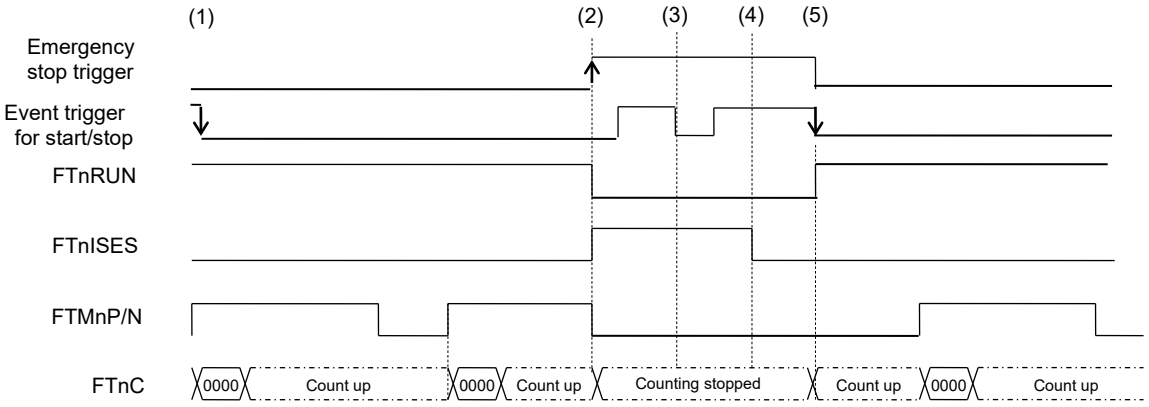


Figure 11-8 Sampling Timing of External Input

11.3.7.3. Emergency Stop Operation

When FTnEMGEN is set to "1", the emergency stop function is enabled. Set this bit after the trigger source is selected in FTnEST.
If an emergency stop trigger input (rising edge) is detected, the counter stops, the output is set to L, and an emergency stop interrupt occurs.
To restart the counter, clear the emergency stop interrupt status (write "1" to FTnICES) and "1" is set to run bit.
Figure 11-9 shows the operation timing at emergency stop.
After the emergency stop, the RUN bit is cleared to 0, the counter stops after one timer clock, and the STAT bit is cleared to 0. When the STAT bit is 1, setting the RUN to 1 is not accepted. Confirm that the STAT has changed to 0 after clearing the interrupt status before running the next RUN.



(1) The counter operation starts at an event trigger (falling edge).
(2) The counter stops at an emergency stop trigger (rising edge). An emergency stop interrupt occurs.
(3) The event trigger is disabled due to the emergency stop in progress.
(4) Clear the emergency stop interrupt to enable the operation.
(5) The counter operation restarts at an event trigger (falling edge).
(In this example, the pulse output restarts after one cycle because the counter is not cleared)

Figure 11-9 Operation Timing Diagram at Emergency Stop

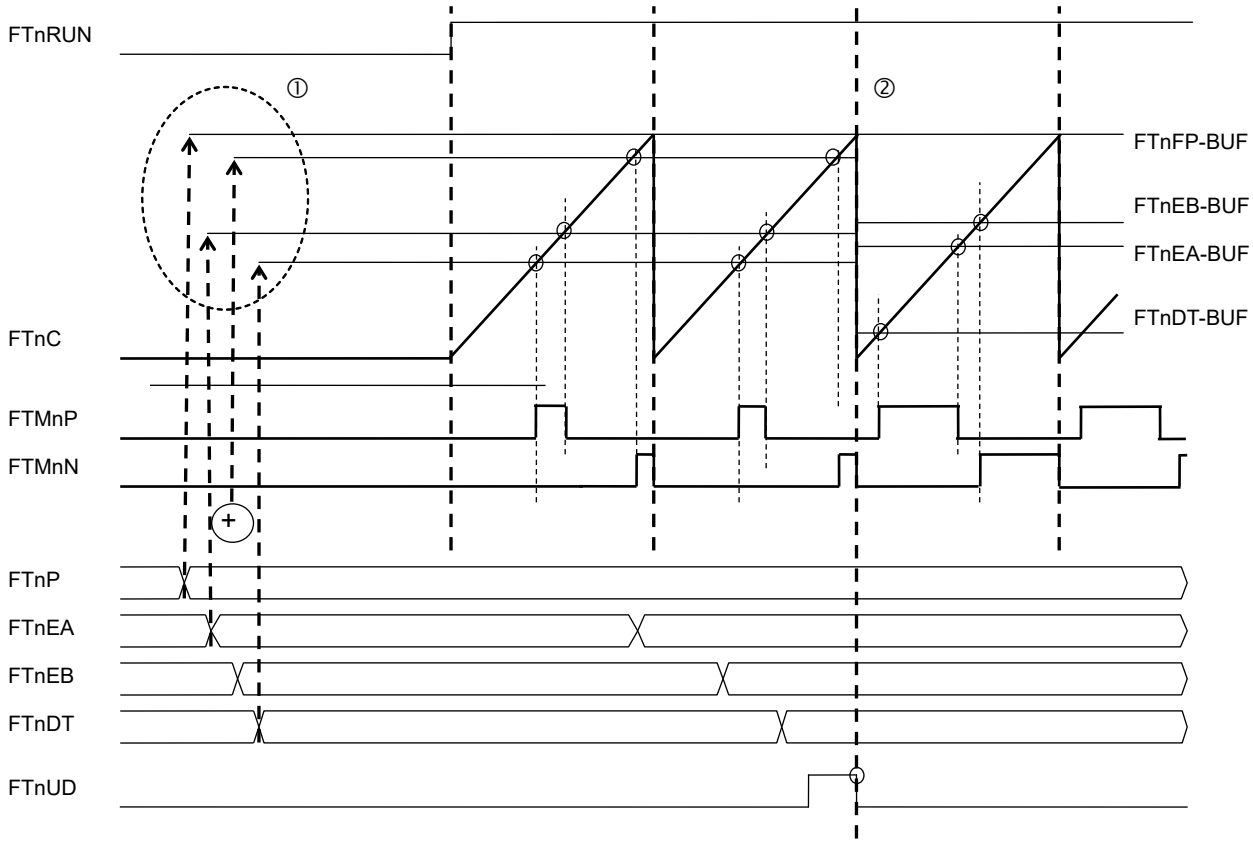
11.3.8. Output at Counter Stop

The FTMnP and FTMnN states depend on the setting of FTnSTPO when the counter stops by a software/Event trigger. If FTnSTPO is "0", FTMnP/FTMnN is set to "L" at the same time as stop. If the counter is restarted in this state, the FTMnP/FTMnN outputs keep "L" during that period, and they change according to the counter value from the next period.
When FTnSTPO is "1", FTMnP/FTMnN keep the state at stop. When the counter is restarted, their states change according to the counter value.
When the FTnEXCL bit of the FTnTRG register is set to "1" or the software clears the counter after counter stop, the counter value is counted up from "0000", and the output depends on the counter value.

11.3.9. Changing Period, Event A/B, and Dead Time during Operation

The period, event A/B, and dead time can be changed in the next cycle when the timer is counting.
To do so, set desired registers (FTnP, FTnEA, FTnEB, FTnDT, etc.), and then write "1" to the FTnUD bit of the FTnCON1 register to request the update. The values in the buffers for the period, event A/B, and dead time are updated at the beginning of the next period, and the FTnUD bit is set to "0".

Here is an example in the PWM2 mode (DTEN=1).



① Each buffer is updated at set timing during operation stopped.
② Each buffer is updated at the beginning of the next period where PFUD is set to "1" during operation.

Figure 9-10 Update Timing during Operation

11.3.10. Interrupt Source

This section describes the interrupt source and how to clear it.
When a target interrupt enable (FTnIE*) is set to "1", the interrupt status is enabled, and the interrupt controller is notified of the source.
Note that the emergency stop interrupt enable does not exist. When the emergency stop is enabled, its interrupt is also enabled.
If the interrupt status is set to "1" for a source, clear it by an appropriate processing.

Name	Mode	Status	How to clear
Period coincident interrupt	ALL	FTnISP	Write "1" to FTnICP
Event A coincident interrupt	TIMER/PWM1/PWM2	FTnISA	Write "1" to FTnICA
Capture A interrupt	CAPTURE	FTnISA	Write "1" to FTnICA or read FTnEA
Event B coincident interrupt	TIMER/PWM1	FTnISB	Write "1" to FTnICB
Capture B interrupt	CAPTURE	FTnISB	Write "1" to FTnICB or read FTnEB
Trigger stop interrupt	ALL	FTnISTS	Write "1" to FTnICTS
Trigger start interrupt	ALL	FTnISTR	Write "1" to FTnICTR
Emergency stop interrupt	ALL	FTnISES	Write "1" to FTnICES

The period coincident interrupt/event A coincident interrupt/event B coincident interrupt can be selected as the interrupt trigger output.

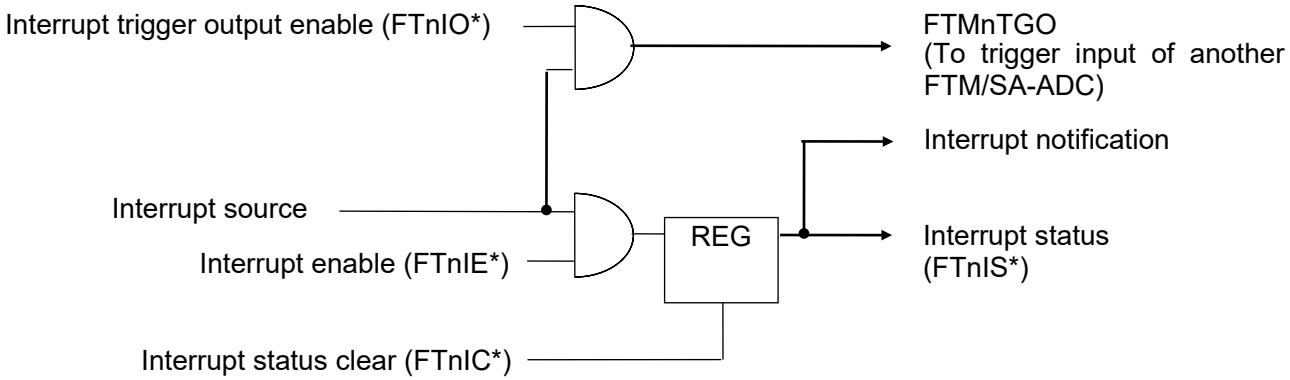


Figure 11-11 interrupt controlling

Chapter 12

Real Time Clock

12. Real Time Clock

12.1. Overview

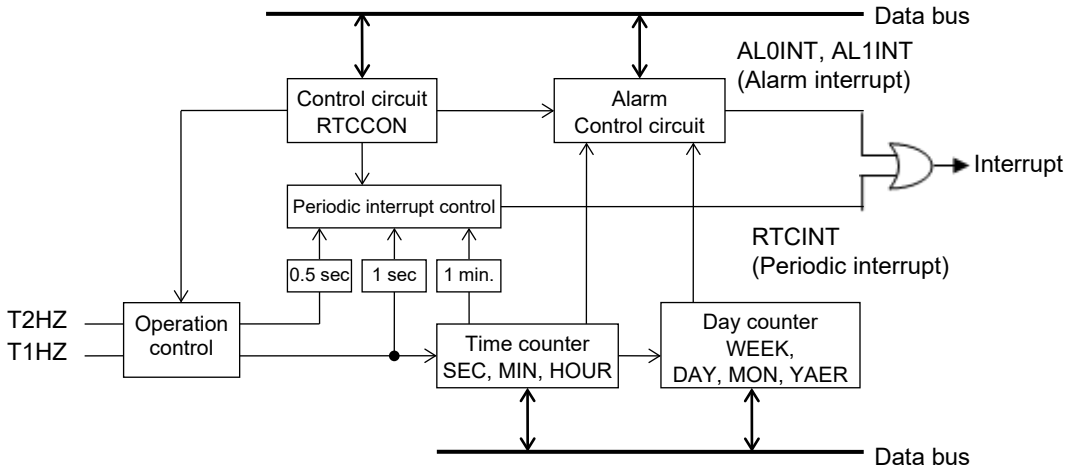
This LSI includes real time clock (RTC).
For input clocks, see Chapter 9, "Time Base Counter". For interrupt permission and interrupt request flags described in this chapter, see Chapter 7, "Interrupts".

12.1.1. Features

- Date counting function including year, month, day, and day of the week, and clock counting function including hour, minute, and second
- Auto calendar function with leap year checking function
- Periodic interrupt function with selection range of 0.5 seconds, 1 second, and 1 minute
- Alarm interrupt function according to coincidence of month, day, hour, and minute

12.1.2. Configuration

Figure 12-1 shows the configuration of the real time clock.



RTCCON: Real time clock control register

Figure 12-1 Configuration of Real Time Clock

12.2. Description of Registers

12.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_2300	Real time clock second register	RTCSEC	R/W	32	0x0000_0000
0x5C00_2304	Real time clock minute register	RTCMIN	R/W	32	0x0000_0000
0x5C00_2308	Real time clock hour register	RTCHOUR	R/W	32	0x0000_0000
0x5C00_230C	Real time clock week register	RTCWEEK	R/W	32	0x0000_0007
0x5C00_2310	Real time clock day register	RTCDAY	R/W	32	0x0000_0001
0x5C00_2314	Real time clock month register	RTCMON	R/W	32	0x0000_0001
0x5C00_2318	Real time clock year register	RTCYEAR	R/W	32	0x0000_0000
0x5C00_231C	Real time clock control register	RTCCON	R/W	32	0x0000_0000
0x5C00_2320	Real time clock alarm 0 minute register	AL0MIN	R/W	32	0x0000_0000
0x5C00_2324	Real time clock alarm 0 hour register	AL0HOUR	R/W	32	0x0000_0000
0x5C00_2328	Real time clock alarm 0 week register	AL0WEEK	R/W	32	0x0000_0000
0x5C00_232C	Real time clock alarm 1 minute register	AL1MIN	R/W	32	0x0000_0000
0x5C00_2330	Real time clock alarm 1 hour register	AL1HOUR	R/W	32	0x0000_0000
0x5C00_2334	Real time clock alarm 1 day register	AL1DAY	R/W	32	0x0000_0000
0x5C00_2338	Real time clock alarm 1 month register	AL1MON	R/W	32	0x0000_0000
0x5C00_2350	Real time clock hour/minute/second register	RTCHMS	R	32	0x0000_0000
0x5C00_2354	Real time clock year/month/day/week register	RTCYMDW	R	32	0x0001_0107
0x5C00_2360	Real time clock interrupt status register	RTCINTST	R/W	32	0x0000_0000

12.2.2. Real Time Clock Second Register (RTCSEC)

Address: 0x5C00_2300
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	RS[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCSEC is a special function register (SFR) to store decimal second data.

[Description of Bits]
- **RS[6:0]** (bit 6 to 0)
  The RS[6:0] bits are used to store decimal second data (0x00 to 0x59). During RTC operation, RTCSEC increments on the rising edge of the T1Hz signal of the low-speed time base counter (LTBC).

Note:
When setting second data in RTCSEC, stop RTC (RTCEN=0).
Do not write unrealistic second data to RTCSEC.
When reading RTCSEC, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.3. Real Time Clock Minute Register (RTCMIN)

Address: 0x5C00_2304
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	RM[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCMIN is a special function register (SFR) to store decimal minute data.

[Description of Bits]
- **RM[6:0]** (bit 6 to 0)
  The RM[6:0] bits are used to store decimal minute data (0x00 to 0x59). RTCMIN increments at occurrence of carry from RTCSEC (Second: 0x59→0x00).

Note:
When setting minute data in RTCMIN, stop RTC (RTCEN=0).
Do not write unrealistic minute data to RTCMIN.
When reading RTCMIN, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.4. Real Time Clock Hour Register (RTCHOUR)

Address: 0x5C00_2308
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RH[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCHOUR is a special function register (SFR) to store decimal hour data.

[Description of Bits]
- **RH[5:0]** (bit 5 to 0)
  The RH[5:0] bits are used to store decimal hour data (0x00 to 0x23). RTCnHOUR increments at occurrence of carry from RTCMIN (Minute: 0x59→0x00).

[Note]
When setting hour data in RTCHOUR, stop RTC (RTCEN=0).
Do not write unrealistic hour data to RTCHOUR.
When reading RTCHOUR, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.5. Real Time Clock Week Register (RTCWEEK)

Address: 0x5C00_230C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RW[2:0]		
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCWEEK is a special function register (SFR) to store decimal day-of-the-week data.

[Description of Bits]
- **RW[2:0]** (bit 2 to 0)
  The RW[2:0] bits are used to store decimal day-of-the-week data (0x01 to 0x07). RTCWEEK is incremented at occurrence of carry from RTCHOUR (Hour: 0x23→0ξ00). Day-of-the-week data can be associated with any actual day of the week since their relation is not fixed.

[Note]
When setting day-of-the-week data in RTCWEEK, stop RTC (RTCEN=0).
Do not write unrealistic day-of-the-week data to RTCWEEK.
When reading RTCWEEK, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.6. Real Time Clock Day Register (RTCDAY)

Address: 0x5C00_2310
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RD[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCDAY is a special function register (SFR) to store decimal day data.

[Description of Bits]
- **RD[5:0]** (bit 5 to 0)
  The RD[5:0] bit are used to store decimal day data (0x01 to 0x31). RTCDAY increments at occurrence of carry from RTCHOUR (Hour: 0x23→0x00).

[Note]
When setting day data in RTCDAY, stop RTC (RTCEN=0).
Do not write unrealistic day data to RTCDAY.
When reading RTCDAY, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.7. Real Time Clock Month Register (RTCMON)

Address: 0x5C00_2314
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RMO[4:0]				
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCMON is a special function register (SFR) to store decimal month data.

[Description of Bits]
- **RMO[4:0]** (bit 4 to 0)
  The RMO[4:0] bits are used to store decimal month data (0x01 to 0x12). RTCMON increments at occurrence of carry from RTCDAY (Day: 0x28/0x29/0x30/0x31→0x01).

[Note]
When setting month data in RTCMON, stop RTC (RTCEN=0).
Do not write unrealistic month data to RTCMON.
When reading RTCMON, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.8. Real Time Clock Year Register (RTCYEAR)

Address: 0x5C00_2318
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	RY[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCYEAR is a special function register (SFR) to store decimal year data.

[Description of Bits]
- **RY[7:0]** (bit 7 to 0)
  The RY[7:0] bits are used to store decimal year data (0x00 to 0x99). RTCYEAR increments at occurrence of carry from RTCMON (Month: 0x12→0x01).

[Note]
When setting month data in RTCYEAR, stop RTC (RTCEN=0).
Do not write unrealistic year data to RTCYEAR.
When reading RTCYEAR, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.9. Real Time Clock Control Register (RTCCON)

Address: 0x5C00_231C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	RIN[1:0]		RTCEN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCCON is a special function register (SFR) to control the real time clock.

[Description of Bits]
- **RTCEN** (bit 0)
  RTCEN is a bit to control the operation start/stop of the RTC.

RTCEN	Description
0	Stops RTC operation (initial value).
1	Starts RTC operation.

[Note]
Before Starting RTC operation, setting each RTC registers and clearing the interrupts.

- **RIN[1:0]** (bit 2 to 1)
  The RIN[1:0] bits are used to control a periodic interrupt. These bits allow selection of periodic interrupt prohibition, 0.5-second interrupt permission, 1-second interrupt permission, and 1-minute interrupt permission.

RIN[1]	RIN[0]	Description
0	0	Prohibits periodic interrupts (initial value).
0	1	Permits 0.5-second interrupts.
1	0	Permits 1-second interrupts.
1	1	Permits 1-minute interrupts.

[Note]
A 0.5-second interrupt and a 1-second interrupt request a RTC periodic interrupt (RTCINT) even if RTC is being stopped (RTCEN is "0"). A 1-minute interrupt does not request a RTC periodic interrupt while RTC is stopped.
Even if the T1HZ bit of LTBR register of time base counter is "1", RTCSEC is not +1 when RTCEN bit of the RTCCON register is "1" to "0".
Reset after waiting for low-speed clock 1 cycle after having made RTCEN "0" when reset time of RTC.

12.2.10. Real Time Clock Alarm 0 Minute Register (AL0MIN)

Address: 0x5C00_2320
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL0M[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL0MIN is a special function register (SFR) to set an alarm 0 interrupt time..
Set minute data in AL0MIN for generation of an alarm.

[Description of Bits]
- **AL0M[6:0]** (bit 6 to 0)
  The AL0M[6:0] bits are used to store decimal minute data (0x00 to 0x59) for generation of an alarm.

[Note]
Setting an unrealistic time in AL0MIN does not generate an alarm 0 interrupt (AL0INT).

12.2.11. Real Time Clock Alarm 0 Hour Register (AL0HOUR)

Address: 0x5C00_2324
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL0H[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL0HOUR is a special function register (SFR) to set an alarm 0 interrupt time.
Set hour data in AL0HOUR for generation of an alarm.

[Description of Bits]
- **AL0H[5:0]** (bit 5 to 0)
  The AL0H[5:0] bits are used to store decimal hour data (0x00 to 0x23) for generation of an alarm.

[Note]
Setting an unrealistic time in AL0HOUR does not generate an alarm 0 interrupt (AL0INT).

12.2.12. Real Time Clock Alarm 0 Week Register (AL0WEEK)

Address: 0x5C00_2328
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL0W[2:0]		
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL0WEEK is a special function register (SFR) to set an alarm 0 interrupt time.
Set week data in AL0WEEK for generation of an alarm.

[Description of Bits]
- **AL0W[2:0]** (bit 2 to 0)
  The AL0W[2:0] bits are used to store decimal week data (0x00 to 0x07) for generation of an alarm.

[Note]
When AL0WEEK is not used as comparison data for generating an alarm, set AL0WEEK to "0x00".

12.2.13. Real Time Clock Alarm 1 Minute Register (AL1MIN)

Address: 0x5C00_232C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL1M[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL1MIN is a special function register (SFR) to set an alarm 1 interrupt time..
Set minute data in AL1MIN for generation of an alarm.

[Description of Bits]
- **AL1M[6:0]** (bit 6 to 0)
  The AL1M[6:0] bits are used to store decimal minute data (0x00 to 0x59) for generation of an alarm.

[Note]
Setting an unrealistic time in AL1MIN does not generate an alarm 1 interrupt (AL1INT).

12.2.14. Real Time Clock Alarm 1 Hour Register (AL1HOUR)

Address: 0x5C00_2330
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL1H[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL1HOUR is a special function register (SFR) to set an alarm 1 interrupt time.
Set hour data in AL1HOUR for generation of an alarm.

[Description of Bits]
- **AL1H[5:0]** (bit 5 to 0)
  The AL1H[5:0] bits are used to store decimal hour data (0x00 to 0x23) for generation of an alarm.

[Note]
Setting an unrealistic time in AL1HOUR does not generate an alarm 1 interrupt (AL1INT).

12.2.15. Real Time Clock Alarm 1 Day Register (AL1DAY)

Address: 0x5C00_2334
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL1D[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL1DAY is a special function register (SFR) to set an alarm 1 interrupt time..
Set day data in AL1DAY for generation of an alarm.

[Description of Bits]
- **AL1D[5:0]** (bit 5 to 0)
  The AL1D[5:0] bits are used to store decimal day data (0x01 to 0x31) for generation of an alarm.

[Note]
Setting an unrealistic value for day in AL1DAY does not generate an alarm 1 interrupt (AL1INT).
When AL1DAY is not used as comparison data for generating an alarm, set AL1nDAY to "0x00".

12.2.16. Real Time Clock Alarm 1 Month Register (AL1MON)

Address: 0x5C00_2338
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	AL1MO[4:0]				
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AL1MON is a special function register (SFR) to set an alarm 1 interrupt time..
Set month data in AL1MON for generation of an alarm.

[Description of Bits]
- **AL1MO[4:0]** (bit 4 to 0)
  The AL1MO[4:0] bits are used to store decimal month data (0x01 to 0x12) for generation of an alarm.

[Note]
Setting an unrealistic value for month in AL1MON does not generate an alarm 1 interrupt (AL1INT).
When AL1MON is not used as comparison data for generating an alarm, set AL1MON to "0x00".

12.2.17. Real Time Clock Hour/Minute/Second Register (RTCHMS)

Address: 0x5C00_2350
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RHR[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	RMR[6:0]							–*	RSR[6:0]						
Access	–	R	R	R	R	R	R	R	–	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCHMS is a special function register (SFR) to indicate decimal second data, decimal minute data, and decimal hour data .

[Description of Bits]
- **RSR[6:0]** (bit 6 to 0)
  The RSR[6:0] bits are same the value as RS[6:0] bits of RTCSEC.

- **RMR[6:0]** (bit 14 to 8)
  The RMR[6:0] bits are same the value as RM[6:0] bits of RTCMIN.

- **RHR[5:0]** (bit 21 to 16)
  The RHR[5:0] bits are same the value as RH[5:0] bits of RTCHOUR.

[Note]
When reading RTCHMS, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.18. Real Time Clock Year/Month/Day/Week Register (RTCYMDW)

Address: 0x5C00_2354
Access: R
Access size: 32 bit
Initial value: 0x0001_0107

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	RYR[7:0]								–*	–*	–*	RMOR[4:0]				
Access	R	R	R	R	R	R	R	R	–	–	–	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	RDR[5:0]						–*	–*	–*	–*	–*	RWR[2:0]		
Access	–	–	R	R	R	R	R	R	–	–	–	–	–	R	R	R
Initial value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RTCYMDW is a special function register (SFR) to indicate decimal day-of-the-week data, day, month, and year.

[Description of Bits]
- **RWR[2:0]** (bit 2 to 0)
  The RWR[2:0] bits are same the value as RW[2:0] bits of RTCWEEK.

- **RDR[5:0]** (bit 13 to 8)
  The RDR[5:0] bits are same the value as RD[5:0] bits of RTCDAY.

- **RMOR[4:0]** (bit 20 to 16)
  The RMOR[4:0] bits are same the value as RMO[4:0] bits of RTCMON.

- **RYR[7:0]** (bit 31 to 24)
  The RYR[7:0] bits are same the value as RY[7:0] bits of RTCYEAR.

[Note]
When reading RTCYMDW, read consecutively it twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock.

12.2.19. Real Time Clock Interrupt Status Register (RTCINTST)

Address: 0x5C00_2360
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	AL1 INT	AL0 INT	RTC INT
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
The RTCINTST register is used to display the source of interrupt.

[Description of Bits]

- **RTCINT (bit 0)**
  This bit is set to "1" when RTCINT interrupt request is generated. The RTCINT interrupt can be clear by writing "1" to this bit.

- **AL0INT (bit 1)**
  This bit is set to "1" when AL0INT interrupt request is generated. The AL0INT interrupt can be clear by writing "1" to this bit.

- **AL1INT (bit 2)**
  This bit is set to "1" when AL1INT interrupt request is generated. The AL1INT interrupt can be clear by writing "1" to this bit.

12.3. Description of Operation

RTC stops operation after reset release. As each bit of the date and time registers (RTCSEC, RTCMIN, RTCHOUR, RTCWEEK, RTCDAY, RTCMON, and RTCYEAR) is the initial value, set a date and a time through the software.
Set a date and a time after stopping RTC operation by setting the RTCEN bit of RTCCON to "0".
When starting RTC operation, first reset the low-speed time base counter by writing in the low-speed time base counter register (LTBR) of the low-speed time base counter (LTBC), then set the RTCEN bit to "1" to start RTC operation. By resetting the time base counter, the count in the second register (RTCSEC) can be incremented about one second after the start of RTC operation. See Chapter 9, "Time Base Counter," for the low-speed time base counter.
Table 10-1 lists the count values of each register.

Table 12-1 Count Values of Each Register

Register name		Count value	Remarks
Second register	RTCSEC	0x00 to 0x59	
Minute register	RTCMIN	0x00 to 0x59	
Hour register	RTCHOUR	0x00 to 0x23	24-hour system
Week register	RTCWEEK	0x01 to 0x07	
Day register	RTCDAY	0x01 to 0x31	Jan., Mar., May, Jul., Aug., Oct., Dec.
		0x01 to 0x30	Apr., Jun., Sep., Nov.
		0x01 to 0x28	Feb. without leap day
		0x01 to 0x29	Feb. with leap day
Month register	RTCMON	0x01 to 0x12	
Year register	RTCYEAR	0x00 to 0x99	

When reading data of each register of RTC, read data from all the registers twice and check that the values coincide to prevent the reading of undefined data during counting.

RTC can generate a periodic interrupt (RTCINT) that occurs at a fixed cycle, an alarm 0 interrupt (AL0INT) that occurs as a result of the coincidence of week, hour, or minute data and an alarm 1 interrupt (AL1INT) that occurs as a result of the coincidence of month, day, hour, or minute data.

Options available for periodic interrupts by using the RINT1 and RINT0 bit of RTCCON include periodic interrupt prohibition, 0.5-second interrupt, 1-second interrupt, and 1-minute interrupt.

An alarm 0 interrupt (AL0INT) occurs when carry (RTCSEC: 59 seconds→00 seconds) from the second register (RTCSEC) occurs and the value of the real time clock alarm 0 register (AL0WEEK, AL0HOUR or AL0MIN) and the value of the week, hour, or minute register (RTCWEEK, RTCHOUR, or RTCMIN) coincide.

An alarm 1 interrupt (AL1INT) occurs when carry (RTCSEC: 59 seconds→00 seconds) from the second register (RTCSEC) occurs and the value of the real time clock alarm 1 register (AL1MON, AL1DAY, AL1HOUR, or AL1MIN) and the value of the month, day, hour, or minute register (RTCMON, RTCDAY, RTCHOUR, or RTCMIN) coincide.

When AL0WEEK, AL1MON, or AL1DAY is not used as comparison data of the alarm, set "0x00". For instance, to set the alarm to 8:30 a.m. of each day, set "0x00" in AL0WEEK and set data of hour 8 and minute 30 in AL0HOUR and AL0MIN respectively.

Chapter 13

1 kHz Timer (1kHzTM)

13. 1 kHz Timer (1kHzTM)

13.1. Overview

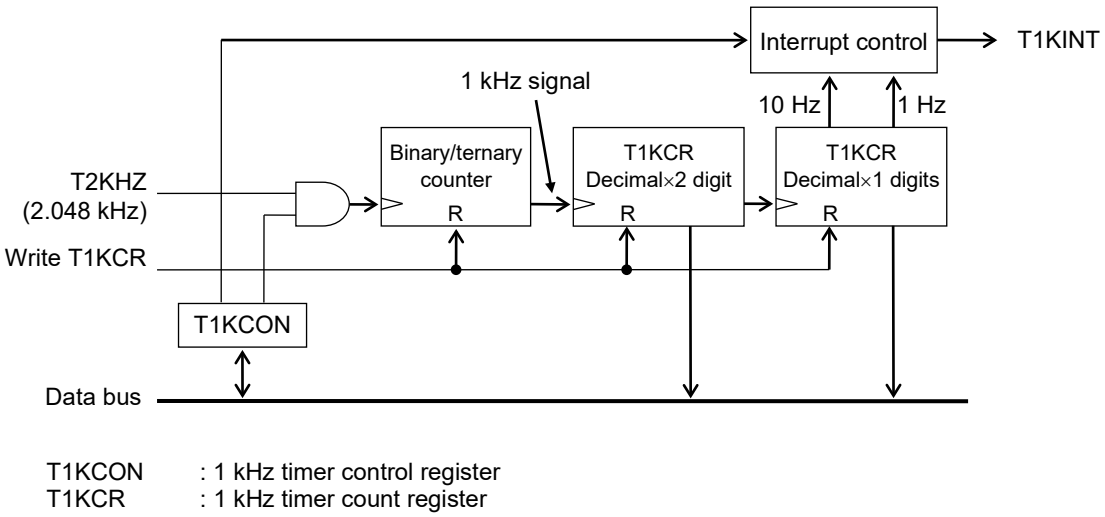
This LSI includes a 1 kHz timer to measure 1/1000 seconds.
The 1 kHz timer counts the 1 kHz signal created by dividing the T2KHZ output frequency (2.048 kHz) of the low-speed time base counter (LTBC) and generates a 10 Hz or 1 Hz interrupt (1 kHz timer interrupt).
With the 1 kHz timer, 1/1000 second, which is difficult to generate on a time-base-counter basis, represented by a decimal number can be obtained easily. The timer can be applied to period measurement for stopwatches.
For the timer base counter, see Chapter 9, "Time Base Counter".

13.1.1. Features

- 10 Hz/1 Hz interrupt select function

13.1.2. Configuration

Figure 13-1 shows the configuration of the 1 kHz timer.



T1KCON : 1 kHz timer control register
T1KCR : 1 kHz timer count register

Figure 13-1 Configuration of 1 kHz Timer

13.2. Description of Registers

13.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_2200	1 kHz timer count register	T1KCRL	R/W	32	0x0000_0000
0x5C00_2204	1 kHz timer control register	T1KCON	R/W	32	0x0000_0000

13.2.2. 1 kHz Timer Count Register (T1KCR)

Address: 0x5C00_2200
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*
Access	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	—*	—*	—*	T1KC[12:0]												
Access	—	—	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
T1KCR is special function registers (SFRs) to read the decimal count values of the 1 kHz timer.
When the write operation to T1KCR, the valid bit of T1KCR is "0".

[Description of Bits]
- **T1KC[12:0]** (bit 12 to 0)
  T1KC[12:0] indicate the count values of the 1 kHz timer.

T1KC[12] is a figure for 1 second.
T1KC[11:8] is a figure for 1/10 second.
T1KC[7:4] is a figure for 1/100 second.
T1KC[3:0] is a figure for 1/1000 second.

Stores the decimal number count level corresponding to the above. (becomes the count to 0-1999).

Count Level (decimal)	**T1KC**												
	12	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
…	…												
99	0	0	0	0	0	1	0	0	1	1	0	0	1
100	0	0	0	0	1	0	0	0	0	0	0	0	0
…	…												
999	0	1	0	0	1	1	0	0	1	1	0	0	1
1000	1	0	0	0	0	0	0	0	0	0	0	0	0
…	…												
1998	1	1	0	0	1	1	0	0	1	1	0	0	0
1999	1	1	0	0	1	1	0	0	1	1	0	0	1

13.2.3. 1 kHz Timer Control Register (T1KCON)

Address: 0x5C00_2204
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*
Access	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	—*	T1KSEL[2:0]			T1KRUN
Access	—	—	—	—	—	—	—	—	—	—	—	—	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
T1KCON is a special function register (SFR) to control the 1 kHz timer.

[Description of Bits]
- **T1KRUN** (bit 0)
  The T1KRUN bit is used to control start/stop of the count operation of the 1 kHz timer counter.

T1KRUN	Description
0	Stops 1 kHz timer operation (initial value).
1	Starts 1 kHz timer operation.

- **T1KSEL[2:0]** (bit 3 to 1)
  The T1KSEL[2:0] bit is used to select the interrupt period of the 1 kHz timer. The 80Hz, 60Hz, 40Hz, 20Hz, 10Hz, or 1Hz interrupt can be selected.

T1KSEL2	T1KSEL1	T1KSEL0	Description
0	0	0	10 Hz interrupt (initial value)
0	0	1	20 Hz interrupt
0	1	0	1 Hz interrupt
0	1	1	1 Hz interrupt
1	0	0	40 Hz interrupt
1	0	1	60 Hz interrupt
1	1	0	80 Hz interrupt
1	1	1	1 Hz interrupt

13.3. Description of Operation

By setting the T1KRUN bit of the 1kHz timer control register (T1KCON) to "1", the 1kHz timer starts counting of the 1kHz timer counter registers (T1KCR).
By dividing the T2KHz signal (2.048kHz) of the low-speed timer base counter (LTBC) by the binary/ternary counter, the timer generates a 1kHz signal. Based on the 1kHz signal, a 1kHz timer interrupt request signal (T1KINT) is generated by the decimal counters of T1KCR. The period of the 1kHz timer interrupt can be selected between the 10Hz interrupt or 1Hz interrupt using the T1KSEL bit of T1KCON.
When write operation is performed for T1KCR, the value of the binary/ternary counter and the value of T1KCR is cleared to "0".
Data can be read from T1KCR. When reading data from T1KCR in the 1kHz timer operation start state, read T1KCR twice and check that the values match to prevent the reading of undefined data during counting.

Chapter 14

Watchdog Timer

14. Watchdog Timer

14.1. Overview

Watchdog timer is free run counter that is used for detection of program abnormal behavior.
The watchdog timer starts counting automatically after system reset release and requests WDT interrupt when the first overflow occurs.
When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 7, "Interrupts," and for WDT interrupt see Chapter 4, "Reset Function".

14.1.1. Features

- Free running (stop setting in DEEP-HALT and ULTRA-DEEP-HALT mode is available)
- Count low-speed clock 128 period.
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s @LSCLK=32.768kHz) selectable by software
- Requests a WDT interrupt (non-maskable interrupt) by the first overflow
- Reset generated by the second overflow

14.1.2. Configuration

Figure 14-1 shows the configuration of the watchdog timer.

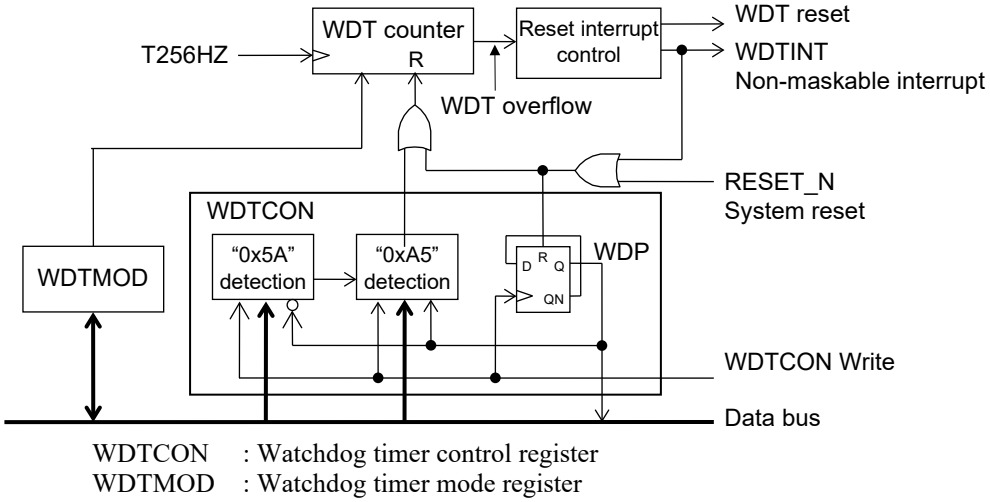


Figure 14-1 Configuration of Watchdog Timer

14.2. Description of Registers

14.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_2000	Watchdog timer control register	WDTCON	R/W	32	0x0000_0000
0x5C00_2004	Watchdog timer mode register	WDTMOD	R/W	32	0x0000_0082

14.2.2. Watchdog Timer Control Register (WDTCON)

Address: 0x5C00_2000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	d[7:1]							WDP/ d[0]
Access	–	–	–	–	–	–	–	–	W	W	W	W	W	W	W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
WDTCON is a special function register (SFR) to control the Watchdog Timer.
When some data is written to WDTCON, the value of the internal pointer (WDP) is reversed.
WDT counter is cleared when "0x5A" and "0xA5" is written to WDTCON in succession.
The value in WDP is read from bit0 when WDTCON is read. In this time "0" is read from bit7 to bit1.
WDP is set to "0" at system reset and at WDT counter overflow.

To clear the WDT counter, write "0x5A" when WDP state is "0", and then write "0xA5" when WDP state is "1".
This register requires byte access always.

[Description of Bits]
- WDP (bit 0)

The value of the internal pointer (WDP) is read from this bit. The WDP is set to "0" at the system reset or the WDT counter overflow, and then the WDP is inverted every writing to WDTCON.

- d[7:0] (bit 7 to 0)

These bits are used to write data to clear the WDT counter. The WDT counter can be cleared by writing "0x5A" with the internal pointer (WDP) "0", then writing "0xA5" with the internal pointer (WDP) "1".

[Note]
When the WDT interrupt (WDTINT) is occurred by the WDT counter first overflow, the WDT counter and the internal pointer (WDP) are initialized for 1/2 clock period of low-speed clock (approximately 15.26us@32.768kHz). Therefore the writing to the WDTCON becomes invalid during the period and WDP is not reversed. In processing clear WDT when WDT interrupt occur and system clock is in high-speed clock state, Confirm that WDP is inverted by writing to WDTCON and confirm the writing to WDTCON is done normally.

14.2.3. Watchdog Timer Mode Register (WDTMOD)

Address: 0x5C00_2004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0082

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	HLTEN	–*	–*	–*	–*	–*	WDT[1:0]	
Access	–	–	–	–	–	–	–	–	R/W	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
WDTMOD is a special function register to set the overflow period of the WDT counter.

[Description of Bits]
- WDT[1:0] (bit 1 to 0)

These bits are used to select an overflow period of the watchdog timer.
The WDT1 and WDT0 bit set an overflow period (T_{WOV}) of the WDT counter. It is selectable from the following.

WDT[1]	WDT[0]	Description
0	0	4096 counts at LSCLK (125 ms*)
0	1	16384 counts at LSCLK (500 ms*)
1	0	65536 counts at LSCLK (2 s*) (initial value)
1	1	262144 counts at LSCLK (8 s*)

*: where LSCLK = 32.768kHz.

- HLTEN (bit 7)

This bit sets the count up or not during DEEP-HALT and ULTRA-DEEP-HALT mode.

HLTEN	Description
0	Stop counting up during DEEP-HALT and ULTRA-DEEP-HALT mode
1	Keep counting up during DEEP-HALT and ULTRA-DEEP-HALT mode (initial value)

14.3. Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock (LSCLK) oscillation starts.
The WDT counter can be cleared by writing "0x5A" with the internal pointer (WDP) "0", then writing "0xA5" with the internal pointer (WDP) "1".
The WDP is set to "0" at the time of system reset or the WDT counter overflow. And it is inverted whenever data is written to WDTCON.
A watchdog timer interrupt (WDTINT) occurs when the WDT counter is not cleared within the WDT counter overflow period (T_{WOV}). And then WDT reset occurs and the mode shifts to a system reset mode, when the watchdog timer interrupt and overflow occur again before the WDT counter is cleared by the software processing performed.
For the overflow period (T_{WOV}) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 12-1.

Table 14-1 Clear Period of WDT Counter

WDT[1]	WDT[0]	T_{WOV}	T_{WCL}
0	0	4096 counts at LSCLK (125 ms*)	3968 counts at LSCLK (Approx. 121 ms*)
0	1	16384 counts at LSCLK (500 ms*)	16256 counts at LSCLK (Approx. 496 ms*)
1	0	65536 counts at LSCLK (2000 ms*)	65408 counts at LSCLK (Approx. 1996 ms*)
1	1	262144 counts at LSCLK (8000 ms*)	262016 count at LSCLK (Approx. 7996 ms*)

*: where LSCLK = 32.768kHz. T_{WOV} and T_{WCL} depend on a frequency of the LSCLK.

[Note]
WDT counter clock is T256HZ that is divided by 128 of LSCLK. Therefore, keep on supply the LSCLK during not reset and STOP-mode conditions.

The time of Table 14-1 is changed with the frequency of the LSCLK to be used. It is calculable by the frequency of low speed crystal oscillator to be used as follows.

Ex) Operate by LSCLK=32.768kHz (set WDT[1:0]=00)

T_{WOV} : 1 / ((32.768[kHz]) / 128 [dividing]) * 32 [clock] = 125 [msec]

Figure 14-2 shows an example of watchdog timer operation.

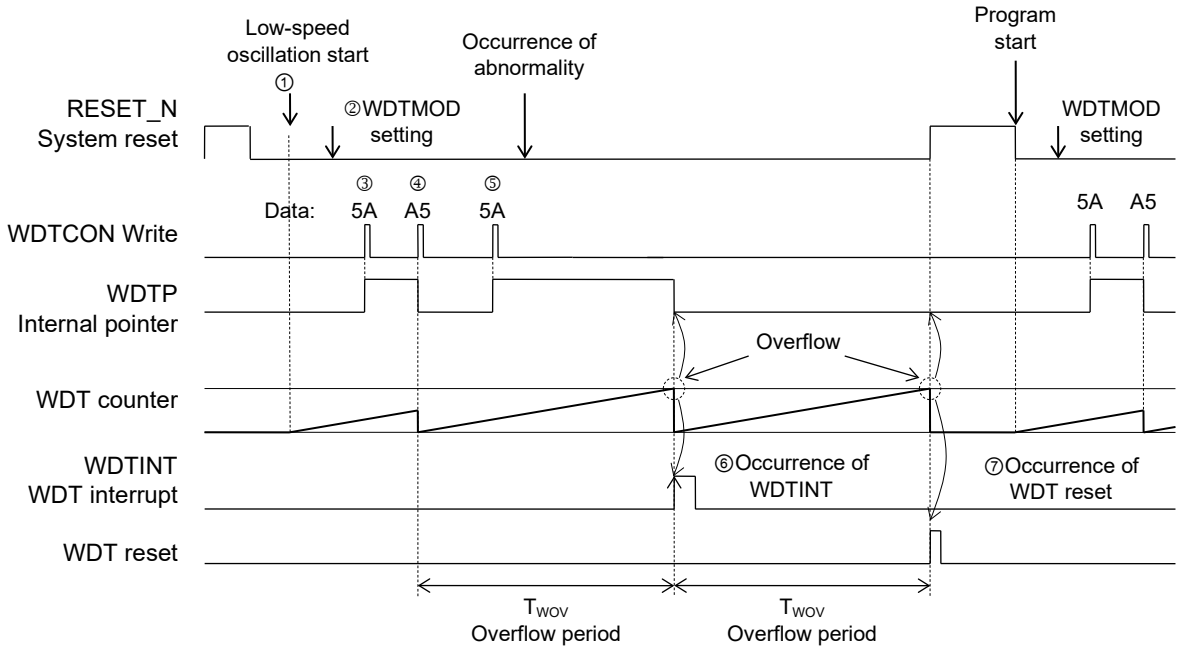


Figure 14-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.
③ Write "0x5A" to WDTCON. (Internal pointer 0→1)
④ Write "0xA5" to WDTCON and clear the WDT counter. (Internal pointer 1→0)
⑤ Write "0x5A" to WDTCON. (Internal pointer 0→1)
⑥ If abnormalities occur and the writing of "0xA5" is not performed, WDT counter overflows. Watchdog timer interrupt occurs because the overflow is the first overflow after reset of WDT counter. In addition, during the period of the half clock of LSCLK, WDT counter and internal pointer are initialized. While it is initialized, the writing to WDTCON becomes invalid, and internal pointer doesn't invert.
⑦ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

[Note]
- In STOP mode, the watchdog timer operation also stops. When the WDT interrupt occurs, the HALT (ULTRA-DEEP-HALT, DEEP-HALT, HALT-H, HALT) mode is released.
- The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

14.3.1. The process example when not using Watchdog Timer

Watchdog timer is a free-run counter, so it cannot be stopped. Even when the watchdog timer function is not used as fail-safe function, it is necessary to clear the WDT counter.
The example programming code is shown, in order to clear the WDT counter when WDT interrupt occurs and control the system reset by WDT.

The example of programming code:

```
do
 {
   WDT->WDTCON = 0x5a;
 } while((WDT->WDTCON) & 0x1 != 0x1)
   WDT->WDTCON = 0xa5;
```

Chapter 15

Synchronous Serial Port (SSIO)

15. Synchronous Serial Port

15.1. Overview

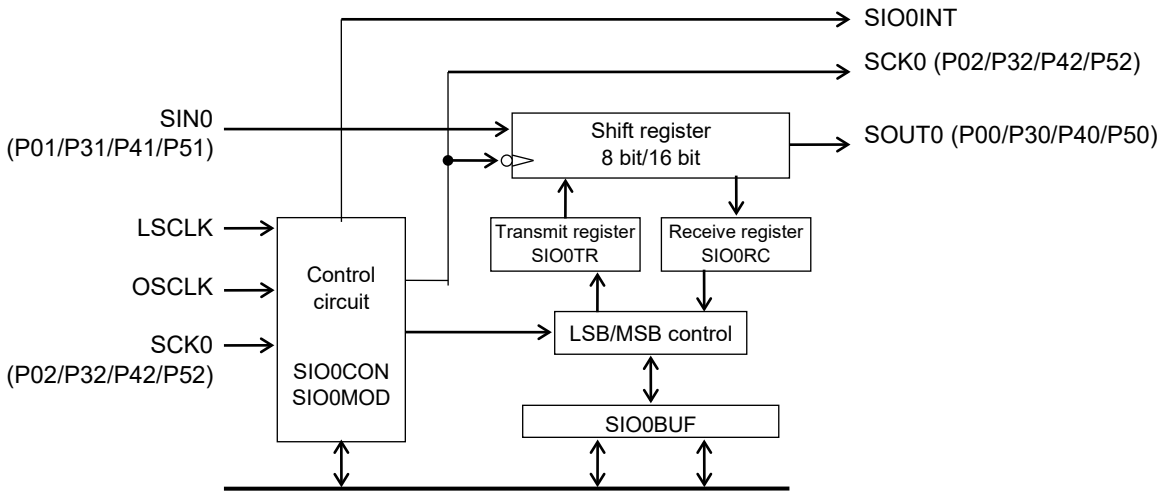
This LSI includes one channel of the 8/16 bit synchronous serial port (SSIO) and can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.
The use of SSIO requires the function setting of the ports 0, 3, 4 and 5. For the port function setting, see Chapter 22"Port".

15.1.1. Features

- Master or slave selectable
- MSB first or LSB first selectable
- 8 bit length or 16 bit length selectable fro the data length
- Selectable phase and polarity of clock

15.1.2. Configuration

Figure **15**-1 shows the configuration of the synchronous serial port.



SIO0BUF: Serial port transmit/receive buffer
SIO0CON: Serial port control register
SIO0MOD: Serial port mode register

Figure 15-1Configuration of Synchronous Serial Port

15.1.3. List of Pins

Pin name	I/O	Description
SIN0	I	Receive data input.
SCK0	I/O	Synchronous clock input/output.
SOUT0	O	Transmit data output.

15.2. Description of Registers

15.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4100_0000	Serial port 0 transmit/receive buffer	SIO0BUF	R/W	32	0x0000_0000
0x4100_0004	Serial port 0 control register	SIO0CON	R/W	32	0x0000_0000
0x4100_0008	Serial port 0 mode register	SIO0MOD	R/W	32	0x0000_0000

15.2.2. Serial Port 0 Transmit/Receive Buffer (SIO0BUF)

Address: 0x4100_0000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	S0B[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SIO0BUF are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port 0.
When data is written in SIO0BUF, the data is written in the transmit registers (SIO0TR) and when data is read from SIO0BUF, the contents of the receive registers (SIO0RC) are read.
When the data length is 16 bit length, S0B[15:0] is valid.
When the data length is 8 bit length, S0B[7:0] is valid.

15.2.3. Serial Port 0 Control Register (SIO0CON)

Address: 0x4100_0004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	S0EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SIO0CON is a special function register (SFR) to control the synchronous serial port 0.

[Description of Bits]

- **S0EN** (bit 0)

The S0EN bit is used to specify start of synchronous serial communication. Writing a “1” to this bit starts 8/16 bit data communication. This bit is set to “0” automatically when 8/16 bit data communication is terminated.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

[Note]
Set the mode of SSIO and pin setting before S0EN is set to “1”

15.2.4. Serial Port 0 Mode Register (SIO0MOD)

Address: 0x4100_0008
Access: R/W
Access size: 32bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	S0 NEG	S0 CKT	–*	S0CK[2:0]			–*	–*	–*	–*	S0LG	S0MD[1:0]		S0 DIR
Access	–	–	R/W	R/W	–	R/W	R/W	R/W	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SIO0MOD is a special function register (SFR) to set mode of the synchronous serial port 0.

[Description of Bits]

- **S0DIR** (bit 0)

The S0DIR is used to select LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

- **S0MD[1:0]** (bit 2 to 1)

The S0MD[1:0] bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port.

S0MD1	S0MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

- **S0LG** (bit 3)

The S0LG bit is used to specify the bit length of the transmit/receive buffer, 8 bit or 16 bit length.

S0LG	Description
0	8 bit length (initial value)
1	16 bit length

- **S0CK[2:0]** (bit 10 to 8)

The S0CK[2:0] bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S0CK[2]	S0CK[1]	S0CK[0]	Description
0	0	0	1/1 LSCLK (initial value)
0	0	1	1/2 LSCLK
0	1	0	1/4 OSCLK
0	1	1	1/8 OSCLK
1	0	0	1/16 OSCLK
1	0	1	1/32 OSCLK
1	1	0	External clock 0 (SCK0)
1	1	1	reserved

- **S0CKT** (bit 12)

The S0CKT bit is used to select a tansfer clock output phase.

S0CKT	Description
0	Clock type 0: Clock is output with a “H” level being the default. (Initial value)
1	Clock type 1: Clock is output with a “L” level being the default.

- **S0NEG** (bit 13)

The S0NEG bit is used to select the positive or negative logic of the transfer clock output.

S0NEG	Description
0	Positive logic (Initial value)
1	Negative logic

[Note]
- Do not change any of the SIO0MOD register settings during transmission/reception.
- SCK0 Max clock input frequency is 1/4 of SYSCLK or 2MHz at slave mode.
- SCK0 Max clock output frequency is 4MHz if using P32, P42, and P52 as SCK0 in master mode.
- SCK0 Max clock output frequency is 2MHz if using P02 as SCK0 in master mode.

15.3. Description of Operation

15.3.1. Transmit Operation

When "1" is written to the S0MD[1] bit and "0" is written to the S0MD[0] bit of the serial mode register (SIO0MOD), this LSI is set to a transmit mode.
When transmit data is written to the serial port transmit/receive buffer (SIO0BUF) and the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission starts. When transmission of 8/16 bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Transmit data is output from SOUT0 pin.
When an internal clock is selected in the serial port mode register (SIO0MOD), the LSI is set to a master mode and when an external clock (SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD) enables selection of MSB first/LSB first.
The transmit data output pin (SOUT0) and transfer clock input/output pin (SCK0) must be set to the tertiary functions.
Figures 15-2, 15-3, 15-4 and 15-5 show the transmit operation waveforms of the synchronous serial ports for "clock type 0 and positive-logic", "clock type 0 and negative-logic", "clock type 1 and positive-logic" and "clock type 1 and negative-logic", respectively (8 bit length, LSB first).

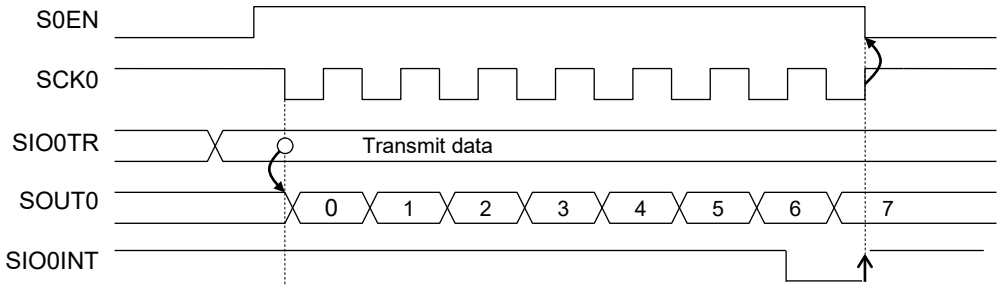


Figure 15-2 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8 bit Length, LSB first, Positive Logic)

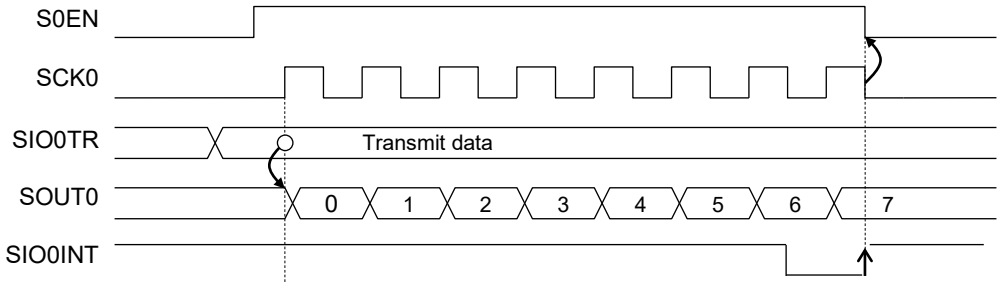


Figure 15-3 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8 bit Length, LSB first, Negative Logic)

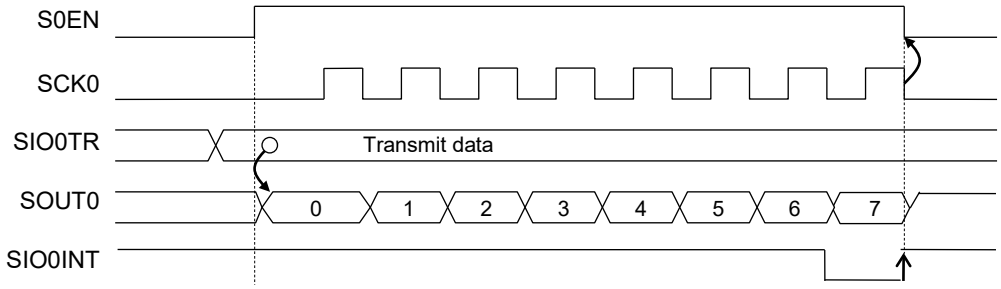


Figure 15-4 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8 bit Length, LSB first, Positive Logic)

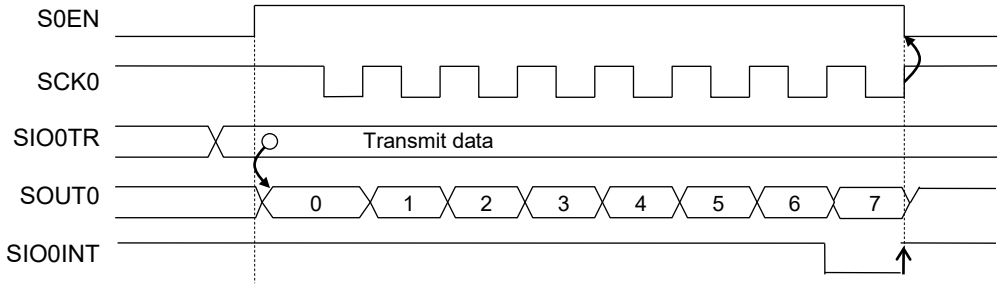


Figure 15-5 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8 bit Length, LSB first, Negative Logic)

15.3.2. Receive Operation

When "0" is written to the S0MD[1] bit and "1" is written to the S0MD[0] bit of the serial mode register (SIO0MOD), this LSI is set to a receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", reception starts. When reception of 8/16 bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the SIN0 pin.
When an internal clock is selected in the serial port mode register (SIO0MD), the LSI is set to a master mode and when an external clock (SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD) enables selection of MSB first or LSB first.
The receive data input pin (SIN0) and transfer clock input/output pin (SCK0) must be set to the tertiary function.
Figures 15-6,15-7,15-8 and 15-9 show the receive operation waveforms of the synchronous serial ports for "clock type 0 and positive-logic", "clock type 0 and negative-logic", "clock type 1 and positive-logic" and "clock type 1 and negative-logic", respectively (8 bit length, MSB first).

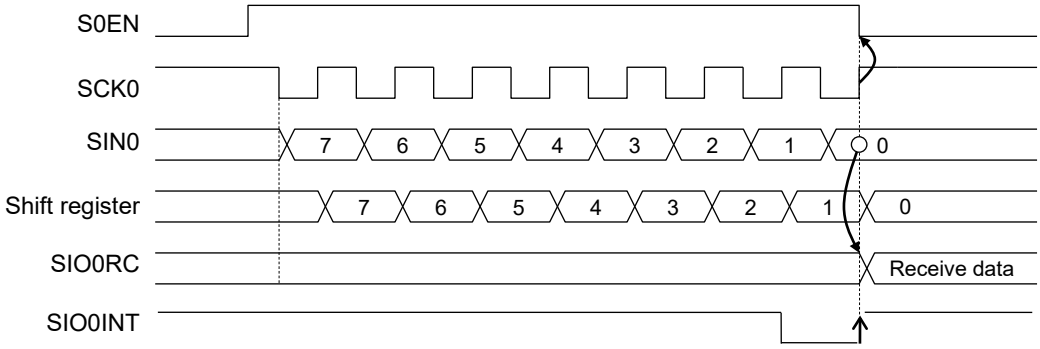


Figure 15-6 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8 bit Length, MSB first, Positive Logic)

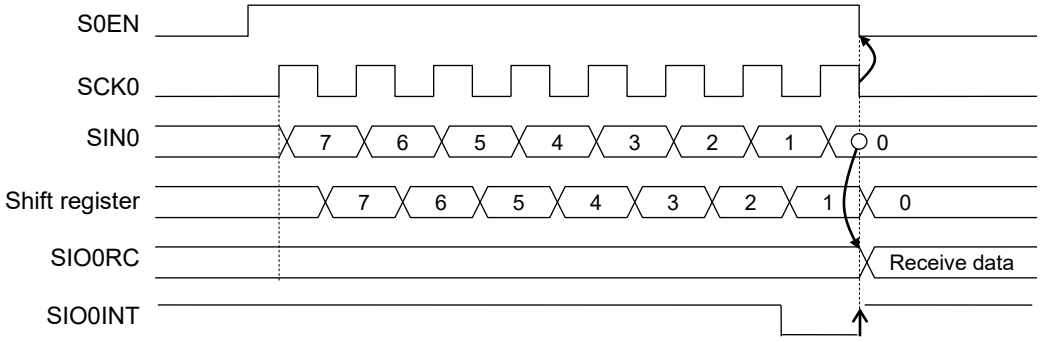


Figure 15-7 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8 bit Length, MSB first, Negative Logic)

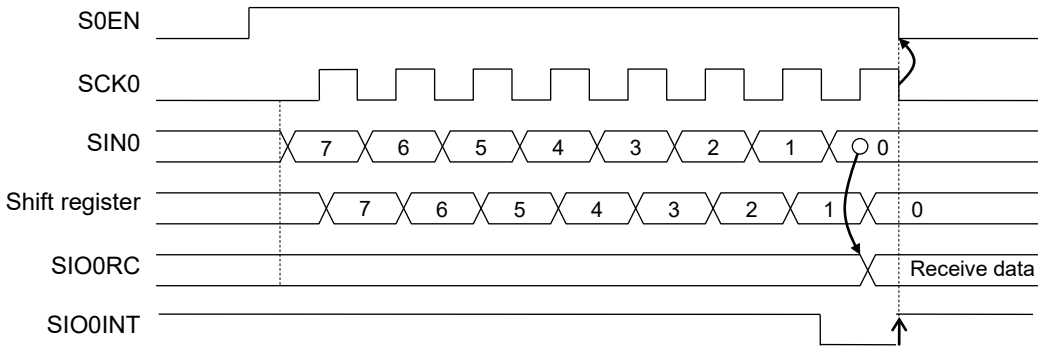


Figure 15-8 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8 bit Length, MSB first, Positive Logic)

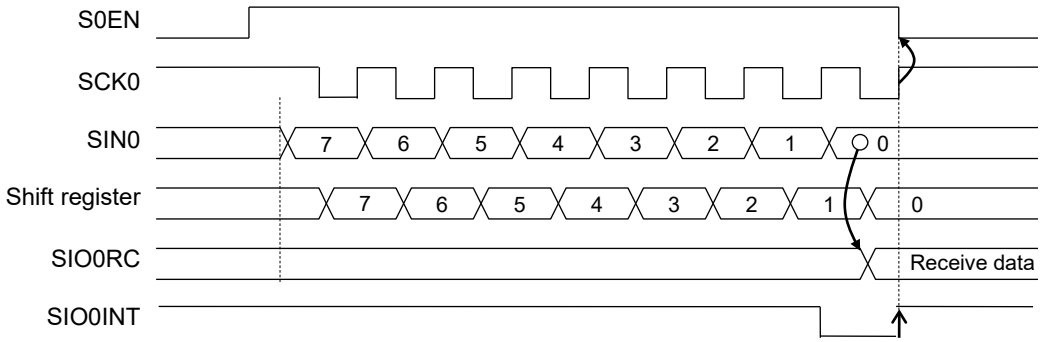


Figure 15-9 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8 bit Length, MSB first, Negative Logic)

[Note]
When the SOUT0 pin is set to the tertiary function output in receive mode, a “H” level is output from the SOUT0 output pin.

15.3.3. Transmit/Receive Operation

When "1" is written to the S0MD[1] bit and "1" is written to the S0MD[0] bit of the serial mode register (SIO0MOD), this LSI is set to a transmit/receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission/reception starts. When transmission/reception of 8/16 bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the SIN0 pin, and transmit data is output from the SOUT0 pin.
When an internal clock is selected in the serial port mode register (SIO0MD), the LSI is set to a master mode and when an external clock (SCK0) is selected, the LSI is set ot a slave mode.
The serial port mode register (SIO0MOD) enables selection of MSB first or LSB first.
The receive data input pin (SIN0), the transmit data output pin (SOUT0), and transfer clock input/output pin (SCK0) must be set to the tertiary function.
Figure 15-10 shows the transmit/receive operation waveforms of the synchronous serial port (16 bit length, LSB first, clock types 0 and positive-logic).

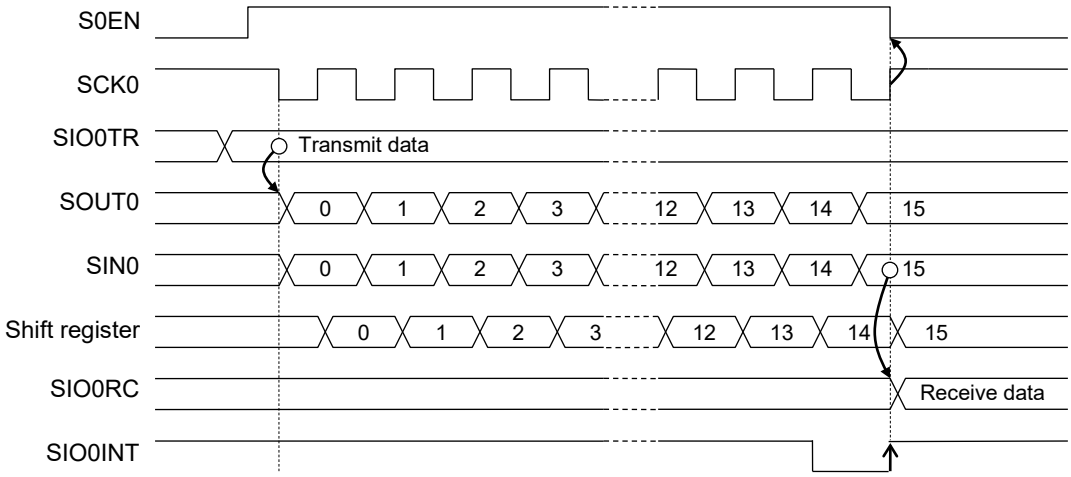


Figure 15-10 Transmit/Receive Operation Waveforms of Synchronous Serial Port
(16 bit Length, LSB first, Clock Type 0 and positive-logic)

15.3.4. Pin Settings

To enable the SSIO function, the applicable bit of each related port register needs to be set. See Chapter 22, "Port" for details about the port registers.
For SIN0, SCK0 and SOUT0, the ports can be selected from several possibilities.
Be sure to select one of the following combinations of ports for SIN0/SCK0/SOUT0.

	SSIO pin	Combination #1	Combination #2	Combination #3	Combination #4
SSIO	SIN0,SCK0, SOUT0	P01,P02, P00	P31,P32, P30	P41,P42, P40	P51,P52, P50

[Note]
If using P32, P42, and P52 as SCK0 in master mode, SCK0 Max clock output frequency is 4MHz.
If using P02 as SCK0 in master mode, SCK0 Max clock output frequency is 2MHz.

Chapter 16

Synchronous Serial Port with FIFO (SSIOF)

16. Synchronous Serial Port with FIFO (SSIOF)

16.1. General Description

This LSI includes one channel of the 8/16 bit synchronous serial port (SSIO) with FIFO and can also be used to control the device incorporated with the SPI interface.
The use of SSIOF requires the function setting of the ports 2, 3, 4 and 5. For the port function setting, see Chapter 22 "Port".

16.1.1. Features

- Full-duplex data transfer
- Master or Slave mode can be selected
- Built-in 16-stage FIFO on each of transmit- and receive-sides
- For the transfer size, 8 bit (byte) or 16 bit (half word) selectable
- The number of received data that cause interrupts can be set to 1 to 16 data.
- The number of untransmitted data that cause interrupts can be set to 0 to 15 data.
- Either LSB first or MSB first can be selected
- The polarity and phase of the serial clock are selectable
- In Master mode, the HSCLK 2 to 2046-division clocks can be selected as the sync clock (1023 types)
- In Master mode, the interval before/after transfer can be controlled
- State bit indicating transmission/receive complete and FIFO state
- Detects a mode fault error to avoid multi-master bus contention
- Detects a write overflow error if any further writing is attempted when the transmit FIFO is in the full state
- Generates an interrupt when the transmit/receive FIFO is in a specific state or when a cause such as mode fault error occurs
- Generates transmission/receive DMA request

16.1.2. Configuration

Figure 16-1 shows the configuration of the SSIOF.

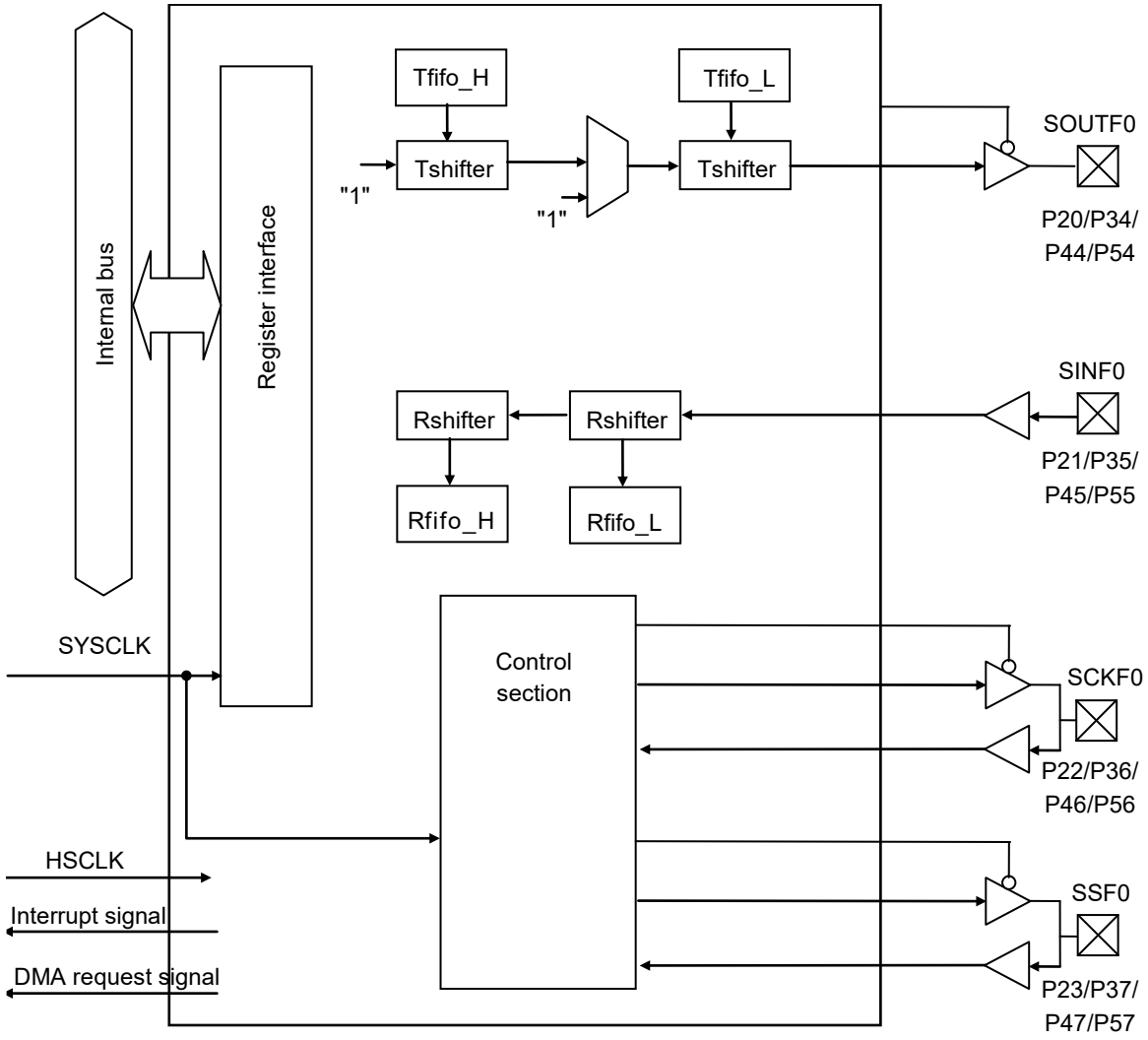


Figure 16-1 Configuration of SSIOF

16.1.3. List of Pins

Pin Name	I/O	Function
SOUTF0	O	Master serial output/slave serial output signal
SINF0	I	Master serial input/slave serial input signal
SCKF0	I/O	Baud rate clock
SSF0	I/O	Slave selection signal

16.2. Description of Registers

16.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4100_0800	SIOF0 control register	SF0CTRL	R/W	32	0x0000_0000
0x4100_0804	SIOF0 interrupt control register	SF0INTC	R/W	32	0x0000_0000
0x4100_0808	SIOF0 transfer interval control register	SF0TRAC	R/W	32	0x0000_0002
0x4100_080C	SIOF0 baud rate register	SF0BRR	R/W	32	0x0000_5002
0x4100_0810	SIOF0 status register	SF0SRR	R	32	0x0000_1400
0x4100_0814	SIOF0 status clear register	SF0SRC	W	32	0x0000_0000
0x4100_0818	SIOF0 FIFO status register	SF0FSR	R	32	0x0000_0000
0x4100_081C	SIOF0 write data register	SF0DWR	R/W	32	0x0000_0000
0x4100_0820	SIOF0 read data register	SF0DRR	R	32	0x0000_0000

16.2.2. SIOF0 Control Register (SF0CTRL)

Address: 0x4100_0800
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	SF0MOZ	SF0SOZ	SF0SSZ	SF0FICL	–*	SF0CPOL	SF0CPHA	SF0LSB	SF0MDFE	SF0SIZ	SF0MST	SF0SPE
Access	–	–	–	–	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0CTRL is a special function register (SFR) used to control the operation of the SSIOF.

[Description of Bits]

- **SF0SPE** (bit 0)
  SF0SPE sets whether or not to enable the transfer of the SSIOF.

SF0SPE	Description
0	Disable SSIOF transfer (initial value)
1	Enable SSIOF transfer

- **SF0MST** (bit 1)
  SF0MST sets the master/slave selection.

SF0MST	Description
0	Slave (initial value)
1	Master

- **SF0SIZ** (bit 2)
  SF0SIZ sets the transfer size.

SF0SIZ	Description
0	8 bit (initial value)
1	16 bit

- **SF0MDFE** (bit 3)
  SF0MDFE sets the mode fault control signal.
  The mode fault can be executed when SF0MST = 1, SF0MDFE = 1, and not transferring.

SF0MDFE	Description
0	The mode fault is not executed. (Initial value)
1	The mode fault is executed when not transferring.

- **SF0LSB** (bit 4)
  SF0LSB sets the data transfer order.

SF0LSB	Description
0	LSB first (initial value)
1	MSB first

- **SF0CPHA** (bit 5)
  SF0CPHA sets the serial clock phase.

SF0CPHA	Description
0	The data is sampled at the first edge and shifted at the second edge (initial value)
1	The data is shifted at the first edge and sampled at the second edge

- **SF0CPOL** (bit 6)
  SF0CPOL sets the serial clock polarity.

SF0CPOL	Description
0	Serial clock default is "0" ("0" during transmission/reception)(initial value)
1	Serial clock default is "1" ("1" during transmission/reception)

- **SF0FICL** (bit 8)
  SF0FICL sets the FIFO clearance. After clearance, set this to "0".

SF0FICL	Description
0	None (initial value)
1	Clear the receive/transmit byte (word) count

- **SF0SSZ** (bit 9)
  SF0SSZ sets the SSF0 output control.

SF0SSZ	Description
0	0/1 output (initial value)
1	Hi-Z

- **SF0SOZ** (bit 10)
  SF0SOZ sets the SOUTF0 output control when SSF0 = 1.

SF0SOZ	Description
0	0/1 output (initial value)
1	Hi-Z

- **SF0MOZ** (bit 11)
  SF0MOZ sets the SOUTF0, SCKF0 output control.

SF0MOZ	Description
0	0/1 output (initial value)
1	Hi-Z

16.2.3. SIOF0 Interrupt Control Register (SF0INTC)

Address: 0x4100_0804
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	SF0RFIC[3:0]				SF0TFIC[3:0]				–*	–*	–*	SF0MFIE	SF0ORIE	SF0FIE	SF0RFIE	SF0TFIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0INTC is a special function register (SFR) used to control the interrupt operation of the SSIOF.

[Description of Bits]

- **SF0TFIE** (bit 0)
  SF0TFIE sets whether or not to enable the transmission interrupt of the SSIOF.

SF0TFIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0RFIE** (bit 1)
  SF0RFIE sets whether or not to enable the reception interrupt of the SSIOF.

SF0RFIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0FIE** (bit 2)
  SF0FIE sets whether or not to enable the transfer end interrupt.

SF0FIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0ORIE** (bit 3)
  SF0ORIE sets whether or not to enable the overrun error interrupt.

SF0ORIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0MFIE** (bit 4)
  SF0MFIE sets whether or not to enable the SSIOF mode fault interrupt.

SF0MFIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0TFIC3-0** (bit 11 to 8)
  SF0TFIC3-0 set the remaining data count interrupt control for the transmit FIFO.
  These bits are used to generate DMA request.

SF0TFIC[3]	SF0TFIC[2]	SF0TFIC[1]	SF0TFIC[0]	Description
0	0	0	0	An interrupt occurs when the number of remaining byte to transmit becomes 0 bytes (0 half words) (initial value)
0	0	0	1	An interrupt occurs when the number of remaining byte to transmit becomes 1 byte (1 half word)
0	0	1	0	An interrupt occurs when the number of remaining byte to transmit becomes 2 bytes (2 half words)
0	0	1	1	An interrupt occurs when the number of remaining bytes to transmit becomes 3 bytes (3 half words)
0	1	0	0	An interrupt occurs when the number of remaining byte to transmit becomes 4 byte (4 half word)
0	1	0	1	An interrupt occurs when the number of remaining byte to transmit becomes 5 bytes (5 half words)
0	1	1	0	An interrupt occurs when the number of remaining bytes to transmit becomes 6 bytes (6 half words)
0	1	1	1	An interrupt occurs when the number of remaining byte to transmit becomes 7 byte (7 half word)
1	0	0	0	An interrupt occurs when the number of remaining byte to transmit becomes 8 bytes (8 half words)
1	0	0	1	An interrupt occurs when the number of remaining bytes to transmit becomes 9 bytes (9 half words)
1	0	1	0	An interrupt occurs when the number of remaining byte to transmit becomes 10 byte (10 half word)
1	0	1	1	An interrupt occurs when the number of remaining byte to transmit becomes 11 bytes (11 half words)
1	1	0	0	An interrupt occurs when the number of remaining bytes to transmit becomes 12 bytes (12 half words)
1	1	0	1	An interrupt occurs when the number of remaining byte to transmit becomes 13 byte (13 half word)
1	1	1	0	An interrupt occurs when the number of remaining byte to transmit becomes 14 bytes (14 half words)
1	1	1	1	An interrupt occurs when the number of remaining bytes to transmit becomes 15 bytes (15 half words)

- **SF0RFIC[3:0]** (bit 15 to 12)
  SF0RFIC[3:0] set the receive FIFO interrupt control.

SF0RFIC[3]	SF0RFIC[2]	SF0RFIC[1]	SF0RFIC[0]	Description
0	0	0	0	An interrupt occurs when 1 byte (1 half word) has been received(initial value)
0	0	0	1	An interrupt occurs when 2 bytes (2 half words) have been received
0	0	1	0	An interrupt occurs when 3 bytes (3 half words) have been received
0	0	1	1	An interrupt occurs when 4 bytes (4 half words) have been received
0	1	0	0	An interrupt occurs when 5 bytes (5 half words) have been received
0	1	0	1	An interrupt occurs when 6 bytes (6 half words) have been received
0	1	1	0	An interrupt occurs when 7 bytes (7 half words) have been received
0	1	1	1	An interrupt occurs when 8 bytes (8 half words) have been received
1	0	0	0	An interrupt occurs when 9 bytes (9 half words) have been received
1	0	0	1	An interrupt occurs when 10 bytes (10 half words) have been received
1	0	1	0	An interrupt occurs when 11 bytes (11 half words) have been received
1	0	1	1	An interrupt occurs when 12 bytes (12 half words) have been received
1	1	0	0	An interrupt occurs when 13 bytes (13 half words) have been received
1	1	0	1	An interrupt occurs when 14 bytes (14 half words) have been received
1	1	1	0	An interrupt occurs when 15 bytes (15 half words) have been received
1	1	1	1	An interrupt occurs when 16 bytes (16 half words) have been received

16.2.4. SIOF0 Transfer Interval Control Register (SF0TRAC)

Address: 0x4100_0808
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	SF0DTL[8:0]								
Access	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0TRAC is a special function register (SFR) used to set the minimum data transfer interval in Master mode.
For details, see 16.3.7, "Transfer Interval Setting".

16.2.5. SIOF0 Baud Rate Register (SF0BRR)

Address: 0x4100_080C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_5002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	SF0LAG[1:0]		SF0LEAD [1:0]		–*	–*	SF0BR[9:0]									
Access	R/W	R/W	R/W	R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0BRR is a special function register (SFR) used to set the operation mode.
Do not change the setting of this register during transfer. Operation is not guaranteed if it is changed during transfer.

[Description of Bits]

- **SF0BR[9:0]** (bit 9 to 0)
  Sets the baud rate (f_{SCK})(setting enabled in Master mode).
  $f_{SCK}=f_{HSCLK}/(2\times SF0BR[9:0])$
  f_{HSCLK}: HSCLK frequency(depending on the SYSC[2:0] bit of FCON01 register)

SF0BR[9:0]										Description
9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	2 dividing
0	0	0	0	0	0	0	0	0	1	2 dividing
0	0	0	0	0	0	0	0	1	0	4 dividing (initial value)
0	0	0	0	0	0	0	0	1	1	6 dividing
:										:
1	1	1	1	1	1	1	1	1	1	2046 dividing

[Note]
The maximum SSIOF transfer frequency is 4MHz. This setting should not exceed 4MHz.
If using P22 as SCKF0 in master mode, the max frequency is 2MHz.

- **SF0LEAD[1:0]** (bit 13 to 12)
  SF0LEAD[1:0] set the SSF0 –SCKF0 delay interval (setting enabled only in Master mode).

SF0LEAD[1]	SF0LEAD[0]	Description
0	0	0.5 X SCK
0	1	0.5 X SCK (initial value)
1	0	1.0 X SCK
1	1	1.5 X SCK

- **SF0LAG[1:0]** (bit 15 to 14)
  SF0LAG[1:0] set the SCKF0-SSF0(H) delay interval (setting enabled only in Master mode).

SF0LAG[1]	SF0LAG[0]	Description
0	0	0.5 X SCK
0	1	0.5 X SCK (initial value)
1	0	1.0 X SCK
1	1	1.5 X SCK

16.2.6. SIOF0 Status Register (SF0SRR)

Address: 0x4100_0810
Access: R
Access size: 32 bit
Initial value: 0x0000_1400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	SF0RFE	SF0RFF	SF0TFE	SF0TFF	SF0WOF	–*	–*	SF0SPIF	SF0MDF	SF0ORF	SF0FI	SF0RFI	SF0TFI
Access	–	–	–	R	R	R	R	R	–	–	R	R	R	R	R	R
Initial value	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0SRR is a special function register (SFR) used to indicate the data transfer state and error state of the SSIOF.

[Description of Bits]

- **SF0TFI** (bit 0)
  SF0TFI indicates a transmission interrupt.
  A transmission interrupt occurs if the remaining data in the transmit FIFO matches the byte count selected with SF0TFIC.

SF0TFI	Description
0	No interrupt request (initial value)
1	Interrupt request

- **SF0RFI** (bit 1)
  SF0RFI indicates a reception interrupt.
  If the number of data received in the receive FIFO is equal or more byte count selected with SF0RFIC , reception interrupt occur.

SF0RFI	Description
0	No interrupt request (initial value)
1	Interrupt request

- **SF0FI** (bit 2)
  SF0FI indicates a transfer end interrupt. (the transmit FIFO is empty and the transfer of the last one byte (one word) is finished)

SF0FI	Description
0	No interrupt request (initial value)
1	Interrupt request

- **SF0ORF** (bit 3)
  SF0ORF indicates the overrun error flag.

SF0ORF	Description
0	Normal (initial value)
1	An overrun error occurred (an interrupt is generated)

- **SF0MDF** (bit 4)
  SF0MDF indicates a mode fault.

SF0MDF	Description
0	Normal (initial value)
1	A mode fault occurs (an interrupt occurs)

- **SF0SPIF** (bit 5)
  SF0SPIF indicates the SSIOF one byte (word) transfer end.

SF0SPIF	Description
0	No end of transfer (initial value)
1	End of transfer

- **SF0WOF** (bit 8)
  SF0WOF indicates a write overflow.

SF0WOF	Description
0	Normal (initial value)
1	A write overflow occurred (No interrupt is generated)

- **SF0TFF** (bit 9)
  SF0TFF indicates the transmit FIFO Full.

SF0TFF	Description
0	Not Full (initial value)
1	Full (No interrupt is generated)

- **SF0TFE** (bit 10)
  SF0TFE indicates the transmit FIFO Empty.

SF0TFE	Description
0	Not Empty
1	Empty (No interrupt is generated) (initial value)

- **SF0RFF** (bit 11)
  SF0RFF indicates the receive FIFO Full.

SF0RFF	Description
0	Not Full (initial value)
1	Full (No interrupt is generated)

- **SF0RFE** (bit 12)
  SF0RFE indicates the receive FIFO Empty.

SF0RFE	Description
0	Not Empty
1	Empty (No interrupt is generated) (initial value)

16.2.7. SIOF0 Status Clear Register (SF0SRC)

Address: 0x4100_0814
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	SF0WOFC	–*	–*	SF0SPIFC	SF0MDFC	SF0ORFC	SF0FC	SF0RFC	SF0TFC
Access	–	–	–	–	–	–	–	W	–	–	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0SRC is a special function register (SFR) used to clear the data transfer state and error state of the SSIOF.

[Description of Bits]

- **SF0TFC** (bit 0)
  SF0TFC is the bit to clear the interrupt request of the transmission interrupt. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0TFI bit of the SF0SRR register.

- **SF0RFC** (bit 1)
  SF0RFC is the bit to clear the interrupt request of the receiving interrupt. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0RFI bit of the SF0SRR register.

- **SF0FC** (bit 2)
  SF0FC is the bit to clear the interrupt request of the transfer end interrupt. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0FI bit of the SF0SRR register.

- **SF0ORFC** (bit 3)
  SF0ORFC is the bit to clear the interrupt request of the overrun error flag. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0ORF bit of the SF0SRR register.

- **SF0MDFC** (bit 4)
  SF0MDFC is the bit clear the interrupt request of the mode fault. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0MDF bit of the SF0SRR register.

- **SF0SPIFC** (bit 5)
  SF0SPIFC is the bit to clear the SSIOF1 byte (word) transfer end. The transfer end flag (SF0SPIF) is cleared by writing "1".

- **SF0WOFC** (bit 8)
  SF0WOFC is the bit to clear a write overflow. The write overflow flag (SF0WOF) is cleared by writing "1".

16.2.8. SIOF0 FIFO Status Register (SF0FSR)

Address: 0x4100_0818
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	SF0RFD[4:0]					–*	–*	–*	SF0TFD[4:0]				
Access	–	–	–	R	R	R	R	R	–	–	–	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0FSR is a special function register (SFR) used to indicate the count transmitted and received by FIFO.

[Description of Bits]

- **SF0TFD[4:0]** (bit 4 to 0)
  SF0TFD[4:0] indicate the untransmitted byte (half word) count of the transmit FIFO.

SF0TFD[4]	SF0TFD[3]	SF0TFD[2]	SF0TFD[1]	SF0TFD[0]	Description
0	0	0	0	0	Empty (initial value)
0	0	0	0	1	1 Byte / 1Half Word
0	0	0	1	0	2 Byte / 2 Half Word
0	0	0	1	1	3 Byte / 3 Half Word
0	0	1	0	0	4 Byte / 4 Half Word
0	0	1	0	1	5 Byte / 5 Half Word
0	0	1	1	0	6 Byte / 6 Half Word
0	0	1	1	1	7 Byte / 7 Half Word
0	1	0	0	0	8 Byte / 8 Half Word
0	1	0	0	1	9 Byte / 9 Half Word
0	1	0	1	0	10 Byte / 10 Half Word
0	1	0	1	1	11 Byte / 11 Half Word
0	1	1	0	0	12 Byte / 12 Half Word
0	1	1	0	1	13 Byte / 13 Half Word
0	1	1	1	0	14 Byte / 14 Half Word
0	1	1	1	1	15 Byte / 15 Half Word
1	0	0	0	0	16 Byte / 16 Half Word(Full)

- **SF0RFD[4:0]** (bit 12 to 8)
  SF0RFD[4:0] indicate the byte (half word) count received in the receive FIFO.

SF0RFD[4]	SF0RFD[3]	SF0RFD[2]	SF0RFD[1]	SF0RFD[0]	Description
0	0	0	0	0	Empty (initial value)
0	0	0	0	1	1 Byte / 1 Half Word
0	0	0	1	0	2 Byte / 2 Half Word
0	0	0	1	1	3 Byte / 3 Half Word
0	0	1	0	0	4 Byte / 4 Half Word
0	0	1	0	1	5 Byte / 5 Half Word
0	0	1	1	0	6 Byte / 6 Half Word
0	0	1	1	1	7 Byte / 7 Half Word
0	1	0	0	0	8 Byte / 8 Half Word
0	1	0	0	1	9 Byte / 9 Half Word
0	1	0	1	0	10 Byte / 10 Half Word
0	1	0	1	1	11 Byte / 11 Half Word
0	1	1	0	0	12 Byte / 12 Half Word
0	1	1	0	1	13 Byte / 13 Half Word
0	1	1	1	0	14 Byte / 14 Half Word
0	1	1	1	1	15 Byte / 15 Half Word
1	0	0	0	0	16 Byte / 16 Half Word(Full)

16.2.9. SIOF0 Write Data Register (SF0DWR)

Address: 0x4100_081C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	SF0WD[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0DWR is an 8 bit (byte) or 16 bit (half word) special function register (SFR) used to hold transmitted data.
Write access to this register should be:
8 bit write access to the SF0WD[7:0] for 8 bit transmission (SF0SIZ bit in the SF0CTRL register =0)
16 bit write access to the SF0WD[15:0] for 16 bit transmission (SF0SIZ bit in the SF0CTRL register =1)

16.2.10. SIOF0 Read Data Register (SF0DRR)

Address: 0x4100_0820
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	SF0RD[15:0]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SF0DRR is an 8 bit (byte) or 16 bit (half word) special function register (SFR) used to hold received data.
Read access to this register should be:
8 bit read access to SF0RD[7:0] register for 8 bit reception (SF0SIZ bit in the SF0CTRL register =0)
16 bit read access to SF0RD[15:0] register for 16 bit reception (SF0SIZ bit in the SF0CTRL register =1)

16.3. Description of Operation

16.3.1. Master Mode and Slave Mode

Master mode and Slave mode are provided as the transmit/receive mode. This is selected by the SF0MST bit of the SIOF0 control register.
SF0BR (baud rate) bit, SF0LEAD (SSF0-SCKF0 delay interval) bit, and SF0LAG (SCKF0-SSF0 delay interval) bit of the SIOF0 baud rate register and SF0DTL (minimum data transfer interval) bit of the SIOF0 transfer interval control register determine SCKF0 and SSF0 operations. And these bit are also only valid during the master operation.
Each bit of SF0CPOL, SF0CPHA, SF0LSB, and SF0SIZ in the SF0CTRL register needs to have the same value for master and slave.

16.3.2. Control of Polarity and Phase of Serial Clock

SF0CPOL bit of the SF0CTRL (SIOF0 control) register controls the clock polarity. SF0CPHA bit of the SF0CTRL (SIOF0 control) register controls the clock phase and determines the shift timing of transmit data and the sampling timing of received data. The master and slave which communicate with each other must have the same setting values for SF0CPOL and SF0CPHA.

16.3.3. Data Transfer Timing When SF0CPHA Is "0"

Figure 16-2 shows the data transfer timing when SF0CPHA is "0". For the SCKF0, two cases are shown (SF0CPOL is "0" and "1"). SSF0 is the slave selection input in Slave mode.
In Master mode, the transfer is started when data is written to the SF0DWR register. In Slave mode, the transfer is started at the SSF0 falling edge. The received data is sampled at the rising-edge of SCKF0 in SF0CPOL is “0” and the falling-edge of SCKF0 in SF0CPOL is “1”. The transmitted data is shifted at the falling-edge of SCKF0 in SF0CPOL is “0” and the rising-edge of SCKF0 in SF0CPOL is “1”.

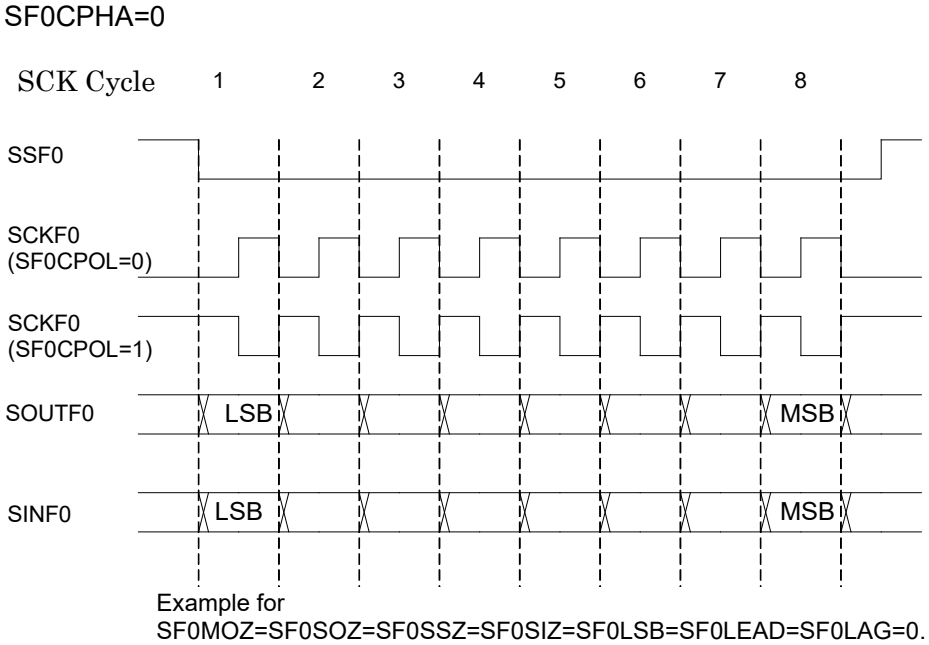


Figure 16-2 Clock Waveform When SF0CPHA = 0

16.3.4. Data Transfer Timing When SF0CPHA Is "1"

Figure 16-3 shows the data transfer timing when SF0CPHA is "1". For the SCKF0, two cases are shown (SF0CPOL is "0" and "1").
SSF0 is the slave selection input in Slave mode.
In Master mode, the transfer is started when data is written to SF0DWR. In Slave mode, the transfer is started at the first edge of SCKF0. The received data is sampled at the falling-edge of SCKF0 in SF0CPOL is “0” and the rising-edge of SCKF0 in SF0CPOL is “1”. The transmitted data is shifted at the rising-edge of SCKF0 in SF0CPOL is “0” and the falling-edge of SCKF0 in SF0CPOL is “1”.

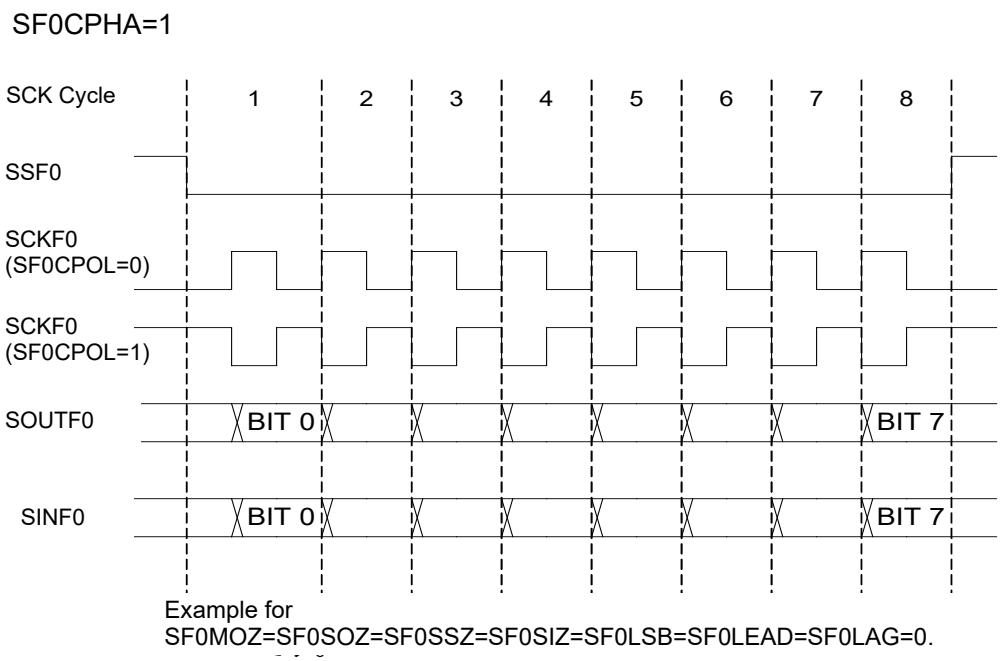


Figure 16-3 Clock Waveform When CPHA = 1

16.3.5. Serial Clock Baud Rate

The baud rate is selected by the SF0BR[9:0] bit of SF0BRR register. This is only valid in Master mode. The baud-rate clock SCKF0 is generated by dividing HSCLK.
The baud rate (f_{SCK}) is calculated as follows.

$f_{SCK}=f_{HSCLK}/(2\times SF0BR[9:0])$

f_{SCK} : Frequency of baud-rate clock
f_{HSCLK} : Frequency of HSCLK
SF0BR : Value set in SF0BR[9:0] of the SF0BRR register (1 to 1023)
If 0 is set the SF0BR register, it is processed as 1.

For SF0BR, it can be selected from 1023 dividing types (2 to 2046).

16.3.6. Transfer Size

The transfer size can be selected in 8 bit (byte) or 16 bit (half word).
Transfer data read/write must be adjusted to the transfer size. As the number of FIFO stages is the same for both byte and half word, the number of transfers is the same.
The master and slaves which communicate with each other must have the same value for SF0SIZ.

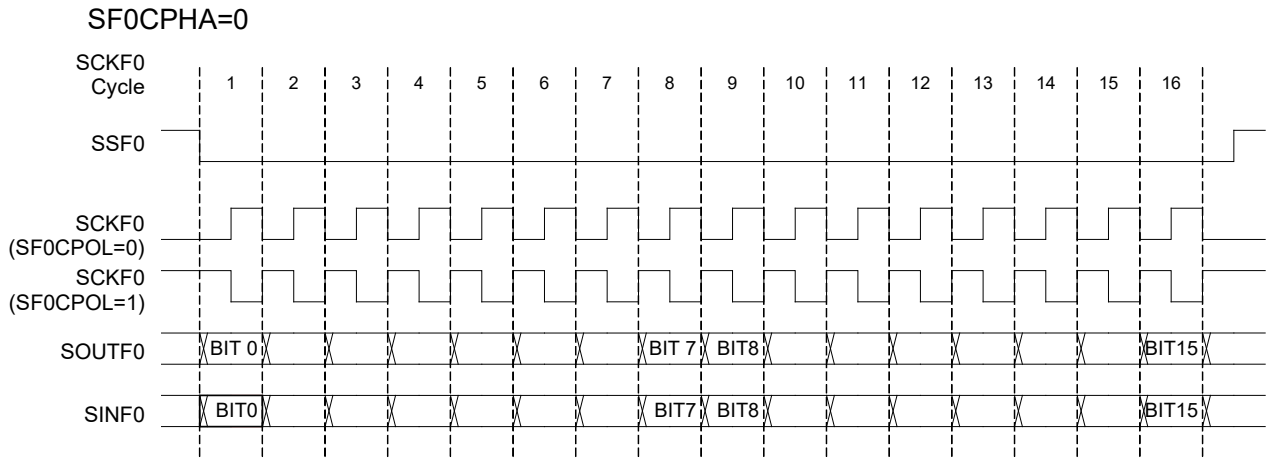


Figure 16-4 SSIOF Bus Waveform When SF0CPHA= 0 (16 Bit)

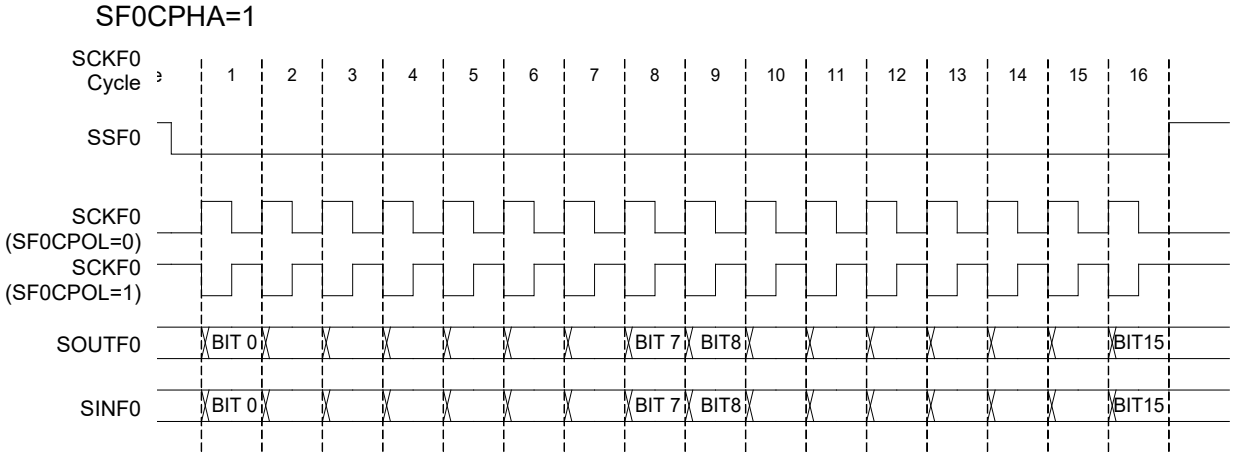


Figure 16-5 SSIOF Bus Waveform When SF0CPHA = 1 (16 Bit)

16.3.7. Transfer Interval Setting

LEAD (SSF0-SCKF0 time), LAG (SCKF0-SSF0(H) time), and TDTL (SSF0(H)-SSF0(H)) can be set to adjust the speed to the slave. This setting is only valid in Master mode. It is ignored in Slave mode.
Setting during transferring is invalid.

(1) LEAD
A value from 0.5 to 1.5SCKF can be set.
(2) LAG
A value from 0.5 to 1.5SCKF can be set.
(3) TDTL
The minimum transfer interval can be controlled in SCKF0 clocks by setting SF0DTL bit of the SF0TRAC register.
If there is any transfer data in FIFO, the time set by this setting (SSF0) changes to "1" during byte/word transfer.
If there is no transfer data in FIFO, this is "1" until any transmitted data is written.
If SF0DTL bit of the SF0TRAC register is set to 0, the interval after transfer (TDTL) disappears and a continuous transfer is performed. SSF0 is held to 0 and returns to 1 after the transfer is finished.

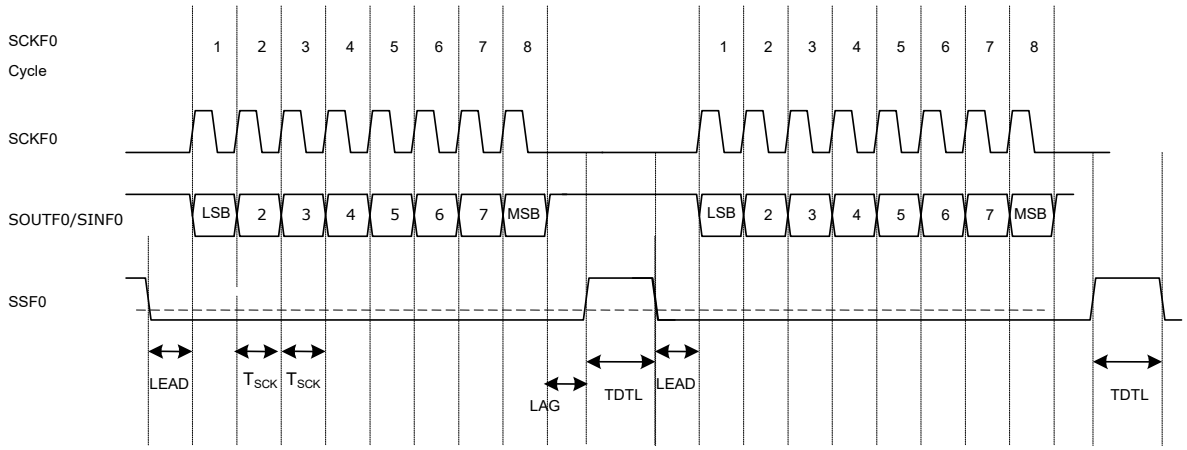


Figure 16-6 Transfer Interval (When SF0DTL Is Not "0")

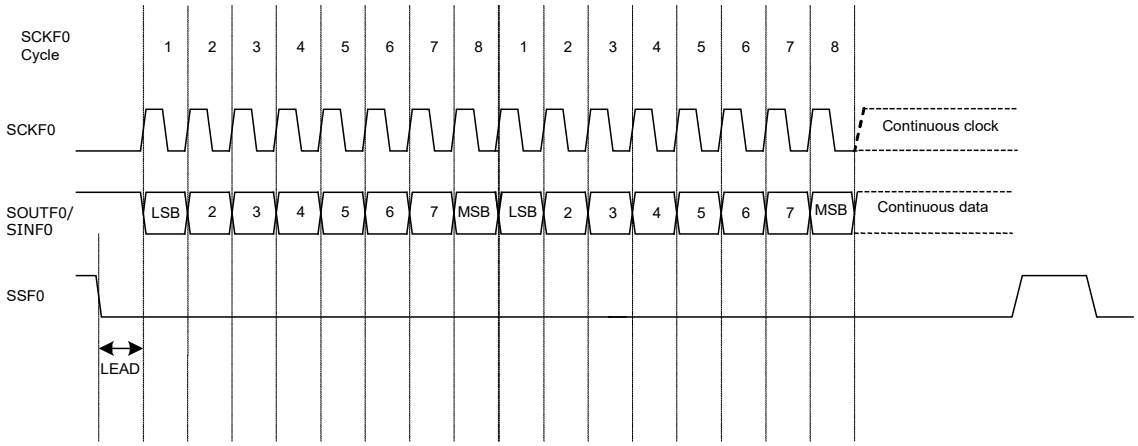


Figure 16-7 Transfer Interval (When SF0DTL Is "0")

16.3.8. Transmit Operation (Master Mode)

① Write the necessary values to SF0CTRL, SF0INTC, SF0BRR, and SF0TRAC, set the SF0MST bit to Master mode, and set the SF0SPE bit to enable the SSIOF transfer.
② When the transmitted data is written to SF0DWR, the transmit FIFO Empty flag changes to 0 (SF0TFE = 0). SSIOF starts the automatic transmission and outputs the transmitted data from LSB or MSB on the SOUTF0 pin according to the SF0LSB setting.
③ The sync clock, which was set by the SF0CPOL, SF0CPHA, and SF0BRR registers, is output from the SCKF0 pin.
④ Transmitted data can be written to SF0DWR successively. However, if further writing is performed when the transmit FIFO is in Full status (SF0TFF = 1), a write overflow occurs. (SF0WOF = 1, No interrupt is generated.)
⑤ The SF0SPIF bit is set each time the transfer of 1 byte is completed. (SF0SPIF=1)
⑥ A transmission interrupt occurs if the remaining data in the transmit FIFO matches the byte count selected with SF0TFIC. (SF0TFI=1)
⑦ If the transmit FIFO becomes empty and the transfer of the last byte is completed, a transfer completion interrupt is generated. (SF0FI=1)

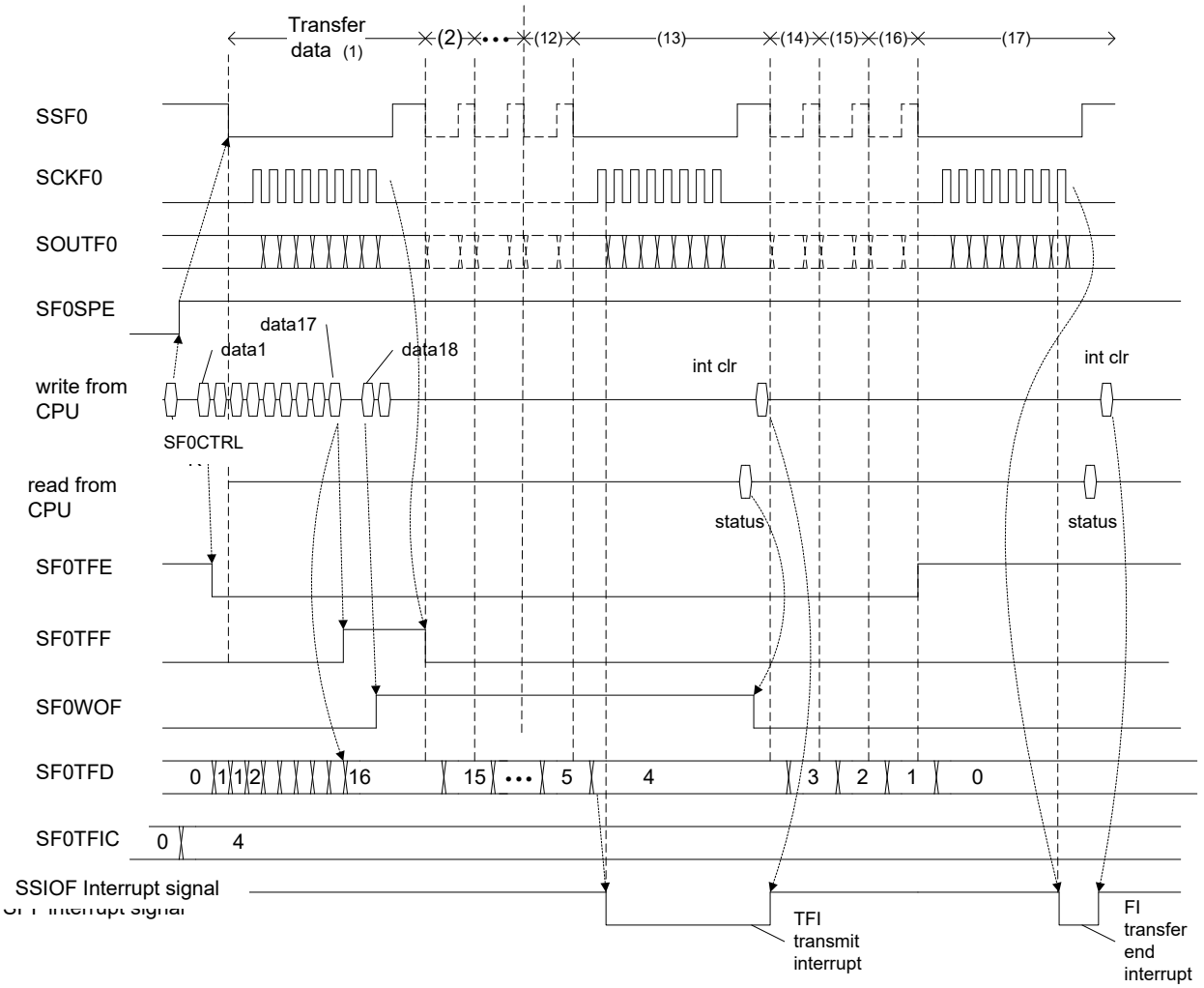


Figure 16-8 Master Mode (Transmit Operation)

16.3.9. Receive Operation (Master Mode)

The master mode of the synchronous serial with FIFO starts by setting data in a transmission buffer.
Data needs to be set into a transmission buffer even master mode reception only.

① Write the necessary values to SF0CTRL, SF0INTC, SF0BRR, and SF0TRAC, set the SF0MST bit to Master mode, and set the SF0SPE bit to enable the SSIOF transfer.
② When the data is written to SF0DWR, the SSIOF transfer is started.
③ The sync clock, which was set by the SF0CPOL, SF0CPHA, and SF0BRR0-1 registers, is output from the SCKF0 pin.
④ On the SINF0 pin, the received data is sampled from LSB or MSB according to the SF0LSB setting and stored in the receive FIFO. The receive FIFO Empty flag changes to 0 (RFE = 0).
⑤ The SF0SPIF bit is set each time the transfer of 1 byte is completed. (SF0SPIF=1)
⑥ If the number of data received in the receive FIFO is equal to or more than matches following the byte count selected with SF0RFIC of SF0CR, SF0RFI of SF0SRR is set to generate a reception interrupt.
⑦ When the receive FIFO becomes Full, the subsequent reception is disabled. If the reception is performed in this state, an overrun error interrupt is generated. (SF0ORF=1)
⑧ If the temporary data of transmit FIFO becomes empty and the transfer of the last byte is completed, a transfer completion interrupt is generated. (SF0FI=1)

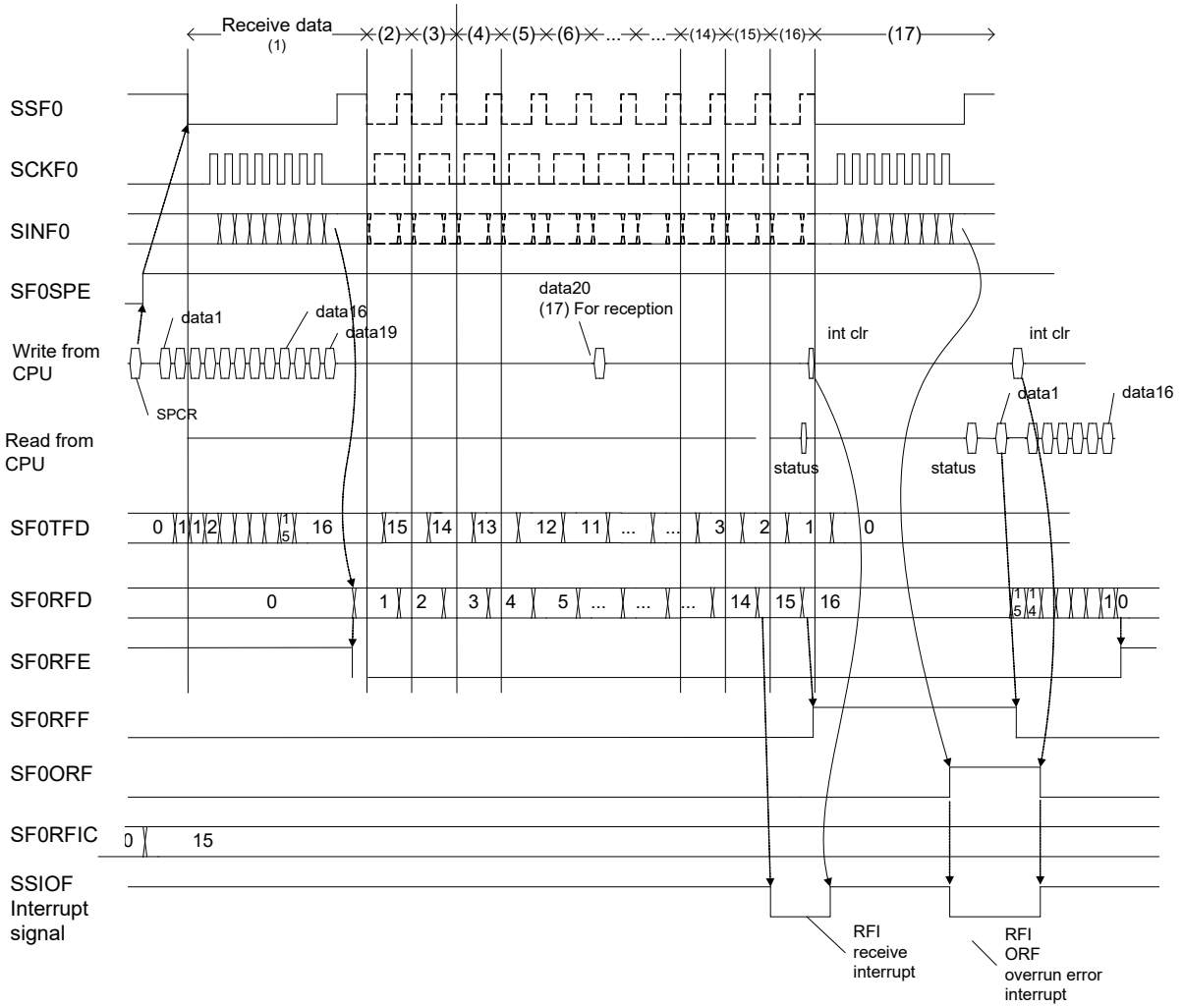


Figure 16-9 Master Mode (Receive Operation)

16.3.10. FIFO Operation

SSIOF includes the receive FIFO of 16 half words and the transmit FIFO of 16 half words. The FIFO state is indicated in the SF0TFF, SF0TFE, SF0RFF, and SF0RFE bits of SF0SRR, and the SF0TFD and SF0RFD bit of SF0FSR.
There are three FIFO states, Full (SF0TFF and SF0RFF), Empty (SF0TFE and SF0RFE), and Depth (SF0TFD and SF0RFD).

16.3.11. Write Overflow

If further writing is performed when the transmit FIFO is in Full status (SF0TFF = 1), a write overflow is set. (SF0WOF=1)
However, interrupt is not generated even when a write overflow occurs.
SF0WOF is cleared when write “1” in SF0WOFC bit of SF0SRC.

16.3.12. Overrun Error

If further reception is performed when the receive FIFO is in Full status (SF0RFF = 1), an overrun error occurs. (SF0ORF=1)
If an overrun error occurs, the SF0ORF bit of SF0SRR is set, and an overrun error interrupt is generated. The newly received data is not held.
Read the content of the receive FIFO, clear the SF0RFF bit, then write "1" in the SF0ORFC bit to clear the SF0ORFC bit.

16.3.13. FIFO Clear

The transmit/receive counter control of FIFO can be initialized to the initial setting state (SF0TFF=0, SF0TFE=1, SF0RFF=0, and SF0RFE=1 in the SF0SRR register and SF0TFD=000 and SF0RFD=000 in the SF0FSR register) by setting the SF0FICL bit of the SF0CTRL register to 1.
The SF0FICL bit of the SF0CTRL register needs to be 0, before next transfer operation.
Even if SF0FICL bit of SF0CTRL register is set to 1, the interrupt is not changed for SF0RFIC, SF0TFIC, SF0ORIE, SF0FIE, SF0RFIE, and SF0TFIE of the SF0INTC register, and SF0ORF, SF0FI, SF0RFI, and SF0TFI of the SF0SRR register.

This bit can be used to discard the data of FIFO when the communication is aborted.

16.3.14. Transfer When Slave Has Different Number of FIFO Transfer Bytes/Half Words

(1) The master sends data only when the transmitted data is already written in FIFO.
(2) As the slave's transmit data count is determined by the master, data is transferred as follows if the number of FIFO transfer bytes/half words of slave is different from that of the master.
If the transmitted data is not written in the slave's FIFO, a 0xFF ((0xFFFF) for half word) is sent, including the state after a reset.

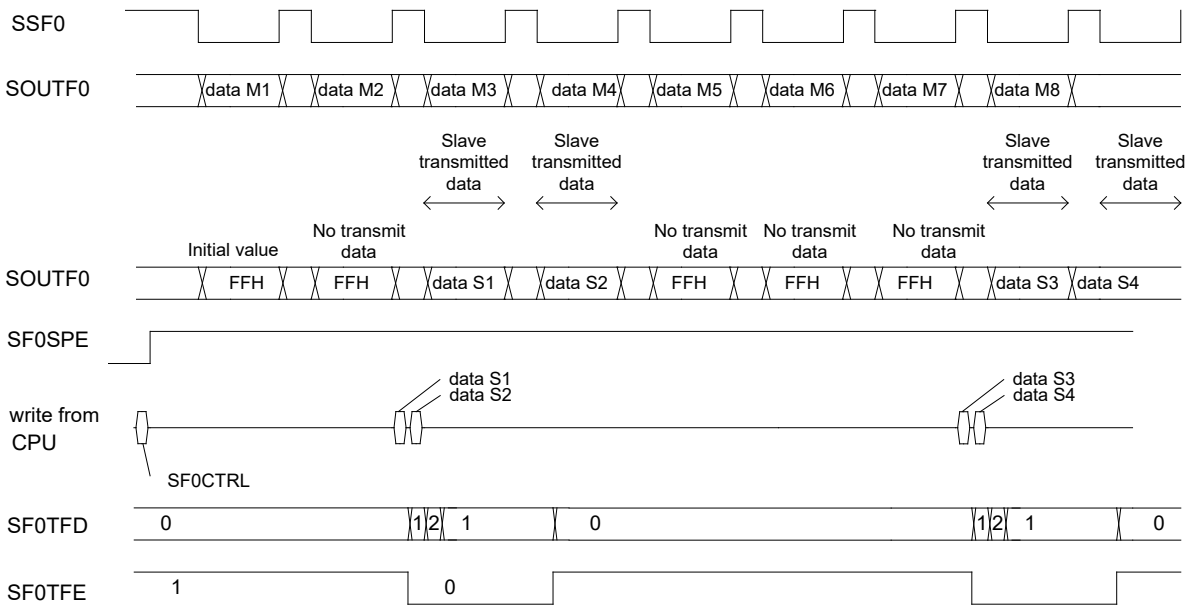


Figure 16-10 Transfer When Slave Has Different Number of FIFO Transfer Bytes/Half Words

16.3.15. Mode Fault (MDF)

A mode fault error occurs if the SSF0 signal becomes low level in Master mode. (SF0SRR's SF0MDF is set.) If this bit becomes 1, it indicates that there is risk of two or more masters competing for the bus.
When a mode fault error occurs, SSIOF performs the following operations since there is a risk of bus latch-up:

1. Automatically sets the SF0MST bit of SF0CTRL to 0 (slave).
2. Automatically sets the SF0SPE bit of SF0CTRL to 0 (disabled) to make the SSIOF unable to transfer.
3. Set SF0MDF of SF0SRR, and also generates an interrupt if the SF0MDFE bit of SF0CTRL is 1 (interrupt permitted).

The system should resolve the causes of the mode fault, and then clear SF0MDF according to the following steps:

1. Write 1 in SF0MDF to clear it.
2. Set SF0CTRL again.

Figure 16-11 shows the timing that allows a mode fault operation.

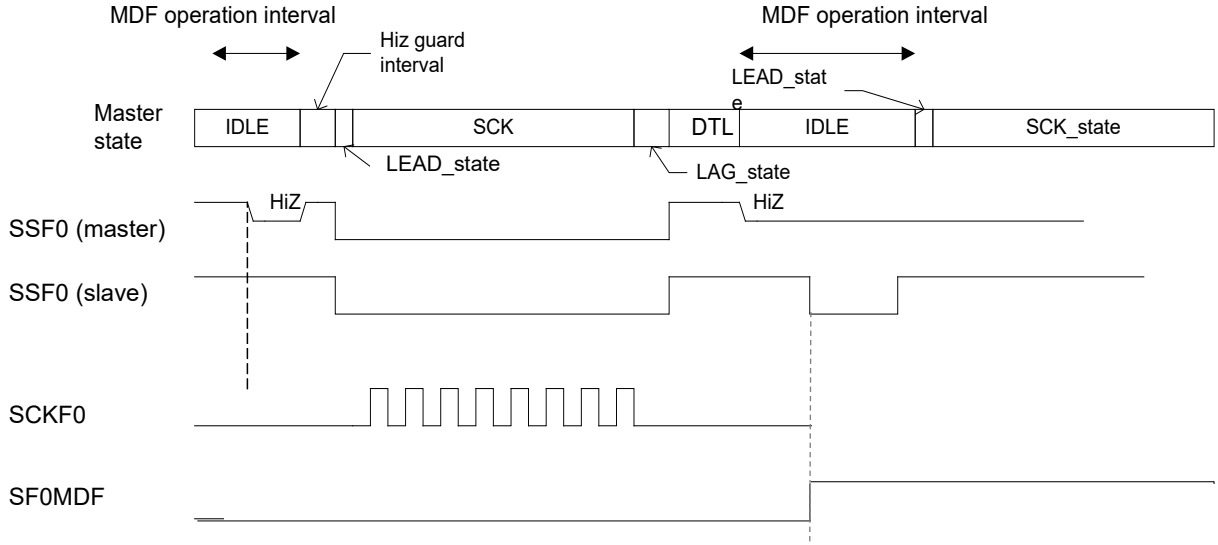


Figure 16-11 Timing That Allows Mode Fault Operation

16.3.16. Interrupt Source

16.3.16.1. SSIOF Interrupt Source

There are the following five types.

- Mode fault
  If a mode fault (multi-master bus contention) occurs, SF0MDF of SF0SRR is set and a mode fault interrupt is generated.
- Overrun
  If an overrun occurs, SF0ORF of SF0SRR is set, and an overrun error interrupt is generated.
- Transmit FIFO threshold
  If the remaining data of the transmit FIFO matches the byte count selected with SF0TFIC, SF0TFI of SF0SRR is set to generate a transmission interrupt.
- Receive FIFO threshold
  If the number of data received in the receive FIFO is equal to or more than following the byte count selected with SF0RFIC of SF0CR, SF0RFI of SF0SRR is set to generate a reception interrupt.
- End of transfer
  If the transmit FIFO becomes empty and the transfer of the last byte is finished, SF0FI of SF0SRR is set to generate a transfer end interrupt.

16.3.16.2. Clear SSIOF Interrupt

An interrupt request is cleared by writing 1 to each interrupt bit (SF0TFC, SF0RFC, SF0FC, SF0ORFC, SF0MDFC, SF0SPIFC, and SF0WOFC) of the SF0SRR.

16.3.16.3. SSIOF Interrupt Timing

Figure 16-12 shows the interrupt timing.
The remaining transmit byte count interrupt (TFI) generates an interrupt in 1 to 2 SYSCLK after the shift clock of the second bit.
For receive byte count interrupt (RFI), transfer completion interrupt (FI), and overrun (ORF), an interrupt is generated in 1 to 2 SYSCLK after the sampling clock at the MSB.
For MDF, an interrupt is generated at a mode fault occurrence.

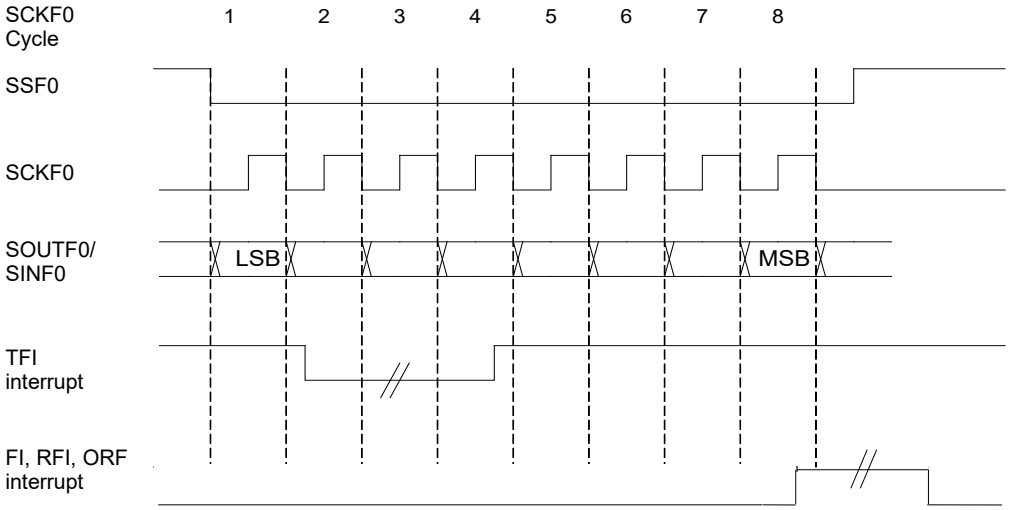


Figure 16-12 Interrupt Timing

16.3.16.4. Interrupt processing flow

Figure 16-13 show the processing flow in the receiving operation of the slave mode.

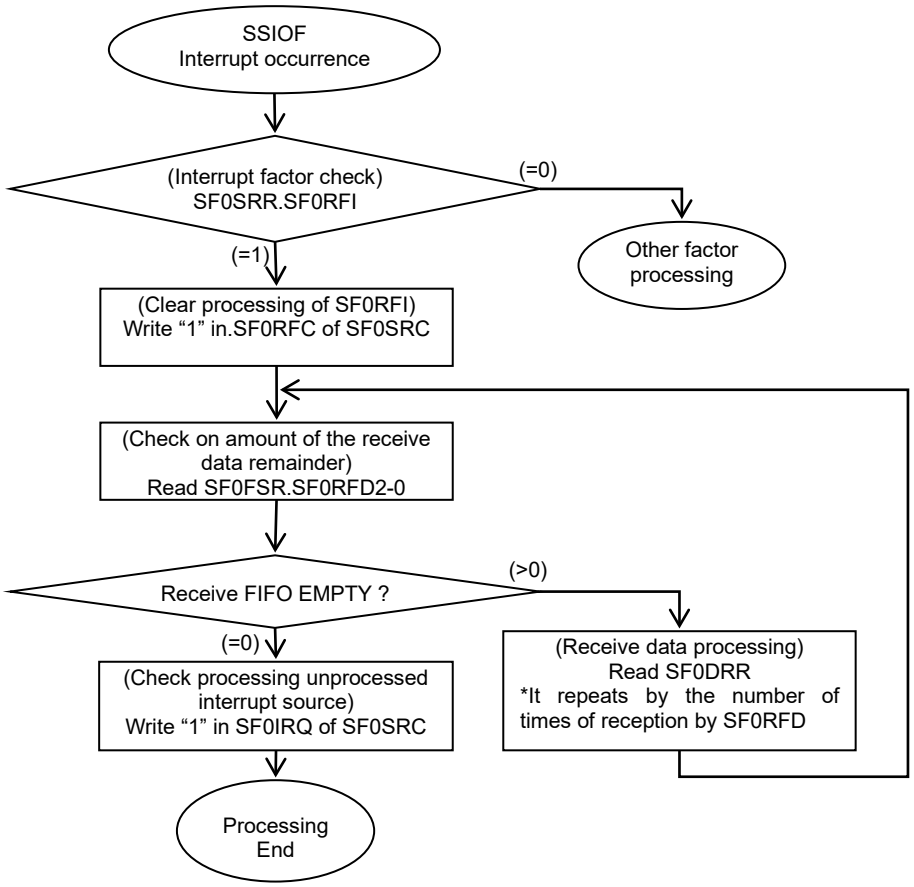


Figure 16-13 Example of the interrupt control flow

16.3.17. Hi-Z Operation

Figure 16-14 shows an example of using Hi-Z (SF0MOZ, SF0SOZ, and SF0SSZ).
The Hi-Z transmit interval of the master is limited to the IDLE time shown below.
To reduce the effect of noise in the Hi-Z state, "1"/"0" is fixed 1SCKF0 before the transmission starts (HiZ guard interval), and "1"/"0" is fixed during the DTL time of the transfer interval. If any of the SF0MOZ, SF0SOZ, and SF0SSZ bit is set to 1, the HiZ guard interval is inserted before the transmission starts.

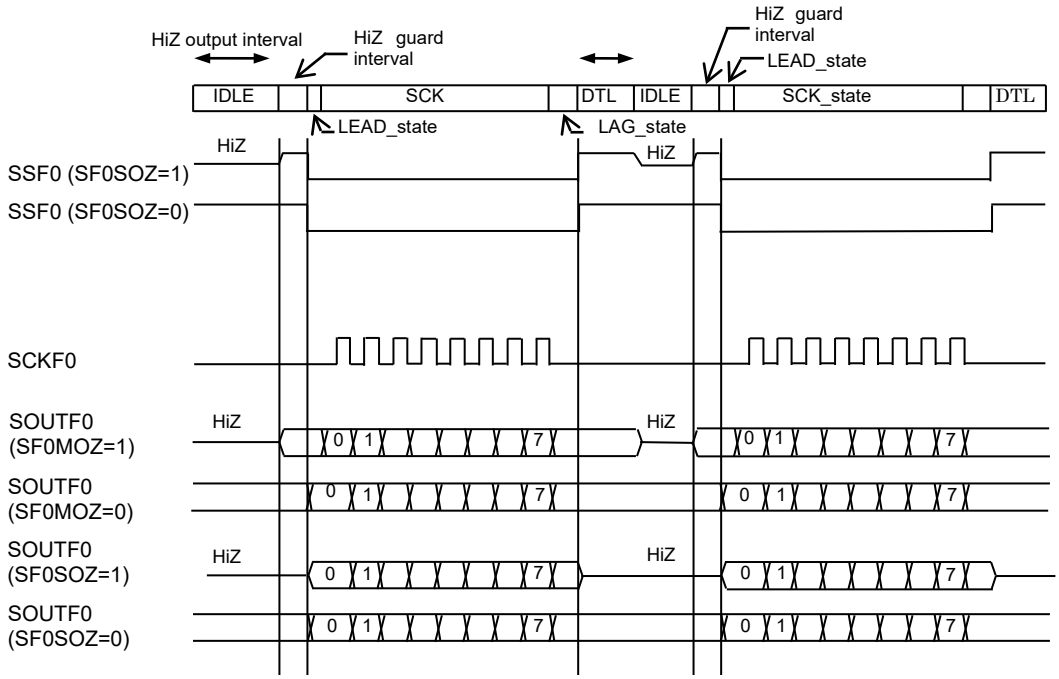


Figure 16-14 Hi-Z Operation

16.3.18. Interval from SF0MST Setting to Transfer Start

The SSIOF bus (SOUTF0, SCKF0, and SSF0) remains high impedance until Master mode is set.
After setting SF0MSTR, wait for at least 100ns before starting the transmission (SF0SPE = 1, or transfer started by data write).

16.3.19. Pin Settings

To enable the SSIOF function, the applicable bit of each related port register needs to be set. See Chapter 22, "Port" for details about the port registers.
For SOUTF0, SINF0, SCKF0 and SSF0, the ports can be selected from several possibilities.
Be sure to select one of the following combinations of ports for SOUTF0/SINF0/SCKF0/SSF0.

	SSIOF pin	Combination 1	Combination 2	Combination 3	Combination 4
SSIOF	SOUTF0,SINF0, SCKF0,SSF0	P20,P21, P22,P23	P34,P35, P36,P37	P44,P45, P46,P47	P54,P55, P56,P57

Note that only one port can be selected as port.
If using P22 as SCKF0 in master mode, the max clock output frequency is 2MHz.

Chapter 17

UART

17. UART

17.1. General Description

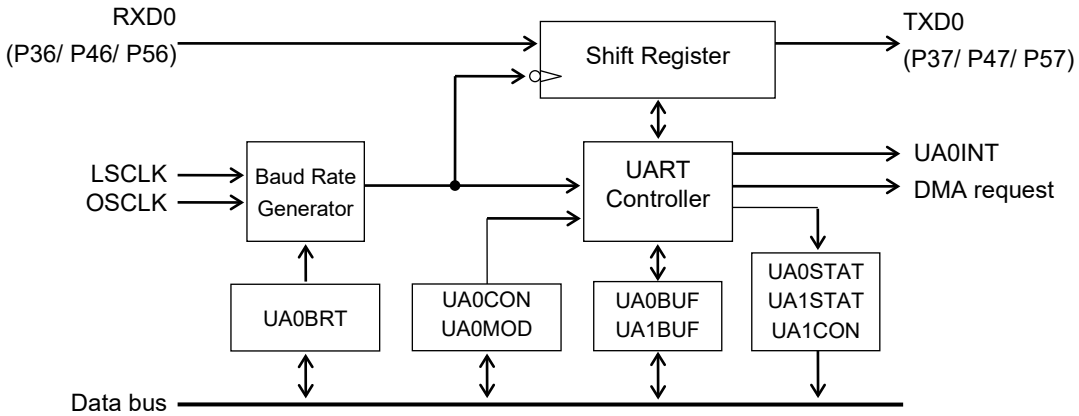
This LSI includes one channel of UART (Universal Asynchronous Receiver Transmitter), a full-duplex communication start-stop synchronous serial interface.
For input clocks, see Chapter 6, "Clock Generation Circuit".
To use the UART, it needs to set the secondary and quintic functions of the ports 3, port4 and port 5. For the port function setting, see Chapter 22 "Port".

17.1.1. Features

- 5 bit/6 bit/7 bit/8 bit data length selectable.
- Odd parity, even parity, or no parity selectable.
- 1 stop bit or 2 stop bit selectable.
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic.
- LSB first or MSB first selectable as a communication direction.
- Communication speed: Settable within the range of 2400bps to 115200bps.
- Built-in baud rate generator.
- Generates transmission/receive DMA request.

17.1.2. Configuration

Figure 17-1 shows the configuration of the UART.



UA0BUF : UART0 receive buffer
UA1BUF : UART0 transmit buffer
UA0BRT : UART0 baud rate register
UA0CON : UART0 control register
UA0MOD : UART0 mode register
UA0STAT : UART0 receive status register
UA1STAT : UART0 transmit status register
UA1CON : UART0 transmit monitor register

Figure 17-1 Configuration of UART

17.1.3. List of Pins

Pin Name	I/O	Function
RXD0	I	UART0 data input pin
TXD0	O	UART0 data output pin

17.2. Description of Registers

17.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4100_1000	UART0 receive buffer	UA0BUF	R	32	0x0000_0000
0x4100_1004	UART0 control register	UA0CON	R/W	32	0x0000_0000
0x4100_1008	UART0 mode register	UA0MOD	R/W	32	0x0000_0000
0x4100_100C	UART0 baud rate register	UA0BRT	R/W	32	0x0000_3FFF
0x4100_1010	UART0 receive status register	UA0STAT	R/W	32	0x0000_0000
0x4100_1020	UART0 transmit buffer	UA1BUF	R/W	32	0x0000_0000
0x4100_1024	UART0 transmit monitor register	UA1CON	R	32	0x0000_0000
0x4100_1030	UART0 transmit status register	UA1STAT	R/W	32	0x0000_0000
0x4100_1038	UART0 interrupt status register	UA0INTST	R/W	32	0x0000_0000

17.2.2. UART0 Receive Buffer (UA0BUF)

Address: 0x4100_1000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	U0B[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA0BUF is a special function register (SFR) used to store the received data.
Since data received at termination of reception is stored in UA0BUF, read the contents of UA0BUF by using the UART0 interrupt at termination of reception. At continuous reception, the UA0BUF register is updated whenever reception terminates.
When the 5 to 7 bit data length is selected, unnecessary bit become "0".

17.2.3. UART0 Transmit Buffer (UA1BUF)

Address: 0x4100_1020
Access: R/W
Access size:32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	U1B[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA1BUF is a special function register (SFR) used to store the transmitted data.
Write data to be transmitted in the UA1BUF. To transmit data consecutively, confirm that the U1FUL flag of the transmit status register (UA1STAT) becomes "0", then write the next transmitted data to UA1BUF. Any value written to UA1BUF can be read. When the 5 to 7 bit data length is selected, unnecessary bit become invalid in the transmit mode.

17.2.4. UART0 Control Register (UA0CON)

Address: 0x4100_1004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	U0EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA0CON is a special function register (SFR) used to start/stop communication of the UART.

[Description of Bits]

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. To terminate the communication, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Start communication

[Note]
After having setting necessary for UART communication, U0EN in "1" after waiting for 3 cycle with the clock which setting in U0CK[1:0] bit, and start communication.

17.2.5. UART0 Transmit Monitor Register (UA1CON)

Address: 0x4100_1024
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	U1EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA1CON is a special function register(SFR) which indicate UART transmission status.

[Description of Bits]

- **U1EN** (bit 0)
  The bit indicates transmission operating status .
  Before a transmission is start, set to “1” by software.
  When a transmission is stopped, the bit becomes “0”. Can confirm a transmission state.
  This bit is not a bit to start the transmission, the UART transmission is possible even if do not use this bit.

U1EN	Description
0	stop transmit (initial value)
1	transmitting

17.2.6. UART0 Mode Register (UA0MOD)

Address: 0x4100_1008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	U0 DIR	U0 NEG	U0 STP	U0PT[1:0]		U0LG[1:0]		–*	U0 RSS	–*	–*	–*	U0CK[1:0]		–*
Access	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W	–	–	–	R/W	R/W	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA0MOD is a special function register (SFR) used to set the transfer mode of the UART.

[Description of Bits]

- **U0CK[1:0]** (bit 2 to 1)
  The U0CK[1:0] bits are used to select the clock to be input to the baud rate generator of the UART.

U0CK[1]	U0CK[0]	Description
0	0	LSCLK (initial value)
0	1	Prohibited
1	0	OSCLK
1	1	Prohibited

- **U0RSS** (bit 6)
  U0RSS is the bit that selects the UART received data input sampling timing.

U0RSS	Description
0	Value set in the UA0BRT registers/2 (initial value)
1	Value set in the UA0BRT registers/2-1

- **U0LG[1:0]** (bit 9 to 8)
  The U0LG[1:0] bit are used to specify the data length in the communication of the UART.

U0LG[1]	U0LG[0]	Description
0	0	8 bit length (initial value)
0	1	7 bit length
1	0	6 bit length
1	1	5 bit length

- **U0PT[1:0]** (bit 11 to 10)
  The U0PT[1:0] bits are used to select "even parity", "odd parity", or "no parity" in the communication of the UART.

U0PT[1]	U0PT[0]	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 12)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bit

- **U0NEG** (bit 13)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 14)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

[Note]
Always set UA0MOD while communication is stopped, and do not rewrite it during communication.

17.2.7. UART0 Baud Rate Register (UA0BRT)

Address: 0x4100_100C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_3FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	U0BR[13:0]													
Access	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA0BRT is special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 17.3.2, "Baud Rate".

[Note]
Always set UA0BRT while communication is stopped, and do not rewrite it during communication.

17.2.8. UART0 Receive Status Register (UA0STAT)

Address: 0x4100_1010
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	U0PER	U0OER	U0FER
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA0STAT is a special function register (SFR) used to indicate the UART state in receive operations.
When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]

- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". U0FER is updated each time reception is completed.

U0FER	Description
0	No framing error (initial value)
1	With framing error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" unless the previously received data is not read. Therefore, make sure that data is always read from the receive buffer even if the data is not required.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated whenever data is received.

U0PER	Description
0	No parity error (initial value)
1	Parity error

17.2.9. UART0 Transmit Status Register (UA1STAT)

Address: 0x4100_1030
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	U1FUL	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA1STAT is a special function register (SFR) used to indicate the UART state in transmit operations.
When any data is written to UA1STAT, the flag is initialized to "0".

[Description of Bits]

- **U1FUL** (bit 3)
  U1FUL indicates the UART transmit buffer state.
  When the transmitted data is written in UA1BUF, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U1FUL flag becomes "0", then write the next transmitted data to the UA1BUF.

U1FUL	Description
0	No data in the transmit buffer (UA1BUF)(initial value)
1	Data present in the transmit buffer (UA1BUF)

17.2.10. UART0 Interrupt Status Register (UA0INTST)

Address: 0x4100_1038
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	U0TXINT	U0RXINT
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UA0INTST is a special function register (SFR) used to display the source of interrupt.

[Description of Bits]

- **U0RXINT** (bit 0)
  This bit is set to "1" when U0RXINT interrupt (reception interrupt) request is generated. The U0RXINT interrupt can be clear by writing "1" to this bit.

U0RXINT	Description
0	UART0 reception interrupt is not occurred (initial value)
1	UART0 reception interrupt is occurred

- **U0TXINT** (bit 1)
  This bit is set to "1" when U0TXINT interrupt (transmission interrupt) request is generated. The U0TXINT interrupt can be clear by writing "1" to this bit.

U0TXINT	Description
0	UART0 transmission interrupt is not occurred (initial value)
1	UART0 transmission interrupt is occurred

17.3. Description of Operation

17.3.1. Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bit can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bit" are available and LSB first or MSB first selectable as a communication direction. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UART0 mode register (UA0MOD1).
Figure 17-2 and Figure 17-3 show the positive logic input/output format and negative logic input/output format, respectively.

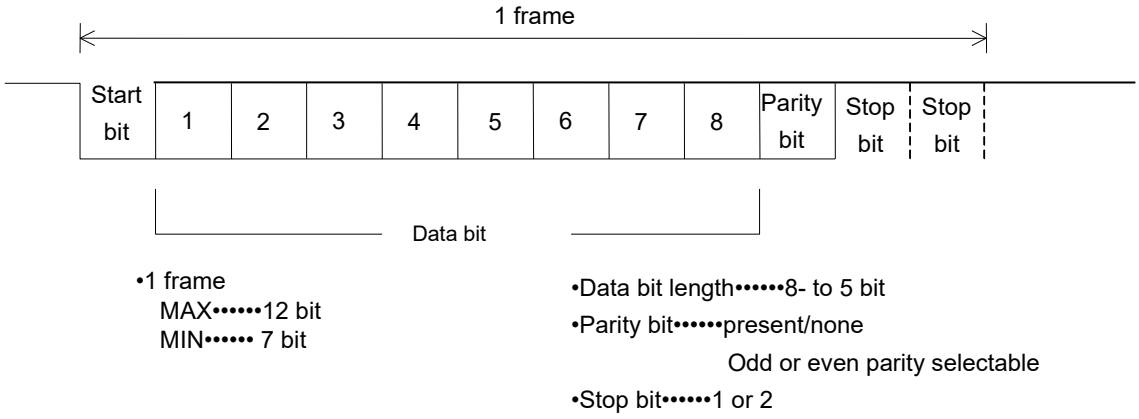


Figure 17-2 Positive Logic Input/Output Format

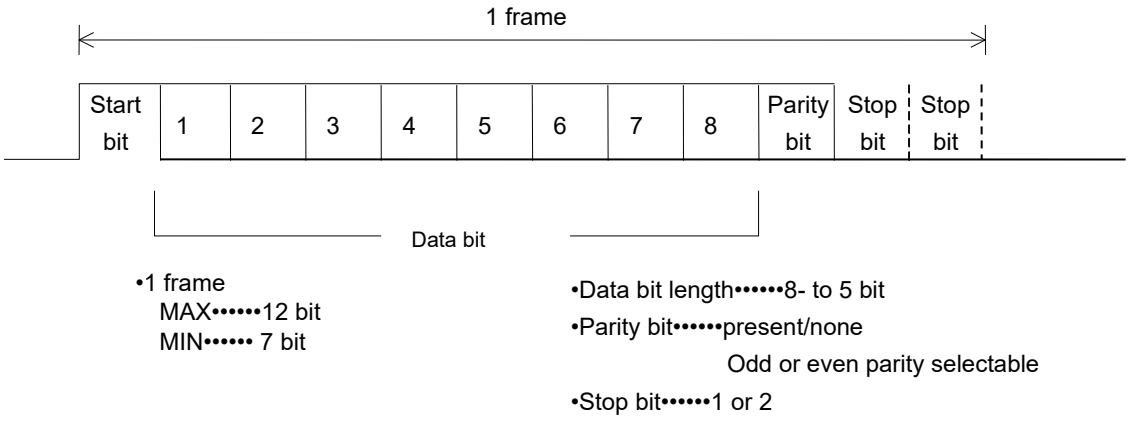


Figure 17-3 Negative Logic Input/Output Format

17.3.2. Baud Rate

Baud rates are generated by the baud rate generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bit (U0CK[1:0]) of the UART0 mode register 0 (UA0MOD0). The count value of the baud rate generator can be set by writing it in the UART0 baud rate register (UA0BRT). The maximum count is 16384.
The setting value of UA0BRT is expressed by the following equation.

$$UA0BRT = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 17-1 lists the count values for typical baud rates.

Table 17-1 Count Values for Typical Baud Rates

Baud rate (Bps)	Baud rate generator clock selection	Baud rate generator counter value			Error*1
	Baud rate clock	Count value	Period of cycle	UA0BRT	
2400	16MHz	6667	Approx. 417us	0x0000_1A0A	0.00%
4800		3333	Approx. 208us	0x0000_0D04	0.01%
9600		1667	Approx. 104us	0x0000_0682	-0.02%
19200		833	Approx. 52us	0x0000_0340	0.04%
38400		417	Approx. 26us	0x0000_01A0	-0.08%
57600		278	Approx. 17.4us	0x0000_0115	-0.08%
115200		139	Approx. 8.7us	0x0000_008A	-0.08%
2400	24MHz	10000	Approx. 417us	0x0000_270F	0.00%
4800		5000	Approx. 208us	0x0000_1387	0.00%
9600		2500	Approx. 104us	0x0000_09C3	0.00%
19200		1250	Approx. 52us	0x0000_04E1	0.00%
38400		625	Approx. 26us	0x0000_0270	0.00%
57600		417	Approx. 17.4us	0x0000_01A0	-0.08%
115200		208	Approx. 8.7us	0x0000_00CF	0.16%

*1:The error does not include the clock error. Use this in consideration of an error of Baud rate clock.

17.3.3. Transmitted Data Direction

Figure 17-4 shows the relationship between the transmit/receive buffer and the transmit/receive data.

Transmit:n=1, Receive:n=0

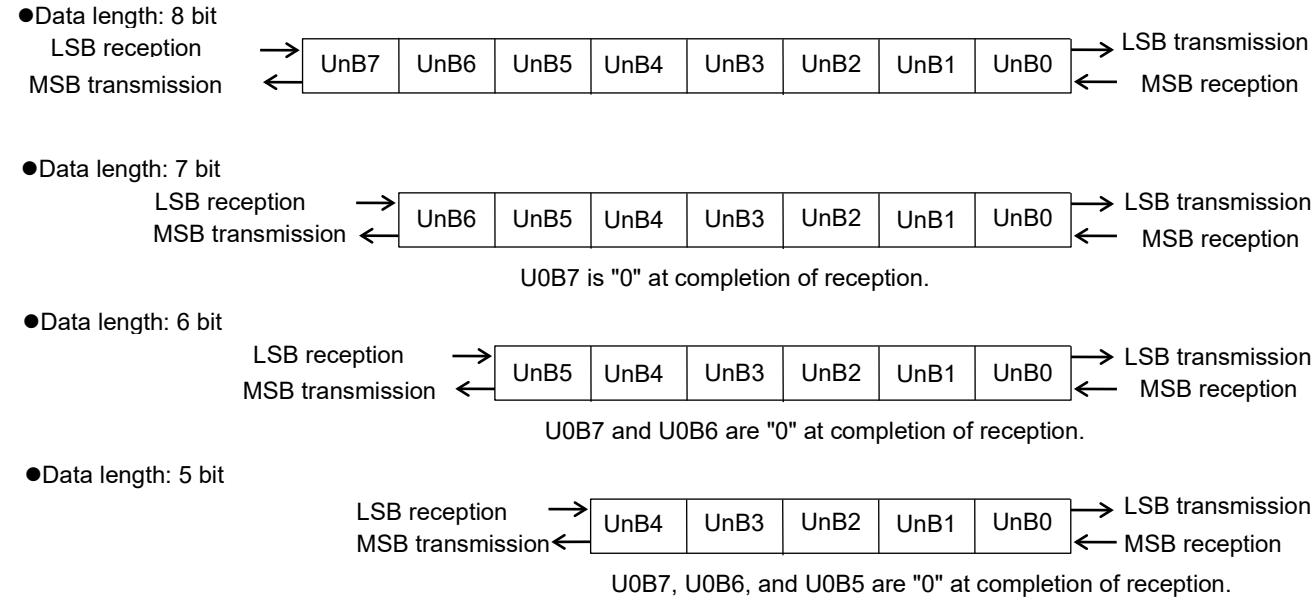


Figure 17-4 Relationship between Transmit/Receive Buffer and Transmit/Receive Data

17.3.4. Transmit Operation

Transmission is started by setting the U0EN bit of the UART0 control register (UA0CON) to "1" and set transfer data to UA1BUF. The order of UA0EN setting and UA1BUF setting does not matter.
Figure 17-5 shows the operation timing for transmission.

When the U0EN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmit operation. Set U1EN to “1” before start transmit.
The start bit is output to the TXD pin by the falling edge of the internal transfer clock (②). Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UART0 interrupt is requested. In the UART0 interrupt routine, the next data to be transmitted is written to the transmit buffer (UA1BUF).
When the next data to be transmitted is written to the transmit buffer (UA1BUF), the transmit buffer status flag (U1FUL) is set to "1" (③) and a UART transmission interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. At this time if the UART transmission interrupt routine is terminated without writing the next data to the transmit buffer, the U1FUL bit is not set to "1" (⑤). The transmit operation stops when the stop bit is sent, the U1EN bit is reset to "0", and the UART transmission interrupt is requested.
The valid period for the next transmit data to be written to the transmit buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

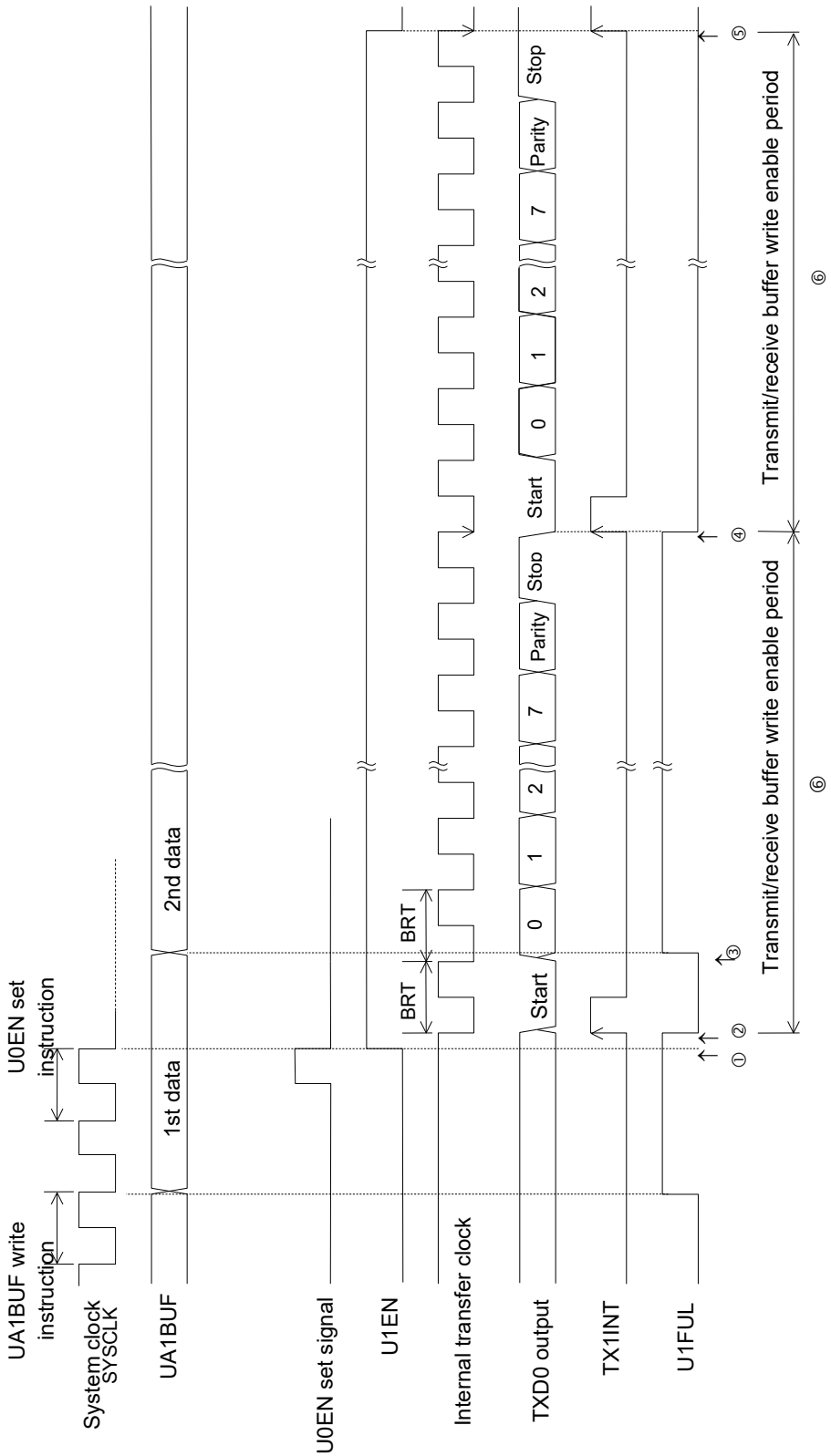


Figure 17-5 Operation Timing in Transmission

17.3.5. Receive Operation

Select the receive data pin using the U0RSEL bit of the UART0 mode register 0 (UA0MOD0). Reception is started by setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 17-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXD and waits for the arrival of a start bit.
When detecting a start bit (②), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5 to 8 bit received data is transferred to the receive buffer (UA0BUF) concurrently with the falling edge of the internal transfer clock of ③.
The LSI requests a UART reception interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UART0 status register (UA0STAT) to "1".

Parity error : U0PER ="1"
Overrun error : U0OER ="1"
Framing error : U0FER ="1"

As shown in Figure 17-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the U0EN bit is reset to "0" by the program. When the U0EN bit is reset to "0" during reception, the received data may be destroyed. When the U0EN bit is reset to "0" during the "U0EN reset enable period" in Figure 17-6, the received data is protected.

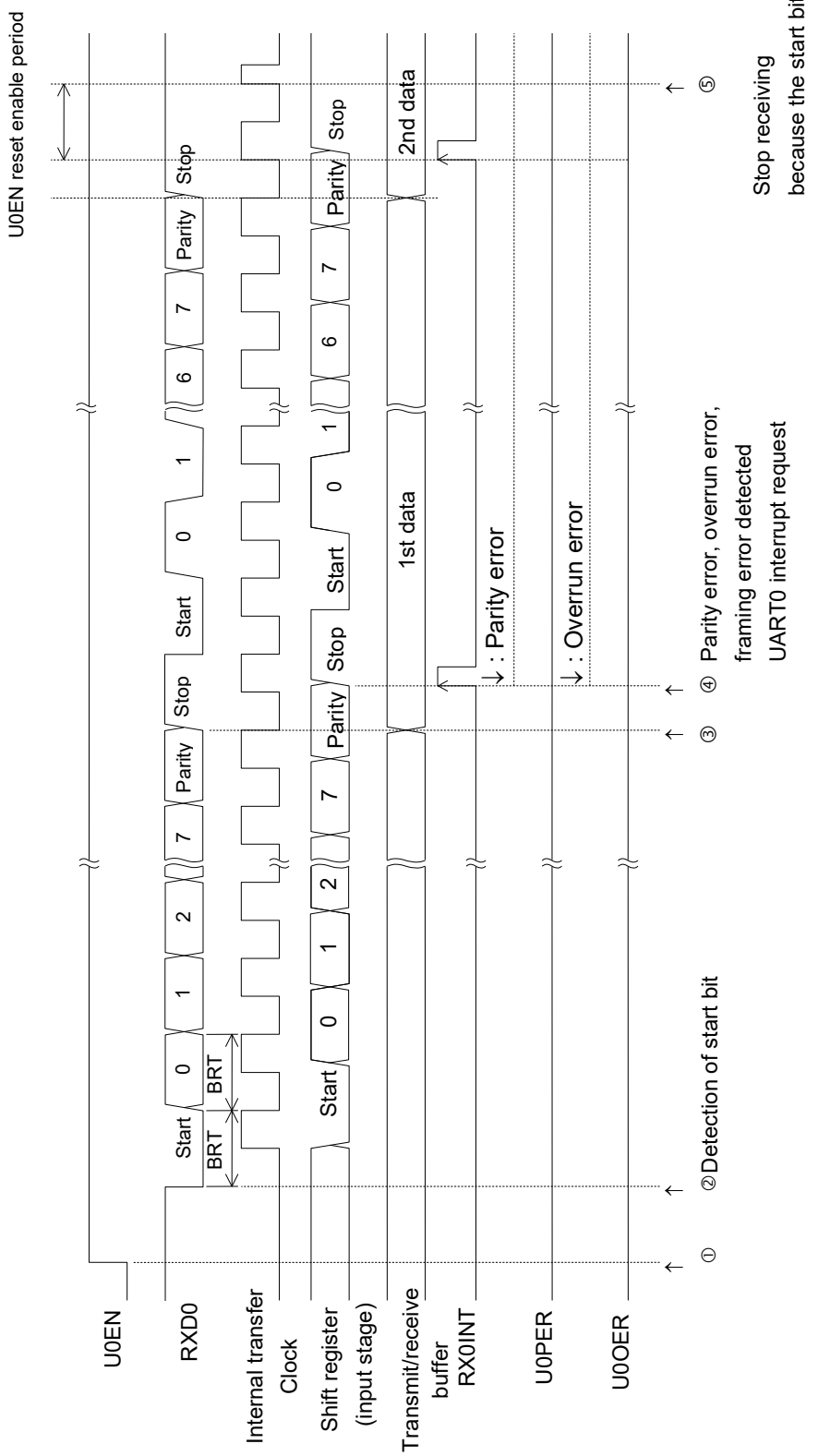


Figure 17-6 Operation Timing in Reception

17.3.5.1. Detection of Start Bit

The start bit is sampled with the baud rate generator clock (OSCLK). Therefore, the start bit detection may be delayed for one cycle of the baud rate generator clock at the maximum.
Figure 17-7 shows the start bit detection timing.

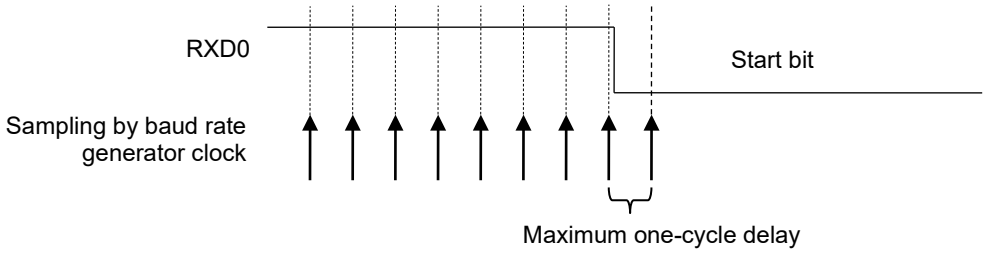
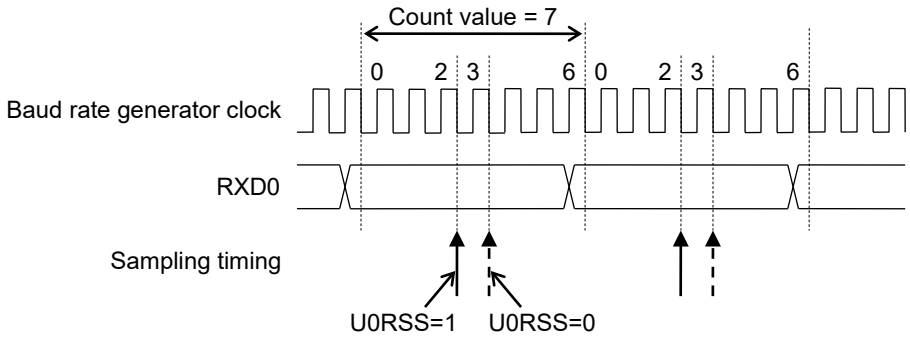


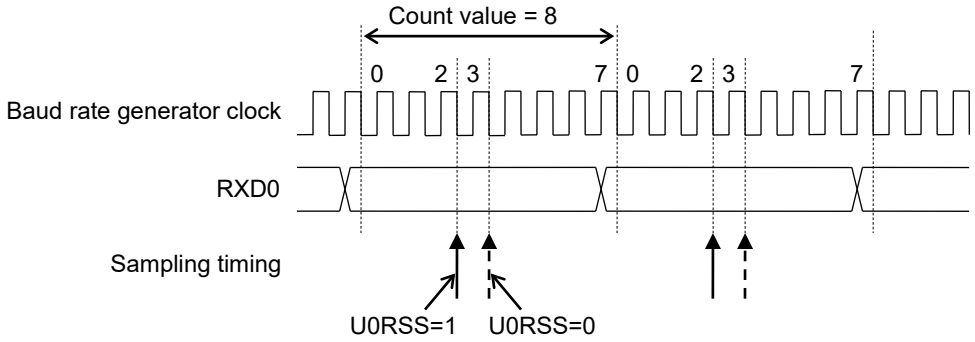
Figure 17-7 Start Bit Detection Timing (Positive Logic)

17.3.5.2. Sampling Timing

When the start bit is detected, the received data that was input to the RXD is sampled almost at the center of the baud rate, then loaded to the shift register.
The loading sampling timing of this shift register can be adjusted for one clock of the baud rate generator clock, using the U0RSS bit of the UART0 mode register (UA0MOD).
Figure 17-8 shows the relationship between the U0RSS bit and the sampling timing.



(1) When the baud rate generator count value is "7" (odd)



(2) When the baud rate generator count value is "8" (even)

Figure 17-8 Relationship between U0RSS Bit and Sampling Timing

17.3.5.3. Receive Margin

If there is an error between the sender baud rate and the baud rate generated by the baud rate generator of this LSI, the error accumulates until the last stop bit loading in one frame, decreasing the receive margin.
Figure 17-9 shows the baud rate errors and receive margin waveforms.

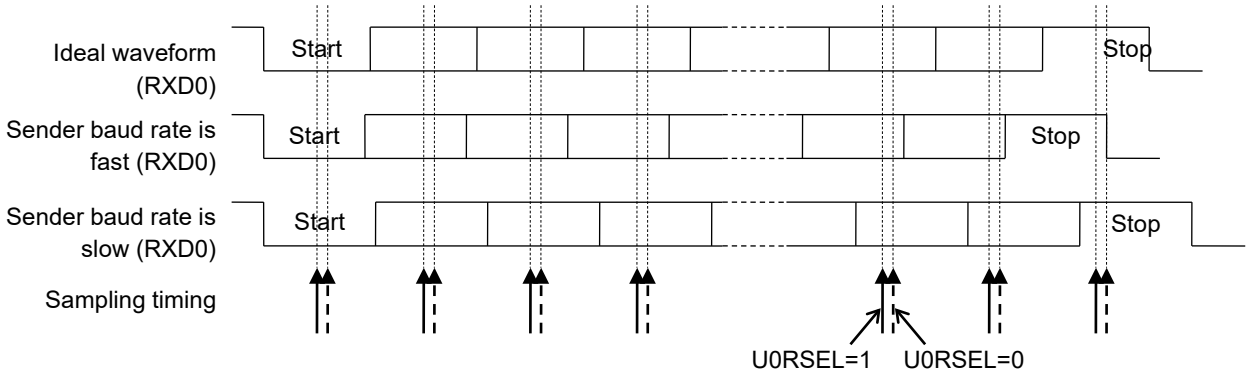


Figure 17-9 Baud Rate Error and Receive Margin

[Note]
In system designing, ensure a sufficient receive margin considering the baud rate difference between sender and receiver, start bit detection delay, distortion in receive data, and influence of noise.

17.3.6. DMA Request

UART generates the external request to DMAC.
As external request of UART (receive) is generated when the data is received, read the received data from UART0 Receive Buffer Register (UA0BUF) by the DMAC.
As external request of UART (transmit) is generated when transmit data is empty, write the transmit data toUART0 Transmit Buffer Register (UA1BUF) by the DMAC.

Chapter 18

UART with FIFO (UARTF)

18. UART with FIFO (UARTF)

18.1. General Description

The UART with FIFO (UARTF) functions as the input/output interface, carries out serial-to-parallel conversion of the data sent from the peripheral devices, and also converts the parallel data sent from the CPU into serial data. The UART has a 16-byte FIFO for transmission and reception, capable of storing up to 16 bytes of data during transmission/reception in the FIFO mode.
Further, the receive FIFO generates 3 bits of error data for every byte of received data. The CPU can read out the UARTF state at any time. The information that can be read out consists of the type and status of the transfer operation under execution, and the statuses of errors such as parity, overrun, framing errors, and break interrupt, etc.

The I/O pins of the UARTF are assigned as the quaternary function of the port 0 and secondary function of port3, 4, and 5. For the ports 0, 3, 4, and 5, see Chapter 22 "Port".

18.1.1. Features

- Full duplex buffer system
- All status reporting function
- 16-byte transmit and receive FIFOs
- Independent control of transmit, receive, line status data set interrupt and FIFO
- Programmable serial interface
  - 5, 6, 7, and 8 bit characters
  - Odd parity, even parity, no parity generation and verification
  - 1, 1.5, or 2 stop bit
- Communication speed: Settable within the range of 2400bps to 115200bps.
- Built-in baud rate generator.
- Generates transmission/receive DMA request

18.1.2. Configuration

Figure 18-1 shows the configuration of the UARTF.

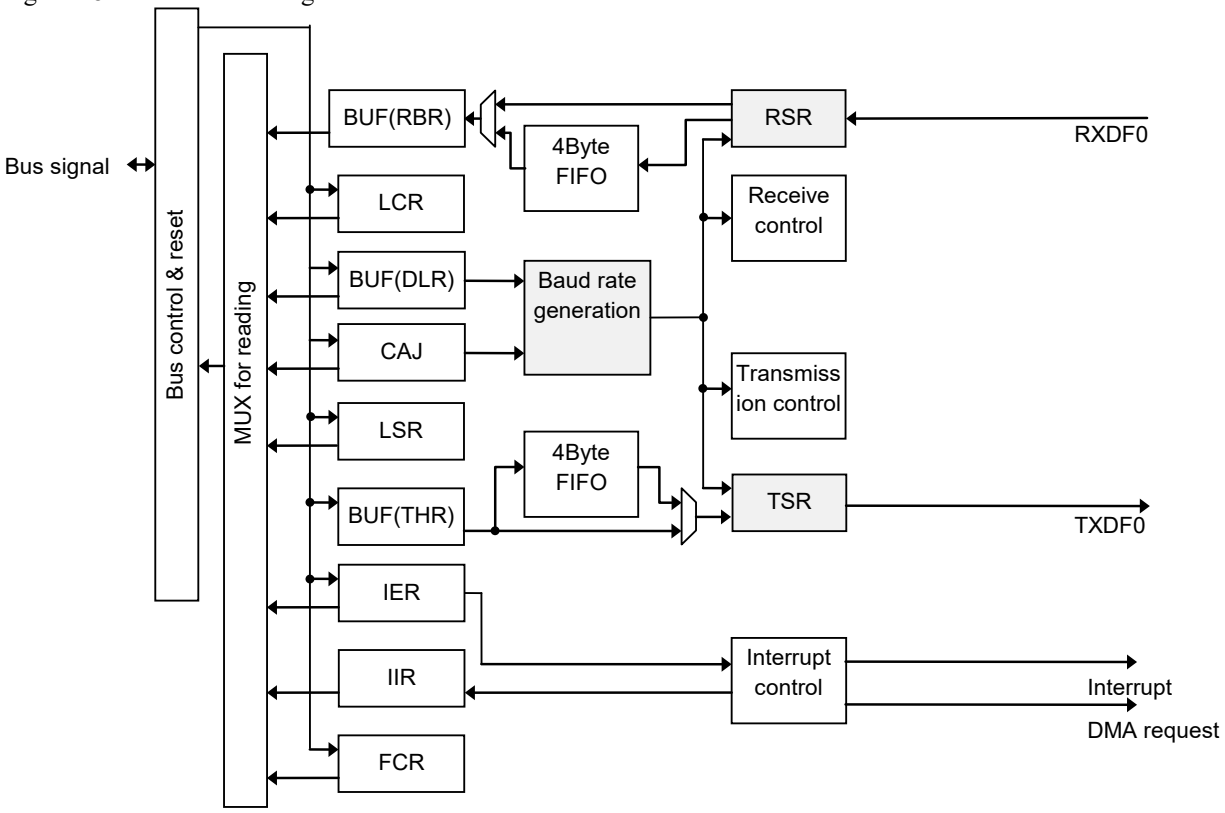


Figure 18-1 Configuration of UARTF

Table 18-1 Corresponding Port list

PIN Name	Corresponding Port
RXDF0	P00/P32/P42/P52
TXDF0	P01/P33/P43/P53

18.1.3. List of Pins

Pin Name	I/O	Function
RXDF0	I	UARTF0 data input pin
TXDF0	O	UARTF0 data output pin

18.2. Description of Registers

18.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4100_1800	UARTF0 transmit/receive buffer	UAF0BUF	R/W	32	0x0000_00xx
0x4100_1804	UARTF0 interrupt enable register	UAF0IER	R/W	32	0x0000_0000
0x4100_1808	UARTF0 interrupt status register	UAF0IIR	R	32	0x0000_0001
0x4100_180C	UARTF0 mode register	UAF0MOD	R/W	32	0x0000_0000
0x4100_1810	UARTF0 line status register	UAF0LSR	R	32	0x0000_0160
0x4100_1814	UARTF0 clock adjustment register	UAF0CAJ	R/W	32	0x0000_000D

18.2.2. UARTF0 Transmit/Receive Buffer (UAF0BUF)

Address: 0x4100_1800
Access: R/W
Access size: 32 bit
Initial value: 0x0000_00xx

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	UF0B[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UAF0BUF is a special function register (SFR) that provides the following three functions.

[Description of Bits]

(1) Read-only register for buffering received data: Receiver Buffer Register (RBR)
RBR is the register that holds received data from 5 to 8 bit depending on the character length.
The bit 0 of a data word is always the first serial data bit received. If data less than 8 bit is received, the data is entered in the right justified manner towards the LSB.
When the UART carries out parallel-to-serial or serial-to-parallel conversion operation, the register has the double buffer configuration so that read operations can be made.
RBR can be read by program when UF0DLAB of UAF0MOD is 0. When UAF0BUF is read, RBR can be read from UF0B[7:0]. For UF0B[15:8], 0x00 can be read.
The reset value is undefined.

(2) Write-only register for setting transmitted data: Transmitter Holding Register (THR)
THR is the register that holds transmitted data from 5 to 8 bit depending on the character length.
The bit 0 of the data word is always the first serial data bit that is transmitted.
When the UART carries out parallel-to-serial or serial-to-parallel conversion operation, the register has the double buffer configuration so that write operations can be made.
THR can be written by program when UF0DLAB of UAF0MOD is 0. When UAF0BUF is written, the UF0B[7:0] data is written to THR. The UF0B[15:8] data are invalid.

(3) 16 bit divisor latch for baud rate generator: Divisor Latch Resister (DLR)
DLR can be read/written by program when UF0DLAB of UAF0MOD is 1. For details, see "Baud rate clock generation".

	UF0DLAB = 0		UF0DLAB = 1	
	UAF0BUF[15:8]	UAF0BUF[7:0]	UAF0BUF[15:8]	UAF0BUF[7:0]
Read	0x00	RBR	DLR[15:8]	DLR[7:0]
Write	Disabled	THR	DLR[15:8]	DLR[7:0]

18.2.3. UARTF0 Interrupt Enable Register (UAF0IER)

Address: 0x4100_1804
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	UF0TEMTI	_*	_*	_*	UF0ELSI	UF0ETBEI	UF0ERBFI
Access	–	–	–	–	–	–	–	–	–	R/W	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UAF0IER is a special function register (SFR) used to set whether to enable/disable the UART interrupt source.

[Description of Bits]

- **UF0ERBFI** (bit 0)
  UF0ERBFI is used to set Enable/disable the received data read request interrupt (including character timeout interrupt in the FIFO mode).

UF0ERBFI	Description
0	Disable the received data read request interrupt (Includes the character timeout interrupt when FIFO is enabled) (initial value)
1	Enable the received data read request interrupt (Includes the character timeout interrupt when FIFO is enabled)

- **UF0ETBEI** (bit 1)
  UF0ETBEI is used to set Enable/disable the transmitted data write request interrupt.

UF0ETBEI	Description
0	Disable the transmitted data write request interrupt (initial value)
1	Enable the transmitted data write request interrupt

- **UF0ELSI** (bit 2)
  UF0ELSI is used to set Enable/disable the received data error interrupt.

UF0ELSI	Description
0	Disable the received data error interrupt (initial value)
1	Enable the received data error interrupt

- **UF0TEMTI** (bit 6)
  UF0TEMTI is used to set Enable/disable of the transmission idle interrupt.

UF0TEMTI	Description
0	Disable the transmission idle interrupt (initial value)
1	Enable the transmission idle interrupt

18.2.4. UARTF0 Interrupt Status Register (UAF0IIR)

Address: 0x4100_1808
Access: R
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	UF0FMD[1:0]		–*	–*	UF0IRID[2:0]			UF0IRP
Access	–	–	–	–	–	–	–	–	R	R	–	–	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UAF0IIR is a special function register (SFR) used to indicate the UART state in interrupt transmit/receive operations. UAF0IIR stores information indicating that an interrupt with a certain priority level is pending, along with the type of that interrupt. IIR indicates the interrupt with the highest priority level that is pending.

[Description of Bits]

- **UF0IRP** (bit 0)
  UF0IRP indicates whether a UARTF0 interrupt was generated.

UF0IRP	Description
0	Interrupt was generated
1	Interrupt was not generated (initial value)

- **UF0IRID[2:0]** (bit 3 to 1)
  UF0IRID[2:0] indicate the interrupt source of the UARTF0 interrupt.
  LVL=1 is the highest priority. The highest-priority interrupt source is notified.

UF0IRID[2:0]	LVL	Flag	Source	Reset Process
000	–	–	No interrupt source (initial value)	–
011	1	Received data error	Overrun error, parity error, framing error, break interrupt	Read UAF0LSR
010	2	Received data read request	FIFO disabled: The received data is available. FIFO enabled: Reached the Trigger level	Read RBR, or when FIFO drops below trigger level
110	2	Character timeout	At least one character is present in the receive FIFO, and no other character was placed into or read out within 4 character time.	Read RBR
001	3	Transmitted data write request	FIFO disabled: THR write enabled. FIFO enabled: The transmit FIFO data becomes empty.	Read UAF0IIR or write THR
101	4	Transmission idle	THR and TSR are empty and not during the UART transmission.	Write THR

- **UF0FMD[1:0]** (bit 7 to 6)
  UF0FMD[1:0] indicate the FIFO mode.

UF0FMD [1]	**UF0FMD [0]**	Description
0	0	Non-FIFO mode (initial value)
0	1	Unused
1	0	Unused
1	1	FIFO mode

18.2.5. UARTF0 Mode Register (UAF0MOD)

Address: 0x4100_180C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	UF0FTL[3:0]				–*	UF0TFR	UF0RFR	UF0FEN	UF0DLAB	UF0BC	UF0PT[2:0]			UF0STP	UF0LG[1:0]	
Access	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UAF0MOD is a special function register (SFR) used to set the mode of the UART.

[Description of Bits]

- **UF0LG[1:0]** (bit 1 to 0)
  UF0LG[1:0] specify the character length of UARTF0.

UF0LG[1]	UF0LG[0]	Description
0	0	5 bit length (initial value)
0	1	6 bit length
1	0	7 bit length
1	1	8 bit length

- **UF0STP** (bit 2)
  UF0STP selects the stop bit count of the character transmitted by UARTF0.

UF0STP	Description
0	1 stop bit (initial value)
1	1.5 stop bit (when character length = 5 bit) 2 stop bit (when character length = 6, 7, or 8 bit)

- **UF0PT[2:0]** (bit 5 to 3)
  UF0PT[2:0] select the parity bit of UARTF0.

UF0PT[2]	UF0PT[1]	UF0PT[0]	Description
*	*	0	No parity bit (initial value)
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Parity bit fixed to "1"
1	1	1	Parity bit fixed to "0"

- **UF0BC** (bit 6)
  UF0BC selects the break control of UARTF0.
  Turning this to "1" brings the UARTF0 data output (TXDF0) to the spacing state (logical 0). The control by this bit is valid only on the TXDF0 pin. This means that TXDF0 is masked but the transmit operation continues internally. The use of the break control allows the CPU to send an alarm to the terminal of the computer communication system.

UF0BC	Description
0	Break control not implemented (initial value)
1	Break control implemented

- **UF0DLAB** (bit 7)
  UF0DLAB selects the access register of UAF0BUF.
  When this is "0", RBR and THR are accessible. When this is "1", DLR is accessible.

UF0DLAB	Description
0	RBR and THR of UAF0BUF are accessible (initial value)
1	DLR of UAF0BUF is accessible

- **UF0FEN** (bit 8)
  UF0FEN selects whether FIFO is enabled or disabled for UARTF0.

UF0FEN	Description
0	FIFO disabled (initial value)
1	FIFO enabled

[Note]
FIFO will be cleared when switching between FIFO enable/disable.

- **UF0RFR** (bit 9)
  UF0RFR instructs to reset the receive FIFO of UARTF0.

UF0RFR	Description
0	Receive FIFO normal operation (initial value)
1	Clears the receive FIFO

[Note]
When the receive clearance is selected, data being received is not cleared.

- **UF0TFR** (bit 10)
  UF0TFR selects to clear the transmit FIFO of UARTF0.

UF0TFR	Description
0	Transmit FIFO normal operation (initial value)
1	Clears the transmit FIFO

[Note]
When the transmit clearance is selected, data being transmitted is not cleared.

- **UF0FTL[3:0]** (bit 15 to 12)
  UF0FTL[3:0] select the trigger level for the receive FIFO interrupt.

UF0FTL[3]	UF0FTL[2]	UF0FTL[1]	UF0FTL[0]	Description
0	0	0	0	1 byte (initial value)
0	0	0	1	2 bytes
0	0	1	0	3 bytes
0	0	1	1	4 bytes
0	1	0	0	5 byte
0	1	0	1	6 bytes
0	1	1	0	7 bytes
0	1	1	1	8 bytes
1	0	0	0	9 byte
1	0	0	1	10 bytes
1	0	1	0	11 bytes
1	0	1	1	12 bytes
1	1	0	0	13 byte
1	1	0	1	14 bytes
1	1	1	0	15 bytes
1	1	1	1	16 bytes

18.2.6. UARTF0 Line Status Register (UAF0LSR)

Address: 0x4100_1810
Access: R
Access size: 32 bit
Initial value: 0x0000_0160

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	UF0TIDL	UF0RFE	UF0TEMT	UF0THRE	UF0BI	UF0FER	UF0PER	UF0OER	UF0DR
Access	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UAF0LSR is a special function register (SFR) used to display the status.
UAF0LSR is normally the first register read out by the CPU for determining the interrupt cause or for polling the status of the serial communication channel.
UF0OER, UF0PER, UF0FER, and UF0BI are error conditions, which generate a received data error interrupt (a LVL=1 interrupt in the IIR) if any of the states is detected. This interrupt is enabled by setting UF0ELSI of UARTF0IER to 1.

[Description of Bits]

- **UF0DR** (bit 0)
  UF0DR is set to 1 when the input character has been received and transmitted to RBR. This bit is cleared when the RBR data is read.

UF0DR	Description
0	No valid data in RBR (initial value)
1	There is valid data in RBR

- **UF0OER** (bit 1)
  UF0ER indicates that an overrun error occurred. The overrun error indicates that the CPU did not read the data in RBR before the next character was sent to RBR to overwrite the previous character. In FIFO mode, an overrun error occurs after the FIFO has become full when the next character is completely received. Reading UAF0LSR after an overrun error will clear the overrun error. The character during reception is overwritten instead of being transferred to FIFO. This bit is cleared when UAF0LSR is read.

UF0OER	Description
0	No overrun error (initial value)
1	Overrun error occurred

- **UF0PER** (bit 2)
  UF0PER indicates that a parity error occurred. This is enabled only when parity is enabled. This bit is cleared when UAF0LSR is read. In FIFO mode, this bit indicates that an error exists for the leading data. If a parity error occurs in the data that is not the leading data in the FIFO, it is not reflected to this bit.

UF0PER	Description
0	No parity error (initial value)
1	Parity error occurred

- **UF0FER** (bit 3)
  UF0FER indicates that a framing error occurred. A framing error indicates that there is no valid stop bit in the received character. This bit is set to "1" when the stop bit after the last data bit or after the parity bit is "0" (spacing level). This bit is cleared when UAF0LSR is read. In FIFO mode, the framing error is related to a specific character in the FIFO. This bit indicates that an error is present when that character comes to the beginning of the FIFO.

UF0FER	Description
0	No framing error (initial value)
1	Framing error occurred

- **UF0BI** (bit 4)
  UF0BI indicates that a break interrupt occurred. This bit is set to "1" when the input data is maintained in the spacing ("0") state during the transmission of one frame (start bit + data bit + parity bit + stop bit). This bit will be cleared when the CPU reads UAF0LSR. In FIFO mode, this is related to a specific character in the FIFO. This bit reflects the break interrupt state when the break character comes to the beginning of the FIFO. The CPU erases the error if the related character comes to the beginning of the FIFO before the first reading of UAF0LSR. When a break interrupt occurs, only one zero character will be loaded into the FIFO.

UF0BI	Description
0	No break interrupt (initial value)
1	Break interrupt occurred

- **UF0THRE** (bit 5)
  UF0THRE indicates that preparations have been made for calling a new character to be transmitted by the UART. This bit is set to "1" when the character is transferred from THR to the shift register for transmission (TSR). This bit is cleared to "0" by writing to THR. This bit will not be cleared by reading out the UAF0LSR register. In FIFO mode, this bit is set when the transmit FIFO is empty. This bit is cleared when one byte is written to the transmit FIFO. If the THRE interrupt is enabled by UF0ETBEI of UAF0IER, THRE initiates the third-order priority interrupt to UAF0IIR.

UF0THRE	Description
0	Transmit data still present in the THR
1	THR ready for transmission (initial value)

- **UF0TEMT** (bit 6)
  UF0TEMT is set to "1" when both THR and the shift register for transmission (TSR) are empty. When a character is loaded into THR, this bit is cleared to "0" and remains "0" until the character is transferred from TXDF0. This bit is not cleared to "0" by reading UAF0LSR.
  In FIFO mode, this bit is set to "1" when both the transmit FIFO and the shift register are empty.

UF0TEMT	Description
0	Transmitted data remains in either THR or TSR
1	Both THR and TSR are empty (initial value)

[Note]
After transmission data were sent by TXDF0 port, this bit becomes "1", but the transmission of parity bit and the stop bit is not completed at that point.

- **UF0RFE** (bit 7)
  UF0RFE is always 0 when FIFO is disabled. In the FIFO enable, this bit is set to "1" if any of parity, framing, and break interrupt data errors exists within FIFO. This bit will be cleared when the data causing the error is read out from the RBR, or when the data causing the error is cleared by the FIFO clear and then reading out the UAF0LSR.

UF0RFE	Description
0	No data error in FIFO mode (initial value)
1	A parity error, framing error, or break interrupt occurred in FIFO mode

- **UF0TIDL** (bit 8)
  UF0TIDL becomes "1" in a transmission idle. The transmission idle shows THR and TSR are empty and UART is not transmitting. This bit is cleared by "0" by writing in THR. This bit is not cleared even if read UAF0LSR register. This bit is not cleared even if read UAF0LSR register. In the UART transmission, send the last data and become "1" after the transmission in stop bit.

UF0TIDL	Description
0	Not transmission idle
1	Transmission idle(initial value)

18.2.7. UARTF0 Clock Adjustment Register (UAF0CAJ)

Address: 0x4100_1814
Access: R/W
Access size: 32 bit
Initial value: 0x0000_000D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	UF0RMV	–*	UF0CAJ[4:0]				
Access	–	–	–	–	–	–	–	–	–	R/W	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
UAF0CAJ is a special function register (SFR) used to adjust the base clock for the baud rate clock of UARTF0.

[Description of Bits]

- **UF0CAJ[4:0]** (bit 4 to 0)
  UF0CAJ[4:0] bit adjust the base clock for the baud rate clock of UARTF0.
  Each setting of different clocks of SYSCLK is as below.

SYSCLK	UF0CAJ[4]	UF0CAJ[3]	UF0CAJ[2]	UF0CAJ[1]	UF0CAJ[0]
16/12/8/6/4MHz	0	1	1	0	1
24MHz	0	0	0	0	0

  [Note]
  When using UARTF0, always set SYSCLK to 4MHz or more. If SYSCLK is 4MHz or less, it does not work normally. For details, see 18.3.4 "Baud rate Clock Generation".

- **UF0RMV** (bit 6)
  UF0RMV bit selects the adjustment mode for the baud rate clock.

UF0RMV	Description
0	Adjustment modeEnable (initial value)
1	Adjustment mode Disable

18.3. Description of Operation

The UART is programmed with UAF0IER, UAF0MOD, DLR(UAF0BUF), and UAF0CAJ. These registers define the character length, number of stop bit, parity, baud rate, etc.
Though the registers can be written in any order, UAF0IER needs to be written to last because it controls the interrupt enable. Once the UART is programmed to be operable, these registers can be updated any time when the UART is not transmitting or receiving data.

18.3.1. Data Transmission

Figure 18-2 shows the transmission timing.

Writing data to THR will transfer the contents through the transmit FIFO to the transmit shift register. Within 16 baud rate clocks after the THRE bit rise is detected, the start bit is sent, followed by the data one bit at a time from the least significant bit. When the data to be transmitted is 7 bit, the most significant bit will not be sent. If parity is enabled by UF0PT[2:0] of UAF0MOD, then the parity bit is sent. This is followed by the stop bit which indicates the end of transmitting one frame of data.
After the data is transmitted, the UF0THRE bit of UAF0LSR is set to "1" to indicate that it is ready for the next transmission. This bit is cleared when one byte is written to the transmit FIFO. Also, if the THRE interrupt is enabled by UF0ETBEI of UAF0IER, THRE initiates a LVL=3 interrupt to UAF0IIR. If THRE is the interrupt source indicated in UAF0IR, this bit is cleared by reading the UAF0IIR register.

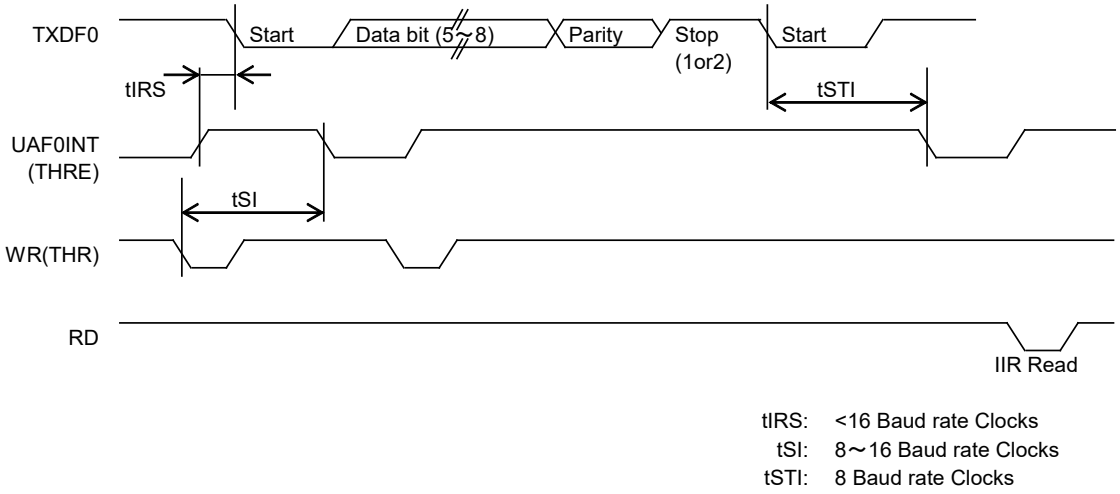


Figure 18-2 Transmission Timing

[Note]
Even if transmit FIFO is an empty state, there are some cases that all transmit processing doesn't complete. Confirm that it became the transmission idle state in UF0TIDL bit of UAF0LSR register before stopping high-speed clock (Transition to modes such as STOP / ULTRA-DEEP-HALT / DEEP-HALT / HALT-H). Or confirm that a transmission completion interrupt occurred.

18.3.2. Transmission Flow

Figure 18-3 shows the transmission flow.

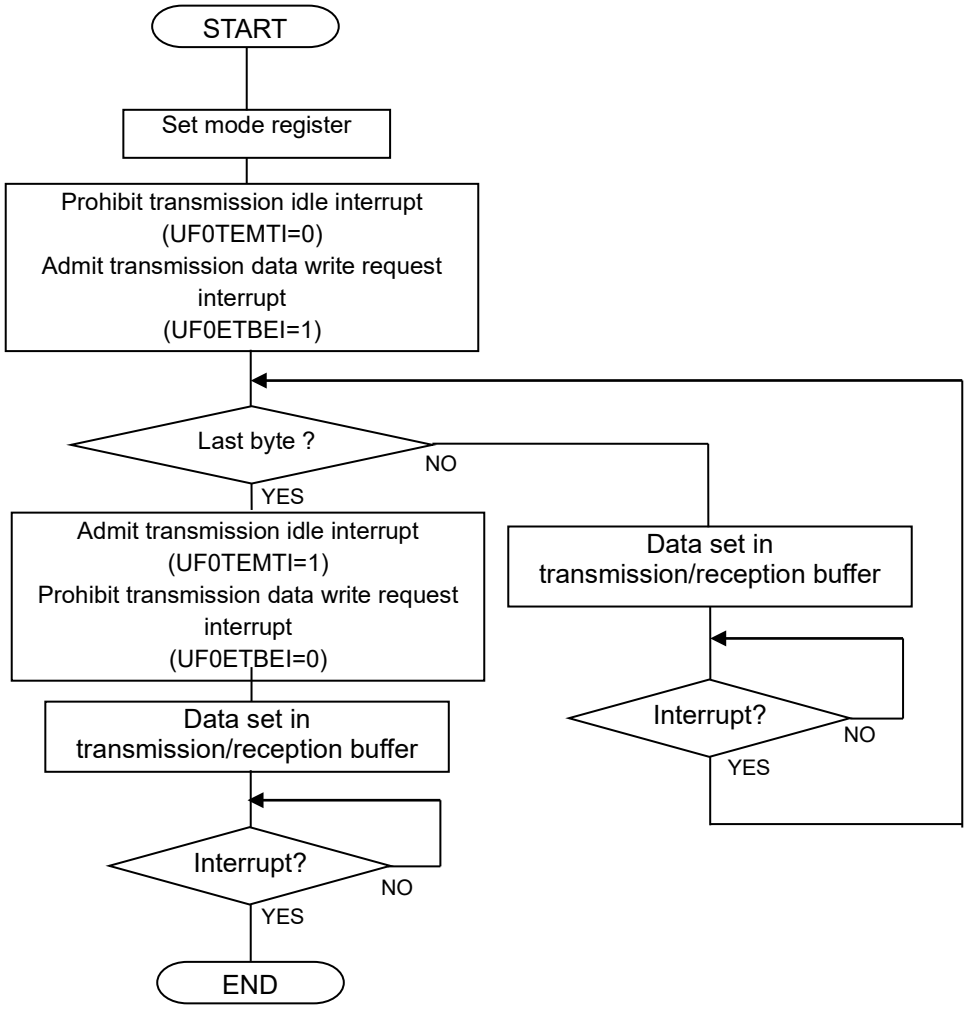


Figure 18-3 Transmission Flow

18.3.3. Data Reception

Figure 18-4 shows the relation between Baud Rate Clock and Sample CLK. Figure 18-5 shows the reception timing. Figure 18-6 shows the timing when the first byte in the receive FIFO is read, and Figure 18-7 the reception timing when the remaining bytes in the receive FIFO are read.

The sampling clock is obtained by dividing the baud rate clock by 8.
First, when the start bit is detected from RXDF0, subsequent data is obtained and transferred to the receive shift register. The data in the receive shift register is transferred to RBR through the receive FIFO.
When the data reaches RBR, UF0DR of UAF0LSR is set to "1" to indicate there is valid data in RBR. This bit is cleared by reading the data in RBR.

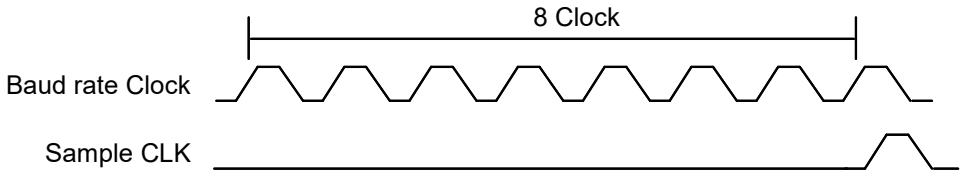


Figure 18-4 Relation between Baud Rate Clock and Sample CLK

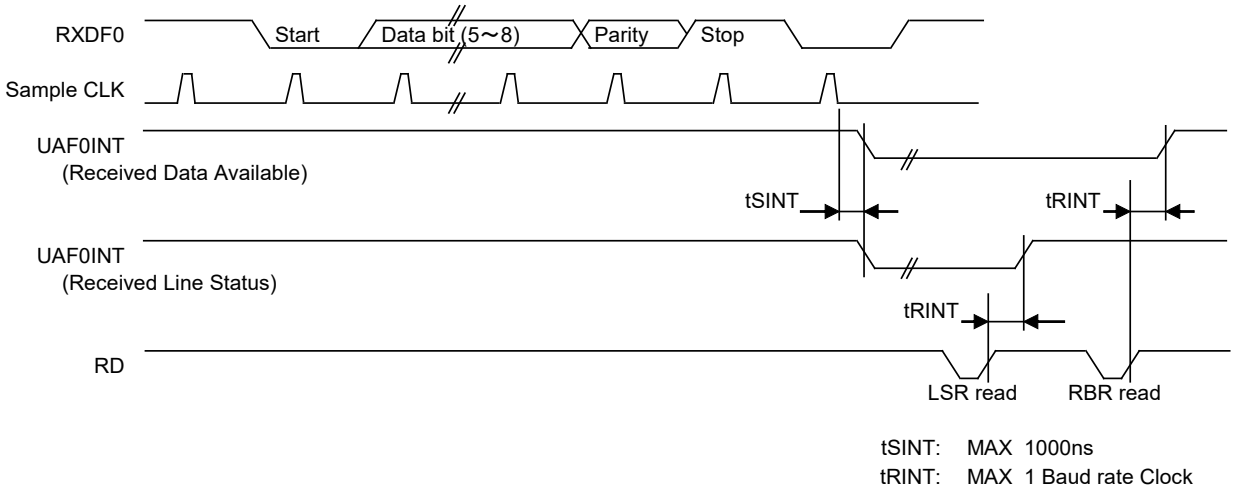


Figure 18-5 Reception Timing

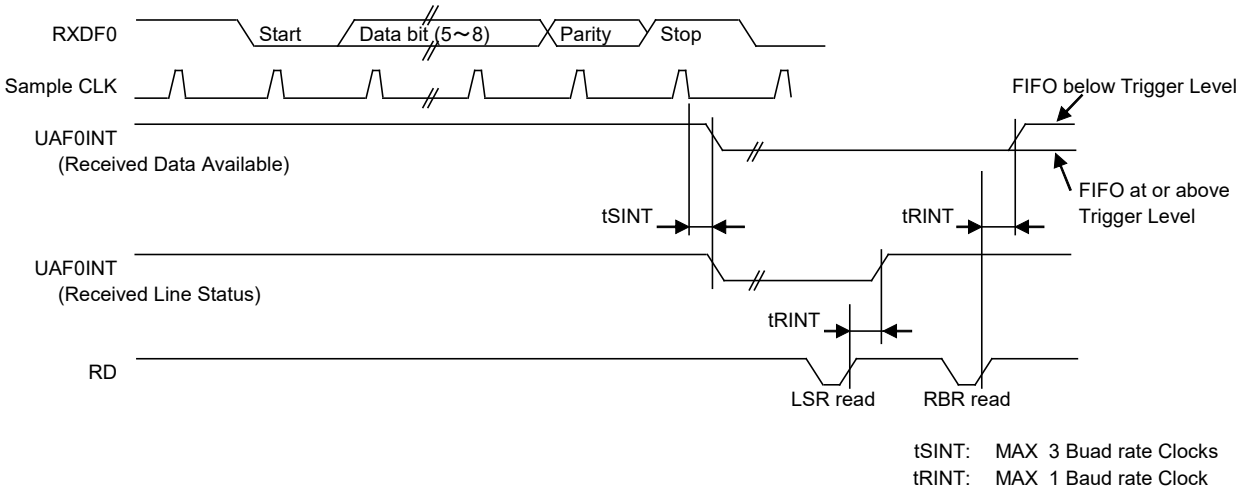


Figure 18-6 First Byte of Receive FIFO (Set RBR)

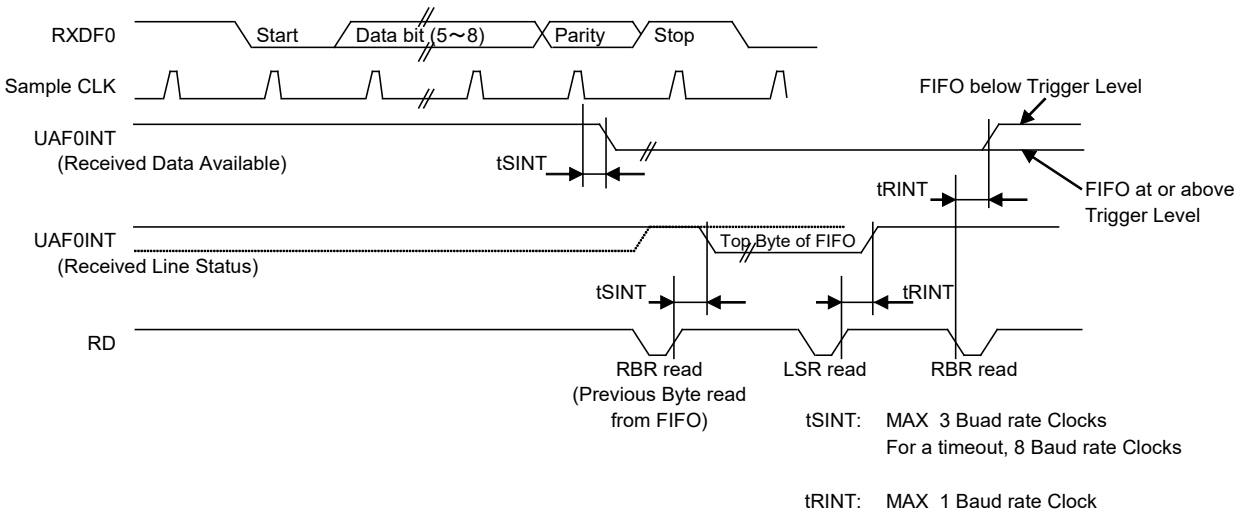


Figure 18-7 Remaining Bytes in Receive FIFO

18.3.4. Baud Rate Clock Generation

A baud rate is obtained by the following expression:

Baud rate frequency = SYSCLK x (UAF0CAJ-1)/UAF0CAJ/(DLR[15:0] x 16)

Although actually available baud rate for communication depends on the software processing, a 115200bps baud rate can be used for communication with the DLR=8 setting in an ideal state of 16MHz SYSCLK.
Make sure that the margin of error between the actual and set baud rates is within a few percent.

[Note]
Divisor (DLR[15:0]) cannot be set to 1. Set a value of 0 (stop) or greater than 2.

The following table shows the relation among SYSCLK, DLR, and baud rates.

Baud Rate (bps)	SYSCLK	UF0CAJ[4:0] (Hex)	DLR (Hex)	Error*1 (%)
2400	16MHz	0D	0181	-0.10
4800			00C0	0.16
9600			0060	0.16
19200			0030	0.16
38400			0018	0.16
57600			0010	0.16
115200			0008	0.16
2400	24MHz	00	0271	0.00
4800			0139	-0.16
9600			009C	0.16
19200			004E	0.16
38400			0027	0.16
57600			001A	0.16
115200			000D	0.16

*1: The error does not include the clock error. User this in consideration of an error of SYSCLK.

18.3.5. FIFO Mode

When the receive FIFO and reception interrupt are both enabled, reception interrupts are generated as follows:

(A) If the number of characters present within the FIFO exceeds the programmed trigger level, a received data read request interrupt is generated. This interrupt is immediately cleared when the number of characters present within the FIFO drops below the trigger level.

(B) As with the received data read request interrupt, the UAnIIR received data read request display is set to "1" if the number of characters present within the FIFO exceeds the trigger level, and cleared to "0" if it drops below the trigger level.

(C) The received data error interrupt has a higher priority than the received data read request interrupt.

(D) The received data read request flag is set to "1" as soon as the data is transferred from the receive shift register to the FIFO, and cleared to "0" when the FIFO becomes empty.

When the receive FIFO and the reception interrupt are both enabled, a character timeout interrupt is generated as follows.

(A) A character timeout interrupt is generated when the following conditions are met.

- There is at least one character present in the FIFO.
- An amount of time required to transfer at least 4 characters has elapsed since a character was last received (if 2 stop bit are specified, the time after the first stop bit is calculated).
- An amount of time required to transfer at least 4 characters has elapsed since the receive FIFO was last read.

For example, if 1 start bit + 8 character bit + 1 parity bit + 2 stop bit is specified, and the transfer speed is 2400bps, the said amount of time will be approximately 20 ms.

(B) SYSCLK is used to calculate the character time.

(C) When a character is read out from the FIFO, the character timeout interrupt and the timer used for timeout detection will be cleared.

(D) When no character timeout interrupt is generated, the timeout detection timer will be cleared when a character is read out from the FIFO or a new character is received.

The transmission interrupt is generated as follows when the transmitter section and the transmit FIFO interrupts have been enabled.

(A) If the transmit FIFO is empty, a transmitted data write request interrupt occurs. This interrupt is cleared when a character is written to the transmit FIFO or when UAnIIR is read out.

(B) When the following conditions are met, the transmitted data write request interrupt will be delayed for an amount of time equivalent to "time required to transmit one character – time when last stop bit occurred".

- There was a period when only one character was present in the FIFO after THRE (transmitted data write request) was last set.
- THRE was set.

[Note]

Transmit FIFO is an empty state, but there is the case that all transmit processing doesn't complete. Confirm that transmit shift register (TSR) became empty in UF0TIDL bit of UAF0LSR register before stopping high-speed clock (Transition to modes such as STOP / ULTRA-DEEP-HALT / DEEP-HALT / HALT-H). Or confirm that a transmission completion interrupt occurred.

18.3.6. FIFO Polled Mode

If FIFO is enabled and UF0ELSI, UF0ETBEI, UF0TEMTI and UF0ERBFI of UAF0IER are "0", the UART operates in the FIFO polled mode. Since the receiver section and transmitter section can be controlled separately, either one (or both) can be set to FIFO polled mode. In FIFO polled mode, the states of the receiver and transmitter sections must be checked by reading out the UAF0LSR (since no interrupt is generated).

- A state in which at least one character is present in the receive FIFO can be confirmed by the value "1" set to UF0DR.
- When UF0PER is cleared to "0", an interrupt will not be generated even if an error is detected while receiving a character. The error state will not be indicated on the UAF0IIR value. Therefore, the error type must be checked with the UF0BI, UF0FER, UF0PER, and UF0OER values.
- It can be known that the transmit FIFO is empty by the fact that UF0THRE has been set to "1".
- A state in which the transmit FIFO and transmit shift register are both empty can be confirmed by the value "1" set to UF0TEMT.
- A state in which the character associated with an error at the time of reception is present in the receive FIFO can be confirmed by the value "1" set to UF0RFE.
- UF0TIDL is set "1", can know that it is a transmission idle.

In FIFO polled mode, FIFO will operate; however, trigger level and timeout detection will not be performed (since they are only notified by interrupts).

18.3.7. Error Status

(a) Overrun error

An overrun error indicates that the data in RBR was not read before the next character was sent to RBR to overwrite the previous character.
At this time, UF0OER of UAF0LSR is set.

(b) Parity error

A parity error indicates that the parity of the received data and the received parity bit did not match. At this time, UF0PER of UAF0LSR is set.
Note that, this error will only occur when parity is enabled.
In FIFO mode, this bit indicates that an error exists for the leading data. If a parity error occurs in the data that is not the leading data in the FIFO, it is not reflected to UF0PER of UAF0LSR.

(c) Framing error

A framing error indicates that there is no valid stop bit in the received character. This error will occur when the stop bit after the last data bit or after the parity bit is "0" (spacing level).
At this time, UF0FER of UAF0LSR is set.
In FIFO mode, this is related to a specific character in the FIFO. UF0FER indicates that an error is present when that character comes to the beginning of the FIFO.

(d) Break interrupt

A break interrupt indicates that the input data received was maintained in the spacing ("0") state during the transmission of one frame (start bit + data bit + parity bit + stop bit).
At this time, UF0BI of the UAF0LSR register is set.
In FIFO mode, this is related to a specific character in the FIFO. UF0BI indicates that the break character is present at the beginning of the FIFO.

Chapter 19

I^2C Bus Interface

19. I²C Bus Interface

19.1. General Description

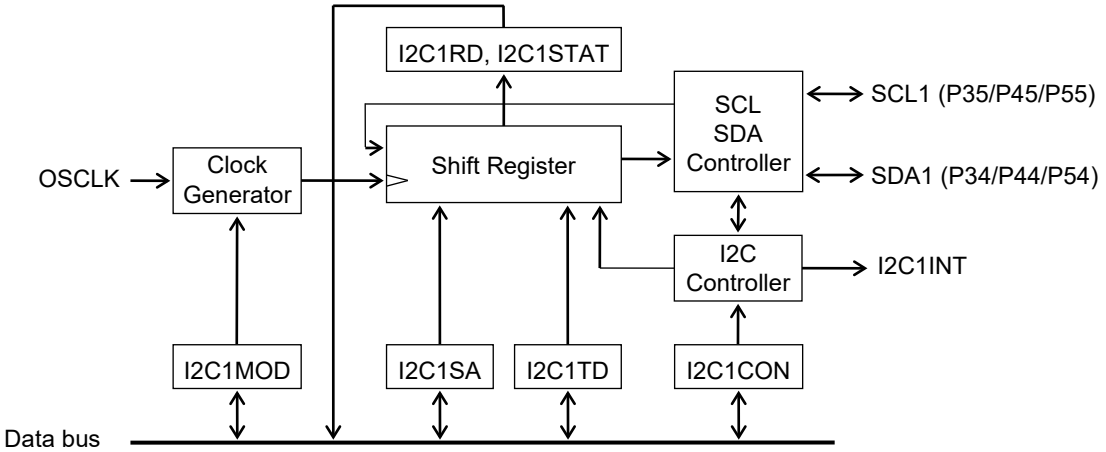
The I²C bus interface operates as the master device of I²C bus and can communicate with the slave device.
This LSI includes one channel of I²C bus interface.
The I²C bus interface data I/O pin and the I²C bus interface clock I/O pin are assigned as the secondary function of the ports 3, 4 and 5. For the ports 3, 4 and 5, see Chapter 22 "Port".

19.1.1. Features

- Master function (Multi-master, stretch is not supported)
- Communication speeds supported include standard mode (100kbps) and fast mode (400kbps).
- 7 bit address format (10 bit address can be supported)

19.1.2. Configuration

Figure 19-1 shows the configuration of the I²C bus interface.



I2C1RD : I²C bus 1 receive data register
I2C1SA : I²C bus 1 slave address register
I2C1TD : I²C bus 1 transmit data register
I2C1CON : I²C bus 1 control register
I2C1MOD : I²C bus 1 mode register
I2C1STAT : I²C bus 1 status register

Figure 19-1 Configuration of I²C Bus Interface

19.1.3. List of Pins

Pin name	I/O	Function
SDA1	I/O	I²C bus interface data I/O pin
SCL1	I/O	I²C bus interface clock I/O pin

19.2. Description of Registers

19.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4100_2000	I²C bus 1 receive data register	I2C1RD	R	32	0x0000_0000
0x4100_2004	I²C bus 1 slave address register	I2C1SA	R/W	32	0x0000_0000
0x4100_2008	I²C bus 1 transmit data register	I2C1TD	R/W	32	0x0000_0000
0x4100_200C	I²C bus 1 control register	I2C1CON	R/W	32	0x0000_0000
0x4100_2010	I²C bus 1 mode register	I2C1MOD	R/W	32	0x0000_0000
0x4100_2014	I²C bus 1 status register	I2C1STA	R	32	0x0000_0000

19.2.2. I²C Bus 1 Receive Data Register (I2C1RD)

Address: 0x4100_2000
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	I21R[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2C1RD is a read-only special function register (SFR) to store the received data.
I2C1RD is updated after completion of each reception.

[Description of Bits]

- **I21R[7:0]** (bit 7 to 0)
  The I21R[7:0] bit are used to store the received data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

19.2.3. I²C Bus 1 Slave Address Register (I2C1SA)

Address: 0x4100_2004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	I21A[6:0]							I21RW
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2C1SA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

[Description of Bits]

- **I21RW** (bit 0)
  The I21RW bit is used to select the data transmit mode (write) or data receive mode (read).

I21RW	Description
0	Data transmit mode (initial value)
1	Data receive mode

- **I21A[6:0]** (bit 7 to 1)
  The I21A[6:0] bits are used to set the address of the communication partner.

19.2.4. I²C Bus 1 Transmit Data Register (I2C1TD)

Address: 0x4100_2008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	I21T[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2C1TD is a special function register (SFR) used to set the transmitted data.

[Description of Bits]

- **I21T[7:0]** (bit 7 to 0)
  The I21T[7:0] bits are used to set the transmit data.

19.2.5. I²C Bus 1 Control Register (I2C1CON)

Address: 0x4100_200C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	I21ACT	–*	–*	–*	–*	I21RS	I21SP	I21ST
Access	–	–	–	–	–	–	–	–	R/W	–	–	–	–	W	W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2C1CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

- **I21ST** (bit 0)
  The I21ST bit is used to control the communication operation of the I²C bus interface. When the I21ST bit is set to "1", communication starts. When "1" is overwritten to the I21ST bit in a control register setting wait state after transmission/reception of acknowledgment, communication restarts. When the I21ST bit is set to "0", communication is stopped forcibly.
  The I21ST bit can be set to "1" only when the I²C bus interface is in an operation enable state (I21EN = "1").When the I21SP bit is set to "1", the I21ST bit is set to "0".

I21ST	Description
0	Stops communication (initial value)
1	Start communication

- **I21SP** (bit 1)
  The I21SP bit is a write-only bit used to request a stop condition. When the I21SP bit is set to "1", the bus shifts to the stop condition and communication stops. When the I21SP bit is read, "0" is always read.

I21SP	Description
0	No stop condition request (initial value)
1	Stop condition request

- **I21RS** (bit 2)
  The I21RS bit is a write-only bit used to request a restart. When this bit is set to "1" during data communication, the I²C bus shifts to the restart condition and communication restarts from the slave address. I21RS can be set to "1" only while communication is active (I21ST ="1"). When the I21RS bit is read, "0" is always read.

I21RS	Description
0	No restart request (initial value)
1	Restart request

- **I21ACT** (bit 7)
  The I21ACT bit is used to set the acknowledge signal to be output at completion of reception.

I21ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

19.2.6. I²C Bus 1 Mode Register (I2C1MOD)

Address: 0x4100_2010
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	I21DW[1:0]		I21MD	I21EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2C1MOD is a special function register (SFR) used to set the operation mode.

[Description of Bits]

- **I21EN** (bit 0)
  The I21EN bit is used to enable the operation of the I²C bus interface. Only when I21EN is "1", the I21ST bit can be set and the I2C1 bus becomes available. When I21EN is set to "0", all the SFRs related to I²C bus 1 are initialized.

I21EN	Description
0	Stops I²C operation (initial value)
1	Enables I²C operation

- **I21MD** (bit 1)
  The I21MD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected.

I21MD	Description
0	Standard mode (initial value)/100 kbps
1	Fast mode/400 kbps

- **I21DW[1:0]** (bit 3 to 2)
  The I21DW[1:0] bits are used to set the communication speed reduction rate of the I²C bus interface. Set this bit so that the communication speed does not exceed 100kbps/400kbps.

I21DW[1]	I21DW[0]	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

19.2.7. I²C Bus 1 Status Register (I2C1STAT)

Address: 0x4100_2014
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	I21ER	I21ACR	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2C1STAT is a read-only special function register (SFR) to indicate the state of the I²C bus interface.

[Description of Bits]

- **I21ACR** (bit 1)
  The I21ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I21ACR bit is set to "0" when the I21EN bit of I2C1MOD is "0".

I21ACR	Description
0	Receives acknowledgment "0" (initial value)
1	Receives acknowledgment "1"

- **I21ER** (bit 2)
  The I21ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". The SDA pin output continues until the subsequent byte data communication terminates, even if the I21ER bit is set to "1".
  The I21ER bit is set to "0" when a write operation to I2C1CON is performed. The I21ER bit is set to "0" when the I21EN bit of I2C1MOD is set to "0".

I21ER	Description
0	No transmit error (initial value)
1	Transmit error

19.3. Description of Operation

19.3.1. Communication Operation Mode

Communication is started when communication mode is selected by using the I²C bus n mode register (I2C1MOD), the I²C function is enabled by using the I21EN bit, a slave address and a data communication direction are set in the I²C bus n slave address register (I2C1SA), and "1" is written to the I21ST bit of the I²C bus n control register (I2C1CON).

19.3.1.1. Start Condition

When "1" is written to the I21ST bit of the I²C bus n control register (I2C1CON) while communication is stopped (the I21ST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to the slave address transmit mode.

19.3.1.2. Restart Condition

When "1" is written to the I21RS and I2nST bit of the I²C bus n control register (I2C1CON) during communication (the I21ST bit is "0"), the restart condition waveform is output to the SDA and SCL pins.
After execution of the restart condition, the LSI shifts to the slave address transmit mode.

19.3.1.3. Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I²C bus n slave address register (I2C1SA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I21ACR bit of the I²C bus n status register (I2C1STAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus n control register (I2C1CON) setting wait state (control register setting wait state).
The value of I2C1SA output from the SDA pin is stored in I2C1RD.

19.3.1.4. Data Transmit Mode

In data transmit mode, the value of I2C1TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I21ACR bit of the I²C bus n status register (I2C1STAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus n control register (I2C1CON) setting wait state (control register setting wait state).
The value of I2C1TD output from the SDA pin is stored in I2C1RD.

19.3.1.5. Data receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I21ACT bit of the I²C bus n control register (I2C1CON) is output.
At completion of acknowledgment transmission, the LSI shifts to the I²C bus n control register (I2C1CON) setting wait state (control register setting wait state).
The data received is stored in I2C1RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I21ACR bit of the I²C bus n status register (I2C1STAT).

19.3.1.6. Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I²C bus n interface interrupt (I2C1INT) is generated.
In the control register setting wait state, the transmit error flag (I21ER) of the I²C bus n status register (I2C1STAT) and acknowledgment receive data (I21ACR) are confirmed and at data reception, the contents of I2C1RD are read in the CPU and the next operation mode is selected.
When "1" is written to the I21ST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I21SP bit, the LSI shifts to the stop condition. When "1" is written to the I21RS bit, the LSI shifts to the restart condition.

19.3.1.7. Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I²C bus n interface interrupt (I2C1INT) is generated.

19.3.2. Communication Operation Timing

Figures 19-2 to 19-4 show the operation timing and control method for each communication mode.

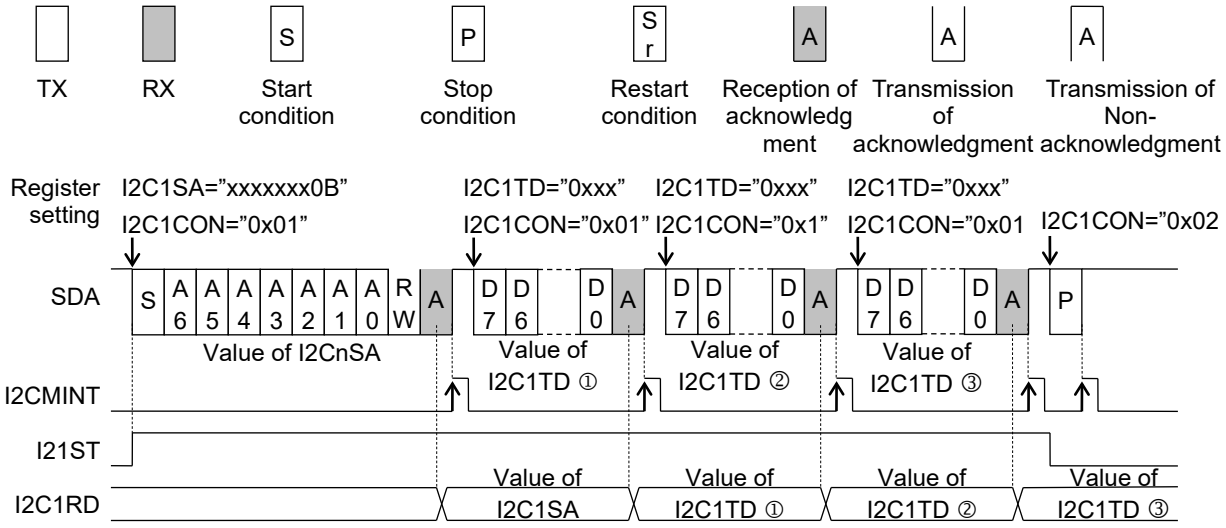


Figure 19-2 Operation Timing in Data Transmit Mode (Write)

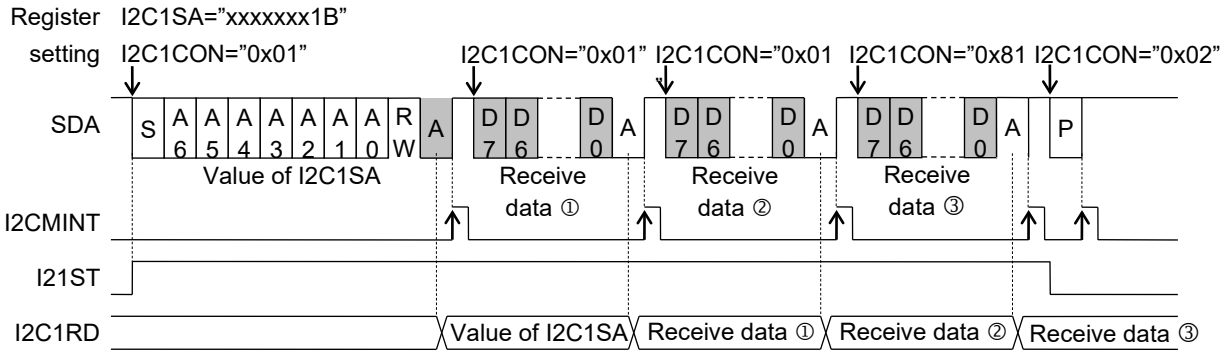


Figure 19-3 Operation Timing in Data Receive Mode (Read)

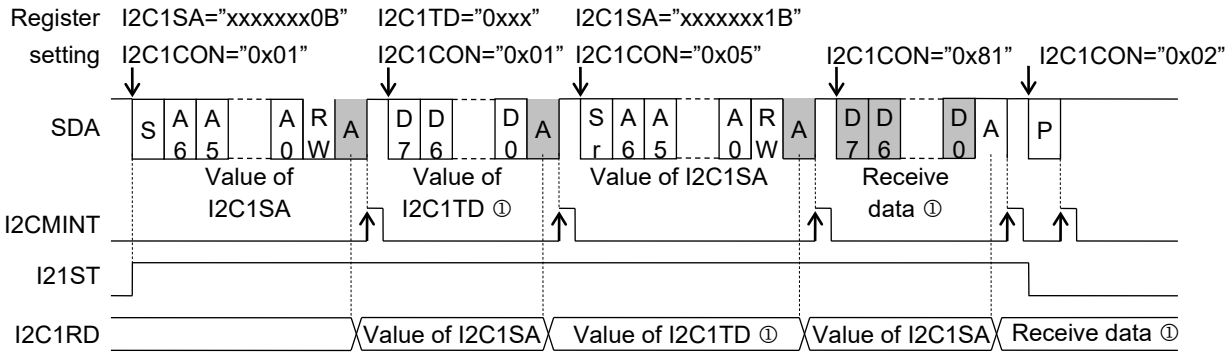


Figure 19-4 Operation Timing at Data Transmit/Receive Mode (Write/Read) Switching

Figure 19-5 shows the operation timing and control method when an acknowledgment error occurs.

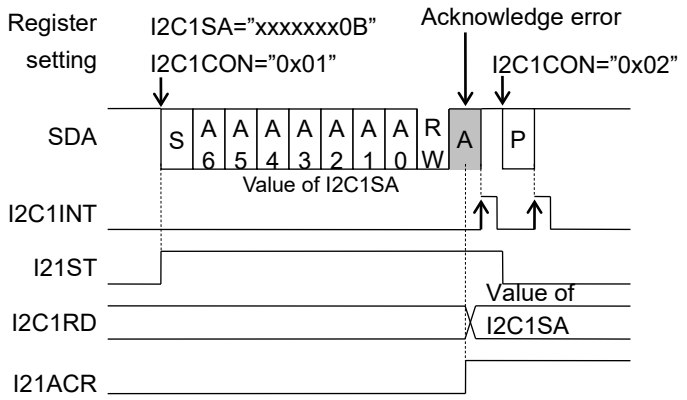


Figure 19-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide, the I21ER bit of the I²C bus n status register (I2C1STAT) is set to "1" and the SDA pin output is disabled until termination of the subsequent byte data communication.
Figure 19-6 shows the operation timing and control method when transmission fails.

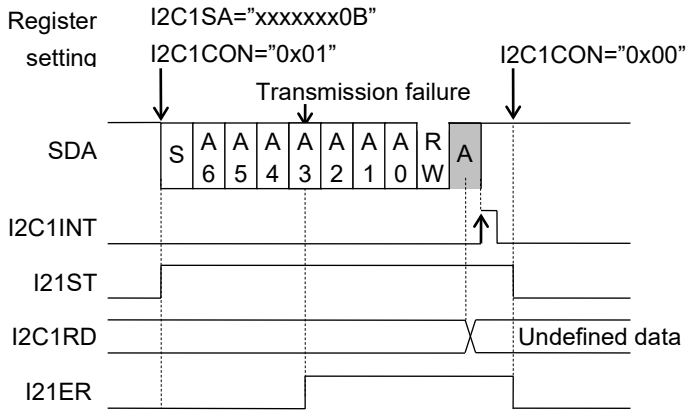


Figure 19-6 Operation Timing When Transmission Fails

19.3.3. Operation Waveforms

Figure 19-7 shows the operation waveforms of the SDA and SCL signals. Table 19-2 shows the relationship between communication speeds and 4MHz clock counts.

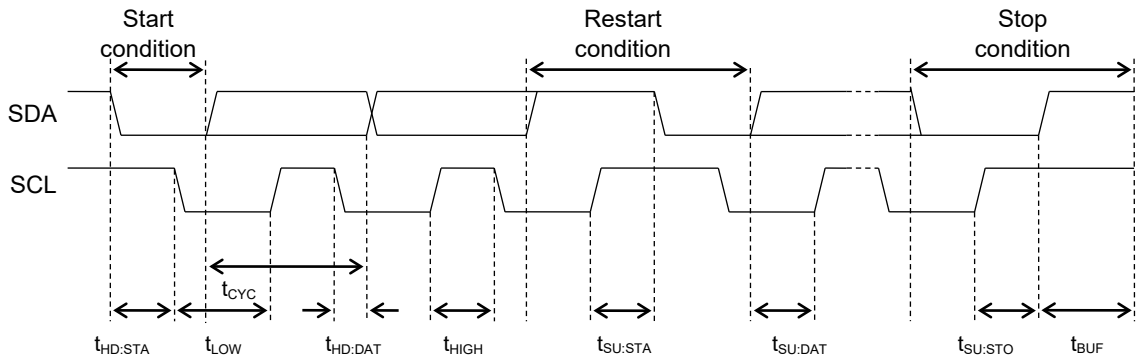


Figure 19-7 Operation Waveforms of SDA and SCL Signals

Table 19-2 Relationship between Communication Speeds and 4MHz Clock Counts

Communication speed (I21SP)	Speed reduction (I21DW[1:0])	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100kbps	No reduction	40φ	18φ	22φ	4φ	18φ	22φ	18φ	18φ	22φ
	10% reduction	44φ	20φ	24φ	4φ	20φ	24φ	20φ	20φ	24φ
	20% reduction	48φ	22φ	26φ	4φ	22φ	26φ	22φ	22φ	26φ
	30% reduction	52φ	24φ	28φ	4φ	24φ	28φ	24φ	24φ	28φ
Fast mode 400kbps	No reduction	10φ	4φ	6φ	2φ	4φ	6φ	4φ	4φ	6φ
	10% reduction	11φ	4φ	7φ	2φ	4φ	7φ	5φ	4φ	7φ
	20% reduction	12φ	5φ	7φ	2φ	5φ	7φ	5φ	5φ	7φ
	30% reduction	13φ	5φ	8φ	2φ	5φ	8φ	6φ	5φ	8φ

φ: Clock cycle of 4MHz

19.3.4. Pin Settings

To enable the I²C function, the applicable bit of each related port register needs to be set. See Chapter 22, "Port" for details about the port registers.
For SCL1 and SDA1, the ports can be selected from several possibilities.
Be sure to select one of the following combinations of ports for SCL/SDA.

	I²C pin	Combination 1	Combination 2	Combination 3
I²C1	SCL1,SDA1	P35,P34	P45,P44	P55,P54

Moreover, being able to select as a port is only in one port.

Chapter 20

I^2C Bus Interface with FIFO (I2CF)

20. I²C Bus Interface with FIFO

20.1. Overview

This LSI includes one channel of I²C bus interface that conforms to the typical I²C bus specification.

20.1.1. Features

- Master / Slave function (multi-master non-correspondence)
- The communication speed is selectable with two kinds of standard-mode, fast-mode.
- The 16-byte buffer function is provided.
- Generates transmission/receive DMA request

20.1.2. Configuration

Figure 20-1 shows the configuration diagram of the I²CF.

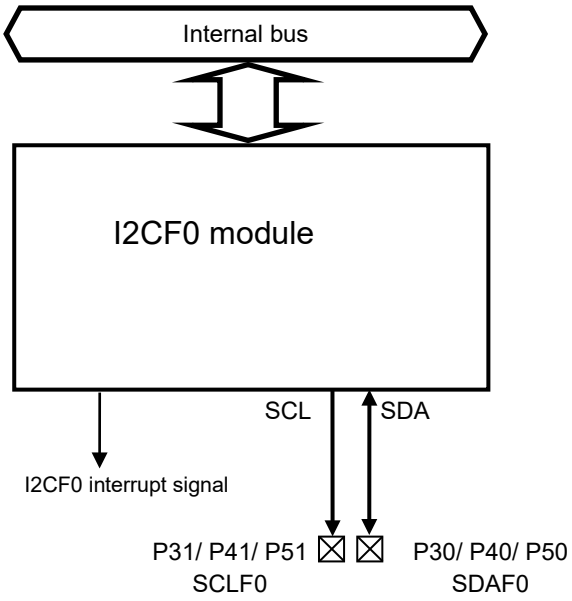


Figure 20-1 Configuration Diagram

20.1.3. List of Pins

Table 20-1 List of Pins Interfaced with the Outside of LSI

Pin name	I/O	Description
SDAF0	I/O	Serial data input/output pin
SCLF0	I/O	Serial data transfer clock

20.2. Description of Registers

20.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4100_2800	I²CF0 slave address register	I2F0SAD	R/W	32	0x0000_0000
0x4100_2804	I²CF0 control register	I2F0CTL	R/W	32	0x0000_0000
0x4100_2808	I²CF0 status register	I2F0SR	R/W	32	0x0000_0000
0x4100_280C	I²CF0 data register	I2F0DR	R/W	32	0x0000_0000
0x4100_2810	I²CF0 bus monitor register	I2F0MON	R	32	0x0000_0003
0x4100_2814	I²CF0 bus transfer rate setup counter	I2F0BC	R/W	32	0x0000_0000
0x4100_2818	I²CF0 mode register	I2F0MOD	R/W	32	0x0000_0000
0x4100_281C	I²CF0 buffer mode slave address register	I2F0BSV	R/W	32	0x0000_0000
0x4100_2820	I²CF0 buffer mode sub address register	I2F0BSB	R/W	32	0x0000_0000
0x4100_2824	I²CF0 buffer mode format register	I2F0BFR	R/W	32	0x0000_0000
0x4100_2828	I²CF0 buffer mode control register	I2F0BCT	R/W	32	0x0000_0000
0x4100_282C	I²CF0 buffer mode interrupt mask register	I2F0BMK	R/W	32	0x0000_0000
0x4100_2830	I²CF0 buffer mode status register	I2F0BSR	R/W	32	0x0000_0000
0x4100_2834	I²CF0 buffer mode level register	I2F0BLV	R/W	32	0x0000_0000
0x4100_2848	I²CF0 timer register	I2F0TMR	R/W	32	0x0000_0000
0x4100_2850	I²CF0 input noise filter setting register	I2F0NF	R/W	32	0x0000_0001

[Note]
These registers are written with system clock is high-speed clock only.

20.2.2. I²C Slave Address Register (I2F0SAD)

Address: 0x4100_2800
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	I2F0SA[10:1]										–*
Access	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0SAD is a special function register (SFR) to set the slave address.

[Description of Bits]

- **I2F0SA[10:1]** (bit 10 to 1)
  The I2F0SA[10:1] bits are used for the slave address in the I²C slave communication. I2F0SA[7:1] bits are needed to set the 7 bit slave address, and I2F0SA[10:8] bits are needed to set to “0”

20.2.3. I²C Control Register (I2F0CTL)

Address: 0x4100_2804
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	I2F0CS	I2F0DLEN	I2F0STPI	_*	I2F0CFIE	_*	I2F0MEN	I2F0ASIE	I2F0MSTA	I2F0MTX	I2F0TXAK	I2F0RSTA	I2F0MD[1:0]	
Access	–	–	R/W	R/W	R/W	–	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0CTL is a register controlling the transmission and reception of the I2C bus. About each interrupt permission register of I2F0ASIE, I2F0CFIE, I2F0STPI, I2F0DLEN, control only an interrupt and do not control bit to support of the status register. (even in the case of interrupt disable, the status register changes).
Use only I2F0MD, I2F0MEN bit in the buffer mode setting.

[Description of Bits]

- **I2F0MD[1:0]** (bit 1 to 0)
  Select the standard-mode or the fast-mode.

I2F0MD[1:0]	Description
00	Selects the standard-mode (100 kHz).
01	Selects the fast-mode (400 kHz).
10	Setting prohibited
11	Setting prohibited

- **I2F0RSTA** (bit 2)
  Specifies to transmit the repeated START condition. When the I²CF module writes in "1" during communication in masters, send out repeated START condition to the bus. This bit is automatically reset to "0" after sending a repeated START condition.

[Note]
When sending a repeated START condition, overwrite I2F0MSTA as is with the setting of "1". Operation cannot be guaranteed if "1" is written to this bit I2F0RSTA and "0" to the I2F0MSTA bit. Because this bit is automatically reset to "0" after sending the repeated START condition, if another bit in the control register will be set after this bit is set to "1", set this bit to "0" or keep the previous value. If "1" is written again, the repeated START condition will be sent at that moment.

- **I2F0TXAK** (bit 3)
  Specifies transmission of ACK or NACK in the receive mode. The acknowledge data that was set to this bit in advance is sent to the transmit device after data is received. But, about the ACK reply after the header data reception in the slave mode, not precocious by this setting. Return NACK at the time of the slave address disagreement, and return ACK at the time of slave address agreement or non-decision.

I2F0TXAK	Description
0	At acknowledge output timing, outputs “0”. ACK output
1	At acknowledge output timing, outputs “1”. NACK output

- **I2F0MTX** (bit 4)
  Selects the data transfer direction.

I2F0MTX	Description
0	Received by master.
1	Transmitted by master.

- **I2F0MSTA** (bit 5)
  Specifies to transmit a START condition or a STOP condition. If this bit is rewritten from “0” to “1”, a start sequence is sent to the bus. When this bit is cleared, a stop sequence is sent, and switch to slave mode.

I2F0MSTA	Description
0	Sends a STOP condition.
1	Sends a START condition.

- **I2F0ASIE** (bit 6)
  Specifies to enable or disable an MAAS interrupt. The I2F0MAAS status will change even if an interrupt is disabled by this bit.

I2F0ASIE	Description
0	Disables MAAS interrupt.
1	Enables MAAS interrupt.

- **I2F0MEN** (bit 7)
  Specifies to initialize this I²C module. Set this bit to “1” when using this I²C module.

I2F0MEN	Description
0	Initializes this I²C module
1	Enables this I²C module.

[Note]
If the I2F0MEN bit is set to “0”, the I²C bus control section, I²C status register (including the I2F0MBB bit), I²C buffer level register, and I²C buffer mode status register will be initialized.
The I²C buffer mode format register, I²C control register, I²C data register, I²C bus monitor register, I²C bus transfer rate setup counter, I²C mode register, I²C buffer mode slave address register, I²C buffer mode sub address register, I²C buffer mode control register, I²C buffer mode interrupt mask register, I²C timer register and I²C input noise filter setting register will not be initialized.

- **I2F0CFIE** (bit 9)

Specifies to enable or disable an MCF interrupt. The I2C0MCF status will change even if an interrupt is disabled by this bit.

I2F0CFIE	Description
0	Disables MCF interrupt.
1	Enables MCF interrupt.

- **I2F0STPI** (bit 11)

Specifies to enable or disable an STP interrupt. The I2F0STP status will change even if an interrupt is disabled by this bit.

I2F0STPI	Description
0	Disables STP interrupt.
1	Enables STP interrupt.

- **I2F0DLEN** (bit 12)

Specifies to enable or disable a DR_LD interrupt. The I2F0DRLD status will change even if an interrupt is disabled by this bit.

I2F0DLEN	Description
0	Disables DR_LD interrupt.
1	Enables DR_LD interrupt.

- **I2F0CS** (bit 13)

Specifies to halt SCL. SCL stops subsequently to an MCF interrupt that is generated after this bit is set to "1". When inserting a repeated start after executing the transmit mode, set this bit to "1" during a 1-byte data transfer period immediately before the insertion. After the completion of the transfer, set the I2F0RSTA bit to "1" and, at the same time, clear this bit. Specifies to enable or disable an STP interrupt. The I2F0STP status will change even if an interrupt is disabled by this bit.

I2F0CS	Description
0	Continues SCL output.
1	Stops SCL output upon completion of the next transfer.

20.2.4. I²C Status Register (I2F0SR)

Address: 0x4100_2808
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	I2F0STP	–*	I2F0MCF	I2F0MAAS	I2F0MBB	–*	I2F0DRLD	I2F0SRW	I2F0MIF	I2F0RXAK
Access	–	–	–	–	–	–	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0SR is a register indicating the status of the I2C bus.
About each bit except I2F0RXAK, I2F0SRW, I2F0MBB, cleared by writing in “0”. In addition, use only I2F0MBB bit in the buffer mode setting.

[Description of Bits]

- **I2F0RXAK** (bit 0)
  I2F0RXAK bit indicates the reception status of ACK/NACK. Acknowledge data to be replied by the receiving device in the transmit mode is stored. This bit is updated every time ACK/NACK is received, and this bit holds the acknowledge data received last even after the bus is released. In the transmit mode, check this bit at the time of an MCF interrupt. If a NACK is received, finish the transfer.

I2F0RXAK	Description
0	Received an ACK.
1	Received a NACK.

- **I2F0MIF** (bit 1)
  I2F0MIF bit indicates that an interrupt has been requested. This bit is an interrupt line monitoring bit. If interrupt is enabled for MCF interrupt, MAAS interrupt, DR_LD interrupt and STP interrupt, this bit is set to “1” at the same time that the bit (I2F0MCF, I2F0DRLD, I2F0STP, and I2F0MAAS) for each interrupt source is set to “1”.

I2CMIF	Description
0	No interrupt request
1	Interrupt request

[Note]
Whether or not to enable each interrupt is set by the I2F0CTL register. For details, refer to "20.2.3 I²C Control Register (I2F0CTL)".

- **I2F0SRW** (bit 2)
  This bit indicates whether the access type from the master device is "read" or "write" during the slave mode. This bit is updated at getting R/W bit in the address data. (R/W bit is the last bit of the address data)

I2F0SRW	Description
0	Write type: master device transmits to slave device
1	Read type: mater device receives from slave device

- **I2F0DRLD** (bit 3)
  This bit indicates that the transmit buffer is emptied and transmit data can be loaded to the I2F0DR register. After this bit has been set to "1" in the transmit mode, the data to be sent next can be written into the data register without destroying the previously transmitted data. This bit is cleared by writing "0" by software. This bit is set to "1" when the transfer of 2 bit out of 8 bit transmit data is finished (at a falling edge of SCL). By using this bit (interrupt), transmit data can be written before an MCF interrupt.

I2F0DRLD	Description
0	Data load to the data register is not allowed.
1	Data load to the data register is allowed.

- **I2F0MBB** (bit 5)
  This bit indicates the status of the I²C bus. This bit is set to "1" when a START condition is detected; this bit is reset to "0" when a STOP condition is detected. By reading this bit, it is possible to check whether the bus is currently occupied or released. This bit is set to "1" after a START condition is detected (at a falling edge of SCL after SDA changes from "1" to "0" when SCL is "1"), and is set to "0" after a STOP condition is detected (at a rising edge of SDA when SCL is "1").

I2F0MBB	Description
0	The I²C bus is open.
1	The I²C bus is occupied.

[Note]
Before starting a master transmit or master receive transfer, read this bit and make sure that the bus is open.

- **I2F0MAAS** (bit 6)
  This bit indicates whether the external master device specifies this MCU as their slave device or not. This bit is set to 1 when the slave address in the I2F0SAD register is matched to the slave address from the external master device. To clear this bit, the software writes "0" in this bit.
  This bit becomes "1" with the MCF interrupt that the transfer of address data completed.
  It becomes "1" after 2Byte transfer in the 10bit address after 1Byte transfer in the 7bit address.

I2F0MAAS	Description
0	The external master device doesn't specifyas the slave device.
1	The external master device specifies as the slave device.

- **I2F0MCF** (bit 7)
  This bit indicates that data transfer has been completed. This bit is set to "1" when the transmission/reception of 1-byte data(*1) is completed.
  This bit is cleared by writing "0" by software. This bit is set to "1" at a rising edge of SCL when a 1-byte transfer is complete and an ACK response is started.

  (*1) The data signifies all of the 1-byte transfer, which includes the transfer of an address immediately after start/repeated start that the master transmits.

I2CMCF	Description
0	Before data transfer start or during data transfer.
1	Data transfer is completed.

[Note]
In the receive mode, clear this bit by writing "0" to it after reading the receive data from the I2CDR register. If any data is left in the receive buffer, this bit cannot be cleared even if "0" is written to it.

- **I2F0STP** (bit 9)
  This bit indicates that data reception is completed in the receive mode. The completion of data reception is fixed by receiving the STOP condition or the repeated START condition in the compound mode from the master device.
  This bit is cleared by writing "0" by software. This bit is set to "1" when STOP condition is detected, or when the slave address is mismatched after the repeated START condition.

I2F0STP	Description
0	Data reception is not completed in the slave mode.
1	Data reception is completed in the slave mode.

[Note]
This bit is valid only at data reception in the slave mode.

20.2.5. I²C Data Register (I2F0DR)

Address: 0x4100_280C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	I2F0DA[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0DR is a register setting the transmit data or indicating received data.

[Description of Bits]

- I2F0DA[7:0] (bit 7 to 0)

I2F0DA[7:0] set transmit data or indicate received data. In the buffer mode, up to 16 bytes of transmit data can be stored in the buffer by writing this register. When receiving data, the received data stored in the buffer can be read by reading this register.

20.2.6. I²C Bus Monitor Register (I2F0MON)

Address: 0x4100_2810
Access: R
Access size: 32 bit
Initial value: 0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	I2F0SDA	I2F0SCL
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0MON is a register expressing a level of SDA,SCL of the I2C bus.

[Description of Bits]

- **I2F0SCL** (bit 0)

Monitors the level of the SCL line.

- **I2F0SDA** (bit 1)

Monitors the level of the SDA line.

20.2.7. I²C Bus Transfer Rate Setup Counter (I2F0BC)

Address: 0x4100_2814
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0BC[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BC is a register setting a count level for a counter generating the transfer timing of the I2C bus from system clock. Use it for SCL/SDA generation in a master mode, but please usually set it by all means because you use the verge of the slave transmission to find data set up time at the time of resumption from SCL clock stop. Therefore, perform this setting by all means.

[Description of Bits]

- **I2F0BC[6:0]** (bit 6-0)

The relationship between the setting value of I2CBC and the transfer rate of the I²C bus is as follows:

I²C bus transfer rate [bps] = System clock frequency / (I2F0BC setting value × 8)

Therefore,

I2F0BC = System clock frequency / (I²C bus transfer rate [bps] × 8)

Calculate the system clock frequency with the value that added a frequency error.
The following table gives examples of setting values:

System clock frequency	I2F0BC	
	Standard Mode 100 kbps (I2F0MD = “00”)	Fast Mode 400 kbps (I2F0MD = “01”)
24MHz	0x1E Ref. Rate: around 98kbps	0x08 Ref. Rate: around 348kbps
16MHz	0x15 Ref. Rate: around 97kbps	0x06 Ref. Rate: around 317kbps
12MHz	0x0F Ref. Rate: around 96kbps	0x04 Ref. Rate: around 324kbps
8MHz	0x0B Ref. Rate: around 92kbps	0x03 Ref. Rate: around 311kbps
6MHz	0x08 Ref. Rate: around 87kbps	0x03(*) Ref. Rate: around 207kbps
4MHz	0x06 Ref. Rate: around 84kbps	0x03(*) Ref. Rate: around 162kbps
3MHz	0x04 Ref. Rate: around 81kbps	Setting prohibited
2MHz	0x03 Ref. Rate: around 84kbps	Setting prohibited

If “0” is set in the I2F0BC register, the timing generation counter stops.

In fast-mode, system clock does not work by the calculation mentioned above at 6 or 4MHz. Set the value of the table.
In addition, the reference speed is an aim. Changes by an outside condition.

[Note]
- In Standard-mode, set the system clock in 24 / 16 / 12 / 8 / 6 / 4 / 3 / 2MHz.
- In Fast-mode, set the system clock in 24 / 16 / 12 / 8 / 6 / 4MHz.
- Set the I2F0BC register before setting the I2F0CTL register.
- Can't communicate the I^2C master that does not confirm the input state, because SCL is low for satisfying the data setup time at transmitting of the slave mode.

20.2.8. I²C Mode Register (I2F0MOD)

Address: 0x4100_2818
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0BMEN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0MOD is a register choosing buffer mode use / not use for master transfer (the master transmission and the master reception).

[Description of Bits]

- **I2F0BMEN** (bit 0)
  Set this bit to "1" to use I²C in the buffer mode.

I2F0BMEN	Description
0	Buffer mode is not used
1	Buffer mode is used

[Note]

- Set this register in the initial setting flow or before the master transfer start. Operation cannot be guaranteed if the value of this register is changed during transfer.
- During buffer mode setting, cannot use the slave function. Even if other master devices send out a slave address, this I2CF module returns NACK and is not appointed to a slave device.

20.2.9. I²C Buffer Mode Slave Address Register (I2F0BSV)

Address: 0x4100_281C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	I2F0BA[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BSV is a register setting the slave address of the forwarding address device. In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BA[15:0]** (bit 15-0)
  Set the slave address of the transfer destination device.
  Set I2F0BA[7:1] to 7 bit address. Set I2F0BA[15:8] and [0] to "0".

	7	6	5	4	3	2	1	0
I2F0BSVL	A7	A6	A5	A4	A3	A2	A1	“0”

	15	14	13	12	11	10	9	8
I2F0BSVH	“0”	“0”	“0”	“0”	“0”	“0”	“0”	“0”

[Note]
Set this bit in the initial setting flow or before the master transfer start.
Operation cannot be guaranteed if the value of this bit is changed during transfer.

20.2.10. I²C Buffer Mode Sub Address Register (I2F0BSB)

Address: 0x4100_2820
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	I2F0BS1[7:0]								I2F0BS0[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BSB is a register setting a subaddress to transmit to a forwarding address device. In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BS0[**7:0] (bit 7-0)
  This register sets the sub address 0 sent to the transfer destination device.

- **I2F0BS1[**7:0] (bit 15-8)
  This register sets the sub address 1 sent to the transfer destination device.

  When the value set for I2F0BSL[1:0] of the I2F0BFR register is “00”, the setting value of this register is disabled, and the sub address is not sent.
  When the setting value of I2F0BSL[1:0] is “01”, the data in I2F0BS0 is sent to the I²C bus.
  When the setting value of I2F0BSL[1:0] is “10”, the data in I2F0BS1 and I2F0BS0 is sent to the I²C bus in this order.

  [Note]
  Set this bit in the initial setting flow or before the master transfer start.
  Operation cannot be guaranteed if the value of this bit is changed during transfer.

20.2.11. I²C Buffer Mode Format Register (I2F0BFR)

Address: 0x4100_2824
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	I2F0BDL[4:0]					–*	–*	–*	–*	I2F0BMRW	–*	I2F0BSL[1:0]	
Access	–	–	–	R/W	R/W	R/W	R/W	R/W	–	–	–	–	R/W	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BFR is a register setting the communication format in the buffer mode. Set the data head of the subaddress to transmit, the transfer direction of data, the number of bytes of data to transfer. In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BSL[1:0]** (bit 1-0)
  These bit indicate the data length of the transferred sub address in the buffer mode. “00” to “10” can be set.
  When it is set to “00”, the sub address is not sent.
  When it is set to “01” or “10”, the sub address of the I2F0BS register is sent.
  When these bit are set to more than “11”, it will be set to “00”.

- **I2F0BMRW** (bit 3)
  This bit indicates the data transfer direction in the buffer mode.
  “1” and “0” show data reception and data transmission respectively.

- **I2F0BDL[4:0]** (bit 12-8)
  This register sets the transferred byte count in the buffer mode. 0 to 16 bytes (“0000” to “10000”) can be set. When these bit are set to more than “10001”, it will be set to “00000”. When starting transfer with these bit set to “00000”, I2F0BMDZ will be set to 1, and transfer will not be started.

[Note]
Set this bit in the initial setting flow or before the master transfer start.
Operation cannot be guaranteed if the value of this bit is changed during transfer.

20.2.12. I²C Buffer Mode Control Register (I2F0BCT)

Address: 0x4100_2828
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0BMST
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BCT is a register appointing a start of the I2C movement in a buffer mode. In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BMST** (bit 0)
  This bit indicates starting the transfer in the buffer mode.
  Before the transfer, it is necessary to set the I2C0BSV, I2C0BSB, I2C0BFR, I2C0BMK, and I2C0TMR registers, and to write the transmit data to the buffer. And then the transfer starts when setting this bit to "1". This bit will be cleared to "0" after starting transfer when the transfer of the specified bytes is finished, or transfer is stopped due to errors such as NACK reception, unexpected STOP condition, and timeout.
  If the number of transferred bytes is different from the value of the buffer mode level register, the transmission does not start. This bit will be cleared to "0", and an I2F0BMAG interrupt will occur. If the number of transferred bytes is "0", the transmission and reception does not start. This bit will be cleared to "0", and an I2F0BMDZ interrupt will occur.

I2F0BMST	Description
0	Transfer in the I²C buffer mode is stopped
1	Transfer in the I²C buffer mode is started

20.2.13. I²C Buffer Mode Interrupt Mask Register (I2F0BMK)

Address: 0x4100_282C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0BDIE	I2F0BAIE	I2F0BSIE	I2F0BTIE	I2F0BNIE	–*	I2F0BFIE
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BMSK is a register controlling each interrupt signal in the buffer mode. Do not control the bit to support of the status register. (in the case of the interrupt suppression, the status register changes.)
In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BFIE** (bit 0)
  Specifies to enable or disable an I2F0BMFI interrupt.
  The I2F0BMFI status will change even if an interrupt is disabled by this bit.

I2F0BFIE	Description
0	Disables I2F0BMFT interrupt.
1	Enables I2F0BMFT I interrupt.

- **I2F0BNIE** (bit 2)
  Specifies to enable or disable an I2F0BMNA interrupt.
  The I2F0BMNA status will change even if an interrupt is disabled by this bit.

I2F0BNIE	Description
0	Disables I2F0BMNA interrupt.
1	Enables I2F0BMNA interrupt.

- **I2F0BTIE** (bit 3)
  Specifies to enable or disable an I2F0BMTO interrupt.
  The I2F0BMTO status will change even if an interrupt is disabled by this bit.

I2F0BTIE	Description
0	Disables I2F0BMTO interrupt.
1	Enables I2F0BMTO interrupt.

- **I2F0BSIE** (bit 4)
  Specifies to enable or disable an I2F0BMIS interrupt.
  The I2F0BMIS status will change even if an interrupt is disabled by this bit.

I2F0BSIE	Description
0	Disables I2F0BMIS interrupt.
1	Enables I2F0BMIS interrupt.

- **I2F0BAIE** (bit 5)
  Specifies to enable or disable an I2F0BMAG interrupt.
  The I2F0BMAG status will change even if an interrupt is disabled by this bit.

I2F0BAIE	Description
0	Disables I2F0BMAG interrupt.
1	Enables I2F0BMAG interrupt.

- **I2F0BDIE** (bit 6)
  Specifies to enable or disable an I2F0BMDZ interrupt.
  The I2F0BMDZ status will change even if an interrupt is disabled by this bit.

I2F0BDIE	Description
0	Disables I2F0BMDZ interrupt.
1	Enables I2F0BMDZ interrupt.

[Note]
Set this bit in the initial setting flow or before the master transfer start.
Operation cannot be guaranteed if the value of this bit is changed during transfer.

20.2.14. I²C Buffer Mode Status Register (I2F0BSR)

Address: 0x4100_2830
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0BMDZ	I2F0BMAG	I2F0BMIS	I2F0BMTO	I2F0BMNA	–*	I2F0BMFI
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0BSR register is a register indicating each status in the buffer mode. About each bit, cleared by writing in "0". In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BMFI** (bit 0)
  It is set to "1" when this I²C module finishes the transfer in the buffer mode.
  This bit is cleared by writing "0" by software.

I2F0BMFI	Description
0	Transfer in the buffer mode is not completed
1	Transfer in the buffer mode is completed

- **I2F0BMNA** (bit 2)
  It is set to "1" when it receives a NACK and the transfer is finished.
  This bit is cleared by writing "0" by software.

I2F0BMNA	Description
0	Has not received a NACK.
1	Received a NACK and terminated transfer.

- **I2F0BMTO** (bit 3)
  It is set to "1" when a timeout occurs before the end of the transfer, and the transfer ends abnormally. For example, when SCL prolonging by the slave device is not terminated in a certain time, this bit is set to "1".
  This bit is cleared by writing "0" by software.

I2F0BMTO	Description
0	Timeout has not occurred
1	Timeout has occurred

- **I2F0BMIS** (bit 4)
  This bit is set to "1" if a STOP condition occurs at unexpected timing, and the transfer ends abnormally. This bit is set to "1" if a STOP condition is detected before this I²C device transmits a STOP condition during a transfer in the buffer mode.
  This bit is cleared by writing "0" by software.

I2F0BMIS	Description
0	Has not detected an unexpected STOP condition
1	Detected an unexpected STOP condition.

- **I2F0BMAG** (bit 5)
  This bit is set to "1" if the number of transferred bytes set in I2F0BDL and the value of I2F0BML do not match at the start of the transmission (when I2F0BMRW is set to "0" and "1" is written to I2F0BMST). In this case, the transfer is not started.
  This bit is cleared by writing "0" by software.

I2F0BMAG	Description
0	The number of transferred bytes and the buffer capacity match at the start of the transmission
1	The transmission has not been started because the number of transferred bytes and the buffer capacity do not match at the start of the transmission

- **I2F0BMDZ** (bit 6)
  This bit is set to "1" if the number of transferred bytes set in I2F0BDL is 0 at the start of the transmission (when "1" is written to I2F0BMST). In this case, the transfer is not started.
  This bit is cleared by writing "0" by software.

I2F0BMDZ	Description
0	The number of transferred bytes is not 0 at the start of transmission
1	The transmission has not been started because the number of transferred bytes is 0 at the start of transmission

20.2.15. I²C Buffer Mode Level Register (I2F0BLV)

Address: 0x4100_2834
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0BML[4:0]				
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
The I2F0BLV shows the residual quantity of the data which collected in the buffer. In addition, this register is effective only when use a buffer mode.

[Description of Bits]

- **I2F0BML[4:0]** (bit 4-0)
  These bit indicated the amount of data remaining in the buffer. The buffer size is 16-byte. The value in this register increases one-byte, when one byte is written to the I2F0DR register or one byte is received. Meanwhile, the value in this register decreases one-byte when one byte is read from the I2F0DR register or one byte is sent. The range of I2F0BML bit are 0 to 16.

[Note]
When before data transmission start of the buffer transfer, writing in “0” at Low side I2F0BLVL of this register and buffer cleared. And write in transmission data at I2F0DR register. Can collect transmission data in the buffer for 16 bytes. When before data reception start of the buffer transfer, writing in “0” at Low side I2F0BLVL of this register and buffer cleared.

.

20.2.16. I²C Timer Register (I2F0TMR)

Address: 0x4100_2848
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	I2F0T[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0TMR is a register setting distance of the time-out outbreak in the buffer mode. In addition, this register is effective only when use a buffer mode.
Set the I2F0BMTO bit of the I2F0BSR register in "1" when it takes the time that transmission and reception transfer every 1 byte takes more than a set point of the time-out in the buffer mode. When time-out occurs, the transfer is stopped.

[Description of Bits]

- **I2F0T[15:0]** (bits 15-0)

The timeout interval can be calculated from the setting value of I2F0T bit as follows:

Timeout interval = (I2F0T setting value * 8) / System clock frequency

Here are the examples of setting the timeout interval to 1ms and 8ms.

System clock frequency	I2F0T[15:0]	
	For 1ms interval	For 8ms interval
24 MHz	0x0FA0	0x5DC0
16 MHz	0x07D0	0x3E80
12 MHz	0x05DC	0x2EE0
8 MHz	0x03E8	0x1F40
6 MHz	0x02EE	0x1770
4 MHz	0x01F4	0x0FA0

When I2F0T is set to ”0”, a timeout interrupt does not occur.

[Note]
Set this bit in the initial setting flow or before the master transfer start.
Operation cannot be guaranteed if the value of this bit is changed during transfer.
Setting I2F0T to less than the time required for the transfer always results in a timeout.
One-byte transfer takes 90 μs in the standard mode (100 kbps) and 22.5 μs in the fast mode (400 kbps).

20.2.17. I²C Input Noise Filter Setting Register (I2F0NF)

Address: 0x4100_2850
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	I2F0NFON
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
I2F0NF is a register to set SCL and noise filter use / nonuse for the SDA input.

[Description of Bits]

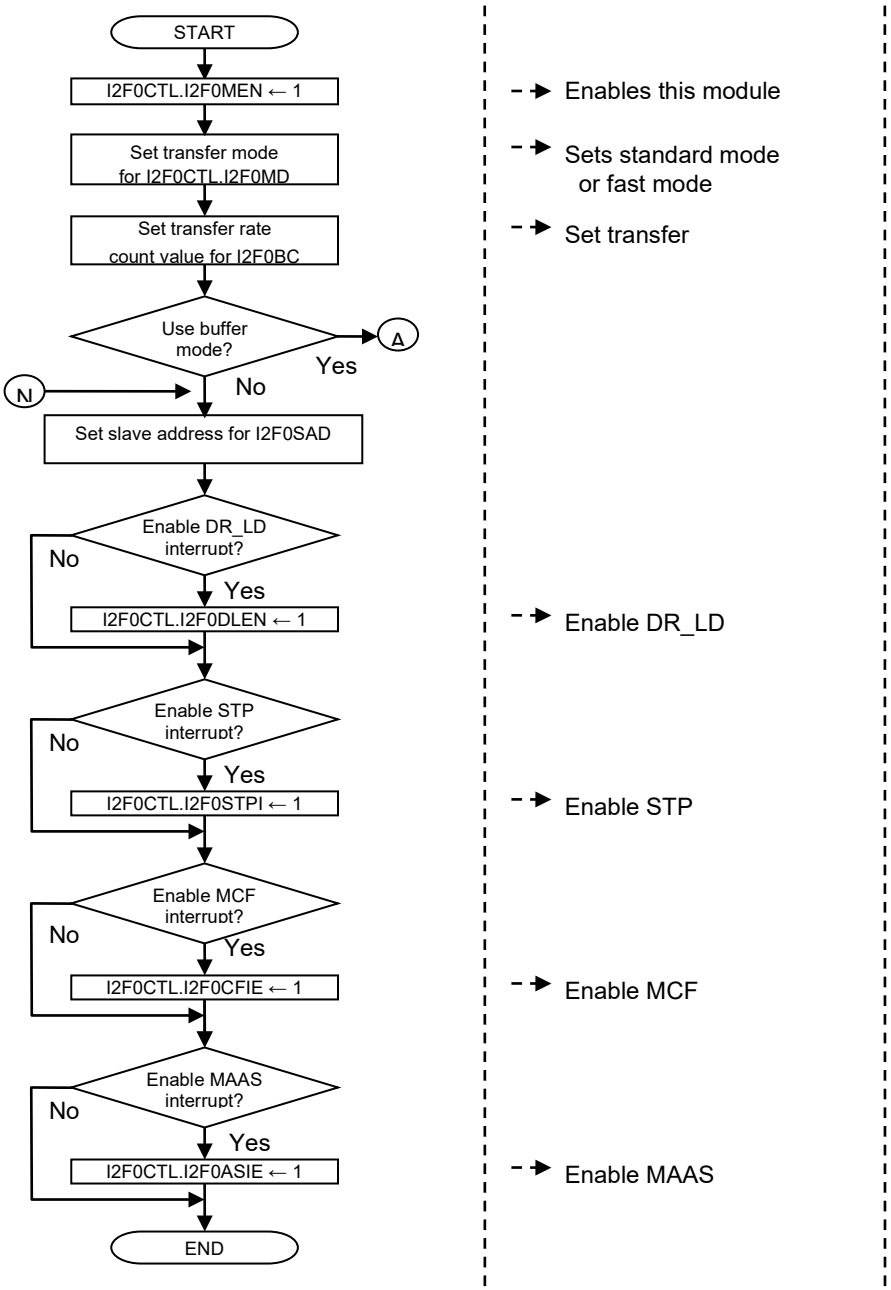
- **I2F0FON** (bit 0)
  This bit indicates whether or not to use the input noise filter for I²C.
  The initial value is "1", in which case the noise filter is used.

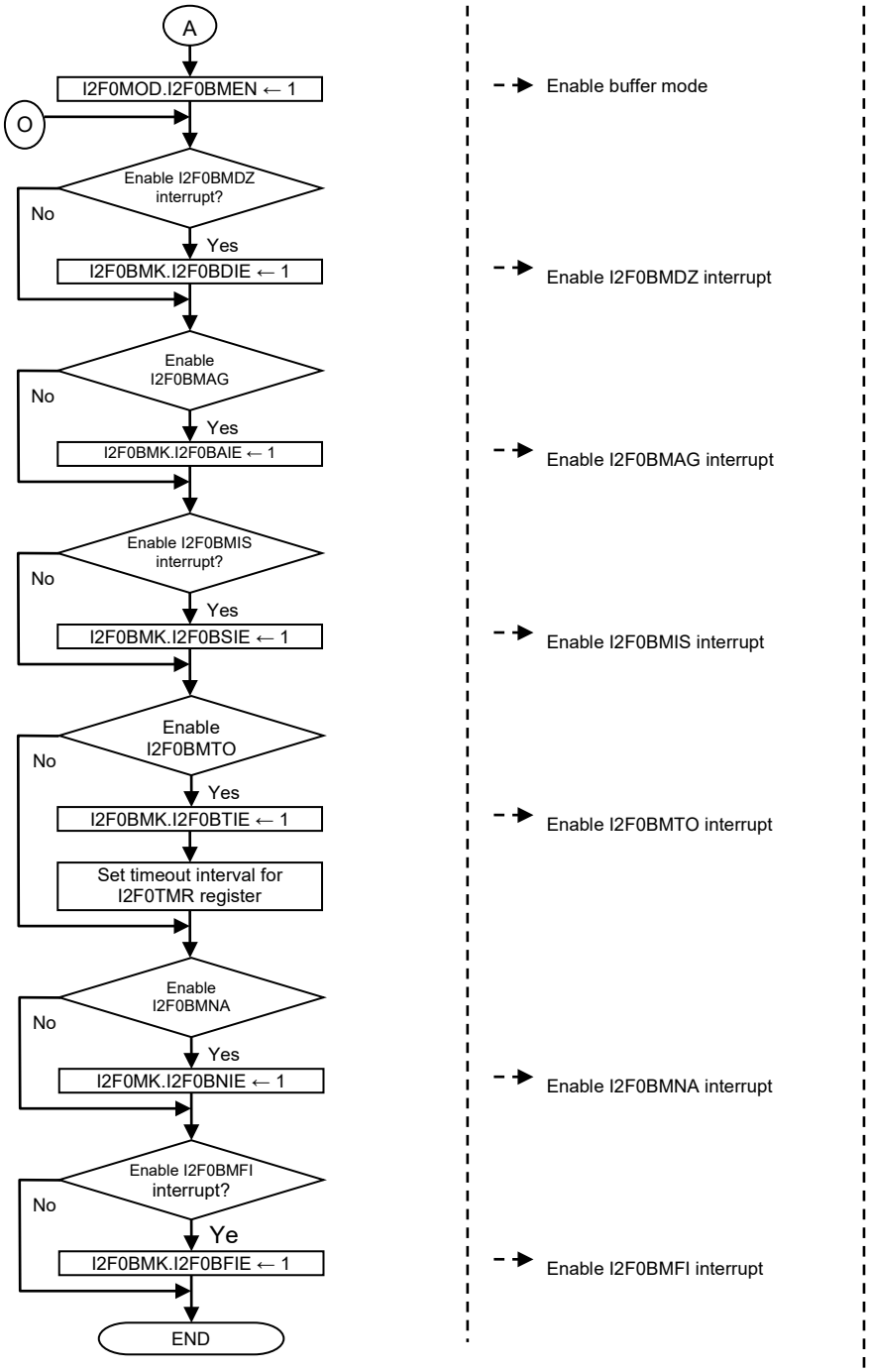
I2F0NFON	Description
0	Noise filter is not used
1	Noise filter is used

20.3. Description of Operation

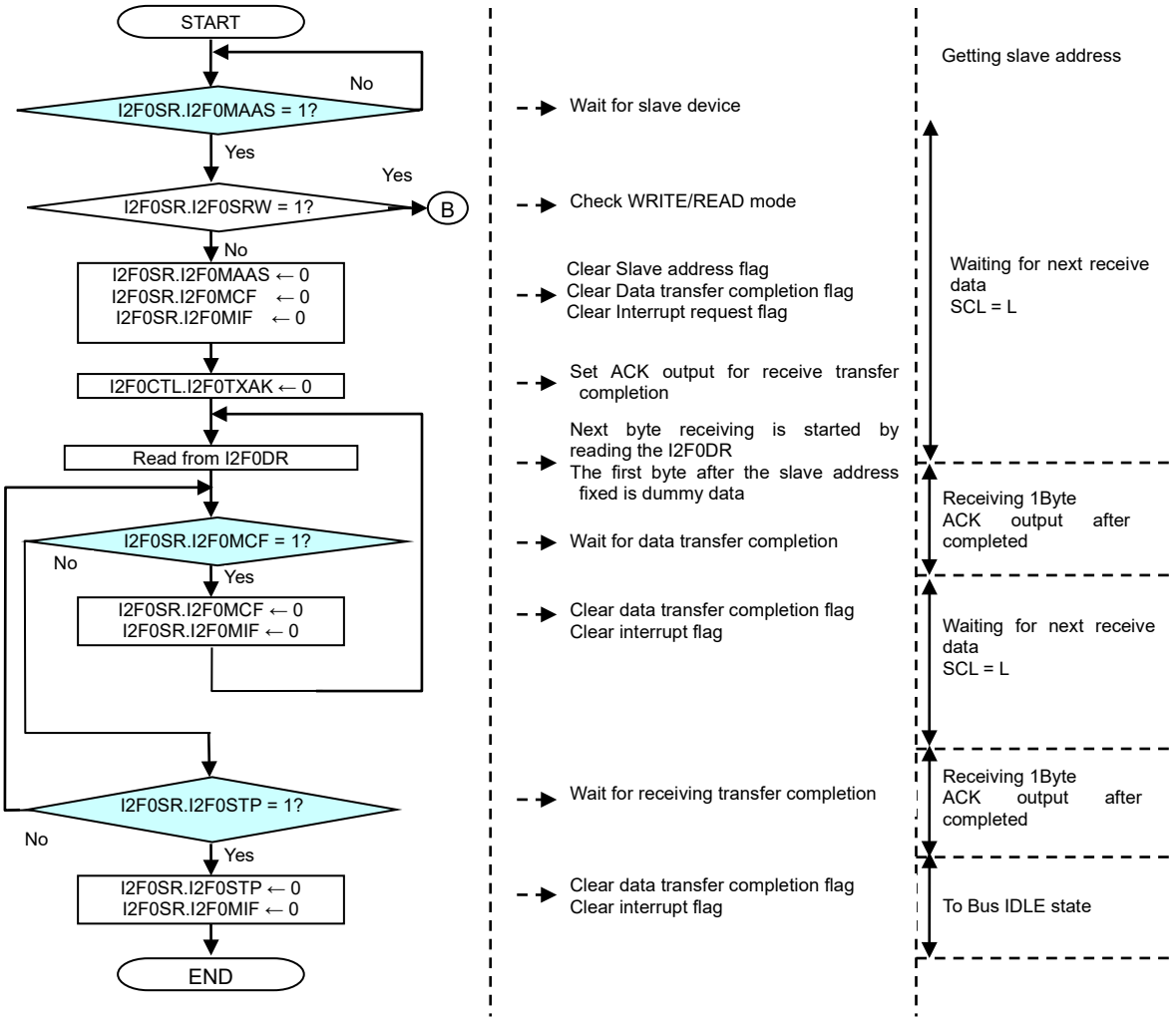
20.3.1. Flow of Initial Setting

This section shows the initial setting flow. "bit name ← 1(0)" represents that software writes 1(0) to this bit. The shaded portions show interrupt sources.

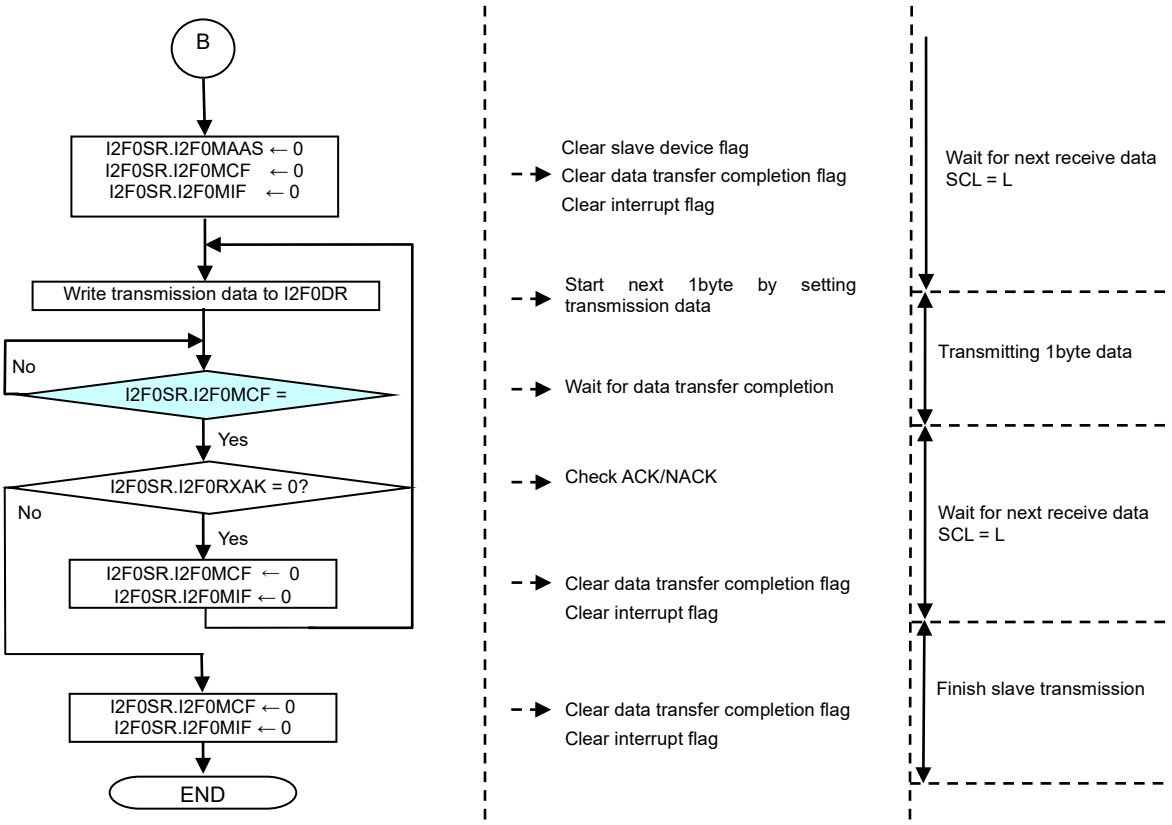



A
I2F0MOD.I2F0BMEN ← 1
O
Enable I2F0BMDZ interrupt?
No
Yes
I2F0BMK.I2F0BDIE ← 1
Enable I2F0BMAG
No
Yes
I2F0BMK.I2F0BAIE ← 1
Enable I2F0BMIS interrupt?
No
Yes
I2F0BMK.I2F0BSIE ← 1
Enable I2F0BMTO
No
Yes
I2F0BMK.I2F0BTIE ← 1
Set timeout interval for I2F0TMR register
Enable I2F0BMNA
No
Yes
I2F0MK.I2F0BNIE ← 1
Enable I2F0BMFI interrupt?
No
Ye
I2F0BMK.I2F0BFIE ← 1
END
Enable buffer mode
Enable I2F0BMDZ interrupt
Enable I2F0BMAG interrupt
Enable I2F0BMIS interrupt
Enable I2F0BMTO interrupt
Enable I2F0BMNA interrupt
Enable I2F0BMFI interrupt

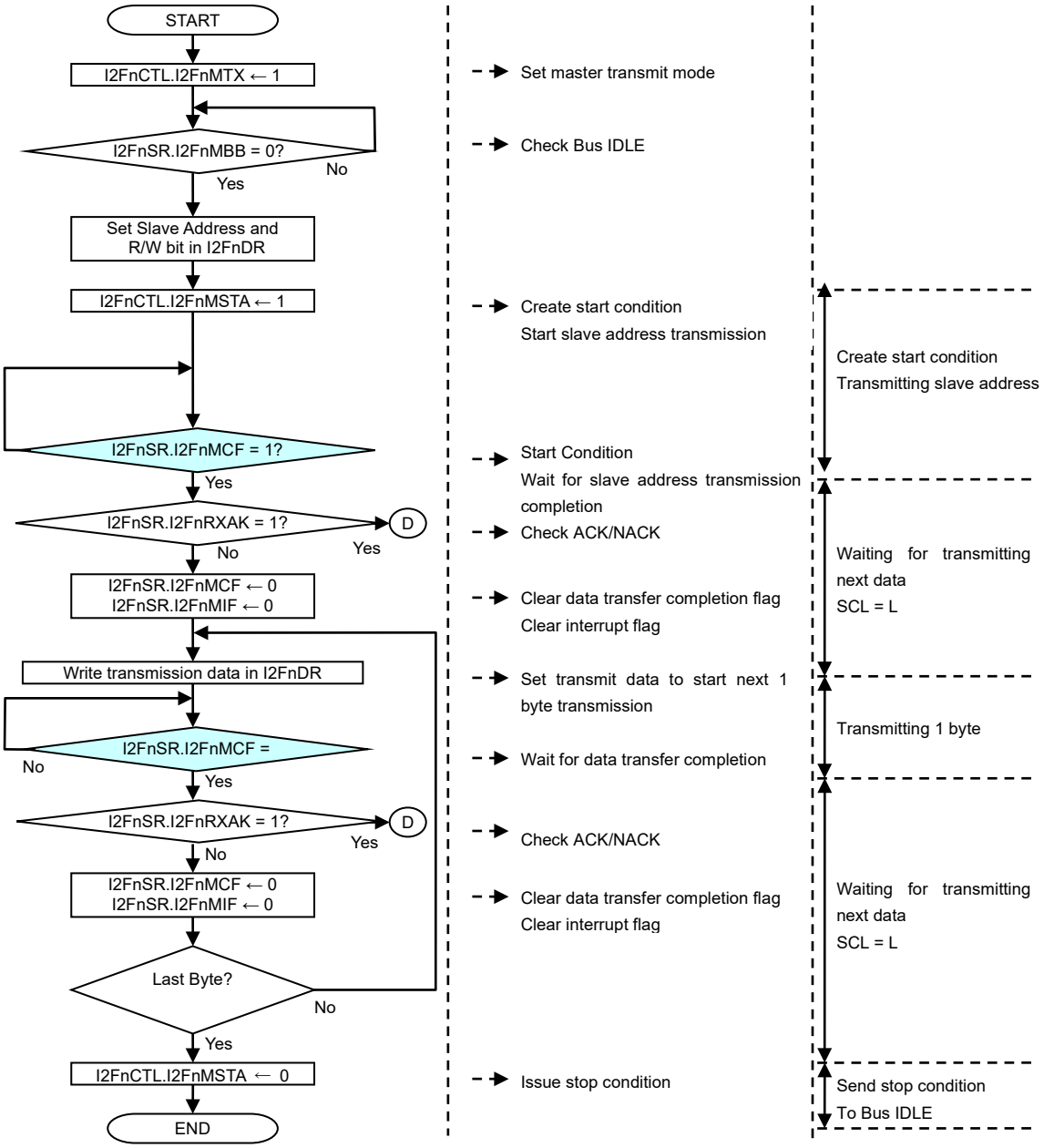
20.3.2. Flow of Slave Reception



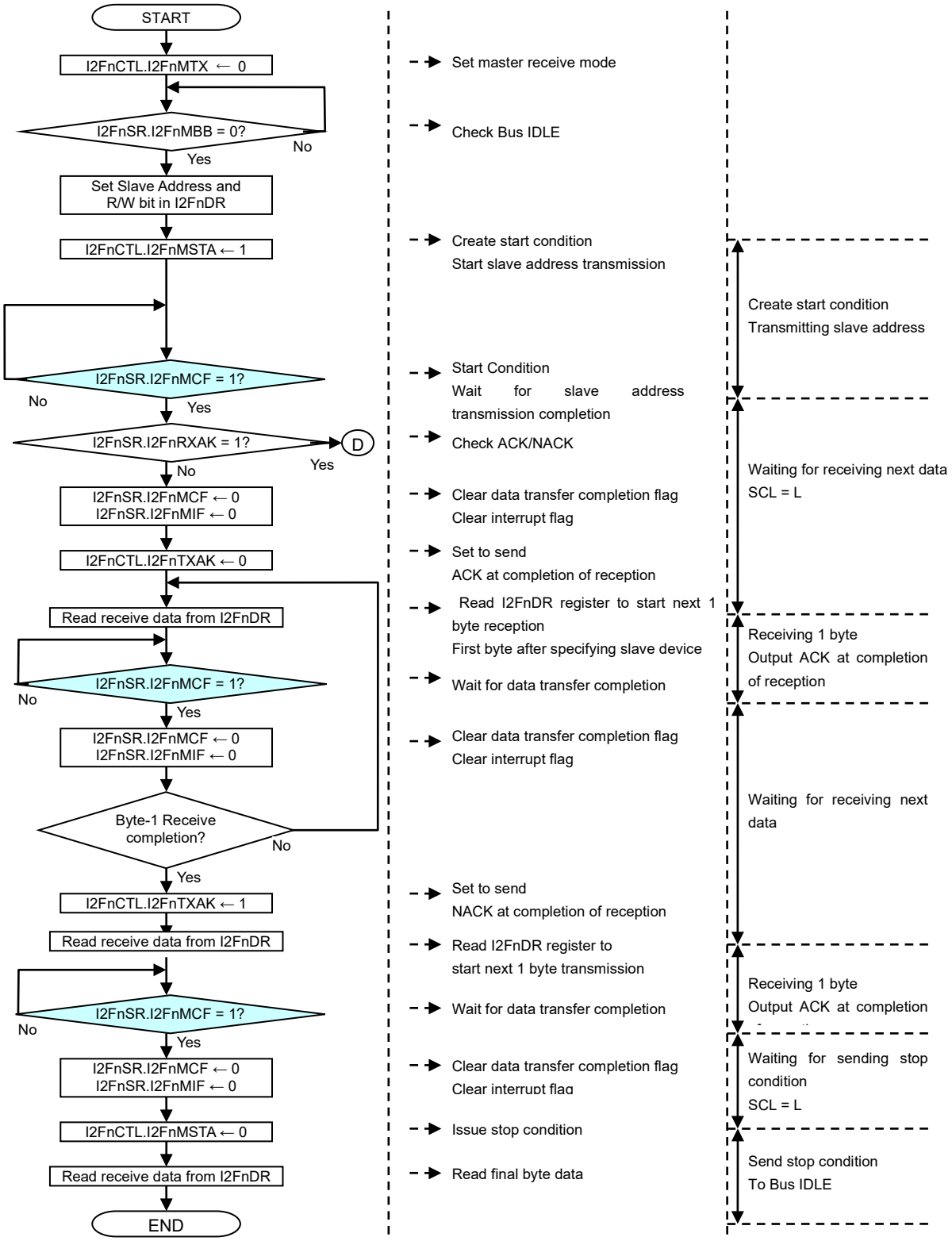
20.3.3. Flow of Slave Transmission



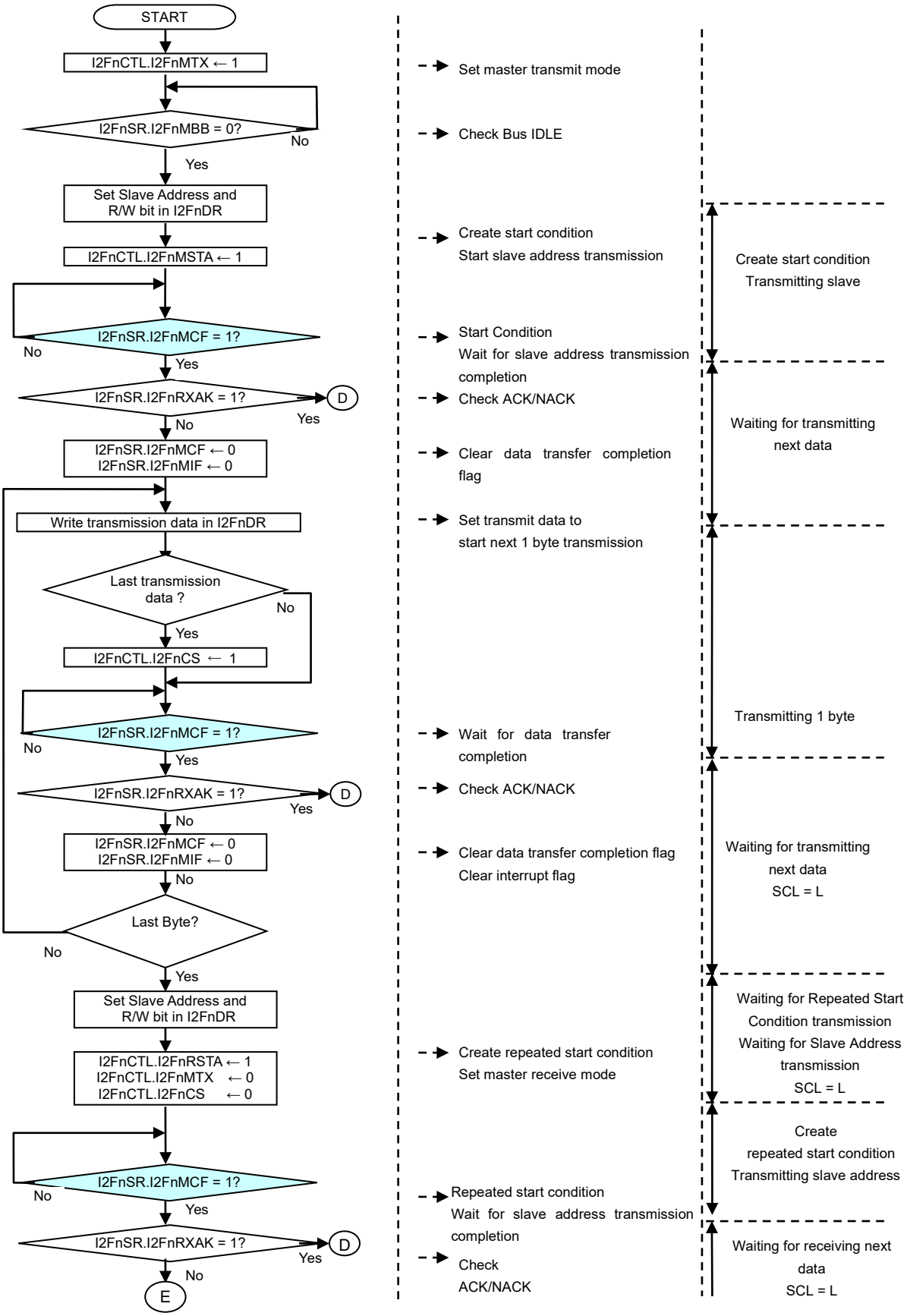
20.3.4. Flow of Master Transmission

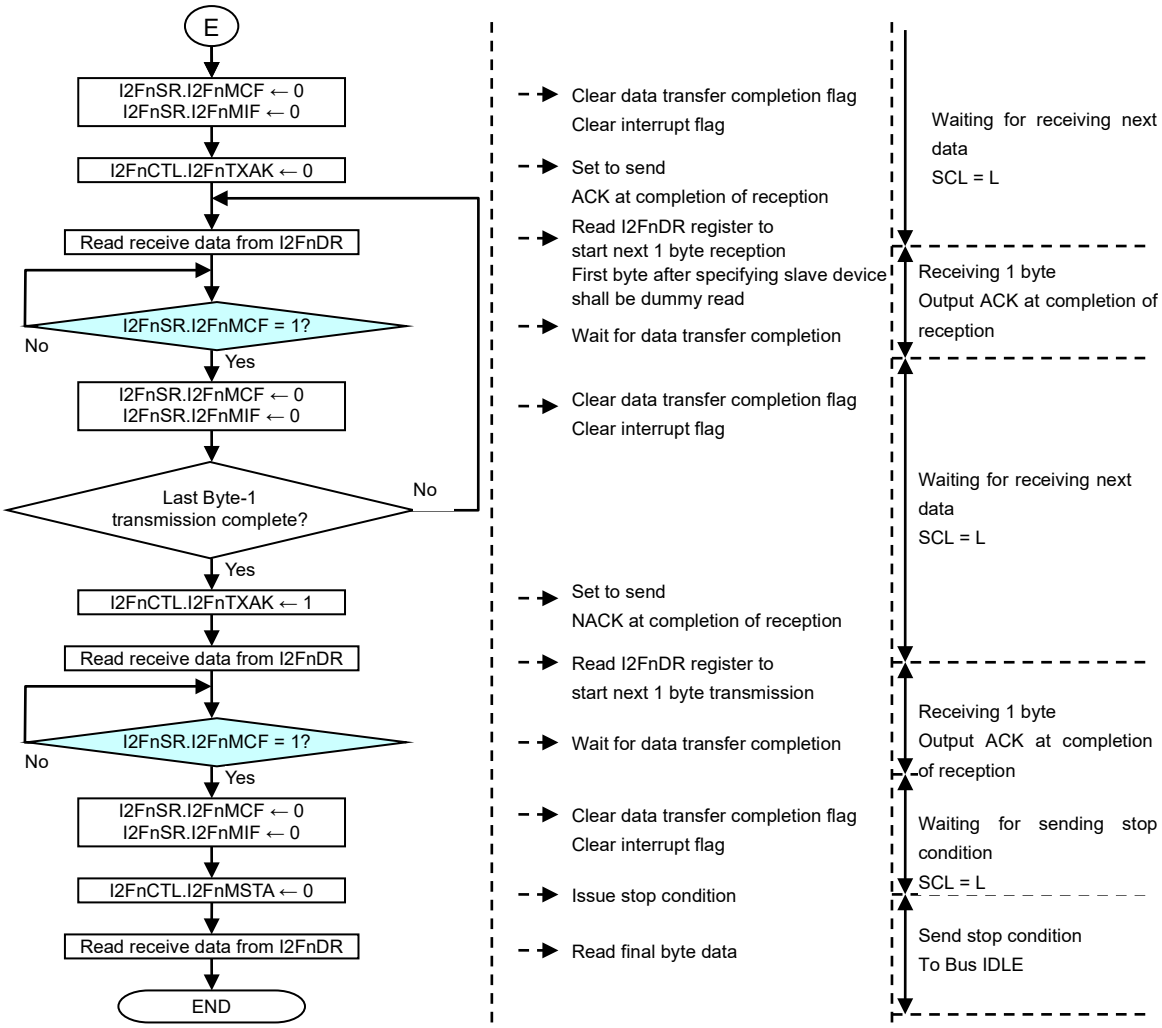


20.3.5. Flow of Master Reception

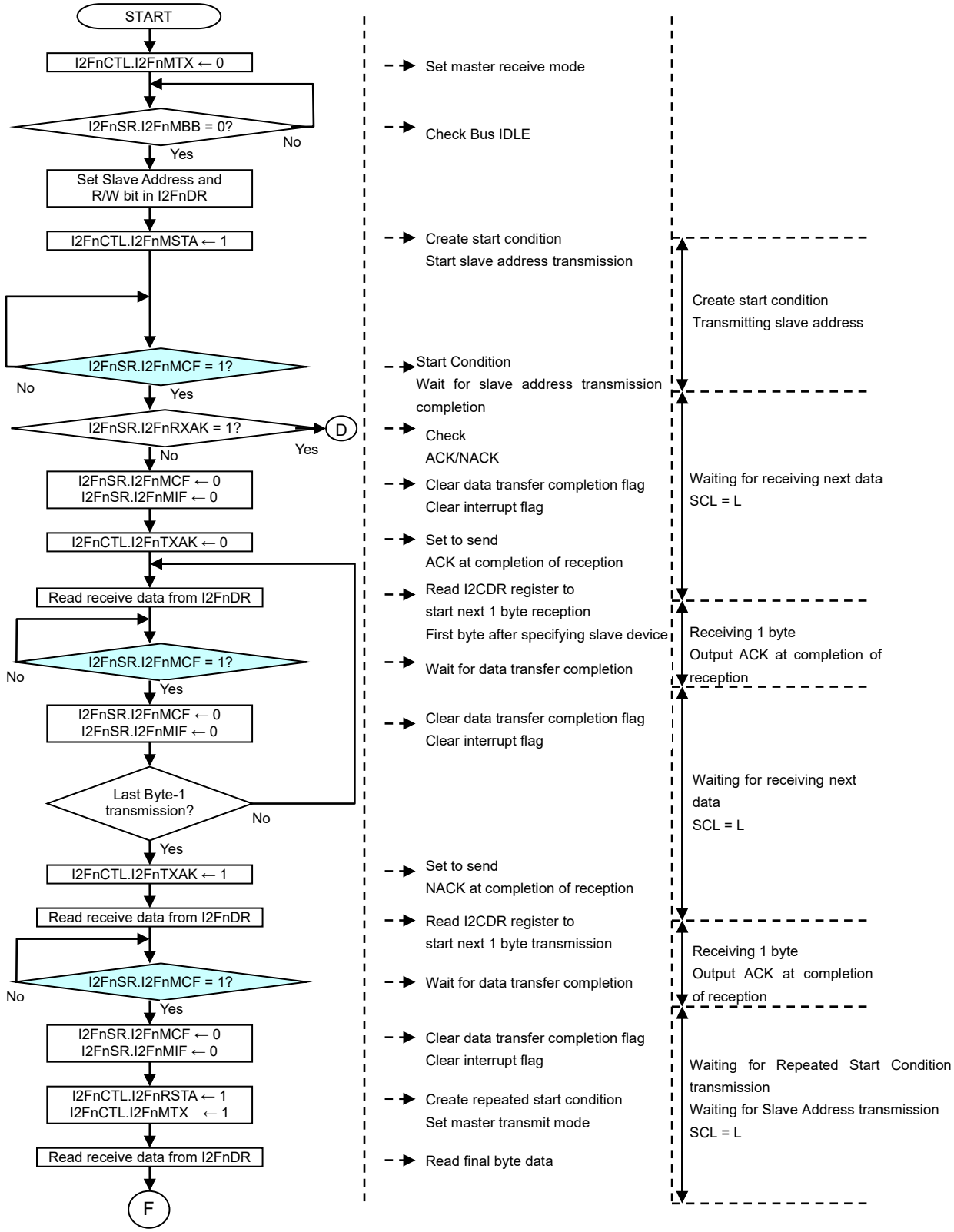


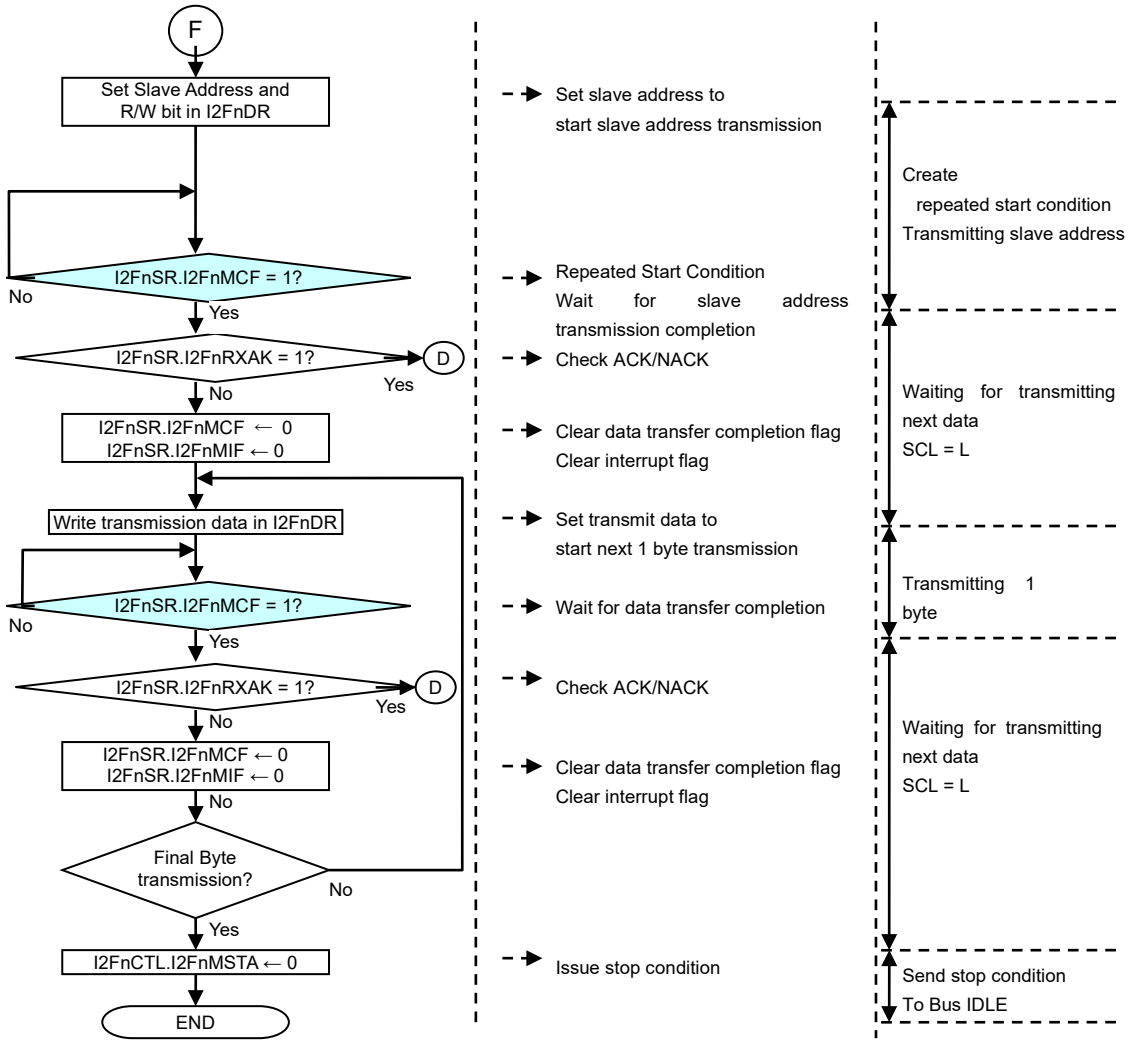
20.3.6. Flow of Compound Mode (Receiving by Master after Transmitting from Master)



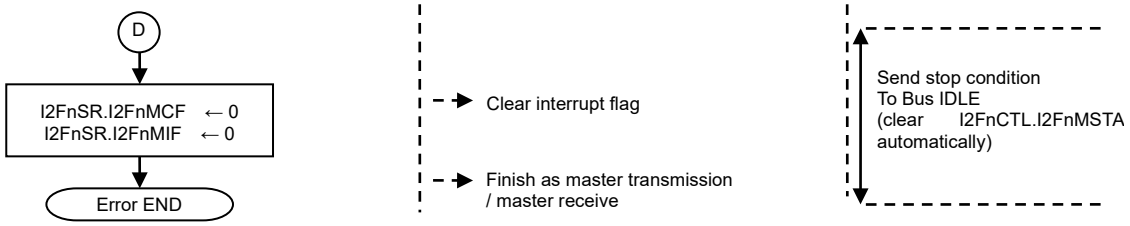

E
I2FnSR.I2FnMCF ← 0
I2FnSR.I2FnMIF ← 0
I2FnCTL.I2FnTXAK ← 0
Read receive data from I2FnDR
I2FnSR.I2FnMCF = 1?
No
Yes
I2FnSR.I2FnMCF ← 0
I2FnSR.I2FnMIF ← 0
Last Byte-1 transmission complete?
No
Yes
I2FnCTL.I2FnTXAK ← 1
Read receive data from I2FnDR
I2FnSR.I2FnMCF = 1?
No
Yes
I2FnSR.I2FnMCF ← 0
I2FnSR.I2FnMIF ← 0
I2FnCTL.I2FnMSTA ← 0
Read receive data from I2FnDR
END
Clear data transfer completion flag
Clear interrupt flag
Set to send
ACK at completion of reception
Read I2FnDR register to
start next 1 byte reception
First byte after specifying slave device
shall be dummy read
Wait for data transfer completion
Clear data transfer completion flag
Clear interrupt flag
Set to send
NACK at completion of reception
Read I2FnDR register to
start next 1 byte transmission
Wait for data transfer completion
Clear data transfer completion flag
Clear interrupt flag
Issue stop condition
Read final byte data
Waiting for receiving next data
SCL = L
Receiving 1 byte
Output ACK at completion of reception
Waiting for receiving next data
SCL = L
Receiving 1 byte
Output ACK at completion of reception
Waiting for sending stop condition
SCL = L
Send stop condition
To Bus IDLE

20.3.7. Flow of Compound Mode (Transmitting from Master after Receiving by Master)

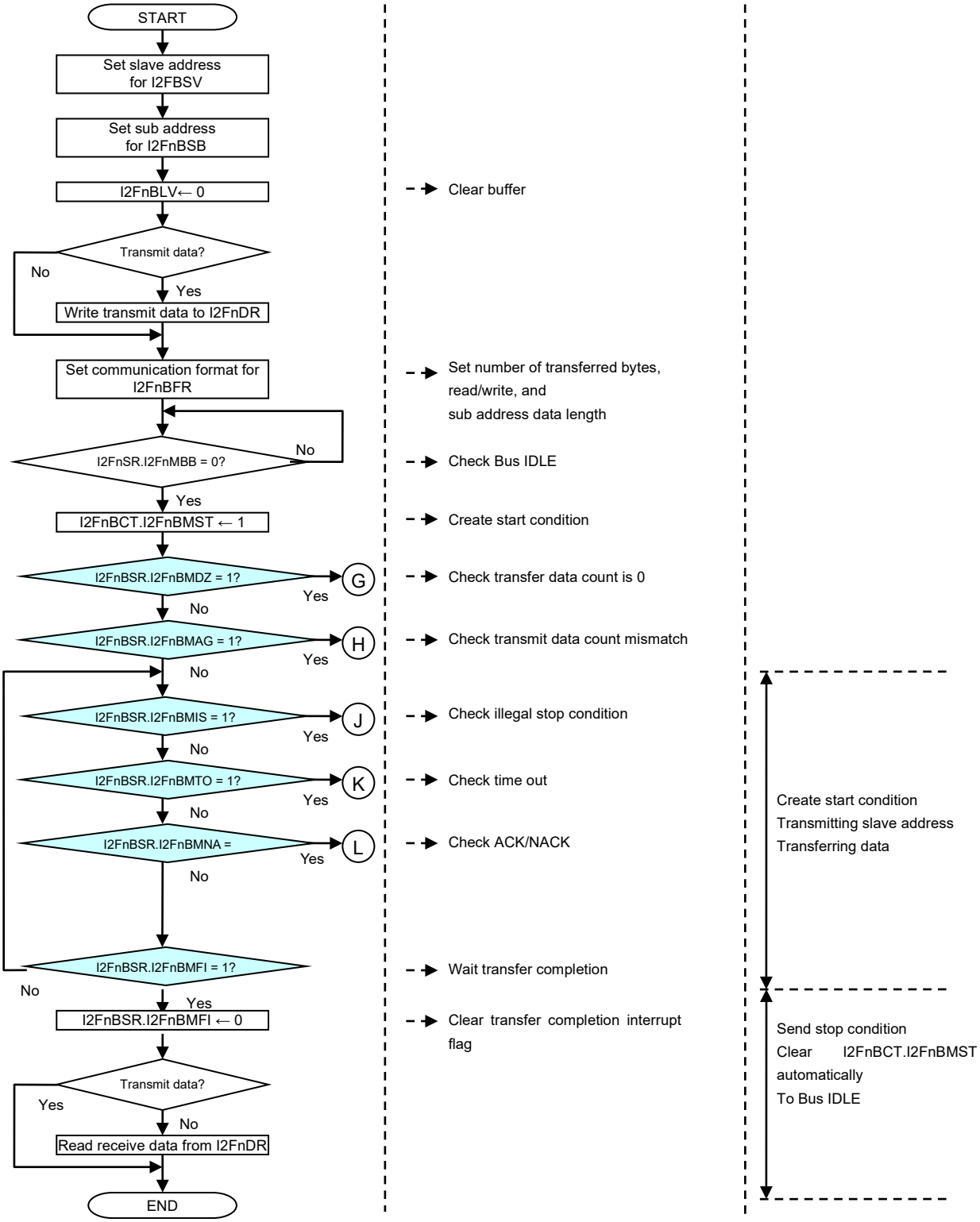


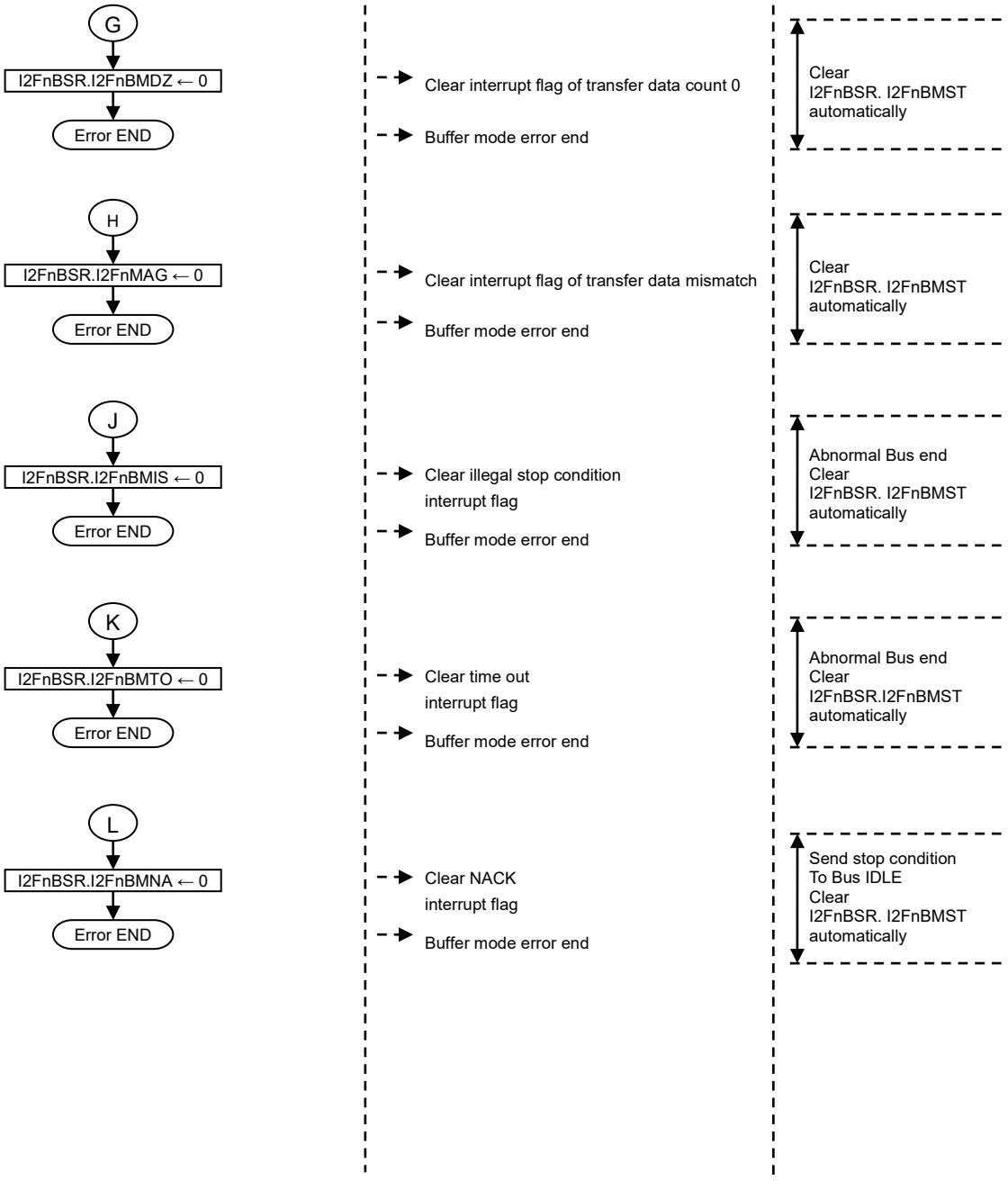


20.3.8. Flow of NACK Receiving



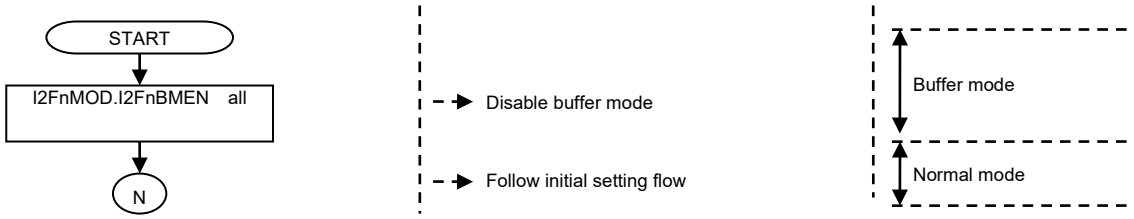
20.3.9. Flow When Using Buffer Mode



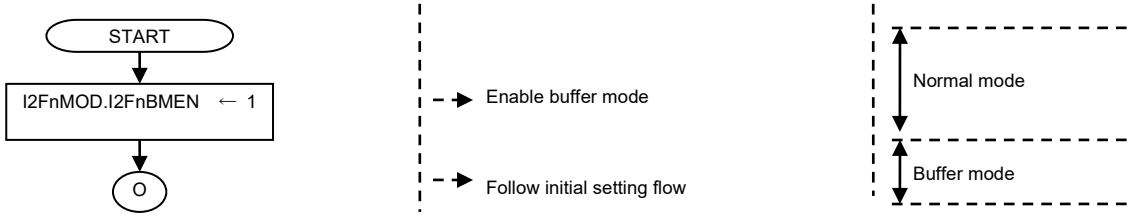

G
I2FnBSR.I2FnBMDZ ← 0
Error END
Clear interrupt flag of transfer data count 0
Buffer mode error end
Clear
I2FnBSR. I2FnBMST
automatically
H
I2FnBSR.I2FnMAG ← 0
Error END
Clear interrupt flag of transfer data mismatch
Buffer mode error end
Clear
I2FnBSR. I2FnBMST
automatically
J
I2FnBSR.I2FnBMIS ← 0
Error END
Clear illegal stop condition
interrupt flag
Buffer mode error end
Abnormal Bus end
Clear
I2FnBSR. I2FnBMST
automatically
K
I2FnBSR.I2FnBMTO ← 0
Error END
Clear time out
interrupt flag
Buffer mode error end
Abnormal Bus end
Clear
I2FnBSR.I2FnBMST
automatically
L
I2FnBSR.I2FnBMNA ← 0
Error END
Clear NACK
interrupt flag
Buffer mode error end
Send stop condition
To Bus IDLE
Clear
I2FnBSR. I2FnBMST
automatically

20.3.10. Flow of Mode Switching

20.3.10.1. Flow of Switching to Normal Mode



20.3.10.2. Flow of Switching to Buffer Mode

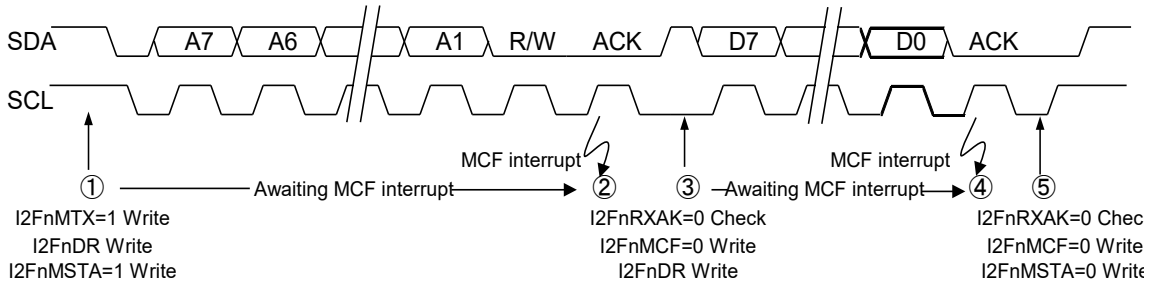


[Note]
Be sure to switch modes before starting I²C transfer. When change the buffer mode during slave movement, an internal buffer mode signal is replaced after slave movement.

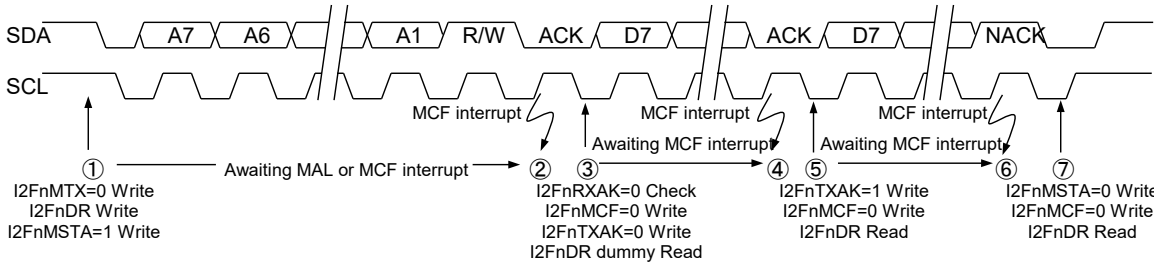
20.4. Waveform in Each Mode

In the figures below, the hatched portions are the segments that are driven by the transfer destination, and n=0.

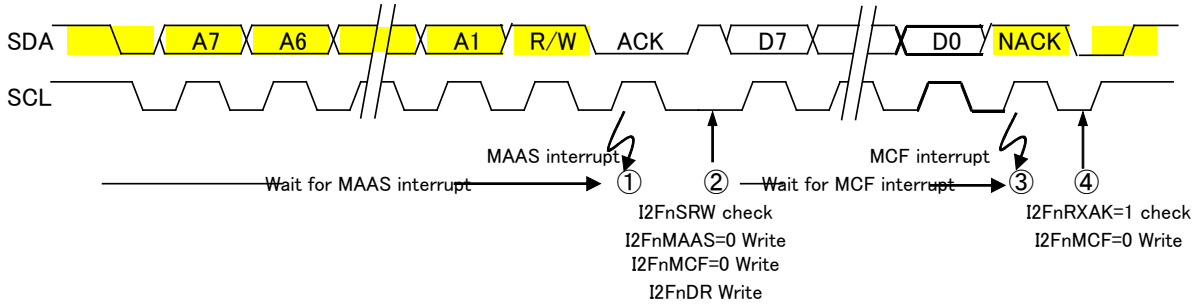
20.4.1. Waveform Transmitted by Master



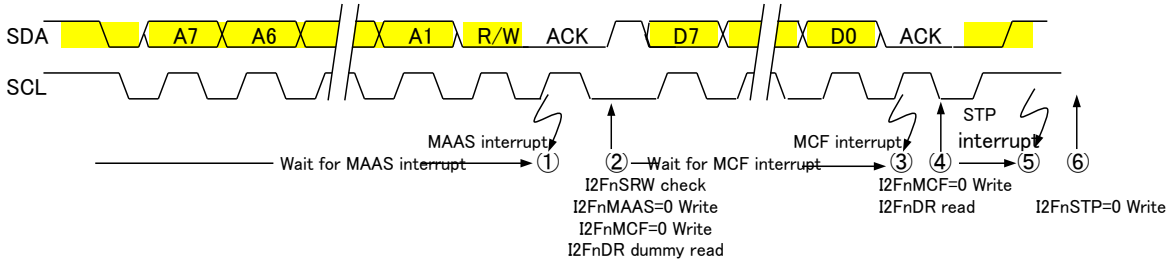
20.4.2. Waveform Received by Master



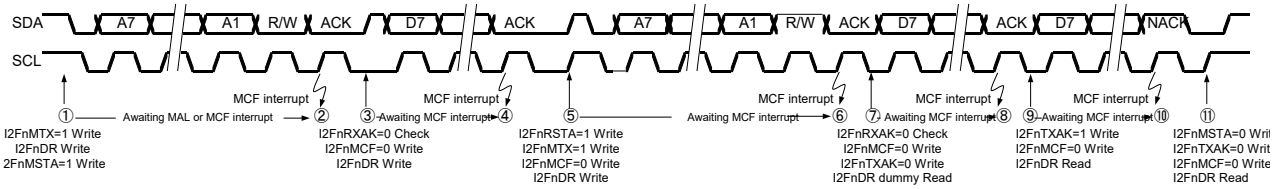
20.4.3. Waveform Transmitted by Slave



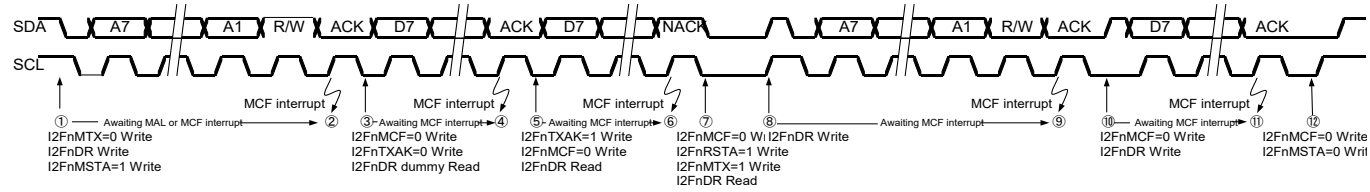
20.4.4. Waveform Received by Slave



20.4.5. Waveform of Compound Format (Master Transmission + Master Reception)

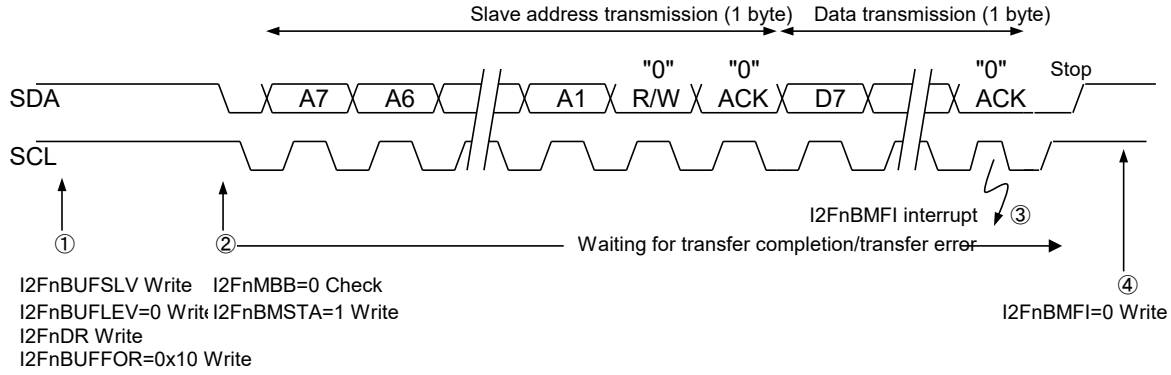


20.4.6. Waveform of Compound Format (Master Reception + Master Transmission)



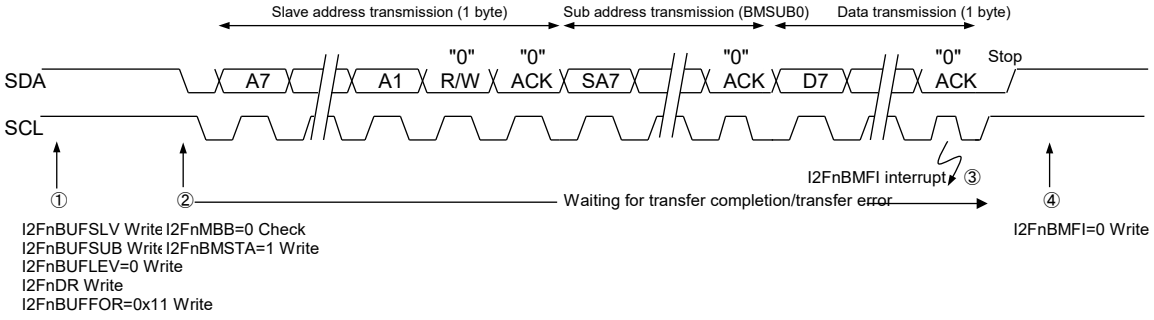
20.4.7. Waveform 1 When Using Buffer Mode

(When data length of sub address = 0, data transmission, number of transferred bytes = 1)



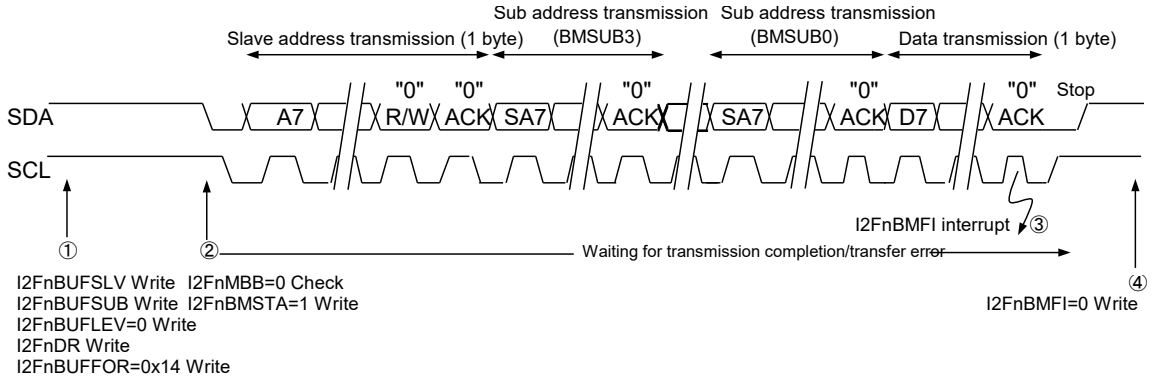
20.4.8. Waveform 2 When Using Buffer Mode

(When data length of sub address = 1, data transmission, number of transferred bytes = 1)



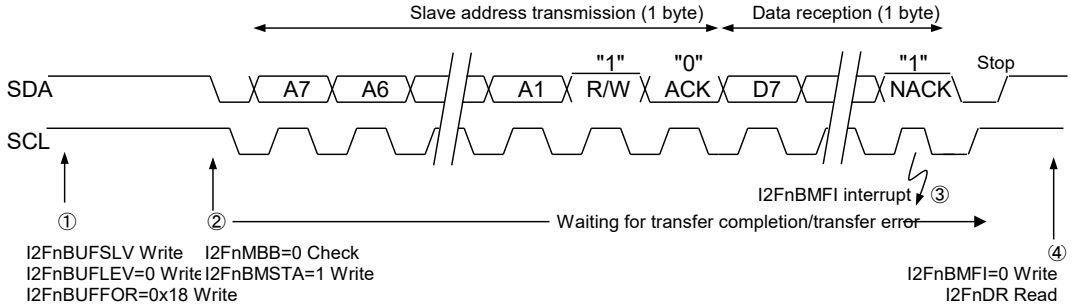
20.4.9. Waveform 3 When Using Buffer Mode

(When data length of sub address = 4, data transmission, number of transferred bytes = 1)



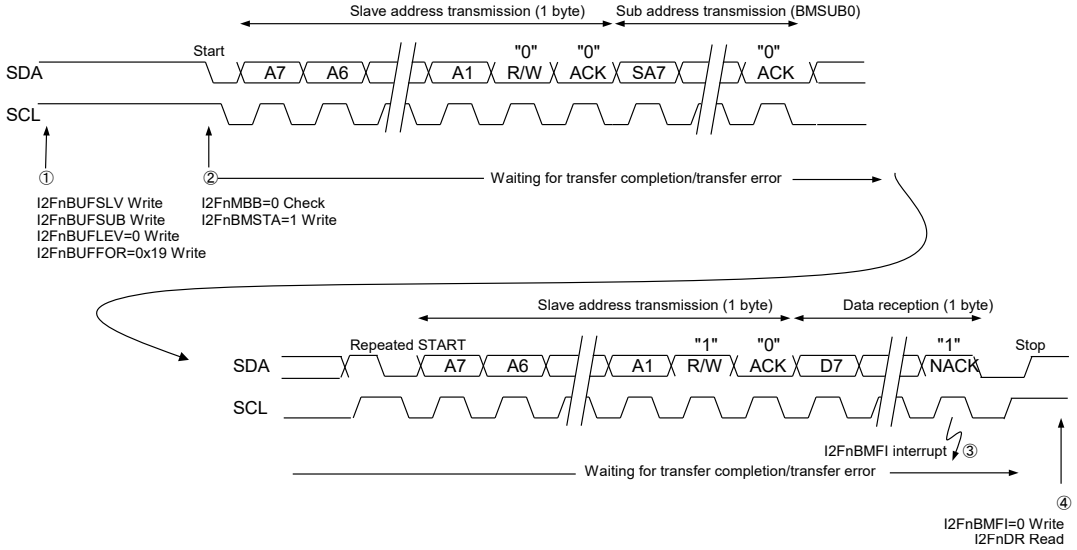
20.4.10. Waveform 4 When Using Buffer Mode

(When data length of sub address = 0, data reception, number of transferred bytes = 1)



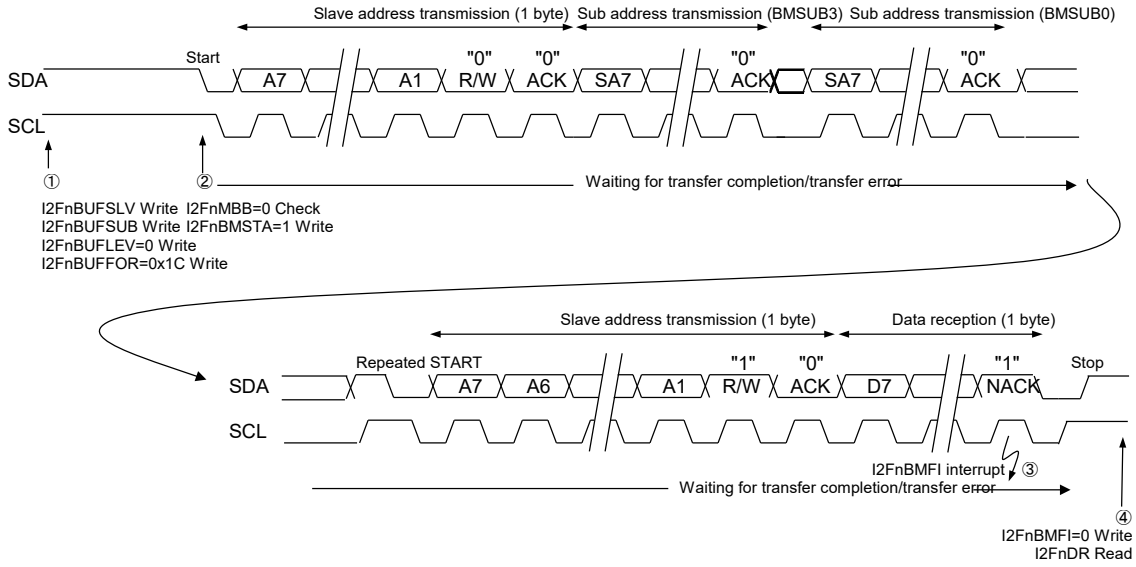
20.4.11. Waveform 5 When Using Buffer Mode

(When data length of sub address = 1, data reception, number of transferred bytes = 1)



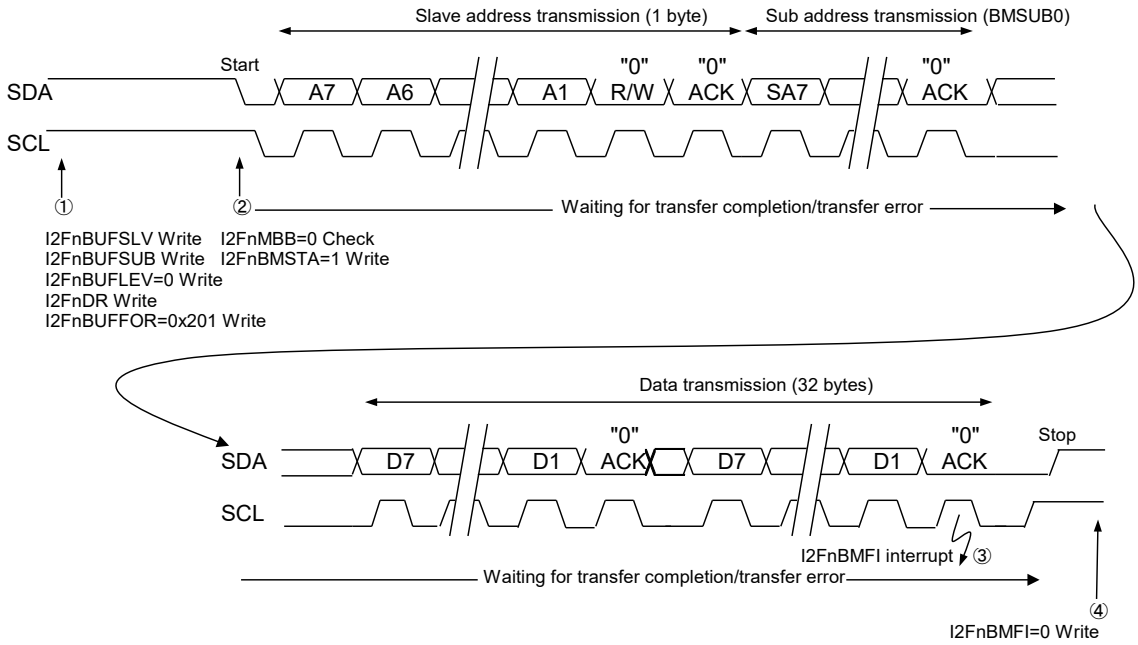
20.4.12. Waveform 6 When Using Buffer Mode

(When data length of sub address = 2, data reception, number of transferred bytes = 1)



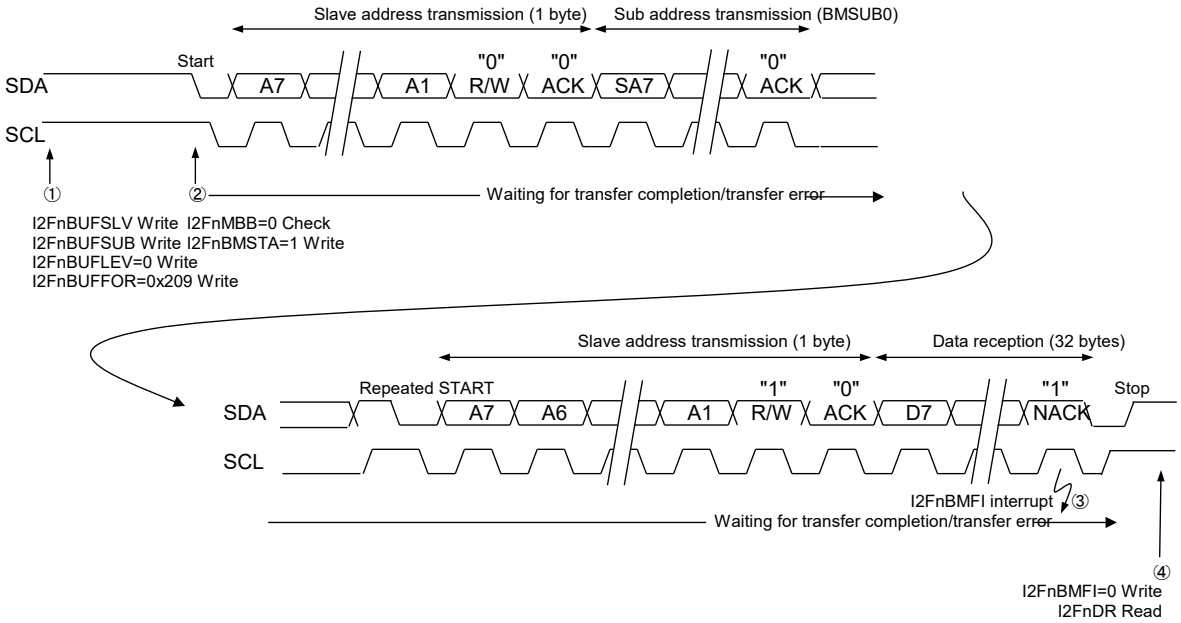
20.4.13. Waveform 7 When Using Buffer Mode

(When data length of sub address = 1, data transmission, number of transferred bytes = 32)



20.4.14. Waveform 8 When Using Buffer Mode

(When data length of sub address = 1, data reception, number of transferred bytes = 32)



20.5. Restrictions

[I2C Master transmission mode]

If there is a NACK response after data is transferred in the I²C master transmit mode, a STOP condition is automatically sent at the same time it enters the IDLE state. To resume the transmission, it is necessary to set the I2F0MSTA of the control register to 1 and send a START condition again.

In the I²C master transmit mode, be sure to write the first byte of the transmit data before setting I2F0MSTA=1 (sending START condition). (The data transmission is automatically started after sending START condition)
Write subsequent bytes of the transmit data after the DR_LD status is set to 1. Any transmit data written to the data register with the DR_LD status set to 0 cannot be guaranteed.

In the I²C master transmit mode, be sure to set the STOP condition (I2F0MSTA=0) after transferring the data (after the I2F0MCF status is set to 1). The STOP condition sending is started after the ACK response cycle. If it is set at any other timing than an ACK cycle, the STOP condition will be sent immediately, which may cause a failure.

Chapter 21

USB DEVICE

21. USB DEVICE

21.1. General Description

This is a Universal Serial Bus (USB) general-purpose device controller.
This USB DEVICE supports control transfer mode, bulk transfer mode, interrupt transfer mode, and isochronous transfer mode and also supports 5 or 6 endpoints.

21.1.1. Features

- Compliant with USB2.0.
- Supports Full-speed (12 Mbps).
- Supports 4 data transfer types:
  Control transfer, bulk transfer, interrupt transfer, isochronous transfer
- Endpoints: 5 or 6
  Control EP: 1
  Bulk/Interrupt EP: 3
  Isochronous/bulk/interrupt EP: 1 or 2
- Built-in FIFOs for storing data
- The FIFOs of EP1, EP2, EP4, and EP5 are double sided.
- Supports 8-/16-/32-bit read/write from the CPU for the FIFOs EP0 to 5.
- Supports bus-powered devices.
  The USB DEVICE enters power-saving mode by automatically detecting suspend conditions.
  The USB DEVICE returns to normal operation when resume conditions are detected.

21.1.2. Configuration

Figure 21-1 shows the configuration of the USB DEVICE.

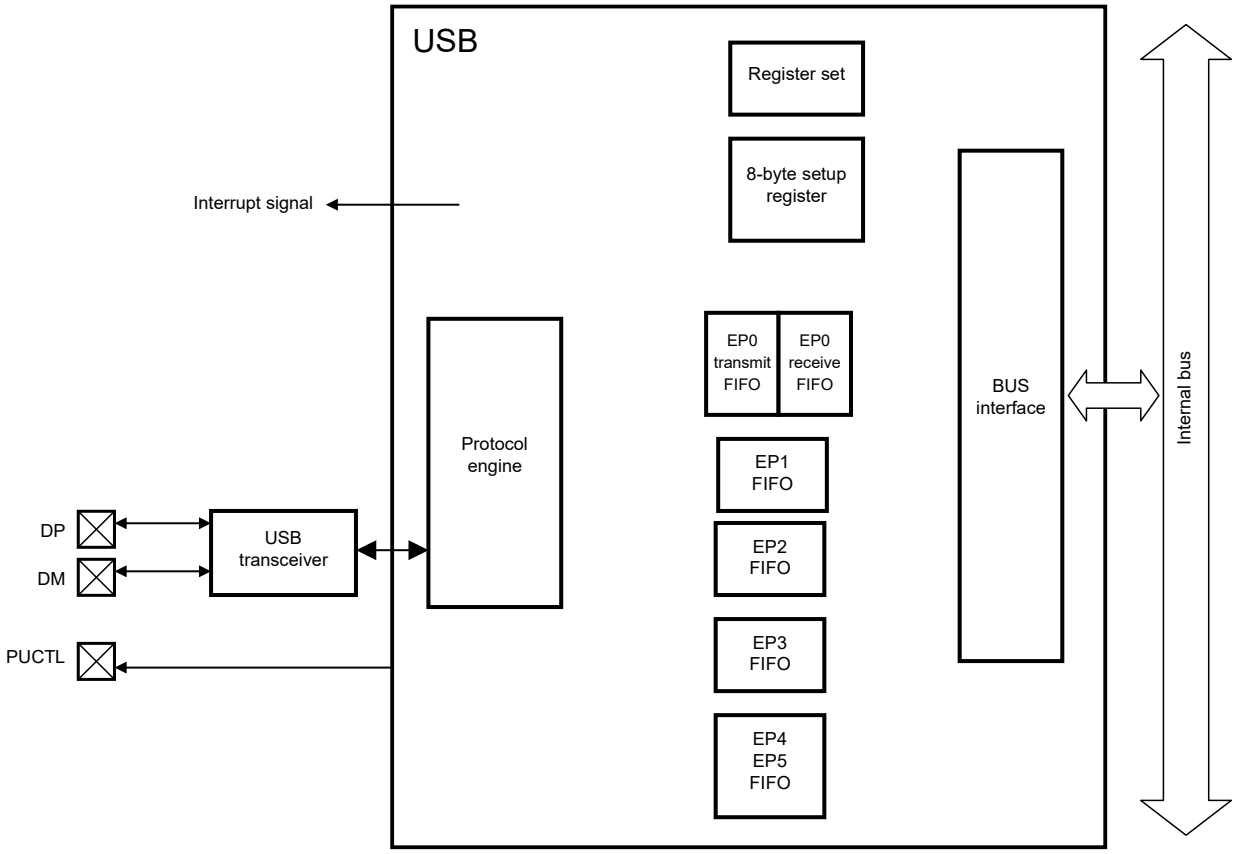


Figure 21-1 Configuration of USB DEVICE

- Configuration of Endpoints and FIFOs
  A 5EP mode that allows 5 EPs and a 6EP mode that allows 6 EPs are available for the USB block through register setting. The available transfer mode is fixed for EP0, however, for EP1, EP2, and EP3, either bulk transfer or an interrupt transfer can be selected. For EP4 and EP5, one of transfer modes of isochronous, bulk, and interrupt can be selected. For EP1 to EP5, a data transfer direction can be selected.

Endpoint	5EP mode			6EP mode		
	FIFO capacity	Transfer mode	Remarks	FIFO capacity	Transfer mode	Remarks
EP0	Receive 32 Transmit 32	Control		Receive 32 Transmit 32	Control	
EP1	64x2	Bulk/Interrupt (IN/OUT)		64x2	Bulk/Interrupt (IN/OUT)	
EP2	64x2	Bulk/Interrupt (IN/OUT)		64x2	Bulk/Interrupt (IN/OUT)	
EP3	32	Bulk/Interrupt (IN/OUT)		32	Bulk/Interrupt (IN/OUT)	
EP4	128x2 (64x2)	Isochronous/ Bulk/Interrupt (IN/OUT)		64x2	Isochronous/ Bulk/Interrupt (IN/OUT)	
EP5	—	—		64x2	Isochronous/ Bulk/Interrupt (IN/OUT)	

Unit of FIFO capacity: Byte

Note 1: Use the SYSCON register for selection between the 5EP mode and the 6EP mode.

Note 2: EP1, EP2, and EP3 can be assigned to either bulk transfer or interrupt transfer independently. For both bulk transfer and interrupt transfer, up to 64 (32 for EP3) bytes can be set as the packet size.

Note 3: For EP4 and EP5, one of isochronous, bulk, and interrupt transfer modes can be set. When bulk transfer is set, up to 64 bytes can be set as the packet size.

Note 4: When using EP4 and EP5 for isochronous transfer:
In 5EP mode, the maximum packet size of EP4 is 128 bytes. EP5 is not allowed.
In 6EP mode, the maximum packet size for both EP4 and EP5 is 64 bytes.

21.1.3. List of Pins

Table 21-1 List of Pins Interfaced with the Outside of LSI

Pin name	I/O	Function
DM	IO	USBdev D-
DP	IO	USBdev D+
PUCTL	O	USBdev PUCTL

21.2. Description of Registers

21.2.1. List of Registers

• Common section

Table 21-2 USB DEVICE Registers (1/3)

Address	Name	Symbol	R/W	Size	Initial value
0x4100_4000	bmRequestType setup register	BMREQUESTTYPE	R	32	0x0000_0000
0x4100_4004	bRequest setup register	BREQUEST	R	32	0x0000_0000
0x4100_4008	wValueLSB setup register	WVALUELSB	R	32	0x0000_0000
0x4100_400C	wValueMSB setup register	WVALUEMSB	R	32	0x0000_0000
0x4100_4010	wIndexLSB setup register	WINDEXLSB	R	32	0x0000_0000
0x4100_4014	wIndexMSB setup register	WINDEXMSB	R	32	0x0000_0000
0x4100_4018	wLengthLSB setup register	WLENGTHLSB	R	32	0x0000_0000
0x4100_401C	wLengthMSB setup register	WLENGTHMSB	R	32	0x0000_0000
0x4100_4080	Device address register	DVCADR	R/W	32	0x0000_0000
0x4100_4084	Interrupt status register 1	INTSTAT1	R	32	0x0000_0000
0x4100_4088	Interrupt status register 2	INTSTAT2	R/W	32	0x0000_0000
0x4100_4090	Interrupt enable register 1	INTENBL1	R/W	32	0x0000_0001
0x4100_4094	Interrupt enable register 2	INTENBL2	R/W	32	0x0000_0000
0x4100_40B0	Isochronous mode select register	ISOMODESEL	R/W	32	0x0000_0000
0x4100_40B4	Frame number register LSB	FRAMELSB	R	32	0x0000_0000
0x4100_40B8	Frame number register MSB	FRAMEMSB	R	32	0x0000_0000
0x4100_40BC	System control register	SYSCON	R/W	32	0x0000_0000
0x4100_40C0	Polarity select register	POLSEL	R/W	32	0x0000_0000
0x4100_40E8	Oscillation test register	OSCTEST	R/W	32	0x0000_0000
0x4100_40FC	Transmit clock control register	TXCLKCONT	R/W	32	0x0000_0000

• For EPs

Table 21-3 USB DEVICE Registers (2/3)

Address	Name	Symbol	R/W	Size	Initial value
0x4100_4100	EP0 configuration register	EP0CONF	R	32	0x0000_0000
0x4100_4104	EP1 configuration register	EP1CONF	R/W	32	0x0000_0000
0x4100_4108	EP2 configuration register	EP2CONF	R/W	32	0x0000_0000
0x4100_410C	EP3 configuration register	EP3CONF	R/W	32	0x0000_0000
0x4100_4110	EP4 configuration register	EP4CONF	R/W	32	0x0000_0000
0x4100_4114	EP5 configuration register	EP5CONF	R/W	32	0x0000_0000
0x4100_4120	EP0 control register	EP0CONT	R/W	32	Undefined
0x4100_4124	EP1 control register	EP1CONT	R/W	32	0x0000_0000
0x4100_4128	EP2 control register	EP2CONT	R/W	32	0x0000_0000
0x4100_412C	EP3 control register	EP3CONT	R/W	32	0x0000_0000
0x4100_4130	EP4 control register	EP4CONT	R/W	32	0x0000_0000
0x4100_4134	EP5 control register	EP5CONT	R/W	32	0x0000_0000
0x4100_4140	EP0 payload register	EP0PLD	R/W	32	0x0000_0020
0x4100_4144	EP1 payload register	EP1PLD	R/W	32	0x0000_0000
0x4100_4148	EP2 payload register	EP2PLD	R/W	32	0x0000_0000
0x4100_414C	EP3 payload register	EP3PLD	R/W	32	0x0000_0000
0x4100_4150	EP4 payload register	EP4PLD	R/W	32	0x0000_0000
0x4100_4154	EP5 payload register	EP5PLD	R/W	32	0x0000_0000
0x4100_4160	EP0 receive byte counter	EP0RXCNT	R	32	0x0000_0000
0x4100_4164	EP1 receive byte counter	EP1RXCNT	R	32	0x0000_0000
0x4100_4168	EP2 receive byte counter	EP2RXCNT	R	32	0x0000_0000
0x4100_416C	EP3 receive byte counter	EP3RXCNT	R	32	0x0000_0000
0x4100_4170	EP4 receive byte counter	EP4RXCNT	R	32	0x0000_0000
0x4100_4174	EP5 receive byte counter	EP5RXCNT	R	32	0x0000_0000
0x4100_4180	EP0 status register	EP0STAT	R/W	32	0x0000_0000
0x4100_4184	EP1 status register	EP1STAT	R/W	32	0x0000_0000
0x4100_4188	EP2 status register	EP2STAT	R/W	32	0x0000_0000
0x4100_418C	EP3 status register	EP3STAT	R/W	32	0x0000_0000
0x4100_4190	EP4 status register	EP4STAT	R/W	32	0x0000_0000
0x4100_4194	EP5 status register	EP5STAT	R/W	32	0x0000_0000

• FIFO section

Table 21-4 USB DEVICE Registers (3/3)

Address	Name	Symbol	R/W	Size	Initial value
0x4100_41C0	EP0 transmit FIFO	EP0TXFIFO	W	32	Undefined
0x4100_41E0	EP0 receive FIFO	EP0RXFIFO	R	32	Undefined
0x4100_41E4	EP1 transmit/receive FIFO	EP1FIFO	R or W	32	Undefined
0x4100_41E8	EP2 transmit/receive FIFO	EP2FIFO	R or W	32	Undefined
0x4100_41EC	EP3 transmit/receive FIFO	EP3FIFO	R or W	32	Undefined
0x4100_41F0	EP4 transmit/receive FIFO	EP4FIFO	R or W	32	Undefined
0x4100_41F4	EP5 transmit/receive FIFO	EP5FIFO	R or W	32	Undefined

Note:
Accesses to undefined addresses are prohibited since the operation is not guaranteed.

21.2.2. bmRequestType Set-up Register (BMREQUESTTYPE)

Address: 0x4100_4000
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D7	D[6:5]				D[4:0]		
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Register]
In the set-up stage of control transfer based on a request from the host, the 8-byte set-up data to be transmitted from the host is automatically received by this block, and then stored in eight registers including this register. The data format is defined in Section 9.3 of the USB standard.

[Description of Bits]

- **D[4:0]** (bits 0-4)
  These bits indicate definition on the receive side.

D[4:0]	Description
00000	Device
00001	Interface
00010	Endpoint
00011	Others
00100	Reserved

- **D[6:5]** (bits 5-6)
  These bits indicate definition on the type.

D[5:6]	Description
00	Standard
01	Class
10	Vendor
11	Reserved

- **D7** (bit 7)
  This bit indicates the data transfer direction.

D7	Description
0	Host to device
1	Device to host

21.2.3. bRequest Set-up register (BREQUEST)

Address: 0x4100_4004
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Register]
The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its second byte is stored in this register. The description of the request code is defined in Section 9.3 of the USB standard and related standards.

[Description of Bits]
- **D[7:0]** (bits 0-7)
  These bits indicate a request code.

21.2.4. wValueLSB Set-up register (WVALUELSB)

Address: 0x4100_4008
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its thrid byte is stored in this register. This is the lower byte of 2-byte data.

21.2.5. wValueMSB Set-up register (WVALUEMSB)

Address: 0x4100_400C
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its fourth byte is stored in this register. This is the upper byte of 2-byte data.

21.2.6. wIndexLSB Set-up register (WINDEXLSB)

Address: 0x4100_4010
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its fifth byte is stored in this register. This is the lower byte of 2-byte data.

21.2.7. wIndexMSB Set-up register (WINDEXMSB)

Address: 0x4100_4014
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its sixth byte is stored in this register. This is the upper byte of 2-byte data.

21.2.8. wLengthLSB Set-up register (WLENGTHLSB)

Address: 0x4100_4018
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its seventh byte is stored in this register. This is the lower byte of 2-byte data.

21.2.9. wLengthMSB Set-up register (WLENGTHMSB)

Address: 0x4100_401C
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  The 8-byte set-up data, which is transmitted from the host during the set-up stage of control transfer, is automatically received by this block, and its eighth byte is stored in this register. This is the upper byte of 2-byte data.

21.2.10. Device address register (DVCADR)

Address: 0x4100_4080
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

Note:
*: The D7 bit is fixed to “0”; writing “1” is thus invalid.

[Description of Bits]

- **D[6:0]** (bits 0-6)
  The CPU writes into this register the device address provided by the SET_ADDRESS request from the host. Thereafter, this block judges the specified address of a token from the host, and operates so that only the token packet transmitted to this device address is processed by this device.

21.2.11. Interrupt Status Register 1 (INTSTAT1)

Address: 0x4100_4084
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D7	D6	D5	D4	D3	D2	D1	D0
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Register]
If any of the interrupts occurs, the corresponding status bit is set to "1".The status is cleared by writing "1" into the status bit itself.

[Description of Bits]

- **D0** (bit 0)
  This bit indicates set-up ready interrupt status.

D0	Description
0	No set-up ready interrupt
1	Set-up ready interrupt

- **D1** (bit 1)
  This bit indicates EP1 packet ready interrupt status.

D1	Description
0	No EP1 packet ready interrupt
1	EP1 packet ready interrupt

- **D2** (bit 2)
  This bit indicates EP2 packet ready interrupt status.

D2	Description
0	No EP2 packet ready interrupt
1	EP2 packet ready interrupt

- **D3** (bit 3)
  This bit indicates EP3 packet ready interrupt status.

D3	Description
0	No EP3 packet ready interrupt
1	EP3 packet ready interrupt

- **D4** (bit 4)
  This bit indicates EP4 packet ready interrupt status.

D4	Description
0	No EP4 packet ready interrupt
1	EP4 packet ready interrupt

- **D5** (bit 5)
  This bit indicates EP5 packet ready interrupt status.

D5	Description
0	No EP5 packet ready interrupt
1	EP5 packet ready interrupt

- **D6** (bit 6)
  This bit indicates EP0 receive packet ready interrupt status.

D6	Description
0	No EP0 receive packet ready interrupt
1	EP0 receive packet ready interrupt

- **D7** (bit 7)
  This bit indicates EP0 transmit packet ready interrupt status.

D7	Description
0	No EP0 transmit packet ready interrupt
1	EP0 transmit packet ready interrupt

21.2.12. Interrupt Status Register 2 (INTSTAT2)

Address: 0x4100_4088
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D4	D3	D2	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Register]
If any of the interrupts occurs, the corresponding status bit is set to "1". The status is cleared by writing "1" into the status bit itself.

[Description of Bits]

- **D0** (bit 0)
  This bit indicates SOF interrupt status.

D0	Description
0	No SOF interrupt
1	SOF interrupt

- **D1** (bit 1)
  This bit indicates USB bus reset assert interrupt status.

D1	Description
0	No USB bus reset assert interrupt
1	USB bus reset assert interrupt

- **D2** (bit 2)
  This bit indicates USB bus reset de-assert interrupt status.

D2	Description
0	No USB bus reset de-assert interrupt
1	USB bus reset de-assert interrupt

- **D3** (bit 3)
  This bit indicates device suspended state interrupt status.

D3	Description
0	No device suspended state interrupt
1	device suspended state interrupt

- **D4** (bit 4)
  This bit indicates device awake state interrupt status.

D4	Description
0	No device awake state interrupt
1	device awake state interrupt

21.2.13. Interrupt Enable Register 1 (INTENBL1)

Address: 0x4100_4090
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D7	D6	D5	D4	D3	D2	D1	D0
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Register]
This register is used to set notification of interrupt when an interrupt source occurs. When the interrupt disable is set, no notification of interrupt is issued even if the corresponding interrupt occurs.

[Description of Bits]

- **D0** (bit 0)
  This bit indicates set-up ready interrupt status.

D0	Description
0	Disables set-up ready interrupt
1	Enables set-up ready interrupt

- **D1** (bit 1)
  This bit indicates EP1 packet ready interrupt enable.

D1	Description
0	Disables EP1 packet ready interrupt
1	Enables EP1 packet ready interrupt

- **D2** (bit 2)
  This bit indicates EP2 packet ready interrupt enable.

D2	Description
0	Disables EP2 packet ready interrupt
1	Enables EP2 packet ready interrupt

- **D3** (bit 3)
  This bit indicates EP3 packet ready interrupt enable.

D3	Description
0	Disables EP3 packet ready interrupt
1	Enables EP3 packet ready interrupt

- **D4** (bit 4)
  This bit indicates EP4 packet ready interrupt enable.

D4	Description
0	Disables EP4 packet ready interrupt
1	Enables EP4 packet ready interrupt

- **D5** (bit 5)
  This bit indicates EP5 packet ready interrupt enable.

D5	Description
0	Disables EP5 packet ready interrupt
1	Enables EP5 packet ready interrupt

- **D6** (bit 6)
  This bit indicates EP0 receive packet ready interrupt enable.

D6	Description
0	Disables EP0 receive packet ready interrupt
1	Enables EP0 receive packet ready interrupt

- **D7** (bit 7)
  This bit indicates EP0 transmit packet ready interrupt enable.

D7	Description
0	Disables EP0 transmit packet ready interrupt
1	Enables EP0 transmit packet ready interrupt

21.2.14. Interrupt Enable Register 2 (INTENBL2)

Address: 0x4100_4094
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D4	D3	D2	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Register]
This register is used to set notification of interrupt when an interrupt source occurs. When the interrupt disable is set, no notification of interrupt is issued even if the corresponding interrupt occurs.

[Description of Bits]

- **D0** (bit 0)
  This bit indicates SOF interrupt status.

D0	Description
0	Disables SOF interrupt
1	Enables SOF interrupt

- **D1** (bit 1)
  This bit indicates USB bus reset assert interrupt enable.

D1	Description
0	Disables USB bus reset assert interrupt
1	Enables USB bus reset assert interrupt

- **D2** (bit 2)
  This bit indicates USB bus reset de-assert interrupt enable.

D2	Description
0	Disables USB bus reset de-assert interrupt
1	Enables USB bus reset de-assert interrupt

- **D3** (bit 3)
  This bit indicates device suspended state interrupt enable.

D3	Description
0	Disables device suspended state interrupt
1	Enables device suspended state interrupt

- **D4** (bit 4)
  This bit indicates device awake state interrupt enable.

D4	Description
0	Disables device awake state interrupt
1	Enables device awake state interrupt

21.2.15. Isochronous (ISO) Mode Selection Register (ISOMODESEL)

Address: 0x4100_40B0
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D5	D4	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Register]
This register is enabled when the applicable EP has been configured for ISO IN transfer. Specify the switching of two sides of each FIFO for EP4 and EP5 as well as the timing to clear the FIFOs.
This register references the above bit at the timing when this block has received an SOF, and then performs the applicable operation. If EP4 and EP5 have been configured for other than ISO IN transfer, the setting of this bit is ignored.

[Description of Bits]
- **D4** (bit 4)
  This bit indicates EP4ISO mode select.

D4	Description
0	Executes the switching of two sides of a FIFO for each SOF reception, and clears the FIFO.
1	Executes the switching of two sides of a FIFO and clears the FIFO only if an IN token for each EP has been transmitted from the host in the preceding frame.

- **D5** (bit 5)
  This bit indicates EP5ISO mode select.

D5	Description
0	Executes the switching of two sides of a FIFO for each SOF reception, and clears the FIFO.
1	Executes the switching of two sides of a FIFO and clears the FIFO only if an IN token for each EP has been transmitted from the host in the preceding frame.

21.2.16. Frame Number Register LSB (FRAMELSB)

Address: 0x4100_40B4
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  This register is valid when an endpoint for isochronous transfer is included. When the start of frame (SOF) packet has been transmitted from the host, this block automatically writes it into FRAMELSB and FRAMEMSB.

21.2.17. Frame Number Register MSB (FRAMEMSB)

Address: 0x4100_40B8
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[2:0]		
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read.

[Description of Bits]

- **D[2:0]** (bits 0-2)
  This register is valid when an endpoint for isochronous transfer is included. When the start of frame (SOF) packet has been transmitted from the host, this block automatically writes it into FRAMELSB and FRAMEMSB.

21.2.18. System Control Register (SYSCON)

Address: 0x4100_40BC
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D4	D3	D2	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	W	R/W	R/W	R/W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Bits]

- **D0** (bit 0)
  This bit is used to set a software reset.
  When "1" is written in this bit, system reset is executed for the USB module.
  This is functionally the same as a hardware reset.
  This bit itself remains as "0."
  Note:
  Write-only bit. When this bit is read, the read value is always "0".

- **D1** (bit 1)
  This bit is used to set the power-down mode.
  When this bit is "0," the clock oscillation in the USB module does not stop even if suspended.
  When this bit is set to"1," the clock oscillation in the USB module stops if suspended and the power saving state is activated.

D1	Description
0	No power saving at suspend
1	Power saving at suspend

- **D2** (bit 2)
  This bit is used to set the EP mode.
  When this bit is "0," the 6EP mode is set; when this bit is "1," the 5EP mode is set.

D2	Description
0	EP0 to EP5
1	EP0 to EP4

- **D3** (bit 3)
  This bit is used to control pull-up/pull-down of USB.
  Output as a PUCTL signal.

D3	Description
0	Pull-down
1	Pull-up

- **D4** (bit 4)
  This bit is used to control remote wake-up.
  When "1" is written in this bit, remote wakeup is executed.
  This bit itself remains as "0."

D4	Description
1	Remote wake-up

Note:
Write-only bit. When this bit is read, the read value is always "0".

21.2.19. Polarity Select Register (POLSEL)

Address: 0x4100_40C0
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D4	–*2	–*2	–*2	–*2
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.
*2: Writing to the bits 0-3 does not affect the operation. These bits are not useable.

[Description of Bits]

- **D4** (bit 4)
  This bit indicates the polarity of the interrupt signal from the USB module to the CPU.
  In this LSI, always fix this bit to "0" (active "Low").

D4	Description
0	Active Low
1	Active High

21.2.20. Oscillation Test Register (OSCTEST)

Address: 0x4100_40E8
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D2	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Bits]

- **D0** (bit 0)
  This is a register setting enable bit for the single end receiver enable signal of the USB pin. When this bit is set to “1”, the single end receiver can be forced to power-down mode by setting the D1 bit to “0”. The LSI goes to normal mode when “0” is written to this bit. Set this bit to “0” whenever USB is used.

- **D1** (bit 1)
  This bit is enabled only when the D0 and D2 bits are set to “1”.

  - The single end receiver or the differential input receiver can forcibly be set to power-down mode by writing “0” to this bit.
  - The single end receiver or the differential input receiver can forcibly be set to the enable state by writing “1” to this bit.

- **D2** (bit 2)
  This bit is a register setting enable bit for the differential input receiver enable signal of the USB pin. When this bit is set to “1”, the differential input receiver can be forced to power-down mode by setting the D1 bit to “0”. The LSI goes to normal mode when “0” is written to this bit. Set this bit to “0” whenever USB is used.

21.2.21. Transmit Clock Control Register (TXCLKCONT)

Address: 0x4100_40FC
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D0
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.
Always fix this register to “0”. When a value other than “0” is written, operation is not guaranteed.

[Description of Bits]

- **D0** (bit 0)
  This bit is used to select the clock to transmit the USB data to be supplied to the USB module in the LSI.
  Always set this register to “0” in this LSI.

21.2.22. EP0 Configuration Register (EP0CONF)

Address: 0x4100_4100
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D4	–*	–*	D[1:0]	
Access	–	–	–	–	–	–	–	–	–	–	–	R	–	–	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Bits]

- **D[1:0]** (bits 0-1)
  This bit indicates a transfer type. This bit is fixed to “00b” since EP0 is preset for control transfer.
  This bit cannot be written from the CPU.

- **D4** (bit 4)
  The configuration bit of EP0 is set to “1” by a USB bus reset.
  When this bit is “1,” data transmitted from the host to this endpoint can be received, and data can be transmitted from this endpoint to the host.
  When this bit is “0,” no action is taken to transactions aimed at this EP. This bit cannot be written from the CPU.

D4	Description
0	No action is taken to transactions aimed at this EP.
1	Data transmitted from the host to this endpoint can be received, and data can be transmitted from this endpoint to the host.

Note:
Read-only bit.

21.2.23. EPn Configuration Register (EPnCONF: n = 1 to 5)

Address: 0x4100_4104 (n=1)
Address: 0x4100_4108 (n=2)
Address: 0x4100_410C (n=3)
Address: 0x4100_4110 (n=4)
Address: 0x4100_4114 (n=5)
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D7	–*	–*	D4	–*	–*	D[1:0]	
Access	–	–	–	–	–	–	–	–	R/W	–	–	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Bits]

- **D[1:0]** (bits 0-1)
  These bits indicate a transfer type. Only EP4 and EP5 can be set for isochronous transfer.

D[1:0]	Description
00	Prohibited *1
01	EP1, 2, 3: Prohibited *2 EP4, 5: Isochronous transfer
10	Bulk transfer
11	Interrupt transfer

Note:
*1 Since operation is not guaranteed when USB communication is started with this setting, do not set these bits to "00b".
*2 Since EP1, 2, 3 do not support isochronous transfer, do not set these bits to "01b".

- **D4** (bit 4)
  Configuration bit.
  If a set configuration request for making that EP active has been received from the host, write "1" from the CPU in the status stage of control transfer.
  When this bit is "1," data transmission/reception between the host and an EP becomes possible.
  When this bit is "0," no action is taken to transactions executed to this EP.

D4	Description
0	No action is taken to transactions executed to an EP.
1	Data transmission/reception between the host and an EP becomes possible.

- **D7** (bit 7)
  This bit is used to set the data transfer direction of an EP.

D7	Description
0	Receive
1	Transmit

21.2.24. EP0 Control Register (EP0CONT)

Address: 0x4100_4120
Access: R/W
Access size: 32 bits
Initial value:Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D4	–*	–*	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	R	–	–	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	Un-defined	0	0	Un-defined	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Bits]

- **D0** (bit 0)
  Stall bit.
  If a packet with a byte count that exceeds the maximum packet size described in EP0PLD (or EOP loss) is received during EP0 reception (in the data stage of control write transfer), this block automatically sets this bit to “1.” This bit is automatically reset to “0” after receiving a setup packet.

D0	Description
0	Within the maximum packet size
1	Byte count that exceeds the maximum packet size

- **D1** (bit 1)
  Data sequence toggle bit for reception.
  This block automatically performs synchronization by using the data sequence toggle mechanism.

  Note:
  Write operation to this bit is invalid.

- **D4** (bit 4)
  Data sequence toggle bit for transmission.
  This block automatically performs synchronization by using the data sequence toggle mechanism.

  Note:
  Write operation to this bit is invalid.

21.2.25. EPn Control Register (EPnCONT: n = 1 to 5)

Address: 0x4100_4124 (n=1)
Address: 0x4100_4128 (n=2)
Address: 0x4100_412C (n=3)
Address: 0x4100_4130 (n=4)
Address: 0x4100_4134 (n=5)
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*Note	D2	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.
*Note: Writing of a value other than "0" is prohibited. Operation is not guaranteed when a value other than "0" is written.

[Description of Bits]

- **D0** (bit 0)
  Stall bit.
  If a packet with a byte count that exceeds the maximum packet size described in EPnPLD (or EOP loss) is received during EPn reception, this block automatically sets this bit to "1."
  It can be cleared by writing "0" in this bit.

D0	Description
0	Clear
1	Byte count that exceeds the maximum packet size

- **D1** (bit 1)
  Data sequence toggle bit.
  This bit is reset when "1" is written in this bit.
  When initializing an EP, write "1" in this bit, reset the toggle bit of the data packet, and specify the PID of DATA0 (this bit is also set to "0.").
  The subsequent synchronous operation by using the data sequence toggle mechanism is automatically performed.

- **D2** (bit 2)
  FIFO clear bit.
  This bit is valid only when an EP has been set for transmission by the EP control register.
  When "1" is written into this bit, the transmit FIFO of that EP is cleared.
  The transmit FIFO is cleared when a clear operation is instructed in time for transmission, and the read value (EP clear status) is set to "0." However, if a transmission has already been started when a clear operation is instructed, the EP clear status stays "1" until the transmission finishes.
  In this case, the local host cannot access that EP until the EP clear status is set to "0."

21.2.26. EP0 Payload Register (EP0PLD)

Address: 0x4100_4140
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*			D[5:0]			
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Bits]

- **D[5:0]** (bits 0-5)
  These bits indicate the maximum packet size.
  Because the FIFO for EP0 is 32 bytes in this block, do not set a value larger than 20h in the bMaxPacketSize0 byte of the device descriptor.
  If data with a byte count that exceeds the maximum packet size set in this register is received, the stall bit of the EP0 status register is asserted and stall is returned to the host.

21.2.27. EPn Payload Register (EPnPLD: n = 1, 2)

Address: 0x4100_4144(n=1)
Address: 0x4100_4148(n=2)
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[6:0]						
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Bits]

- **D[6:0]** (bits 0-6)
  These bits indicate the maximum packet size.
  Write the wMaxPacketSize value of the endpoint descriptor selected by the Set_Configuration request of the host into this register from the CPU.
  Specify in byte units the packet size of packets other than short packets.
  If an EP is set for reception, when the EP receives data with a byte count that exceeds the maximum packet size set in this register, the receive packet ready is not asserted, the stall bit is set by an EOP, and stall handshake is returned to the host.
  On the other hand, if an EP is set for transmission, the contents of this register are ignored.

21.2.28. EP3 Payload Register (EP3PLD)

Address: 0x4100_414C
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Bits]

- **D[5:0]** (bits 0-5)
  These bits indicate the maximum packet size.
  Write the wMaxPacketSize value of the endpoint descriptor selected by the Set_Configuration request of the host into this register from the CPU.
  Specify in byte units the packet size of packets other than short packets.
  Since the FIFO is 32 bytes, set a value of 20h (32 bytes) or smaller.
  If an EP3 is set for reception, when the EP receives data with a byte count that exceeds the maximum packet size set in this register, the receive packet ready is not asserted, the stall bit is set by an EOP, and stall handshake is returned to the host.
  If EP3 is used for transmission, the contents of this register are ignored.

21.2.29. EPm Payload Register (EPmPLD: m = 4, 5)

Address: 0x4100_4150(m=4)
Address: 0x4100_4154(m=5)
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D7*1	D6	D5	D4	D3	D2	D1	D0
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.
*1: EP4PLD is D[7:0]. EP5PLD is D[6:0].

[Description of Bits]

- **D[7:0]** (bits 0-7): EP4PLD
- **D[6:0]** (bits 0-6): EP5PLD

  These bits indicate the maximum packet size.
  Write the wMaxPacketSize value of the endpoint descriptor selected by the Set_Configuration request of the host into this register from the CPU.
  Specify in byte units the size of packets other than short packets.
  If an EP is set for reception, when the EP receives data with a byte count that exceeds the maximum packet size set in this register, the receive packet ready is not asserted, the stall bit is set by an EOP, and stall handshake is returned to the host.
  If EPm is used for transmission, the contents of this register are ignored.

21.2.30. EP0 Receive Byte Counter (EP0RXCNT)

Address: 0x4100_4160
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[5: 0]					
Access	–	–	–	–	–	–	–	–	–	–	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Bits]

- **D[5:0]** (bits 0-5)
  This block automatically counts the number of bytes of a packet currently receiving. In the case of a full packet, only the number of bytes up to the maximum packet size described in the payload register is counted. However, in the case of a short packet, the number of bytes to be counted will be less. The CPU references this value, and reads one packet of data from the EP0 receive FIFO.
  The EP0RXCNT is cleared under following conditions:

  1. When the CPU has reset EP receive packet ready.
  2. When a set-up packet has been received.
  3. When the CPU has written “0” in the stall bit.

21.2.31. EPn Receive Byte Counter (EPnRXCNT: n = 1, 2)

Address: 0x4100_4164(n=1)
Address: 0x4100_4168(n=2)
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[6:0]						
Access	–	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Bits]

- **D[6:0]** (bits 0-6)
  This block automatically counts the number of bytes of a packet currently receiving. In the case of a full packet, only the number of bytes up to the maximum packet size described in the payload register is counted. However, in the case of a short packet, the number of bytes to be counted will be less. The CPU references this value, and reads one packet of data from the EP1 or EP2 receive FIFO.
  If the transfer direction of an EP has been set to the transmission side, this register is disabled.
  These registers are cleared under the following conditions:

  1. When an OUT token for EP1/2 is received.
  2. When the CPU has reset EP receive packet ready.
  3. When the CPU has written “0” in the stall bit.

21.2.32. EP3 Receive Byte Counter (EP3RXCNT)

Address: 0x4100_416C
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[5: 0]					
Access	–	–	–	–	–	–	–	–	–	–	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Bits]

- **D[5:0]** (bits 0-5)
  This block automatically counts the number of bytes of a packet currently receiving. In the case of a full packet, only the number of bytes up to the maximum packet size described in the payload register is counted. However, in the case of a short packet, the number of bytes to be counted will be less. The CPU references this value, and reads one packet of data from the EP3 receive FIFO.
  If the transfer direction of an EP3 has bee set to the transmission side, this register is disabled.
  This register is cleared under the following conditions:

  1. When an OUT token for EP3 is received.
  2. When the CPU has reset EP receive packet ready.
  3. When the CPU has written “0” in the stall bit.

21.2.33. EPm Receive Byte Counter (EPmRXCNT: m = 4, 5)

Address: 0x4100_4170 (m=4)
Address: 0x4100_4174 (m=5)
Access: R
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	D[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read.

[Description of Bits]

- **D[7:0]** (bits 0-7)
  This block automatically counts the number of bytes of a packet currently receiving. In the case of a full packet, only the number of bytes up to the maximum packet size described in the payload register is counted. However, in the case of a short packet, the number of bytes to be counted will be less. The CPU references this value, and reads one packet of data from the EP4 or EP5 receive FIFO.
  If the transfer direction of an EP has been set to the transmission side, this register is disabled.
  These registers are cleared under the following conditions:

  1. When an OUT token for EP4/5 is received.
  2. When the CPU has reset EP receive packet ready.
  3. When the CPU has written “0” in the stall bit.

21.2.34. EP0 Status Register (EP0STAT)

Address: 0x4100_4180
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D[5:4]		–*	D2	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read “0” when read. Write a “0” for write.

[Description of Bits]

- **D0** (bit 0)
  EP0 receive packet ready bit.
  This bit can be read from the CPU. This bit can be cleared by writing “1”.

  – Conditions for this bit = “1”:
    1) When data has been received by EP0 and stored in its FIFO.
    2) When a set-up packet has been received during control read or write transfer.
       When this bit is “1”, EP0 is locked.
       (A NAK is automatically returned when packet data has arrived from the host.)
  – Conditions for this bit = “0”:
    1) When the CPU has written “1” to this bit.
    2) When the CPU has reset the set-up ready bit during control write transfer.
       When this bit is “0”, EP0 is ready to receive data.

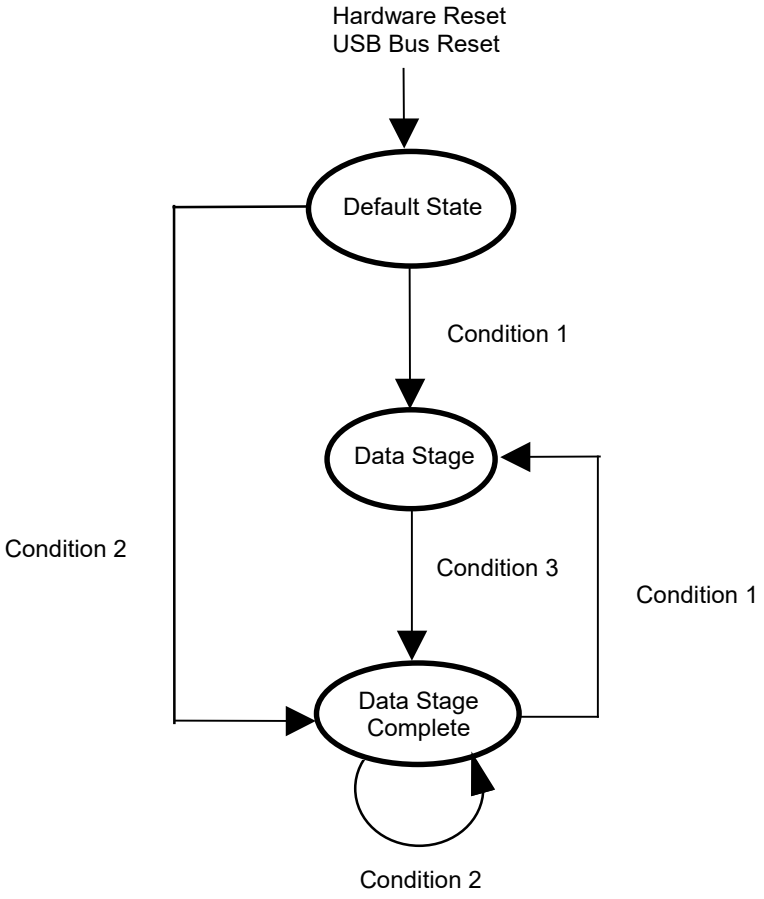
- **D1** (bit 1)
  EP0 transmit packet ready bit.
  This bit can be read from the CPU. This bit can be set to “1” by writing “1”.

  – Conditions for this bit = “1”:
    1) When the CPU has written “1” to this bit.
       When this bit is “1”, EP0 is ready to transmit data.
  – Conditions for this bit = “0”:
    1) When an ACK for data transmission from EP0 has been received from the host.
    2) When a set-up packet has been received.
       When this bit is “0”, EP0 is locked.
       (A NAK is automatically returned when an IN token has arrived from the host.)

- **D2** (bit 2)
  Set-up ready bit.
  When a set-up packet to be stored in the 8-byte set-up registers has arrived normally, this bit is automatically set and the EP0 receive FIFO is locked.
  If the D0 bit of INTENBL1 has been set to "1", the interrupt signal is automatically asserted when this bit is set.
  When the CPU finishes reading 8-byte set-up data, it must write "1" in this bit.
  By doing so, the set-up ready bit is reset, and the interrupt signal is also deasserted.
  The EP0 packet ready bit is also reset in the control write transfer mode, and then the lock is cancelled, enabling to receive packets at EP0 in the data stage.
  Note that the register value does not change even if "0" is written in this bit.

- **D[5:4]** (bits 4-5)
  These bits indicate EP0 stage.
  A stage transition during control transfer is displayed. The following shows a transition condition diagram among stages.

D[5:4]	Description
00	Default state
01	Data stage
10	Data stage complete



Condition 1: Receives a set-up packet in control read transfer or control write transfer mode.
Condition 2: Receives a set-up packet in non-data control transfer mode.
Condition 3: Receives a token (IN/OUT) in the flow direction opposite to that of data in the data stage.

Figure 21-2 Transition Condition Diagram among Stages

21.2.35. EPn Status Register (EPnSTAT: n = 1, 2, 4, 5)

Address: 0x4100_4184 (n=1)
Address: 0x4100_4188 (n=2)
Address: 0x4100_4190 (n=4)
Address: 0x4100_4194 (n=5)
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Register]
This register is enabled only when the corresponding EP has been set for bulk transfer or interrupt transfer.

[Description of Bits]

- **D0** (bit 0)
  EP1, 2, 4, 5 receive packet ready bit.
  This bit can be read from the CPU. This bit can be cleared by writing "1". Each of EP1, EP2, EP4, and EP5 has a dual-side FIFO configuration, and the packet ready bit is provided separately for each of sides A and B of the FIFO. The USB module automatically switches these two sides of the FIFO.

  – Conditions for this bit = "1":
    1) When a packet not containing an error in either side of A or B has been received.
       When this bit is "1", The EPn receive FIFO can be read from the CPU.
       When both sides A and B have received packet data, EPn is locked.
  – Conditions for this bit = "0":
    1) When the CPU has written "1" to this bit (both sides A and B have been reset).
       When this bit is "0", EPn is ready to receive data.

- **D1** (bit 1)
  EP1, 2, 4, 5 transmit packet ready bit.
  This bit can be read from the CPU. This bit can be set to "1" by writing "1". Each of EP1, EP2, EP4, and EP5 has a dual-side FIFO configuration, and the packet ready bit is provided separately for each of sides A and B of the FIFO. The USB module automatically switches these two sides of the FIFO.

  – Conditions for this bit = "1":
    1) When the CPU has written "1" to this bit and both sides A and B have been set.
       When this bit is "1" or either side A or B is set to "1", EPn is ready to transmit data.
  – Conditions for this bit = "0":
    1) When an ACK for data transmission to either side A or B has been received from the host.
  When neither side of A or B has data ready for transmission, EPn is locked.

Note:
If this bit is set when suspended, only one side is asserted. Note that the register value does not change even if “0” is written in this bit.

21.2.36. EP3 Status Register (EP3STAT)

Address: 0x4100_418C
Access: R/W
Access size: 32 bits
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	D1	D0
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note:
*: Reserved bit for future expansion. It will always read "0" when read. Write a "0" for write.

[Description of Register]
This register is enabled only when the corresponding EP has been set for bulk transfer or interrupt transfer.

[Description of Bits]

- **D0** (bit 0)
  EP3 receive packet ready bit.
  This bit can be read from the CPU. This bit can be cleared by writing "1".

  – Conditions for this bit = "1":
    1) When a packet not containing an error has been received.
       When this bit is "1", EP3 is locked.
  – Conditions for this bit = "0":
    1) When the CPU has written "1" to this bit.
       When this bit is "0", EP3 is ready to receive data.

- **D1** (bit 1)
  EP3 transmit packet ready bit.
  This bit can be read from the CPU. This bit can be set to "1" by writing "1".

  – Conditions for this bit = "1":
    1) When the CPU has written "1" to this bit.
       When this bit is "1", EP3 is ready to transmit data.
  – Conditions for this bit = "0":
    1) When an ACK for data transmission from EP3 has been received from the host.
       When this bit is "0", EP3 is locked.

21.2.37. EP0 transmit FIFO (EP0TXFIFO)

Address: 0x4100_41C0
Access: W
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  EP0 transmit data.
  EP0 transmit data can be written by writing the data to this address.
  Transmit data from the host in the data stage in control read transfer is stored in this register. When an EP0 transmit packet ready interrupt is requested from the USB module, the CPU writes transmit data to this address. Packet data can be sequenctially written by writing data consecutively.

  The EP0 transmit FIFO is cleared under the following conditions:

  1. When this block has received an ACK for data transmission from EP0 from the host.
  2. When a set-up packet has been received.

21.2.38. EP0 Receive FIFO (EP0RXFIFO)

Address: 0x4100_41E0
Access: R
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  EP0 receive data.
  Transmit data to the host in the data stage of control write transfer is stored in this register. When an EP0 receive packet ready interrupt is requested from this block, the CPU reads EP0 receive data by reading this address. Packet data can be read in sequence by reading receive data continuously.

  The EP0 receive FIFO is cleared under the following conditions:

  1. When the CPU has reset EP0 receive packet ready.
  2. When a set-up packet has been received.
  3. When the CPU has written “0” in the stall bit.

21.2.39. EP1 Transmit/Receive FIFO (EP1FIFO)

Address: 0x4100_41E4
Access: R or W
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  These bits are EP1 transmit data or EP1 receive data.
  The transfer direction of EP1 can be specified by setting the EP1 configuration register EP1CONF. The FIFO address of EP1 is common to both the transmit and receive directions.

  When EP1CONF(D7) = 0, the data transfer of EP1 is in the receive direction, and the EP1FIFO is read only.
  When EP1CONF(D7) = 1, the data transfer of EP1 is in the transmit direction, and the EP1FIFO is write only.

  If the transmission direction has been set, all bytes of the EP1 FIFO can be cleared by writing “1” in EP1CONT(D2).

21.2.40. EP2 Transmit/Receive FIFO (EP2FIFO)

Address: 0x4100_41E8
Access: R or W
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  These bits are EP2 transmit data or EP2 receive data.
  The transfer direction of EP2 can be specified by setting the EP2 configuration register EP2CONF. The FIFO address of EP2 is common to both the transmit and receive directions.

  When EP2CONF(D7) = 0, the data transfer of EP2 is in the receive direction, and the EP2FIFO is read only.
  When EP2CONF(D7) = 1, the data transfer of EP2 is in the transmit direction, and the EP2FIFO is write only.

  If the transmission direction has been set, all bytes of the EP2 FIFO can be cleared by writing “1” in EP2CONT(D2).

21.2.41. EP3 Transmit/Receive FIFO (EP3FIFO)

Address: 0x4100_41EC
Access: R or W
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  These bits are EP3 transmit data or EP3 receive data.
  The transfer direction of EP3 can be specified by setting the EP3 configuration register EP3CONF. The FIFO address of EP3 is common to both the transmit and receive directions.

  When EP3CONF(D7) = 0, the data transfer of EP3 is in the receive direction, and the EP3FIFO is read only.
  When EP3CONF(D7) = 1, the data transfer of EP3 is in the transmit direction, and the EP3FIFO is write only.

  If the transmission direction has been set, all bytes of the EP3 FIFO can be cleared by writing “1” in EP3CONT(D2).

21.2.42. EP4 Transmit/Receive FIFO (EP4FIFO)

Address: 0x4100_41F0
Access: R or W
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  These bits are EP4 transmit data or EP4 receive data.
  The transfer direction of EP4 can be specified by setting the EP4 configuration register EP4CONF. The FIFO address of EP4 is common to both the transmit and receive directions.

  When EP4CONF(D7) = 0, the data transfer of EP4 is in the receive direction, and the EP4FIFO is read only.
  When EP4CONF(D7) = 1, the data transfer of EP4 is in the transmit direction, and the EP4FIFO is write only.

  If the transmission direction has been set, all bytes of the EP4 FIFO can be cleared by writing “1” in EP4CONT(D2).

21.2.43. EP5 Transmit/Receive FIFO (EP5FIFO)

Address: 0x4100_41F4
Access: R or W
Access size: 32 bits
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol	D[31:16]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	D[15:0]															
Access	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW	RorW
Initial value	← Undefined →															

[Description of Bits]

- **D[31:0]** (bits 0-31)
  These bits are EP5 transmit data or EP5 receive data.
  In this block, either the 5EP mode that has five endpoints or the 6EP mode that has six endpoints can be selected according to the setting in the system control register SYSCON. For the 5EP mode, there are EP0 through EP4, but not EP5. For the 6EP mode, all of EP0 through EP5 are available.
  The transfer direction of EP5 can be specified by setting the EP5 configuration register EP5CONF. The FIFO address of EP5 is common to both the transmit and receive directions.

  When EP5CONF(D7) = 0, the data transfer of EP5 is in the receive direction, and the EP5FIFO is read only.
  When EP5CONF(D7) = 1, the data transfer of EP5 is in the transmit direction, and the EP5FIFO is write only.

  If the transmission direction has been set, all bytes of the EP5 FIFO can be cleared by writing “1” in EP5CONT(D2).

- Note on Read Access to EPnFIFO
  Three types of read access (bytes, half words, and words) are possible to the transmit/receive FIFOs.
  However, the following must be observed:

  Byte Access (8 bits) : Always possible.

  Half Word Access (16 bits) : If the data remaining in a FIFO is only one byte, it cannot be read by half word access. In this case, read only one byte by byte access.

  Word Access (32 bits) : If the data remaining in a FIFO is one to three bytes, it cannot be read by word access. In this case, read only remaining bytes using byte or half word access.

21.3. Description of Operation

21.3.1. USB Interface

This module handles the following functional components that make up the basis of the USB protocol. Therefore, the application side can focus on the processing of the functional parts that belong to applications.

- Bit synchronization
- Encoding/decoding of NRZI signal
- Generation and detection of Sync byte
- Bit stuffing
- Generation and inspection of CRCs (CRC5, CRC16)
- Encoding/decoding of PIDs (packet identifiers)
  1. Decoding of tokens
  2. Encoding and decoding of handshake packets
- Generation and detection of SOP
- Packetization and de-packetization
- Comparison of device addresses
- Storing of 8-byte set-up data from the host into the set-up registers
- Transmitting of data from the transmit FIFO
- Storing of receive data into the receive FIFO of the corresponding endpoint.

21.3.2. USB Transfer Mode

This module supports all of the four transfer modes, namely control transfer, interrupt transfer, bulk transfer, and isochronous transfer, defined in the USB standard.

(a) The control transfer mode is effective in receiving configurations and commands from the host, transmitting their responses, and exchanging status information between the host and peripherals.
(b) The bulk transfer mode enables the transfer of a large amount of data when the bandwidth of the USB bus becomes sufficient.
(c) The interrupt transfer mode is used when it is necessary to communicate a small amount of data less frequently but with a limited service cycle.
(d) The isochronous transfer mode is suitable for continuously transferring audio data and motion picture data in time series.

21.3.3. Endpoint and FIFO

This circuit allows selection of either the 5EP mode with five endpoints or the 6EP mode with six endpoints according to the settings in the register SYSCON. For EP0, a fixed transfer mode (i.e., control transfer) is used; for EP1, EP2 and EP3, either bulk transfer or interrupt transfer can be selected; and for EP4 and EP5, one of isochronous transfer, bulk transfer and interrupt transfer can be selected. Furthermore, for EP1 through EP5, the direction of data transfer is selectable.

Endpoint	5EP Mode			6EP Mode		
	FIFO Capacity (bytes)	Transfer Mode *1	Notes	FIFO Capacity (bytes)	Transfer Mode *1	Notes
EP0	Reception: 32 Transmission: 32	C	—	Reception: 32 Transmission: 32	C	—
EP1	64x2	B/Int (IN/OUT)		64x2	B/Int (IN/OUT)	
EP2	64x2	B/Int (IN/OUT)		64x2	B/Int (IN/OUT)	
EP3	32	B/Int (IN/OUT)	Rate	32	B/Int (IN/OUT)	
EP4	128x2 (64x2)	Iso/B/Int (IN/OUT)		64x2	Iso/B/Int (IN/OUT)	
EP5	—	—	—	64x2	Iso/B/Int (IN/OUT)	

*1 C = Control Transfer
B = Bulk Transfer
Int = Interrupt Transfer
Iso = Isochronous Transfer

21.3.4. Operation of Control Transfer

The control transfer mode consists of three stages.

(a) Set-up Stage
In this stage, a set-up token and 8-byte set-up data are transferred from the host. The USB module decodes the set-up token and automatically stores the 8-byte set-up data in the set-up registers. Once these operations finish normally, the USB module returns an ACK to the host.
The 8-byte set-up data consists of a standard request code defined in Section 9.3 of the USB standard, or a request code specific to each device class. Requests are decoded by the CPU side.

(b) Data Stage
If a request to be specified by 8-byte set-up data requires the transfer of parameter data from the host to a device, it is control write transfer; thus, an OUT token and data packet are transmitted from the host. Once the USB module receives them normally, it stores the parameter data in the EP0 receive FIFO and returns an ACK to the host.
If a request requires the transfer of parameter data from a device to the host, it is control read transfer, and the host will transfer an IN token. Therefore, the USB module transmits the parameter data already stored in the EP0 transmit FIFO that has been transmitted from the CPU. Once the host receives the parameter data normally, it returns an ACK to the USB module.
On the other hand, in the case of a request that does not contain parameter data to be transmitted or received, there is no data stage, and it proceeds directly to the status stage from the set-up stage.

(c) Status stage
The status stage is used to report the status of the request execution result from a device to the host. As the host sends an IN token to the USB module in control write transfer or non-data control transfer, this block returns a response. As the host sends an OUT token and zero-length data to the USB module in control read transfer, the USB module returns a response.

During the above control transfer, the CPU only needs to read/write the 8-byte set-up registers mapped at B770_0000H to B770_001CH, the EP0 transmit FIFO mapped at B770_01C0H, and the EP0 receive FIFO mapped at B770_01E0H according to the interrupt factor; all other operations are automatically performed by the USB module.

21.3.5. Data Packet Transmit/Receive Procedures of Bulk Transfer and Interrupt Transfer

The USB module of this LSI is normally used on the peripheral device side. If used in such a way, the USB module is connected with the host via a USB bus, and is also connected with a local microcontroller (CPU) inside a peripheral device via a parallel interface, etc.
Other than control transfer, data transfer is mainly performed. When transferring data packets between the USB module and the host, the following packet communication is performed via the USB bus for each transfer of one packet of data.

(a) Token packet transfer (IN token or OUT token) from the host to the USB module
(b) Data packet transfer in the target direction (from the host to a device, or from a device to the host)
(c) Handshake packet transfer in the direction opposite to the data packet direction

Once packet transfer is performed normally, an ACK packet is returned in the packet communication (c) above, and then it proceeds to the next packet transfer.
The USB module requests the CPU to transfer packet data by asserting the interrupt signal. Packet ready is used as an interrupt factor. The transmit packet ready interrupt requests to write packet data that needs to be transmitted into the transmit FIFO, and the receive packet ready interrupt requests to read the data that has been received and stored in the receive FIFO.
The following explains the procedures for transferring one packet of data both at transmission and reception.

1) At Transmission
   The CPU writes one packet of data that needs to be transmitted into the transmit FIFO of the USB module's corresponding EP, and sets the transmit packet ready bit in the USB module's corresponding EP status register. When the host has transmitted an IN token packet that specifies the communication method, etc. to the USB module, the USB module transmits the packet data stored in the transmit FIFO previously described to the host. Once the host has successfully received one packet of data, the host returns an ACK packet to the USB module. Then, the USB module resets the transmit packet ready bit, and completes one packet of USB transmission. When the transmit packet ready bit is reset, the USB module requests a transmit packet ready interrupt to the CPU and prompts to write the next packet of data.

2) At Reception
   The host transmits an OUT token to the USB module, immediately followed by a data packet. The USB module stores receive data in the receive FIFO of the corresponding EP. Once the USB module verifies that all packet data has been accumulated in the receive FIFO without any error, it returns an ACK packet to the host. At the same time, the USB module sets the receive packet ready bit in the corresponding EP status register, and requests an interrupt to the CPU. In response, the CPU reads the received data from the USB module, and resets the receive packet ready bit.

21.3.6. Data Packet Transmit/Receive Procedures of Isochronous Transfer

In isochronous transfer, the transfer of data is mainly performed. When transferring data packets between the USB module and the host, the following packet communication is performed via the USB bus for each transfer of one packet of data.

(a) Token packet transfer (IN token or OUT token) from the host to the USB module
(b) Data packet transfer in the target direction (from the host to a device, or from a device to the host)

In isochronous transfer, there is no handshaking to report whether or not packet transfer has been performed normally.
The USB module requests the CPU to transfer packet data by asserting the interrupt signal. SOF is used as an interrupt cause. As a result of this interrupt, the CPU writes packet data in the transmit FIFO for an EP set for transmission (ISO IN) in isochronous transfer, and reads data from the receive FIFO for an EP set for reception (ISO OUT) in isochronous transfer.
The following explains the procedures for transferring one packet of data both at transmission and reception.

1) At Transmission

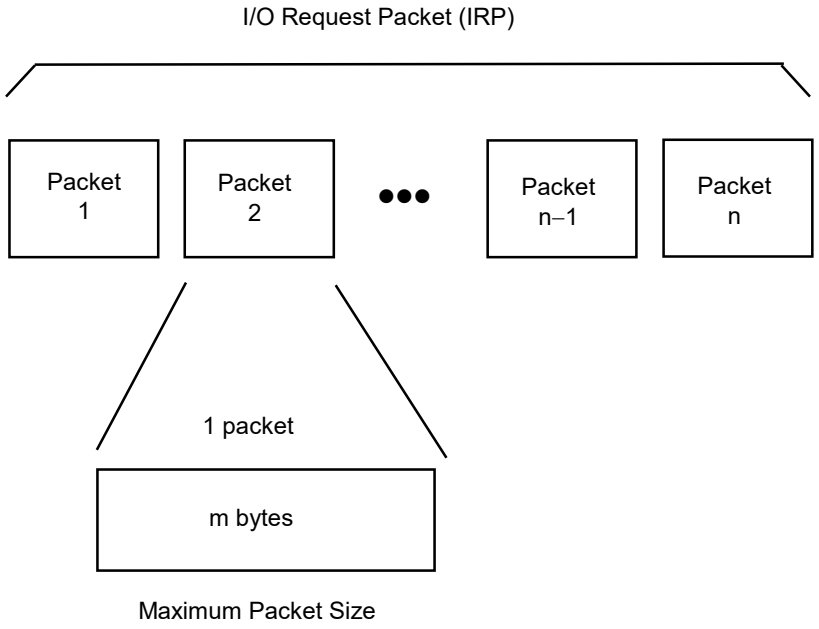
The EP for ISO IN has a dual-side FIFO configuration. One side of the FIFO stores packet data when the CPU writes packet data. The other side of the FIFO transmits the stored data to the USB bus when an IN token has been received. When an SOF packet is received, the roles of both FIFOs are swapped.
In response to an SOF interrupt, the CPU writes packet data, which needs to be transmitted in the next frame, into the transmit FIFO of the USB module's corresponding EP. When the host has transmitted an IN token packet to the USB module, the USB module transmits the packet data stored in the transmit FIFO of the previous frame to the host.

2) At Reception

The EP for ISO OUT has a dual-side FIFO configuration. One side of the FIFO outputs stored data when the CPU has read packet data. The other side of the FIFO stores a packet received from the USB bus. When an SOF packet is received, the roles of both FIFOs are swapped.
In response to an SOF interrupt, the CPU reads the packet data received in the previous frame from the receive FIFO of the USB module's corresponding EP. When the host has transmitted an OUT token packet and data packet to the USB module, the USB module stores that packet data in the receive FIFO, and that stored data is read by the CPU in the next frame.

21.3.7. Packets and Packet Size

This circuit packetizes transmit data and de-packetizes received data. A block of data that the software client must be aware of is a data group consisting of one or multiple packets, which is called an I/O request (IRP).
Among multiple packets of IRPs, all packets except the last packet are transferred in the maximum packet size. Only the last packet can be transferred in a size smaller than the maximum packet size; i.e., a short packet.



This circuit has a payload register for each endpoint, in which the maximum packet size of each endpoint can be set. The maximum packet size must be within the range of the corresponding FIFO capacity, and it must be

(1) 32 bytes or less for EP0 reception,
(2) 32 bytes or less for EP0 transmission,
(3) 64 bytes or less for EP1 transmission/reception,
(4) 64 bytes or less for EP2 transmission/reception,
(5) 32 bytes or less for EP3 transmission/reception,
(6) 64 bytes or less for EP4 bulk/interrupt transmission/reception,
    128 bytes or less for EP4 isochronous transfer in the 5EP mode,
    64 bytes or less for EP4 isochronous transfer in the 6EP mode,
(7) 64 bytes or less for EP5 bulk/interrupt transfer in the 6EP mode, and
    64 bytes or less for EP5 isochronous transfer in the 6EP mode.

A special signal state called an end of packet (EOP) is appended to the end of individual packets on the USB bus to identify the end of each packet. The USB module automatically appends EOPs at transmission, and detects and deletes EOPs at reception.

(1) Once the CPU has asserted the transmit packet ready bit after having written data the desired number of bytes into the transmit FIFO at transmission, it is considered as the end of a packet. An EOP is actually appended when data is transmitted to the USB bus that is executed after waiting for an IN token from the host. If the transmit packet ready bit is asserted after writing data the number of bytes without reaching the maximum packet size, that packet becomes a short packet. In particular, if the transmit packet ready bit has been asserted without writing any data, a null packet with zero data length can be created.

(2) If an EOP is detected in a data string, the USB module recognizes the end of a receiving packet and asserts the receive packet ready bit. The number of bytes of a packet received is automatically counted in the receive byte counter register that corresponds to each endpoint.

21.3.8. Interrupt

The USB module generates an interrupt to the CPU. Interrupt causes include

(a) Set-up ready for 8-byte set-up data
(b) EP0 receive packet ready
(c) EP0 transmit packet ready
(d) EP1 transmit/receive packet ready
(e) EP2 transmit/receive packet ready
(f) EP3 transmit/receive packet ready
(g) EP4 transmit/receive packet ready
(h) EP5 transmit/receive packet ready
(i) SOF
(j) USB bus reset assert
(k) USB bus reset de-assert
(l) Suspend
(m) Awake

There is only one source of interrupt by the USB module that can be recognized from the interrupt controller, but the CPU can identify the contents of an interrupt by referencing the interrupt status register 1 (INTSTAT1) and interrupt status register 2 (INTSTAT2). Also, these interrupts can be masked dynamically by individually setting the interrupt enable register 1 (INTENBL1) and interrupt enable register 2 (INTENBL2).
The following describes the interrupt causes, conditions and responses.
As for the behaviors of the set-up ready bit and packet ready bit, there are some special cases in which the USB module automatically operates in addition to those mentioned here. For more information, see the description of the EP0STAT to EP5STAT registers.

21.3.8.1. Set-up Ready Interrupt

Operation	Operation source	Description (conditions, response, etc.)
Set-up ready interrupt occurrence	USB module	When 8-byte set-up control data from the host has been normally received and stored into a group of the set-up registers, the set-up ready bit (D2 bit of EP0STAT) is asserted. At this time, if the D0 bit of INTENBL1 has been asserted, an interrupt is generated. → Firmware then becomes capable of reading a group of the set-up registers.
Set-up ready interrupt end	CPU (firmware)	When firmware reads 8-byte set-up data, write “1” in the D2 bit of the EP0 status register (EP0STAT). By writing “1” to the D2 bit, this bit is cleared to “0”. If new 8-byte set-up data is received in between, the interrupt is not cleared. In such a case, discard the set-up data that was in the process of reading, and read the new 8-byte set-up data.

21.3.8.2. EP0 Receive Packet Ready Interrupt

This interrupt is mainly used for data packet reception in control write transfer.

Operation	Operation source	Description (conditions, response, etc.)
EP0 receive packet ready interrupt occurrence	USB module	In control write transfer, when the set-up stage has changed to the data stage, this block has detected an EOP of a data packet, and data without any error has been stored in the EP0 receive FIFO, the EP0 receive packet ready bit (D0 bit of EP0STAT) is set to “1”. The arrival of an EOP is recognized as the end of a packet regardless of whether it is a full packet or short packet. At this time, if the EP0 receive packet ready interrupt enable bit (D6 bit of INTENBL1) is “1”, an interrupt is generated. (EOP: End Of Packet)
EP0 receive packet ready interrupt end	CPU (firmware)	In the case of EP0 reception, when EP0 receive FIFO data is read the number of bytes indicated in the EP0 receive byte counter (EP0RXCNT), write “1” in the EP0 receive packet ready bit (D0 bit of EP0STAT).

Note:
Short packet: A packet consisting of the number of bytes less than the maximum packet size

21.3.8.3. EP0 Transmit Packet Ready Interrupt

This interrupt is mainly used for data packet transmission in control read transfer.

Operation	Operation source	Description (conditions, response, etc.)
EP0 transmit packet ready interrupt occurrence	USB module	In control read transfer, when the set-up stage has changed to the data stage and the transmit data can be written in the FIFO, the EP0 transmit packet ready bit (D1 bit of EP0STAT) is set to “0”. At this time, if the EP0 transmit packet ready interrupt enable bit (D7 bit of INTENBL1) is “1”, an interrupt is generated. For the second and subsequent packets, in addition to this condition, no interrupt is generated unless an ACK response arrives from the host in response to the packet transmitted previously.
EP0 transmit packet ready interrupt end	CPU (firmware)	In the case of EP0 transmission, write one packet of EP0 transmit data in EP0TXFIFO, and then write “1” in the EP0 transmit packet ready bit (D1 bit of EP0STAT). As a result, the USB module is placed in a transmit enable state (i.e., it can transmit a data packet when an IN token arrives), and the interrupt is cleared at the same time. Although the write data count does not reach the maximum packet size, a packet becomes ready to be transmitted by writing “1” in the transmit packet ready bit. This supports the transmission of short packets.

21.3.8.4. Receive Packet Ready Interrupt (EP1, EP2, EP3, EP4 Bulk, EP5 Bulk)

This interrupt is generated when each EP receives valid packet data from the USB bus and the CPU becomes capable of reading that data.

Operation	Operation source	Description (conditions, response, etc.)
Receive Packet Ready interrupt occurrence	USB module	When this block has detected the EOP of a data packet at the time of data reception and data without any error has been stored in the FIFO, the receive packet ready bit (D0) in each corresponding EP status register (EPnSTAT) is set to “1”. At this time, if the corresponding packet ready interrupt enable bit is “1”, an interrupt is generated. (EOP: End Of Packet)
Receive packet ready interrupt end	CPU (firmware)	Once each EP receive FIFO data (EPnFIFO) is read the number of bytes indicated in each EP receive byte counter (EPnRXCNT), write “1” in the D0 bit of each EP status register (EPnSTAT). (Writing “1” means resetting.)

21.3.8.5. Transmit Packet Ready Interrupt (EP1, EP2, EP3, EP4 Bulk, EP5 Bulk)

This interrupt is generated when the CPU becomes capable of writing packet data that needs to be transmitted from each EP to the USB bus.

Operation	Operation source	Description (conditions, response, etc.)
Transmit packet ready interrupt occurrence	USB module	(1) Bulk Transfer, Interrupt Transfer If each EP has been set for transmission and it becomes possible to write transmit data in the FIFO, the transmit packet ready bit (D1 bit of EPnSTAT) of the corresponding EP is set to “0”. At this time, if the EP0 receive packet ready interrupt enable bit (D6 bit of INTENBL1) is “1”, an interrupt is generated. For the second and subsequent packets, no interrupt is generated unless an ACK response has been returned from the host in response to the previous packet.
Transmit packet ready interrupt end	CPU (firmware)	(1) Bulk Transfer, Interrupt Transfer Write transmit data in the transmit FIFO of each EP, and then write “1” in the EP transmit packet ready bit (D1 bit of EPnSTAT). As a result, data can be transmitted and the interrupt is cleared. Although the write data count does not reach the maximum packet size, a packet becomes ready to be transmitted by writing “1” in the transmit packet ready bit.

21.3.8.6. SOF Interrupt

Operation	Operation source	Description (conditions, response, etc.)
SOF interrupt occurrence	USB module	When an SOF packet has been detected on the USB bus.
SOF interrupt end	CPU (firmware)	When “1” has been written in the corresponding bit in the interrupt status register 2 (INTSTAT2).

21.3.8.7. USB Bus Reset Assert Interrupt

Operation	Operation source	Description (conditions, response, etc.)
USB bus reset assert interrupt occurrence	USB module	When the SE0 state has continued at least 2.5 μs on the DP or DM pin, this block automatically detects it. → Perform firmware processing corresponding to the bus reset.
USB bus reset assert interrupt end	CPU (firmware)	When "1" has been written in the corresponding bit in the interrupt status register 2 (INTSTAT2).

21.3.8.8. USB Bus Reset De-assert Interrupt

Operation	Operation source	Description (conditions, response, etc.)
USB bus reset de-assert interrupt occurrence	USB module	When the SE0 state of at least 2.5 μs has returned to the J state on the DP or DM pin. → Perform firmware processing corresponding to the bus reset.
USB bus reset de-assert interrupt end	CPU (firmware)	When "1" has been written in the corresponding bit in the interrupt status register 2 (INTSTAT2).

21.3.8.9. Suspended State Interrupt

Operation	Operation source	Description (conditions, response, etc.)
Suspended state interrupt occurrence	USB module	When the idle state has continued at least 3 ms on the DP or DM pin. → The internally generating clock of this block automatically stops 2 ms after the idle state has elapsed since the generation of this interrupt. Firmware can take a measure to set devices in low current consumption mode.
Suspended state interrupt end	CPU (firmware)	When "1" has been written in the corresponding bit in the interrupt status register 2 (INTSTAT2).

21.3.8.10. Awake Interrupt

Operation	Operation source	Description (conditions, response, etc.)
Awake interrupt occurrence	USB module	When a resume signal (SE0 state of approximately 1344 ns immediately after K state) has been detected on the DP or DM pin.
Awake interrupt end	CPU (firmware)	When "1" has been written in the applicable bit in the interrupt status register 2 (INTSTAT2).

21.3.9. Power Down

This LSI allows power down of the USB module and the USB transceiver according to the system used.

21.3.9.1. Power Down Modes and Settings

(1) Self Power Mode
When the idle state of the USB continues 5 ms, the oscillation of internal 12 MHz clock stops regardless of the suspend power-saving setting.

(2) Bus Power Mode (Suspend Power Saving)
When the D1 bit of the system control register (SYSCON) is set to “1” and the idle state of the USB continues 5 ms, the oscillation of the internal 12 MHz clock stops and the USB transceiver block shifts to power-down mode.

(3) Power Down Setting of Single-End Receivers
When the D0 bit of the oscillation test register (OSCTEST) is set to “1”, the power down signal of the single-end receiver can be controlled forcibly with the D1 bit, allowing setting of power down.
For details, refer to the register specification of the OSCTEST register.

(4) Power Down Setting of Differential Input Receivers
When the D2 bit of the oscillation test register (OSCTEST) is set to “1”, the oscillation enable signal of the differential input receiver can be controlled forcibly with the D1 bit, allowing setting of power down.
For details, refer to the register specification of the OSCTEST register.

(5) Clock Disable Setting
This setting allows the stop of clock supply to the USB module in the LSI.
For details, see Chapter 5.

21.3.9.2. USB Suspend ⇔ Awake Operation

There are two types of awake operations from the suspend state: awaking with a resume signal from the USB host, and awaking by remote wake-up from the USB device side.

(1) Resuming from the host

Idle State
↓ (3ms)
Suspend Interrupt
↓ Cancel the interrupt (write “1” in the interrupt status bit)
Idle State
↓ (2 ms: 5 ms in total when 3 ms above is added)
Stop USB's internal clock (12 MHz). This enables the USB transceiver to shift to low-power mode.
↓
Resume signal from the host. (∗) Since the internal clock is stopped, the resume signal is detected asynchronously.
↓
The USB transceiver is in normal mode
Resume internal 12 MHz clock operation of the USB module.
After resuming the clock operation, execute resume interrupt by detecting the end of the resume signal (LS EOP).
↓
Normal data exchange between the host and the device can be executed.

(2) Resuming from a device

Idle State
↓ (3ms)
Suspend Interrupt
↓ Cancel interrupt (write “1” in the interrupt status bit)
Idle State
↓ (2 ms: 5 ms in total when 3 ms above is added)
Stop USB's internal clock (12 MHz). This causes the USB transceiver to shift to low-power mode.
↓ Write “1” in the remote wake-up bit from the CPU.
Resume internal CLK operation of the USB module. The USB transceiver shifts to normal mode (remote wake-up operation).
Transmit K state (DM/DP = L/H: 10 ms or more) on the USB bus at the same time
↓
Normal data exchange between the host and the device can be executed.

21.3.10. Operation of Dual-Side FIFO Configuration in Bulk Transfer

The FIFOs for EP1 and EP2 have a dual configuration of 64 bytes on each side. The FIFO for EP4 also has a dual configuration of 64 bytes on each side when allocated for bulk transfer. Therefore, it is possible to temporarily store up to 128 bytes of bulk transfer data.

(1) 2-Layer reception operation ("O" indicates the assert condition and "×" indicates deassert condition)

	In the case of 1→2→3→4→5a→6 In the case of 1→2→3→4→5b→6	Side A 64 bytes	Side B 64 bytes	Side A PKT RDY	Side B PKT RDY	EPn receive PKT RDY	Interrupt
1	Reception. Start storing data in side A.			×	×	×	×
2	Data of one packet has been stored.			○	×	○	○
3	Start reception and storing of data in side B.			○	×	○	○
4	CPU starts reading side A.			○	×	○	○
5a	When the storing of packet in side B is completed before the completion of reading side A			○	○	○	○
5b	When the reading of packet in side A is completed before the completion of storing data in side B.			×	×	×	×
6	From 5a: Side A has become empty. From 5b: Side B has become full.			×	○	○	○
7	CPU starts reading side B.			×	○	○	○

- When one packet of receive data is stored in side A of the FIFO and an EOP is received, the USB module asserts the EPn packet ready and then asserts the interrupt signal. This makes it possible for the CPU to read the received data.
- Subsequently, the USB module can receive data from the host, so it switches to side B of the FIFO in order to store data.
- Once the one packet of data mentioned previously has been read from side A of the FIFO, reset the EPn receive packet ready bit (by writing "1" in the D0 bit of EPnSTAT) from the CPU.
- If side B has not completed receiving data when the EPn receive packet ready is reset, the USB module resets the EPn receive packet ready bit, and deasserts the interrupt signal.
- If side B has completed receiving data when the EPn receive packet read bit is reset, the USB module denies the EPn receive packet ready reset request from the CPU, and maintains the state of the EPn receive packet ready bit ("1") and the assert state of the internal signal.

(2) 2-Side transmission operation ("O" indicates the assert condition and "×" indicates deassert condition)

	In the case of 1→2→3→4→5a→6 In the case of 1→2→3→4→5b→6	Side A 64 bytes	Side B 64 bytes	Side A PKT RDY	Side B PKT RDY	EPn transmit PKT RDY	Interrupt
1	Side A and side B are both empty.			×	×	×	○
2	CPU starts writing into side A.	■		×	×	×	○
3	Writing of one packet is completed.	■			×	×	○
4	While the data of side A is transmitted, the next packet is written in side B.	■	■	○	×	×	○
5a	When the writing in side B is completed before side A becomes empty.	■	■	○	○	○	×
5b	When side A becomes empty before the writing in side B is completed.		■	×	×	×	○
6	From 5a: Side A has become empty. From 5b: Side B has become full.		■	×	○	×	○
7	CPU starts transmission of side B.		■	×	○	×	○

- When the EPn transmit packet ready interrupt enable bit of INTENBL1 is set to "1", the EPn transmit packet ready interrupt is asserted if the transmit FIFO is empty and the EPn transmit packet ready bit is "0". This makes it possible to write transmit data in the EPn transmit FIFO.
- Once one packet of data has been written in side A of the FIFO, set the transmit packet ready bit (D1 bit of EPnSTAT) from the CPU. When the transmit packet ready bit is set, data can be transmitted to the host. Here, since side B is still empty, the interrupt signal still maintains the assert state and thus the next packet of data can be written in side B. In this case, although the D1 bit of EPnSTAT stays "0", the USB module recognizes that side A can make transmission, so the USB module starts transmission once it receives an IN token from the host.
- While transmitting data from side A to the USB bus, the CPU can write the next packet of transmit data into side B of the FIFO.
- When writing data to be transmitted to side B is completed, the CPU sets the transmit packet ready bit. Unless the transmission of side A has been completed up to this time (i.e., an ACK has been received from the host and the transmit packet ready bit has been reset), the interrupt signal is cleared. (The CPU cannot write the packet after the next packet.)
- If side A has been emptied and data has been transmitted normally before side B becomes possible to transmit, an ACK is returned from the host. In this case, since the interrupt signal is still in the assert state, and the CPU can write data into side A of the FIFO immediately after writing to side B.
- If side A has been emptied after continuous transmission of the data in side A from state 5a, an ACK is returned from the host when the transmission is completed normally. Therefore, the USB module asserts the interrupt signal, prompting writing of data into side A.

21.3.11. Error Processing and Retry Operation

1) Error Processing at Transmission

If errors such as a CRC error are detected in the data transmitted by the USB module, the host does not return an ACK packet. Therefore, the USB module does not reset the transmit packet ready bit, and stands by while retaining the current packet data. The current packet data is re-transmitted by the next IN token from the host.

2) Error Processing at Reception

If an error is found in the data received via the USB bus, the USB module neither asserts an interrupt signal to the CPU nor returns anything to the host (generates time-out).

The host recognizes the occurrence of an error from a time-out, so it can take an action such as re-transmission. In addition, because the host does not request an interrupt, the CPU does not read any data containing an error.

Chapter 22

Port

22. Port

22.1. PORT0

22.1.1. Overview

PORT0 is comprised of 6 bit input/output port (P00 to P05), and have not only an input/output port functin but also external interrupt, FTM, SSIO, UARTF, RC-ADC and SA-ADC function.
See the following chapters for reference.

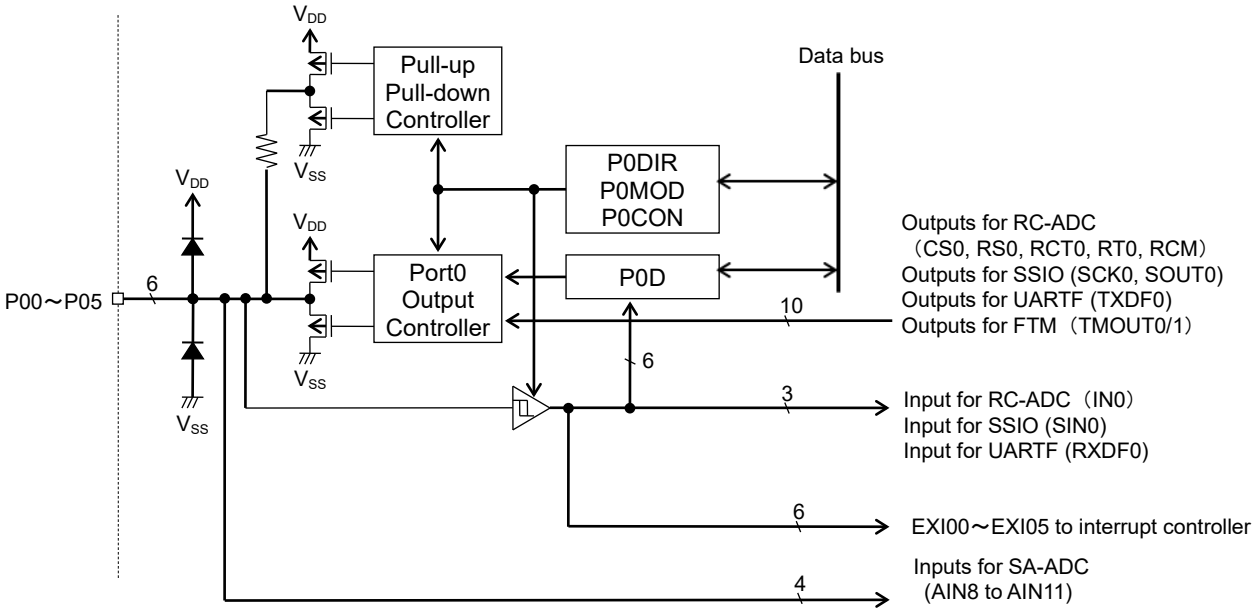
FTM	Chapter 11 "Function Timer(FTM)"
SSIO	Chapter 15 "Synchronous serial port (SSIO)"
UARTF	Chapter 18 "UART with FIFO(UARTF)"
RC-ADC	Chapter 25 "RC oscillation type A/D converter (RC-ADC)"
SA-ADC	Chapter 26 "Successive approximation type A/D converter (SA-ADC)"

22.1.1.1. Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resister,m or input with a pull-up resister for each bit in input mode.
- The external interrupt pins (EXI00, EXI01, EXI02, EXI03, EXI04, EXI05), FTM output pins (TMOUT0, TMOUT1), SSIO pins (SOUT0, SIN0, SCK0), UART with FIFO pins (RXDF0, TXDF0), RC-ADC oscillation pins (IN0, CS0, RS0, RCT0, RT0, RCM) and SA-ADC input pins (AIN8, AIN9, AIN10, AIN11) can be used as the secondary or the tertiary or the quaternary function.

22.1.1.2. Configuration

Figure 22-1 shows the configuration of the port 0.



P0D : Port 0 data register
P0DIR : Port 0 direction register
P0CON : Port 0 controll register
P0MOD : Port 0 mode register

Figure 22-1 Configuration of Port 0

22.1.1.3. List of Pins

Pin Name	I/O	Primary Function	Secondary Function	Tertiary Function	Quaternary Function
P00/EXI00/AIN8/ IN0/ SOUT0/ RXDF0	I/O	Input/output port / External Interrupt Input /SA-ADC Input (AIN8)	Oscillation wave form input (IN0) for RC-ADC	Synchronous serial output pin (SOUT0)	UART with FIFO input pin (RXDF0)
P01/EXI01/AIN9/ CS0/ SIN0/ TXDF0	I/O	Input/output port / External Interrupt Input / SA-ADC Input (AIN9)	Reference capacitor connection pin (CS0) for RC-ADC	Synchronous serial input pin (SIN0)	UART with FIFO output pin (TXDF0)
P02/EXI02/AIN10/ RCT0/ SCK0/ TMOUT0	I/O	Input/output port / External Interrupt Input / SA-ADC Input (AIN10)	Resistor/capacitor sensor connection pin (RCT0) for RC-ADC	Synchronous serial clock output pin (SCK0)	Functional timer output (TMOUT0)
P03/EXI03/AIN11/ RS0/ TMOUT1	I/O	Input/output port / External Interrupt Input /SA-ADC Input (AIN11)	Reference resistor connection pin (RS0) for RC-ADC	-	Functional timer output (TMOUT1)
P04/EXI04/ RT0	I/O	Input/output port / External Interrupt Input	Resistor sensor connection pin (RT0) for RC-ADC	-	-
P05/EXI05/ RCM	I/O	Input/output port / External Interrupt Input	RC oscillation monitor pin (RCM) for RC-ADC	-	-

22.1.2. Description of Registers

22.1.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4000	Port 0 data register	P0D	R/W	32	0x0000_0000
0x5C00_4004	Port 0 direction register	P0DIR	R/W	32	0x0000_0000
0x5C00_4008	Port 0 control register	P0CON	R/W	32	0x0000_0000
0x5C00_400C	Port 0 mode register	P0MOD	R/W	32	0x0000_0000

22.1.2.2. Port 0 Data Register (P0D)

Address: 0x5C00_4000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P0D[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P0D is a special function register (SFR) to set the value to be output to the Port 0 pin or to read the input level of the Port 0. In output mode, the value of this register is output to the Port 0 pin. The value written to P0D is readable. In input mode, the input level of the Port 0 pin is read when P0D is read. Output mode or input mode is selected by using the port 0 direction register (P0DIR) described later.

[Description of Bits]
- **P0D[5:0]** (bit 5 to 0)
  The P0D[5:0] bits are used to set the output value of the Port 0 pin in output mode and to read the pin level of the Port 0 pin in input mode.

P0D[n]	Description
0	Output or input level of the P0n pin: ”L”
1	Output or input level of the P0n pin: ”H”

n=0 to 5

22.1.2.3. Port 0 Direction Register (P0DIR)

Address: 0x5C00_4004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P0DIR[5:0]					
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P0DIR is a special function register (SFR) to select the input/output mode of Port 0.

[Description of Bits]
- **P0DIR[5:0]** (bit 5 to 0)
  The P0DIR[5:0] pins are used to set the input/output direction of the Port 0 pin.

P0DIR[n]	Description
0	P0n pin: Output (initial value)
1	P0n pin: Input

n=0 to 5

22.1.2.4. Port 0 Control Register (P0CON)

Address: 0x5C00_4008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P0CON5 [1:0]		–*	–*	P0CON4 [1:0]	
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P0CON3 [1:0]		–*	–*	P0CON2 [1:0]		–*	–*	P0CON1 [1:0]		–*	–*	P0CON0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P0CON is special function register (SFR) to select input/output state of the Port 0 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P0DIR register.

[Description of Bits]
- **P0CONn[1:0]** (n=0 to 5)
  The P0CONn[1:0] bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P0n pin	When output mode is selected (P0DIR[n] bit = “0”)	When input mode is selected (P0DIR[n] bit = “1”)
P0CONn[1:0]	Description	
00	P0n pin: High-impedance output (initial value)	P0n pin: High-impedance input
01	P0n pin: P-channel open drain output	P0n pin: Input with a pull-down resistor
10	P0n pin: N-channel open drain output	P0n pin: Input with a pull-up resistor
11	P0n pin: CMOS output	P0n pin: High-impedance input

n=0 to 5

22.1.2.5. Port 0 Mode Register (P0MOD)

Address: 0x5C00_400C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P0MOD5 [1:0]		–*	–*	P0MOD4 [1:0]	
Access	–	–	–	–	–	–	–	–	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P0MOD3 [1:0]		–*	–*	P0MOD2 [1:0]		–*	–*	P0MOD1 [1:0]		–*	–*	P0MOD0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P0MOD is a special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 0.

[Description of Bits]
- **P0MOD0[1:0]** (bit 1 to 0)
  The P0MOD0[1:0] bits are used to select the primary or secondary or tertiary or quaternary function of the P00 pin.

P0MOD0[1]	P0MOD0[0]	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	RC oscillation waveform input pin for RC-ADC (IN0)
1	0	SSIO data output (SOUT0)
1	1	UART with FIFO data input mode (RXDF0)

- **P0MOD1[1:0]** (bit 5 to 4)
  The P0MOD1[1:0] bits are used to select the primary or secondary or tertiary or quaternary function of the P01 pin.

P0MOD1[1]	P0MOD1[0]	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Reference capacitor connection pin for RC-ADC (CS0)
1	0	SSIO data input (SIN0)
1	1	UART with FIFO data output mode (TXDF0)

- **P0MOD2[1:0]** (bit 9 to 8)
  The P0MOD2[1:0] bits are used to select the primary or secondary or tertiary or quaternary function of the P02 pin.

P0MOD2[1]	P0MOD2[0]	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (RCT0)
1	0	SSIO clock input/output (SCK0)
1	1	FTM output (TMOUT0)

- **P0MOD3[1:0]** (bit 13 to 12)
  The P0MOD3[1:0] bits are used to select the primary or secondary or quaternary function of the P03 pin.

P0MOD3[1]	P0MOD3[0]	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Reference resistor connection pin for RC-ADC (RS0)
1	0	Prohibited
1	1	FTM output (TMOUT1)

- **P0MOD4[1:0]** (bit 17 to 16)
  The P0MOD4[1:0] bits are used to select the primary, secondary of the P04 pin.

P0MOD4[1]	P0MOD4[0]	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (RT0)
1	0	Prohibited
1	1	Prohibited

- **P0MOD5[1:0]** (bit 21 to 20)
  The P0MOD5[1:0] bits are used to select the primary or secondary function of the P05 pin.

P0MOD5[1]	P0MOD5[0]	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	RC oscillation monitor pin for RC-ADC (RCM)
1	0	Prohibited
1	1	Prohibited

[Note]
If any bit combination out of the above is set to “Prohibited” and the corresponding bit of the port 0 is sepecified to output mode (selected in port0 control register), status of corresponding pin is fixed, regardless the contents of Port0 register (P0D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to “L”
CMOS output mode: High-impedance: Fixed to “L”

The terminal state is not automatically replaced even if set P0MOD register. Perform appropriate setting in P0CON register.

22.1.3. Description of Operation

22.1.3.1. Input / Output Port Function

For each pin of Port 0, either output or input is selected by setting the Port 0 direction register (P0DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 0 control registers 0 and 1 (P0CON).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 0 control registers 0 and 1 (P0CON).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, “L” or “H” level is output to each pin of Port 0 depending on the value set by the Port 0 data register (P0D).
In input mode, the input level of each pin of Port 0 can be read from the Port 0 data register (P0D).

22.1.3.2. Primary Function Except for Input / Output Port

Port 0 is assigned to the SA-ADC input pins (AIN8, AIN9, AIN10, AIN11), External interrupts (EXI00, EXI01, EXI02, EXI03, EXI04, EXI05).
When used as the SA-ADC input pins, set the applicable port to the high impedance output state.
When used as the External interrupts, set the applicable port to the input state.

22.1.3.3. Secondary, Tertiary and Quaternary Functions

Secondary, tertiary and quaternary functions are assigned to Port 0 as the RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, RCT0, RCM), the SSIO pins (SIN0, SOUT0,SCK0), the UART with FIFO pins (RXDF0, TXDF0), FTM output pins(TMOUT0,TMOUT1). These pins can be used in a secondary or tertiary or quaternary function mode by setting the P0MODn[1:0] (n=0 to 5) bits of the Port 0 mode registers (P0MOD).
When used as the RC-ADC, set the P00 to P04 to the high impedance input state and P05 to CMOS output mode and RC-ADC mode.

22.2. PORT2

22.2.1. Overview

PORT2 is comprised of a 4 bit input/output port (P20 to P23), and have not only an input/output port functin but also external interrupt, FTM, SSIOF, RC-ADC and SA-ADC function.
See the following chapters for reference.

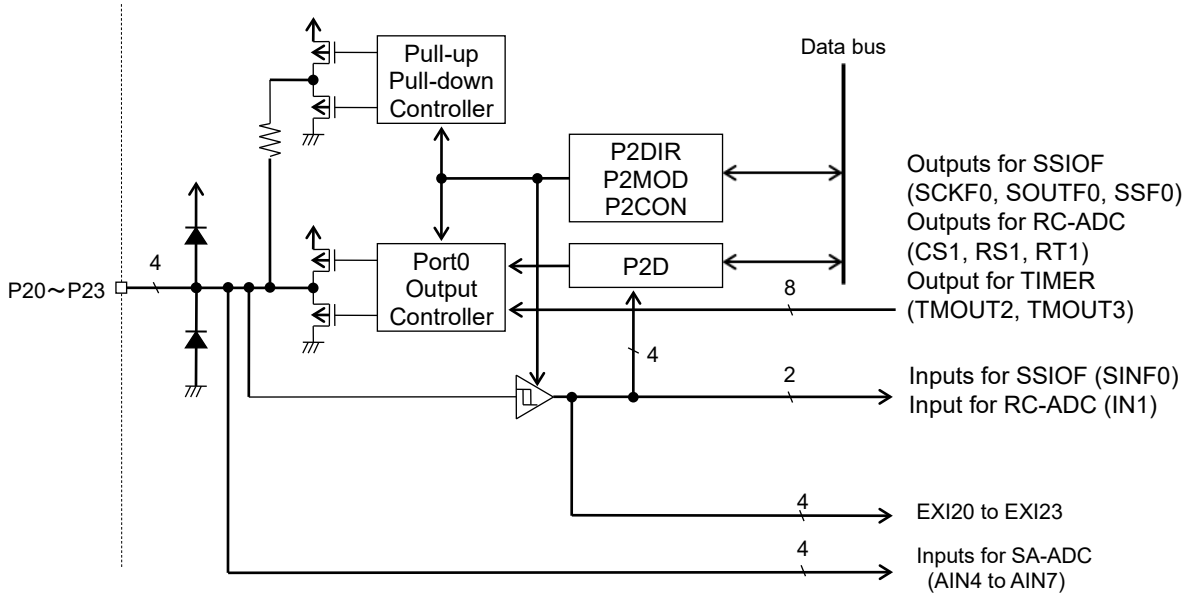
FTM	Chapter 11 "Function Timer(FTM)"
SSIOF	Chapter 16 " Synchronous serial port with FIFO (SSIOF)"
RC-ADC	Chapter 25 " RC oscillation type A/D converter (RC-ADC)"
SA-ADC	Chapter 26 " Successive approximation type A/D converter (SA-ADC)"

22.2.1.1. Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resister,m or input with a pull-up resister for each bit in input mode.
- The external interrupt pins (EXI20, EXI21, EXI22, EXI23), FTM output pins (TMOUT2, TMOUT3), SSIOF pins (SOUTF0, SINF0, SCKF0, SSF0), RC-ADC oscillation pins (IN1, CS1, RS1, RT1) and SA-ADC input pins (AIN4, AIN5, AIN6, AIN7) can be used as the secondary or the tertiary or the quaternary function.

22.2.1.2. Configuration

Figure 22-3 shows the configuration of the port 2.



P2D : Port 2 data register
P2DIR : Port 2 direction register
P2CON : Port 2 controll register
P2MOD : Port 2 mode register

Figure 22-2 Configuration of Port 2

22.2.1.3. List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quaternary function
P20/EXI20/AIN4/ IN1/ SOUTF0	I/O	Input/output port External interrupt SA-ADC AIN4	RC oscillation waveform input pin for RC-ADC IN1	SSIOF data output SOUTF0	-
P21/EXI21/AIN5/ CS1/ SINF0	I/O	Input/output port External interrupt SA-ADC AIN5	Reference capacitor connection pin for RC-ADC CS1	SSIOF data input SINF0	-
P22/EXI22/AIN6/ RS1/ SCKF0/ TMOUT2	I/O	Input/output port External interrupt SA-ADC AIN6	Reference resistor connection pin for RC-ADC RS1	SSIOF clock input/output SCKF0	FTM output TMOUT2
P23/EXI23/AIN7/ RT1/ SSF0/ TMOUT3	I/O	Input/output port External interrupt SA-ADC AIN7	Resistor sensor connection pin for measurement for RC-ADC RT1	SSIOF enable input/output SSF0	FTM output TMOUT3

22.2.2. Description of Registers

22.2.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4200	Port 2 data register	P2D	R/W	32	0x0000_0000
0x5C00_4204	Port 2 direction register	P2DIR	R/W	32	0x0000_0000
0x5C00_4208	Port 2 control register	P2CON	R/W	32	0x0000_0000
0x5C00_420C	Port 2 mode register	P2MOD	R/W	32	0x0000_0000

22.2.2.2. Port 2 Data Register (P2D)

Address: 0x5C00_4200
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P2D[3:0]			
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P2D is a special function register (SFR) to set the value to be output to the Port 2 pin or to read the input level of the Port 2. In output mode, the value of this register is output to the Port 2 pin. The value written to P2D is readable. In input mode, the input level of the Port 2 pin is read when P2D is read. Output mode or input mode is selected by using the port mode register (P2DIR) described later.

[Description of Bits]
- **P2D[3:0]** (bit 3 to 0)
  The P2D[3:0] bits are used to set the output value of the Port 2 pin in output mode and to read the pin level of the Port 2 pin in input mode.

P2D[n]	Description
0	Output or input level of the P2n pin: ”L”
1	Output or input level of the P2n pin: ”H”

n=0 to 3

22.2.2.3. Port 2 Direction Register (P2DIR)

Address: 0x5C00_4204
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P2DIR[3:0]			
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P2DIR is a special function register (SFR) to select the input/output mode of Port 2.

[Description of Bits]
- **P2DIR[3:0]** (bit 3 to 0)
  The P2DIR[3:0] bits are used to set the input/output direction of the Port 2 pin.

P2DIR[n]	Description
0	P2n pin: Output (initial value)
1	P2n pin: Input

n=0 to 3

22.2.2.4. Port 2 Control Register (P2CON)

Address: 0x5C00_4208
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P2CON3 [1:0]		–*	–*	P2CON2 [1:0]		–*	–*	P2CON1 [1:0]		–*	–*	P2CON0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P2CON is a special function register (SFRs) to select input/output state of the Port 2 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P2DIR register.

[Description of Bits]
- **P2CONn[1:0]** (n=0 to 3)
  The P2CONn[1:0] bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P2n pin	When output mode is selected (P2DIR[n] bit = “0”)	When input mode is selected (P2DIR[n] bit = “1”)
P2CONn[1:0]	Description	
00	P2n pin: High-impedance output (initial value)	P2n pin: High-impedance input
01	P2n pin: P-channel open drain output	P2n pin: Input with a pull-down resistor
10	P2n pin: N-channel open drain output	P2n pin: Input with a pull-up resistor
11	P2n pin: CMOS output	P2n pin: High-impedance input

n=0 to 3

22.2.2.5. Port 2 Mode Register (P2MOD)

Address: 0x5C00_420C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P2MOD3 [1:0]		–*	–*	P2MOD2 [1:0]		–*	–*	P2MOD1 [1:0]		–*	–*	P2MOD0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P2MOD is a special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 2.

[Description of Bits]
- **P2MOD0[1:0]** (bit 1 to 0)
  The P2MOD0[1:0] bits are used to select the primary, secondary, or tertiary function of the P20 pin.

P2MOD0[1]	P2MOD0[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	RC oscillation waveform input pin for RC-AD (IN1)
1	0	SSIOF data output (SOUTF0)
1	1	Prohibited

- **P2MOD1[1:0]** (bit 5 to 4)
  The P2MOD1[1:0] bits are used to select the primary, secondary, or tertiary function of the P21 pin.

P2MOD1[1]	P2MOD1[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	Reference capacitor connection pin for RC-ADC (CS1)
1	0	SSIOF data input (SINF0)
1	1	Prohibited

- **P2MOD2[1:0]** (bit 9 to 8)
  The P2MOD2[1:0] bit are used to select the primary, secondary, or tertiary function of the P22 pin.

P2MOD2[1]	P2MOD2[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	Reference resistor connection pin for RC-ADC (RS1)
1	0	SSIOF clock input/output (SCKF0)
1	1	FTM output mode (TMOUT2)

- **P2MOD3[1:0]** (bit 13 to 12)
  The P2MOD3[1:0] bits are used to select the primary, secondary, or tertiary function of the P23 pin.

P2MOD3[1]	P2MOD3[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	Resistor sensor connection pin for measurement for RC-ADC (RT1)
1	0	SSIOF enable input/output (SSF0)
1	1	FTM output mode (TMOUT3)

[Note]
If any bit combination out of the above is set to “Prohibited” and the corresponding bit of the Port 2 is specified to output mode (selected in Port 2 control register), status of corresponding pin is fixed, regardless the contents of Port 2 register (P2D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to “L”
CMOS output mode: High-impedance: Fixed to “L”

22.2.3. Description of Operation

22.2.3.1. Input/Output Port Functions

For each pin of Port 2, either output or input is selected by setting the Port 2 direction register (P2DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 2 control register (P2CON).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 2 control register (P2CON).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, “L” or “H” level is output to each pin of Port 2 depending on the value set by the Port 2 data register (P2D).
In input mode, the input level of each pin of Port 2 can be read from the Port 2 data register (P2D).

22.2.3.2. Primary Function Except for Input/Output Port

Port 2 is assigned to the SA-A/DC input pins (AIN4, AIN5, AIN6, AIN7), External interrupts (EXI20, EXI21, EXI22, EXI23).
When used as the SA-ADC input pins, set the applicable port to the high impedance output state.
When used as the External interrupts, set an applicable port to the input state.

22.2.3.3. Secondary, Tertiary and Quaternary Functions

Secondary, tertiary and quaternary functions are assigned to Port 2 as RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1), the SSIOF pins (SCKF0, SINF0, SOUTF0, SSF0), FTM output pin (TMOUT2, TMOUT3),.
These pins can be used in a secondary or tertiary or quaternary function mode by setting the P2MODn[1:0] (n=0 to 3) bits of the Port 2 mode registers (P2MOD).
When used as the RC-ADC, set the P20 to P23 to the high impedance input state and RC-ADC mode.

22.3. PORT3

22.3.1. Overview

This LSI includes an 8 bit input/output port, port 3 (P30 to P37).
It can function as an external interrupt, a successive approximation type A/D converter input, a VLS input, timer clock inputs and a comparator input, as well as an I^2C bus, an I^2C bus with FIFO, a synchronous serial port, a synchronous serial port with FIFO, a UART, a UART with FIFO, a 32kHz clock output and a functional timer output pin as the secondary, tertiary, or quaternary function.

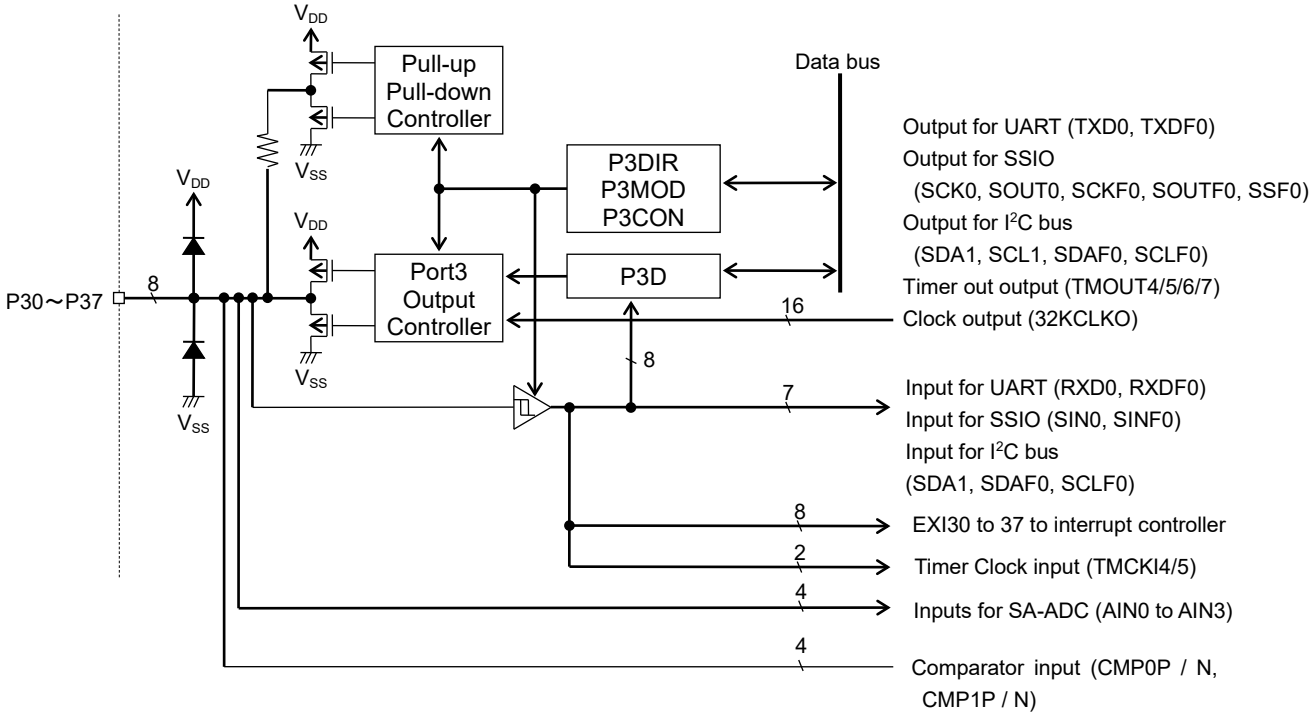
Timer	Chapter 10 “Timers”
FTM	Chapter 11 “Function Timer”
SSIO	Chapter 15 “Synchronous Serial Port”
SSIOF	Chapter 16 “Synchronous Serial Port with FIFO”
UART	Chapter 17“UART”
UARTF	Chapter 18“UART with FIFO”
I^2C	Chapter 19 “I^2C Bus Interface”
I^2CF	Chapter 20 “I^2C Bus Interface with FIFO”
SA-ADC	Chapter 26 “Successive approximate type A/D converter”
CMP	Chapter 28 “Analog Comparator”
VLS	Chapter 30 “Voltage Level Supervisor”

22.3.1.1. Features

- Direct LED drive is available.
- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Can be used as an external interrupt pin (EXI30, EXI31, EXI32, EXI33, EXI34, EXI35, EXI36, EXI37), a successive approximation type A/D converter pin (AIN0/1/2/3), a comparator input (CMP0P/N, CMP1P/N), Timer clock input (TMCKI4/5), an I^2C bus pin (SDA1, SCL1), an I^2C bus with FIFO pin (SDAF0, SCLF0), a synchronous serial port pin (SIN0, SCK0, SOUT0), a synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), a UART pin (RXD0, TXD0), a UART with FIFO pin (RXDF0, TXDF0), a 32kHz clock output (32KCLKO) or a timer out pin (TMOUT4/5/6/7).

22.3.1.2. Configuration

Figure 22-4 shows the configuration of Port 3.



P3D : Port 3 data register
P3DIR : Port 3 direction register
P3CON : Port 3 control register
P3MOD : Port 3 mode register

Figure 22-3 Configuration of Port 3

22.3.1.3. List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quaternary function
P30/EXI30/CMP0P/ VLSin/ SDAF0/ SOUT0/	I/O	I/O port External interrupt Comparator + side input 0 VLS input	I^2C with FIFO data I/O SDAF0	Synchronous serial data output SOUT0	–
P31/EXI31/CMP0M/ SCLF0/ SIN0	I/O	I/O port External interrupt Comparator - side input 0	I^2C with FIFO clock output SCLF0	Synchronous serial data input SIN0	–
P32/EXI32/CMP1P/ AIN2/ RXDF0/ SCK0/ TMOUT4	I/O	I/O port External interrupt Comparator + side input1 Successive approximation type A/D converter input AIN2	UART with FIFO data input RXDF0	Synchronous serial clock output SCK0	FTM output TMOUT4
P33/EXI33/CMP1M/ AIN3/ 32KCLKO/ TMOUT5	I/O	I/O port External interrupt Comparator - side input 1 Successive approximation type A/D converter input AIN3	UART with FIFO data output TXDF0	32kHz Clock output 32KCLKO	FTM output TMOUT5
P34/EXI34/ AIN0/ LED/ SDA1/ SOUTF0	I/O	I/O port External interrupt Successive approximation type A/D converter input AIN0 LED direct drive	I^2C data I/O SDA1	Synchronous serial data with FIFO output SOUTF0	–
P35/EXI35/ AIN1/ LED/ SCL1/ SINF0/	I/O	I/O port External interrupt Successive approximation type A/D converter input AIN1 LED direct drive	I^2C output SCL1	Synchronous serial data with FIFO input SINF0	–
P36/ EXI36/ AIN2/ TMCKI4/ RXD0/ SCKF0/ TMOUT6	I/O	I/O port External interrupt Timer Clock input TMCKI4	UART data input RXD0	Synchronous serial clock with FIFO output SCKF0	FTM output TMOUT6
P37/ EXI37/ AIN3/ TMCKI5/ TXD0/ SSF0/ TMOUT7	I/O	I/O port External interrupt Timer Clock input TMCKI5	UART data output TXD0	Synchronous serial chip with FIFO select output SSF0	FTM output TMOUT7

22.3.2. Description of Registers

22.3.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4300	Port 3 data register	P3D	R/W	32	0x0000_0000
0x5C00_4304	Port 3 direction register	P3DIR	R/W	32	0x0000_0000
0x5C00_4308	Port 3 control register	P3CON	R/W	32	0x0000_0000
0x5C00_430C	Port 3 mode register	P3MOD	R/W	32	0x0000_0000

22.3.2.2. Port 3 Data Register (P3D)

Address: 0x5C00_4300
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	P3D[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P3D is a special function register (SFR) to set the value to be output to the Port 3 pin or to read the input level of the Port 3. In output mode, the value of this register is output to the Port 3 pin. The value written to P3D is readable. In input mode, the input level of the Port 3 pin is read when P3D is read.
Output mode or input mode is selected by using the port mode register (P3DIR) described later.

[Description of Bits]

- **P3D[7:0]** (bit 7 to 0)
  The P3D[7:0] bits are used to set the output value of the Port 3 pin in output mode and to read the pin level of the Port 3 pin in input mode.

P3D[n]	Description
0	Output or input level of the P3n pin: ”L”
1	Output or input level of the P3n pin: ”H”

n=0 to 7

22.3.2.3. Port 3 Direction Register (P3DIR)

Address: 0x5C00_4304
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	P3DIR[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P3DIR is a special function register (SFR) to select the input/output mode of Port 3.

[Description of Bits]

- **P3DIR[7:0]** (bit 7 to 0)
  The P3DIR[7:0] bits are used to set the input/output mode of the port 3 pin.

P3DIR[n]	Description
0	P3n pin: Output (initial value)
1	P3n pin: Input

[Note]
The P30 to P35 pins are assigned to successive approximation type A/D converter input or comparator input. If it is used as a successive approximation type A/D converter input or comparator input, set the appropriate port to the output mode.

22.3.2.4. Port 3 Control Register (P3CON)

Address: 0x5C00_4308
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	P3CON7 [1:0]		–*	–*	P3CON6 [1:0]		–*	–*	P3CON5 [1:0]		–*	–*	P3CON4 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P3CON3 [1:0]		–*	–*	P3CON2 [1:0]		–*	–*	P3CON1 [1:0]		–*	–*	P3CON0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P3CON is a special function register (SFRs) to select input/output state of the Port 3 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P3DIR register.

[Description of Bits]

- **P3CONn[1:0]** (n=0 to 7)
  The P3CONn[1:0] bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
  To perform the direct LED drive, select N-channel open drain output mode.

Setting of P3n pin	When output mode is selected (P3DIR[n] bit = “0”)	When input mode is selected (P3DIR[n] bit = “1”)
P3CONn[1:0]	Description	
00	P3n pin: High-impedance output (initial value)	P3n pin: High-impedance input
01	P3n pin: P-channel open drain output	P3n pin: Input with a pull-down resistor
10	P3n pin: N-channel open drain output	P3n pin: Input with a pull-up resistor
11	P3n pin: CMOS output	P3n pin: High-impedance input

n=0 to 7

[Note]
The P30 to P35 pins are assigned to successive approximation type A/D converter input or comparator input . If it is used as a successive approximation type A/D converter input or comparator input, set the appropriate port to the high-impedance output mode.

22.3.2.5. Port 3 Mode Register (P3MOD)

Address: 0x5C00_430C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	P3MOD7 [1:0]		–*	–*	P3MOD6 [1:0]		–*	–*	P3MOD5 [1:0]		–*	–*	P3MOD4 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P3MOD3 [1:0]		–*	–*	P3MOD2 [1:0]		–*	–*	P3MOD1 [1:0]		–*	–*	P3MOD0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P3MOD is a special function registers (SFRs) to the primary, secondary, tertiary, or quaternary function of the port 3.

[Description of Bits]

- **P3MOD0[1:0]** (bit 1 to 0)
  The P3MOD0[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P30 pin.

P3MOD0[1]	P3MOD0[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	I^2C with FIFO bus data input/output mode (SDAF0)
1	0	Synchronous serial port data output mode (SOUT0)
1	1	Prohibited

- **P3MOD1[1:0]** (bit 5 to 4)
  The P3MOD1[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P31 pin.

P3MOD1[1]	P3MOD1[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	I^2C with FIFO bus clock output mode (SCLF0)
1	0	Synchronous serial port data input mode (SIN0)
1	1	Prohibited

- **P3MOD2[1:0]** (bit 9 to 8)
  The P3MOD2[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P32 pin.

P3MOD2[1]	P3MOD2[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	UART with FIFO data input mode (RXDF0)
1	0	Synchronous serial port clock input/output mode (SCK0)
1	1	FTM output mode (TMOUT4)

- **P3MOD3[1:0]** (bit 13 to 12)
  The P3MOD3[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P33 pin.

P3MOD3[1]	P3MOD3[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	UART with FIFO data output mode (TXDF0)
1	0	32kHz clock output mode (32KCLKO)
1	1	FTM output mode (TMOUT5)

- **P3MOD4[1:0]** (bit 17 to 16)
  The P3MOD4[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P34 pin.

P3MOD4[1]	P3MOD4[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	I^2C bus data input/output mode (SDA1)
1	0	Synchronous serial port with FIFO data output mode (SOUTF0)
1	1	Prohibited

- **P3MOD5[1:0]** (bit 21 to 20)
  The P3MOD5[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P35 pin.

P3MOD5[1]	P3MOD5[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	I^2C bus clock output mode (SCL1)
1	0	Synchronous serial port with FIFO data input mode (SINF0)
1	1	Prohibited

- **P3MOD6[1:0]** (bit 25 to 24)
  The P3MOD6[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P36 pin.

P3MOD6[1]	P3MOD6[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	UART data input mode (RXD0)
1	0	Synchronous serial port with FIFO clock input/output mode (SCKF0)
1	1	FTM output mode (TMOUT6)

- **P3MOD7[1:0]** (bit 29 to 28)
  The P3MOD7[1:0] bits are used to select the primary, secondary, tertiary, or quaternary function of the P37 pin.

P3MOD7[1]	P3MOD7[0]	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	UART data output mode (TXD0)
1	0	Synchronous serial port with FIFO chip select input/output mode (SSF0)
1	1	FTM output mode (TMOUT7)

[Note]

When the pin is set to “Prohibited” and the output mode is selected (by the Port 3 control register), the Port 3 output pin state is fixed as follows regardless of the data of the port data register P3D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to “L”
When CMOS output is selected: Output pin is fixed to “L”

22.3.3. Description of Operation

22.3.3.1. Input/Output Port Functions

For each pin of Port 3, either output or input is selected by setting the Port 3 direction register (P3DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 3 control registers (P3CON).
In the input mode, set the port 3 control register (P3CON) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, “L” or “H” level is output to each pin of Port 3 depending on the value set by the Port 3 data register (P3D).
In input mode, the input level of each pin of Port 3 can be read from the Port 3 data register (P3D).

22.3.3.2. Primary Function Except for Input/Output Port

The successive approximation type A/D converter input (AIN0 to AIN3), comparator input (CMP0P/N, CMP1P/N), VLS input (VLSin), the timer clock input (TMCLKI4/5) or external interrupt input (EXI30 to EXI37) can be assigned to the port 3 as the primary function other than the input/output port.
To use the port as the successive approximation type A/D converter input (AIN0 to AIN3) or comparator input (CMP0P/N, CMP1P/N), set the appropriate port as high-impedance output.
To use the port as the timer clock input (TMCLKI4/5) , or the external interrupt input (EXI30 to EXI37), set the appropriate port to the input state.

22.3.3.3. Secondary, Tertiary, Quaternary and Quinary Functions

The I2C bus pin (SDA1, SCL1), I2C bus with FIFO pin (SDAF0, SCLF0), synchronous serial port pin (SIN0, SCK0, SOUT0), synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), UART pin (RXD0, TXD0), UART with FIFO pin (RXDF0, TXDF0), 32k clock output pin (32kCLKO) and FTM output pin (TMOUT4/5/6/7) are assigned to the port 3 as the secondary, tertiary, or quaternary function. Each of them can be used as the tertiary or quaternary function by setting the P3MODn[1:0] (n=0 to 7) bits of the port 3 mode register (P3MOD).

22.4. PORT4

22.4.1. Overview

This LSI includes an 8 bit input/output port, port 4 (P40 to P47).
It can function as an external interrupt and timer clock inputs, as well as an I^2C bus, an I^2C bus with FIFO, a synchronous serial port, a synchronous serial port with FIFO, a UART, a UART with FIFO, a 32kHz clock output, a LCD segment port and a functional timer output pin as the secondary, tertiary, quaternary, or quinary function.

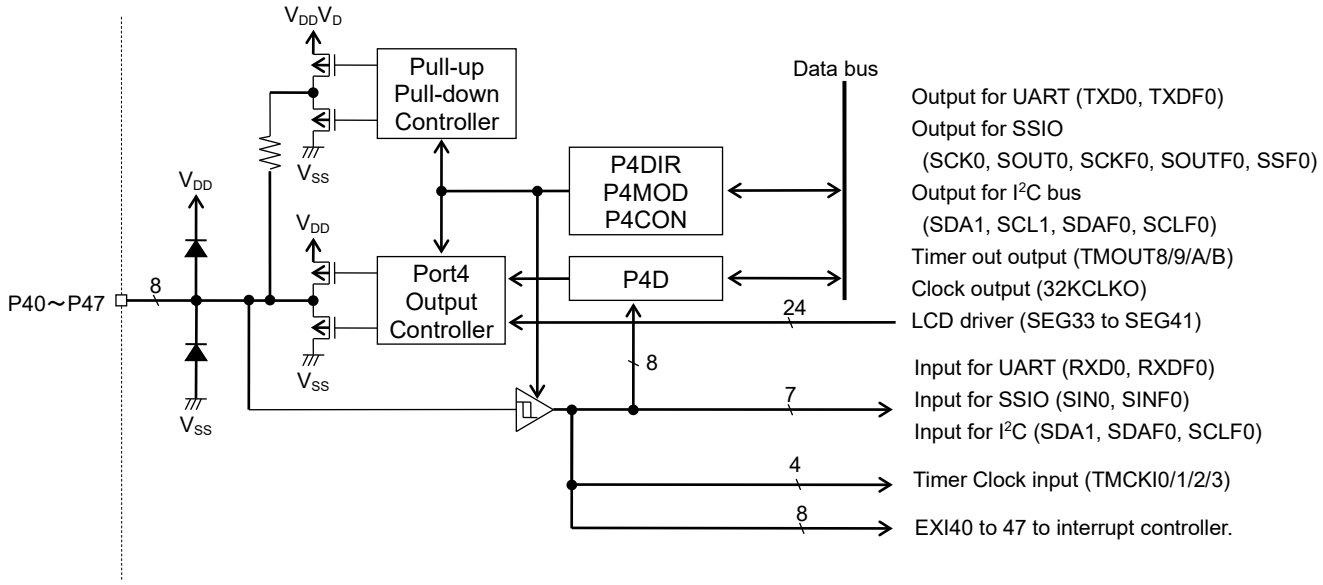
TIMER	Chapter 10 “Timers”
FTM	Chapter 11 “Function Timer”
SSIO	Chapter 15 “Synchronous Serial Port”
SSIOF	Chapter 16 “Synchronous Serial Port with FIFO”
UART	Chapter 17“UART”
UARTF	Chapter 18“UART with FIFO”
I^2C	Chapter 19 “I^2C Bus Interface”
I^2CF	Chapter 20 “I^2C Bus Interface with FIFO”
LCD Driver	Chapter 27 “LCD Driver”

22.4.1.1. Features

- Direct LED drive is available.
- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Can be used as an external interrupt pin (EXI40, EXI41, EXI42, EXI43, EXI44, EXI45, EXI46, EXI47), Timer clock input (TMCKI0/1/2/3), an I2C bus pin (SDA1, SCL1), an I2C bus with FIFO pin (SDAF0, SCLF0), a synchronous serial port pin (SIN0, SCK0, SOUT0), a synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), a UART pin (RXD0, TXD0), a UART with FIFO pin (RXDF0, TXDF0), a 32kHz clock output (32KCLKO), LCD driver pin (SEG33 to SEG41) or a timer out pin (TMOUT8/9/A/B).

22.4.1.2. Configuration

Figure 22-5 shows the configuration of Port 4.



P4D : Port 4 data register
P4DIR : Port 4 direction register
P4CON : Port 4 control register
P4MOD : Port 4 mode register

Figure 22-4 Configuration of Port 4

22.4.1.3. List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quaternary function	Quinary Function
P40/EXI40/LED/ SDAF0/ SOUT0/ SEG34	I/O	I/O port External interrupt LED direct drive	I^2C with FIFO data I/O SDAF0	Synchronous serial data output SOUT0	–	LCD segment pin SEG34
P41/EXI41/LED/ SCLF0/ SIN0/ SEG35	I/O	I/O port External interrupt LED direct drive	I^2C with FIFO clock output SCLF0	Synchronous serial data input SIN0	–	LCD segment pin SEG35
P42/EXI42/TMCKI0/ RXDF0/ SCK0/ TMOUT8 SEG36	I/O	I/O port External interrupt Timer Clock input TMCKI0	UART with FIFO data input RXDF0	Synchronous serial clock output SCK0	FTM output TMOUT8	LCD segment pin SEG36
P43/EXI43/TMCKI1/ TXDF0/ 32KCLKO/ TMOUT9/ SEG37	I/O	I/O port External interrupt Timer Clock input TMCKI1	UART with FIFO data output TXDF0	32kHz Clock output 32KCLKO	FTM output TMOUT9	LCD segment pin SEG37
P44/EXI44/ SDA1/ SOUTF0/ SEG38	I/O	I/O port External interrupt	I^2C data I/O SDA1	Synchronous serial data with FIFO output SOUTF0	–	LCD segment pin SEG38
P45/EXI45/ SCL1/ SINF0/ SEG39	I/O	I/O port External interrupt	I^2C output SCL1	Synchronous serial data with FIFO input SINF0	–	LCD segment pin SEG39
P46/EXI46/TMCKI2 RXD0/ SCKF0/ TMOUTA/ SEG40	I/O	I/O port External interrupt Timer Clock input TMCKI2	UARTdata input RXD0	Synchronous serial clock with FIFO output SCKF0	FTM output TMOUTA	LCD segment pin SEG40
P47/EXI47/TMCKI3 TXD0/ SSF0/ TMOUTB/ SEG41	I/O	I/O port External interrupt Timer Clock input TMCKI3	UART data output TXD0	Synchronous serial chip with FIFO select output SSF0	FTM output TMOUTB	LCD segment pin SEG41

22.4.2. Description of Registers

22.4.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4400	Port 4 data register	P4D	R/W	32	0x0000_0000
0x5C00_4404	Port 4 direction register	P4DIR	R/W	32	0x0000_0000
0x5C00_4408	Port 4 control register	P4CON	R/W	32	0x0000_0000
0x5C00_440C	Port 4 mode register	P4MOD	R/W	32	0x0000_0000

22.4.2.2. Port 4 Data Register (P4D)

Address: 0x5C00_4400
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	P4D[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable. In input mode, the input level of the Port 4 pin is read when P4D is read.
Output mode or input mode is selected by using the port mode register (P4DIR) described later.

[Description of Bits]

- **P4D[7:0]** (bit 7 to 0)
  The P4D[7:0] bits are used to set the output value of the Port 4 pin in output mode and to read the pin level of the Port 4 pin in input mode.

P4D[n]	Description
0	Output or input level of the P4n pin: ”L”
1	Output or input level of the P4n pin: ”H”

n=0 to 7

22.4.2.3. Port 4 Direction Register (P4DIR)

Address: 0x5C00_4404
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	P4DIR[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

[Description of Bits]

- **P4DIR[7:0]** (bit 7 to 0)
  The P4DIR[7:0] bits are used to set the input/output mode of the port 4 pin.

P4DIR[n]	Description
0	P4n pin: Output (initial value)
1	P4n pin: Input

n=0 to 7

22.4.2.4. Port 4 Control Register (P4CON)

Address: 0x5C00_4408
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	P4CON7 [1:0]		–*	–*	P4CON6 [1:0]		–*	–*	P4CON5 [1:0]		–*	–*	P4CON4 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P4CON3 [1:0]		–*	–*	P4CON2 [1:0]		–*	–*	P4CON1 [1:0]		–*	–*	P4CON0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P4CON is a special function register (SFRs) to select input/output state of the Port 4 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P4DIR register.

[Description of Bits]

- **P4CONn[1:0]** (n=0 to 7)
  The P4CONn[1:0] bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
  To perform the direct LED drive, select N-channel open drain output mode.

Setting of P4n pin	When output mode is selected (P4DIR[n] bit = “0”)	When input mode is selected (P4DIR[n] bit = “1”)
P4CONn[1:0]	Description	
00	P4n pin: High-impedance output (initial value)	P4n pin: High-impedance input
01	P4n pin: P-channel open drain output	P4n pin: Input with a pull-down resistor
10	P4n pin: N-channel open drain output	P4n pin: Input with a pull-up resistor
11	P4n pin: CMOS output	P4n pin: High-impedance input

n=0 to 7

22.4.2.5. Port 4 Mode Register (P4MOD)

Address: 0x5C00_440C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	P4MOD7[2:0]			–*	P4MOD6[2:0]			–*	P4MOD5[2:0]			–*	P4MOD4[2:0]		
Access	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	P4MOD3[2:0]			–*	P4MOD2[2:0]			–*	P4MOD1[2:0]			–*	P4MOD0[2:0]		
Access	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P4MOD is a special function registers (SFRs) to the primary, secondary, tertiary, quaternary, or quinary function of the port 4.

[Description of Bits]

- **P4MOD0[2:0]** (bit 2 to 0)
  The P4MOD0[2:0] bits are used to select the primary, secondary, tertiary, quaternary or quinary function of the P40 pin.

P4MOD0[2]	P4MOD0[1]	P4MOD0[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I²C with FIFO bus data input/output mode (SDAF0)
0	1	0	Synchronous serial port data output mode (SOUT0)
0	1	1	Prohibited
1	x	x	LCD SEG34 port

- **P4MOD1[2:0]** (bit 6 to 4)
  The P4MOD1[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P41 pin.

P4MOD1[2]	P4MOD1[1]	P4MOD1[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I²C with FIFO bus clock output mode (SCLF0)
0	1	0	Synchronous serial port data input mode (SIN0)
0	1	1	Prohibited
1	x	x	LCD SEG35 port

- **P4MOD2[2:0]** (bit 10 to 8)
  The P4MOD2[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P42 pin.

P4MOD2[2]	P4MOD2[1]	P4MOD2[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART with FIFO data input mode (RXDF0)
0	1	0	Synchronous serial port clock input/output mode (SCK0)
0	1	1	FTM output mode (TMOUT8)
1	x	x	LCD SEG36 port

- **P4MOD3[2:0]** (bit 14 to 12)
  The P4MOD3[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P43 pin.

P4MOD3[2]	P4MOD3[1]	P4MOD3[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART with FIFO data output mode (TXDF0)
0	1	0	32kHz clock output mode (32KCLKO)
0	1	1	FTM output mode (TMOUT9)
1	x	x	LCD SEG37 port

- **P4MOD4[2:0]** (bit 18 to 16)
  The P4MOD4[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P44 pin.

P4MOD4[2]	P4MOD4[1]	P4MOD4[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I^2C bus data input/output mode (SDA1)
0	1	0	Synchronous serial port with FIFO data output mode (SOUTF0)
0	1	1	Prohibited
1	x	x	LCD SEG38 port

- **P4MOD5[2:0]** (bit 22 to 20)
  The P4MOD5[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P45 pin.

P4MOD5[2]	P4MOD5[1]	P4MOD5[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I^2C bus clock output mode (SCL1)
0	1	0	Synchronous serial port with FIFO data input mode (SINF0)
0	1	1	Prohibited
1	x	x	LCD SEG39 port

- **P4MOD6[2:0]** (bit 26 to 24)
  The P4MOD6[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P46 pin.

P4MOD6[2]	P4MOD6[1]	P4MOD6[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART data input mode (RXD0)
0	1	0	Synchronous serial port with FIFO clock input/output mode (SCKF0)
0	1	1	FTM output mode (TMOUTA)
1	x	x	LCD SEG40 port

- **P4MOD7[2:0]** (bit 30 to 28)
  The P4MOD7[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P47 pin.

P4MOD7[2]	P4MOD7[1]	P4MOD7[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART data output mode (TXD0)
0	1	0	Synchronous serial port with FIFO chip select input/output mode (SSF0)
0	1	1	FTM output mode (TMOUTB)
1	x	x	LCD SEG41 port

[Note]

When the pin is set to “Prohibited” and the output mode is selected (by the Port 4 control register), the Port 4 output pin state is fixed as follows regardless of the data of the port data register P4D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to “L”
When CMOS output is selected: Output pin is fixed to “L”

22.4.3. Description of Operation

22.4.3.1. Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control register (P4CON).
In the input mode, set the port 4 control register (P4CON) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, “L” or “H” level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

22.4.3.2. Primary Function Except for Input/Output Port

The external interrupt input (EXI40 to EXI47), or the timer clock input (TMCLKI0/1/2/3) can be assigned to the port 4 as the primary function other than the input/output port.
To use the port as the timer clock input (TMCLKI0/1/2/3) , or the external interrupt input (EXI40 to EXI47), set the appropriate port to the input state.

22.4.3.3. Secondary, Tertiary and Quaternary Functions

The I2C bus pin (SDA1, SCL1), I2C bus with FIFO pin (SDAF0, SCLF0), synchronous serial port pin (SIN0, SCK0, SOUT0), synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), UART pin (RXD0, TXD0), UART with FIFO pin (RXDF0, TXDF0), 32k clock output pin (32kCLKO), LCD segment port (SEG34 to 41) and FTM output pin (TMOUT8/9/A/B) are assigned to the port 4 as the secondary, tertiary, quaternary, or quinary function. Each of them can be used as the tertiary or quaternary function by setting the P4MODn[2:0] (n=0 to 7) bits of the port 4 mode register (P4MOD).

22.5. PORT5

22.5.1. Overview

This LSI includes an 8 bit input/output port, port 5 (P50 to P57).
It can function as an external interrupt and timer clock inputs, as well as an I^2C bus, an I^2C bus with FIFO, a synchronous serial port, a synchronous serial port with FIFO, a UART, a UART with FIFO, a 32kHz clock output, a LCD segment port and a functional timer output pin as the secondary, tertiary, quaternary, or quinary function.

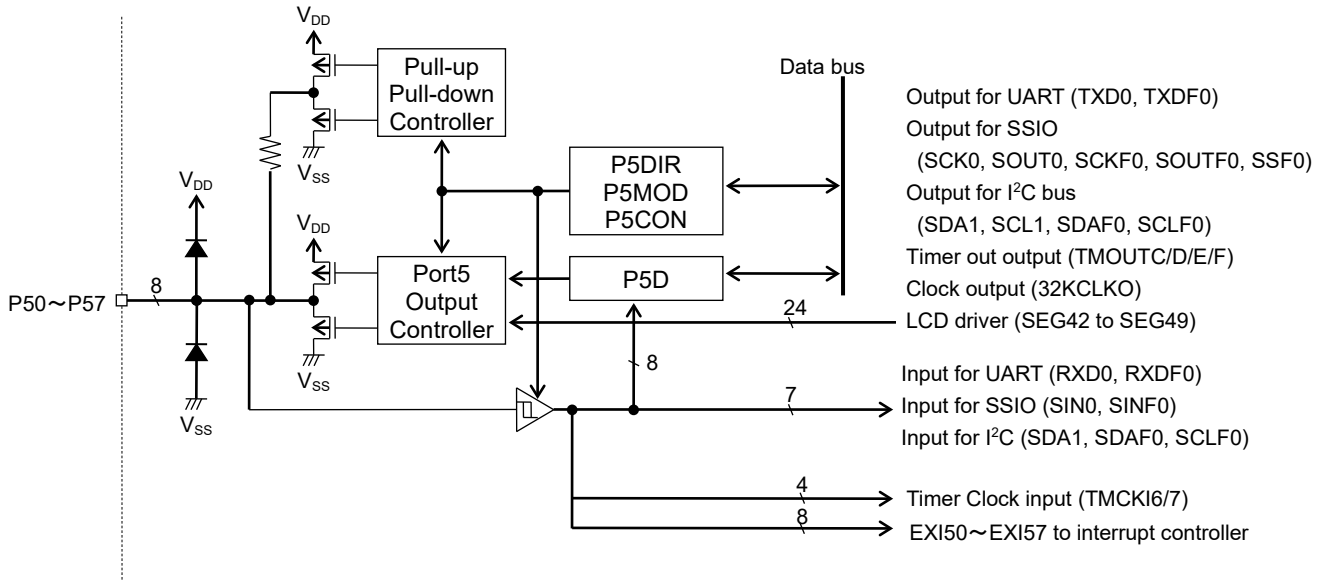
TIMER	Chapter 10 “Timers”
FTM	Chapter 11 “Function Timer”
SSIO	Chapter 15 “Synchronous Serial Port”
SSIOF	Chapter 16 “Synchronous Serial Port with FIFO”
UART	Chapter 17“UART”
UARTF	Chapter 18“UART with FIFO”
I^2C	Chapter 19 “I^2C Bus Interface”
I^2CF	Chapter 20 “I^2C Bus Interface with FIFO”
LCD Driver	Chapter 27 “LCD Driver”

22.5.1.1. Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Can be used as an external interrupt pin (EXI50, EXI51, EXI52, EXI53, EXI54, EXI55, EXI56, EXI57), Timer clock input (TMCKI6/7), an I2C bus pin (SDA1, SCL1), an I2C bus with FIFO pin (SDAF0, SCLF0), a synchronous serial port pin (SIN0, SCK0, SOUT0), a synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), a UART pin (RXD0, TXD0), a UART with FIFO pin (RXDF0, TXDF0), a 32kHz clock output (32KCLKO), LCD segment pin (SEG42 to SEG49) or a timer out pin (TMOUTC/D/E/F).

22.5.1.2. Configuration

Figure 22-6 shows the configuration of Port 5.



P5D : Port 5 data register
P5DIR : Port 5 direction register
P5CON : Port 5 control register
P5MOD : Port 5 mode register

Figure 22-5 Configuration of Port 5

22.5.1.3. List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quaternary function	Quinary Function
P50/EXI50/ SDAF0/ SOUT0/ SEG42	I/O	I/O port External interrupt	I^2C with FIFO data I/O SDAF0	Synchronous serial data output SOUT0	–	LCD segment pin SEG42
P51/EXI51 / SCLF0/ SIN0/ SEG43	I/O	I/O port External interrupt	I^2C with FIFO clock output SCLF0	Synchronous serial data input SIN0	–	LCD segment pin SEG43
P52/EXI52/TMCKI0/ RXDF0/ SCK0/ TMOUTC SEG44	I/O	I/O port External interrupt	UART with FIFO data input RXDF0	Synchronous serial clock output SCK0	FTM output TMOUTC	LCD segment pin SEG44
P53/EXI53/TMCKI1/ TXDF0/ 32KCLKO/ TMOUTD/ SEG45	I/O	I/O port External interrupt	UART with FIFO data output TXDF0	32kHz Clock output 32KCLKO	FTM output TMOUTD	LCD segment pin SEG45
P54/EXI54/ SDA1/ SOUTF0/ SEG46	I/O	I/O port External interrupt	I^2C data I/O SDA1	Synchronous serial data with FIFO output SOUTF0	–	LCD segment pin SEG46
P55/EXI55/ SCL1/ SINF0/ SEG47	I/O	I/O port External interrupt	I^2C output SCL1	Synchronous serial data with FIFO input SINF0	–	LCD segment pin SEG47
P56/EXI56/TMCKI6 RXD0/ SCKF0/ TMOUTE/ SEG48	I/O	I/O port External interrupt Timer Clock input TMCKI6	UARTdata input RXD0	Synchronous serial clock with FIFO output SCKF0	FTM output TMOUTE	LCD segment pin SEG48
P57/EXI57/TMCKI7 TXD0/ SSF0/ TMOUTF/ SEG49	I/O	I/O port External interrupt Timer Clock input TMCKI7	UART data output TXD0	Synchronous serial chip with FIFO select output SSF0	FTM output TMOUTF	LCD segment pin SEG49

22.5.2. Description of Registers

22.5.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4500	Port 5 data register	P5D	R/W	32	0x0000_0000
0x5C00_4504	Port 5 direction register	P5DIR	R/W	32	0x0000_0000
0x5C00_4508	Port 5 control register	P5CON	R/W	32	0x0000_0000
0x5C00_450C	Port 5 mode register	P5MOD	R/W	32	0x0000_0000

22.5.2.2. Port 5 Data Register (P5D)

Address: 0x5C00_4500
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	P5D[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P5D is a special function register (SFR) to set the value to be output to the Port 5 pin or to read the input level of the Port 5. In output mode, the value of this register is output to the Port 5 pin. The value written to P5D is readable. In input mode, the input level of the Port 5 pin is read when P5D is read.
Output mode or input mode is selected by using the port mode register (P5DIR) described later.

[Description of Bits]

- **P5D[7:0]** (bit 7 to 0)
  The P5D[7:0] bits are used to set the output value of the Port 5 pin in output mode and to read the pin level of the Port 5 pin in input mode.

P5D[n]	Description
0	Output or input level of the P5n pin: ”L”
1	Output or input level of the P5n pin: ”H”

n=0 to 7

22.5.2.3. Port 5 Direction Register (P5DIR)

Address: 0x5C00_4504
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	P5DIR[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P5DIR is a special function register (SFR) to select the input/output mode of Port 5.

[Description of Bits]

- **P5DIR[7:0]** (bit 7 to 0)
  The P5DIR[7:0] bits are used to set the input/output mode of the port 5 pin.

P5DIR[n]	Description
0	P5n pin: Output (initial value)
1	P5n pin: Input

n=0 to 7

22.5.2.4. Port 5 Control Register (P5CON)

Address: 0x5C00_4508
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	P5CON7 [1:0]		–*	–*	P5CON6 [1:0]		–*	–*	P5CON5 [1:0]		–*	–*	P5CON4 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P5CON3 [1:0]		–*	–*	P5CON2 [1:0]		–*	–*	P5CON1 [1:0]		–*	–*	P5CON0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P5CON is a special function register (SFRs) to select input/output state of the Port 5 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P5DIR register.

[Description of Bits]

- **P5CONn[1:0]** (n=0 to 7)
  The P5CONn[1:0] bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
  To perform the direct LED drive, select N-channel open drain output mode.

Setting of P5n pin	When output mode is selected (P5DIR[n] bit = “0”)	When input mode is selected (P5DIR[n] bit = “1”)
P5CONn[1:0]	Description	
00	P5n pin: High-impedance output (initial value)	P5n pin: High-impedance input
01	P5n pin: P-channel open drain output	P5n pin: Input with a pull-down resistor
10	P5n pin: N-channel open drain output	P5n pin: Input with a pull-up resistor
11	P5n pin: CMOS output	P5n pin: High-impedance input

n=0 to 7

22.5.2.5. Port 5 Mode Register (P5MOD)

Address: 0x5C00_450C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	P5MOD7[2:0]			–*	P5MOD6[2:0]			–*	P5MOD5[2:0]			–*	P5MOD4[2:0]		
Access	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	P5MOD3[2:0]			–*	P5MOD2[2:0]			–*	P5MOD1[2:0]			–*	P5MOD0[2:0]		
Access	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P5MOD is a special function registers (SFRs) to the primary, secondary, tertiary, quaternary, or quinary function of the port 5.

[Description of Bits]

- **P5MOD0[2:0]** (bit 2 to 0)
  The P5MOD0[2:0] bits are used to select the primary, secondary, tertiary, quaternary or quinary function of the P50 pin.

P5MOD0[2]	P5MOD0[1]	P5MOD0[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I^2C with FIFO bus data input/output mode (SDAF0)
0	1	0	Synchronous serial port data output mode (SOUT0)
0	1	1	Prohibited
1	x	x	LCD SEG42 port

- **P5MOD1[2:0]** (bit 6 to 4)
  The P5MOD1[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P51 pin.

P5MOD1[2]	P5MOD1[1]	P5MOD1[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I^2C with FIFO bus clock output mode (SCLF0)
0	1	0	Synchronous serial port data input mode (SIN0)
0	1	1	Prohibited
1	x	x	LCD SEG43 port

- **P5MOD2[2:0]** (bit 10 to 8)
  The P5MOD2[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P52 pin.

P5MOD2[2]	P5MOD2[1]	P5MOD2[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART with FIFO data input mode (RXDF0)
0	1	0	Synchronous serial port clock input/output mode (SCK0)
0	1	1	FTM output mode (TMOUTC)
1	x	x	LCD SEG44 port

- **P5MOD3[2:0]** (bit 14 to 12)
  The P5MOD3[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P53 pin.

P5MOD3[2]	P5MOD3[1]	P5MOD3[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART with FIFO data output mode (TXDF0)
0	1	0	32kHz clock output mode (32KCLKO)
0	1	1	FTM output mode (TMOUTD)
1	x	x	LCD SEG45 port

- **P5MOD4[2:0]** (bit 18 to 16)
  The P5MOD4[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P54 pin.

P5MOD4[2]	P5MOD4[1]	P5MOD4[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I^2C bus data input/output mode (SDA1)
0	1	0	Synchronous serial port with FIFO data output mode (SOUTF0)
0	1	1	Prohibited
1	x	x	LCD SEG46 port

- **P5MOD5[2:0]** (bit 22 to 20)
  The P5MOD5[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P55 pin.

P5MOD5[2]	P5MOD5[1]	P5MOD5[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	I^2C bus clock output mode (SCL1)
0	1	0	Synchronous serial port with FIFO data input mode (SINF0)
0	1	1	Prohibited
1	x	x	LCD SEG47 port

- **P5MOD6[2:0]** (bit 26 to 24)
  The P5MOD6[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P56 pin.

P5MOD6[2]	P5MOD6[1]	P5MOD6[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART data input mode (RXD0)
0	1	0	Synchronous serial port with FIFO clock input/output mode (SCKF0)
0	1	1	FTM output mode (TMOUTE)
1	x	x	LCD SEG48 port

- **P5MOD7[2:0]** (bit 30 to 28)
  The P5MOD7[2:0] bits are used to select the primary, secondary, tertiary, quaternary, or quinary function of the P57 pin.

P5MOD7[2]	P5MOD7[1]	P5MOD7[0]	Description
0	0	0	General-purpose input/output mode / External interrupt (initial value)
0	0	1	UART data output mode (TXD0)
0	1	0	Synchronous serial port with FIFO chip select input/output mode (SSF0)
0	1	1	FTM output mode (TMOUTF)
1	x	x	LCD SEG41 port

[Note]

When the pin is set to “Prohibited” and the output mode is selected (by the Port 5 control register), the Port 5 output pin state is fixed as follows regardless of the data of the port data register P5D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to “L”
When CMOS output is selected: Output pin is fixed to “L”

22.5.3. Description of Operation

22.5.3.1. Input/Output Port Functions

For each pin of Port 5, either output or input is selected by setting the Port 5 direction register (P5DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 5 control register (P5CON).
In the input mode, set the port 5 control register (P5CON) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, “L” or “H” level is output to each pin of Port 5 depending on the value set by the Port 5 data register (P5D).
In input mode, the input level of each pin of Port 5 can be read from the Port 5 data register (P5D).

22.5.3.2. Primary Function Except for Input/Output Port

The external interrupt input (EXI50 to EXI57) , or the timer clock input (TMCLKI6/7) can be assigned to the port 5 as the primary function other than the input/output port.
To use the port as the external interrupt input (EXI50 to EXI57), or the timer clock input (TMCLK6/7), set the appropriate port to the input state.

22.5.3.3. Secondary, Tertiary, Quaternary and Quinary Functions

The I2C bus pin (SDA1, SCL1), I2C bus with FIFO pin (SDAF0, SCLF0), synchronous serial port pin (SIN0, SCK0, SOUT0), synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), UART pin (RXD0, TXD0), UART with FIFO pin (RXDF0, TXDF0), 32k clock output pin (32kCLKO), LCD segment port (SEG42 to 49) and FTM output pin (TMOUTC/D/E/F) are assigned to the port 5 as the secondary, tertiary, quaternary, or quinary function. Each of them can be used as the tertiary or quaternary function by setting the P5MODn[2:0] (n=0 to 7) bits of the port 5 mode register (P5MOD).

22.6. PORT6

22.6.1. Overview

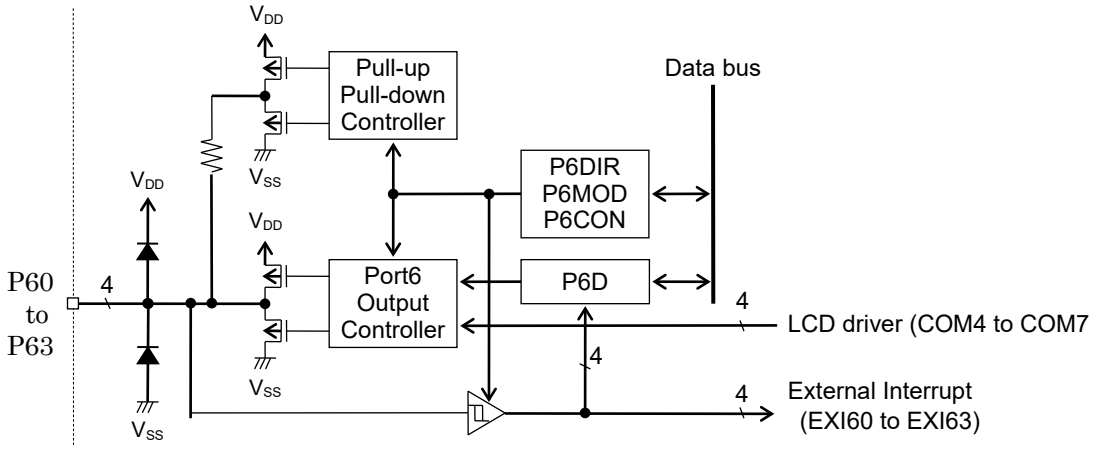
This LSI includes a 4 bit input/output port, port 6 (P60 to P63).
It can function as an external interrupt, as well as a LCD common port as the secondary function.
LCD Driver Chapter 27 “LCD Driver”

22.6.1.1. Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resister,m or input with a pull-up resister for each bit in input mode.
- The external interrupt pins (EXI60, EXI61, EXI62, EXI63) and LCD common pin (COM4 to COM7) can be used as the secondary function.

22.6.1.2. Configuration

Figure 22-7 shows the configuration of the port 6



P6D : Port 6 data register
P6DIR : Port 6 direction register
P6CON : Port 6 controll register
P6MOD : Port 6 mode register

Figure 22-6 Configuration of Port 6

22.6.1.3. List of Pins

Pin name	I/O	Primary function	Secondary function
P60/EXI60/ COM4	I/O	Input/output port External interrupt	LCD common pin COM4
P61/EXI61/ COM5	I/O	Input/output port External interrupt	LCD common pin COM5
P62/EXI62/ COM6	I/O	Input/output port External interrupt	LCD common pin COM6
P63/EXI63/ COM7	I/O	Input/output port External interrupt	LCD common pin COM7

22.6.2. Description of Registers

22.6.2.1. List of Resigers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4600	Port 6 data register	P6D	R/W	32	0x0000_0000
0x5C00_4604	Port 6 direction register	P6DIR	R/W	32	0x0000_0000
0x5C00_4608	Port 6 control register	P6CON	R/W	32	0x0000_0000
0x5C00_460C	Port 6 mode register	P6MOD	R/W	32	0x0000_0000

22.6.2.2. Port 6 Data Register (P6D)

Address: 0x5C00_4600
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P6D[3:0]			
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P6D is a special function register (SFR) to set the value to be output to the Port 6 pin or to read the input level of the Port 6. In output mode, the value of this register is output to the Port 6 pin. The value written to P6D is readable. In input mode, the input level of the Port 6 pin is read when P6D is read.
Output mode or input mode is selected by using the port mode register (P6DIR) described later.

[Description of Bits]

- **P6D[3:0]** (bit 3 to 0)
  The P6D[3:0] bits are used to set the output value of the Port 6 pin in output mode and to read the pin level of the Port 6 pin in input mode.

P6D[n]	Description
0	Output or input level of the P6n pin: ”L”
1	Output or input level of the P6n pin: ”H”

n=0 to 3

22.6.2.3. Port 6 Direction Register (P6DIR)

Address: 0x5C00_4604
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	P6DIR[3:0]			
Access	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P6DIR is a special function register (SFR) to select the input/output mode of Port 6.

[Description of Bits]

- **P6DIR[3:0]** (bit 3 to 0)
  The P6DIR[3:0] bits are used to set the input/output mode of the port 6 pin.

P6DIR[n]	Description
0	P6n pin: Output (initial value)
1	P6n pin: Input

n=0 to 3

22.6.2.4. Port 6 Control Register (P6CON)

Address: 0x5C00_4608
Access: R/W
Access size:32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	P6CON3 [1:0]		–*	–*	P6CON2 [1:0]		–*	–*	P6CON1 [1:0]		–*	–*	P6CON0 [1:0]	
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P6CON is a special function register (SFRs) to select input/output state of the Port 6 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P6DIR register.

[Description of Bits]

- **P6CONn[1:0]** (n=0 to 3)
  The P6CONn[1:0] bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P6n pin	When output mode is selected (P6DIR[n] bit = “0”)	When input mode is selected (P6DIR[n] bit = “1”)
P6CONn[1:0]	Description	
00	P6n pin: High-impedance output (initial value)	P6n pin: High-impedance input
01	P6n pin: P-channel open drain output	P6n pin: Input with a pull-down resistor
10	P6n pin: N-channel open drain output	P6n pin: Input with a pull-up resistor
11	P6n pin: CMOS output	P6n pin: High-impedance input

n=0 to 3

22.6.2.5. Port 6 Mode Register (P6MOD)

Address: 0x5C00_460C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	P6MOD3	–*	–*	–*	P6MOD2	–*	–*	–*	P6MOD1	–*	–*	–*	P6MOD0
Access	–	–	–	R/W	–	–	–	R/W	–	–	–	R/W	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
P6MOD is a special function registers (SFRs) to the primary or secondary function of the port 6.

[Description of Bits]

- **P6MOD0** (bit 0)
  The P6MOD0 bit is used to select the primary or secondary function of the P60 pin.

P6MOD0	Description
0	General-purpose input/output mode / External interrupt (initial value)
1	LCD COM4 port

- **P6MOD1** (bit 4)
  The P6MOD1 bit is used to select the primary or secondary function of the P61 pin.

P6MOD1	Description
0	General-purpose input/output mode / External interrupt (initial value)
1	LCD COM5 port

- **P6MOD2** (bit 8)
  The P6MOD2 bit is used to select the primary or secondary function of the P62 pin.

P6MOD2	Description
0	General-purpose input/output mode / External interrupt (initial value)
1	LCD COM6 port

- **P6MOD3** (bit 12)
  The P6MOD3 bit is used to select the primary or secondary function of the P63 pin.

P6MOD3	Description
0	General-purpose input/output mode / External interrupt (initial value)
1	LCD COM7 port

22.6.3. Description of Operation

22.6.3.1. Input/Output Port Functions

For each pin of Port 6, either output or input is selected by setting the Port 6 direction register (P6DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 6 control register (P6CON).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 6 control register (P6CON).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, “L” or “H” level is output to each pin of Port 6 depending on the value set by the Port 6 data register (P6D).
In input mode, the input level of each pin of Port 6 can be read from the Port 6 data register (P6D).

22.6.3.2. Primary Function Except for Input/Output Port

The external interrupt input (EXI60 to EXI63) can be assigned to the port 6 as the primary function other than the input/output port.
To use the port as the external interrupt input (EXI60 to EXI63), set the appropriate port to the input state.

22.6.3.3. Secondary Function

Secondary function is assigned to Port 6 as LCD common port (COM4 to 7). These pins can be used in a secondary function mode by setting the P6MODn bits (n=0 to3) of the Port 6 mode registers (P6MOD).

Chapter 23

AES

23. AES

23.1. General Description

The AES module provides the AES encryption/decryption function described in NIST FIPS 197, “Advanced Encryption Standard (AES)”, and the block encryption mode function described in NIST Special Publication 800-38A, 2001 Edition, “Recommendation for Block Cryptographic Modes of Operation”.

NIST: National Institute of Standards and Technology
FIPS: Federal Information Processing Standard

23.1.1. Features

- AES encryption/decryption system (AES encryption core function).
  - ✧ Conforms to NIST FIPS 197, “Advanced Encryption Standard (AES)”
    - Plaintext/cipher text size: 128 bits fixed
    - Key size: 128/192/256 bits

- Provides three types of block encryption modes
  - ✧ Conforms to “Recommendation for Block Cryptographic Modes of Operation,” NIST Special Publication 800-38A, 2001 Edition
    - ECB (Electronic CodeBook) mode
    - CBC (Cipher Block Chaining) mode
    - CTR (Counter) mode

23.1.2. Configuration

Figure 23-1 shows the configuration of the AES.

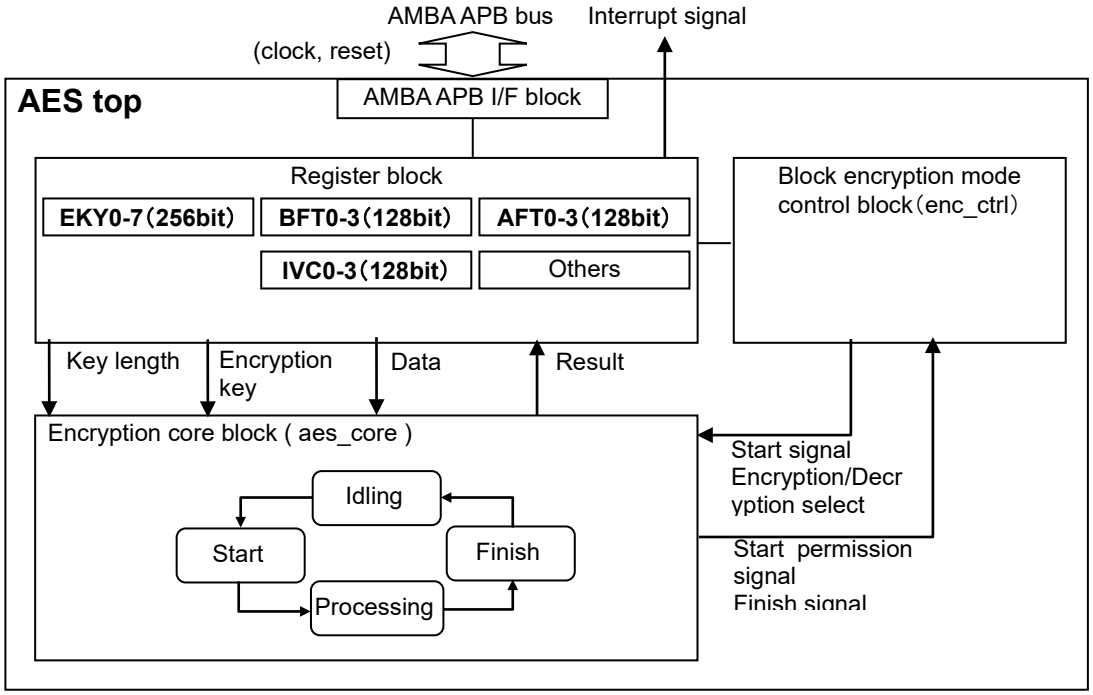


Figure 23-1 Configuration of AES

23.2. Description of Registers

23.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4000_1000	Interrupt Request Register	AESIREQ	R/W	32	0x0000_0000
0x4000_1004	Interrupt Mask Register	AESIMSK	R/W	32	0x0000_0003
0x4000_1008	Starting Number Register	AESSTRT	R/W	32	0x0000_0000
0x4000_100C	Status Register	AESSTAT	R	32	0x0000_0001
0x4000_1010	Control Register	AESCTRL	R/W	32	0x0000_0000
0x4000_1014	Initialization Vector & Counter Register 0	AESIVC0	R/W	32	0x0000_0000
0x4000_1018	Initialization Vector & Counter Register 1	AESIVC1	R/W	32	0x0000_0000
0x4000_101C	Initialization Vector & Counter Register 2	AESIVC2	R/W	32	0x0000_0000
0x4000_1020	Initialization Vector & Counter Register 3	AESIVC3	R/W	32	0x0000_0000
0x4000_1024	Before Processing Data Register 0	AESBFT0	R/W	32	0x0000_0000
0x4000_1028	Before Processing Data Register 1	AESBFT1	R/W	32	0x0000_0000
0x4000_102C	Before Processing Data Register 2	AESBFT2	R/W	32	0x0000_0000
0x4000_1030	Before Processing Data Register 3	AESBFT3	R/W	32	0x0000_0000
0x4000_1034	After Processing Data Register 0	AESAFT0	R	32	0x0000_0000
0x4000_1038	After Processing Data Register 1	AESAFT1	R	32	0x0000_0000
0x4000_103C	After Processing Data Register 2	AESAFT2	R	32	0x0000_0000
0x4000_1040	After Processing Data Register 3	AESAFT3	R	32	0x0000_0000
0x4000_1044	Encryption Key Register 0	AESEKY0	W	32	0x0000_0000
0x4000_1048	Encryption Key Register 1	AESEKY1	W	32	0x0000_0000
0x4000_104C	Encryption Key Register 2	AESEKY2	W	32	0x0000_0000
0x4000_1050	Encryption Key Register 3	AESEKY3	W	32	0x0000_0000
0x4000_1054	Encryption Key Register 4	AESEKY4	W	32	0x0000_0000
0x4000_1058	Encryption Key Register 5	AESEKY5	W	32	0x0000_0000
0x4000_105C	Encryption Key Register 6	AESEKY6	W	32	0x0000_0000
0x4000_1060	Encryption Key Register 7	AESEKY7	W	32	0x0000_0000

23.2.2. Interrupt Request Register (AESIREQ)

Address: 0x4000_1000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	IREQ_EVRY	IREQ_ALL
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AESIREQ is a special function register (SFR) used to indicate the causes of the interrupt. Regardless of the value of AESIMSK register, the bit related to the cause of interrupt is set to "1" when the interrupt requests are detected. The bits of AESIREQ can be cleared to "0" by writing these bits "1".

[Description of Bits]

- **IREQ_ALL** (bit 0)
  The IREQ_ALL bit is set to “1” when the encryption processes are finished the same times as setting of AESSTRT register.

IREQ_ALL	Description
0	No request (Initial value)
1	Interrupt requests are detected

- **IREQ_EVRY** (bit 1)
  The IREQ_EVRY bit is set to “1” when the every encryption is finished.

IREQ_EVRY	Description
0	No request (Initial value)
1	Interrupt requests are detected

23.2.3. Interrupt Mask Register (AESIMSK)

Address: 0x4000_1004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	IMSK_EVRY	IMSK_ALL
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AESIMSK is a special function register (SFR) used to mask the interrupt requests which AESIREQ register indicates.

[Description of Bits]

- **IMSK_ALL** (bit 0)
  The IMSK_ALL bit is set to “1”, and then the interrupt requests caused by finishing all of encryption processes are masked.

IMSK_ALL	Description
0	The interrupt requests caused by finishing all of encryption processes are not masked
1	The interrupt requests caused by finishing all of encryption processes are masked (Initial value)

- **IMSK_EVRY** (bit 1)
  The IMSK_EVRY bit is set to “1”, and then the interrupt requests caused by finishing every encryption process are masked.

IMSK_EVRY	Description
0	The interrupt requests caused by finishing every encryption process are not masked
1	The interrupt requests caused by finishing every encryption process are masked (Initial value).

23.2.4. Starting Number Register (AESSTRT)

Address: 0x4000_1008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	STRT_REQ_CNT[7:0]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing

[Description of Register]
AESSTRT is a special function register (SFR) used to start and iterate encryption/decryption process. Set this register the value (from 0000_0001H to 0000_00FFH), which is subtracted “1” every time encryption/decryption process is executed, and the encryption/decryption process starts and iterates until the value of this register becomes 0000_0000H.

[Description of Bits]

- **STRT_REQ_CNT** (bit 7 to 0)
  The STRT_REQ_CNT[7:0] is the number of startup of encryption/decryption process.

[Note]
Usually set 0000_00001H to this register.

23.2.5. Status Register (AESSTAT)

Address: 0x4000_100C
Access: R
Access size: 32 bit
Initial value: 0x0000_0001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	STRT_EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AESSTAT is a special function register(SFR) which indicates the encryption/decription status.

[Description of Bits]

- **STRT_EN** (bit 0)
  The bit indicates the status of encryption/decryption process .This bit is “0” while every encryption/decryption process is operating, and this bit becomes “1” when every encryption/decryption process is finished.. The state that AESSTRT is 0000_0000H and this bit is “1” means that the encryption and decryption process is stopped (all of these processes are finished).

STRT_EN	Description
0	encryption/decryption process is operating
1	encryption/decryption process is finished (initial value)

23.2.6. Control Register (AESCTRL)

Address: 0x4000_1010
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	R_END	W_END	–*	–*	KY_SZ[1:0]		–*	–*	MK_DKY	MODE	INIT	BCMODE[2:0]		
Access	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
AESCTRL is a special function register (SFR) used to set the operation mode.

[Description of Bits]

- **BCMODE[2:0]** (bit 2 to 0)
  The BCMODE[2:0] bits are used to set the block encryption mode. When change the block encryption mode, confirming that the encryption/decryption process is stopped (that AESSTRT is 0000_00001H and AESSTAT is 0000_0001H).

BCMODE[2:0]	Description
000	ECB mode (initial value)
001	CBC mode
100	CTR mode
others	Prohibited

- **INIT** (bit 3)
  In the CBC mode, INIT is the bit to select whether to use the initial vector (IV). Set this bit “1” at the head of block (128bit), and AESIVC0-3 is used as IV when the encryption/decryption is executed. And same time, this bit is cleared to “0”.

INIT	Mode	Description
0	CBC mode	Initial vector is not used (initial value)
	ECB mode CTR mode	No effect (initial value)
1	CBC mode	Initial vector is used
	ECB mode CTR mode	No effect

- **MODE** (bit 4)
  The MODE bit is used to select which process to operate encryption or decryption.

MODE	Description
0	Encryption (initial value)
1	Decryption

- **MK_DKY** (bit 5)
  The MK_DKY is the bit to select whether to generate the new decryption key. Set this bit "1" before encryption/decryption process, and the generation of decryption key is executed. The decryption key is generated, and then this bit is cleared to "0". After that the encryption/decryption is executed. Set "1" to this bit, when encryption keys (AESEKY0 to 7) are modified.
  In the CTR mode, the decryption key is not used, but the decryption key is generated when this bit is set to "1".

MK_DKY	Description
0	Present decryption key is used (initial value)
1	New decryption key is generated

- **KY_SZ[1:0]** (bit 9 to 8)
  The KY_SZ[1:0] bits are set the key size.

KY_SZ[1:0]	Description
00	128 bits (initial value)
01	192 bits
10	256 bits
11	Invalid

- **W_END** (bit 12)
  The W_END bit is selected to convert the endian or not when writing the value to AESIVC0-3, AESBFT0-3, and AESEKY0-7.

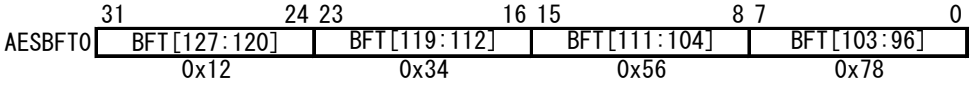
W_END	Description
0	Not convert the endian (initial value)
1	Convert the endian

- **R_END** (bit 13)
  The R_END bit is selected to convert the endian or not when reading the value from AESIVC0-3, AESBFT0-3, and AESEKY0-7.

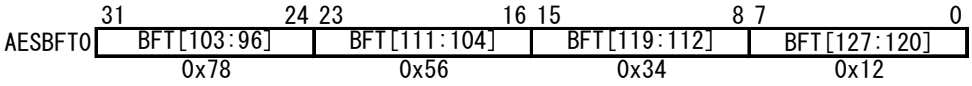
R_END	Description
0	Not convert the endian (initial value)
1	Convert the endian

[Endian conversion example]
The case that the top 32bits of BFT[127:0] are 0x1234_5678 is shown below. By W_END bit or R_END bit, the bit order of the register access is modified.

・The case of no endian conversion:W_END=0, R_END=0



・The case of endian conversion:W_END=1, R_END=1



(Setting example 1) W_END=1, R_END=0
It is used in the case below etc.
The cipher text sent from MSB by the 1 byte is decrypted, and the result (plaintext) is compared with the known value.

(Setting example 2) W_END=0, R_END=1
It is used in the case below etc.
A plaintext is encrypted, and the result (cipher text) is sent from MSB by the 1 byte.

23.2.7. Initialization Vector & Counter Register n (AESIVCn (n=0 to 3))

Address: 0x4000_1014 (AESIVC0), 0x4000_1018 (AESIVC1),
0x4000_101C (AESIVC2), 0x4000_1020 (AESIVC3)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	IVC															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	IVC															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]

AESIVCn (n=0 to 3) is special function registers (SFRs) to set the initial value of the initialization vector (IV) or the counter (Counter). The initial value (IV) is used in the CBC mode. The counter (Counter) is used in the CTR mode. This register is not used in the ECB mode.

The endian of the access to this register can be changed by W_END bit and R_END bit of AESCTRL.

Register	Bit 31 to 0
AESIVC0	IVC[127:96]
AESIVC1	IVC[95:64]
AESIVC2	IVC[63:32]
AESIVC3	IVC[31:0]

[Description of Bits]

- **IVC[127:0]**

  - CBC mode

    This register is used as the initialization vector (IV) when INIT bit of AESCTRL register is “1”.

  - CTR mode

    This register is used as the counter (Counter). IVC[15:0] is incremented by 1 whenever encryption/decryption process starts.

  - ECB mode

    This register value is ignored.

23.2.8. Before Processing Data Register n (AESBFTn (n=0 to 3))

Address: 0x4000_1024 (AESBFT0), 0x4000_1028 (AESBFT1),
0x4000_102C (AESBFT2), 0x4000_1030 (AESBFT3)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	BFT															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	BFT															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
AESBFTn (n=0 to 3) is special function registers (SFRs) to set the plain text for the encryption processes or the cipher text for the decryption processes.
The endian of the access to this register can be changed by W_END bit and R_END bit of AESCTRL.

Register	Bit 31 to 0
AESBFT0	BFT[127:96]
AESBFT1	BFT[95:64]
AESBFT2	BFT[63:32]
AESBFT3	BFT[31:0]

[Description of Bits]

- **BFT[127:0]**
  - Encryption
    Set the plain text (128bit).

  - Decryption
    Set the cipher text (128bit).

23.2.9. After Processing Data Register n (AESAFTn (n=0 to 3))

Address: 0x4000_1034 (AESAFT0), 0x4000_1038 (AESAFT1),
0x4000_103C (AESAFT2), 0x4000_1040 (AESAFT3)
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	AFT															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	AFT															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
AESAFTn (n=0 to 3) is special function registers (SFRs) to indicate the result of encryption/decryption.
The lower 128-u bits of the last block in CTR mode are invalid data.(processing data: u bit).
The endian of the access to this register can be changed by R_END bit of AESCTRL.

Register	Bit 31 to 0
AESAFT0	AFT[127:96]
AESAFT1	AFT[95:64]
AESAFT2	AFT[63:32]
AESAFT3	AFT[31:0]

[Description of Bits]

- **AFT[127:0]**
  - Encryption
    These bits are indicated the cipher text (128bits) as an encryption result.

  - Decryption
    These bits are indicated the plain text (128bits) as a decryption result.

23.2.10. Encryption Key Register n (AESEKYn (n=0 to 7))

Address: 0x4000_1044 (AESEKY0), 0x4000_1048 (AESEKY1),
0x4000_104C (AESEKY2), 0x4000_1050 (AESEKY3),
0x4000_1054 (AESEKY4), 0x4000_1058 (AESEKY5),
0x4000_105C (AESEKY6), 0x4000_1060 (AESEKY7)
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	EKY															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	EKY															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
AESKEYn (n=0 to 7) is special function registers (SFRs) to set the encryption key. When reading this register, the data is 0x0000_0000.
The endian of the access to this register can be changed by W_END bit of AESCTRL.

Register	Bit 32 to 0
AESEKY0	EKY[255:224]
AESEKY1	EKY[223:192]
AESEKY2	EKY[191:160]
AESEKY3	EKY[159:128]
AESEKY0	EKY[127:96]
AESEKY1	EKY[95:64]
AESEKY2	EKY[63:32]
AESEKY3	EKY[31:0]

[Description of Bits]

- **EKY[255:0]**
  - 128 bit length key
    Set the encryption key (128 bit) to EKY[255:128] of AESEKY0-3.

  - 192 bit length key
    Set the encryption key (192 bit) to EKY[255:64] of AESEKY0-5.

  - 256 bit length key
    Set the encryption key (256 bit) to EKY[255:0] of AESEKY0-7.

23.3. Description of Operation

23.3.1. AES basic control flow

Table 23-1 shows Control register (AESCTRL) setting examples.

Table 23-1 Control register (AESCTRL) setting examples

Block encryption mode	Encryption/ Decryption	AESCTRL setting example	KY_SZ [1:0]	MK_DKY	MODE	INIT	BCMODE [2:0]
ECB	Encryption	0000_0000H	00 to 10	D.C.	0	D.C.	000
	Decryption	0000_0030H		1[*1]	1		
CBC	Encryption	0000_0009H		D.C.	0	1[*2]	001
	Decryption	0000_0039H		1[*1]	1		
CTR	Encryption	0000_0004H		D.C.	0	D.C.	100
	Decryption	0000_0014H			1		

D.C : Don't care

[*1]: Set to "1", when setting a new encryption key or changing the encryption key. Before encryption/decryption, the decryption key is generated, and this bit is cleared to "0".
[*2]: Set to "1" at the top block. When the encryption/decryption process starts, this bit is cleared to "0".

Figure 23-2 shows a basic control flow (block encryption mode).

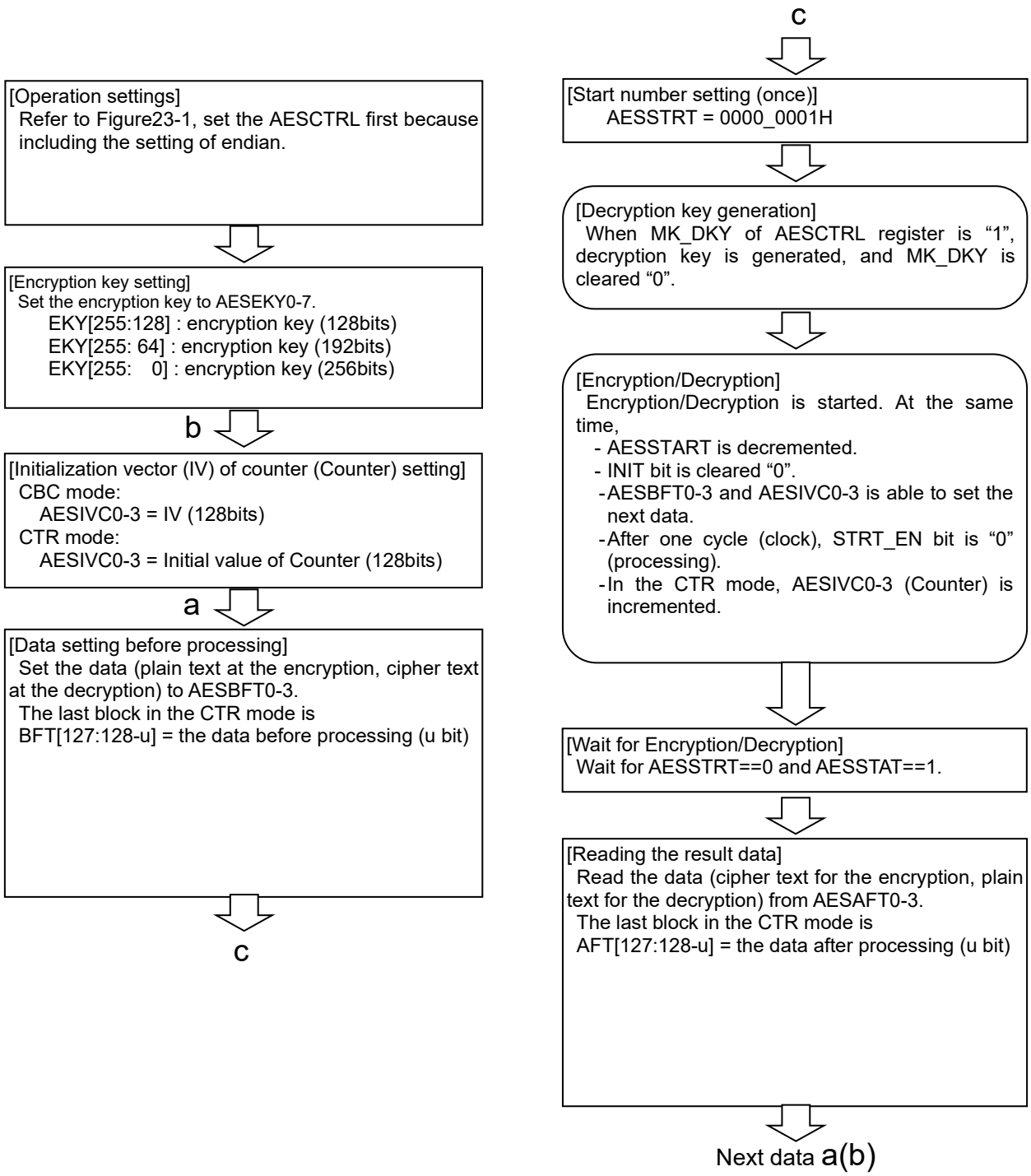


Figure 23-2 basic control flow (block encryption mode)

23.3.2. AES encryption

Figre23-3 shows explanation of the AES encryption.

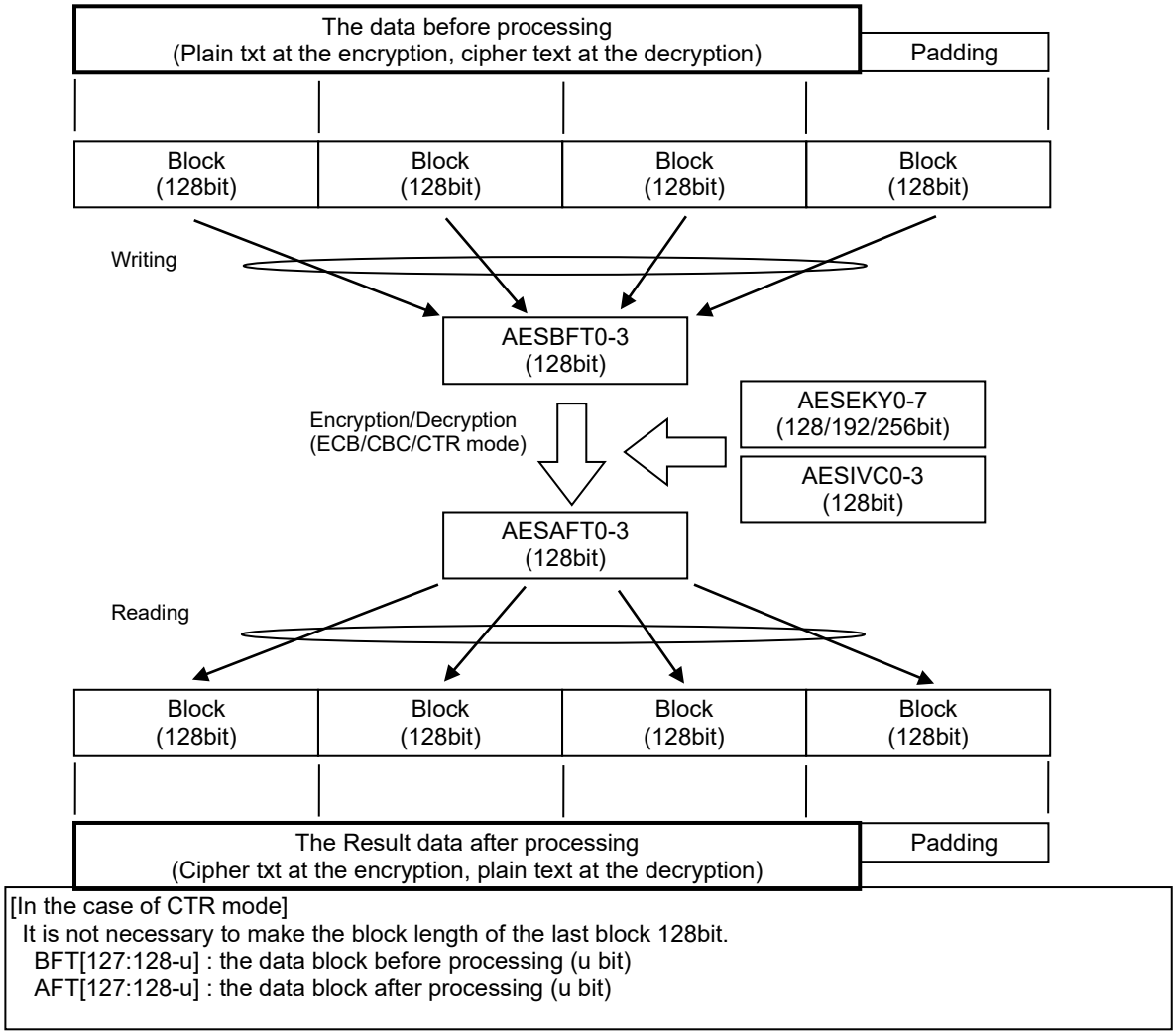


Figure 23-3 explanation of the AES encryption.

23.3.3. Interrupt

Figure 23-4 shows the behavior of IRQ_ALL and IRQ_EVRY bit of AESIREQ register.

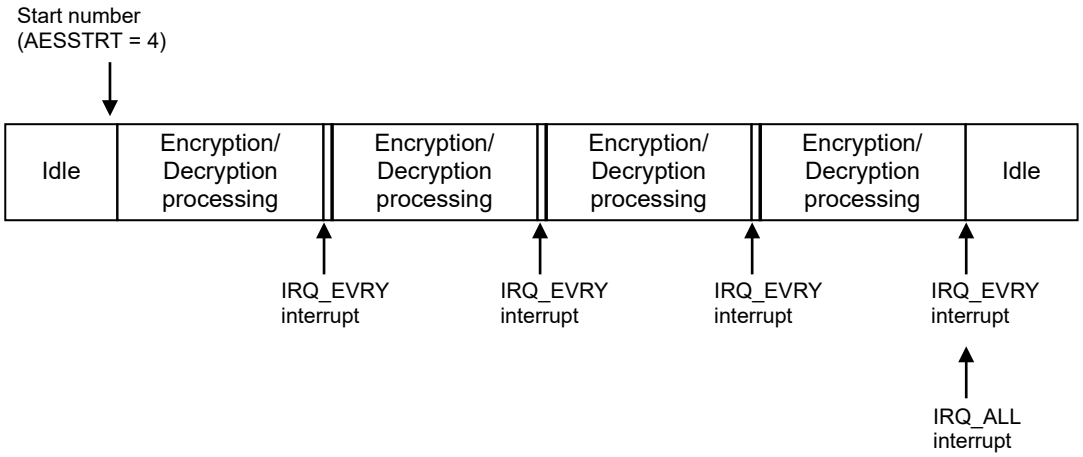


Figure 23-4 explanation of the AES encryption.

Chapter 24

Random Number Generator

24. Random Number Generator

24.1. Overview

This block is a random number generation circuit.

24.1.1. Features

- Generates 8-bit random numbers.

24.1.2. Configuration

Figure 24-1 shows the configuration of the reset generation circuit.

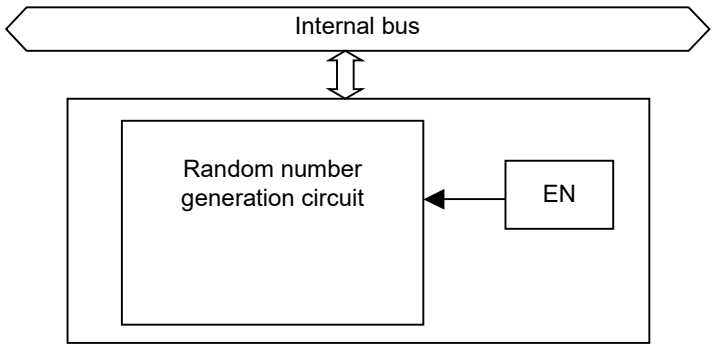


Figure 24-1 Configuration of RANDOM

24.2. Description of Registers

24.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4000_1800	Random number generation register	RNDDT	R	32	Undefined
0x4000_1804	Random number generation enable register	RNDEN	R/W	32	0x0000_0000

24.2.2. Random Number Generating Register (RNDDT)

Address: 0x4000_1800
Access: R/W
Access size: 32 bit
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	RNDDT[7:0]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	← Undefined →							

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

When the register is accessed consecutively for a short period of time, values containing similar bit patterns may be output.
When accessing this register for read, provide an interval of 10 instructions (200 ns) or more from the last access to the registers (RNDDT, RNDEN) of this module.

[Description of Register]
RNDDT can be used to read random numbers that are output by the random number generating circuit.

24.2.3. Random Number Generating Enable Register (RNDEN)

Address: 0x4000_1804
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	EN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RNDEN sets the operation of the random number generating circuit.

[Description of Bits]
• **EN** (bit 0)
This bit is used to start/stop the random number generating circuit.
Power consumption can be controlled by stopping the circuit.
When the setting of this bit is changed from "0" (stop) to "1" (start), provide an interval of 10 instructions (200 ns) or more after the setting change before performing reading of the RND register.

EN	Description
0	Stops the random number generating circuit (initial value)
1	Starts the random number generating circuit

Chapter 25

RC Oscillation type A/D Converter(RC-ADC)

25. RC Oscillation Type A/D Converter (RC-ADC)

25.1. General Description

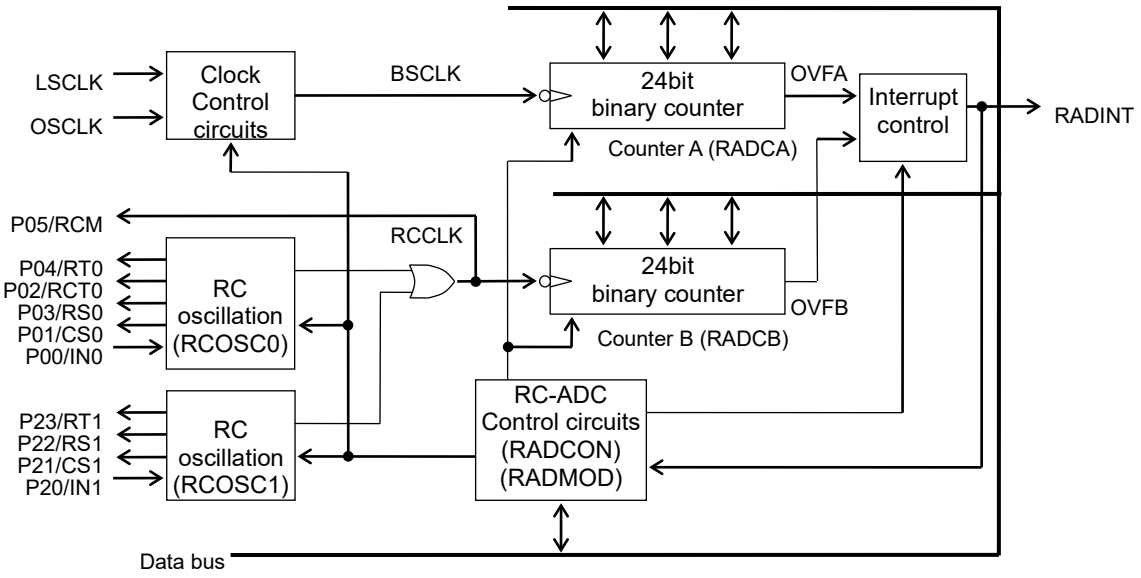
The RC oscillation type A-D Converter (RC-ADC) converts resistance values or capacitance values to digital values by counting the oscillator clock whose frequency changes according to the resistor or capacitor connected to the RC oscillator circuits. By using a thermistor or humidity sensor as a resistor, a thermometer or hygrometer can be formed.
In addition, a different sensor for each of the two channels of RC-ADC's RC oscillator circuit can be used to broaden RC-ADC applications; for example, the converter can be used for expansion of measurement range or measurement at two points.
For input clocks, see Chapter 6, "Clock Generation Circuit".

25.1.1. Features

- 2-channel system by time division

25.1.2. Configuration

The RC-ADC consists of two RC oscillator circuits to form two channels, Counter A (RADCA) and Counter B (RADCB) as 24-bit binary counters, and an RC-ADC control circuit (RADCON, RADMOD). Figure 25-1 shows the configuration of the RC-ADC.



RADMOD : RC-ADC mode register
RADCONL : RC-ADC control register
RADCA : RC-ADC counter A register
RADCB : RC-ADC counter B register

Figure 25-1 Configuration of RC-ADC

25.1.3. List of Pins

Pin name	I/O	Function
IN0	I	Channel 0 oscillation input pin
CS0	O	Channel 0 reference capacitor connection pin
RS0	O	Channel 0 reference resistor connection pin
RCT0	O	Pin for connection with a resistive/capacitive sensor for measurement on Channel 0
RT0	O	Pin for connection with a resistive sensor for measurement on Channel 0
RCM	O	RC oscillation monitor pin Used as the secondary function of the P05 pin.
IN1	I	Channel 1 oscillation input pin
CS1	O	Channel 1 reference capacitor connection pin
RS1	O	Channel 1 reference resistor connection pin
RT1	O	Channel 1 resistive sensor for measurement connection pin

25.2. Description of Registers

25.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4200_0000	RC-ADC counter A register	RADCA	R/W	32	0x0000_0000
0x4200_0004	RC-ADC counter B register	RADCB	R/W	32	0x0000_0000
0x4200_0008	RC-ADC mode register	RADMOD	R/W	32	0x0000_0000
0x4200_000C	RC-ADC control register	RADCON	R/W	32	0x0000_0000
0x4200_0010	RC-ADC trigger register	RADTRG	R/W	32	0x0000_0000
0x4200_0020	RC-ADC continuous measurement 0 register	RADCM0	R/W	32	0x0000_0000
0x4200_0024	RC-ADC continuous measurement 1 register	RADCM1	R/W	32	0x0000_0000
0x4200_0028	RC-ADC continuous measurement 2 register	RADCM2	R/W	32	0x0000_0000
0x4200_002C	RC-ADC continuous measurement 3 register	RADCM3	R/W	32	0x0000_0000
0x4200_0030	RC-ADC continuous measurement 4 register	RADCM4	R/W	32	0x0000_0000
0x4200_0040	RC-ADC result counter register	RADRC	R	32	0x0000_0000

25.2.2. RC-ADC Counter A Register (RADCA)

Address: 0x4200_0000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	RADCA[23:16]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	RADCA[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADCA is a special function register (SFR) used to read from and write to the Counter A of the RC-ADC.
RADCA is a 24-bit binary counter.

[Note]
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

25.2.3. RC-ADC Counter B Register (RADCB)

Address: 0x4200_0004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	RADCB[23:16]							
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	RADCB[15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADCB is a special function register (SFR) used to read from and write to the Counter B of the RC-ADC.
RADCB is a 24-bit binary counter.

[Note]
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

25.2.4. RC-ADC Mode Register (RADMOD)

Address: 0x4200_0008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	RACK[2:0]			RADI	OM[3:0]			
Access	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADMOD is a special function register (SFR) used to select the A/D conversion mode of the RC-ADC.

[Description of Bits]

- **OM[3:0]** (bits 3 to 0)
  OM[3:0] is used to select the oscillation mode for the RC oscillation circuit.

OM[3]	OM[2]	OM[1]	OM[0]	Description
0	0	0	0	IN0 pin external clock input mode (initial value)
0	0	0	1	RS0-CS0 oscillation mode
0	0	1	0	RT0-CS0 oscillation mode
0	0	1	1	RT0-1-CS0 oscillation mode
0	1	0	0	RS0-CT0 oscillation mode
0	1	0	1	RS1-CS1 oscillation mode
0	1	1	0	RT1-CS1 oscillation mode
0	1	1	1	IN1 pin external clock input mode
1	*	*	*	Prohibited

- **RADI** (bit 4)
  The RADI bit is used to choose whether to generate the RC-ADC interrupt request signal (RADINT) by an overflow at Counter A or Counter B.

RADI	Description
0	Generates an interrupt request by Counter A overflow (initial value)
1	Generates an interrupt request by Counter B overflow

- **RACK[2:0]** (bits 7 to 5)
  RACK[2:0] bits are used to select the base clock of Counter A (BSCLK).

RACK[2]	RACK[1]	RACK[0]	Description
0	0	0	LSCLK (initial value)
0	0	1	OSCLK
0	1	0	1/2OSCLK
0	1	1	1/4OSCLK
1	0	0	1/8OSCLK
1	0	1	1/16OSCLK
1	1	0	1/32OSCLK
1	1	1	1/64OSCLK

25.2.5. RC-ADC Control Register (RADCON)

Address: 0x4200_000C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RARUN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADCON is a special function register (SFR) used to control A/D conversion operation of the RC-ADC.

[Description of Bits]

- **RARUN** (bit 0)
  The RARUN bit is used to start or stop A/D conversion of the RC-ADC. Set RARUN to "1" to start the A/D conversion, and "0" to stop it. If Counter A or Counter B overflows with RARUN set to "1", the bit is automatically reset to "0".
  RARUN is set to "0" at system reset.

RARUN	Description
0	Stops A/D conversion (initial value)
1	Starts A/D conversion

[Note]
If you set RARUN to "0" to stop the conversion, set RRAD of RSTCON to "1" and CRAD of CLKCON to "0" to stop the operation once. When you want to start it again, set CRAD of CLKCON to "1" and RRAD of RSTCON to "0", set registers again, and then set RARUN to "1".
When the RAST0 bit of the RC-ADC trigger register (RADTRG) is set to "1", writing to the RARUN bit is disabled.

25.2.6. RC-ADC Trigger Register (RADTRG)

Address: 0x4200_0010
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	RASTS [4:0]					–*	–*	–*	–*	–*	–*	–*	RAST0
Access	–	–	–	R/W	R/W	R/W	R/W	R/W	–	–	–	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADTRG is a special function register (SFR) used to select the external trigger for the A/D conversion.

[Description of Bits]

- **RAST0** (bit 0)
  This bit is used to select the A/D conversion start mode.

RAST0	Description
0	Normal mode (initial value) RARUN of the RADCON register is set to "1" using the software to start the A/D conversion.
1	Trigger mode RARUN is set to "1" by the trigger event selected in RASTS to start the A/D conversion. Even if another trigger event occurs during the A/D conversion (when SARUN is "1"), it is ignored, and the running A/D conversion continues. Also, consecutive A/D conversion and control of RARUN by the software are not available.

- **RASTS[4:0]** (bits 12 to 8)
  This bit is used to select a trigger event for the A/D conversion.

RASTS[4]	RASTS[3]	RASTS[2]	RASTS[1]	RASTS[0]	Description
0	0	0	0	0	TM0INT
0	0	0	0	1	TM1INT
0	0	0	1	0	TM2INT
0	0	0	1	1	TM3INT
0	0	1	0	0	TM4INT
0	0	1	0	1	TM5INT
0	0	1	1	0	TM6INT
0	0	1	1	1	TM7INT
0	1	*	*	*	prohibited
1	0	0	0	0	FTM0TGO
1	0	0	0	1	FTM1TGO
1	0	0	1	0	FTM2TGO
1	0	0	1	1	FTM3TGO
1	0	1	*	*	prohibited
1	1	*	*	*	prohibited

[Note]

- Modifying the RASTS bits under RAST0=0. It is prohibited that this bits setting and RAST0=1 are set at the same time.
- The timer interrupt request (TM0-7INT) is an interrupt request signal independent of the interrupt enabled/disabled setting of the interrupt enable register. The function timer trigger output (FTM0-3TGO) is a signal specific to the trigger event.
- If a prohibited setting is specified, the A/D conversion is not started by any trigger event.

25.2.7. RC-ADC Continuous Measurement Register n (RADCMn) n=0 to 4

Address: 0x4200_0020 (RADCM0), 0x4200_0024 (RADCM1), 0x4200_0028 (RADCM2), 0x4200_002C (RADCM3), 0x4200_0030 (RADCM4)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	RADVn	–*	RADCVn	RADIn	OMn[3:0]				RADCn [23:16]							
Access	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	RADCn [15:0]															
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADCMn (n=0 to 4) is a special function register (SFR) used to configure up to four consecutive A/D conversions.

[Description of Bits]

- **RADCn[23:0]** (n=0 to 4, bits 23 to 0)
  RADCn[23:0] are used to set a reference counter value.
  In case of A reference, the counter value of B reference is 0x0000_0000, and in case of B reference, the counter value of A reference is 0x0000_0000.

- **OMn[3:0]** (n=0 to 4, bits 27 to 24)
  OMn[3:0] is used to select the oscillation mode for the RC oscillation circuit.

OMn[3]	OMn[2]	OMn[1]	OMn[0]	Description
0	0	0	0	IN0 pin external clock input mode (initial value)
0	0	0	1	RS0-CS0 oscillation mode
0	0	1	0	RT0-CS0 oscillation mode
0	0	1	1	RT0-1-CS0 oscillation mode
0	1	0	0	RS0-CT0 oscillation mode
0	1	0	1	RS1-CS1 oscillation mode
0	1	1	0	RT1-CS1 oscillation mode
0	1	1	1	IN1 pin external clock input mode
1	*	*	*	prohibited

- **RADIn** (n=0 to 4, bit 28)
  The RADIn bit is used to choose whether to stop the counter by an overflow at Counter A or Counter B.

RADIn	Description
0	Stops the count by Counter A overflow (initial value)
1	Stops the count by Counter B overflow

- **RADCVn** (n=1 to 4, bit 29)
  RADCVn is used to select the counter setting value.

RADCVn	Description
0	Values of RADCn[23:0] (initial value)
1	0x0100_0000 - (Result of n-1 channel)

[Note]
Set this bit to "0" for channel 0. When setting it to "1", RADCn[23:0] is set.

- **RADVn** (n=0 to 4, bit 31)
  RADVn is used to select enable/disable of RADCn, RADIn, and OMn.
  The operation is performed for channels where this bit is set to "1", starting from the smallest channel number.

RADVn	Description
0	This register setting disabled (initial value)
1	This register setting enabled

25.2.8. RC-ADC Result Counter Register (RADRC)

Address: 0x4200_0040
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	RADC [23:16]							
Access	–	–	–	–	–	–	–	–	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	RADC [15:0]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
RADC is a special function register used to read the counter values of channels enabled in RADCM0-4 (RADVn="1").
They can be read starting from the smallest channel number where RADVn=1.

[Note]
The count value can be read after the A/D conversion completes (RARUN = 0).

25.3. Description of Operation

Counter A (RADCA) is a 24 bit binary counter for counting the base clock (BSCLK), which is used as the standard of time. Counter A can count up to 0FFFFFFH.
Counter B (RADCB) is a 24 bit binary counter for counting the oscillator clock (RCCLK) of the RC oscillator circuits. Counter B can count up to 0FFFFFFH.
Counters A and B are provided with overflow flags (OVFA and OVFB, respectively). Each overflow output generates an RC-ADC interrupt request signal (RADINT). RADI bit of RC-ADC mode register (RADMOD) selects which of the counter A side or the counter B side generates the interrupt by overflow.
The overflow of Counter A is selected by setting RADI to “0”.
The overflow of Counter B is selected by setting RADI to “1”

The RARUN bit of the RC-ADC control register (RADCONL) is used to start or stop RC-ADC conversion operation. When RARUN is set to “0”, the oscillator circuits stop, so that counting will not be performed. When RARUN is set to “1”, RC oscillation starts. The count of the oscillation clock(RCCLK) and the count of the base clock(BSCLK) are started by counter B and counter A.

The RC oscillation section has a total of eight types of oscillation modes based on the two oscillator circuits of RCOSC0 and RCOSC1. These modes are selected by the RC-ADC mode register (RADMOD).
When RC oscillation circuit (RCOSC0) is used, set “P00 to P04” to secondary function. When ROSC1 is used, set “P20 to P23” to secondary function. When RC monitor pin (RCM), which outputs RC oscillation waveform, is used, set P05 to secondary function.
For the RC oscillator circuit configuration, see "25.1.2 Configuration". For the secondary functions of Port 0 and Port2, see Chapter 22, “Port”.

25.3.1. RC Oscillator Circuits

RC-ADC performs A/D conversion by converting the oscillation frequency ratio between a reference resistor (or capacitor) and a resistive sensor (or capacitive sensor) such as a thermistor to digital data.
By making RC oscillation occur both on the reference side and on the sensor side with the reference capacitor the error factor that the RS oscillator circuit itself is eliminated, thereby making it possible to perform the A/D conversion of the characteristics of the sensor itself.
Also, by calculating the ratio between the oscillation frequency on the reference side and that on the sensor side and then calculating the correlation between the calculated ratio and temperatures that the sensor characteristics have in advance, a temperature can be obtained based on that calculated ratio.
Table 25-1 lists the eight types of oscillation modes, one of which is selected by the RC-ADC mode register (RADMOD) OM[3:0] bits.

Table 25-1 Oscillation Modes from Which Selection Is Made by OM[3:0] Bits

mode No.	RADMOD				RCOSC0 output pin				RCOSC1 output pin			mode	
	OM3	OM2	OM1	OM0	RS0	RT0	RCT0	CS0	RS1	RT1	CS1		
0	0	0	0	0	Z	Z	Z	Z	Z	Z	Z	IN0 External clock input mode	
1	0	0	0	1	1/0	Z	Z	0/1	Z	Z	Z	RS0–CS0 oscillation	RCOSC0 oscillation mode
2	0	0	1	0	Z	1/0	Z	0/1	Z	Z	Z	RT0–CS0 oscillation	
3	0	0	1	1	Z	Z	1/0	0/1	Z	Z	Z	$RT_{0\text{-}1}$–CS0 oscillation	
4	0	1	0	0	1/0	Z	0/1	Z	Z	Z	Z	RS0–CT0 oscillation	
5	0	1	0	1	Z	Z	Z	Z	1/0	Z	0/1	RS1–CS1 oscillation	RCOSC1 oscillation mode
6	0	1	1	0	Z	Z	Z	Z	Z	1/0	0/1	RT1–CS1 oscillation	
7	0	1	1	1	Z	Z	Z	Z	Z	Z	Z	IN1 External clock input mode	
8	1	*	*	*	Z	Z	Z	Z	Z	Z	Z	(Prohibited)	

Note) * : Indicates arbitrary.
Z : Indicates high-impedance output.
1/0, 0/1 : Indicates active output.
(Prohibited) : The oscillator clock is not supplied even by setting the RARUN bit to "1" or by starting A/D conversion.

In Table 25-1, mode No.0 and mode No.7 are modes where external clocks to be input to the IN0 or IN1 pin are used for measurement with the RC oscillator circuit stopped.
As shown in Table 25-1, the two oscillator circuits, RCOSC0 and RCOSC1, are so specified that they cannot operate concurrently in order to prevent interference in oscillation from occurring when they oscillate concurrently.
The relationship between an oscillation frequency f_{RCCLK} and an RC constant is expressed by the following equation:

$$\frac{1}{f_{RCCLK}} = t_{RCCLK} = k_{RCCLK} \cdot R \cdot C$$

The t_{RCCLK} is the period of the oscillator clock, k_{RCCLK} the proportional constant, and R x C the product of capacitances CS, CT, (CS+CVR) and (CT+CVR) and resistances RS and RT. The value of k_{RCCLK} slightly changes depending on the value of the supply voltage VDD, RI, R, or C.
Table 25-2 lists the typical k_{RCCLK} values.

Table 25-2 Typical Values of the Proportional Constant k_{RCCLK} of RC Oscillator Circuits

VDD (V)	CSn, CTn (pF)	CVRn (pF)	RSn, RTn (kΩ)	k_{RCCLK} (Typ.)
3	560	820	100	1.2
	560	820	10	1.2

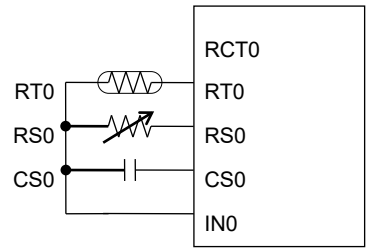
Note) n = 0, 1, 0-1

[Note]

•Pins that are to be used for the RC-ADC function must be configured as secondary function input or output using the mode register (P0MOD, P2MOD) of the corresponding port.

•All the Port 3 pins except P05/RCM (see Section 25.1.3, “List of Pins”) are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, the Port 0 pins except P05 cannot be used as their primary functions in oscillation mode No. 0, 1, 2, 3 or 4, which is selected by the RADMOD register. In the same way, the P20 to P23 pins of Port 2 cannot be used as their primary functions in oscillation mode No. 5, 6 or 7.

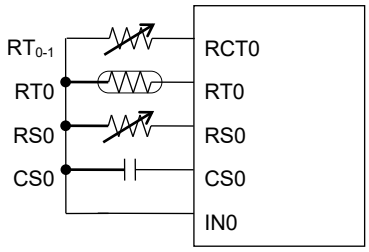
Figures 25-2 to 25-5 show the oscillator circuit configurations, the modes of oscillation for each configuration, and the OM3–0 bit settings.



OM[3]	OM[2]	OM[1]	OM[0]	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0

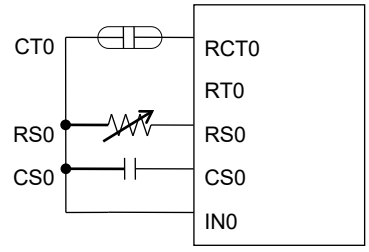
Figure 25-2 When RCOSC0 Is Used for Measurement with One Resistive Sensor

[Note]
The unused pin RCT0 shown in the Figure 25-2 is configured as a pin dedicated to the RC-ADC function during A/D conversion. Therefore, RCT0 cannot be used as a primary function port (P02) during A/D conversion.



OM[3]	OM[2]	OM[1]	OM[0]	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0
0	0	1	1	Oscillates with the reference resistor RT_{0-1} and CS0

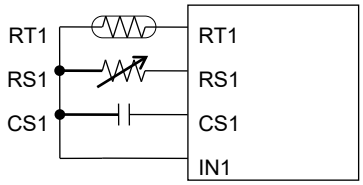
Figure 25-3 When RCOSC0 Is Used for Measurement with One Resistive Sensor
(Two points are adjusted with two reference resistors)



OM[3]	OM[2]	OM[1]	OM[0]	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	1	0	0	Oscillates with the sensor RS0 and CT0

Figure 25-4 When RCOSC0 Is Used for Measurement with One Capacitive Sensor

[Note]
The unused pin RT0 shown in the Figure 25-4 is configured as a pin dedicated to the RC-ADC function during A/D conversion. Therefore, RT0 cannot be used as a primary function port (P04) during A/D conversion.



OM[3]	OM[2]	OM[1]	OM[0]	oscillation mode
0	1	0	1	Oscillates with the reference resistor RS1 and CS1
0	1	1	0	Oscillates with the sensor RT1 and CS1

Figure 25-5 When RCOSC1 Is Used for Measurement with One Resistive Sensor

25.3.2. Counter A/B Reference Modes

There are the following two modes of RC-ADC conversion operation:

- Counter A reference mode (RADMOD RADI = "0")
  In this mode, a gate time is determined by Counter A and the base clock (BSCLK), which is used as the time reference, then the RC oscillator clock (RCCLK) is counted by Counter B within the gate time to make the content of Counter B the A/D conversion value.
  The A/D conversion value is proportional to RC oscillation frequency.

- Counter B reference mode (RADMOD RADI = "1")
  In this mode, a gate time is determined by Counter B and the RC oscillator clock (RCCLK), and the base clock (BSCLK), which is used as the time reference, is counted by Counter A within the gate time to make the content of Counter A the A/D conversion value.
  The A/D conversion value is inverse proportional to RC oscillation frequency.

(1) Operation in Counter A reference mode

Figure 25-6 shows the operation timing in Counter A reference mode.
Following is an example of operation procedure in Counter A reference mode:

①Preset to Counter A (RADCA0 and RADCA1) the value obtained by subtracting the count value "nA0" from the maximum value + 1 (1000000H). The product of the count value "nA0" and the BSCLK clock cycle indicates the gate time.
②Preset "000000H" in Counter B (RADCB0 and RADCB1).
③Set the OM3–OM0 bit of RADMOD to desired oscillation mode. (See Table 25-1)
④Set the RADI bit of RADMOD to "0" to specify generating of an interrupt request signal by Counter A overflow.
⑤Set the RARUN bit of RADCONL to "1" to start A/D conversion.

Counter A starts counting of the base clock (BSCLK) when RARUN is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to "1". When Counter A overflows, the RARUN bit is automatically reset to "0" (⑥) and counting is terminated. At the same time, an RC-ADC interrupt request (RADINT) occurs (⑦).

When the RCON signal is set to "1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When the RARUN bit is reset to "0" due to overflow of Counter A, RC oscillation stops and Counter B stops counting.
The final count value "nB0" of Counter B is the RCCLK count value during the gate time "nA0 x t_{BSCLK}" and is expressed by the following expression:

$$nB0 \cong nA0 \bullet \frac{t_{BSCLK}}{t_{RCCLK}} \propto f_{RCCLK}$$

The t_{BSCLK} indicates the BSCLK period and t_{RCCLK} the RCCLK period. That is, "nB0" is a value proportional to the RC oscillation frequency f_{RSCLK}.

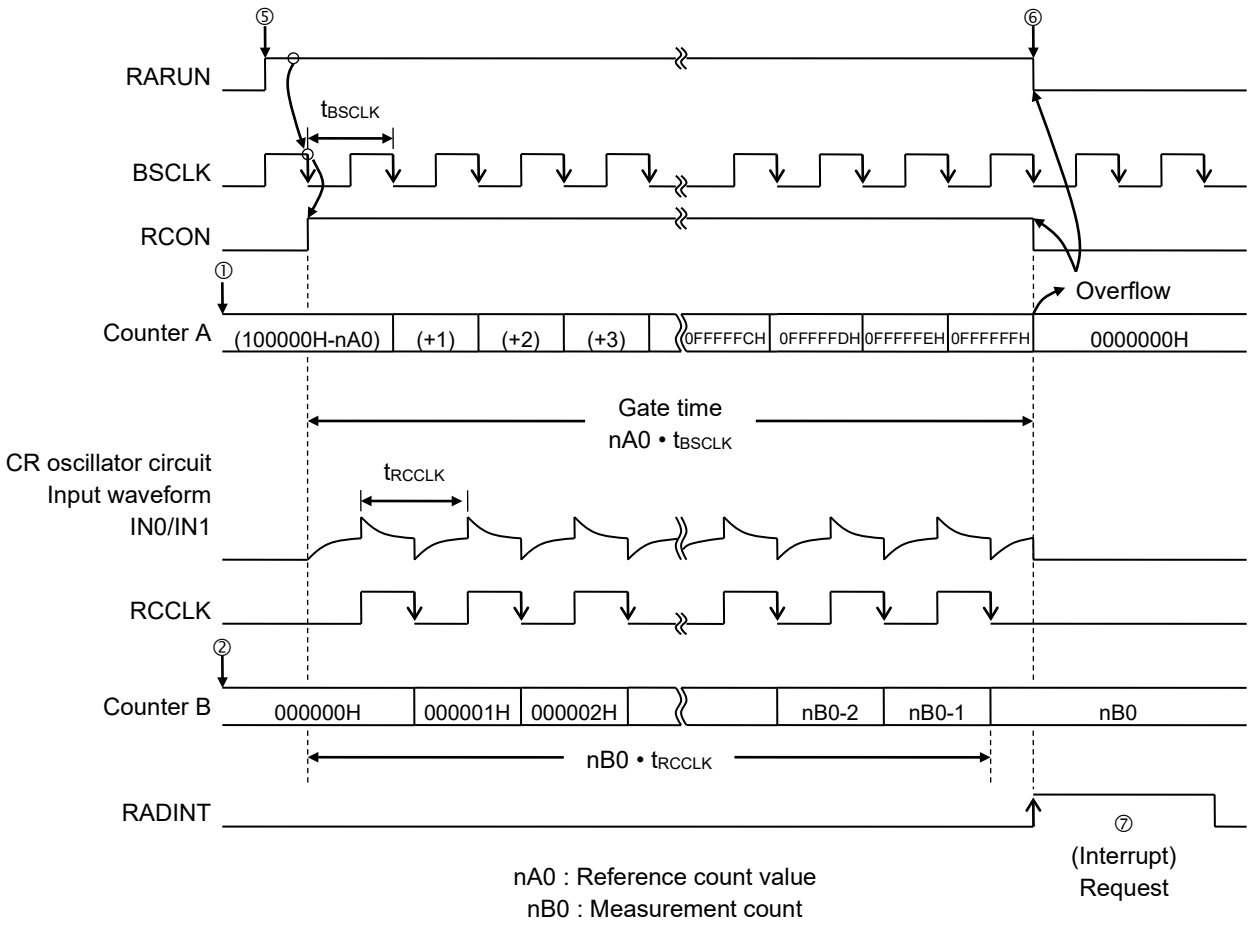


Figure 25-6 Operation Timing in Counter A Reference Mode

(2) Operation in Counter B reference mode

Figure 25-7 shows the operation timing in Counter B reference mode.
Following is an example of operation procedure in Counter B reference mode:

①Preset to Counter B (RADCB) the value obtained by subtracting the count value "nB1" from the maximum value + 1 (1000000H). The product of the count value "nB1" and the RCCLK clock cycle indicates the gate time.
②Preset "000000H" in Counter A (RADCA).
③Set the OM[3:0] bit of RADMOD to desired oscillation mode. (See Table 25-1)
④Set the RADI bit of RADMOD to "1" to specify generating of an interrupt request signal by Counter B overflow.
⑤Set the RARUN bit of RADCON to "1" to start A/D conversion.

When the RARUN bit is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to"1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When Counter B overflows, the RARUN bit is automatically reset (⑥) and conversion operation terminates. At the same time, an RC-ADC interrupt request (RADINT) occurs. (⑦)

When the RCON signal is set to "1", Counter A starts counting of the base clock (BSCLK). When the RARUN bit is reset due to overflow of Counter B, Counter A stops counting.
The final count value "nA1" of Counter A is the CLK count value during the gate time "nB1 x t_{RCCLK}" and is expressed by the following expression:

$$nA1 \cong nB1 \bullet \frac{t_{RCCLK}}{t_{BSCLK}} \propto \frac{1}{f_{RCCLK}}$$

That is, "nA1" is a value inversely proportional to the RC oscillation frequency f_{RCCLK}.

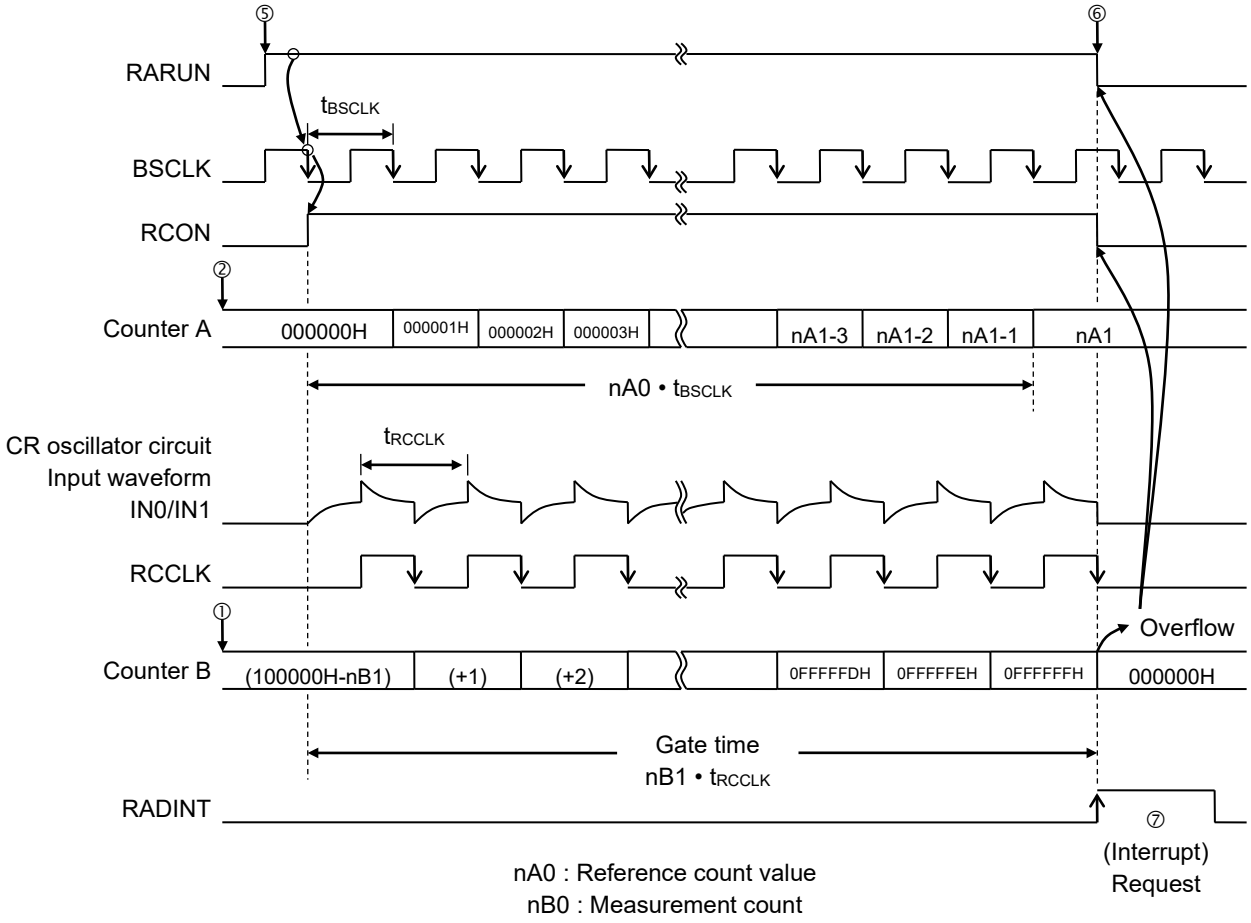


Figure 25-7 Operation Timing in Counter B Reference Mode

25.3.3. Example of Use of RC Oscillation Type A/D Converter

This section describes the method of performing A/D conversion for sensor values in Counter A and B reference modes by taking temperature measurement by a thermistor as an example.
Figure 25-8 shows the configuration of 1-thermistor RC oscillator circuit using RCOSC0.

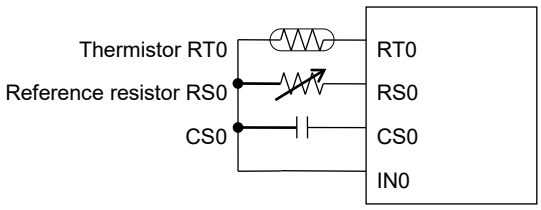


Figure 25-8 Configuration of 1-Thermistor RC Oscillator Circuit Using RCOSC0

Figure 25-9 shows the temperature characteristics of the thermistor resistance RT0.

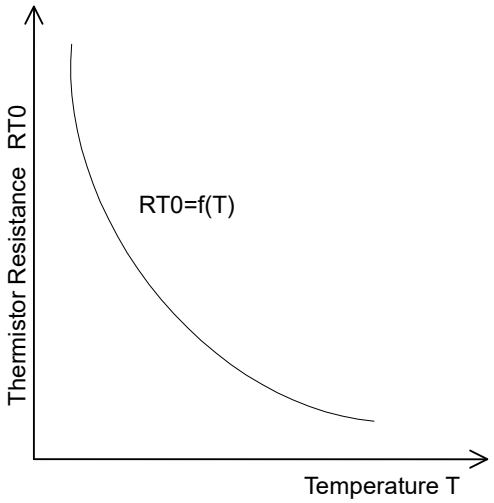


Figure 25-9 Temperature Characteristics of Thermistor

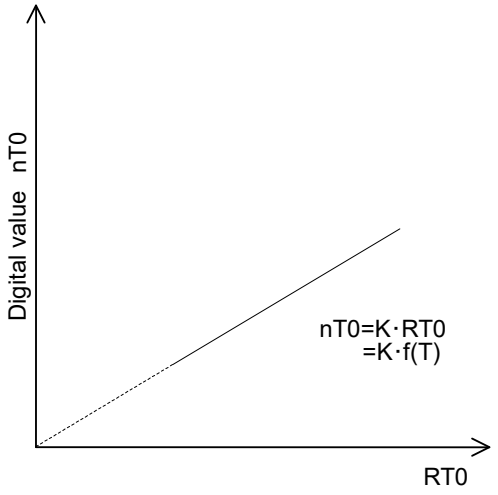


Figure 25-10 A/D Conversion Characteristics (Ideal characteristics when nT0 is proportional to RT0)

RT0 is expressed as a function of temperature T by the following equation:

$$RT0 = f(T)$$

Figure 25-10 shows the ideal characteristics of A/D conversion with the assumption that RT0 is an analog quantity. In the ideal characteristics, the A/D conversion value nT0 will purely depend on RT0 only. Assuming that nT0 is proportional to RT0, let proportional constant be K, then nT0 has the following relationship with temperature T:

$$nT0 = K \cdot RT0 = K \cdot f(T) \quad \text{... Expression A}$$

Therefore, temperature T can be expressed as a digital value by performing the conversion processing that accord with the characteristics shown in Figure 25-9 for nT0 by software.

To convert from an RT0 value to a digital value, the ratio is used between a) the RC oscillation frequency by the thermistor connected to the RT0 pin and the capacitor connected to the CS0 pin and b) the oscillation frequency by the reference resistor (which ideally should have no temperature characteristics) connected to the RS0 pin and the capacitor connected to the CS0 pin. This is for making the conditions other than resistance equal to eliminate the error factor in RC oscillation characteristics.
As shown in Figures 25-9 and 25-11, the RT0 value depends on temperature T and the RS0 value is assumed to be constant regardless of temperature T. It is ideal if the characteristics of the oscillation frequency f_{OSC} to temperature T using these resistances will be like the solid lines in Figures 25-12 and 25-13; however, in reality, it would appear that they will be like the dotted lines due to error factors such as IC temperature characteristics. Since the condition of f_{RCCLK} (RT0) and that of f_{RCCLK} (RS0) are the same except for the resistances, the error ratios are almost the same; therefore, errors can almost be eliminated by using the ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0).

The ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0) is equivalent to the above-mentioned A/D conversion value nT0 that should ideally depend only on RT0.

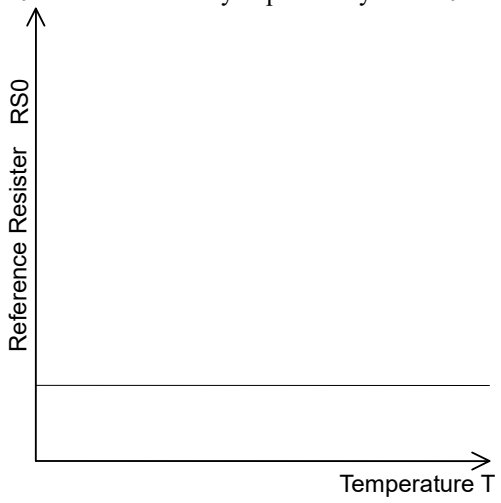


Figure 25-11 Temperature Characteristics of Reference Resistor

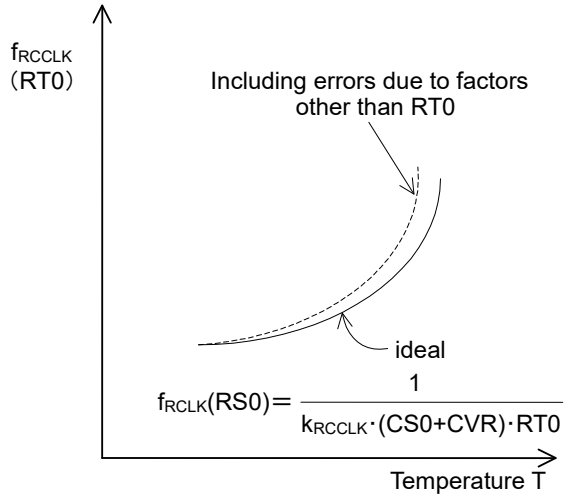


Figure 25-12 Oscillation Characteristics of Thermistor

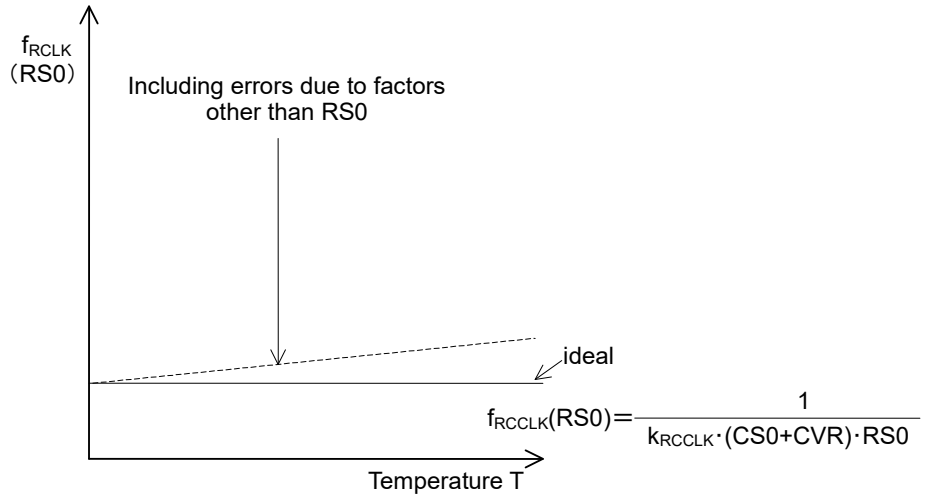


Figure 25-13 Oscillation Characteristics of Reference Resistor

Figure 25-14 shows, as an example of method, a timing diagram of one cycle of conversion from analog value RT0 to a digital value, that is, A/D conversion.

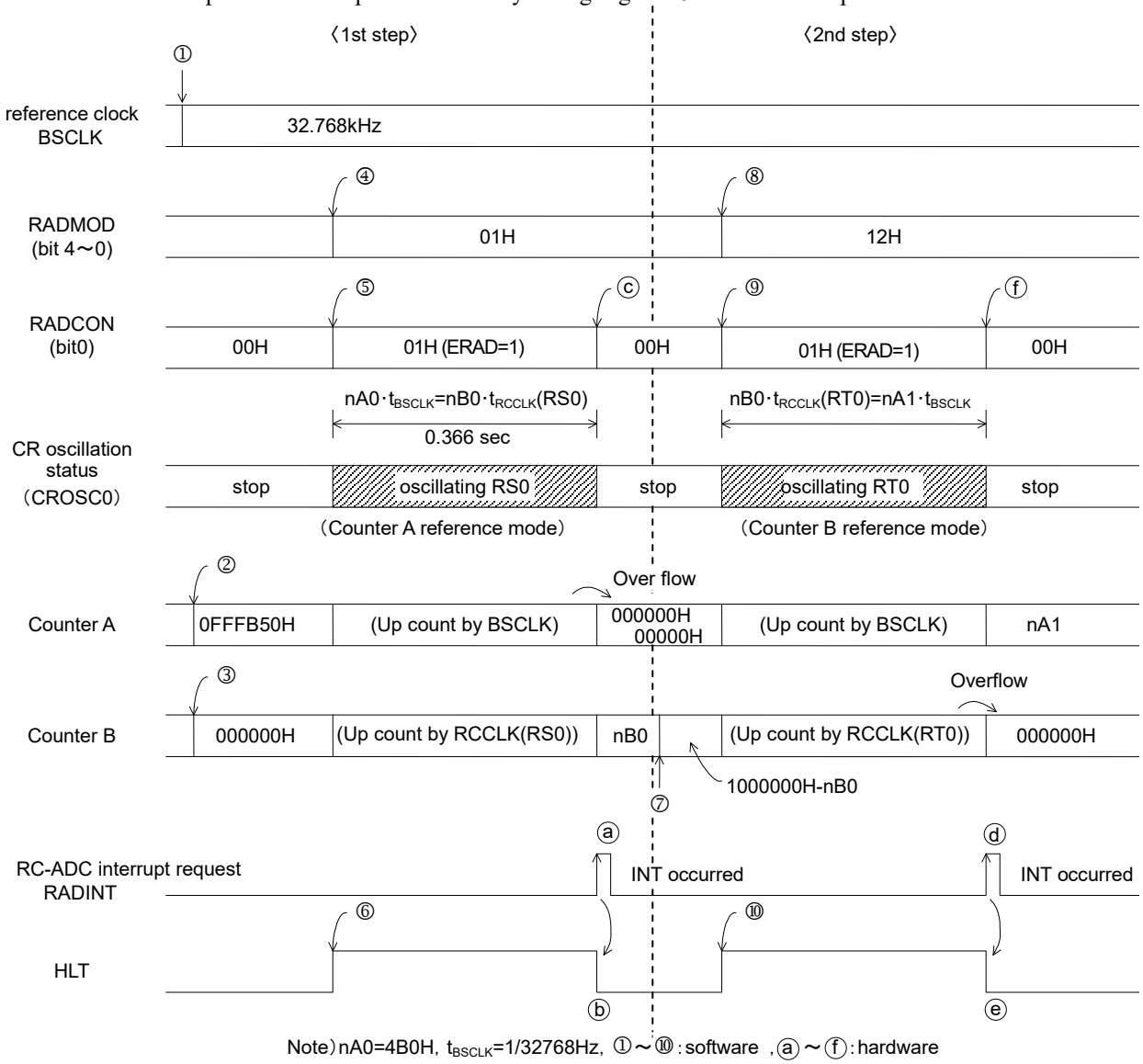
Basically, one A/D conversion cycle must consist of two steps, as shown in Figure 25-14. The reason for requiring two steps is that the reference resistor and the thermistor must first be oscillated separately and then the ratio between the oscillation frequencies of them is used, as described above.
In the example below, operation for these two steps is performed using the following combination:

- First step = RC oscillation with RS0 in Counter A reference mode
- Second step = RC oscillation with RT0 in Counter B reference mode

Besides this, there would be several possible A/D conversion methods.
In the above method, the operation time (gate time) for the second step fluctuates depending on the value of thermistor RT0. To avoid the fluctuation of the operation time, using a method that uses the following combination is recommended:

- First step = RC oscillation with RS0 in Counter B reference mode
- Second step = RC oscillation with RT0 in Counter A reference mode

A/D conversion procedure is explained below by taking Figure 25-14 as an example.



Note）nA0=4B0H, t_{BSCLK}=1/32768Hz, ①～⑩：software ,ⓐ～ⓕ：hardware

Figure 25-14 Timing Diagram for 1 Cycle of A/D Conversion (Example)

<First step>

①Set the base clock to LSCLK (32.768kHz).

②Preset “1000000H – nA0” in Counter A.
③Preset “000000H” in Counter B.
④Write “01H” in RADMOD to select Counter A reference mode and the oscillation mode that uses reference resistance RS0.
⑤Write “01H” in RADCONL to start A/D conversion operation.
⑥ (6) Write "1" in the HLT bit of SBYCON to set the device to HALT mode using the WFI/WFE command.

[Note]
In this example, nA0 is set to 4B0H because the gate time “nA0 x tBSCLK” in oscillation mode with reference resistor RS0 is set to 0.366 second. The value of nA0 is related to how much the margin of the quantization error of the A/D conversion is: the greater the nA0 value is, the smaller the margin of error becomes.
To reduce noise contamination to the RC oscillator circuit caused by CPU operation, it is recommended to constantly put the device into HALT/HALT-H mode during operation of RC oscillation.

From this point of time, the RC oscillator circuit (RCOSC0) continues oscillation for about 0.366 second with the reference resistance RS0. Then, when Counter A overflows, the RADINT signal is set to “1” and an RC-ADC interrupt request is generated. (Section a). Also, the generation of interrupt request releases HALT mode (section b) and at the same time, A/D conversion operation stops. (Section c, RARUN bit = "0"). At this time, Counter A is set to “000000H”.
The content of Counter B at this time is expressed by the following expression:

$$nB0 = nA0 \bullet \frac{t_{BSCLK}}{t_{RCCLK}\ (RS0)} \quad \text{... Expression B}$$

That completes the operations in First Step.

<Second step>

⑦Calculate “1000000H – nB0” from the content of Counter B “nB0” and set the obtained value in Counter B.
At this point, Counter A needs to be cleared; however, no processing is required since the counter is already set to “000000H”.
⑧Write “12H” in RADMOD to select Counter B reference mode and the oscillation mode that uses thermistor RT0.
⑨Write “01H” in RADCONL to start A/D conversion operation.
⑩Write "1" in the HLT bit of SBYCON to set the device to HALT mode using the WFI/WFE command.

The RC oscillator circuit (RCOSC0) oscillates with thermistor RT0 from this point until Counter B overflows. This period is equal to the product of “nB0” obtained in the First Step and the oscillation period t_{RCCLK} (RT0) using RT0.
When Counter B overflows, the RADINT signal is set to “1” and an RC-ADC interrupt request is generated. (Section d). Also, the generation of interrupt request releases HALT mode (section e) and at the same time, A/D conversion operation stops. (Section f, RARUN bit = "0").
This completes the operations in Second Step.

The content of Counter A at this time becomes the A/D conversion value nA1, which is expressed by the following expression:

$$nA1 = nB0 \bullet \frac{t_{RCCLK}(RT0)}{t_{BSCLK}} \quad \text{... Expression C}$$

From expressions B and C, nA1 is expressed by the following expression:

$$nA1 = nA0 \bullet \frac{t_{RCCLK}(RT0)}{t_{RCCLK}(RS0)} \quad \text{... Expression D}$$

The t_{RCCLK} (RS0) is the oscillator clock period by reference resistor RS0 and t_{RCCLK} (RT0) the oscillator clock period by thermistor RT0.
Since the oscillation period is expressed by "$t_{RCCLK} = k_{RCCLK}$ x R x C", t_{RCCLK} (RS0) and t_{RCCLK} (RT0) are expressed by the following expressions:

$$t_{RCCLK}(RS0) = k_{RCCLK} \bullet (CS0+CVR) \bullet RS0$$

$$t_{RCCLK}(RT0) = k_{RCCLK} \bullet (CS0+CVR) \bullet RT0 \quad \text{... Expression E}$$

When expression E is substituted for expression D, nA1 will be:

$$nA1 = nA0 \bullet \frac{RT0}{RS0}$$

Since “nA0” (“4B0H” in this example) and RS0 are constants whose values are fixed, “nA1” is a digital value proportional to RT0. This very “nA1” corresponds to “nT0” in expression A.

That concludes the description of the A/D conversion method using a thermistor. “nA1” that has been obtained must further be converted to a value such as a temperature indication value for thermometer by program according to the temperature-to-resistance characteristics of the thermistor.

25.3.4. Monitoring RC Oscillation

The RC oscillator clock (RCCLK) can be output using the secondary function of the P05. See Chapter 22, “Port” for the details of the secondary function of P05.
Monitoring RC oscillation is useful for checking the characteristics of the RC oscillator circuit. That is, the relationship between a sensor, such as a thermistor, and the oscillation frequency can be measured. For instance, the coefficient for conversion from the above-described nA1 value to a temperature indication value can be obtained by checking the relationship between the ambient temperature of a thermistor-incorporated RC oscillator circuit, the oscillation frequency with thermistor RT0, and the oscillation frequency with reference resistor RS0.

[Note]
P05 (RCM) is a monitor pin for oscillation clock. The Channel 0 and Channel 1 share the monitor pin.
Use P05 (RCM) pin for the evaluation purpose and disable the output while operating in an actual application to minimize the noise.

Chapter 26

Successive Approximation Type A/D Converter (SA-ADC)

26. Successive Approximation Type A/D Converter (SA-ADC)

26.1. General Description

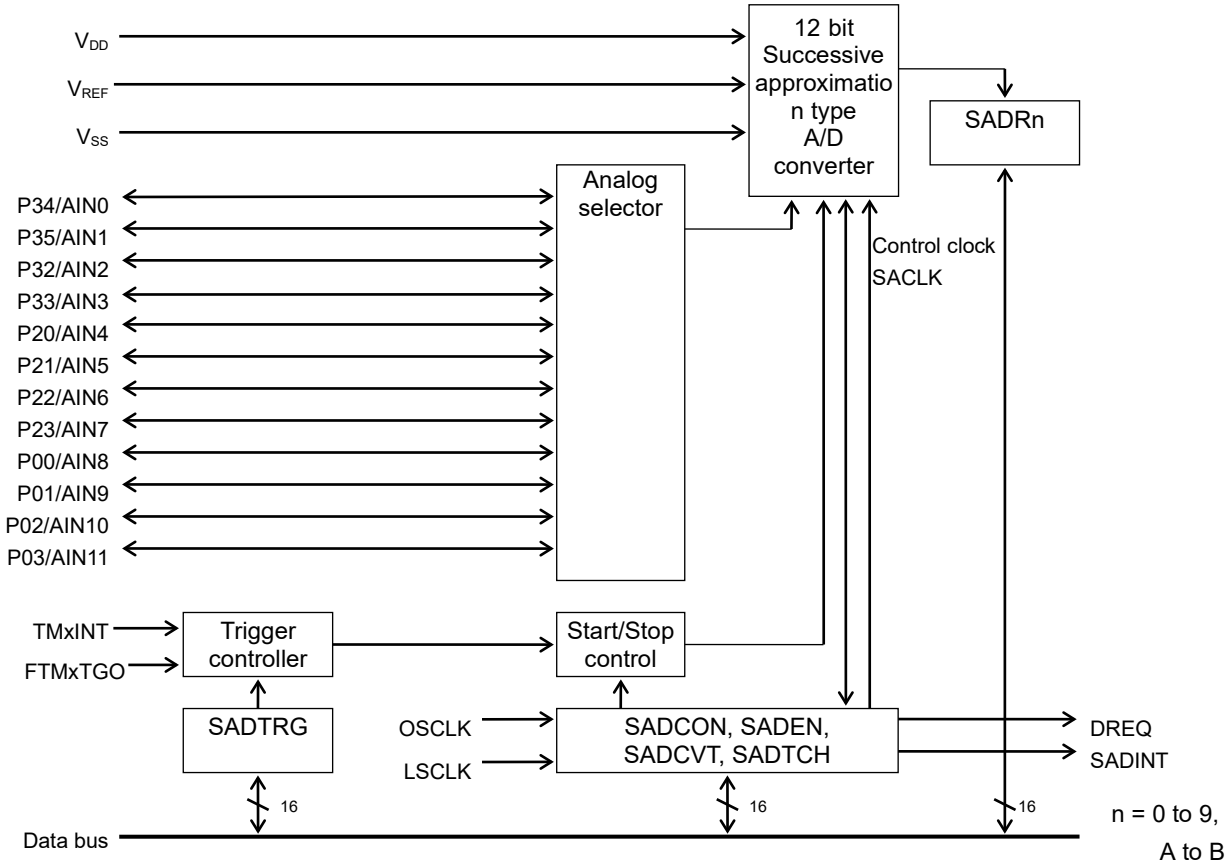
The successive approximation type A-D converter (SA-ADC) has 12 channels with a built-in function supporting an electrostatic capacity type switch (touch sensor supported) in addition to the normal A/D conversion.

26.1.1. Features

- Built-in sample/hold 12 bit successive approximation type A-D converter, which enables channel selection from multiple channels.
- Supports to start the A/D conversion using the timer.(trigger mode)
- Touch sensor supported.

26.1.2. Configuration

Figure 26-1 shows the configuration of SA-ADC.



SADRn : SA-ADC result register n
SADCON0/1: SA-ADC control register 0/1
SADEN : SA-ADC enable register
SADCVT : SA-ADC accuracy control register
SADTRG : SA-ADC trigger register
SADTCH : SA-ADC touch sensor register

Figure 26-1 Configuration of SA-ADC

26.1.3. List of Pins

Pin name	I/O	Function
P34/AIN0	I	Successive approximation type A/D converter input pin 0 Use as P34 pin primary function
P35/AIN1	I	Successive approximation type A/D converter input pin 1 Use as P35 pin primary function
P32/AIN2	I	Successive approximation type A/D converter input pin 2 Use as P32 pin primary function
P33/AIN3	I	Successive approximation type A/D converter input pin 3 Use as P33 pin primary function
P20/AIN4	I	Successive approximation type A/D converter input pin 4 Use as P20 pin primary function
P21/AIN5	I	Successive approximation type A/D converter input pin 5 Use as P21 pin primary function
P22/AIN6	I	Successive approximation type A/D converter input pin 6 Use as P22 pin primary function
P23/AIN7	I	Successive approximation type A/D converter input pin 7 Use as P23 pin primary function
P00/AIN8	I	Successive approximation type A/D converter input pin 8 Use as P00 pin primary function
P01/AIN9	I	Successive approximation type A/D converter input pin 9 Use as P01 pin primary function
P02/AIN10	I	Successive approximation type A/D converter input pin 10 Use as P02 pin primary function
P03/AIN11	I	Successive approximation type A/D converter input pin 11 Use as P03 pin primary function
V_{REF}	I	Reference voltage input pin for the successive approximation type A/D converter

26.2. Description of Registers

26.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4200_1000	SA-ADC result register 0	SADR0	R	32	0x0000_0000
0x4200_1004	SA-ADC result register 1	SADR1	R	32	0x0000_0000
0x4200_1008	SA-ADC result register 2	SADR2	R	32	0x0000_0000
0x4200_100C	SA-ADC result register 3	SADR3	R	32	0x0000_0000
0x4200_1010	SA-ADC result register 4	SADR4	R	32	0x0000_0000
0x4200_1014	SA-ADC result register 5	SADR5	R	32	0x0000_0000
0x4200_1018	SA-ADC result register 6	SADR6	R	32	0x0000_0000
0x4200_101C	SA-ADC result register 7	SADR7	R	32	0x0000_0000
0x4200_1020	SA-ADC result register 8	SADR8	R	32	0x0000_0000
0x4200_1024	SA-ADC result register 9	SADR9	R	32	0x0000_0000
0x4200_1028	SA-ADC result register A	SADRA	R	32	0x0000_0000
0x4200_102C	SA-ADC result register B	SADRB	R	32	0x0000_0000
0x4200_1040	SA-ADC control register 0	SADCON0	R/W	32	0x0000_0002
0x4200_1044	SA-ADC control register 1	SADCON1	R/W	32	0x0000_0000
0x4200_1048	SA-ADC enable register	SADEN	R/W	32	0x0000_0000
0x4200_104C	SA-ADC touch sensor register	SADTCH	R/W	32	0x0000_0000
0x4200_1050	SA-ADC trigger register	SADTRG	R/W	32	0x0000_0000
0x4200_1054	SA-ADC accuracy control register	SADCVT	R/W	32	0x0000_FFFF
0x4200_1060	SA-ADC result register	SADR	R	32	0x000F_0000

26.2.2. SA-ADC Result Register n (SADRn) n=0 to 9, A, B

Address: 0x4200_1000 (SADR0), 0x4200_1004 (SADR1), 0x4200_1008 (SADR2), 0x4200_100C (SADR3), 0x4200_1010 (SADR4), 0x4200_1014 (SADR5), 0x4200_1018 (SADR6), 0x4200_101C (SADR7), 0x4200_1020 (SADR8), 0x4200_1024 (SADR9), 0x4200_1028 (SADRA), 0x4200_102C (SADRB)
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	SARn[11:0]											
Access	–	–	–	–	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADRn is a special function register (SFR) used to store SA-ADC conversion results on channel n.
SADRn is updated after A/D conversion.

[Description of Bits]

- **SARn[11:0]** (bit 11 to 0)
  Stores the A/D conversion result (12 bit) of the channel n.

[Note]
It is prohibited that this resister is read by the DMAC. When the result is read by the DMAC, the result is read from SA-ADC Result Register (SADR)

26.2.3. SA-ADC Control Register 0(SADCON0)

Address: 0x4200_1040
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	SATCM	SACK	SALP
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SALP** (bit 0)
  This bit is used to select whether A/D conversion is performed once only for each channel or consecutively. When this bit is set to "0", A/D conversion is performed once only for each channel. And when it is set to "1", A/D conversion is performed consecutively according to the settings of the SA-ADC enable register (SADEN).
  Consecutive A/D conversion cannot be used in the trigger mode (SAST0 bit of SADTRG register is "1"). Therefore, set SALP to "0".

SALP	Description
0	Single A/D conversion only (initial value)
1	Consecutive A/D conversion

- **SACK** (bit 1)
  This bit is used to set the clock used for the A/D conversion.
  When SACK is set to "0", A/D conversion is preceded by using LSCLK. When SACK is set to "1", A/D conversion is performed by using OSCLK. If OSCLK is selected, the input clock of SA-ADC is 4MHz.
  If selecting the touch sensor conversion, set SACK to "1".

SACK	Description
0	LSCLK
1	OSCLK (initial value)

- **SATCM** (bit 2)
  This bit is used to select the touch sensor supported A/D conversion.
  By setting SATCM to "1", the channel, which was selected by SADTCH, is A/D converted by the touch sensor support.

SATCM	Description
0	Touch sensor unsupported A/D conversion (initial value)
1	Touch sensor supported A/D conversion

26.2.4. SA-ADC Control Register1 (SADCON1)

Address: 0x4200_1044
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	SARUN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADCON is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

- **SARUN** (bit 0)
  This bit is used to start or stop the SA-ADC conversion. Set this bit to "1" to start the A/D conversion, and "0" to stop it.
  When SALP is “0” and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to “0”. In the case of a trigger mode, the control by the software isn’t possible. This bit is set to “1” when the A/D conversion starts by the trigger event, and when conversion is finished, it becomes “0”.
  In addition, don’t start A/D conversion in a state with all bit of SA-ADC enable register (SADEN) as “0”. If the A/D conversion is started in this state, the A/D conversion circuit does not work.

SARUN	Description
0	Stops conversion (initial value)
1	Starts conversion

26.2.5. SA-ADC Enable Register (SADEN)

Address: 0x4200_1048
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	SACH[11:0]											
Access	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADEN is a special function register (SFR) used to choose A/D conversion channel(s).

[Description of Bits]

- **SACH[11:0]** (bit 11 to 0)
  The SACH[11:0] bits are used to select channel(s) on which A/D conversion is performed.
  If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.
  Do not start the A/D conversion with all SACH[11:0] set to "0". If the A/D conversion is started in this state, the A/D conversion circuit does not work.

SACH[n]	Description
0	Stops conversion on channel n (initial value)
1	Performs conversion on channel n

n = 0 to 11

Channel	Setting bit
0	SACH[0]
1	SACH[1]
2	SACH[2]
3	SACH[3]
4	SACH[4]
5	SACH[5]
6	SACH[6]
7	SACH[7]
8	SACH[8]
9	SACH[9
A(10)	SACH[10]
B(11)	SACH[11]

26.2.6. SA-ADC Touch Sensor Register (SADTCH)

Address: 0x4200_104C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	SATCH[11:0]											
Access	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADTCH is a special function register (SFR) used to select channels to be operated in the touch sensor supported mode.

[Description of Bits]

- **SATCH[11:0]** (bit 11 to 0)
  The SATCH[11:0] bits are used to select channel(s) on which A/D conversion is performed.

SATCH[n]	Description
0	Touch sensor mode disable (initial value)
1	Touch sensor mode enable

n = 0 to 11

[Note]
•Even if SATCH[n] is set to "1" for a bit which is not set to "1" by SADEN, the A/D conversion is not performed.

Channel	Setting bit
0	SATCH[0]
1	SATCH[1]
2	SATCH[2]
3	SATCH[3]
4	SATCH[4]
5	SATCH[5]
6	SATCH[6]
7	SATCH[7]
8	SATCH[8]
9	SATCH[9
A(10)	SATCH[10]
B(11)	SATCH[11]

26.2.7. SA-ADC Trigger Register (SADTRG)

Address: 0x4200_1050
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	SASTS [4:0]					–*	–*	–*	–*	–*	–*	–*	SAST0
Access	–	–	–	R/W	R/W	R/W	R/W	R/W	–	–	–	–	–	–	–	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADTRG is a special function register (SFR) used to select the external trigger for the A/D conversion.

[Description of Bits]

- **SAST0** (bit 0)
  Selects the A/D conversion start mode.

SAST0	Description
0	Normal mode (initial value) Start A/D conversion by setting SARUN of SADCON registers “1” from software.
1	Trigger mode : SARUN is set to “1” by the trigger event selected by SASTS, and then A/D conversion is started. Even if a trigger event occurs during A/D conversion (when SARUN is set to “1”), it is ignored and the A/D conversion in process is continued. In addition, In addition, SARUN cannot be controlled by consecutive A/D conversion nor software.

- **SASTS[4:0]** (bits 12 to 8)
  This bit is used to select a trigger event for the A/D conversion.

SASTS4	SASTS3	SASTS2	SASTS1	SASTS0	Description
0	0	0	0	0	TM0INT
0	0	0	0	1	TM1INT
0	0	0	1	0	TM2INT
0	0	0	1	1	TM3INT
0	0	1	0	0	TM4INT
0	0	1	0	1	TM5INT
0	0	1	1	0	TM6INT
0	0	1	1	1	TM7INT
0	1	*	*	*	Setting prohibited
1	0	0	0	0	FTM0TGO
1	0	0	0	1	FTM1TGO
1	0	0	1	0	FTM2TGO
1	0	0	1	1	FTM3TGO
1	0	1	*	*	Setting prohibited
1	1	*	*	*	Setting prohibited

[Note]
•The timer interrupt request (TM0-7INT) is an interrupt request signal independent of the interrupt enabled/disabled setting of the interrupt enable register. The multifunction timer trigger output(FTM0-3TGO) is a signal for event trigger.
•If a prohibited setting is specified, the A/D conversion is not started by any trigger event.

26.2.8. SA-ADC Accuracy Control Register (SADCVT)

Address: 0x4200_1054
Access: R/W
Access size: 32 bit
Initial value: 0x0000_FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	SAPCT [4:0]					SACPT[2:0]			SADCT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADCVT is a special function register (SFR) used to select the conversion time of the A/D conversion.

SADCVT releate to SACK of SADCON0 and SATCM. Set SADCVT according to the following table.

SACK	SATCM	SAPCT[4:0]	SACPT[2:0]	SADCT[7:0]
0	0	00H	00H	01H
0	1	Setting prohibited	Setting prohibited	Setting prohibited
1	0	00H	03H	78H
1	1	15H	03H	78H

26.2.9. SA-ADC Result Register (SADR)

Address: 0x4200_1060
Access: R
Access size: 32 bit
Initial value: 0x000F_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	RNUM[3:0]			
Access	–	–	–	–	–	–	–	–	–	–	–	–	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	SAR [11:0]											
Access	–	–	–	–	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
SADC is a special function register used to store SA-ADC conversion results on channel n.
The result of the valid channels is read from the smallest channel.

[Description of Bits]

- **SAR[11:0]** (bit 11 to 0)
  SAR[11:0] is stored SA-ADC conversion results on channel which is indicated by RNUM[3:0].

- **RNUM[3:0]** (bit 19 to 16)
  RNUM is indicated the channel number which is SA-ADC conversion results.

26.3. Description of Operation

26.3.1. Setting of A/D Conversion Channels

According to the Table 26-2, set a bit corresponding to each channel on which the A/D conversion is performed.

Table 26-2, Setting channel

SADCON0 SATCM bit	SADEN SACH[n] bit	SADTCH SATCH[n] bit	SA-ADC operation
0	0	X	No operation
0	1	0	Non-touch sensor mode
0	1	1	No operation
1	0	X	No operation
1	1	0	No operation
1	1	1	Touch sensor mode

X:Don't Care

Do not start the A/D conversion with all SACH[11:0] bits set to "0" in the SA-ADC enable register (SADEN). If the A/D conversion is started in this state, an interrupt is not output and the SARUN bit remains as "1".

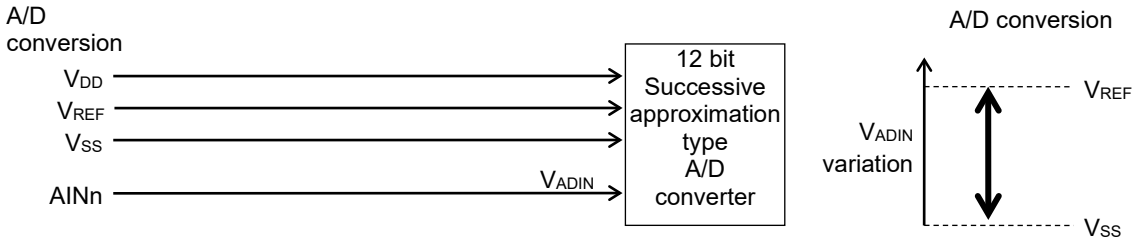


Figure 26-2 A/D Conversion Pins and Conversion Range

26.3.2. Operation of the Successive Approximation Type A/D Converter

For direct input, operate SA-ADC in the following procedure.

(1) Normal mode
1. Wait until the oscillation of the clock used for the A/D conversion is started and stabilized.
2. Set the SA-ADC control register 0 (SADCON0), SA-ADC enable register (SADEN), and SA-ADC accuracy control register (SADCVT).
3. When the bit 2 (SATCM) of the SA-ADC control register 0 (SADCON0) is set to "0" then the bit 0 (SARUN) of the SA-ADC control register 1 (SADCON1) to "1", the SA-ADC circuit starts operating to perform A/D conversion on the channels selected in the SA-ADC enable register (SADEN) from a lower channel number.
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRn), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.

(2) Trigger mode
1. Wait until the oscillation of the clock used for the A/D conversion is started and stabilized.
2. Set the SA-ADC control register 0 (SADCON0), SA-ADC enable register (SADEN), and SA-ADC accuracy control register (SADCVT), where set SALP bit of SADCON0 register.
3 After trigger event source is selected by SA-ADC trigger register (SADTRG), and SAST0 bit is set to "1", the trigger mode is begun.
4. If occur trigger event , the bit 0 (SARUN) of the SA-ADC control register 1 (SADCON1) to "1", the SA-ADC circuit starts operating to perform A/D conversion on the channels selected in the SA-ADC enable register (SADEN) from a lower channel number.
5. A/D conversion results are stored in the applicable SA-ADC result registers (SADRn), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.

Even if the channel is switched during A/D conversion, it is held as selected at the start of A/D conversion until an A/D conversion termination interrupt occurs.
Figure 26-3 shows the operation when channels 0 and 1 are selected.

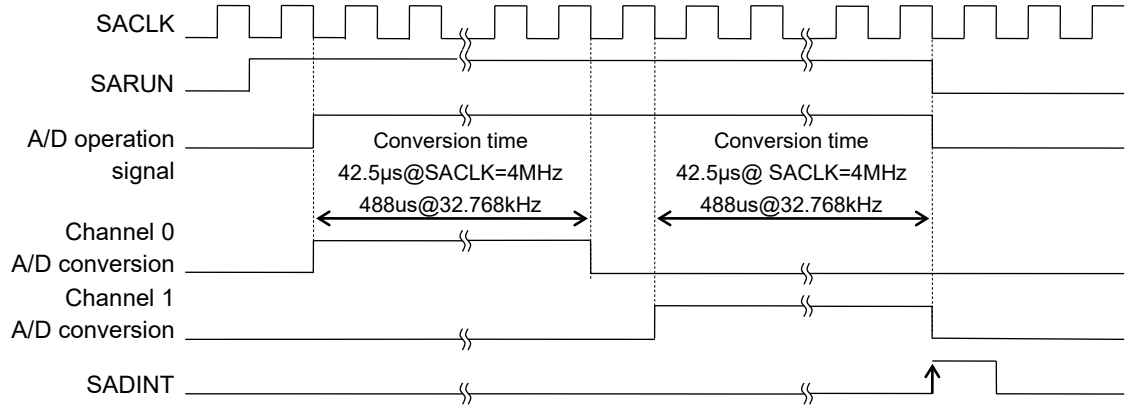


Figure 26-3 Operation Timing Diagram of SA-ADC

26.3.3. Capacitive Touch sensor mode operation

To operate SA-ADC, complete the following procedure.

1. Wait until the oscillation of the clock used for the A/D conversion is started and stabilized.
2. Set the SA-ADC control register 0 (SADCON0), SA-ADC enable register (SADEN), SA-ADC accuracy control register (SADCVT), and SA-ADC touch sensor register (SADTCH).
3. When the bit 2 (SATCH) of the SA-ADC control register 0 (SADCON0) is set to "1" then the bit 0 (SARUN) of the SA-ADC control register 1 (SADCON1) to "1", the SA-ADC circuit starts operating. The touch sensor supported A/D conversion is performed on the channels selected in the SA-ADC enable register (SADEN) from a lower channel number.
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRn), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.

Figure 26-4 shows the operation when channels 0 and 1 are selected.

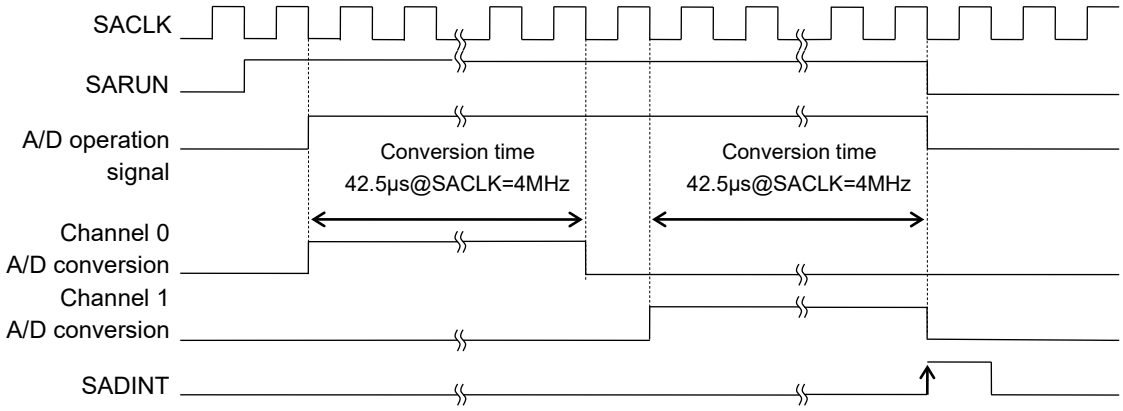


Figure 26-4 Operation Timing Diagram of SA-ADC

26.3.4. Notes on Use of SA-ADC

SA-ADC has an internal capacitor of 51.2pF(Typ), which is charged by the voltage input from AINn (n=0 to 11).
It is possible to charge it by connecting an external capacitor of 0.47uF or more regardless of the input impedance.
Figure 26-5 shows the connection of SA-ADC.
If an external capacitor of less than 0.47uF is used, the measurement accuracy decreases.

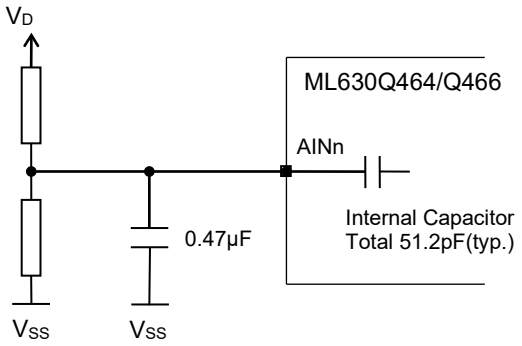


Figure 26-5 Connection of SA-ADC

Chapter 27

LCD Driver

27. LCD Driver

27.1. Overview

This LSI includes LCD drivers that display the contents that are set in the display register.
The LCD drivers handle the LCD display functions with four blocks.

1. Display registers
2. Display allocation
3. Display control
4. Drivers

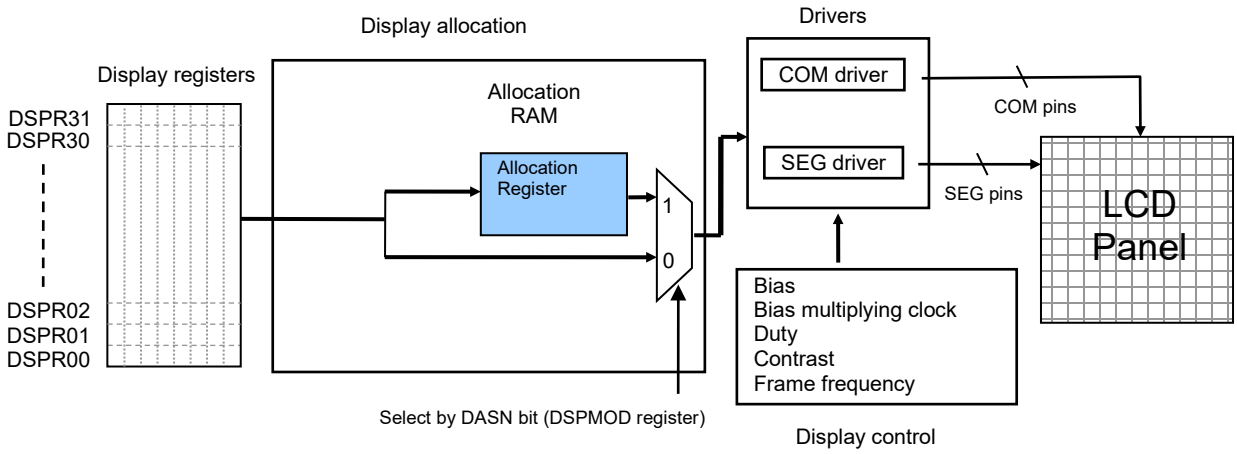


Figure 27-1 Configuration of LCD Display Function

The display registers are used to store the contents to be displayed as bit patterns.
The bit pattern storage method depends on the specification of the LCD panel to be used (display pattern and assignment of the COM pin and SEG pin) and the setting of the display allocation circuit.

The display allocation block controls mapping of the display register for the LCD common/segment.
Using the display allocation register or not using them is selectable. When using them (Set DASN bit of DSPMOD register to "1"), the segment mapping of the display register can be specified in bit units by programming according to the contents of display allocation register. Therefore, the display register array can be changed in flexible and simplify the software process for display (This function is defined as the programmable display allocation function in the user's manual).
When not using the display allocation register (Set DASN bit of DSPMOD register to "0"), control the display with the display register only.

The display control circuit generates LCD drive waveforms according to the characteristics of the LCD.
A bias, a bias voltage multiplying clock, a duty, a frame frequency, and a contrast suitable for the LCD panel can be selected.

A) When not using Programmable display allocation function (DASN bit of DSPMOD register is "0")
Suitable for the dot matrix type LCD panel whose common/segment array is approximated to the bit array of the display register..

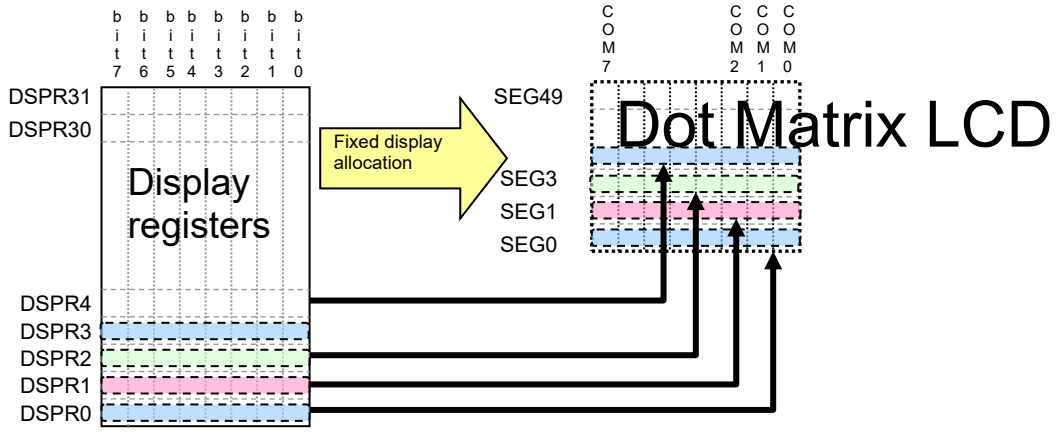
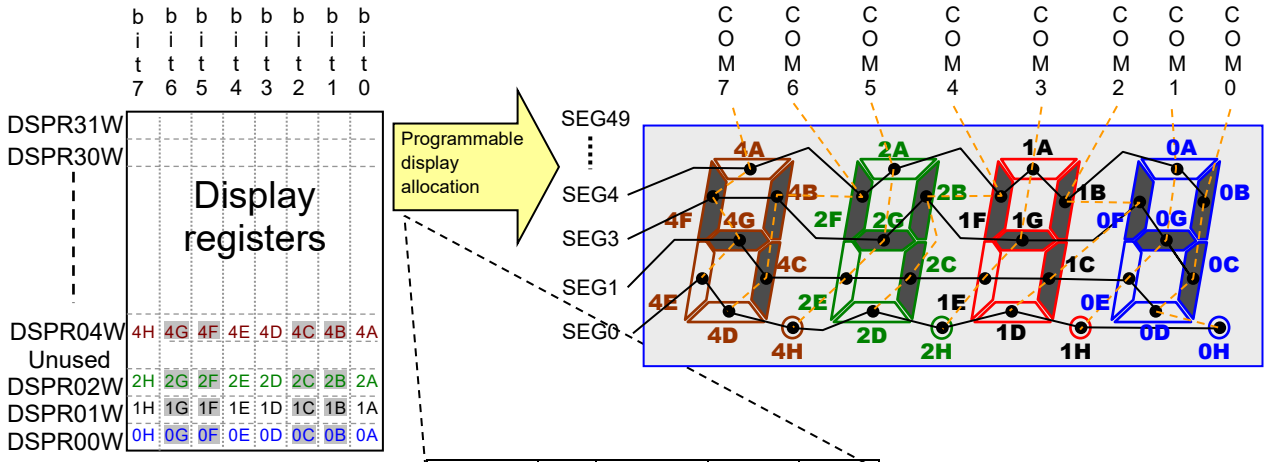


Figure 27-2 An example of correlation between display register and dot matrix type LCD

B) When using Programmable display allocation function (DASN bit of DSPMOD register is "1")
The programmable display allocation function is suitable for the LCD panel of segment type or character type whose common/segment array is restricted by the design or wiring. Segment mapping of the display register can be assigned in bit units by programming according to the contents of display allocation register. Therefore, the display register array can be changed in flexible and simplify the software process for display. Contents of the register (DSmCn) specify addresses and bits of the display registers (DSPR00W to DSPR31W), that are output to common "n" of segment "m".



DSPR	bit	Symbol	COM	SEG
…	…	…	…	…
DSPR4	6	4G	7	1
…	…	…	…	..
DSPR0	2	0C	0	3
DSPR0	1	0B	0	4
DSPR0	0	0A	1	4

Figure 27-3 An example of correlation between display registers and segment type LCD

27.1.1. Features

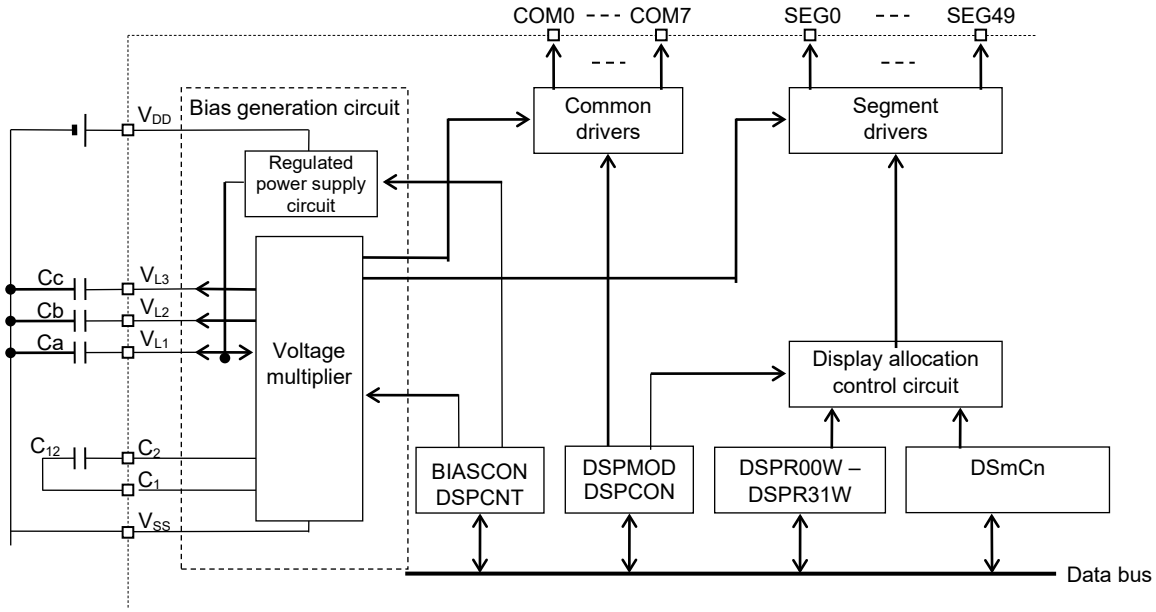
The LCD drivers are applicable to various types of LCD panels.

- Maximum 400-dot matrix (50 segment x 8 common)
- 1/1 to 1/8 duty
- 1/2, 1/3 bias (built-in bias generation circuit)
- Frame frequency selectable (4types)
- Bias voltage multiplying clock selectable (8types)
- Contrast adjustment(32steps)
- Programmable display allocation function

The programmable display allocation function facilitates software display processing.
By using "ALL LCDs on mode" and "ALL LCDs off mode", LCD panel inspection processing software can be easily created.

27.1.2. Configuration of the LCD Drivers

Figure 27-1 shows the configuration of the LCD drivers and the bias generation circuit.



BIASCON : Bias circuit control register
DSPCNT : Display contrast register
DSPMOD : Display mode register
DSPCON : Display control register
DSmCn : Allocation register (m = 0 to 49, n = 0 to 7)
DSPR00W to DSPR31W : Display registers

Figure 27-4 Configuration of LCD controller

27.1.3. Configuration of the Bias Generation Circuit

The bias generation circuit generates LCD drive voltages (V_{L1} to V_{L3}) by multiplying the voltage (V_{L1}) generated by the voltage regulator with the capacitors (C_{12}).
When the BSON bit of the bias circuit control register (BIASCON) is set to "1", the bias generation circuit starts operation.
Display contrast adjustment is possible in 32 steps by using the display contrast register (DSPCNT).
Figure 27-5 shows the configurations of the bias generation circuit with 1/2 bias and with 1/3 bias.

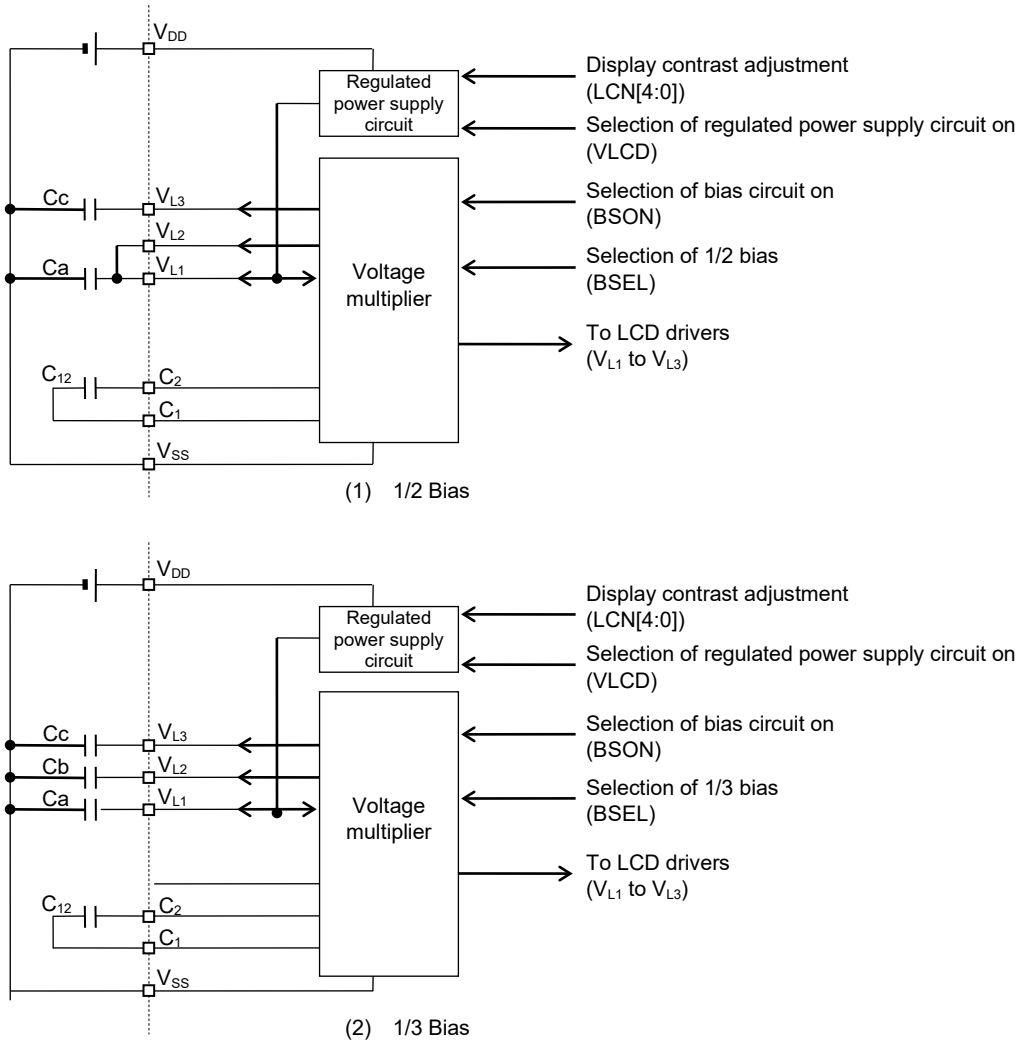


Figure 27-5 Configuration of Bias Generation Circuit

Note:
When using 1/2 bias, connect the V_{L1} pin and the V_{L2} pin externally.

27.1.4. List of Pins

Pin name	I/O	Function
V_{L1} to V_{L3}	-	Power supply pin for LCD bias (internally generated)
C_1 to C_2	-	Capacitor connection pin for LCD bias generation
COM0 to 7	O	LCD common pin
SEG0 to 49	O	LCD segment pin

27.2. Description of Registers

27.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4300_0000	Bias circuit control register	BIASCON	R/W	32	0x0000_0008
0x4300_0004	Display contrast register	DSPCNT	R/W	32	0x0000_0000
0x4300_0008	Display mode register	DSPMOD	R/W	32	0x0000_0000
0x4300_000C	Display control register	DSPCON	R/W	32	0x0000_0000
0x4300_0100 to 0x4300_0131	Display register 00 to Display register 31	DSPR00W to DSPR31W	R/W	8/16/32	Undefined
0x4300_0800 to 0x4300_0FFC	Display register 000 to Display register	DS0C0 to DS49C7	R/W	32	Undefined

27.2.2. Bias Circuit Control Register (BIASCON)

Address: 0x4300_0000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	LOAD
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	VLCD	–*	–*	–*	BSEL	BSN[2:0]			BSON
Access	–	–	–	–	–	–	–	R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
BIASCON is a special function register (SFR) to control the bias generation circuit.

[Description of Bits]

- **BSON** (bit 0)
  The BSON bit is used to control the operation of the bias generation circuit.
  When BSON is set to "1", the bias generation circuit generates the LCD drive voltages. (V_{L1} to V_{L3}).

BSON	Description
0	Bias circuit Off (initial value)
1	Bias circuit On

- **BSN[2:0]** (bit 3 to 1)
  The BSN[2:0] bits are used to select a clock for multiplying the bias voltage in the bias generation circuit.
  1/8 LSCLK to 1/128LSCLK can be selected.

BSN[2]	BSN[1]	BSN[0]	Description
0	0	0	Prohibited
0	0	1	Prohibited
0	1	0	Prohibited
0	1	1	1/8 LSCLK (4 kHz)
1	0	0	1/16 LSCLK (2 kHz) (initial value)
1	0	1	1/32 LSCLK (1 kHz)
1	1	0	1/64 LSCLK (512 Hz)
1	1	1	1/128 LSCLK (256 Hz)

- **BSEL** (bit 4)
  The BSEL bit is used to set the bias in the bias generation circuit.
  1/2 bias or 1/3 bias can be selected.

BSEL	Description
0	1/3 bias (initial value)
1	1/2 bias

- **VLCD** (bit 6)
  The VLCD bit is used to generate the reference voltage for the bias generation circuit.

VLCD	Description
0	Regulated power supply circuit is off (initial value)
1	Regulated power supply circuit is on

27.2.3. Display Contrast Register (DSPCNT)

Address: 0x4300_0004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	_*	LCN[4:0]				
Access	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
DSPCNT is a special function register (SFR) to adjust the contrast of display (32 steps).
For the setting value of DSPCNT and the LCD drive voltages (V_{L1}, V_{L2}, V_{L3}), see Appendix C, "Electrical Characteristics".

[Description of Bits]

- **LCN[4:0]** (bit 4 to 0)

The LCN[4:0] bits are used to adjust the contrast of display (32 steps)

LCN[4]	LCN[3]	LCN[2]	LCN[1]	LCN[0]	contrast	V_{L1} voltage(typ) V
0	0	0	0	0	Low	0.94(initial value)
0	0	0	0	1	↑	0.96
0	0	0	1	0		0.98
0	0	0	1	1		1.00
0	0	1	0	0		1.02
0	0	1	0	1		1.04
0	0	1	1	0		1.06
0	0	1	1	1		1.08
0	1	0	0	0		1.10
0	1	0	0	1		1.12
0	1	0	1	0		1.14
0	1	0	1	1		1.16
0	1	1	0	0		1.18
0	1	1	0	1		1.20
0	1	1	1	0		1.22
0	1	1	1	1		1.24
1	0	0	0	0		1.26
1	0	0	0	1		1.28
1	0	0	1	0		1.30
1	0	0	1	1		1.32
1	0	1	0	0		1.34
1	0	1	0	1		1.36
1	0	1	1	0		1.38
1	0	1	1	1		1.40

1	1	0	0	0			1.42
1	1	0	0	1			1.44
1	1	0	1	0			1.46
1	1	0	1	1			1.48
1	1	1	0	0			1.50
1	1	1	0	1			1.52
1	1	1	1	0		▼	1.54
1	1	1	1	1	High		1.56

[Note]
*: When using 1/2 bias, setting the LCN[4:0] between 0x10 and 0x1F. Setting the value of LCN[4:0] between 0x0 and 0x0F is prohibited.

27.2.4. Display Mode Register 0 (DSPMOD)

Address: 0x4300_0008
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	PLDN	–*	–*	–*	–*	–*	DASN	–*	–*
Access	–	–	–	–	–	–	–	R/W	–	–	–	–	–	R/W	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	FRM[1:0]		–*	–*	DUTY[2:0]		
Access	–	–	–	–	–	–	–	–	–	R/W	R/W	–	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
DSPMOD0 is a special function register (SFR) to control the display of the LCD drivers.

[Description of Bits]

- **DUTY[4:0]** (bit 4 to 0)
  The DUTY[4:0] bits are used to specify the duty in 8 steps (1/1 to 1/8).

DUTY[2	DUTY[1	DUTY[0]	Duty
0	0	0	1/1 duty (initial value)
0	0	1	1/2 duty
0	1	0	1/3 duty
0	1	1	1/4 duty
1	0	0	1/5 duty
1	0	1	1/6 duty
1	1	0	1/7 duty
1	1	1	1/8 duty

- **FRM[1:0]** (bit 6 to 5)
  The FRM[1:0] bits are used to select a frame frequency of the LCD drivers.
  The reference frequency of a frame frequency (LLSCLK = 32.768 kHz) is selectable from 64 Hz, 73 Hz, 85 Hz, or 102 Hz.

FRM[1]	FRM[0]	Description
0	0	Reference frequency: 64 Hz (initial value)
0	1	Reference frequency: 73 Hz
1	0	Reference frequency: 85 Hz
1	1	Reference frequency: 102 Hz

The frame frequency for each duty is listed in Table 27-1.

Table 27-1 Frame Frequency for Each Duty

Duty	Frame frequency [Hz]			
	Reference frequency 64Hz	Reference frequency 73Hz	Reference frequency 85Hz	Reference frequency 102Hz
1/1 duty	64.00	73.14	85.33	102.40
1/2 duty	64.00	73.14	85.33	102.40
1/3 duty	64.25	73.31	85.33	103.04
1/4 duty	64.00	73.14	85.33	102.40
1/5 duty	64.25	73.64	86.23	102.40
1/6 duty	64.25	73.80	85.33	103.04
1/7 duty	64.13	73.14	86.69	104.03
1/8 duty	64.00	73.14	85.33	102.40

- **DASN** (bit 18)
  The DASN bit is used to control the operation of the display allocation function.
  Setting the DASN bit to "1" enables the display allocation function.

DASN	Description
0	Not use Programmable display allocation (initial value)
1	Use Programmable display allocation

- **PLDN** (bit 24)
  The PLDN bit is setting to connect V_{L1}, V_{L2}, and V_{L3} to V_{SS} internally. This bit is used to make the pins of COM/SEG the V_{SS} level.

PLDN	Description
0	V_{L1} to V_{L3} are not connected to GND. (initial value)
1	V_{L1} to V_{L3} are connected to GND.

Note:
When LCD stop mode, Setting PLDN bit to "1", the pins of COM/SEG is the V_{SS} level soon. After LCD stop mode, the display does not go out soon, then setting PLDN bit to "1". It is prohibited that PLDN bit is set to "1" except LCD stop mode.

27.2.5. Display Control Register (DSPCON)

Address: 0x4300_000C
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	LMD[1:0]	
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
DSPCON is a special function register (SFR) to control the LCD drivers.

[Description of Bits]

- **LMD[1:0]** (bit 1, 0)
  The LMD[1:0] bits are used to select an LCD display mode.
  LCD stop mode, all LCDs off mode, LCD display mode, and all LCDs on mode can be selected.
  In LCD stop mode, V_{ss} level is output to all the common drivers and segment drivers. The charge and discharge current to and from the display panel can be stopped.
  In all LCDs off mode, off waveform is output to all the segment drivers irrespective of the contents of the display registers.
  In LCD display mode, the contents of the display registers are output to each segment driver.
  In all LCDs on mode, on waveform is output to all the segment drivers irrespective of the contents of the display registers.

LMD[1]	LMD[0]	Description
0	0	LCD stop mode (initial value)
0	1	All LCDs off mode
1	0	LCD display mode
1	1	All LCDs on mode

27.2.6. Display Registers 00 to 31 (DSPR00W to DSPR31W)

Address: 0x4300_0100 to 0x4300_0131
Access: R/W
Access size: 8/16/32 bit
Initial value: Undefined

(n=0 to 12)	7	6	5	4	3	2	1	0
DSPR4n+3W	c7	c6	c5	c4	c3	c2	c1	c0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

	7	6	5	4	3	2	1	0
DSPR4n+2W	c7	c6	c5	c4	c3	c2	c1	c0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

	7	6	5	4	3	2	1	0
DSPR4n+1W	c7	c6	c5	c4	c3	c2	c1	c0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

	7	6	5	4	3	2	1	0
DSPR4nW	c7	c6	c5	c4	c3	c2	c1	c0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
DSPRxxW (xx = 00 to 2C) are special function registers (SFRs) to store display data.
Each valid bit of DSPRxxW becomes undefined at system reset.
Set data in DSPRxxW before setting LCD display mode.
Tables 27-1lists display registers.

[Description of Bits]

- **c7 to c0** (bit 7 to 0)
  The c7 to c0 bit are used to set display data.

C7 to c0	Description
0	off waveform
1	on waveform

Table 27-1 Display Registers

Register name	Address	Corresponding segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR00W	0x4300_0100	SEG0	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR01W	0x4300_0101	SEG1	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR02W	0x4300_0102	SEG2	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR03W	0x4300_0103	SEG3	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR04W	0x4300_0104	SEG4	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR05W	0x4300_0105	SEG5	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR06W	0x4300_0106	SEG6	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR07W	0x4300_0107	SEG7	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR08W	0x4300_0108	SEG8	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR09W	0x4300_0109	SEG9	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0AW	0x4300_010A	SEG10	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0BW	0x4300_010B	SEG11	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0CW	0x4300_010C	SEG12	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0DW	0x4300_010D	SEG13	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0EW	0x4300_010E	SEG14	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0FW	0x4300_010F	SEG15	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR10W	0x4300_0110	SEG16	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR11W	0x4300_0111	SEG17	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR12W	0x4300_0112	SEG18	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR13W	0x4300_0113	SEG19	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR14W	0x4300_0114	SEG20	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR15W	0x4300_0115	SEG21	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR16W	0x4300_0116	SEG22	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR17W	0x4300_0117	SEG23	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR18W	0x4300_0118	SEG24	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR19W	0x4300_0119	SEG25	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1AW	0x4300_011A	SEG26	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1BW	0x4300_011B	SEG27	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1CW	0x4300_011C	SEG28	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1DW	0x4300_011D	SEG29	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1EW	0x4300_011E	SEG30	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR1FW	0x4300_011F	SEG31	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR20W	0x4300_0120	SEG32	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR21W	0x4300_0121	SEG33	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR22W	0x4300_0122	SEG34	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR23W	0x4300_0123	SEG35	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR24W	0x4300_0124	SEG36	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR25W	0x4300_0125	SEG37	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR26W	0x4300_0126	SEG38	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR27W	0x4300_0127	SEG39	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR28W	0x4300_0128	SEG40	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR29W	0x4300_0129	SEG41	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2AW	0x4300_012A	SEG42	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2BW	0x4300_012B	SEG43	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2CW	0x4300_012C	SEG44	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2DW	0x4300_012D	SEG45	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2EW	0x4300_012E	SEG46	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR2FW	0x4300_012F	SEG47	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR30W	0x4300_0130	SEG48	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR31W	0x4300_0131	SEG49	c7	c6	c5	c4	c3	c2	c1	c0	R/W

27.2.7. Display Allocation Register (DS0C0 to DS49C7)

Address: 0x4300_0800 to 0x4300_0FC4
Access: R/W
Access size: 32 bit
Initial value: Undefined

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	a5	a4	a3	a2	a1	a0	–*	b2	b1	b0
Access	–	–	–	–	–	–	R/W	R/W	R/W	R/W	R/W	R/W	–	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
DSmCn (m= 0 to 49, n = 0 to 7) are special function registers (SFRs) that are used for the programmable display allocation function.
Each valid bit of DSmCn becomes undefined at system reset.
Table 27-2 shows a list of the display allocation register.

[Description of Bits]

- **b2-b0** (bits 2 to 0)

The b2 to b0 bits of DSmCn (m= 0 to 49, n = 0 to 7) are used to select the bits of the display registers (DSPR00W to DSPR31W) that are output to common n of segment m.

b2	b1	b0	Description
0	0	0	Selects bit 0
0	0	1	Selects bit 1
0	1	0	Selects bit 2
0	1	1	Selects bit 3
1	0	0	Selects bit 4
1	0	1	Selects bit 5
1	1	0	Selects bit 6
1	1	1	Selects bit 7

- **a5-a0** (bits 9 to 4)

The a5 to a0 bits of DSmCn (m= 0 to 49, n = 0 to 7) are used to select the lower 8 bits of the addresses of the display registers (DSPR00W to DSPR31W) that are output to common n of segment m.

[Note]
Set DSmCn when the DASN bit of the display mode register (DSPMOD) is "0".
When the DASN bit is "1", access from the CPU is invalid.

Table 27-2 Display Allocation Register

Segment	Common	Register name	Address	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
SEG0	COM0	DS0C0	0x4300_0800	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
SEG1	COM0	DS1C0	0x4300_0804	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
SEG2	COM0	DS2C0	0x4300_0808	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
SEG3	COM0	DS3C0	0x4300_080C	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM0	DS49C0	0x4300_08C4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM1	DS0C1	0x4300_0900	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM1	DS49C1	0x4300_09C4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM2	DS0C2	0x4300_0A00	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
:	:	:	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM2	DS49C2	0x4300_0AC4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM3	DS0C3	0x4300_0B00	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM3	DS49C3	0x4300_0BC4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM4	DS0C4	0x4300_0C00	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM4	DS49C4	0x4300_0CC4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM5	DS0C5	0x4300_0D00	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM5	DS49C5	0x4300_0DC4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM6	DS0C6	0x4300_0E00	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM6	DS49C6	0x4300_0EC4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG0	COM7	DS0C7	0x4300_0F00	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W
-	-	-	:	-	-	-	-	-	-	-	-	-	-	-*
SEG49	COM7	DS49C7	0x4300_0FC4	a5	a4	a3	a2	a1	a0	-	b2	b1	b0	R/W

27.3. Description of Operation

27.3.1. Operation of LCD Drivers and Bias Generation Circuit

Figure 27-6 shows the operation of the LCD drivers and the bias generation circuit.

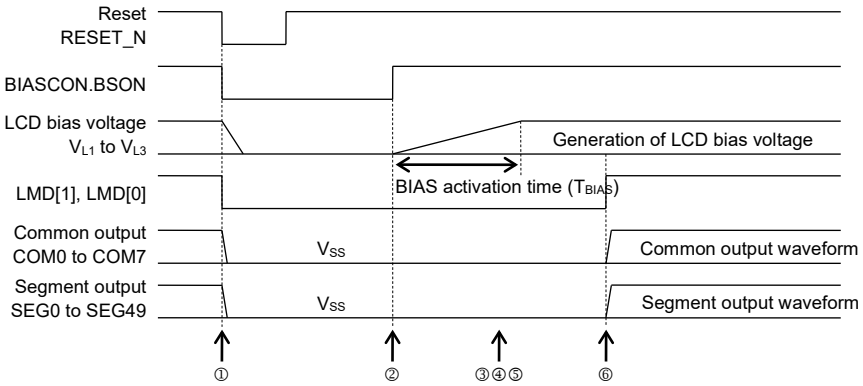


Figure 27-6 Operation of LCD Drivers and Bias Generation Circuit

① System reset causes the bias generation circuit and the LCD drivers to stop operation and Vss level to be output to each of the common and segment pins.
② By using the bias circuit control register (BIASCON), select 1/2 bias or 1/3 bias and lock of bias voltage multiplying, and set the bias generation circuit to on (BSON = "1").
③ When the programmable display allocation function is used, set LCD allocation data in the display allocation register (DS0C0 to DS49C7).
④ Set a frame frequency and a duty by using the display mode register (DSPMOD). When using the programmable display allocation function, set the DASN bit of DSPMOD register to "1".
⑤ Set display data in the display registers (DSPR00W to DSPR31W).
⑥ After elapse of the bias activation time (T_{BIAS}) or longer, set the mode to display mode by using the LMD[1:0] bits of the display control register (DSPCON). (Display waveform is output to each segment pin.)

For the bias activation time (T_{BIAS}), see the "Electrical Characteristics" Section in Appendix C.

27.3.2. Segment Mapping When the Programmable Display Allocation Function is Used

When the programmable display allocation function is used (DASN bit of DSPMOD register is "1"), display registers (DSPR00W to DSPR31W) segment mapping can be set in bit units according to the contents of display allocation register (DSmCn,: m = 0 to49, n = 0 to 7).
Table 27-3 shows the frame frequencies and the duty conditions that allow the use of the programmable allocation function.

Table 27-3 Conditions That Allow the Use of Programmable Allocation Function

Frame frequency	Duty that allows the use of duty
Approx. 64 Hz	1/1 to 1/8 Duty
Approx. 73 Hz	1/1 to 1/7 Duty
Approx. 85 Hz	1/1 to 1/6 Duty
Approx. 102 Hz	1/1 to 1/5 Duty

Note:
- When the duty is other than those indicated in Table 27-3, the programmable allocation function can not be used regardless of the content of the DASN bit of DSPMOD. T

Figure 27-7 shows the configuration when using the programmable display allocation function.

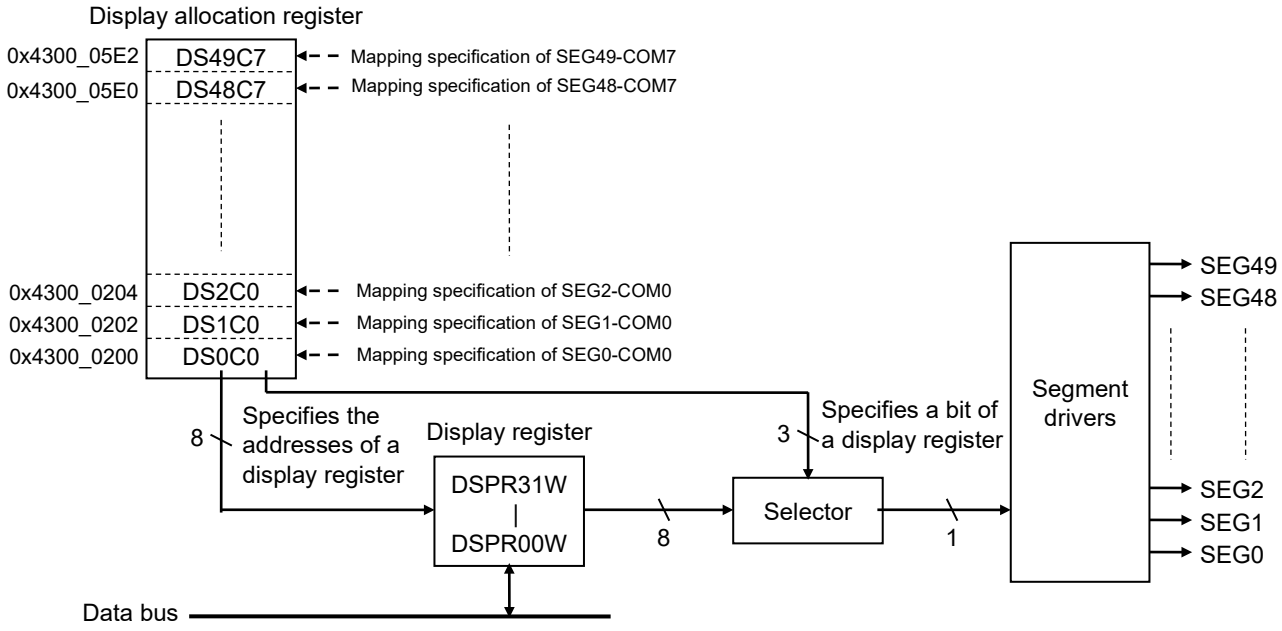


Figure 27-7 Configuration When Using the Programmable Display Allocation Function

In display allocation register (DSmCn: m = 0 to 49, n = 0 to 7), set the bit9-bit4 to the addresses (0x00 to 0x31) of the display registers (DSPR00W to DSPR31W) and set the bit2-bit0 of the display registers (DSPR00W to DSPR31W) that are output to common n of segment m.
For instance, to display bit 5 of display register 23 to common 3 of segment 16, set as follows.

Bit	9	8	7	6	5	4	3	2	1	0
Symbol name	a5	a4	a3	a2	a1	a0	-	b2	b1	b0
DS16C3 Register (0x4300_0B40)	1	0	0	0	1	1	-	1	0	1
	The lower 6 bits (=0x23) of 0x4300_0123							Bit position 5		

Note:
- Set display allocation data to display allocation register when the DASN bit of display control register (DSPMOD) is "0". When the DASN bit is "1", access from the CPU is invalid.

27.3.3. Common Output Waveforms

Figure 27-8 shows the common output waveforms for 1/8 duty and 1/3 bias.

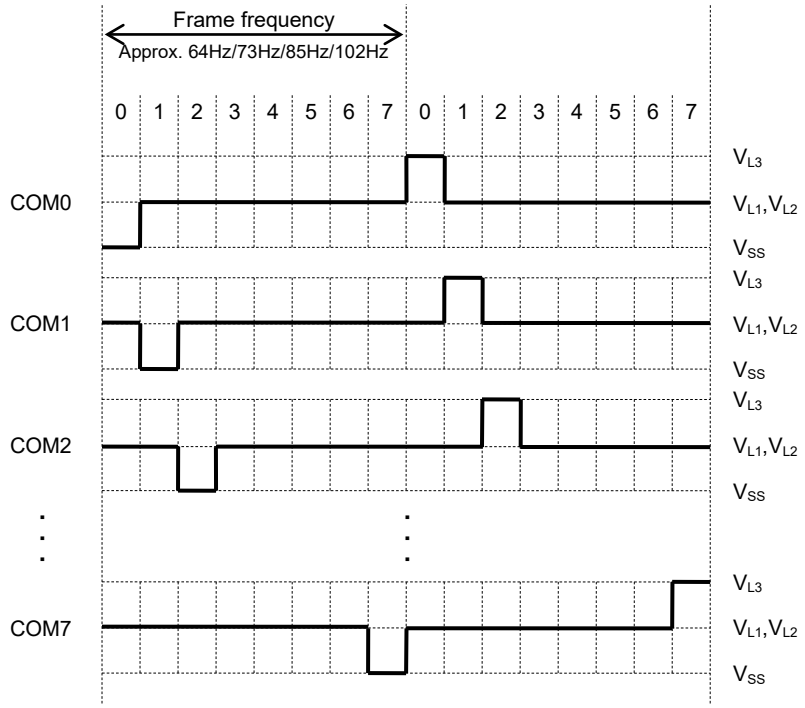


Figure 27-8 (1) Common Output Waveforms for 1/8 Duty and 1/2 Bias

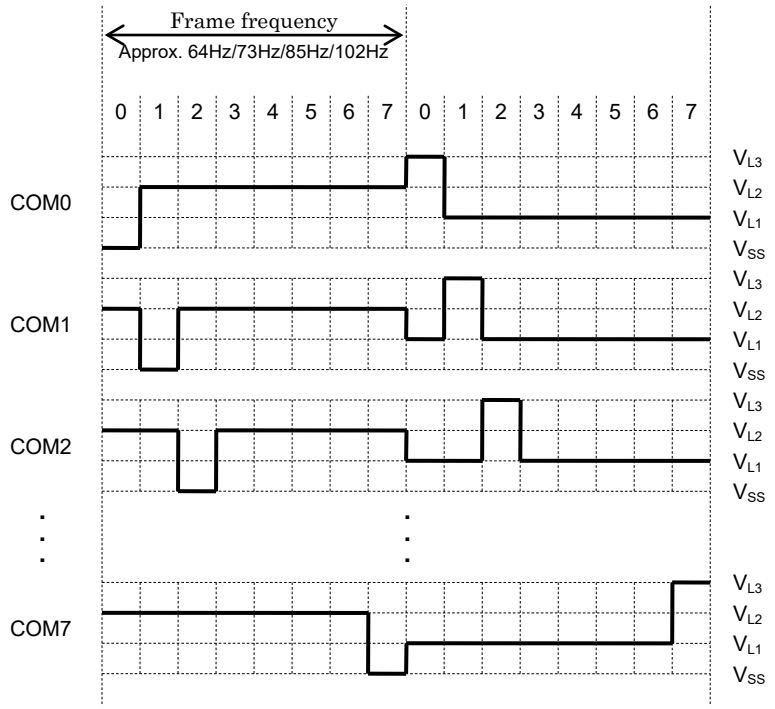


Figure 27-8 (2) Common Output Waveforms for 1/8 Duty and 1/3 Bias

27.3.4. Segment Output Waveforms

Figure 27-9 shows the segment output waveforms for 1/8 duty and 1/2 bias and for 1/8 duty and 1/3 bias.

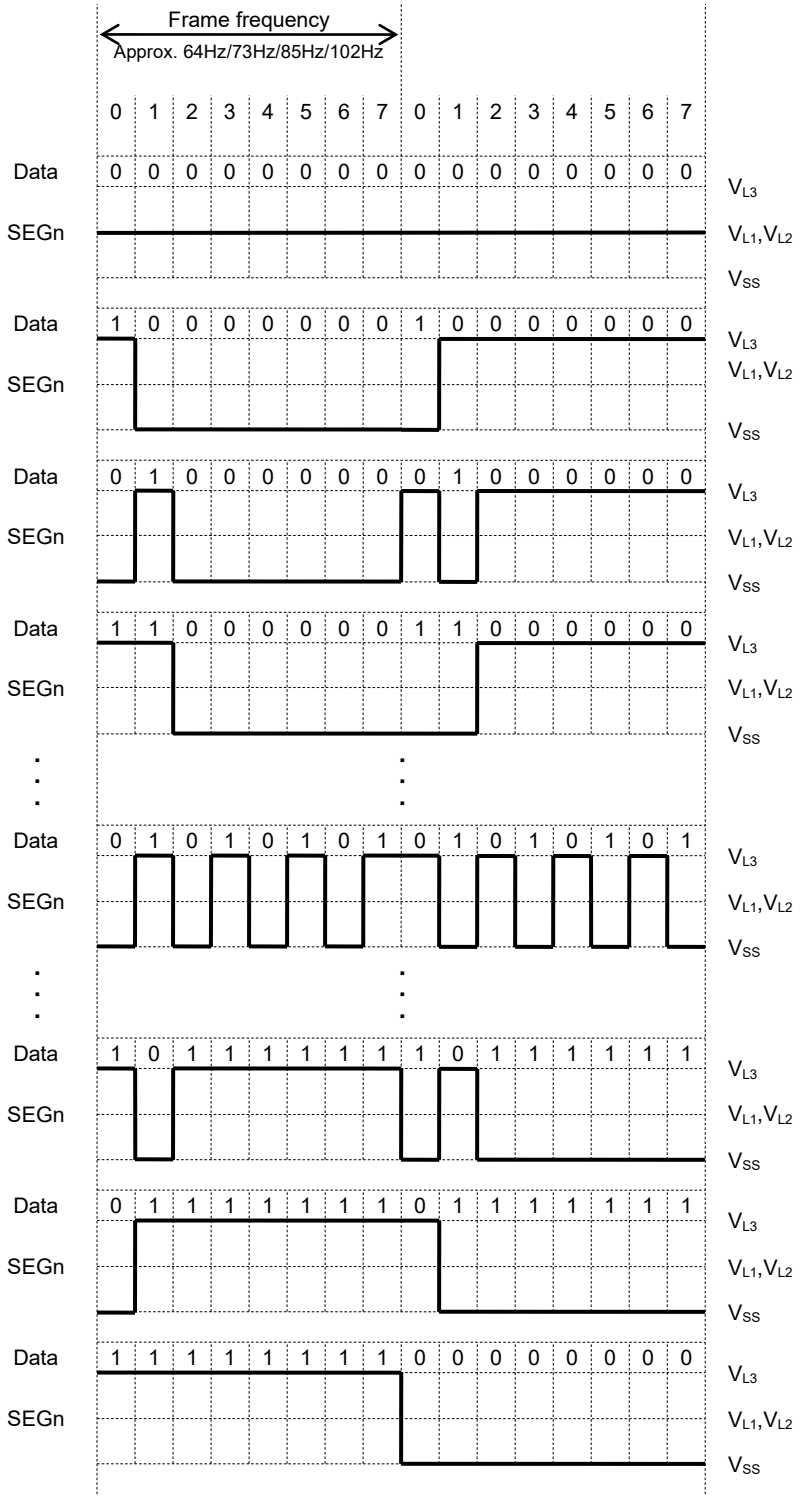


Figure 27-9 (1) Segment Output Waveforms for 1/8 Duty and 1/2 Bias

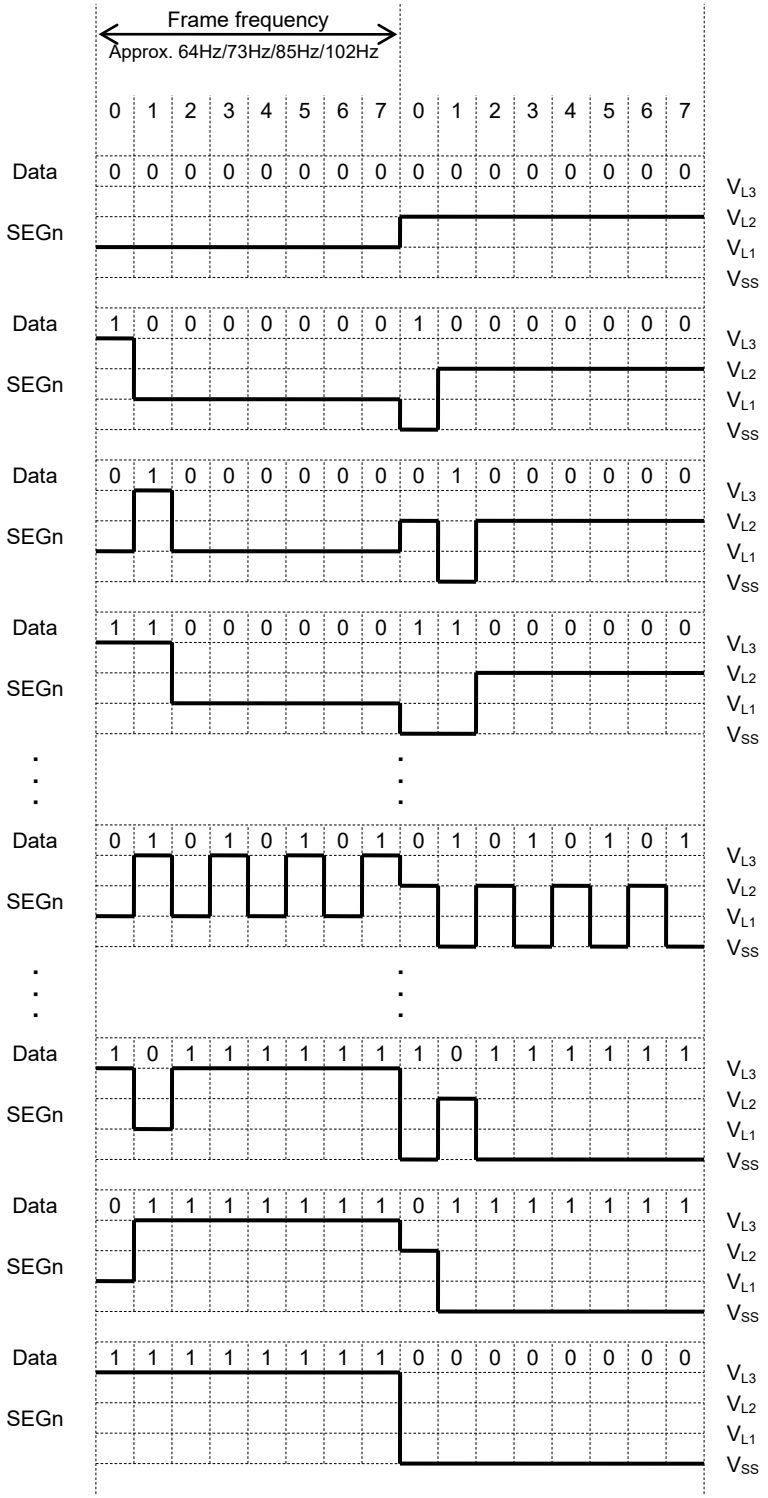


Figure 27-9 (2) Segment Output Waveforms for 1/8 Duty and 1/3Bias

Chapter 28

Analog Comparator

28. Analog Comparator

28.1. Overview

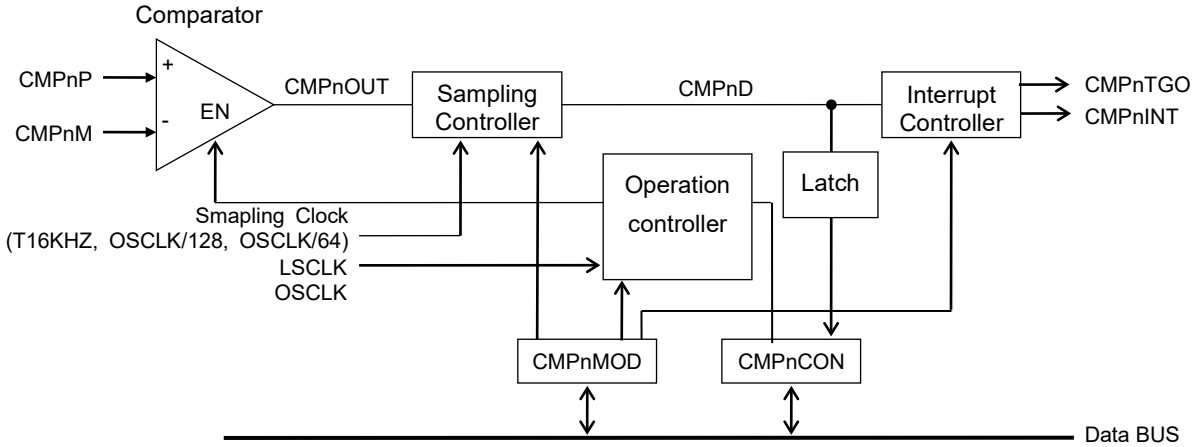
An analog comparator compares 2 input voltage and generate an interrupt corresponding to the comparison result.
This LSI has two channel analog comparator, can compare the voltages (differential input) supplied to two input pins (CMPnP and CMPnM, n=0, 1).

28.1.1. Features

- The comparator output can generate an interrupt.
- Allows selection of falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.
- The enable / disable of the sampling is selectable.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ, OSCLK/128(125kHz@OSCLK=16MHz, 187.5kHz@OSCLK=24MHz), OSCLK/64(250kHz @ OSCLK=16MHz, 375kHz@OSCLK=24MHz))
- The last status of comparator output (CMPnD) remains after the comparator is deactivated.
- Single mode is available.

28.1.2. Configuration

Figure 28-1 shows the configuration of the Comparator.



CMPnCON : Comparator control register n
CMPnMOD : Comparator mode register n
n = 0, 1

Figure 28-1 Configuration of Analog Comparator

28.1.3. List of Pins

Pin name	I/O	Description
P30/CMP0P	I	Analog comparator 0 non-inverted input pin
P31/CMP0M	I	Analog comparator 0 inverted input pin
P32/CMP1P	I	Analog comparator 1 non-inverted input pin
P33/CMP1M	I	Analog comparator 1 inverted input pin

28.2. Description of Registers

28.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_5100	Comparator 0 control register	CMP0CON	R/W	32	0x0000_0000
0x5C00_5104	Comparator 0 mode register	CMP0MOD	R/W	32	0x0000_0000
0x5C00_5180	Comparator 1 control register	CMP1CON	R/W	32	0x0000_0000
0x5C00_5184	Comparator 1 mode register	CMP1MOD	R/W	32	0x0000_0000
0x5C00_51A0	Comparator interrupt status register	CMPINTST	R/W	32	0x0000_0000

28.2.2. Comparator n Control Register (CMPnCON : n=0,1)

Address: 0x5C00_5100(CMP0CON), 0x5C00_5180(CMP1CON)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	CMPnRF	CMPnD	CMPnEN
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
CMPnCON is a special function register (SFR) to control the Comparator n.

[Description of Bits]

- **CMPnEN** (bit 0)
  The CMPnEN bit is used to control activation (ON) or deactivation (OFF) of the Comparator n.
  It is used to indicate Comparator active status.

CMPnEN	Description
0	Deactivates the Comparator n measurement is stopped(initial value)
1	Activates the Comparator n measurement is in progress

- **CMPnD** (bit 1)
  The CMPnD bit indicates the status of comparator n output (CMPnOUT shown in the Figure 28-1).
  It is set to "1" when the voltage at CMPnP pin is larger than the voltage at CMPnM pin (CMPnP > CMPnM), is set to "0" when the voltage at CMPnP pin is smaller than the voltage at CMnPM pin (CMPnP < CMPnM).
  The last status of this bit remains after the comparator is deactivated("0" is set to CMPnEN).

CMPnD	Description
0	CMPnP < CMPnM (initial value)
1	CMPnP > CMPnM

- **CMPnRF** (bit 2)
  The CMPnRF indicate the status of comparator n measurement setting.
  CMPnD is invalid until CMPnRF bit becomes 1 after starting measurement.

CMPnRF	Description
0	CMPnD is invalid (initial value)
1	CMPnD is valid

28.2.3. Comparator n mode Registers (CMPnMOD : n=0,1)

Address: 0x5C00_5104(CMP0MOD), 0x5C00_5184(CMP1MOD)
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	CMPnCK	–*	–*	CMPnSM[1:0]		–*	–*	CMPnMD[1:0]		–*	–*	CMPnE[1:0]	
Access	–	–	–	R/W	–	–	R/W	R/W	–	–	R/W	R/W	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
CMPnMOD is special function registers (SFRs) to set the function mode of Comparator n.
CMPnMOD needs to be set during CMPnEN is "0".

[Description of Bits]
- **CMPnE[1:0]**(bit 1 to 0)
  The CMPnE[1:0] are used to set comparator judge interrupt generation condition. Each function mode has different interrupt generation sources.

CMPnMD	CMPnE[1]	CMPnE[0]	Description
Single mode	0	*	Generate interrupt when CMPnD is "0"
	1	*	Generate interrupt when CMPnD is "1"
Single monitor mode	*	*	Setting is invalid (Generate interrupt once measurement is completed)
Supervisor mode	0	0	No interrupt (initial value)
	0	1	L interrupt : Generate interrupt when CMPnD is "0" CMPnD is "0" when starting measurement or CMPnD is changed from "1" to "0" during measurement.
	1	0	H interrupt : Generate interrupt when CMPnD is "1" CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.
	1	1	Both edge(L and H) interrupt CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" or "1" to "0" during measurement.

[Note]
This setting affects CMPnTGO signal. Refer to 28.3.2 for details. Use the CMPnTGO signal in Supervisor mode.

- **CMPnMD[1:0]** (bit 5 to 4)
  Set function mode.

CMPnMD[1]	CMPnMD[0]	Description
0	0	Single mode(initial value) After CMPnEN is set and complete the compare, if the interrupt condition is match, generate interrupt and stop automatically.
0	1	Single monitor mode After CMPnEN is set and complete the compare, generate interrupt and stop automatically.
1	*	Supervisor mode Compare is started by setting CMPnEN

- **CMPnCK, CMPnSM[1:0]** (bit 12, 9 to 8)
  Set comparator control clock and sampling interval timing for filtering.
  Sampling is always disabled regardless of sampling setting during the STOP mode.

CMPnCK	CMPnSM1	CMPnSM0	Description	
			Operation clock	Sampling period
0	*	0	Low speed LSCLK	No sampling
	*	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	61us
1	0	*	High speed 1/64 of OSCLK	No sampling
	1	0		4us (OSCLK=16MHz)
				2.67us (OSCLK=16MHz)
	1	1	High speed 1/128 of OSCLK	8us (OSCLK=16MHz)
				5.33us (OSCLK=24MHz)

[Note]
Keep OSCLK working at HALT mode when OSCLK is selected as control clock.
Depending on the operation mode, pay attention in the timing to set STOP mode.
Refer to the 28.3.1.1-3 for STOP mode switching timing of each operation mode.

28.2.4. Comparator Interrupt status Registers (CMPINTST)

Address: 0x5C00_51A0
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	CMP1INT	CMP0INT
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
The CMPINTST register is used to display the source of interrupt.

[Description of Bits]

- **CMP0INT** (bit 0)
  This bit is set to "1" when CMP0INT interrupt request is generated. The CMP0INT interrupt can be clear by writing "1" to this bit.

- **CMP1INT** (bit 1)
  This bit is set to "1" when CMP1INT interrupt request is generated. The CMP1INT interrupt can be clear by writing "1" to this bit.

28.3. Function description

28.3.1. Comparator function

The Comparator has following 3 modes.

1. Supervisor mode : Suitable for voltage monitor always.
2. Single mode : Suitable for voltage monitor regurarly. Generate interrupts par specified.
3. Single monitor mode : Suitable for voltage monitor regurarly. Software outputs compare result always.

28.3.2. Supervisor mode

This mode set comparator always on. And generate interrupt by valiation of the compare result.
Without interrupt, compare result can be monitor by reading CMPnD bit from Software.

Setting instruction:

(1) Set Operating clock, filtering, interrupt option, and supervisor mode by CMPnMOD register.
The operation of the CMPnTGO signal changes by this setting..

CMPnE[1:0]	Description	
	Interrupt	CMPnTGO signal
00	No interrupt	Asserted when CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.
01	L interrupt : Generate interrupt when CMPnD is "0" CMPnD is "0" when starting measurement or CMPnD is changed from "1" to "0" during measurement.	Asserted when CMPnD is "0" when starting measurement or CMPnD is changed from "1" to "0" during measurement.
10	H interrupt : Generate interrupt when CMPnD is "1" CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.	Asserted when CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.
11	Both edge(L and H) interrupt CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" or "1" to "0" during measurement.	

(2) Set CMPnEN
In case of interrupt, generate interrupt only when the condition set by CMPnE[1:0] match.

(3)After Trdy progress, CMPnRF becomes "1", and then CMPnD becomes valid;
In case of reading CMPnD with no interrupt or before gnerating interrupt, please make sure CMPnRF is "1".
Because status is stable waiting during CMPnRF is "0" at operation, CMPnD value is invalid.
CMPnRF need to be "1" when switch to STOP mode.

The timing chart is as follows.

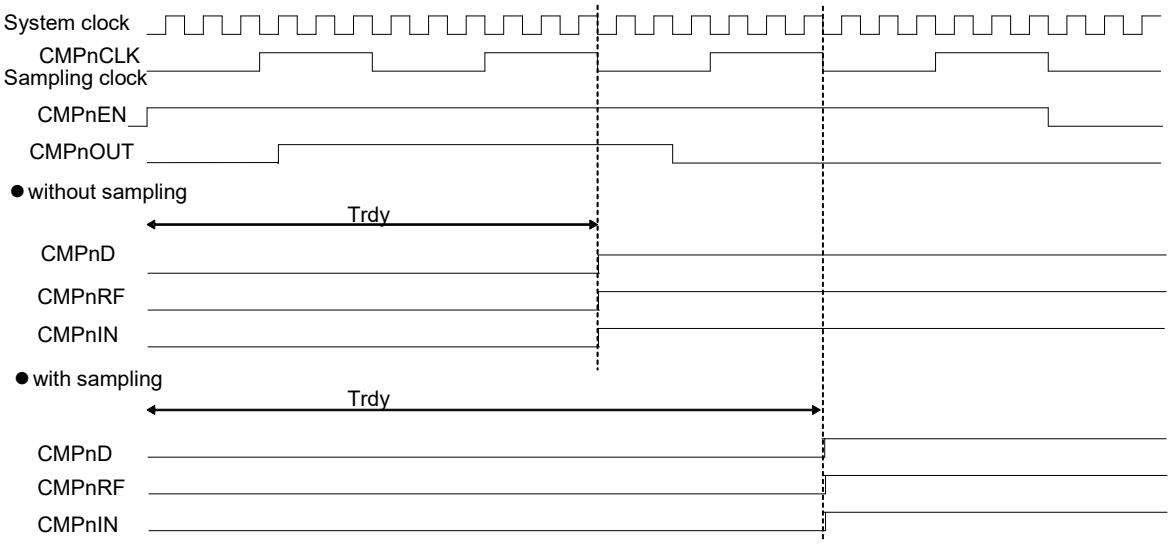


Figure 28-2 Timing in the supervisor mode

Time before CMPnD setting becoming valid is depending on operation/sampling clock setting.

CMPnCK	CMPnSM[1]	CMPnSM[0]	operation clock	Sampling	T_{rdy}	
0	0	0	Low speed LSCLK=32.768kHz	No filtering	3φ	91.6 us
0	0	1		T16KHZ(LTBC output: 1/2 LSCLK)	3φ	183.1 us
1	0	0	High Speed OSCLK=16MHz	No filtering	3φ	12.0 us
1	1	0		1/64 of OSCLK	4φ	16.0 us
1	1	1		1/128 of OSCLK	3φ	24.0 us

28.3.3. Single mode

This mode activate comparator as specified and generate interrupt by compare result, and deactivate comparator automatically by hardware.

Setting instruction:
(1) Set Operating clock, filtering, interrupt option, and single mode by CMPnMOD register.

CMPnE[1:0]	Description
00	Generate interrupt when CMPnD is "0"
01	
10	Generate interrupt when CMPnD is "1"
11	

(2) Set CMPnEN
(3) After Trdy progress, CMPnRF is set to "1", and then data is set to CMPnD. At that time, if the condition that was set by CMPnE[1:0] match, generate interrupt.
(4) After Tend progress, hardware set CMPnEN to "0". CMPnD compare result is kept until CMPnEN is set to "1".

Need interval (Trdy+Tend) of from CMPnEN setting to next MPnEN setting. It is recommended to confirm CMPnEN="0" before set CMPnEN.

It is prohibited to switch to STOP mode during operation. CMPnEN need to be set "0" when switch to STOP mode.

The timing chart is as follows

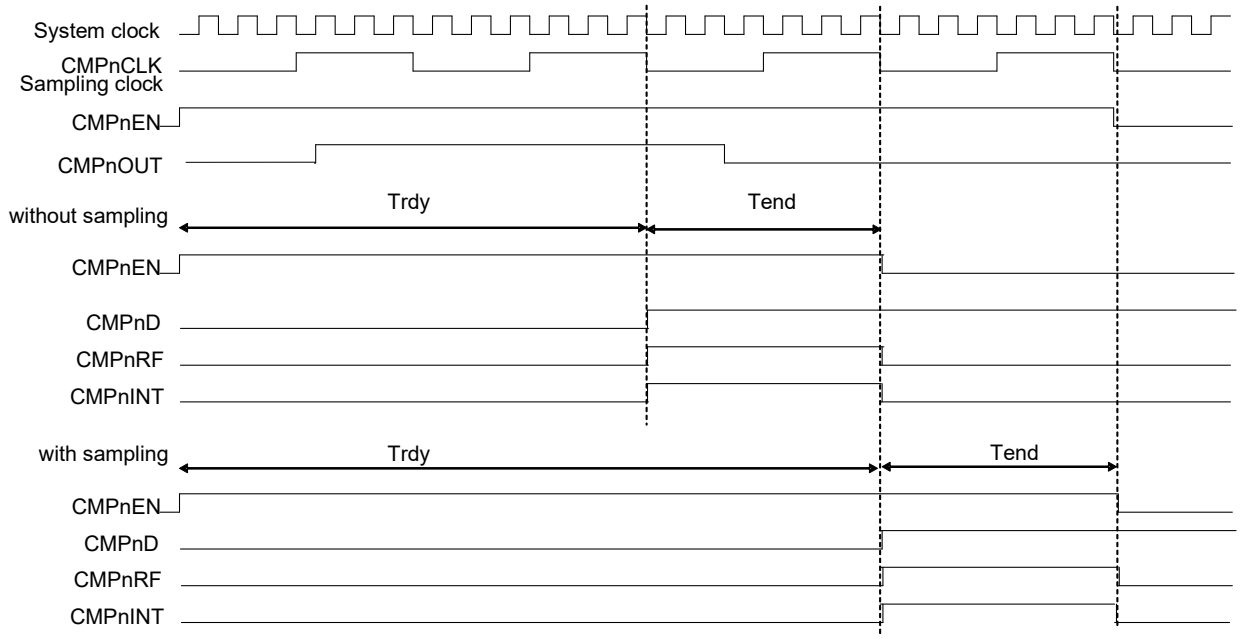


Figure 24-3 Timing in the single mode

Time before CMPnD setting becoming valid is depending on operation/sampling clock setting.

CMPnCK	CMPnSM[1]	CMPnSM[0]	Operation clock	Sampling	T_{rdy} (time to judge(interrupt))		$T_{rdy}+T_{end}$ (time to comparator off)	
0	0	0	Low speed LSCLK	OFF	3φ	91.6 us	3φ	91.6 us
0	0	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	ON	3φ	183.1 us	4φ	244.2 us
1	0	0	High speed 1/64 of OSCLK	OFF	3φ	12.0 us	4φ	16.0 us
1	1	0	High speed 1/64 of OSCLK	ON	4φ	16.0 us	5φ	20.0 us
1	1	1	High speed 1/128 of OSCLK	ON	3φ	24.0 us	4φ	32.0 us

28.3.4. Single monitor mode

This mode activate comparator as specified and generate interrupt after measurment, and deactivate comparator automatically by hardware.

Setting instruction:
(1)Set operation clock, filtering, and single monitor mode by CMPnMOD register.
Interrupt stting is invalid. Only complete interrupt is generated. Also complete interrupt is generated in case of suspend of operation by software.

(2) Set CMPnEN

(3) After Tend progress, comparator is automatically off and generate complete interrupt. Read CMPnD(Compare result) from software. CMPnD (Compare result) is kept until "1" is set to CMPnEN.

It is prohibited switch to STOP mode during operation. CMPnEN need to be "0" when switch to STOP mode.

The timing chart is as follows

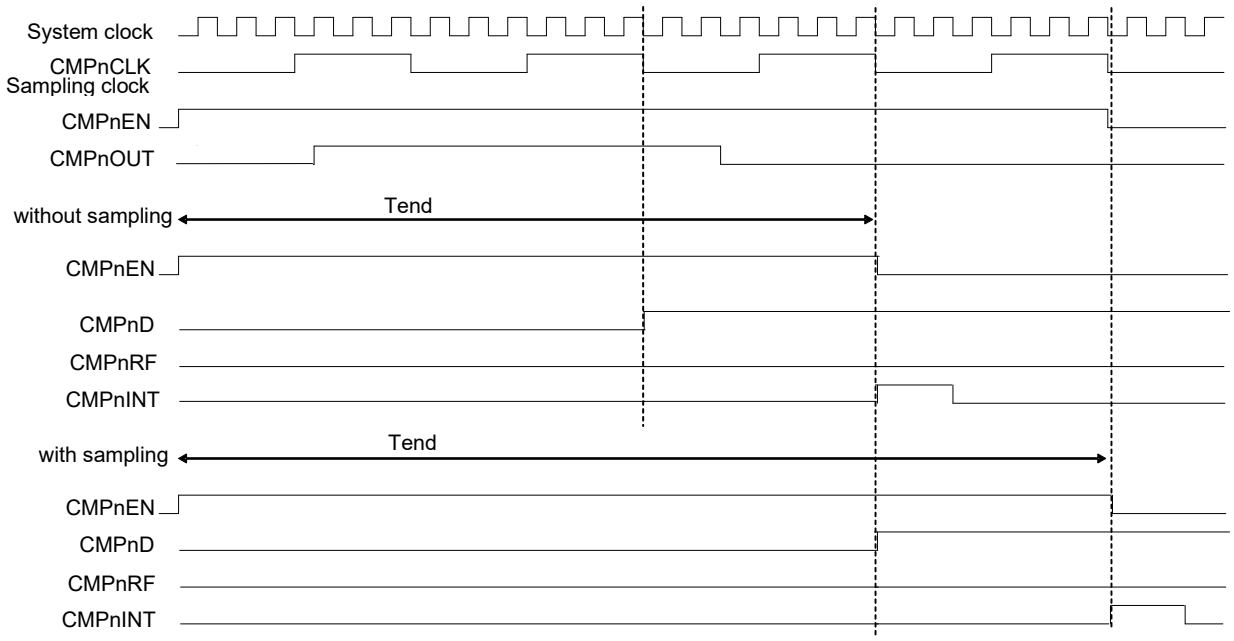


Figure 28-4 Timing in the single-monitor mode

Time before CMPnD setting becoming valid is depending on operation/sampling clock setting.

CMPnCK	CMPnSM[1]	CMPnSM[0]	Operation clock	Sampling	T_{end} (Time before turning off the comparator)	
0	0	0	Low speed LSCLK	OFF	4φ	122.0 us
0	0	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	ON	4φ	244.2 us
1	0	0	High speed 1/64 of OSCLK	OFF	4φ	16.0 us
1	1	0	High speed 1/64 of OSCLK	ON	5φ	20.0 us
1	1	1	High speed 1/128 of OSCLK	ON	4φ	32.0 us

Chapter 29

Flash Programming

29. Flash Programming

29.1. General Description

This LSI includes the self-rewrite function that rewrites the content of the flash memory (program memory space) using a special function register (SFR) programmatically.

29.1.1. Features

The self-rewrite function of the flash memory has the following features:

- Supports the writing by word (32 bits)
- Supports the erase types, sector erase (by 1 KB), block erase (by 8 KB)

29.2. Description of Registers

29.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4000_0400	Flash-ROM status register	FLCSTA	R	32	0x0000_0000
0x4000_0404	Flash-ROM acceptor register	FLCACP	W	32	0x0000_0000
0x4000_0408	Flash-ROM address register	FLCADR	R/W	32	0x1000_0000
0x4000_040C	Flash-ROM write data register	FLCWDA	W	32	0x0000_0000
0x4000_0410	Flash-ROM erase register	FLCERA	R/W	32	0x0000_0000
0x4000_0420	Flash-ROM size register	FLCRSIZ	R	32	0x0001_0800 (Q464) 0x0002_0800 (Q466)
0x4000_0424	Boot program address register	FLCBADR	R	32	0x0000_F000 (Q464) 0x0001_F000 (Q466)

29.2.2. Flash-ROM Status Register (FLCSTA)

Address: 0x4000_0400
Access: R
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	BUSY
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FLCSTA is a read-only, special function register (SFR) to indicate a state of the Flash-ROM.

[Description of Bits]
- **BUSY** (bit 0)
  Indicates a state of the Flash-ROM controller. This bit is "1" during sector erase/block erase/1-word write. It automatically changes to "0" when sector erase/block erase/1-word write is completed.

BUSY	Description
0	Sector erase/block erase/ 1-word write is completed
1	During sector erase/block erase/1-word write

29.2.3. Flash-ROM Acceptor Register (FLCACP)

Address: 0x4000_0404
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	FAC[7:0]							
Access	–	–	–	–	–	–	–	–	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FLCACP is a write-only special function register (SFR) to control enabling/disabling sector erase, block erase, and 1-word write operation for Flash-ROM rewrite.

[Description of Bits]

- **FAC[7:0]** (bit 7 to 0)
  FAC[7:0] is a register used to restrict sector erase, block erase, and 1-word write operations in order to prevent an unintended operation.
  Writing of "0x0000_00FA" and "0x0000_00F5" to FLCACP in this order enables a one-time sector erase, block erase, or 1-word write. When you use sector erase, block erase, or 1-word write in succession, you must write "0x0000_00FA" and "0x0000_00F5" in FLCACP every time.
  Even if another instruction is inserted between “0x0000_00FA” and “0x0000_00F5” written to FLCACP, the sector erase, block erase, or 1-word write is enabled. However, if you write data other than "0x0000_00F5" in FLCACP after writing "0x0000_00FA", it is disabled. Therefore, you must write from "0x0000_00FA" again to enable it. In addition, if you write to FLCACP without executing erase or 1-word write after writing "0x0000_00FA" and "0x0000_00F5", it is disabled regardless of the value. Therefore, you must write "0x0000_00FA" and "0x0000_00F5" in this order again to enable it.

[Note]
If writing ”00” in FLE field with the FLCACP register enabled, it is still maintained as enabled.

29.2.4. Flash-ROM Address Register (FLCADR)

Address: 0x4000_0408
Access: R/W
Access size: 32 bit
Initial value: 0x1000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	FA[31:16]															
Access	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FA[15:2]														–*	–*
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FLCADR is a special function register (SFR) to set Flash-ROM rewrite addresses.

[Description of Bits]

- **FA[31:2]** (bit 31 to 2)
  FA[31:2] are the bits used to set the address for sector erase, block erase, and 1-word write. When the sector erase is operated, FA[31:10] is used. When the block erase is operated, FA[31:13] is used. When the 1-word write is operated, FA[31:2] is use.

[Note]
Rewriting this register while BUSY bit of FLCSTA register is “1” is prohibited.
The read only bit (“Access” is “R”) is not changed.

29.2.5. Flash-ROM Write Data Register (FLCWDA)

Address: 0x4000_040C
Access: W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	FD[31:16]															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FD[15:0]															
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
It will always read "0" when read.

[Description of Register]
FLCWDA is a special function register (SFR) to set Flash-ROM rewrite data.

[Description of Bits]

- **FD[31:0]** (bit 31-0)
  FD[31:0] is a bit used to set write data for 1-word write.
  Write to FD[31:0] starts the 1-word write.

[Note]
Erase the contents of the target write addresses in advance. The content of an overwritten address is not guaranteed.
Rewriting this register while BUSY bit of FLCSTA register is “1” is prohibited.

29.2.6. Flash-ROM Erase Register (FLCERA)

Address: 0x4000_0410
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	FLE[1:0]	
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FLCERA is a special function register (SFR) used to start sector erase, block erase of Flash-ROM.

[Description of Bits]

- **FLE[1:0]** (bit 1 to 0)
  FLE is a bit used to specify the type and start of erase.
  Write to FLE starts erase according to the data. It automatically changes to "00" when the erase is completed. Writing to "00" is prohibited.

FLE[1:0]	Description
00	Erase completed (initial value)
01	Setting prohibited
10	Start block erase
11	Start sector erase

[Note]
Rewriting this register while BUSY bit of FLCSTA register is "1" is prohibited.

29.2.7. Flash-ROM Size Register (FLCRSIZ)

Address: 0x4000_0420
Access: R
Access size: 32 bit
Initial value: 0x0001_0800 (Q464), 0x0002_0800 (Q466)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	FSI[31:16]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	1/0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	FSI[15:0]															
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

[Description of Register]
FLCRSIZ is a special function register (SFR) used to indicate the size of Flash-ROM (in bytes).

[Description of Bits]

- **FSI[31:0]** (bit 31 to 0)

FSI[31:0] is a bit used to indicate the size of Flash-ROM (in bytes) including both the program region and the data region.
In ML630Q464, this size is 66KB. In ML630Q466, this size is 130KB.

29.2.8. Boot Program Address Register (FLCBADR)

Address: 0x4000_0424
Access: R
Access size: 32 bit
Initial value: 0x0000_F000(Q464), 0x0001_F000(Q466)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	BPA[17:16]	
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	BPA[15:2]														–*	–*
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	–	–
Initial value	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
FLCBADR is a special function register (SFR) used to indicate the start address of the boot program area at the hardware remap.

[Description of Bits]

- **BPA[17:2]** (bit 17 to 2)
  BPA[17:2] is a bit used to indicate the start address of the boot program area (4KB) at the hardware remap.

29.3. Description of Operation

29.3.1. Erase/Write Flash-ROM

As Flash-ROM erase function, there are the erase of two types which are the sector erase (1KB), the block erase (8KB). It is possible that the Flash-ROM is able to written on the erased area by 1-word write. It is needed to access the register of the Flash-ROM controller from the CPU according to the procedure for erasing and writing to the Flash-ROM.

It includes the flash rewrite acceptor function which restricts the rewrite operation to prevent an improper rewrite to Flash-ROM. Writing of "0x0000_00FA" and "0x0000_00F5" to the Flash ROM acceptor register (FLCACP) in this order enables sector erase, block erase, or 1-word write only once.

[Note]
Software reset during Flash-ROM erase/write is prohibited.

29.3.2. Sector Erase

This function erases data in the main area of Flash-ROM by sector.

Erase of the specified sector data is started when you write "0x0000_00FA" and "0x0000_00F5" to Flash ROM acceptor register (FLCACP), set the sector address to the Flash ROM address register (FLCADR), and write "11" to FLE bit of Flash ROM erase register (FLCERA). The FLCSTA register is "0x0000_0001" during erase. When erase is completed, the FLCSTA register changes to "0x0000_0000".

The CPU enters the waiting state when reading of Flash-ROM occurs during erase. Write access to the register during erase is prohibited.

Figure 29-1 shows the processing flow of sector erase.

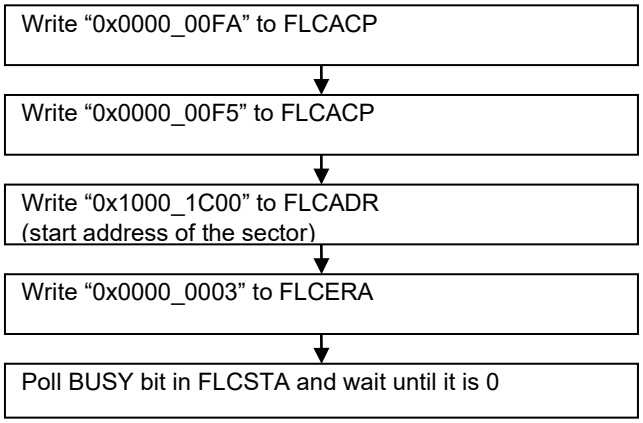


Figure 29-1 Program Flow of Sector Erase (When Executed on RAM)

29.3.3. Block Erase

This function erases data in the main area of Flash-ROM by block.

Erase of the specified block data is started when you write “0x0000_00FA” and “0x0000_00F5” to Flash ROM acceptor register (FLCACP), set the block address to the Flash ROM address register (FLCADR), and write “10” to FLE bit of Flash ROM erase register (FLCERA). The FLCSTA register is “0x0000_0001” during erase. When erase is completed, the FLCSTA register changes to “0x0000_0000”.

The CPU enters the waiting state when reading of Flash-ROM occurs during erase. Write access to the register during erase is prohibited.

Figure 29-2 shows the processing flow of block erase.

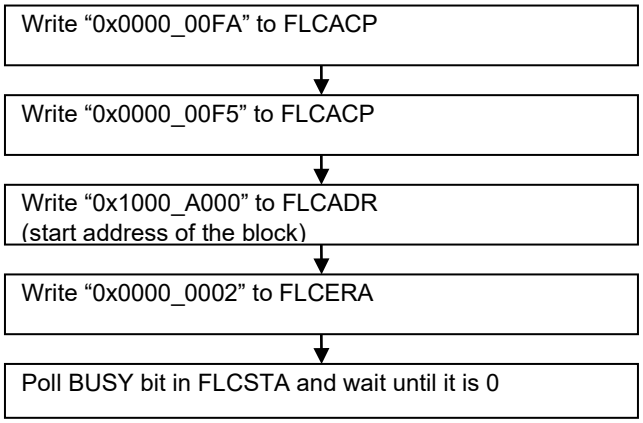


Figure 29-2 Program Flow of Block Erase (When Executed on RAM)

29.3.4. 1-word Write

This function writes data of Flash-ROM in 4 bytes.

Write to the specified address is started when you write "0x0000_00FA" and "0x0000_00F5" to Flash ROM acceptor register (FLCACP), set the address to the Flash ROM address register (FLCADR), and write data to Flash ROM write data register (FLCWDA). During 1-word write, the FLCSTA register is “0x0000_0001”. When write is completed, the FLCSTA register changes to “0x0000_0000”.

The CPU enters the waiting state when reading of Flash-ROM occurs during write. Write access to the register during write is prohibited.

Figure 29-4 shows the program flow of 1-word write.

[Note]
Data should be written to an erased area on Flash-ROM. In addition, when you want to rewrite data that is written once, erase it before writing it again.

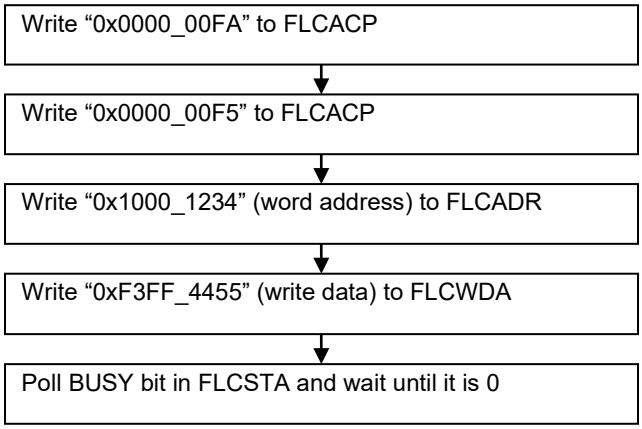


Figure 29-3 Flow of 1-word Write (When Execute on RAM)

29.3.5. Erase/Write to Area Where Flash-ROM Is Not Implemented

It is prohibited to specify an area where Flash-ROM is not implemented to execute the erase or 1-word write. If it is executed, the Flash-ROM is not updated. The BUSY field of the Flash ROM status register (FLCSTA) changes to ”1”, but goes back to ”0” in a short time because the Flash-ROM is not updated.

29.3.6. Notes in Use

If the power is down or the operation is terminated forcibly during the erase or 1-word write, retry the erase and rewrite the area.

Chapter 30

Voltage Level Supervisor (VLS)

30. Voltage Level Supervisor (VLS)

30.1. General Description

This LSI has one channel of built-in Voltage Level Supervisor (VLS).
This function can be used to judge whether the voltage level of V_{DD}/V_{VLSP} is lower than the specified threshold voltage.

30.1.1. Features

- Accuracy: ±3%
- Threshold voltage: Selectable from 64 values (1.200V to 3.550V)
- Can be used as voltage level detection reset (VLS reset)
- Can be used as voltage level detection interrupt (VLS interrupt)
- Selectable V_{DD} or external input pin(V_{VLSP}) as input of the comparator

30.1.2. Configuration

The VLS consists of a comparator and a low level detection reset control circuit.
Figure 30-1 shows the configuration of the VLS.

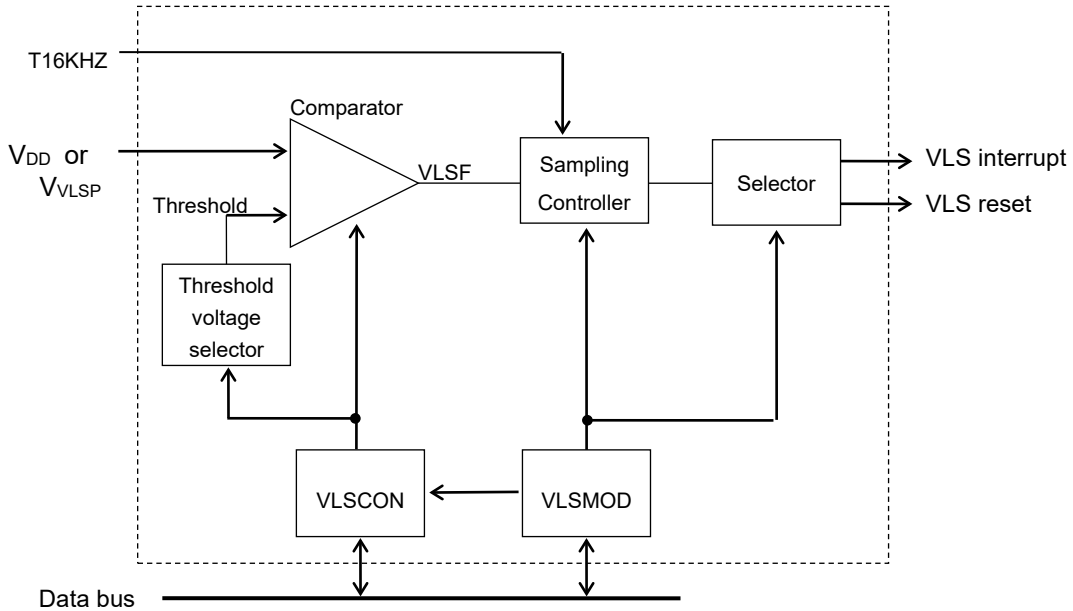


Figure 30-1 Configuration of Voltage Level Supervisor

30.2. Description of Registers

30.2.1. List of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_5000	Voltage level supervisor control register	VLSCON	R/W	32	0x0000_0000
0x5C00_5004	Voltage level supervisor mode register	VLSMOD	R/W	32	0x0000_0000

30.2.2. Voltage level supervisor control register (VLSCON)

Address: 0x5C00_5000
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	VLSPE	–*	–*	–*	–*	VLSRF	VLSF	ENVLS	–*	–*	VLSLV[5:0]					
Access	R/W	–	–	–	–	R	R	R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
VLSCON is a special function register (SFR) used to control the voltage level detector. This register is not initialized when VLS reset is occurred.

[Description of Bits]

- **VLSLV[5:0]** (bit 5 to 0)
  The VLSLV[5:0] bits are used to select the VLS threshold voltage of fall (V_{VLS}). The VLS has the hysteresis characteristics (H_{VLS}). The threshold voltage of rise is $V_{VLS} + H_{VLS}$. For detail, see VLS characteristic in Appendix C. They should be set when the VLS is in the OFF state (ENVLS="0"). 0~17H is available only at the time of VLSPE=1. Cannot set the value that is bigger than V_{DD}.

VLSLV[5]	VLSLV[4]	VLSLV[3]	VLSLV[2]	VLSLV[1]	VLSLV[0]	Description
0	0	0	0	0	0	1.200V
0	0	0	0	0	1	1.225V
0	0	0	0	1	0	1.250V
0	0	0	0	1	1	1.275V
0	0	0	1	0	0	1.300V
0	0	0	1	0	1	1.325V
0	0	0	1	1	0	1.350V
0	0	0	1	1	1	1.375V
0	0	1	0	0	0	1.400V
0	0	1	0	0	1	1.425V
0	0	1	0	1	0	1.450V
0	0	1	0	1	1	1.475V
0	0	1	1	0	0	1.500V
0	0	1	1	0	1	1.525V
0	0	1	1	1	0	1.550V
0	0	1	1	1	1	1.575V

VLSLV[5]	VLSLV[4]	VLSLV[3]	VLSLV[2]	VLSLV[1]	VLSLV[0]	Description
0	1	0	0	0	0	1.600V
0	1	0	0	0	1	1.625V
0	1	0	0	1	0	1.650V
0	1	0	0	1	1	1.675V
0	1	0	1	0	0	1.700V
0	1	0	1	0	1	1.725V
0	1	0	1	1	0	1.750V
0	1	0	1	1	1	1.775V
0	1	1	0	0	0	1.800V
0	1	1	0	0	1	1.825V
0	1	1	0	1	0	1.850V
0	1	1	0	1	1	1.875V
0	1	1	1	0	0	1.900V
0	1	1	1	0	1	1.925V
0	1	1	1	1	0	1.950V
0	1	1	1	1	1	1.975V
1	0	0	0	0	0	2.000V
1	0	0	0	0	1	2.050V
1	0	0	0	1	0	2.100V
1	0	0	0	1	1	2.150V
1	0	0	1	0	0	2.200V
1	0	0	1	0	1	2.250V
1	0	0	1	1	0	2.300V
1	0	0	1	1	1	2.350V
1	0	1	0	0	0	2.400V
1	0	1	0	0	1	2.450V
1	0	1	0	1	0	2.500V
1	0	1	0	1	1	2.550V
1	0	1	1	0	0	2.600V
1	0	1	1	0	1	2.650V
1	0	1	1	1	0	2.700V
1	0	1	1	1	1	2.750V
1	1	0	0	0	0	2.800V
1	1	0	0	0	1	2.850V
1	1	0	0	1	0	2.900V
1	1	0	0	1	1	2.950V
1	1	0	1	0	0	3.000V
1	1	0	1	0	1	3.050V
1	1	0	1	1	0	3.100V
1	1	0	1	1	1	3.150V
1	1	1	0	0	0	3.200V
1	1	1	0	0	1	3.250V
1	1	1	0	1	0	3.300V
1	1	1	0	1	1	3.350V
1	1	1	1	0	0	3.400V

VLSLV[5]	VLSLV[4]	VLSLV[3]	VLSLV[2]	VLSLV[1]	VLSLV[0]	Description
1	1	1	1	0	1	3.450V
1	1	1	1	1	0	3.500V
1	1	1	1	1	1	3.550V

- **ENVLS** (bit 8)
  The ENVLS bit is used to control ON/OFF of the VLS.
  VLS is turned on when ENVLS is set to "1", and off when "0".
  When the VLS reset is issued, the VLS keep the ON state.

ENVLS	Description
0	VLS: OFF (initial value)
1	VLS : ON

[Note]
When set ENVLS effectively after return from HALT-H, set ENVLS effectively after waiting for 60μs from return.

- **VLSF** (bit 9)
  VLSF is the voltage level detection flag.
  It is "0" when the power supply voltage which is selected VLSPE bit (V_{DD} or V_{VLSP}) is higher than the threshold voltage (V_{VLS}), or "1" when the power supply voltage is lower than the threshold voltage.
  VLSF is initialized to 0 when VLS is set to on (ENVLS=1).

VLSF	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

- **VLSRF** (bit 10)
  The VLSRF flag is used to indicate whether the voltage level detection result is valid.
  When the threshold voltage value becomes valid (readable from CPU), this becomes "1".

VLSRF	Description
0	VLS is OFF or VLS is being judged (initial value)
1	VLS judgment result is valid

[Note]
Make sure that the VLSRF bit is set to "1" before enabling the STOP mode.

- **VLSPE** (bit 15)
  The VLSPE bit is used to select VLS input pin or V_{DD} level as the voltage input.

VLSPE	Description
0	V_{DD} is selected (initial value)
1	VLS input pin is selected (V_{VLSP})

30.2.3. Voltage level supervisor mode register (VLSMOD)

Address: 0x5C00_5004
Access: R/W
Access size: 32 bit
Initial value: 0x0000_0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Symbol name	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*	–*
Access	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol name	–*	–*	–*	–*	–*	–*	–*	VLSSM0	–*	–*	–*	–*	–*	–*	VLSSEL[1:0]	
Access	–	–	–	–	–	–	–	R/W	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
*: Reserved bit for future expansion. It will always read "0" when read. Write "0" when writing.

[Description of Register]
VLSMOD is a special function register (SFR) used to control the voltage level detection function.
It is necessary to set this register during the VLS is in the OFF state (ENVLS="0")
This register is not initialized when VLS reset is occurred.

[Description of Bits]

- **VLSSEL[1:0]** (bit 1 to 0)
  The VLSSEL[1:0] bits are used to control enable/disable of the VLS reset/VLS interrupt request functions when the voltage is lower than the threshold voltage.

VLSSEL[1]	VLSSEL[0]	Description
0	0	Reset function: disable, Interrupt request function: disable (initial value)
0	1	Reset function: enable, Interrupt request function: disable
1	0	Reset function: disable, Interrupt request function: enable
1	1	Reset function: enable, Interrupt request function: disable

- **VLSSM0** (bit 8)
  The VLSSM0 bit is used to select whether or not to use sampling for the VLS detection.

VLSSM0	Description
0	Detects without sampling (initial value)
1	Detects with sampling (T16KHZ 2ϕ)

[Note]
In the STOP mode, no sampling is performed regardless of the value set in VLSSM0 since the sampling clock stops. The sampling depends on the frequency of LSCLK.

30.3. Description of Operation

The VLS can judge whether the power supply voltage which is selected VLSPE bit (V_{DD} or V_{VLSP}) is lower or higher than the specified threshold voltage by reading SFR, and also it can issue a VLS interrupt or VLS reset when the power supply voltage becomes lower than the specified threshold voltage.
The VLS has a hysteresis characteristics (H_{VLS}), the threshold voltage of rise is $V_{VLS} + H_{VLS}$. For detail, see VLS characteristic in Appendix C.

The following an operation mode is provided:

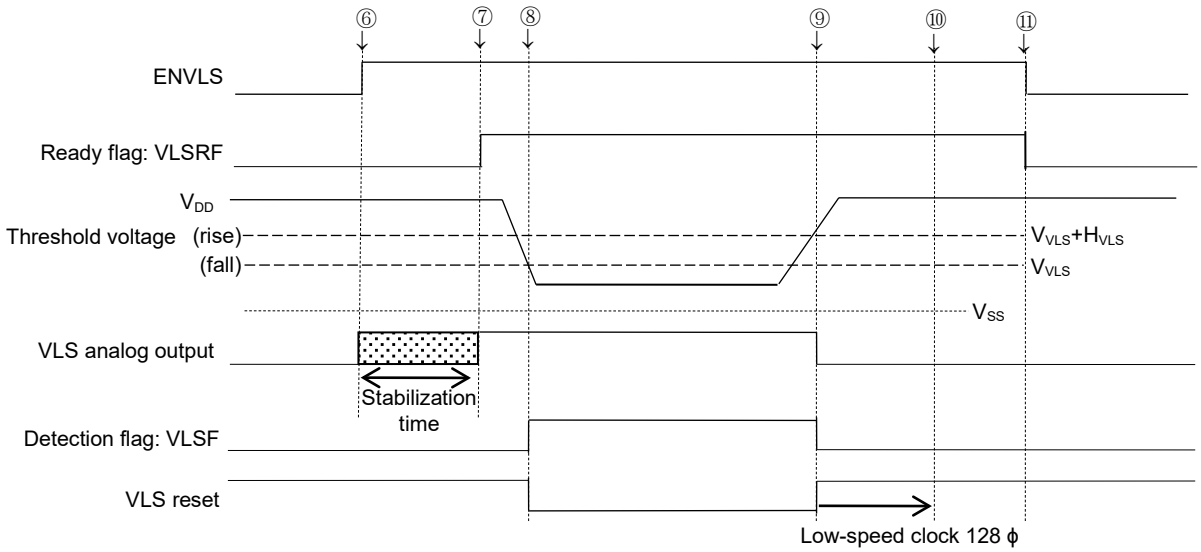
Supervisor mode:

Set ENVLS to ”1” to turn on VLS for voltage judgment. When the judgment result becomes valid, it is notified by using the VLSRF flag. The judgment still continues.
VLS interrupt or VLS reset can be set to constantly monitor the power supply voltage and issue an interrupt or reset when it becomes lower than the threshold voltage.

30.3.1. Supervisor mode

The supervisor mode is useful for using the low voltage detection interrupt/reset with always-ON. The detection flag(VLSF)/reset is masked until the ready flag is asserted.
If VLS interrupt is used, set the VLS interrupt before setting ENVLS.
VLSRF (ready flag) is asserted when T16KHZ 4ϕ (+2 ϕwhen the sampling is enabled) passes after setting ENVLS. The software should read the VLSF value after VLSRF=”1”.
Even if the VLS interrupt or VLS reset is allowed, the issue is allowed after VLSRF is asserted.
When the power supply voltage which is selected VLSPE bit (V_{DD} or V_{VLSP}) becomes lower than the specified threshold voltage, a VLS interrupt or VLS reset is issued.
To turn off the VLS function, set ENVLS to ”0” from the software.

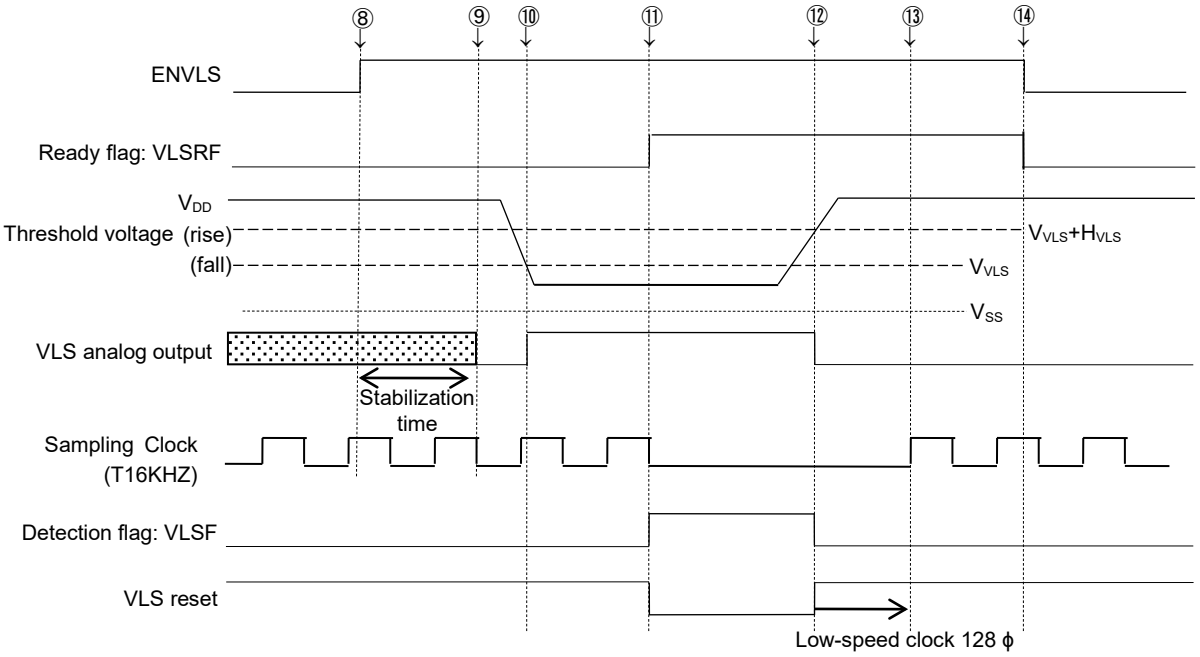
Figure 30-2 shows an example of the operation timing diagram when detecting without sampling and setting the VLS reset issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② When the VLS analog output is stabilized, the ready flag (VLSRF) is set to ”1”.
③ The voltage level detection flag (VLSF) is set to “1” to issue a VLS reset because V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The voltage level detection flag (VLSF) is set to “0” to release the VLS is reset because V_{DD} becomes higher than the specified threshold voltage ($V_{VLS}+H_{VLS}$).
⑤ The CPU starts operation after 128ϕ of low-speed clock.
⑥ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 30-2 Operation Timing Diagram When Detecting without Sampling and Setting VLS Reset Issue

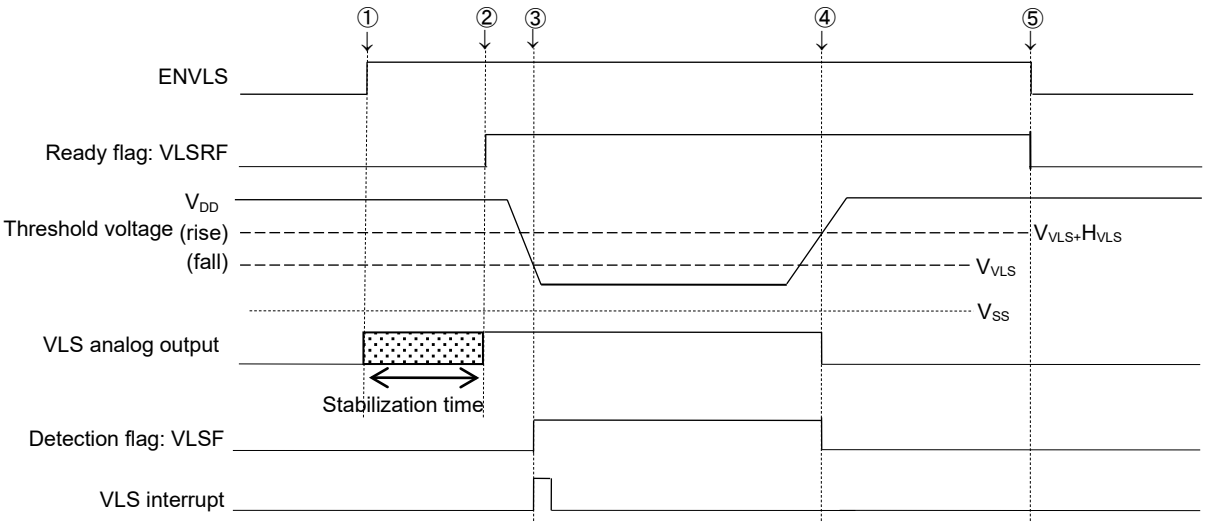
Figure 30-3 shows an example of the operation timing diagram when detecting with sampling and setting the VLS reset issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② The VLS analog output is stabilized.
③ V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The ready flag (VLSRF) is set to “1” after T16KHZ2ϕ. At the same time, the voltage level detection flag (VLSF) is set to “1” to issue a VLS reset because the VLS analog voltage is lower than the threshold voltage (V_{VLS}).
⑤ The voltage level detection flag (VLSF) is set to “0” to release the VLS reset because the V_{DD} returns to higher than the threshold voltage of rise ($V_{VLS}+H_{VLS}$).
⑥ The CPU starts after 128 ϕ of low-speed clock. Then the VLS does not operate while T16KHZ stops.
⑦ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 30-3 Operation Timing Diagram When Detecting with Sampling and Setting VLS Reset Issue

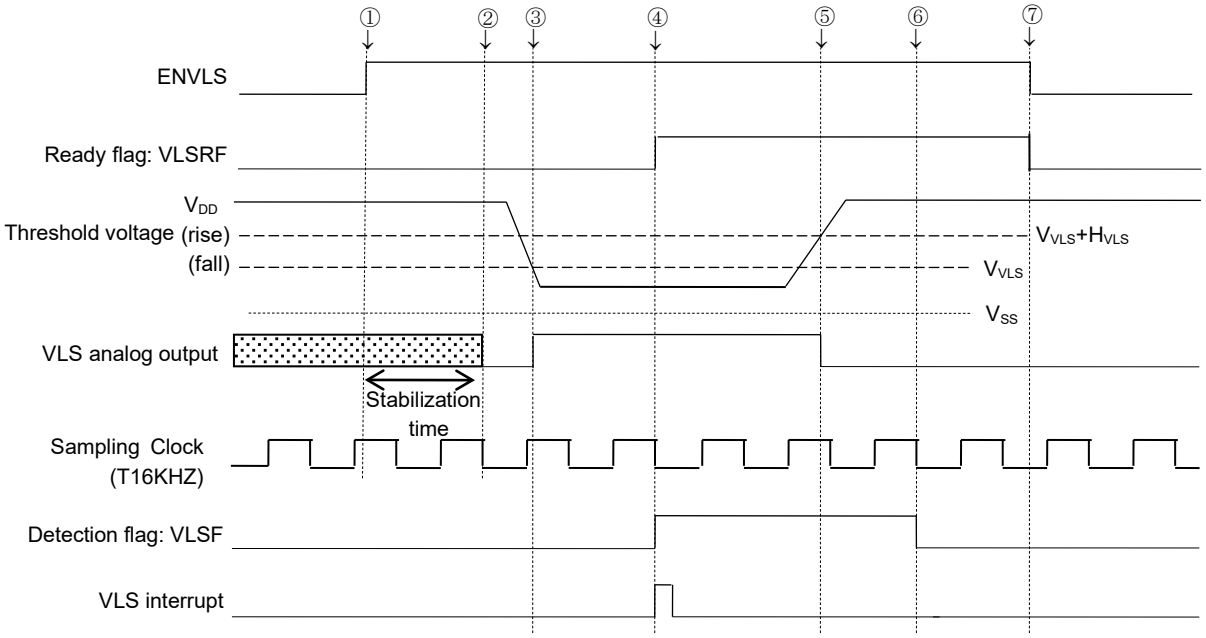
Figure 30-4 shows an example of the operation timing diagram when detecting without sampling and setting the VLS interrupt issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② When the VLS analog output is stabilized, the ready flag (VLSRF) is set to ”1”.
The voltage level detection flag (VLSF) is set to “1” to issue a VLS interrupt because V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
③ The voltage level detection flag (VLSF) is set to “0” because V_{DD} becomes higher than the threshold voltage of rise ($V_{VLS}+H_{VLS}$).
④ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 30-4 Operation Timing Diagram When Detecting without Sampling and Setting VLS Interrupt Issue

Figure 30-5 shows an example of the operation timing diagram when detecting with sampling and setting the VLS interrupt issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② The VLS analog output is stabilized.
③ V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The ready flag (VLSRF) is set to ”1” after T16KHZ2ϕ. At the same time, the voltage level detection flag (VLSF) is set to “1” to issue a VLS interrupt because the VLS analog voltage is lower than the threshold voltage (V_{VLS}).
⑤ V_{DD} returns to higher than the threshold voltage of rise ($V_{VLS}+H_{VLS}$).
⑥ Because it is judged that a VLS analog voltage sampled at T16KHZ is higher than the threshold voltage ($V_{VLS}+H_{VLS}$),
the voltage level detection flag (VLSF) is set to “0”.
⑦ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 30-5 Operation Timing Diagram When Detecting with Sampling and Setting VLS interrupt issue

Chapter 31

LLD circuit

31. LLD circuit

31.1. General Description

LLD circuit monitors Power supply Voltage level. When Power supplly Voltage falls than the threshold voltage, LLD reset this LSI.

31.1.1. Features

- Judgement Voltage:1.8V±0.2V
- generate LSI reset
- Selectable LLD enable/disable

31.2. Description of resister

Control LLD validation by resister setting.
LLD is invaldated initically.
LLD can be validated by setting reset control resister (RSTCON) RLLD bit to "0".

31.3. Description of operation

LLD circuit is controlled by RLLD bit of reset control register (RSTCON).
This circuit compares the power supply voltage with the threshold voltage.If the power supply voltage is below the threshold voltage, LLD generate reset.
See DC characterristics(LLD) of AppendixC "Electrical Characteristcs" for details about the threshold voltage.

Chapter 32

On-Chip Debug Function

32. On-Chip Debug Function

32.1. General Description

This LSI implements a SW-DP (serial wire debug port) as the debug interface.
The connection example is shown in Figure 32-1. For details, see the debugger manual.
[Note] The timer and WDT clock are stopped at break in the debugger.

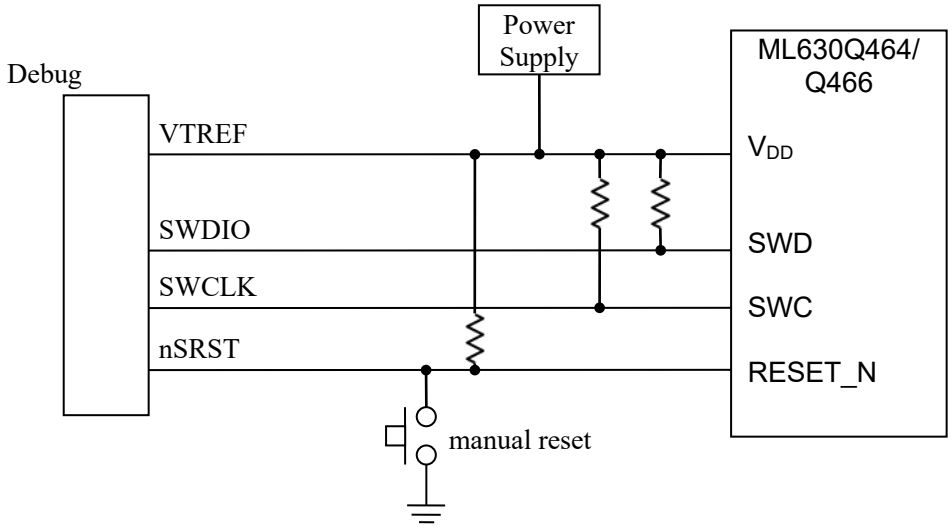


Figure 32-1 Connection with Debug Connector

32.2. Restriction

When connecting the debugger and , HALT mode, HALT-H mode, and DEEP-HALT/ULTRA DEEP-HALT mode are not worked. Therefore these mode are worked as sleep mode.
The behavior of these modes is verified without the debugger.
The difference between connecting the debbuger and Not connecting the debbuger is as follows.

Item	Connecting the debugger (as same as sleep mode)			Not Connecting the debugger		
	HLT	HLTH	DHLT/UDHLT	HLT	HLTH	DHLT/UDHLT
CPU clock	stopped	stopped	stopped	stopped	stopped	stopped
Peripheral clock (high speed)	oscillated	oscillated	oscillated	oscillated	stopped	stopped
Peripheral clock (low speed)	oscillated	oscillated	oscillated	oscillated	oscillated	oscillated
HLT, HLTH, DHLT bits of SBYCON register	low fix	low fix	low fix	Writable	Writable	Writable
WDT	valid	valid	valid	valid	valid	valid/invalid selectable
Return time from interrupt	4cycle (sysclk)	4cycle (sysclk)	4cycle (sysclk)	8cycle (sysclk)	about 200us	about 800us
Return clock when using PLL	PLL	PLL	PLL	PLL	XT32k	XT32k
Return clock when using CR16m	CR16m	CR16m	CR16m	CR16m	CR16m	CR16m

Appendixes

Appendix A Registers

Contents of Registers

Address	Name	Symbol	R/W	Size	Initial value
0x4000_0400	Flash-ROM status register	FLCSTA	R	32	0x0000_0000
0x4000_0404	Flash-ROM acceptor register	FLCACP	W	32	0x0000_0000
0x4000_0408	Flash-ROM address register	FLCADR	R/W	32	0x1000_0000
0x4000_040C	Flash-ROM write data register	FLCWDA	W	32	0x0000_0000
0x4000_0410	Flash-ROM erase register	FLCERA	R/W	32	0x0000_0000
0x4000_0420	Flash-ROM size register	FLCRSIZ	R	32	0x0001_0800 (Q464) 0x0002_0800 (Q466)
0x4000_0424	Boot program address register	FLCBADR	R	32	0x0000_F000 (Q464) 0x0001_F000 (Q466)
0x4000_1000	Interrupt Request Register	AESIREQ	R/W	32	0x0000_0000
0x4000_1004	Interrupt Mask Register	AESIMSK	R/W	32	0x0000_0003
0x4000_1008	Starting Number Register	AESSTRT	R/W	32	0x0000_0000
0x4000_100C	Status Register	AESSTAT	R	32	0x0000_0001
0x4000_1010	Control Register	AESCTRL	R/W	32	0x0000_0000
0x4000_1014	Initialization Vector & Counter Register 0	AESIVC0	R/W	32	0x0000_0000
0x4000_1018	Initialization Vector & Counter Register 1	AESIVC1	R/W	32	0x0000_0000
0x4000_101C	Initialization Vector & Counter Register 2	AESIVC2	R/W	32	0x0000_0000
0x4000_1020	Initialization Vector & Counter Register 3	AESIVC3	R/W	32	0x0000_0000
0x4000_1024	Before Processing Data Register 0	AESBFT0	R/W	32	0x0000_0000
0x4000_1028	Before Processing Data Register 1	AESBFT1	R/W	32	0x0000_0000
0x4000_102C	Before Processing Data Register 2	AESBFT2	R/W	32	0x0000_0000
0x4000_1030	Before Processing Data Register 3	AESBFT3	R/W	32	0x0000_0000
0x4000_1034	After Processing Data Register 0	AESAFT0	R	32	0x0000_0000
0x4000_1038	After Processing Data Register 1	AESAFT1	R	32	0x0000_0000
0x4000_103C	After Processing Data Register 2	AESAFT2	R	32	0x0000_0000
0x4000_1040	After Processing Data Register 3	AESAFT3	R	32	0x0000_0000
0x4000_1044	Encryption Key Register 0	AESEKY0	W	32	0x0000_0000
0x4000_1048	Encryption Key Register 1	AESEKY1	W	32	0x0000_0000
0x4000_104C	Encryption Key Register 2	AESEKY2	W	32	0x0000_0000
0x4000_1050	Encryption Key Register 3	AESEKY3	W	32	0x0000_0000
0x4000_1054	Encryption Key Register 4	AESEKY4	W	32	0x0000_0000
0x4000_1058	Encryption Key Register 5	AESEKY5	W	32	0x0000_0000
0x4000_105C	Encryption Key Register 6	AESEKY6	W	32	0x0000_0000
0x4000_1060	Encryption Key Register 7	AESEKY7	W	32	0x0000_0000
0x4000_1800	Random number generation register	RNDDT	R	32	Undefined
0x4000_1804	Random number generation enable register	RNDEN	R/W	32	0x0000_0000
0x4100_0000	Serial port 0 transmit/receive buffer	SIO0BUF	R/W	32	0x0000_0000
0x4100_0004	Serial port 0 control register	SIO0CON	R/W	32	0x0000_0000
0x4100_0008	Serial port 0 mode register	SIO0MOD	R/W	32	0x0000_0000
0x4100_0800	SIOF0 control register	SF0CTRL	R/W	32	0x0000_0000

Address	Name	Symbol	R/W	Size	Initial value
0x4100_0804	SIOF0 interrupt control register	SF0INTC	R/W	32	0x0000_0000
0x4100_0808	SIOF0 transfer interval control register	SF0TRAC	R/W	32	0x0000_0002
0x4100_080C	SIOF0 baud rate register	SF0BRR	R/W	32	0x0000_5002
0x4100_0810	SIOF0 status register	SF0SRR	R	32	0x0000_1400
0x4100_0814	SIOF0 status clear register	SF0SRC	W	32	0x0000_0000
0x4100_0818	SIOF0 FIFO status register	SF0FSR	R	32	0x0000_0000
0x4100_081C	SIOF0 write data register	SF0DWR	R/W	32	0x0000_0000
0x4100_0820	SIOF0 read data register	SF0DRR	R	32	0x0000_0000
0x4100_1000	UART0 receive buffer	UA0BUF	R	32	0x0000_0000
0x4100_1004	UART0 control register	UA0CON	R/W	32	0x0000_0000
0x4100_1008	UART0 mode register	UA0MOD	R/W	32	0x0000_0000
0x4100_100C	UART0 baud rate register	UA0BRT	R/W	32	0x0000_3FFF
0x4100_1010	UART0 receive status register	UA0STAT	R/W	32	0x0000_0000
0x4100_1020	UART0 transmit buffer	UA1BUF	R/W	32	0x0000_0000
0x4100_1024	UART0 transmit monitor register	UA1CON	R	32	0x0000_0000
0x4100_1030	UART0 transmit status register	UA1STAT	R/W	32	0x0000_0000
0x4100_1038	UART0 interrupt status register	UA0INTST	R/W	32	0x0000_0000
0x4100_1800	UARTF0 transmit/receive buffer	UAF0BUF	R/W	32	0x0000_00xx
0x4100_1804	UARTF0 interrupt enable register	UAF0IER	R/W	32	0x0000_0000
0x4100_1808	UARTF0 interrupt status register	UAF0IIR	R	32	0x0000_0001
0x4100_180C	UARTF0 mode register	UAF0MOD	R/W	32	0x0000_0000
0x4100_1810	UARTF0 line status register	UAF0LSR	R	32	0x0000_0160
0x4100_1814	UARTF0 clock adjustment register	UAF0CAJ	R/W	32	0x0000_000D
0x4100_2000	I2C bus 1 receive data register	I2C1RD	R	32	0x0000_0000
0x4100_2004	I2C bus 1 slave address register	I2C1SA	R/W	32	0x0000_0000
0x4100_2008	I2C bus 1 transmit data register	I2C1TD	R/W	32	0x0000_0000
0x4100_200C	I2C bus 1 control register	I2C1CON	R/W	32	0x0000_0000
0x4100_2010	I2C bus 1 mode register	I2C1MOD	R/W	32	0x0000_0000
0x4100_2014	I2C bus 1 status register	I2C1STA	R	32	0x0000_0000
0x4100_2800	I2CF0 slave address register	I2F0SAD	R/W	32	0x0000_0000
0x4100_2804	I2CF0 control register	I2F0CTL	R/W	32	0x0000_0000
0x4100_2808	I2CF0 status register	I2F0SR	R/W	32	0x0000_0000
0x4100_280C	I2CF0 data register	I2F0DR	R/W	32	0x0000_0000
0x4100_2810	I2CF0 bus monitor register	I2F0MON	R	32	0x0000_0003
0x4100_2814	I2CF0 bus transfer rate setup counter	I2F0BC	R/W	32	0x0000_0000
0x4100_2818	I2CF0 mode register	I2F0MOD	R/W	32	0x0000_0000
0x4100_281C	I2CF0 buffer mode slave address register	I2F0BSV	R/W	32	0x0000_0000
0x4100_2820	I2CF0 buffer mode sub address register	I2F0BSB	R/W	32	0x0000_0000
0x4100_2824	I2CF0 buffer mode format register	I2F0BFR	R/W	32	0x0000_0000
0x4100_2828	I2CF0 buffer mode control register	I2F0BCT	R/W	32	0x0000_0000
0x4100_282C	I2CF0 buffer mode interrupt mask register	I2F0BMK	R/W	32	0x0000_0000
0x4100_2830	I2CF0 buffer mode status register	I2F0BSR	R/W	32	0x0000_0000
0x4100_2834	I2CF0 buffer mode level register	I2F0BLV	R/W	32	0x0000_0000
0x4100_2848	I2CF0 timer register	I2F0TMR	R/W	32	0x0000_0000
0x4100_2850	I2CF0 input noise filter setting register	I2F0NF	R/W	32	0x0000_0001
0x4100_4000	bmRequestType setup register	BMREQUESTTYPE	R	32	0x0000_0000
0x4100_4004	bRequest setup register	BREQUEST	R	32	0x0000_0000
0x4100_4008	wValueLSB setup register	WVALUELSB	R	32	0x0000_0000

Address	Name	Symbol	R/W	Size	Initial value
0x4100_400C	wValueMSB setup register	WVALUEMSB	R	32	0x0000_0000
0x4100_4010	wIndexLSB setup register	WINDEXLSB	R	32	0x0000_0000
0x4100_4014	wIndexMSB setup register	WINDEXMSB	R	32	0x0000_0000
0x4100_4018	wLengthLSB setup register	WLENGTHLSB	R	32	0x0000_0000
0x4100_401C	wLengthMSB setup register	WLENGTHMSB	R	32	0x0000_0000
0x4100_4080	Device address register	DVCADR	R/W	32	0x0000_0000
0x4100_4084	Interrupt status register 1	INTSTAT1	R	32	0x0000_0000
0x4100_4088	Interrupt status register 2	INTSTAT2	R/W	32	0x0000_0000
0x4100_4090	Interrupt enable register 1	INTENBL1	R/W	32	0x0000_0001
0x4100_4094	Interrupt enable register 2	INTENBL2	R/W	32	0x0000_0000
0x4100_40B0	Isochronous mode select register	ISOMODESEL	R/W	32	0x0000_0000
0x4100_40B4	Frame number register LSB	FRAMELSB	R	32	0x0000_0000
0x4100_40B8	Frame number register MSB	FRAMEMSB	R	32	0x0000_0000
0x4100_40BC	System control register	SYSCON	R/W	32	0x0000_0000
0x4100_40C0	Polarity select register	POLSEL	R/W	32	0x0000_0000
0x4100_40E8	Oscillation test register	OSCTEST	R/W	32	0x0000_0000
0x4100_40FC	Transmit clock control register	TXCLKCONT	R/W	32	0x0000_0000
0x4100_4100	EP0 configuration register	EP0CONF	R	32	0x0000_0000
0x4100_4104	EP1 configuration register	EP1CONF	R/W	32	0x0000_0000
0x4100_4108	EP2 configuration register	EP2CONF	R/W	32	0x0000_0000
0x4100_410C	EP3 configuration register	EP3CONF	R/W	32	0x0000_0000
0x4100_4110	EP4 configuration register	EP4CONF	R/W	32	0x0000_0000
0x4100_4114	EP5 configuration register	EP5CONF	R/W	32	0x0000_0000
0x4100_4120	EP0 control register	EP0CONT	R/W	32	Undefined
0x4100_4124	EP1 control register	EP1CONT	R/W	32	0x0000_0000
0x4100_4128	EP2 control register	EP2CONT	R/W	32	0x0000_0000
0x4100_412C	EP3 control register	EP3CONT	R/W	32	0x0000_0000
0x4100_4130	EP4 control register	EP4CONT	R/W	32	0x0000_0000
0x4100_4134	EP5 control register	EP5CONT	R/W	32	0x0000_0000
0x4100_4140	EP0 payload register	EP0PLD	R/W	32	0x0000_0020
0x4100_4144	EP1 payload register	EP1PLD	R/W	32	0x0000_0000
0x4100_4148	EP2 payload register	EP2PLD	R/W	32	0x0000_0000
0x4100_414C	EP3 payload register	EP3PLD	R/W	32	0x0000_0000
0x4100_4150	EP4 payload register	EP4PLD	R/W	32	0x0000_0000
0x4100_4154	EP5 payload register	EP5PLD	R/W	32	0x0000_0000
0x4100_4160	EP0 receive byte counter	EP0RXCNT	R	32	0x0000_0000
0x4100_4164	EP1 receive byte counter	EP1RXCNT	R	32	0x0000_0000
0x4100_4168	EP2 receive byte counter	EP2RXCNT	R	32	0x0000_0000
0x4100_416C	EP3 receive byte counter	EP3RXCNT	R	32	0x0000_0000
0x4100_4170	EP4 receive byte counter	EP4RXCNT	R	32	0x0000_0000
0x4100_4174	EP5 receive byte counter	EP5RXCNT	R	32	0x0000_0000
0x4100_4180	EP0 status register	EP0STAT	R/W	32	0x0000_0000
0x4100_4184	EP1 status register	EP1STAT	R/W	32	0x0000_0000
0x4100_4188	EP2 status register	EP2STAT	R/W	32	0x0000_0000
0x4100_418C	EP3 status register	EP3STAT	R/W	32	0x0000_0000
0x4100_4190	EP4 status register	EP4STAT	R/W	32	0x0000_0000
0x4100_4194	EP5 status register	EP5STAT	R/W	32	0x0000_0000
0x4100_41C0	EP0 transmit FIFO	EP0TXFIFO	W	32	Undefined
0x4100_41E0	EP0 receive FIFO	EP0RXFIFO	R	32	Undefined

Address	Name	Symbol	R/W	Size	Initial value
0x4100_41E4	EP1 transmit/receive FIFO	EP1FIFO	R or W	32	Undefined
0x4100_41E8	EP2 transmit/receive FIFO	EP2FIFO	R or W	32	Undefined
0x4100_41EC	EP3 transmit/receive FIFO	EP3FIFO	R or W	32	Undefined
0x4100_41F0	EP4 transmit/receive FIFO	EP4FIFO	R or W	32	Undefined
0x4100_41F4	EP5 transmit/receive FIFO	EP5FIFO	R or W	32	Undefined
0x4200_0000	RC-ADC counter A register	RADCA	R/W	32	0x0000_0000
0x4200_0004	RC-ADC counter B register	RADCB	R/W	32	0x0000_0000
0x4200_0008	RC-ADC mode register	RADMOD	R/W	32	0x0000_0000
0x4200_000C	RC-ADC control register	RADCON	R/W	32	0x0000_0000
0x4200_0010	RC-ADC trigger register	RADTRG	R/W	32	0x0000_0000
0x4200_0020	RC-ADC continuous measurement 0 register	RADCM0	R/W	32	0x0000_0000
0x4200_0024	RC-ADC continuous measurement 1 register	RADCM1	R/W	32	0x0000_0000
0x4200_0028	RC-ADC continuous measurement 2 register	RADCM2	R/W	32	0x0000_0000
0x4200_002C	RC-ADC continuous measurement 3 register	RADCM3	R/W	32	0x0000_0000
0x4200_0030	RC-ADC continuous measurement 4 register	RADCM4	R/W	32	0x0000_0000
0x4200_0040	RC-ADC result counter register	RADRC	R/W	32	0x0000_0000
0x4200_1000	SA-ADC result register 0	SADR0	R	32	0x0000_0000
0x4200_1004	SA-ADC result register 1	SADR1	R	32	0x0000_0000
0x4200_1008	SA-ADC result register 2	SADR2	R	32	0x0000_0000
0x4200_100C	SA-ADC result register 3	SADR3	R	32	0x0000_0000
0x4200_1010	SA-ADC result register 4	SADR4	R	32	0x0000_0000
0x4200_1014	SA-ADC result register 5	SADR5	R	32	0x0000_0000
0x4200_1018	SA-ADC result register 6	SADR6	R	32	0x0000_0000
0x4200_101C	SA-ADC result register 7	SADR7	R	32	0x0000_0000
0x4200_1020	SA-ADC result register 8	SADR8	R	32	0x0000_0000
0x4200_1024	SA-ADC result register 9	SADR9	R	32	0x0000_0000
0x4200_1028	SA-ADC result register A	SADRA	R	32	0x0000_0000
0x4200_102C	SA-ADC result register B	SADRB	R	32	0x0000_0000
0x4200_1040	SA-ADC control register 0	SADCON0	R/W	32	0x0000_0002
0x4200_1044	SA-ADC control register 1	SADCON1	R/W	32	0x0000_0000
0x4200_1048	SA-ADC enable register	SADEN	R/W	32	0x0000_0000
0x4200_104C	SA-ADC touch sensor register	SADTCH	R/W	32	0x0000_0000
0x4200_1050	SA-ADC trigger register	SADTRG	R/W	32	0x0000_0000
0x4200_1054	SA-ADC accuracy control register	SADCVT	R/W	32	0x0000_FFFF
0x4200_1060	SA-ADC result register	SADR	R	32	0x000F_0000
0x4300_0000	Bias circuit control register	BIASCON	R/W	32	0x0000_0008
0x4300_0004	Display contrast register	DSPCNT	R/W	32	0x0000_0000
0x4300_0008	Display mode register	DSPMOD	R/W	32	0x0000_0000
0x4300_000C	Display control register	DSPCON	R/W	32	0x0000_0000
0x4300_0100 to 0x4300_0131	Display register 00 to Display register 31	DSPR00W to DSPR31W	R/W	8/16/32	Undefined
0x4300_0800 to 0x4300_0FFC	Display register 000 to Display register	DS0C0 to DS49C7	R/W	32	Undefined
0x4700_0000	DMA mode register	DMAMOD	R/W	32	0x0000_0000
0x4700_0004	DMA status register	DMASTA	R	32	0x0000_0000
0x4700_0008	DMA end status register	DMAINT	R	32	0x0000_0000
0x4700_0100	DMA channel mask register	DMACMSK0	R/W	32	0x0000_0001

Address	Name	Symbol	R/W	Size	Initial value
0x4700_0104	DMA transfer mode register	DMACTMOD0	R/W	32	0x0000_0040
0x4700_0108	DMA transfer source address register	DMACSAD0	R/W	32	0x0000_0000
0x4700_010C	DMA transfer destination address register	DMACDAD0	R/W	32	0x0000_0000
0x4700_0110	DMA transfer count register	DMACSIZ0	R/W	32	0x0000_0000
0x4700_0114	DMA end status clear register	DMACCINT0	W	32	0x0000_0000
0x4700_0200	DMA channel mask register	DMACMSK1	R/W	32	0x0000_0001
0x4700_0204	DMA transfer mode register	DMACTMOD1	R/W	32	0x0000_0040
0x4700_0208	DMA transfer source address register	DMACSAD1	R/W	32	0x0000_0000
0x4700_020C	DMA transfer destination address register	DMACDAD1	R/W	32	0x0000_0000
0x4700_0210	DMA transfer count register	DMACSIZ1	R/W	32	0x0000_0000
0x4700_0214	DMA end status clear register	DMACCINT1	W	32	0x0000_0000
0x5C00_0000	Revision register	IDR	R	32	0x0630_46x0
0x5C00_0004	DMA request select register	DREQSEL	R/W	32	0x0000_0000
0x5C00_0008	BRMP control register	BRMPCON	R/W	32	0x0000_0001
0x5C00_0010	Remapping control register	REMAPCON	R/W	32	0x0000_0000
0x5C00_0014	Remapping base address register	REMAPBASE	R/W	32	0x100x_F000
0x5C00_0044	Standby control register	SBYCON	R/W	32	0x0000_0000
0x5C00_0048	Power management control register	PMCON	R/W	32	0x0000_0000
0x5C00_004C	Clock control register	CLKCON	R/W	32	0x0000_0000
0x5C00_0050	Reset control register	RSTCON	R/W	32	0xFFFF_EFFF
0x5C00_0100	External interrupt enable register	EXIEN	R/W	32	0x0000_0000
0x5C00_0104	External Interrupt status register	EXIST	R/W	32	0x0000_0000
0x5C00_0108	External interrupt control register	EXICON	R/W	32	0x0000_0000
0x5C00_010C	External interrupt 03 selection register	EXI03SEL	R/W	32	0x0000_0000
0x5C00_0110	External interrupt 47 selection register	EXI47SEL	R/W	32	0x0000_0000
0x5C00_0200	Reset status register	RSTAT	R/W	32	Undefined
0x5C00_0204	LOCKUP reset setting register	LOCKUPEN	R/W	32	0x0000_0001
0x5C00_0300	Frequency control register 01	FCON01	R/W	32	0x0000_0313
0x5C00_0304	Frequency control register 23	FCON23	R/W	32	0x0000_0002
0x5C00_0308	Frequency status register	FSTAT	R	32	0x0000_0004
0x5C00_1000	Timer 0 data register	TM0D	R/W	32	0x0000_00FF
0x5C00_1004	Timer 0 counter register	TM0C	R/W	32	0x0000_0000
0x5C00_1008	Timer 0 control register	TM0CON	R/W	32	0x0000_0000
0x5C00_1010	Timer 1 data register	TM1D	R/W	32	0x0000_00FF
0x5C00_1014	Timer 1 counter register	TM1C	R/W	32	0x0000_0000
0x5C00_1018	Timer 1 control register	TM1CON	R/W	32	0x0000_0000
0x5C00_1020	Timer 2 data register	TM2D	R/W	32	0x0000_00FF
0x5C00_1024	Timer 2 counter register	TM2C	R/W	32	0x0000_0000
0x5C00_1028	Timer 2 control register	TM2CON	R/W	32	0x0000_0000
0x5C00_1030	Timer 3 data register	TM3D	R/W	32	0x0000_00FF
0x5C00_1034	Timer 3 counter register	TM3C	R/W	32	0x0000_0000
0x5C00_1038	Timer 3 control register	TM3CON	R/W	32	0x0000_0000
0x5C00_1040	Timer 4 data register	TM4D	R/W	32	0x0000_00FF
0x5C00_1044	Timer 4 counter register	TM4C	R/W	32	0x0000_0000
0x5C00_1048	Timer 4 control register	TM4CON	R/W	32	0x0000_0000
0x5C00_1050	Timer 5 data register	TM5D	R/W	32	0x0000_00FF
0x5C00_1054	Timer 5 counter register	TM5C	R/W	32	0x0000_0000
0x5C00_1058	Timer 5 control register	TM5CON	R/W	32	0x0000_0000
0x5C00_1060	Timer 6 data register	TM6D	R/W	32	0x0000_00FF

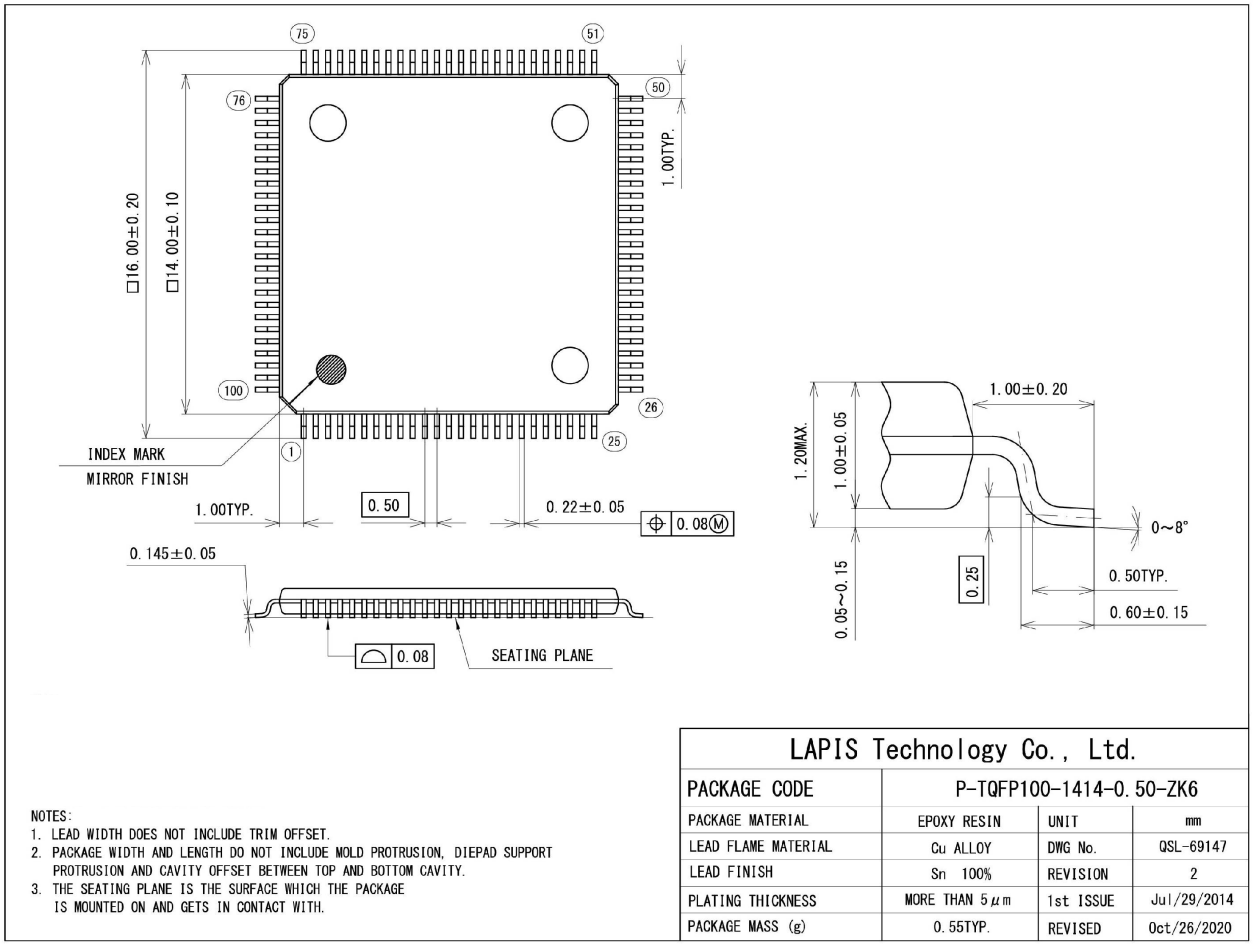
Address	Name	Symbol	R/W	Size	Initial value
0x5C00_1064	Timer 6 counter register	TM6C	R/W	32	0x0000_0000
0x5C00_1068	Timer 6 control register	TM6CON	R/W	32	0x0000_0000
0x5C00_1070	Timer 7 data register	TM7D	R/W	32	0x0000_00FF
0x5C00_1074	Timer 7 counter register	TM7C	R/W	32	0x0000_0000
0x5C00_1078	Timer 7 control register	TM7CON	R/W	32	0x0000_0000
0x5C00_10F0	Timer start register	TMSTR	W	32	0x0000_0000
0x5C00_10F4	Timer stop register	TMSTP	W	32	0x0000_0000
0x5C00_10F8	Timer status register	TMSTAT	R	32	0x0000_0000
0x5C00_2000	Watchdog timer control register	WDTCON	R/W	32	0x0000_0000
0x5C00_2004	Watchdog timer mode register	WDTMOD	R/W	32	0x0000_0082
0x5C00_2100	Low-speed time base counter register	LTBR	R/W	32	0x0000_0000
0x5C00_2104	Low-speed time base counter frequency adjustment register	LTBADJ	R/W	32	0x0000_0000
0x5C00_2108	Low-speed time base counter interrupt select resister	LTBINT	R/W	32	0x0000_0000
0x5C00_210C	Low-speed time base counter interrupt status register	LTBCINTST	R/W	32	0x0000_0000
0x5C00_2200	1 kHz timer count register	T1KCRL	R/W	32	0x0000_0000
0x5C00_2204	1 kHz timer control register	T1KCON	R/W	32	0x0000_0000
0x5C00_2300	Real time clock second register	RTCSEC	R/W	32	0x0000_0000
0x5C00_2304	Real time clock minute register	RTCMIN	R/W	32	0x0000_0000
0x5C00_2308	Real time clock hour register	RTCHOUR	R/W	32	0x0000_0000
0x5C00_230C	Real time clock week register	RTCWEEK	R/W	32	0x0000_0007
0x5C00_2310	Real time clock day register	RTCDAY	R/W	32	0x0000_0001
0x5C00_2314	Real time clock month register	RTCMON	R/W	32	0x0000_0001
0x5C00_2318	Real time clock year register	RTCYEAR	R/W	32	0x0000_0000
0x5C00_231C	Real time clock control register	RTCCON	R/W	32	0x0000_0000
0x5C00_2320	Real time clock alarm 0 minute register	AL0MIN	R/W	32	0x0000_0000
0x5C00_2324	Real time clock alarm 0 hour register	AL0HOUR	R/W	32	0x0000_0000
0x5C00_2328	Real time clock alarm 0 week register	AL0WEEK	R/W	32	0x0000_0000
0x5C00_232C	Real time clock alarm 1 minute register	AL1MIN	R/W	32	0x0000_0000
0x5C00_2330	Real time clock alarm 1 hour register	AL1HOUR	R/W	32	0x0000_0000
0x5C00_2334	Real time clock alarm 1 day register	AL1DAY	R/W	32	0x0000_0000
0x5C00_2338	Real time clock alarm 1 month register	AL1MON	R/W	32	0x0000_0000
0x5C00_2350	Real time clock hour/minute/second register	RTCHMS	R	32	0x0000_0000
0x5C00_2354	Real time clock year/month/day/week register	RTCYMDW	R	32	0x0001_0107
0x5C00_2360	Real time clock interrupt status register	RTCINTST	R/W	32	0x0000_0000
0x5C00_3000	FTM0 period register	FT0P	R/W	32	0x0000_FFFF
0x5C00_3004	FTM0 event register A	FT0EA	R/W	32	0x0000_0000
0x5C00_3008	FTM0 event register B	FT0EB	R/W	32	0x0000_0000
0x5C00_300C	FTM0 dead time register	FT0DT	R/W	32	0x0000_0000
0x5C00_3010	FTM0 counter register	FT0C	R/W	32	0x0000_0000
0x5C00_3014	FTM0 control register 0	FT0CON0	R/W	32	0x0000_0000
0x5C00_3018	FTM0 control register 1	FT0CON1	R/W	32	0x0000_0000
0x5C00_301C	FTM0 mode register	FT0MOD	R/W	32	0x0000_0000
0x5C00_3020	FTM0 clock register	FT0CLK	R/W	32	0x0000_0000
0x5C00_3024	FTM0 trigger register	FT0TRG	R/W	32	0x0000_0000
0x5C00_3030	FTM0 interrupt enable register	FT0INTE	R/W	32	0x0000_0000
0x5C00_3034	FTM0 interrupt status register	FT0INTS	R	32	0x0000_0000
0x5C00_3038	FTM0 interrupt clear register	FT0INTC	W	32	0x0000_0000

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_3100	FTM1 period register	FT1P	R/W	32	0x0000_FFFF
0x5C00_3104	FTM1 event register A	FT1EA	R/W	32	0x0000_0000
0x5C00_3108	FTM1 event register B	FT1EB	R/W	32	0x0000_0000
0x5C00_310C	FTM1 dead time register	FT1DT	R/W	32	0x0000_0000
0x5C00_3110	FTM1 counter register	FT1C	R/W	32	0x0000_0000
0x5C00_3114	FTM1 control register 0	FT1CON0	R/W	32	0x0000_0000
0x5C00_3118	FTM1 control register 1	FT1CON1	R/W	32	0x0000_0000
0x5C00_311C	FTM1 mode register	FT1MOD	R/W	32	0x0000_0000
0x5C00_3120	FTM1 clock register	FT1CLK	R/W	32	0x0000_0000
0x5C00_3124	FTM1 trigger register	FT1TRG	R/W	32	0x0000_0000
0x5C00_3130	FTM1 interrupt enable register	FT1INTE	R/W	32	0x0000_0000
0x5C00_3134	FTM1 interrupt status register	FT1INTS	R	32	0x0000_0000
0x5C00_3138	FTM1 interrupt clear register	FT1INTC	W	32	0x0000_0000
0x5C00_3200	FTM2 period register	FT2P	R/W	32	0x0000_FFFF
0x5C00_3204	FTM2 event register A	FT2EA	R/W	32	0x0000_0000
0x5C00_3208	FTM2 event register B	FT2EB	R/W	32	0x0000_0000
0x5C00_320C	FTM2 dead time register	FT2DT	R/W	32	0x0000_0000
0x5C00_3210	FTM2 counter register	FT2C	R/W	32	0x0000_0000
0x5C00_3214	FTM2 control register 0	FT2CON0	R/W	32	0x0000_0000
0x5C00_3218	FTM2 control register 1	FT2CON1	R/W	32	0x0000_0000
0x5C00_321C	FTM2 mode register	FT2MOD	R/W	32	0x0000_0000
0x5C00_3220	FTM2 clock register	FT2CLK	R/W	32	0x0000_0000
0x5C00_3224	FTM2 trigger register	FT2TRG	R/W	32	0x0000_0000
0x5C00_3230	FTM2 interrupt enable register	FT2INTE	R/W	32	0x0000_0000
0x5C00_3234	FTM2 interrupt status register	FT2INTS	R	32	0x0000_0000
0x5C00_3238	FTM2 interrupt clear register	FT2INTC	W	32	0x0000_0000
0x5C00_3300	FTM3 period register	FT3P	R/W	32	0x0000_FFFF
0x5C00_3304	FTM3 event register A	FT3EA	R/W	32	0x0000_0000
0x5C00_3308	FTM3 event register B	FT3EB	R/W	32	0x0000_0000
0x5C00_330C	FTM3 dead time register	FT3DT	R/W	32	0x0000_0000
0x5C00_3310	FTM3 counter register	FT3C	R/W	32	0x0000_0000
0x5C00_3314	FTM3 control register 0	FT3CON0	R/W	32	0x0000_0000
0x5C00_3318	FTM3 control register 1	FT3CON1	R/W	32	0x0000_0000
0x5C00_331C	FTM3 mode register	FT3MOD	R/W	32	0x0000_0000
0x5C00_3320	FTM3 clock register	FT3CLK	R/W	32	0x0000_0000
0x5C00_3324	FTM3 trigger register	FT3TRG	R/W	32	0x0000_0000
0x5C00_3330	FTM3 interrupt enable register	FT3INTE	R/W	32	0x0000_0000
0x5C00_3334	FTM3 interrupt status register	FT3INTS	R	32	0x0000_0000
0x5C00_3338	FTM3 interrupt clear register	FT3INTC	W	32	0x0000_0000
0x5C00_3F00	FTM output select register 0	FTOSL0	R/W	32	0x0000_0000
0x5C00_3F04	FTM output select register 4	FTOSL4	R/W	32	0x0000_0000
0x5C00_3F08	FTM output select register 8	FTOSL8	R/W	32	0x0000_0000
0x5C00_3F0C	FTM output select register C	FTOSLC	R/W	32	0x0000_0000
0x5C00_4000	Port 0 data register	P0D	R/W	32	0x0000_0000
0x5C00_4004	Port 0 direction register	P0DIR	R/W	32	0x0000_0000
0x5C00_4008	Port 0 control register	P0CON	R/W	32	0x0000_0000
0x5C00_400C	Port 0 mode register	P0MOD	R/W	32	0x0000_0000
0x5C00_4200	Port 2 data register	P2D	R/W	32	0x0000_0000
0x5C00_4204	Port 2 direction register	P2DIR	R/W	32	0x0000_0000

Address	Name	Symbol	R/W	Size	Initial value
0x5C00_4208	Port 2 control register	P2CON	R/W	32	0x0000_0000
0x5C00_420C	Port 2 mode register	P2MOD	R/W	32	0x0000_0000
0x5C00_4300	Port 3 data register	P3D	R/W	32	0x0000_0000
0x5C00_4304	Port 3 direction register	P3DIR	R/W	32	0x0000_0000
0x5C00_4308	Port 3 control register	P3CON	R/W	32	0x0000_0000
0x5C00_430C	Port 3 mode register	P3MOD	R/W	32	0x0000_0000
0x5C00_4400	Port 4 data register	P4D	R/W	32	0x0000_0000
0x5C00_4404	Port 4 direction register	P4DIR	R/W	32	0x0000_0000
0x5C00_4408	Port 4 control register	P4CON	R/W	32	0x0000_0000
0x5C00_440C	Port 4 mode register	P4MOD	R/W	32	0x0000_0000
0x5C00_4500	Port 5 data register	P5D	R/W	32	0x0000_0000
0x5C00_4504	Port 5 direction register	P5DIR	R/W	32	0x0000_0000
0x5C00_4508	Port 5 control register	P5CON	R/W	32	0x0000_0000
0x5C00_450C	Port 5 mode register	P5MOD	R/W	32	0x0000_0000
0x5C00_4600	Port 6 data register	P6D	R/W	32	0x0000_0000
0x5C00_4604	Port 6 direction register	P6DIR	R/W	32	0x0000_0000
0x5C00_4608	Port 6 control register	P6CON	R/W	32	0x0000_0000
0x5C00_460C	Port 6 mode register	P6MOD	R/W	32	0x0000_0000
0x5C00_5000	Voltage level supervisor control register	VLSCON	R/W	32	0x0000_0000
0x5C00_5004	Voltage level supervisor mode register	VLSMOD	R/W	32	0x0000_0000
0x5C00_5100	Comparator 0 control register	CMP0CON	R/W	32	0x0000_0000
0x5C00_5104	Comparator 0 mode register	CMP0MOD	R/W	32	0x0000_0000
0x5C00_5180	Comparator 1 control register	CMP1CON	R/W	32	0x0000_0000
0x5C00_5184	Comparator 1 mode register	CMP1MOD	R/W	32	0x0000_0000
0x5C00_51A0	Comparator interrupt status register	CMPINTST	R/W	32	0x0000_0000
0xE000_E100	Interrupt set-enable register	NVIC_ISER	R/W	32	0x0000_0000
0xE000_E180	Interrupt clear-enable register	NVIC_ICER	R/W	32	0x0000_0000
0xE000_E200	Interrupt set-pending register	NVIC_ISPR	R/W	32	0x0000_0000
0xE000_E280	Interrupt clear-pending register	NVIC_ICPR	R/W	32	0x0000_0000
0xE000_E400	Interrupt priority register 0	NVIC_IPR0	R/W	32	0x0000_0000
0xE000_E404	Interrupt priority register 1	NVIC_IPR1	R/W	32	0x0000_0000
0xE000_E408	Interrupt priority register 2	NVIC_IPR2	R/W	32	0x0000_0000
0xE000_E40C	Interrupt priority register 3	NVIC_IPR3	R/W	32	0x0000_0000
0xE000_E410	Interrupt priority register 4	NVIC_IPR4	R/W	32	0x0000_0000
0xE000_E414	Interrupt priority register 5	NVIC_IPR5	R/W	32	0x0000_0000
0xE000_E418	Interrupt priority register 6	NVIC_IPR6	R/W	32	0x0000_0000
0xE000_E41C	Interrupt priority register 7	NVIC_IPR7	R/W	32	0x0000_0000
0xE000_ED00	CPUID register	CPUID	R	32	0x410C_C200
0xE000_ED04	Interrupt control and state register	ICSR	R/W	32	0x0000_0000
0xE000_ED0C	Application interrupt and reset control register	AIRCR	R/W	32	0xFA05_0000
0xE000_ED10	System control register	SCR	R/W	32	0x0000_0000
0xE000_ED14	Configuration and control register	CCR	R	32	0x0000_0208
0xE000_ED1C	System handler priority register 2	SHPR2	R/W	32	0x0000_0000
0xE000_ED20	System handler priority register 3	SHPR3	R/W	32	0x0000_0000

Appendix B Package Dimensions

● ML630Q464/Q466



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP100-1414-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69147
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.55TYP.	REVISED	Oct/26/2020

Figure B-1 TQFP100

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions(reflow method, temperature and times).

Appendix C Electrical Characteristics

● ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +4.6	V
Power supply voltage 2	V_{DDL}	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 3	V_{L1-3}	Ta=25°C	-0.3 to +6.0	V
Input voltage(P00-P05, P20-P23, P30-P35, SWC, SWD, BRMP, RESET_N, DP, DM)	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Input voltage (5 V tolerant) (P36, P37, P40-P47, P50-P57, P60-P63)	V_{INT}	Ta=25°C	-0.3 to +6.0	V
Output voltage 1	V_{OUT1}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage 2 (COM0 to COM7 SEG0 to SEG49)	V_{OUT2}	Ta=25°C	-0.3 to V_{L1-3}+0.3	V
Output current 1	I_{OUT1}	Port 0, 2 Ta=25°C	-12 to +11	mA
Output current 2	I_{OUT2}	Port 3 to 6 Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	–	-55 to +150	°C

● RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	–	-40 to +85	°C
Operating voltage	V_{DD}	–	1.8 to 3.6	V
Reference voltage	V_{REF}	–	1.8 to V_{DD}	V
Operating frequency (CPU)	f_{OP}	–	LSCLK:32.768k HSCLK:500k to 24M	Hz
Low speed crystal oscillation frequency	f_{XTL}	–	32.768k	Hz
Low speed crystal oscillation external capacitor 1	C_{DL}	Using VT-200-FL(from SII)	6.8 to 12	pF
	C_{GL}		6.8 to 12	
Low speed crystal oscillation external capacitor 2	C_{DL}	Using DT-26(from Daishinku)	12 to 16	pF
	C_{GL}		12 to 16	
Low speed crystal *1 oscillation external capacitor 3	C_{DL}	Using VT-200-F(from SII)	12 to 22	pF
	C_{GL}		12 to 22	
V_{DDL} external capacitor *2	C_L	ESR ≤ 500mΩ	2.2 ± 30%	μF
$V_{L1,2,3}$ pin external capacitor	$C_{a,b,c}$	–	1.0 ± 30%	μF
C_1-C_2 external capacitor	C_{12}	–	1.0 ± 30%	μF
C_{H1}, C_{H2} external capacitor	C_{H12}	–	1.0 ± 30%	μF
V_{HF} external capacitor	C_{VH}	–	1.0 ± 30%	μF

*1 : Please use this crystal except DEEPHALT mode because this LSI may not be functioning at DEEPHALT mode with the crystal. Please evaluate the matching when other crystal oscillator/ceramic oscillator is used.

*2 : Please evaluate on user's conditions, put on C_{L0}(= 0.1uF) if necessary.

See the application note; "Precautions for MCU board design" for details, when designing MCU board.

● Operating Conditions of Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature (Ambience)	T_{OP}	Data area : write/erase		-40 to +85	°C
		Program area : write/erase		0 to +40	°C
Operating voltage Write time	V_{DD}	Write/erase		1.8 to 3.6	V
	C_{EPD}	Data area (1,024B x 2)		10,000	times
	C_{EPP}	Program area		100	times
Erase unit	–	Block erase	Program area	8	KB
			Data area	2	
		Sector erase		1	
Erase time(Maximum)	–	Block erase/Sector erase		100	ms
Write unit	–	–		1 word (4 byte)	–

● AC characteristics (Oscillation)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Low speed crystal oscillation start time	T_{XTL}	–	–	–	2	s	1
Low speed built-in RC oscillation frequency*1*2*3	f_{LCR}	Ta=25°C	typ -1.5%	32.768	typ +1.5%	kHz	
		Ta=-40 to 85°C	typ -5%	32.768	typ +5%		
High speed build-in RC oscillation frequency*1*2	f_{HCR}	Ta=25°C	typ -1%	16	typ +1%	MHz	
		Ta=-40 to 85°C	typ -5%	16	typ +5%		
PLL frequency	f_{PLL}	f_{XTL}=32.768kHz	typ -0.25%	24	typ +0.25%	MHz	
Low speed crystal oscillation stop detection time	T_{STOP}	–	–	600	–	μs	

*1 : Mean value of 1024 cycle.
*2 : Guarantee value at the time of the shipment.
*3 : Except DeepHALT mode and Ultra-DeepHALT mode.

● DC Characteristics (IDD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating*1 Min.	Rating*1 Typ.	Rating*1 Max.	Unit	Measuring circuit
Power consumption 1	IDD1	Stop mode Low/High-speed oscillation is stopped	Ta=25°C	–	0.70	2.5	μA	1
			Ta=-40 to 85°C	–	–	28		
Power consumption 2	IDD2-1	ULTRA-DEEP-HALT mode *3*4 (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped. 2.5V≤V_{DD}	Ta=25°C	–	0.80	2.5	μA	
			Ta=-40 to 85°C	–	–	20		
	IDD2-2	DEEP-HALT mode *3*4 (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped.	Ta=25°C	–	1.30.	3.0	μA	
			Ta=-40 to 85°C	–	–	28		
Power consumption 3	IDD3	HALT mode *3*4 (LTBC function) Low-speed crystal oscillating (32.768kHz) High speed oscillation is stopped.	Ta=25°C	–	2.2	5.0	μA	
			Ta=-40 to 85°C	–	–	32		
Power consumption 4	IDD4	CPU Low-speed *2*4 Low-speed crystal oscillating High speed oscillation is stopped.	Ta=25°C	–	9.0	14	μA	
			Ta=-40 to 85°C	–	–	45		
Power consumption 5	IDD5	CPU High-speed(16MHz) *2*4 High-speed Built-in RC oscillating	Ta=25°C	–	3.8	5.0	mA	
			Ta=-40 to 85°C	–	–	5.5		
Power consumption 6	IDD6	CPU High-speed(24MHz) *2*4 High-speed PLL oscillating	Ta=25°C	–	6.0	7.0	mA	
			Ta=-40 to 85°C	–	–	7.5		

*1 : typ.rating is V_{DD}=3.0V
*2 : at CPU activity rate =100%(No HALT state)
*3 : using 32.768KHz crystal oscillator VT-200-FL (from SII)(C_{GL}/C_{DL}=12pF)
using 32.768KHz crystal oscillator DT-26(from Daishinku)(C_{GL}/C_{DL}=12pF)
*4 : CLKCON valid bits are "0", RSTCON valid bits are "1"

● DC Characteristics (VLS) (1/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS judge voltage (V_{DD}=fall)	V_{VLS}	VLSLV[5:0] = 00H*1	Typ. -3%	1.200	Typ. +3%	V	1
		VLSLV[5:0] = 01H*1		1.225			
		VLSLV[5:0] = 02H*1		1.250			
		VLSLV[5:0] = 03H*1		1.275			
		VLSLV[5:0] = 04H*1		1.300			
		VLSLV[5:0] = 05H*1		1.325			
		VLSLV[5:0] = 06H*1		1.350			
		VLSLV[5:0] = 07H*1		1.375			
		VLSLV[5:0] = 08H*1		1.400			
		VLSLV[5:0] = 09H*1		1.425			
		VLSLV[5:0] = 0AH*1		1.450			
		VLSLV[5:0] = 0BH*1		1.475			
		VLSLV[5:0] = 0CH*1		1.500			
		VLSLV[5:0] = 0DH*1		1.525			
		VLSLV[5:0] = 0EH*1		1.550			
		VLSLV[5:0] = 0FH*1		1.575			
		VLSLV[5:0] = 10H*1		1.600			
		VLSLV[5:0] = 11H*1		1.625			
		VLSLV[5:0] = 12H*1		1.650			
		VLSLV[5:0] = 13H*1		1.675			
		VLSLV[5:0] = 14H*1		1.700			
		VLSLV[5:0] = 15H*1		1.725			
		VLSLV[5:0] = 16H*1		1.750			
		VLSLV[5:0] = 17H*1		1.775			
		VLSLV[5:0] = 18H		1.800			
		VLSLV[5:0] = 19H		1.825			
		VLSLV[5:0] = 1AH		1.850			
		VLSLV[5:0] = 1BH		1.875			
		VLSLV[5:0] = 1CH		1.900			
		VLSLV[5:0] = 1DH		1.925			
		VLSLV[5:0] = 1EH		1.950			
		VLSLV[5:0] = 1FH		1.975			
		VLSLV[5:0] = 20H		2.000			
		VLSLV[5:0] = 21H		2.050			
		VLSLV[5:0] = 22H		2.100			
		VLSLV[5:0] = 23H		2.150			
		VLSLV[5:0] = 24H		2.200			
		VLSLV[5:0] = 25H		2.250			
		VLSLV[5:0] = 26H		2.300			
		VLSLV[5:0] = 27H		2.350			
		VLSLV[5:0] = 28H		2.400			
		VLSLV[5:0] = 29H		2.450			

● DC Characteristics (VLS) (2/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating[*1]			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS judge voltage (V_{DD}=fall)	V_{VLS}	VLSLV[5:0] = 2AH	Typ. -3%	2.500	Typ. +3%	V	1
		VLSLV[5:0] = 2BH		2.550			
		VLSLV[5:0] = 2CH		2.600			
		VLSLV[5:0] = 2DH		2.650			
		VLSLV[5:0] = 2EH		2.700			
		VLSLV[5:0] = 2FH		2.750			
		VLSLV[5:0] =30H		2.800			
		VLSLV[5:0] = 31H		2.850			
		VLSLV[5:0] = 32H		2.900			
		VLSLV[5:0] = 33H		2.950			
		VLSLV[5:0] = 34H		3.000			
		VLSLV[5:0] = 35H		3.050			
		VLSLV[5:0] = 36H		3.100			
		VLSLV[5:0] = 37H		3.150			
		VLSLV[5:0] = 38H		3.200			
		VLSLV[5:0] = 39H		3.250			
		VLSLV[5:0] = 3AH		3.300			
		VLSLV[5:0] = 3BH		3.350			
		VLSLV[5:0] = 3CH		3.400			
		VLSLV[5:0] = 3DH		3.450			
		VLSLV[5:0] = 3EH		3.500			
		VLSLV[5:0] = 3FH		3.550			
V_{VLS} Hysteresis width (V_{DD}=rise)	H_{VLS}	–	V_{VLS} x 1.0%	V_{VLS} x 2.7%	V_{VLS} x 4.5%	V	1

VLSLV[3:0] are bits of the VLSCON register to change detection voltage level.
[*1]: Setable only at the time of select to V_{VLSP} pin.

● DC characteristics (LLD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
LLD judge Voltage	VLLR	–	1.60	1.80	2.00	V	1

● DC/AC characteristics (Analog comparator)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common Input voltage range	V_{CMPIN}	–	0.2	–	V_{DD} -0.2	V	1
Input offset voltage	V_{CMPOF}	–	-30	–	30	mV	
Comparator judge time	T_{CMP}	CMPP- CMPM =40mV	–	–	2	μs	

● DC characteristics (LCD driver 1/2 V_{L1} based) (1/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD}=3.0V, Tj=25°C	LCN[4:0] = 00H*2	0.89	0.94	0.99	V	1
			LCN[4:0] = 01H*2	0.91	0.96	1.01		
			LCN[4:0] = 02H*2	0.93	0.98	1.03		
			LCN[4:0] = 03H*2	0.95	1.00	1.05		
			LCN[4:0] = 04H*2	0.97	1.02	1.07		
			LCN[4:0] = 05H*2	0.99	1.04	1.09		
			LCN[4:0] = 06H*2	1.01	1.06	1.11		
			LCN[4:0] = 07H*2	1.03	1.08	1.13		
			LCN[4:0] = 08H*2	1.05	1.10	1.15		
			LCN[4:0] = 09H*2	1.07	1.12	1.17		
			LCN[4:0] = 0AH*2	1.09	1.14	1.19		
			LCN[4:0] = 0BH*2	1.11	1.16	1.21		
			LCN[4:0] = 0CH*2	1.13	1.18	1.23		
			LCN[4:0] = 0DH*2	1.15	1.20	1.25		
			LCN[4:0] = 0EH*2	1.17	1.22	1.27		
			LCN[4:0] = 0FH*2	1.19	1.24	1.29		
			LCN[4:0] = 10H	1.21	1.26	1.31		
			LCN[4:0] = 11H	1.23	1.28	1.33		
			LCN[4:0] = 12H	1.25	1.30	1.35		
			LCN[4:0] = 13H	1.27	1.32	1.37		
			LCN[4:0] = 14H	1.29	1.34	1.39		
			LCN[4:0] = 15H	1.31	1.36	1.41		
			LCN[4:0] = 16H	1.33	1.38	1.43		
			LCN[4:0] = 17H	1.35	1.40	1.45		
			LCN[4:0] = 18H	1.37	1.42	1.47		
			LCN[4:0] = 19H	1.39	1.44	1.49		
			LCN[4:0] = 1AH	1.41	1.46	1.51		
			LCN[4:0] = 1BH	1.43	1.48	1.53		
			LCN[4:0] = 1CH	1.45	1.50	1.55		
			LCN[4:0] = 1DH	1.47	1.52	1.57		
			LCN[4:0] = 1EH	1.49	1.54	1.59		
			LCN[4:0] = 1FH	1.51	1.56	1.61		
V_{L1} temperature deviation*1	ΔV_{L1}	V_{DD}=3.0V		–	−0.06	–	%/°C	
V_{L1} voltage dependency*1	ΔV_{L1}	V_{DD}=1.8 to 3.6V		–	5	20	mV/V	
V_{L2} voltage	V_{L2}	V_{DD} = 3.0V, Tj = 25°C 1MΩ load (V_{L3}−VSS)		Typ. -10%	V_{L1}×2	Typ. +4%	V	
V_{L3} voltage	V_{L3}			Typ. -10%	V_{L1}×3	Typ. +4%		
LCD bias voltage generation time	T_{BIAS}	—		—	—	600	ms	

*1:V_{L1} can not exceed V_{DD} level. The maximum V_{L1} becomes V_{DD} level when the V_{L1} calculated by the temperature deviation and voltage dependency is going to exceed the V_{DD} level.
*2: 1/3 bias only.

● DC characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWD, PUCTL)	VOH1	IOH=-1.0mA	V_{DD} -0.5	–	–	V	2
	VOL1	IOL=+0.5mA	–	–	0.4		
Output voltage 2 (P34, P35, P40, P41) (LED mode is selected)	VOL2	2.7V ≤ V_{DD} ≤ 3.6V IOL=+5.0mA	–	–	0.6		
		IOL=+2.0mA	–	–	0.4		
Output voltage 3 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55,) (I^2C mode is selected)	VOL3	IOL3= +3mA (I^2Cspec) (V_{DD} ≥ 2V)	–	–	0.4		
Output voltage 4 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I^2C mode is selected)	VOL4	IOL4= +2mA(I^2Cspec) (V_{DD} < 2V)	–	–	V_{DD} ×0.2		
Output voltage 5 (COM0-7 SEG0-49) (LCD mode is selected)	VOH5	1/3bias, IOH5=-0.02mA, V_{L1}=1.2V	V_{L3} -0.2	—	—		
	VOM5	1/3bias, IOM5=+0.02mA, V_{L1}=1.2V	—	—	V_{L2} +0.2		
	VOM5S	1/3bias, IOM5S=-0.02mA, V_{L1}=1.2V	V_{L2} -0.2	—	—		
	VOML5	1/3bias, IOML5=+0.02mA, V_{L1}=1.2V	—	—	V_{L1} +0.2		
	VOML5S	1/3bias, IOML5S=-0.02mA, V_{L1}=1.2V	V_{L1} -0.2	—	—		
	VOL5	1/3bias, IOL5=+0.02mA, V_{L1}=1.2V	—	—	0.2		
Output voltage 5 (COM0-7 SEG0-49) (LCD mode is selected)	VOH5	1/2bias, IOH5=-0.01mA, V_{L1}=1.4V	V_{L3} -0.3	—	—		
	VOM5	1/2bias, IOM5=+0.01mA, V_{L1}=1.4V	—	—	V_{L2} +0.3		
	VOM5S	1/2bias, IOM5S=-0.01mA, V_{L1}=1.4V	V_{L2} -0.3	—	—		
	VOML5	1/2bias, IOML5=+0.01mA, V_{L1}=1.4V	—	—	V_{L1} +0.3		
	VOML5S	1/2bias, IOML5S=-0.01mA, V_{L1}=1.4V	V_{L1} -0.3	—	—		
	VOL5	1/2bias, IOL5=+0.01mA, V_{L1}=1.4V	—	—	0.3		

Output leak 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWD,PUCTL)	IOOH1	VOH=V_{DD} (at high impedance)	–	–	+1	μA	3
	IOOL1	VOL=V_{SS} (at high impedance)	-1	–	–		

● DC characteristics (IIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating*1			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	–	–	1	μA	4
	IIL1	VIL1=V_{SS}	-900	-300	-20		
Input current 3 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63, SWC, SWD, BRMP)	IIH3	VIH3=V_{DD} (at pull down)	1	15	200		
	IIL3	VIL3=V_{SS} (at pull up)	-200	-15	-1		
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1		
	IIL3Z	VIL3=V_{SS} (at high impedance)	-1	–	–		
Input current 4 (P36, P37, P40-P47, P50-P57, P60-P63)	IIH4Z	VIH4=5.0V (at high impedance)	–	–	1		

*1 : typ.rating is Ta=25°C , V_{DD}=3.0V

● DC characteristics (VIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N, SWD, SWC, BRMP, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63)	VIH1	–	0.7 ×V_{DD}	–	V_{DD}	V	5
	VIL1	–	0	–	0.3 ×V_{DD}		
Input terminal capacitance (RESET_N, SWD, SWC, BRMP, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P63)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	–	–	10	pF	–

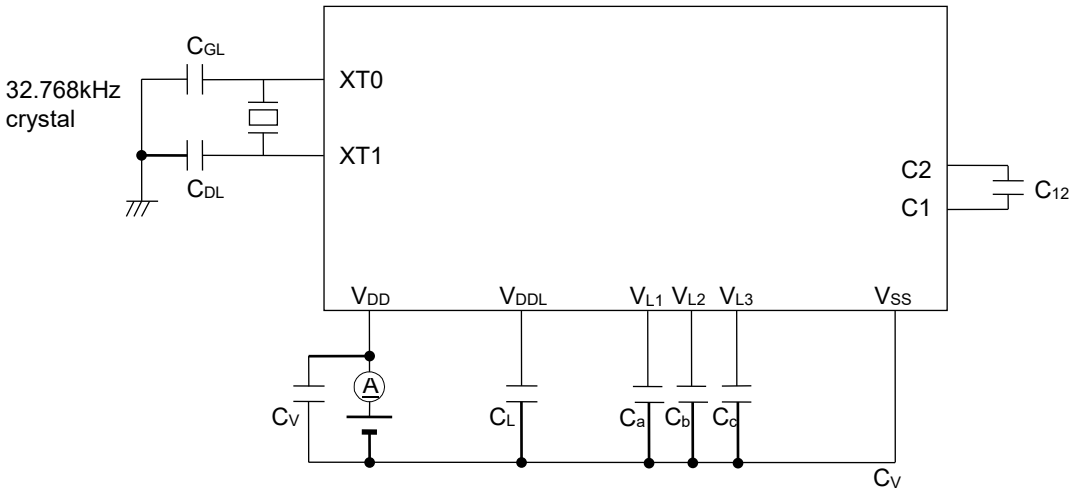
● DC characteristics (USB)

(V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating*1			Unit	Measuring circuit
			Min.	Typ.	Max.		
Differential input sensitivity	V_{DI}	Absolute value of the difference between the DP and DM pins	0.2	-	-	V	–
Differential common mode range	V_{CM}	Includes VDI range	0.8	-	2.5	V	
Single end input threshold voltage	V_{SE}	-	0.8	-	2.0	V	
High level output voltage	V_{OH}	15k W RL is connected to GND	2.8	-	-	V	
Low level output voltage	V_{OL}	1.5k W RL to 3.6 V	-	-	0.3	V	
Hi-Z state input/output leakage current	I_{LO}	0 V < VIN < 3.3 V	-10		10	uA	
Driver output resistance	Z_{DRV}	Steady state	28		44	Ω	

● MEASURING CIRCUITS

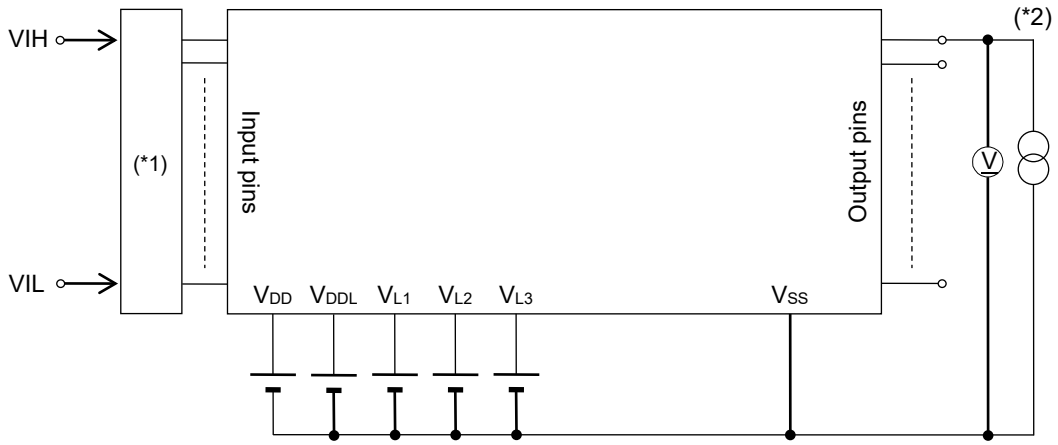
MEASURING CIRCUIT1



C_V	: 1μF
C_L	: 2.2μF
C_a,C_b,C_c	: 1μF
C_{12}	: 1μF
C_{GL}	: 12pF
C_{DL}	:12pF

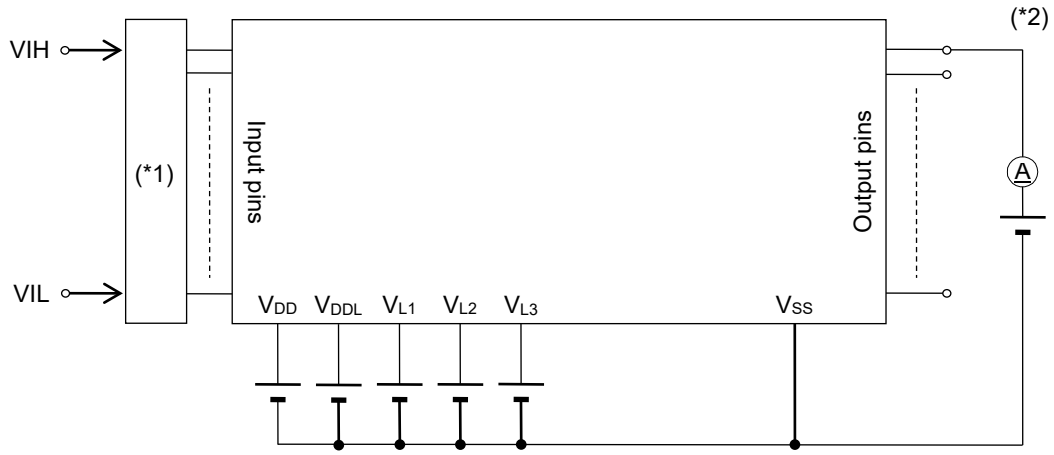
32.768kHz crystal oscilation:
(DT-26 from Daishinku)

MEASURING CIRCUIT 2



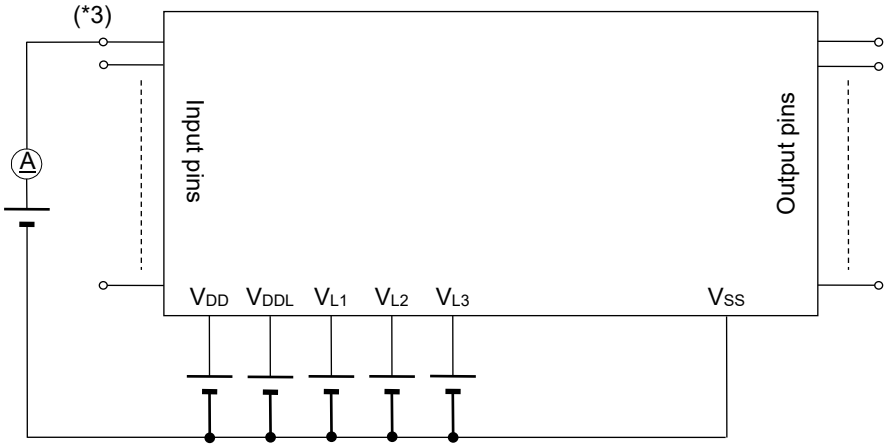
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



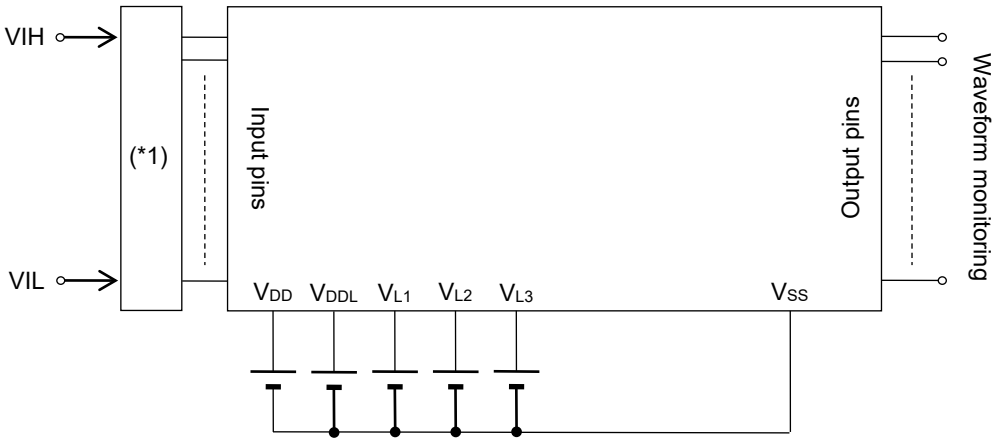
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5



*1: Input logic circuit to determine the specified measuring conditions.

● AC characteristics (USB)

(V_{DD}=3.0 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Applied pin
			Min.	Typ.	Max.		
Rise time (*1)	T_R	C_L = 50 pF	4	-	20	ns	DP,DM
Fall time (*1)	T_F	C_L = 50 pF	4	-	20	ns	
Output signal crossover voltage	V_{CRS}	C_L = 50 pF	0.8	-	2.5	V	
Data rate	T_{DRATE}	Average bit rate (12Mbps ±0.25%)	11.97	-	12.03	Mbps	

* 1: T_R and T_F: Rise time and fall time between 10% and 90% of the pulse amplitude, respectively

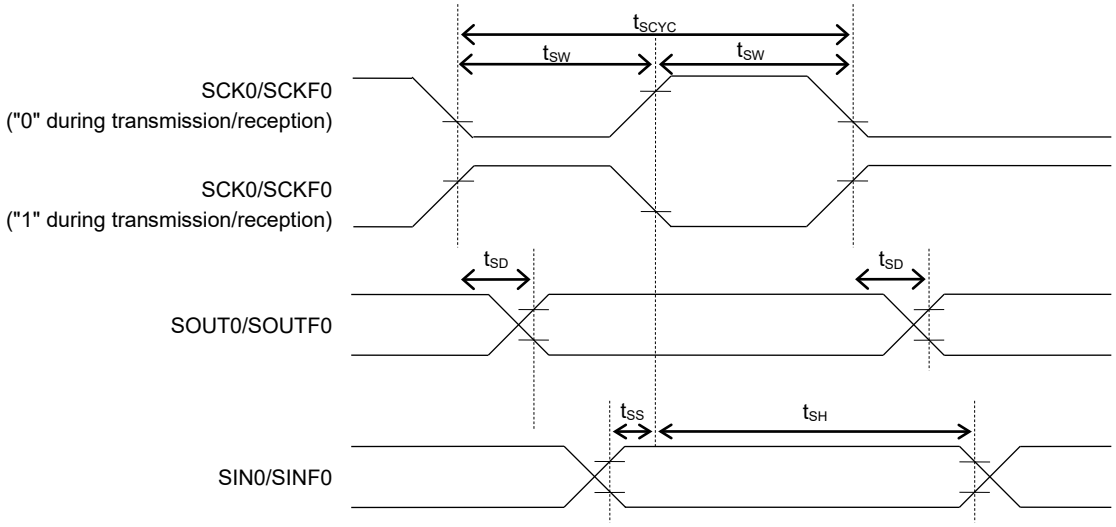
● AC charctoristics (synchronous serial port)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Conditon	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation is not active	10	–	–	μs
		High-speed oscillation is active	500*2	–	–	ns
SCK output cycle (master mode)	t_{SCYC}	–	–	SCK*1	–	s
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation is not active	4	–	–	μs
		High-speed oscillation is active	200	–	–	ns
SCK output pulse width (master mode)	t_{SW}	–	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	–	–	–	180	ns
SOUT output delay time (master mode)	t_{SD}	–	–	–	80	ns
SIN input Setup time (slave mode)	t_{SS}	–	50	–	–	ns
SIN input Setup time (master mode)	t_{SS}	–	130	–	–	ns
SINinput Hold time	t_{SH}	–	50	–	–	ns

*1 : The clock period which is selected by the below registers(min:250ns@ regularly, min:500ns@P02,P22 is used)
In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).
In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)

*2 : In case of SSIOF, Set the period of SYSCLK in half or less of the t_{SCYC} in a period.



● AC characteristics (I^2C Bus interface : Standard mode 100kHz)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

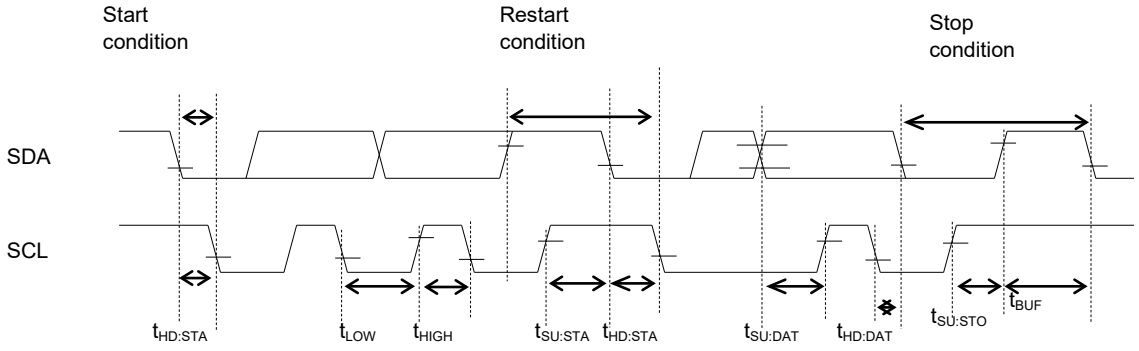
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	100	kHz
SCL hold time (Start/restart condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL"L" level time	t_{LOW}	–	4.7	–	–	µs
SCL"H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL setup time (restart condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA setup time (stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus-free time	t_{BUF}	–	4.7	–	–	µs

● AC characteristics (I^2C bus interface : fast mode 400kHz)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rateing			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	400	kHz
SCLhold time (start/restart condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL"L" level time	t_{LOW}	–	1.3	–	–	µs
SCL"H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL setup time (restart condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA setup time (stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus-free time	t_{BUF}	–	1.3	–	–	µs

*1: Only at the time of SYSCLK=16MHz or 24MHz



● AC characteristics (RC-ADC)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

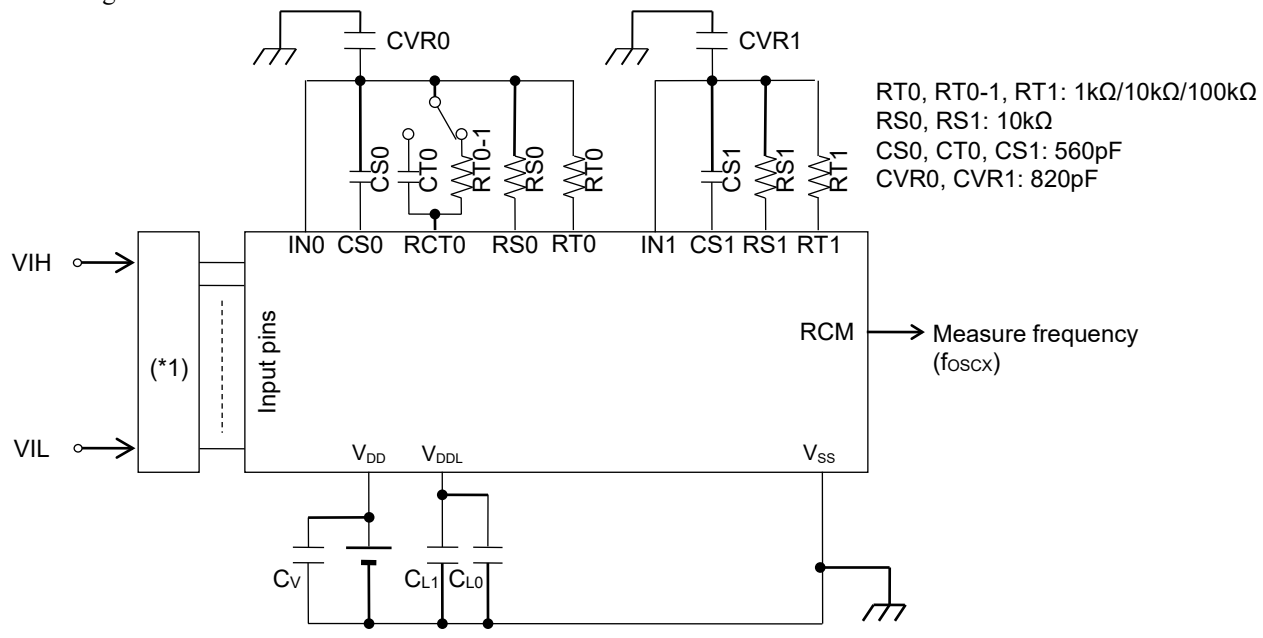
Parameter	Symbol	Condition	Rating			unit
			Min.	Typ.	Max.	
Resister for oscillation	RS0,RS1,RT0 ,RT0-1,RT1	–	1	–	400	kΩ
Oscillation freqency V_{DD} = 3.0V CVR = 820pF CS = 560pF	f_{OSC1_0}	Resister for oscillation =1kΩ	–	528	–	kHz
	f_{OSC2_0}	Resister for oscillation =10kΩ	–	59	–	kHz
	f_{OSC3_0}	Resister for oscillation =100kΩ	–	5.9	–	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V CVR = 820pF CS = 560pF	Kf1_0	RT0, RT0-1, RT1=1kΩ	8.225	8.94	9.655	–
	Kf2_0	RT0, RT0-1, RT1=10kΩ	0.99	1	1.01	–
	Kf3_0	RT0, RT0-1, RT1=100kΩ	0.093	0.101	0.109	–

*1 : Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}}{(RT0\text{-}CS0\ oscillation)} \Big/ \frac{f_{OSCx}}{(RS0\text{-}CS0\ oscillation)}\ ,\ \frac{f_{OSCx}}{(RT0\text{-}1\text{-}CS0\ oscillation)} \Big/ \frac{f_{OSCx}}{(RS0\text{-}CS0\ oscillation)}\ ,\ \frac{f_{OSCx}}{(RT1\text{-}CS1\ oscillation)} \Big/ \frac{f_{OSCx}}{(RS1\text{-}CS1\ oscillation)}$$

(x = 1, 2, 3)

Measuring circuit



(*1) Input logic circuit to determine the specified measuring conditions.

[Note]

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please shield the signal by V_{SS}(GND).
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have

● AC characteristics (Low speed clock output)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

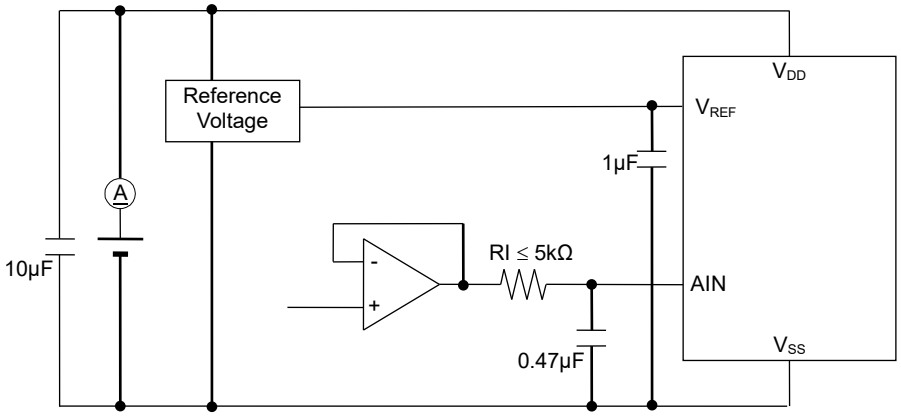
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Clock output frequency	tclk	–	–	32.768	–	kHz

● Electrical Characteristics of SA-ADC

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	–	–	12	–	bit
Integral non-linearity error	INL	2.7V ≤ V_{REF} ≤ 3.6V	−4	–	+4	LSB
		2.2V ≤ V_{REF} < 2.7V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	−3	–	+3	
		2.2V ≤ V_{REF} < 2.7V	−5	–	+5	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−9	–	+9	
Zero-scale error	V_{OFF}	2.2V ≤ V_{REF} ≤ 3.6V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Full-scale error	FSE	2.2V ≤ V_{REF} ≤ 3.6V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Input impidance	RI	–	–	–	5k	Ω
Reference voltage	V_{REF}	–	1.8	–	V_{DD}	V
Conversion time	t_{CONV}	Using High-speed clock(max. 4MHz)	–	170	–	clk
		Using Low-speed clock	–	16	–	

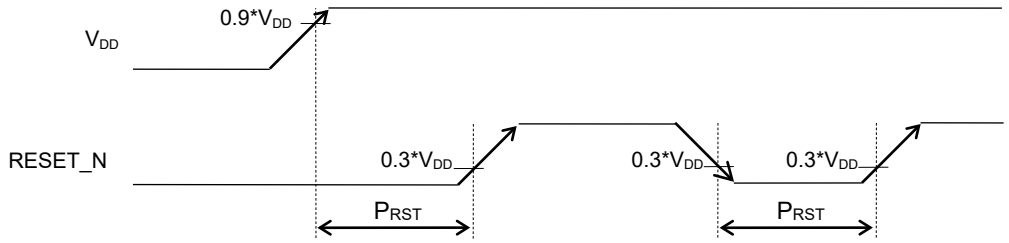
Measuring circuit



● Reset characteristics

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Reset pulse width	P_{RST}	–	200	–	–	μs	1
Reset noise elimination pulse width	P_{NRST}	–	–	–	0.3	μs	
Power-on reset activation power rise time	T_{POR}	–	–	–	10	ms	

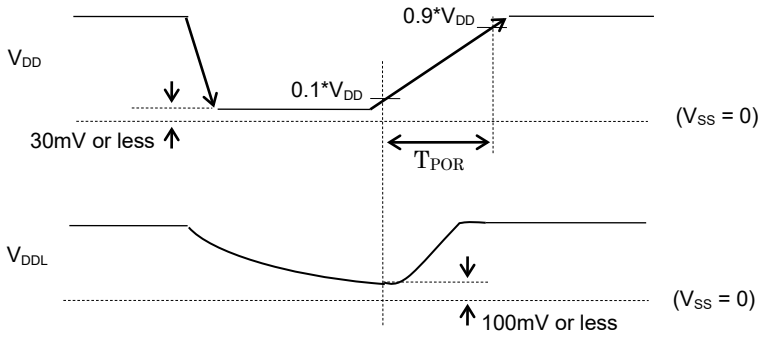


External reset sequence

Power on reset sequence

● Power-on and shutdown Procedures

In case of power-on or shutdown of V_{DD}, the procedures and constraints are shown as following.



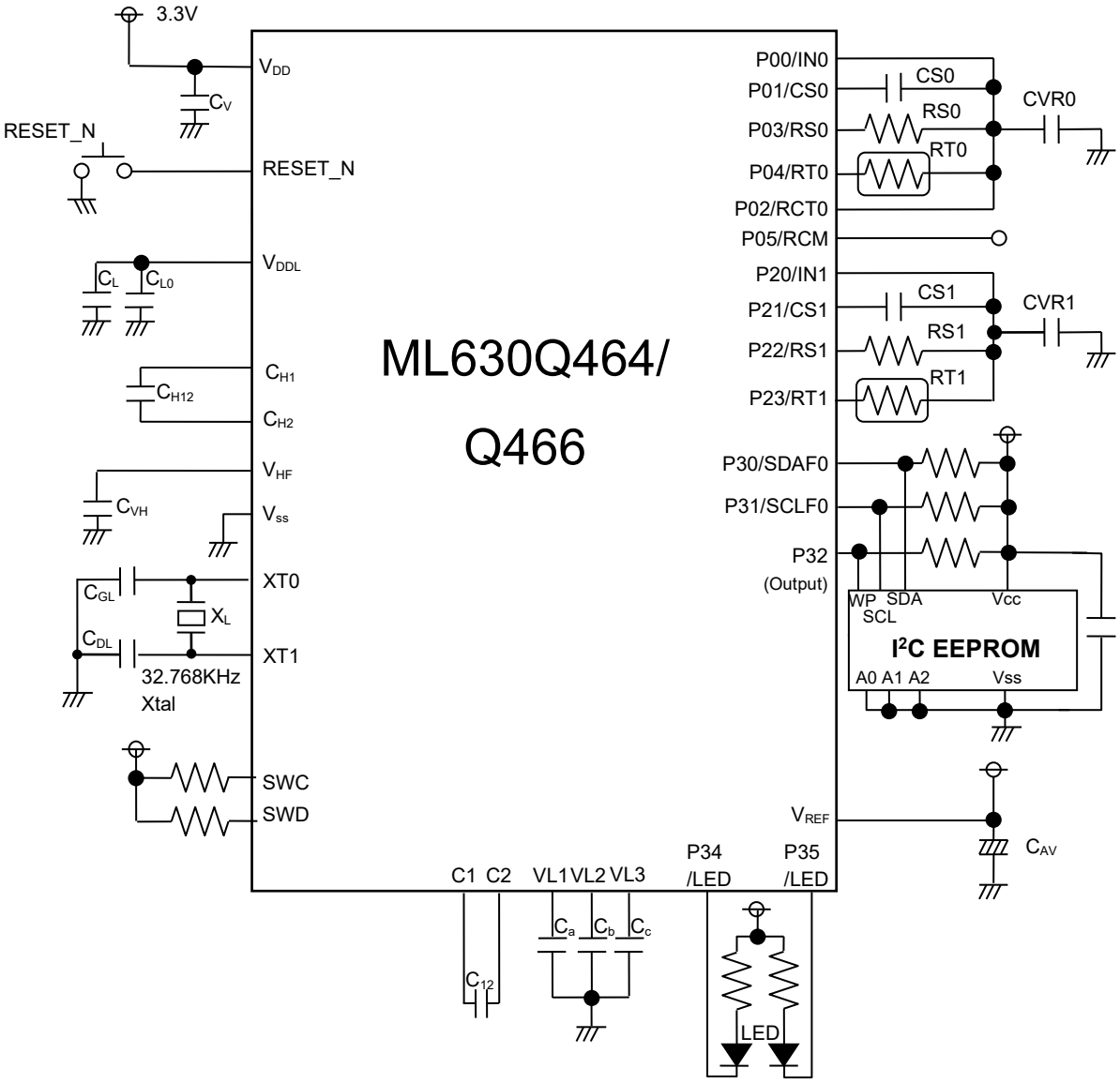
Power down/on and power on reset sequence

Note:

・If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.

・T_{POR} is the value when V_{DD} slope is liner. If V_{DD} slope is not liner in your system, use RESET_N or contact us.

Appendix D Application Circuit Example



C_V	: 1uF*		
C_L	: 2.2uF	C_{L0}	: open*
C_{GL},C_{DL}	: 12 to 16pF*		
C_a~C_c	: 1uF*	C_{12}	: 1uF*
C_{H12}	: 1uF*	C_{VH}	: 1uF*
C_{AV}	: 1uF*	RS0, RS1	: 10 KΩ
CS0, CS1	: 560 pF	CVR0, CVR1	: 820 pF
RT0, RT1	: Thermistor (103AT/Semitec)		
X_L	: DT-26, Daishinku		

*: Make a decision the parameters after evaluating on a user's conditions when designing circuits for mass production.

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL630Q464-01	Nov. 22, 2016	–	–	First edition
FEUL630Q464-02	June. 11, 2021	1-12	1-12	[1.3.4] Updated about RESET_N, BRMP pins in table 1-3.
		6-11	6-11	[6.3.1.2] Updated note.
		9-8	9-8	[9.3.1] Corrected the flow in figure 9-3.
		11-8 11-23	11-8 11-23	[11.2.4][11.2.12] Corrected description of FTnIOB.
		11-9	11-9	[11.2.11] Corrected exposition of bit 0
		12-21	12-21	[12.3] Added an exposition of AL0INT.
		20-8	20-8	[20.2.4] Corrected exposition of bit 6
		30-8 30-9	30-8 30-9	[30.3.1] Corrected exposition.
		C-2	C-2	Added comment in recommended operating conditions.
		C-21	C-21	Corrected "Power-on and shutdown Procedures"
		C-4	C-21	Changed placement of reset characteristics. Added note.
		-	*-*	Corrected typo
FEUL630Q464-03	Dec. 15, 2023	1	1	Rivised the Note.
		-	2	Added Notes for product usage.
		-	1-1	[1] Added aplication information.
		B-1	B-1	Updated Figure B-1.