LogiCoA™ Power Solutions

# Synchronous Buck DCDC Converter Evaluation Board LogiCoA001-EVK-001

## (12V→5V, 5A)

## Introduction

LogiCoA™ Power is a solution adopting analog-digital hybrid control to a switching power supply. This user's guide will provide the steps necessary to operate the evaluation board of LogiCoA™ Power Solution Synchronous buck DCDC converter, LogiCoA001-EVK-001. Bill of materials, operating procedures and application data are included.

## Table of Contents

## 1 Overview of LogiCoA™ Power Solution

Figure 1-1 shows the overview of LogiCoA™ Power Solution. LogiCoA™ Power is a solution adopting analog-digital hybrid control to a switching power supply and consists from 3 elements, (1) Microcontroller for Power Supply Control (LogiCoA™ Microcontroller) ML62Q203x/ML62Q204x (hereinafter referred to ML62Q20xx group), (2) Operating System for Power Supply Control Microcontroller, RMOS, and (3) Power Supply Application. Refer to the explanation application note [1] for detail information of analog-digital hybrid control.

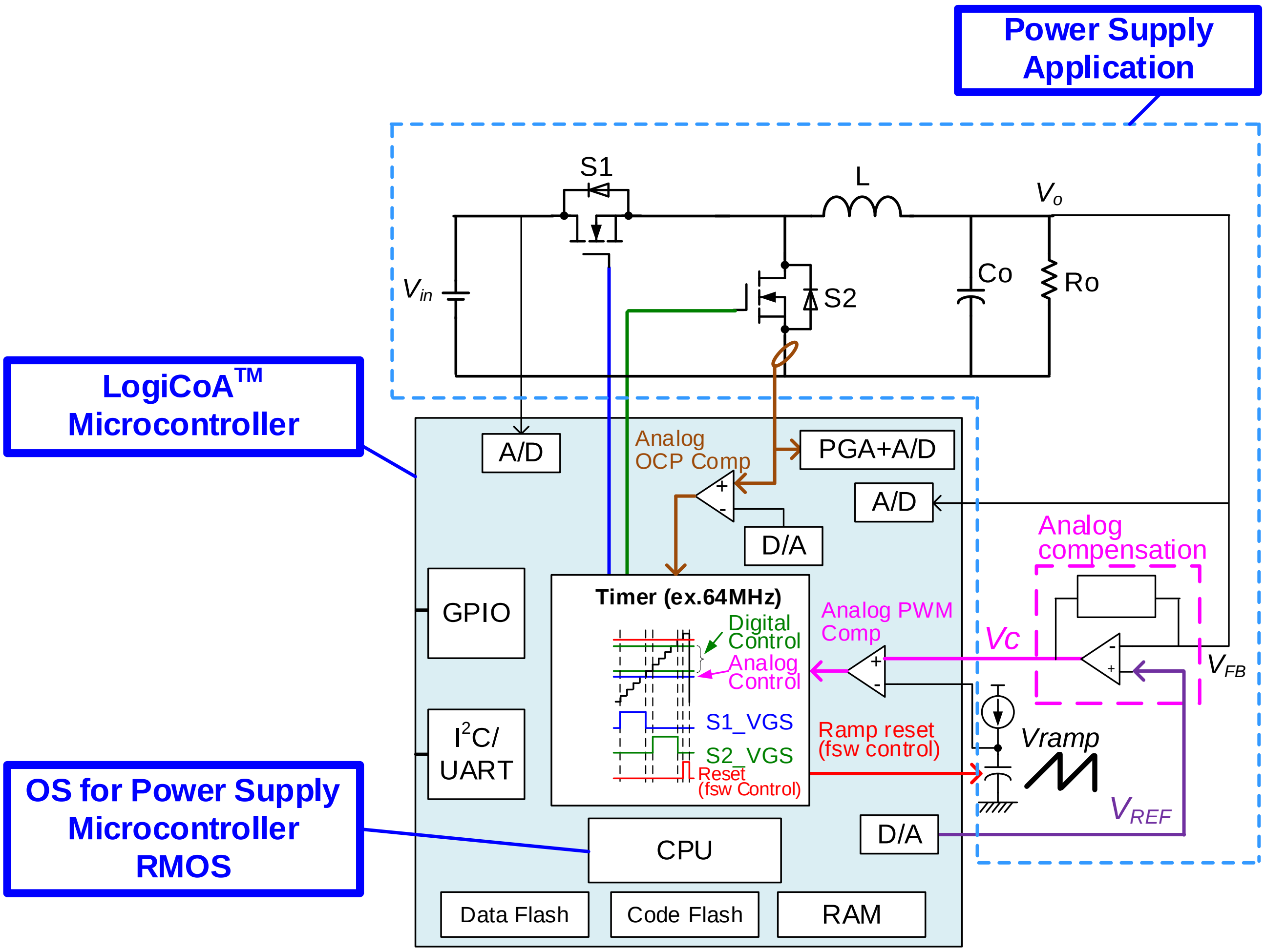



Figure 1-1. System overview of LogiCoA™ Power Solution

(1) Microcontrollers for Power Supply Control (LogiCoA™ Microcontroller)

LogiCoA™ Microcontrollers are suitable ones for power supply control with those analog-digital hybrid control is adopted and ML62Q2033/2035 and ML62Q2043/2045 are released. (at the time of this document's release) On this EVK, ML62Q2035 is mounted. Refer to 4.2 MCU, the datasheet of ML62Q2033/2035/2043/2045 [2] and the user's manual of ML62Q2033/2035/2043/2045 [3] for more detail information about ML62Q2035.

(2) Operating System for Power Supply Control Microcontroller RMOS (**R**eal time **M**icro **O**perating **S**ystem)

RMOS is a multi-task and real-time operating system developed to control switching power supplies and operates on ML62Q20xx group. Refer to the explanation application note [4] for more detail information about RMOS.

(3) Power Supply Application

Power Supply Applications are application circuits correspond to each power supply topology. On this EVK external components such as LDO, gate driver, operational amplifier, MOSFET inductor and so on are mounted as an application circuit of synchronous buck converter.

## 2 Operating Conditions

(Unless otherwise specified Ta=25°C, Vin=12V)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input Voltage | Vin | 7.5 | 12.0 | 38.0 | V | |
| Control Block Supply Voltage(LDO) | Vcc5Vldo | 4.9 | 5.0 | 5.1 | V | Vcc5V=LDO Output |
| Control Block Supply Voltage(USB) | Vcc5Vusb | 4.25 | 5.00 | 5.75 | V | Vin=open, Vcc5V=USB VBUS Output |
| Driver Block Supply Voltage | Vcc12V | 11.4 | 12.0 | 12.6 | V | Vin>13V |
| Output Voltage | Vo | - | 5.0 | - | V | default setting,<br>variable with serial communication |
| Output Voltage Range | Vo_r | 1.0 | - | 8.0 | V | variable with serial communication |
| Output Current | Io | - | - | 5.0 | A | |
| Switching Frequency | fsw | - | 160 | - | kHz | default setting |
| Switching Frequency Range | fsw_r | 80 | - | 500 | kHz | |
| Maximum Duty | Dmax | - | 80 | - | % | default setting |
| Soft Start Time | Tsstart | - | 5 | - | ms | Io=0A |
| Efficiency | η | - | 92 | - | % | Vo=5V, Io=5A |
| Startup Voltage | Vstart | - | 9.0 | - | V | Vin rise, default setting,<br>variable with serial communication |
| Startup Voltage Range | Vstart_r | 7.5 | - | 38.0 | V | |
| Stop Voltage | Vstop | - | 8.0 | - | V | Vin fall, default setting,<br>variable with serial communication |
| Stop Voltage Range | Vstop_r | 7.5 | - | 38.0 | V | |
| Startup Delay Time | Tstart | - | 1000 | - | ms | Vin rise, default setting |
| Startup Delay Time Range | Tstart_r | 10 | - | - | ms | |
| Input Voltage Protection | Vivp | - | 38.0 | - | V | default setting |
| Input Voltage Protection Range | Vivp_r | 7.5 | - | 38.0 | V | |
| Over Current Protection | Iocp | - | 6.0 | - | A | default setting |
| Over Current Protection Range | Iocp_r | 2.5 | - | 8.0 | A | |
| Output Low Voltage Protection | Vlvp | - | 3.0 | - | V | Vo fall, default setting |
| Output Low Voltage Protection Range | Vlvp_r | 1.0 | - | 7.0 | V | |
| Output Low Voltage Protection Mask Time | Tlvp | - | 500 | - | ms | Vo fall, default setting |
| Output Low Voltage Protection Mask Time Range | Tlvp_r | 10 | - | - | ms | |
| Output Over Voltage Protection | Vovp | - | 6.0 | - | V | Vo rise, default setting |
| Output Over Voltage Protection Range | Vovp_r | 1.0 | - | 10.0 | V | |

## 3 Firmware

For this EVK, in addition to the evaluation board, the source code of RMOS and power supply control are supplied. And those can be downloaded from the URL below.

Table 3-1. RMOS download URL and the file name

| | |
|---|---|
| Download URL | https://www.rohm.com/reference-designs/ref66009 |
| Reference Program Name | LogiCoA™ Solution Buck Converter Reference Program |
| File Name | RMOS100-PSFW001.zip |

# 4 Block Diagram and Description

## 4.1 Block Diagram

Figure 4-1 shows the application block diagram of this EVK.

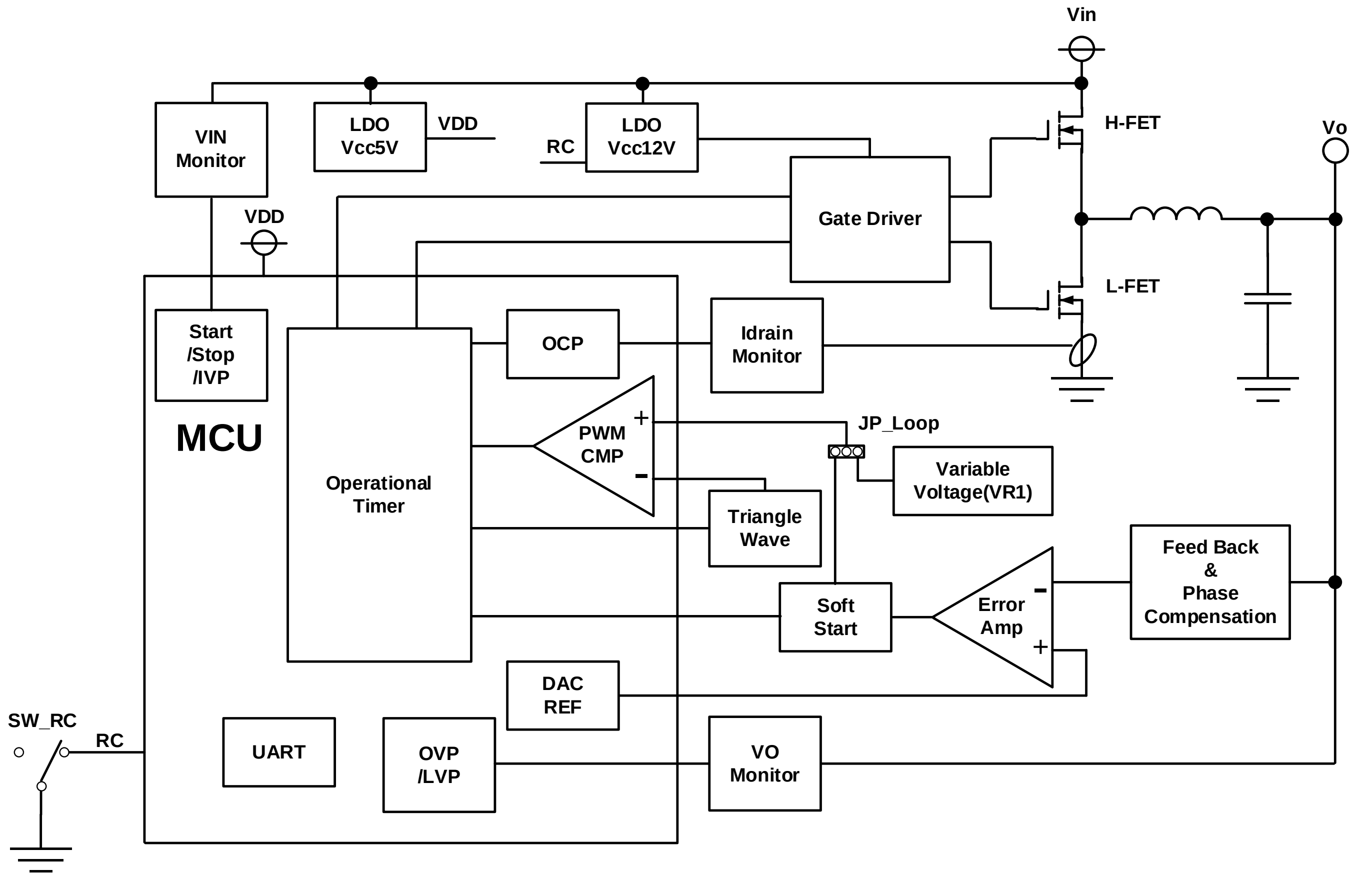



Figure 4-1. Application Block Diagram

## 4.2 MCU

On this EVK, MCU ML62Q2035 is mounted as a power supply controller. VDD voltage of MCU is supplied from the control block power supply Vcc5V, and after supplied voltage becomes over 4.10V (typ) of the threshold voltage of POR, the microcontroller startup and RMOS starts its operation. Each pin's function of ML62Q2035 and selected function in this EVK is listed in Table 4-1.

Table 4-1. Pin list of ML62Q2035

| Pin No. | Pin Name | 1st Function | 2nd Function | 3rd Function | 4th Function | 5th Function | 6th Function | 7th Function | 8th Function |
|---|---|---|---|---|---|---|---|---|---|
| | | GPI/EXI | UART | $I^2C$ | OTM | CMP/DAC | ADC | CMP | CMP/ADC |
| 19 | VDD | — | — | — | — | — | — | — | — |
| 18 | VSS | — | — | — | — | — | — | — | — |
| 17 | VDDL | — | — | — | — | — | — | — | — |
| 16 | P01 | — | — | — | — | CMP0P | — | CMP0P /CMP1P | CMP0P |
| 15 | P02 | — | — | — | OTO4B | CMP0M | — | CMP0M /CMP1M | CMP0M |
| 14 | P03 | EXI0 | — | — | OTO0A | — | — | — | — |
| 13 | P04 | EXI1 | — | — | OTO0B | — | — | — | — |
| 12 | P05 | EXI1 | — | — | OTO1A | — | — | — | — |
| 11 | P06 | EXI2 | — | — | OTO2A | — | — | — | — |
| 10 | P10 | EXI3 | RXD1, (/TXD1) | — | OTO3A | — | — | — | — |
| 9 | P11 | — | — | — | OTO4A | CMP2P | — | CMP2P | CMP2P |
| 8 | P12 | — | RXD0, (/TXD0) | SDAU0 | OTO1B | — | — | — | — |
| 7 | P00/TEST0 | EXI3 | — | — | — | — | — | — | — |
| 6 | P13 | EXI2 | TXD0 | SCLU0 | OTO5B | — | AIN4 | — | — |
| 5 | RESET_N | — | — | — | — | — | — | — | — |
| 4 | P14 | — | — | — | — | CMP1P | AIN0 | CMP1P /CMP2P | AIN0 /CMP1P |
| 3 | P15 | — | — | — | — | CMP1M | AIN1 | CMP1M /CMP2M | AIN1 /CMP1M |
| 2 | P16 | — | — | — | — | CMP2M | AIN2 | CMP2M | AIN2 /CMP2M |
| 1 | P17 | EXI0 | — | — | — | — | AIN3 | — | — |
| 20 | P23 | — | TXD1 | — | OTO5A | DACOUT0 | — | — | — |

(highlighted) selected function in this EVK

Table 4-2 listed the typical specifications of ML62Q2035. Refer to [2] and [3] for more detail information about ML62Q2035.

Table 4-2. Typical specifications of ML62Q2035

| | | |
|---|---|---|
| Part Number | | ML62Q2035 |
| CPU | | 16bit RISC CPU Core(nx-U16/100), Max operating frequency 16MHz |
| Memory | | Code Flash: 32KB, Data Flash: 4KB(Erase Unit:128B), RAM: 2KB |
| Analog Comparator | | 3ch(asynchronous to clock), Response time: Max 100ns |
| Timer | | 16bit timer with PWM/Capture × 6 counters, 10 outputs |
| | | Max 64MHz operation(Resolution 15.625ns) |
| AD Converter | | 12bit SA-ADC: 5ch |
| DA Converter | | 8bit, 2ch |
| Programmable Gain Amplifier | | 1ch, Gain Setting: 4 steps (×4/×8/×16/×32) |
| Serial I/F | | I$^2$C×1, UART×2 |
| I/O Port | | I: 1, I/O: 15 |
| External Interrupt | | 4 |
| Other | | Multiplication/Division Unit, Temperature Sensor, Power ON Reset |
| Clock | Low | Internal RC Oscillator: 32.768kHz ± 1.5%* |
| | High | PLL: 64MHz ± 1.5%*, CPU: 16MHz to 125kHz ± 1.5%* |
| | | PWM/Capture: 64MHz to 500kHz ± 1.5%* |
| Current Consumption(CPU) | | Stop: 80μA, Halt: 90μA, Active: 3.3mA@16MHz |
| Operating Supply Voltage | | 4.5V to 5.5V |
| Operating Temperature | | Ta=-40°C to +105°C(Tj=115°C) (Absolute maximum ratings:Tjmax=125°C) |
| Package | | TSSOP20 |

*: Ta=-20°C to +85°C

## 4.3 Control Block Power Supply

On this EVK, a fixed 5V output LDO BD950N1WG-C is mounted as a power supply (Vcc5V) for control block (MCU and analog control circuit). BD950N1WG-C has standby control function, but in this EVK, VIN pin and EN pin are shorted and so when Vin voltage is applied and VIN pin of BD950N1WG-C voltage is over UVLO rise voltage (typ 2.6V), Vcc5V turns on. Refer to the datasheet of BD9xxN1-C series [5] for more detail information about BD950N1WG-C.

## 4.4 Driver Block Power Supply

On this EVK, a 12V output LDO BD900N1WG-C is mounted as a power supply (Vcc12V) of the gate driver to drive output FET. BD900N1WG-C has standby control function and can be controlled turning ON/OFF by a remote control switch described later. Refer to the datasheet of BD9xxN1-C series [5] for more detail information about BD900N1WG-C.

## 4.5 Remote Control Switch

This EVK has RC (RC: Remote Control) function for external turning ON/OFF control. DCDC operates as the setting below by turning the mechanical switch (SW_RC) connected P10 pin of ML62Q2035 to OPEN or short to GND. To avoid a false detection by noise, there are mask time of 150μs at RC=H detection and 1.25ms at RC=L. P10 pin is set as a GPIO with internal 40kΩ(typ) pulled-up. Refer to [2] about the threshold of operating state because it depends on input/output characteristics of ML62Q2035.

Table 4-3. Operating state of Remote Control Switch

| SW_RC | P10 pin | DCDC |
|---|---|---|
| OPEN | VDD | ON |
| GND SHORT | GND | OFF |

## 4.6 Error Amplifier and Reference Voltage

Figure 4-2 shows the error amplifier and surrounding circuits. BU7481SG is mounted on as an error amplifier. As control block power supply Vcc5V is supplied, the error amplifier starts to operate but startup of the error amplifier output is controlled by the soft start circuit. Refer to the datasheet of that [6] for more detail information about BU7481SG.

The reference voltage of error amplifier Vo_REF is generated by the 8-bits DA converter built-in in the MCU (1.973V at VDD=5V). Output voltage Vo is calculated as following equation.

$$Vo = V_{O\_REF} \times \frac{R_{29} + R_{30} + R_{31}}{R_{31}}$$

Ex.) When Vo_REF=1.973V, $R_{29}$=51Ω, $R_{30}$=3.3kΩ and $R_{31}$=2.2kΩ, output voltage is as below.

$$Vo = 1.973V \times \frac{51\Omega + 3.3k\Omega + 2.2k\Omega}{2.2k\Omega} \cong 4.9782V$$

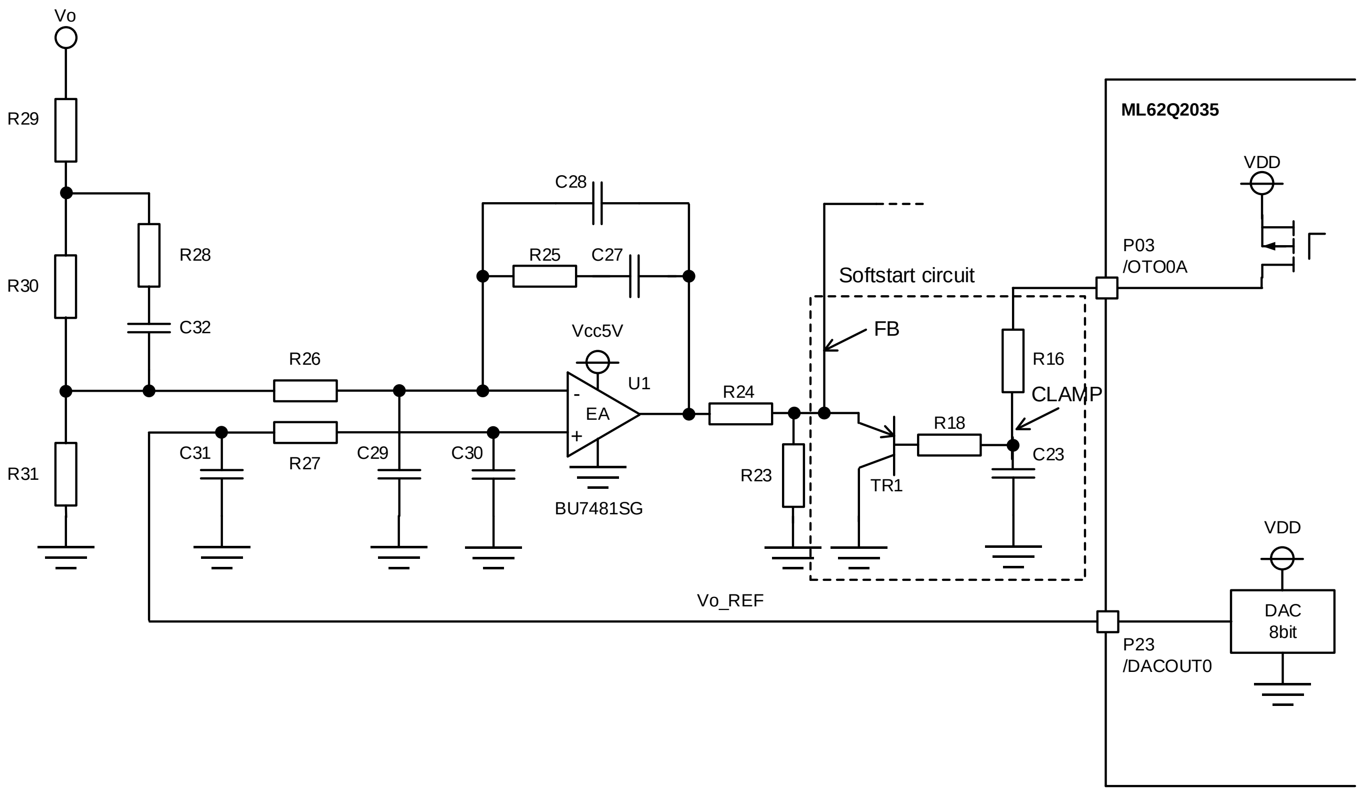



Figure 4-2. Error amplifier and surrounding circuits

## 4.7 Soft Start

In this EVK, to avoid an overshoot and rush current, output of the error amplifier (FB) is clamped while starting up, thus ramp up speed of DCDC output is controlled and starts softly.

The FB voltage is clamped by the CLAMP voltage + $V_{BE}$ of $TR_1$ because the voltage generated at both ends of $R_{18}$ can be considered minute due to $R_{18}$=100Ω and $TR_1$ base current. P03/OTO0A pin has been set as PMOS open drain, and while in startup, clamped voltage rise up slowly by controlling the ON duty of the PMOS. In the steady state, the CLAMP voltage is equal to VDD and thus the FB voltage is not clamped.

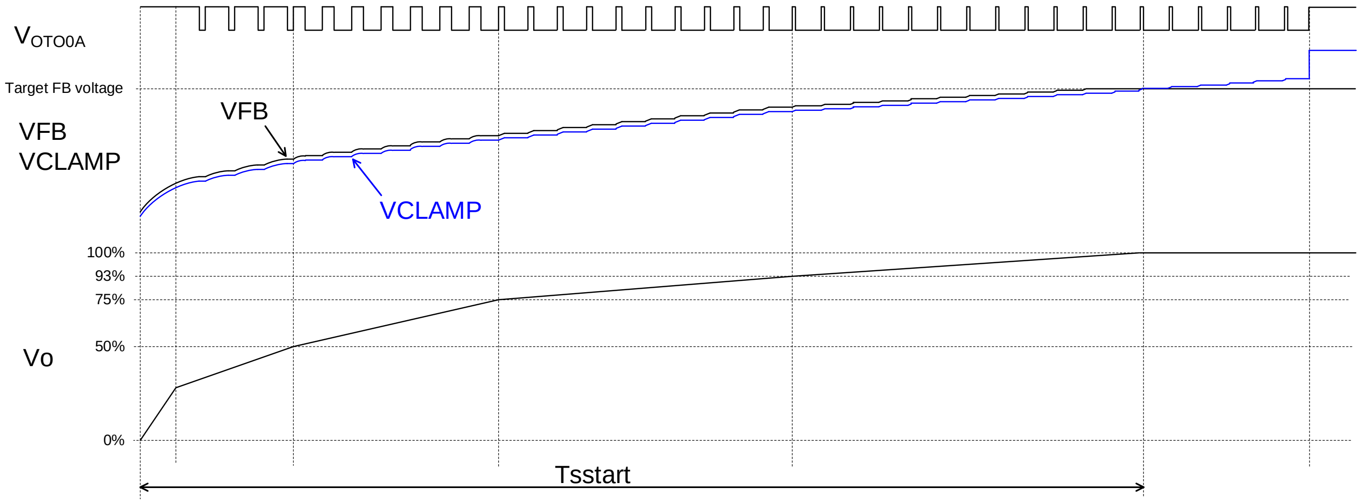



Figure 4-3. Soft start operation timing chart

## 4.8 Triangle Waveform Generator and PWM Comparator

Figure 4-4 and 4-5 shows the triangle waveform generator and surrounding circuits, and timing chart. Triangle waveform is generated at P02/CMP0M pin by clock pulse output from P04/OTO0B pin. P01/CMP0P pin and P02/CMP0M pin have been set as an input of analog comparator and the build-in analog comparator operate as the PWM comparator.

As shown in Figure 4-5, the frequency of clock pulse output from P04/OTO0B pin is the switching frequency of the DCDC converter fsw (160kHz). And while the output of the clock pulse is H, the voltage of TRNGL becomes also H, so the output of the PWM comparator is L. This leads that the L duty of the clock pulse is the Max Duty Dmax (80% typ) of the DCDC converter.

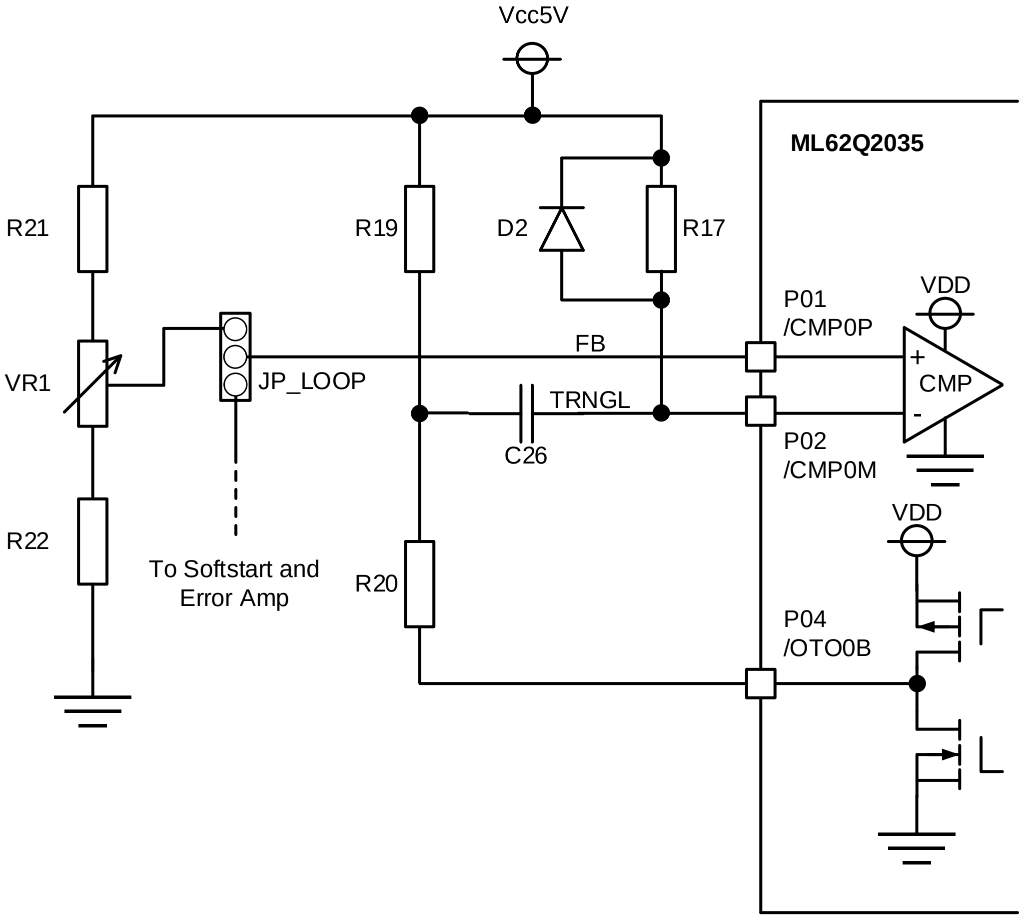



Figure 4-4. Triangle waveform generator and surrounding circuit

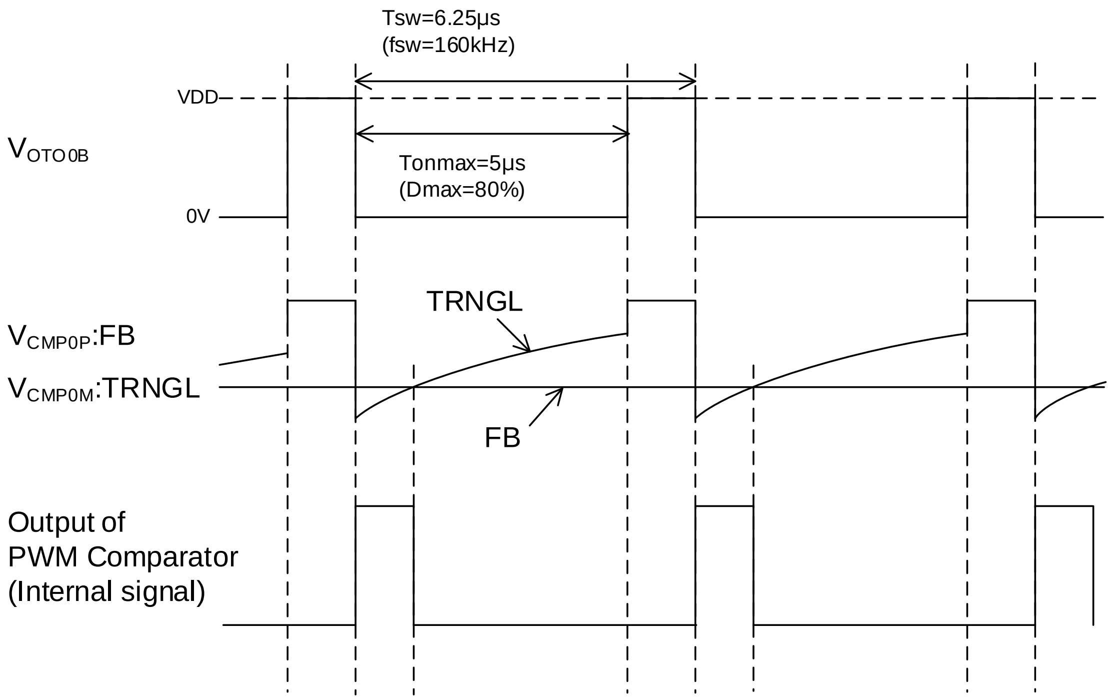



Figure 4-5. Triangle waveform generator timing chart

## 4.9 Volume Resistor for open loop operation (for debug)

This EVK can be operated in open loop without feedback control for debugging. Open loop and closed loop operation can be exchanged by the jumper connection of JP_Loop (refer to Figure 4-1. Application Block Diagram and Figure 4-4. Triangle waveform generator and surrounding circuit.) When open loop operation is selected, the input voltage of the PWM comparator can be tuned using volume resistor $VR_1$. The divided voltage from Vcc5V by $R_{21}$ and 10kΩ volume resistor $VR_1$ will be the FB voltage (0Ω is mounted on $R_{22}$.)

## 4.10 Output Stage

In output stage, the control signals of H-side/L-side FET from the MCU level shifted by the gate driver drive output FETs, and stable voltage smoothed by the LC filter is supplied. BD2320EFJ-LA is mounted on as a gate driver. Refer to the datasheet of that [7] for more detail information of BD2320EFJ-LA.

## 4.11 Input Voltage Detection Block

Figure 4-6 shows the input voltage detection block. The divided Vin voltage by $R_6$ and $R_7$ is input to the P15/AIN1 pin of ML62Q2035, and the digital value of pin input voltage converted by the 12bits AD converter is obtained.

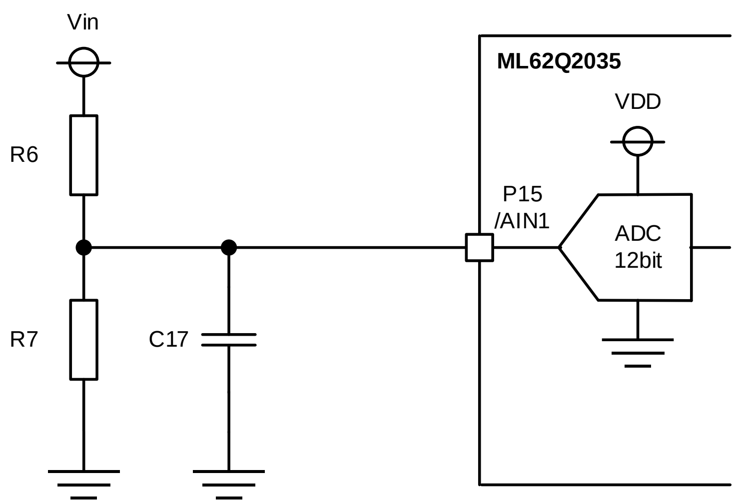



Figure 4-6. Input voltage detection block

### 4.11.1 Startup/Stop Voltage Check

In this EVK, Vin input voltage is monitored by the input voltage detection block described above and when the voltage is over the startup voltage of 9V, DCDC startups after the 1s of the startup delay time. When the input voltage is below 8V, DCDC stops. For a noise reduction, there is a 150µs of mask time in voltage detection.

### 4.11.2 Input Voltage Protection

This EVK has an input over voltage protection function (IVP: Input Voltage Protection). Vin input voltage is monitored by the input voltage detection block described above and when the voltage is over the detect voltage of 38V, the protection works and DCDC stops output switching. For a noise reduction, there is a 250µs of mask time in voltage detection. When the input voltage is below the detect voltage in the normal operation state, count of the mask time is reset. When protection works, DCDC stops latched, and restarts after turning on RC again in the condition that Vin input voltage is under the detection threshold voltage.

## 4.12 Output Voltage Detection Block

Figure 4-7 shows the output voltage detection block. The divided Vo voltage by $R_{32}$ and $R_{33}$ is input to the P14/AIN0 pin of ML62Q2035, and the digital value of pin input voltage converted by the 12bits AD converter is acquired.

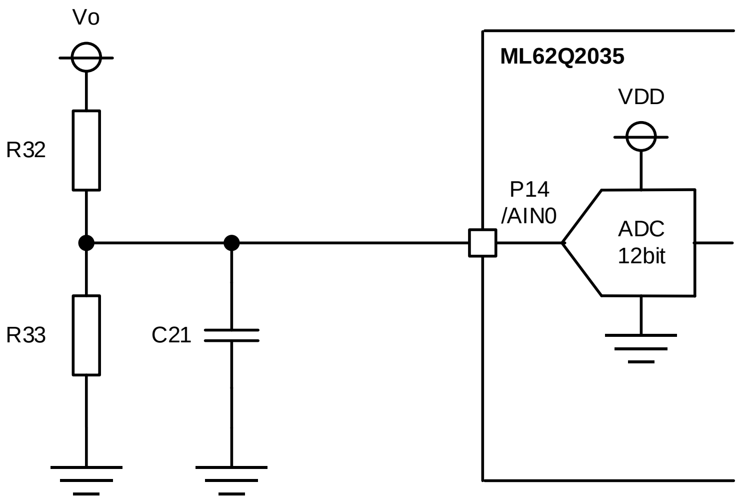



Figure 4-7. Output voltage detection block

### 4.12.1 Low Voltage Protection

This EVK has an output low voltage protection function (LVP: Low Voltage Protection). Vo output voltage is monitored by the output voltage detection block described above and when the voltage drops less than the detect voltage of 3.0V, timer count starts. When the output voltage remains below the detect voltage and 500ms has passed, protection works and DCDC stops output switching. The timer counter is incremented from the initial value by every 500µs, and when the output voltage becomes over the detect voltage while in timer counting, the counter value is decremented. When DCDC stops by the protection or RC, the timer counter is reset. When protection works, DCDC stops latched, and restart after turning on RC again.

### 4.12.2 Over Voltage Protection

This EVK has an output over voltage protection function (OVP: Over Voltage Protection). Vo output voltage is monitored by the output voltage detection block described above and when the voltage is over the detect voltage of 6.0V, the protection works, and DCDC stops output switching. For a noise reduction, there is a 250µs of mask time in voltage detection. When the output voltage drops less than the detect voltage in the normal operation state, count of the mask time is reset. When protection works the DCDC stops latched, and restart after turning on RC again.

## 4.13 Drain Current Detection Block

Figure 4-8 shows the drain current detection block. The drain current $I_d$ flows through low side FET, FET2, is converted to the voltage $V_{SNS}$ in the current sense resistor $R_5$. VSNS divided from Vcc5V by $R_8$, $R_9$ and $R_{10}$, $R_{11}$, and added certain offset voltage to meet the input voltage range of AD converter/analog comparator, are input to P16/AIN2 pin and P11/CMP2P pin of ML62Q2035 each. By the built-in AD converter in P16/AIN2 pin, the digital value of the current is acquired and the built-in comparator in P11/CMP2P pin detect the overcurrent.

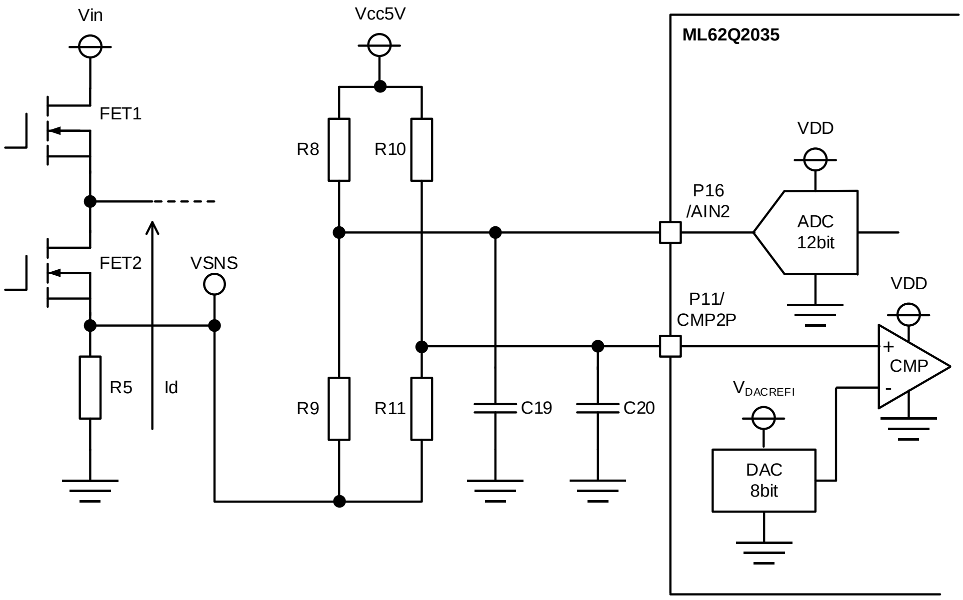



Figure 4-8. Drain current detection block

### 4.13.1 Over Current Protection

This EVK has a pulse-by-pulse over current protection function (OCP: Over Current Protection). The drain current of low side FET is monitored by the analog comparator in the drain current detection block described above. When the current exceeds the detect threshold value of 6.0A, protection works and turning off the FET. After the detection, DCDC restarts from protection automatically, but if the overload state continues, OCP is detected again.

## 4.14 LED Indicator

In this EVK, 2 LEDs of LED1(red) and LED2(green) are mounted on. And each blinking pattern indicates below operating state.

Table 4-4. LED1 Blinking pattern and operating state

| LED1 | State |
|---|---|
| Off | - |
| Blinking | Program writing/Accessing to MCU |

Table 4-5. LED2 Blinking pattern and operating state

| LED2 | State |
|---|---|
| 1 time short blink(100ms x 1) in 1.6ms period | Vin input voltage is below startup voltage(Vin stop state) |
| 2 times short blink(100ms x 2) in 1.6ms period | Vin input voltage is over startup voltage and standby with RC control(RC standby state) |
| 1 time blink(700ms x 1) in 1.6ms period | Normal operation state |
| 5 times short blink(100ms x 5) in 1.6ms period | Abnormal stop state |

## 5 Serial Communication

In this EVK, modification of power supply control parameter and recording the operating log are capable of by a serial communication via the on-board USB-UART covert module from such as an external Windows PC. (Logging function is not implemented at the time of this document's release.) Refer to the explanation application note of communication function and GUI[8] for more detail information about the serial communication and communication commands.

## 6 View of EVK

Figure 6-1 and Figure 6-2 shows the view of EVK.

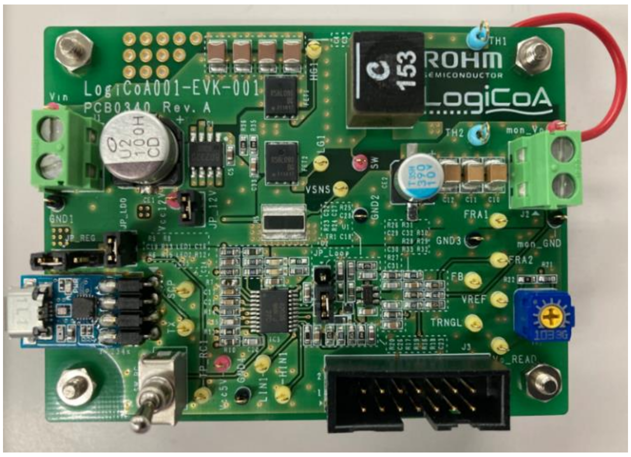



Figure 6-1. LogiCoA001-EVK-001(Top View)

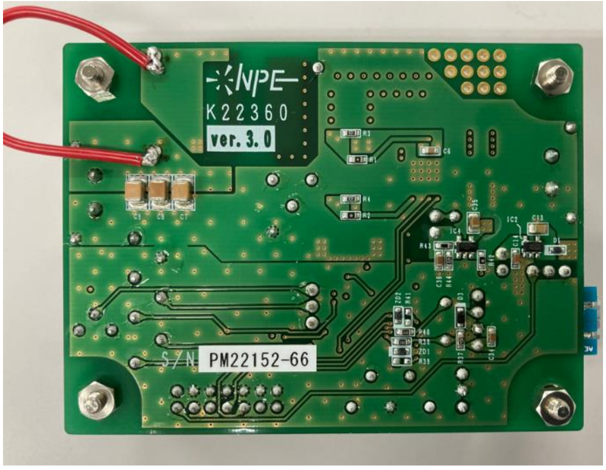



Figure 6-2. LogiCoA001-EVK-001(Bottom View)

## 7 Operating Procedure

1. Short 1-2 pins of the jumper JP_LDO, 1-2 pins of JP_12V, 2-3 pins of JP_Loop and open JP_REG on the EVK.
2. Turn the SW_RC to connect 1-2pins on EVK. (Turn the switch to upper side in the board direction of Figure 6-1.)
3. Turn off the DC power supply and connect it's GND pin to 2 pin of J1 on the EVK.
4. Connect DC power supply's VCC pin to 1 pin of J1 on the EVK.
5. Connect the load between 1 pin and 2 pin of J2 on the EVK. When an electric load is used, turn off the output before connecting to the board.
6. Connect the voltmeter to the mon_Vo pin and mon_GND pin on the EVK.
7. Turn on the DC power supply. Check if the measured value of the voltmeter is 5V.
8. If an electric load is used, turn on the electric load.

*Notes: This EVK does not support hot plugging protection. Do not perform hot plugging on this board.*

## 8 Board Schematic

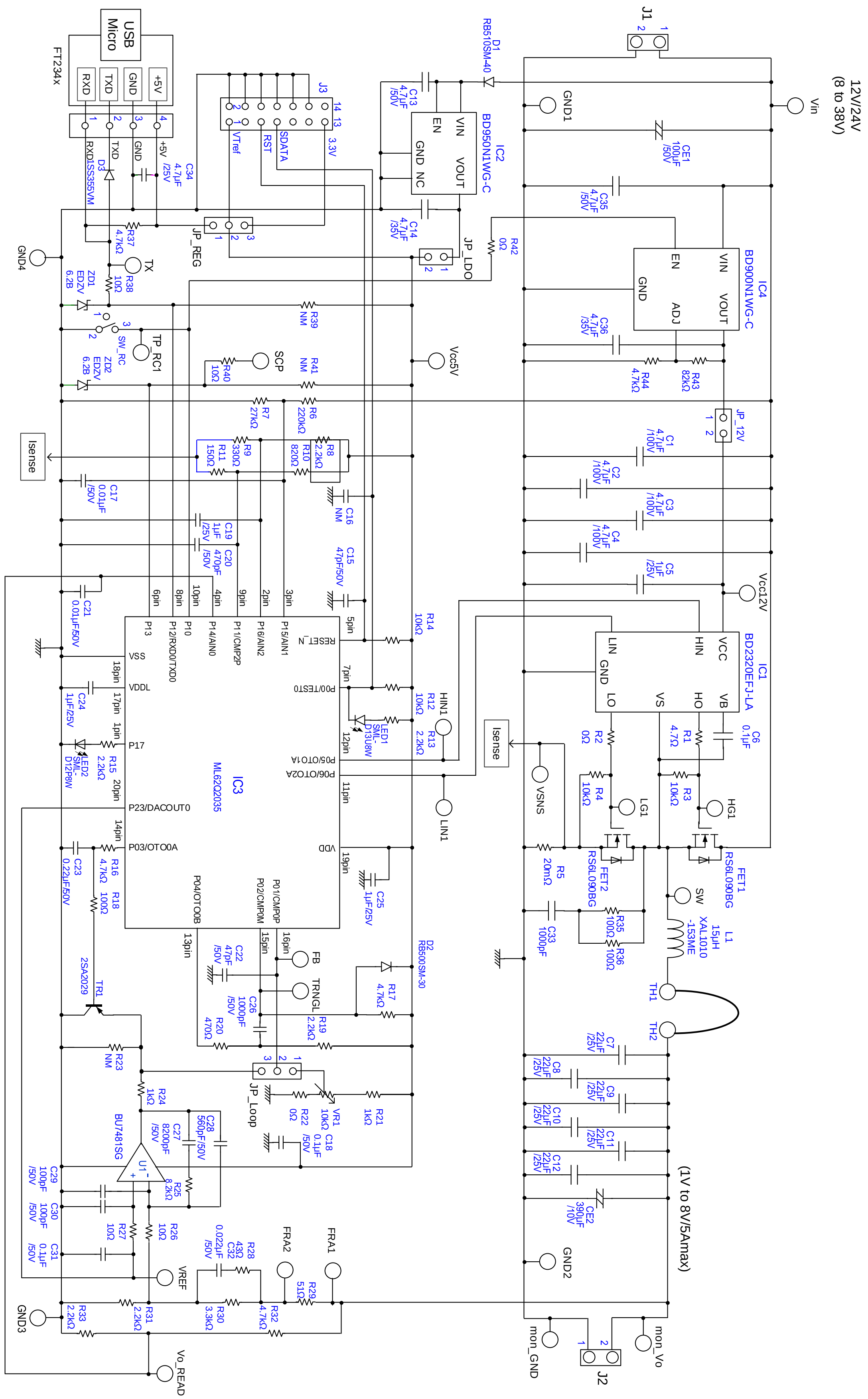


Figure 8-1. Board Schematic

# 9 Board Information and Layout

The board information of this EVK is listed in Table 9-1.

Table 9-1. Board information

| Number of Layers | Material | Board Size | Copper Thickness |
|---|---|---|---|
| 4 | FR-4 | 80mm x 60mm x 1.6mmt | 1oz(35µm) |

Below are EVK layouts.

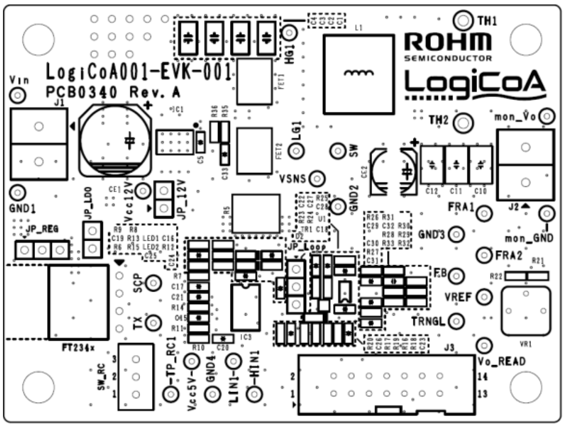



Figure 9-1. Top Silk Screen (Top View)

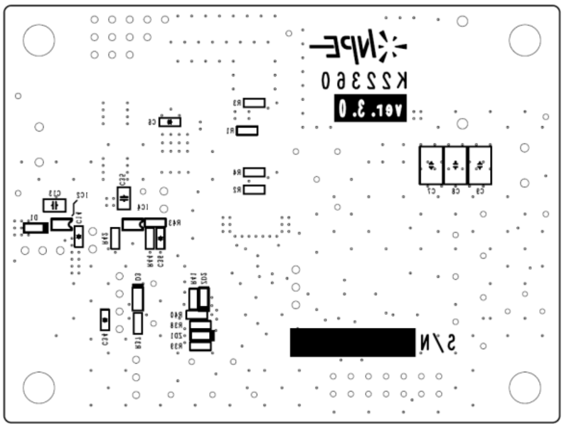


Figure 9-2. Bottom Silk Screen (Top View)

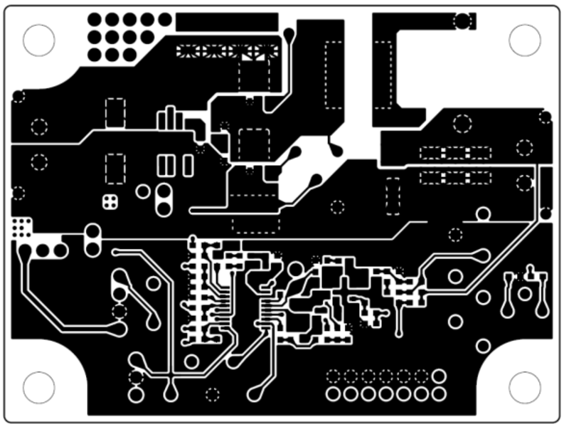


Figure 9-3. Top Layer Layout (Top View)

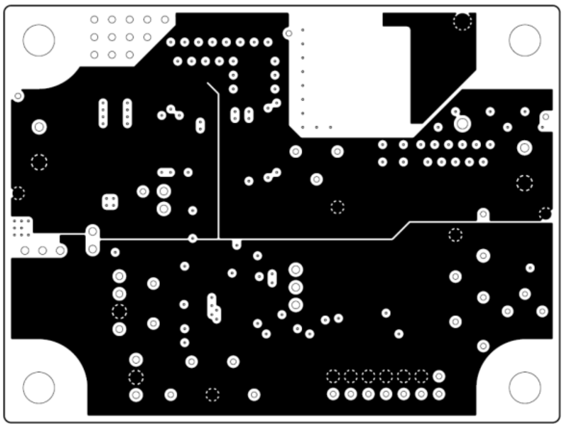


Figure 9-4. Middle1 Layer Layout (Top View)

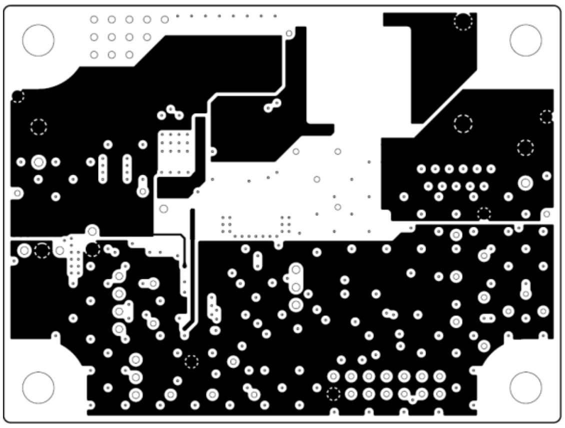


Figure 9-5. Middle2 Layer Layout (Top View)

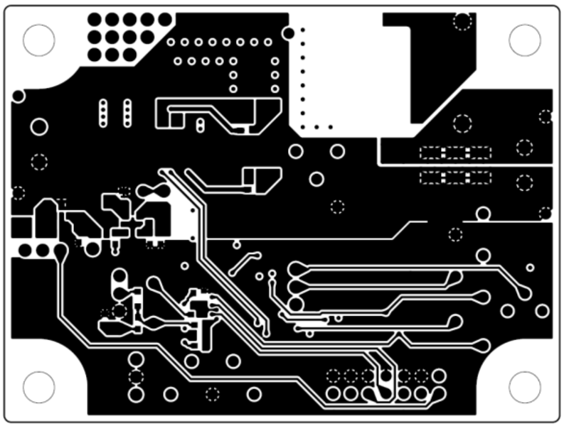


Figure 9-6. Bottom Layer Layout (Top View)

# 10 Bill of Materials

Table 10-1 shows the bill of materials of this EVK.

Table 10-1. Bill of Materials

| Quantity | Reference Designator | Part Number | Manufacturer | Value | Description [Unit: inch(mm)] |
|---|---|---|---|---|---|
| **IC** | | | | | |
| 1 | IC1 | BD2320EFJ-LAE2 | ROHM | - | Gate Driver,14.5V,2024(4960) |
| 1 | IC2 | BD950N1WG-CTR | ROHM | - | LDO, 42V, 5V/150mA,1112(2829) |
| 1 | IC3 | ML62Q2035-NNNTDZWATZ | LAPIS Technology | - | MCU, 5.5V, 32kbyte,2526(6465) |
| 1 | IC4 | BD900N1WG-CTR | ROHM | - | LDO, 42V, 150mA,1112(2829) |
| 1 | U1 | BU7481SG-TR | ROHM | - | 1ch-OPAMP,5.5V,1112(2829) |
| **Resistor** | | | | | |
| 1 | R1 | - | - | 4.7Ω | 0.1W,±1%,0603(1608) |
| 3 | R2,R22,R42 | - | - | 0Ω | 1A,0.1W,0603(1608) |
| 4 | R3,R4,R12,R14 | - | - | 10kΩ | 0.1W,±1%,0603(1608) |
| 1 | R5 | LTR100LJZPFSR020 | ROHM | 20mΩ | 4W,±1%,1225(3264) |
| 1 | R6 | - | - | 220kΩ | 0.1W,±1%,0603(1608) |
| 1 | R7 | - | - | 27kΩ | 0.1W,±1%,0603(1608) |
| 6 | R8,R13,R15,R19,R31,R33 | - | - | 2.2kΩ | 0.1W,±1%,0603(1608) |
| 1 | R9 | - | - | 330Ω | 0.1W,±1%,0603(1608) |
| 1 | R10 | - | - | 820Ω | 0.1W,±1%,0603(1608) |
| 1 | R11 | - | - | 150Ω | 0.1W,±1%,0603(1608) |
| 4 | R16,R17,R32,R44 | - | - | 4.7kΩ | 0.1W,±1%,0603(1608) |
| 3 | R18,R35,R36 | - | - | 100Ω | 0.1W,±1%,0603(1608) |
| 1 | R20 | - | - | 470Ω | 0.1W,±1%,0603(1608) |
| 2 | R21,R24 | - | - | 1kΩ | 0.1W,±1%,0603(1608) |
| 0 | R23 | No mount | - | - | - |
| 1 | R25 | - | - | 8.2kΩ | 0.1W,±1%,0603(1608) |
| 4 | R26,R27,R38,R40 | - | - | 10Ω | 0.1W,±1%,0603(1608) |
| 1 | R28 | - | - | 43Ω | 0.1W,±1%,0603(1608) |
| 1 | R29 | - | - | 51Ω | 0.1W,±1%,0603(1608) |
| 1 | R30 | - | - | 3.3kΩ | 0.1W,±1%,0603(1608) |
| 0 | R39,R41 | No mount | - | - | - |
| 1 | R43 | - | - | 82kΩ | 0.1W,±0.5%,0603(1608) |
| 1 | R44 | - | - | 4.7kΩ | 0.1W,±0.5%,0603(1608) |
| 1 | VR1 | CT-6EP103 | Nidec Copal Electronics | 10kΩ | 70.7V,0.5W,±10%,2828(7070) |
| **Capacitor** | | | | | |
| 4 | C1,C2,C3,C4 | C3225X7S2A475K200AE | TDK | 4.7μF | 100V,X7S,±10%,1210(3225) |
| 4 | C5,C19,C24,C25 | CGA3E1X7R1E105K080AC | TDK | 1μF | 25V,X7R,±10%,0603(1608) |
| 3 | C6,C18,C31 | CGA3E2X7R1H104K080AA | TDK | 0.1μF | 50V,X7R,±10%,0603(1608) |
| 6 | C7,C8,C9,C10,C11,C12 | GRM32ER71E226ME15L | Murata | 22μF | 25V,X7R,±20%,1210(3225) |
| 2 | C13,C35 | GRM21BR61H475ME51L | Murata | 4.7μF | 50V,X5R,±20%,0805(2012) |
| 2 | C14,C36 | GRM188R6YA475ME15D | Murata | 4.7μF | 35V,X5R,±20%,0603(1608) |
| 2 | C15,C22 | CC0603JRNPO9BN470 | Yageo | 47pF | 50V,C0G,±5%,0603(1608) |
| 0 | C16 | No mount | - | - | - |
| 2 | C17,C21 | GRM188B11H103K | Murata | 0.01μF | 50V,B,±10%,0603(1608) |
| 1 | C20 | CGA3E2C0G1H471J080AA | TDK | 470pF | 50V,C0G,±5%,0603(1608) |
| 1 | C23 | CGA3E3X7R1H224K080AB | TDK | 0.22μF | 50V,X7R,±10%,0603(1608) |
| 2 | C26,C33 | CGA3E2X7R1H102K080AA | TDK | 1000pF | 50V,X7R,±10%,0603(1608) |
| 1 | C27 | CGA3E2C0G1H822J080AA | TDK | 8200pF | 50V,C0G,±5%,0603(1608) |
| 1 | C28 | CGA3E2C0G1H561J080AA | TDK | 560pF | 50V,C0G,±5%,0603(1608) |
| 2 | C29,C30 | CGA3E2C0G1H101J080AA | TDK | 100pF | 50V,C0G,±5%,0603(1608) |
| 1 | C32 | CGA3E2X7R1H223M080AA | TDK | 0.022μF | 50V,X7R,±15%,0603(1608) |
| 1 | C34 | C1608X5R1E475M080AC | TDK | 4.7μF | 25V,X5R,±20%,0603(1608) |
| 1 | CE1 | UCDH101MCL6GS | Nichicon | 100μF | 50V,±20%,0.36Ωmax,Φ10 |
| 1 | CE2 | APXT100ARA391MF80G | Chemi-con | 390μF | 10V,±20%,22mΩmax,Φ6.3 |
| **Diode** | | | | | |
| 1 | D1 | RB510SM-40T2R | ROHM | - | 40V,100mA,0603(1608) |
| 1 | D2 | RB500SM-30T2R | ROHM | - | 30V,100mA,0603(1608) |
| 1 | D3 | 1SS355VMTE-17 | ROHM | - | 80V,100mA,1005(2513) |
| 2 | ZD1,ZD2 | EDZVT2R6.2B | ROHM | - | 6.2V,5mA,150mW, 0603(1608) |
| **Transistor** | | | | | |
| 1 | TR1 | 2SA2029T2LR | ROHM | - | -50V,150mA,0505(1211) |
| 2 | FET1,FET2 | RS6L090BGTB1 | ROHM | - | 60V,90A,4.7mΩmax,2024(4960) |
| **Inductor** | | | | | |
| 1 | L1 | XAL1010-153MED | Coilcraft | 15μH | 60V,9.9A,18.6mΩmax,±20%,(10.0 x 11.3) |
| **LED** | | | | | |
| 1 | LED1 | SML-D13U8WT86 | ROHM | - | RED,2.1V,20mA,52mW,0603(1608) |
| 1 | LED2 | SML-D12P8WT86 | ROHM | - | GRN,2.2V,20mA,54mW,0603(1608) |
| **Others** | | | | | |
| 1 | J3 | HIF3FC-14PA-2.54DSA(71) | Hirose Electric | - | 200V,1A,IMD14-2.54-H9.3-HIF3FC_DSA,200Vac,1A |
| 2 | JP_LDO,JP_12V | 61300211121 | Wurth Elektronik | - | 250V,3A,2.54,5.08*2.54 |
| 2 | JP_Loop,JP_REG | 61300311121 | Wurth Elektronik | - | 250V,3A,2.54,7.62*2.54 |
| 1 | SW_RC | ATE1E-2M3-10-Z | Nidec Copal Electronics | - | ON-OFF-ON,2.54-ATE1,60V,50mA,0.4VA |
| 2 | J1,J2 | XW4E-02C1-V1 | Omron | - | 250V,13.5A,5.08-XW4E,250V,13.5A |
| 1 | FT234x | AE-FT234X | AKIZUKI DENSHI TUSHO | - | 5V, 2.54, FT234XD |

## 11 Reference Application Data

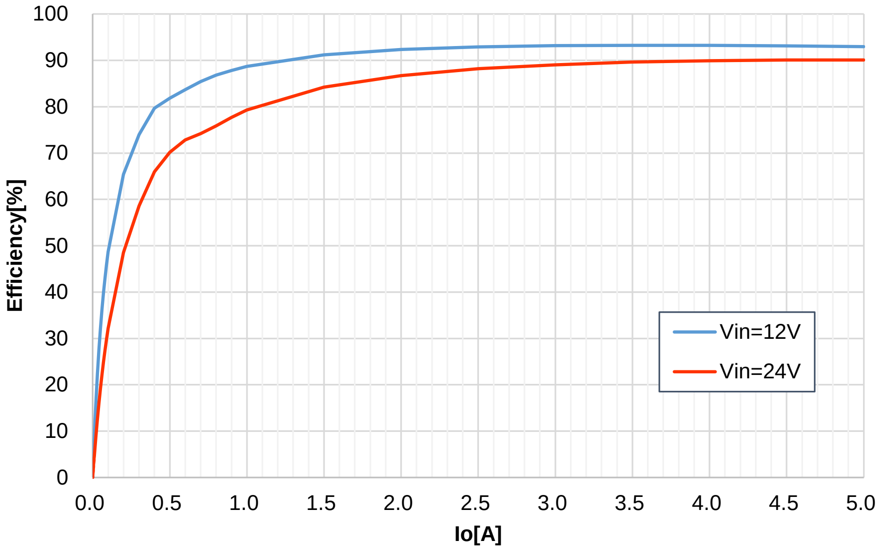
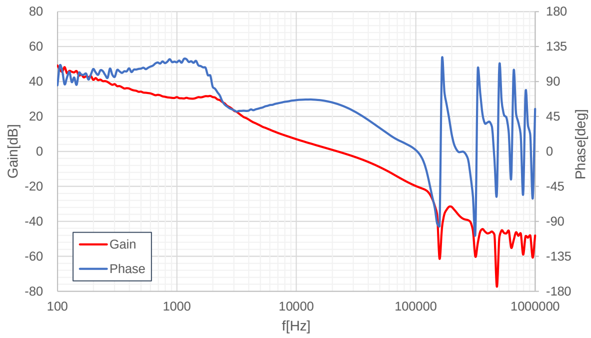


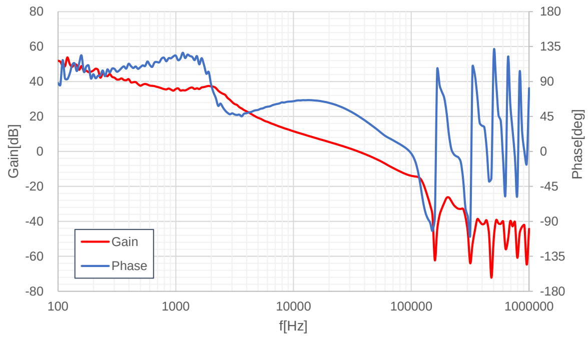

Figure 11-1. Efficiency vs Io




*Measure with OSC level within 5 to 20mVpeak

Figure 11-2. Frequency Characteristics

(Vin=12V, Vo=5V, Io=5A, OSC:20mVpeak)




*Measure with OSC level within 5 to 20mVpeak

Figure 11-3. Frequency Characteristics

(Vin=24V, Vo=5V, Io=5A, OSC:20mVpeak)

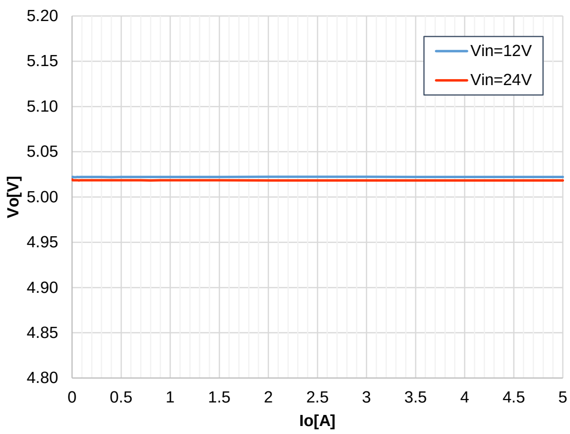



Figure 11-4. Load Regulation

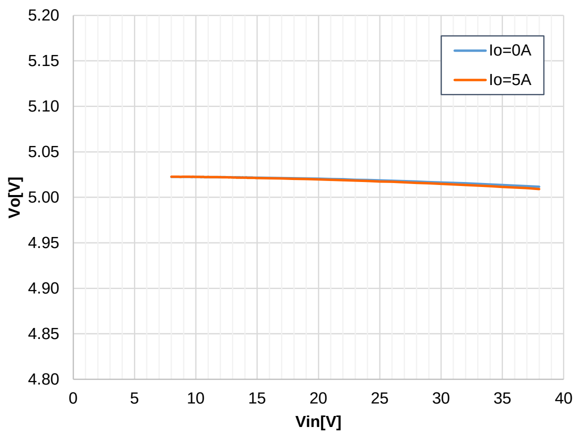



Figure 11-5. Line Regulation

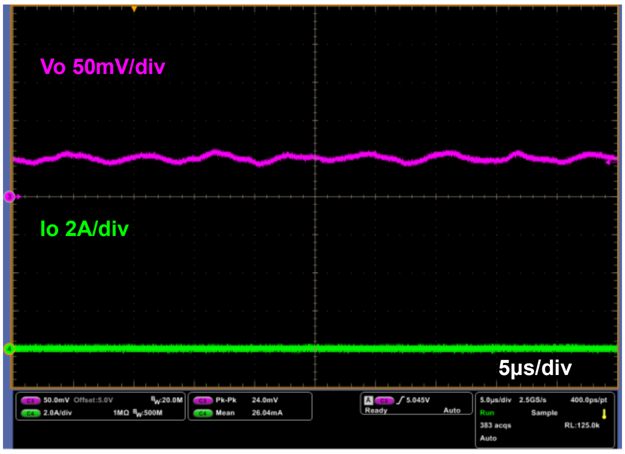



Figure 11-6. Output Ripple Voltage
(Vin=12V, Vo=5V, Io=0A)

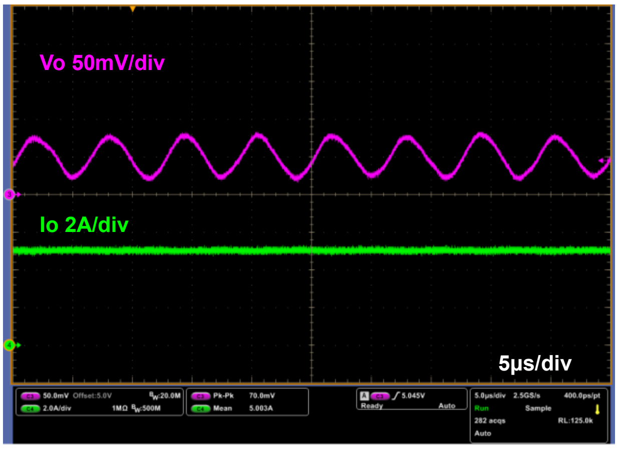



Figure 11-7. Output Ripple Voltage
(Vin=12V, Vo=5V, Io=5A)

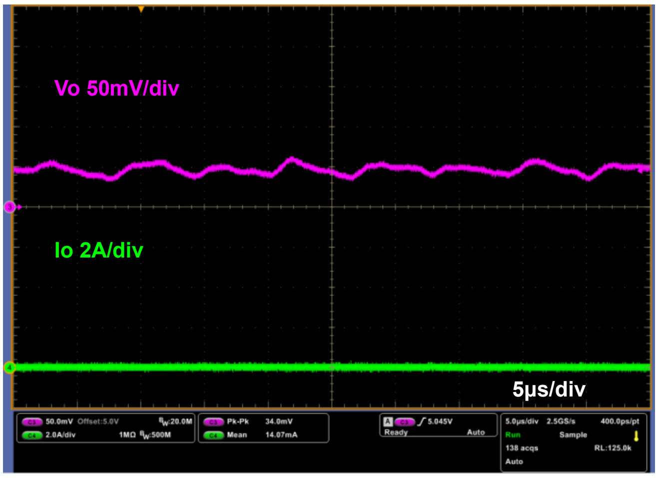



Figure 11-8. Output Ripple Voltage
(Vin=24V, Vo=5V, Io=0A)

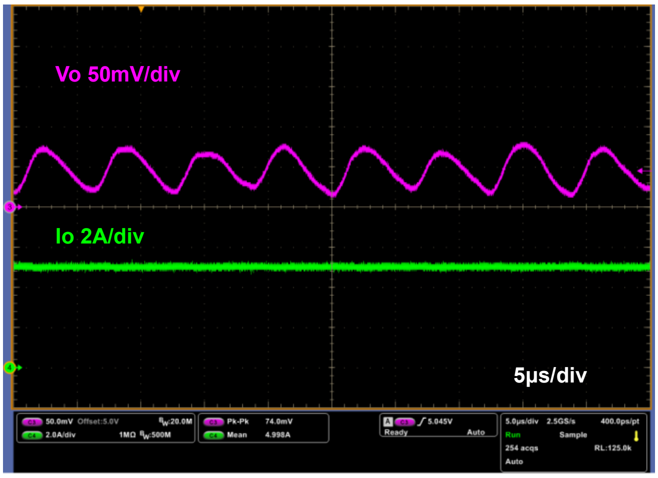



Figure 11-9. Output Ripple Voltage
(Vin=24V, Vo=5V, Io=5A)

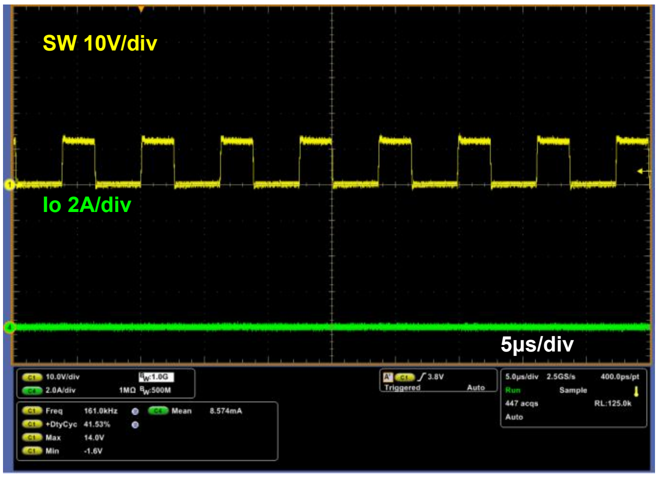



Figure 11-10. Switching Waveform
(Vin=12V, Vo=5V, Io=0A)


Figure 11-11. Switching Waveform
(Vin=12V, Vo=5V, Io=5A)

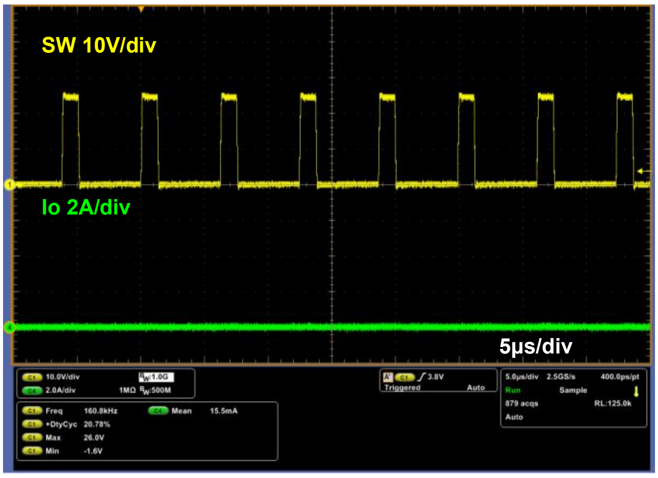



Figure 11-12. Switching Waveform
(Vin=24V, Vo=5V, Io=0A)


Figure 11-13. Switching Waveform
(Vin=24V, Vo=5V, Io=5A)

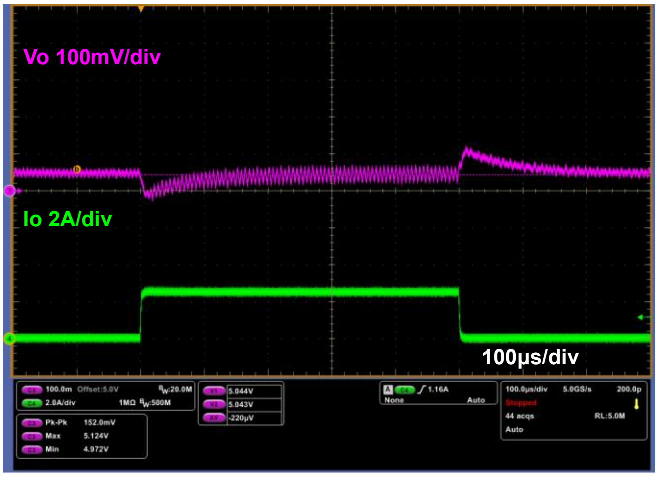



Figure 11-14. Load Transient
(Vin=12V, Vo=5V, Io=0A⇔2.5A, 1A/µs)

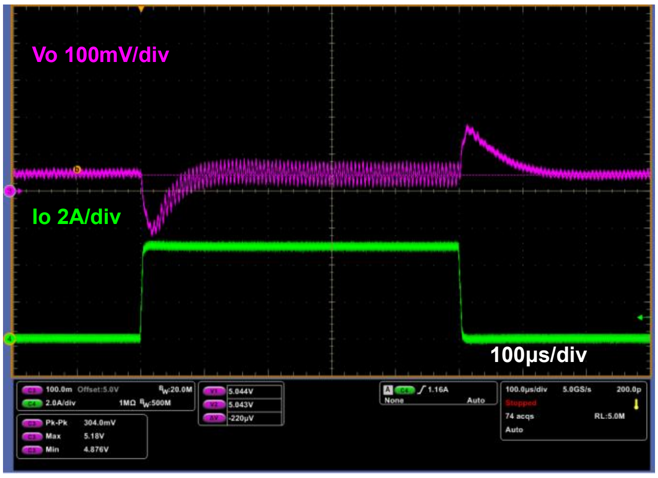



Figure 11-15, Load Transient
(Vin=12V, Vo=5V, Io=0A⇔5A, 1A/µs)

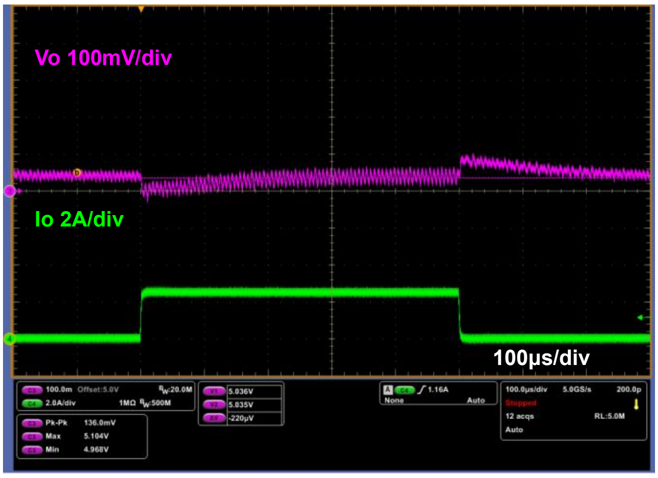



Figure 11-16. Load Transient
(Vin=24V, Vo=5V, Io=0A⇔2.5A, 1A/µs)

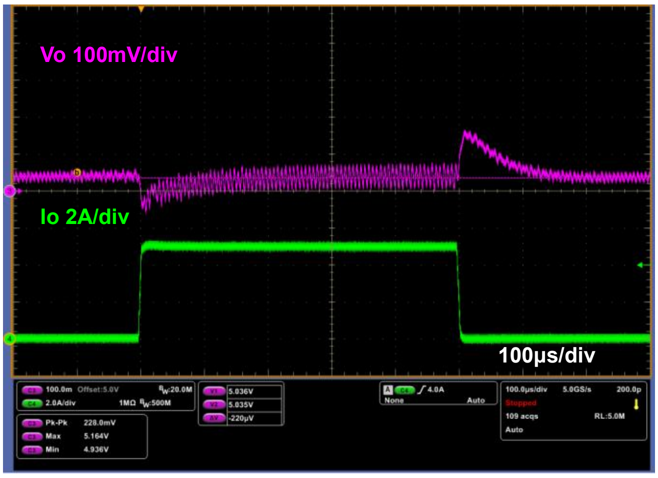



Figure 11-17. Load Transient
(Vin=24V, Vo=5V, Io=0A⇔5A, 1A/µs)

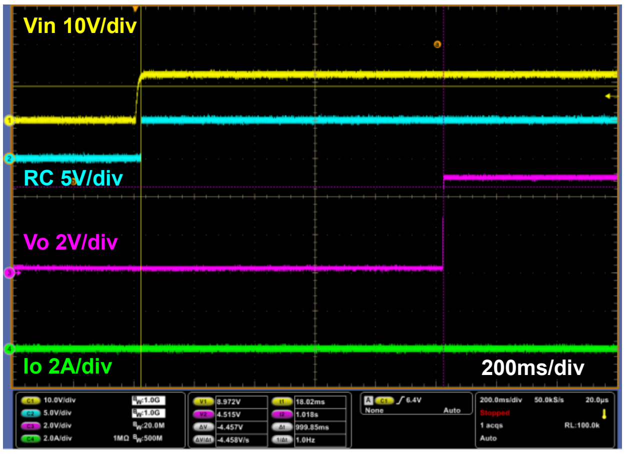



Figure 11-18. Startup Waveform
(Vin=0→12V, Vo=5V, Io=0A, RC=open)

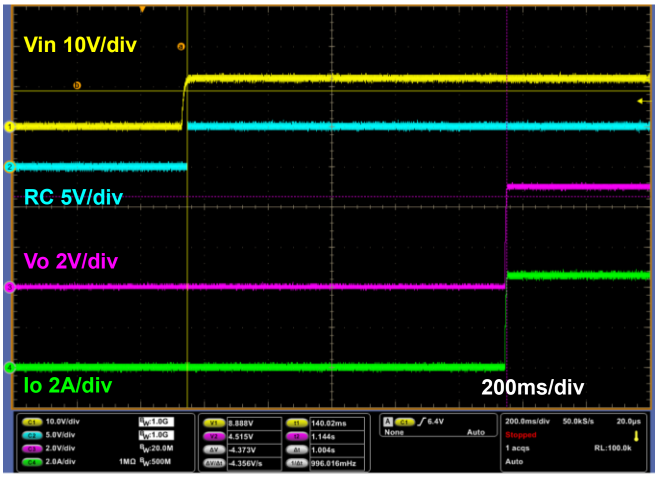



Figure 11-19. Startup Waveform
(Vin=0→12V, Vo=5V, Io=5A, RC=open)

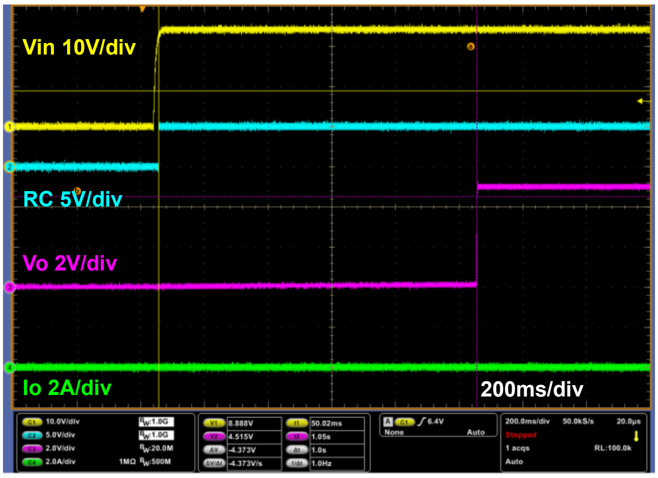



Figure 11-20. Startup Waveform
(Vin=0→24V, Vo=5V, Io=0A, RC=open)

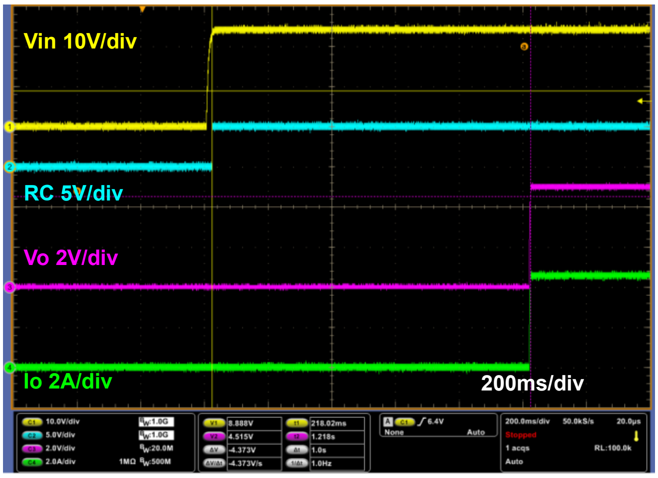



Figure 11-21. Startup Waveform
(Vin=0→24V, Vo=5V, Io=0A, RC=open)

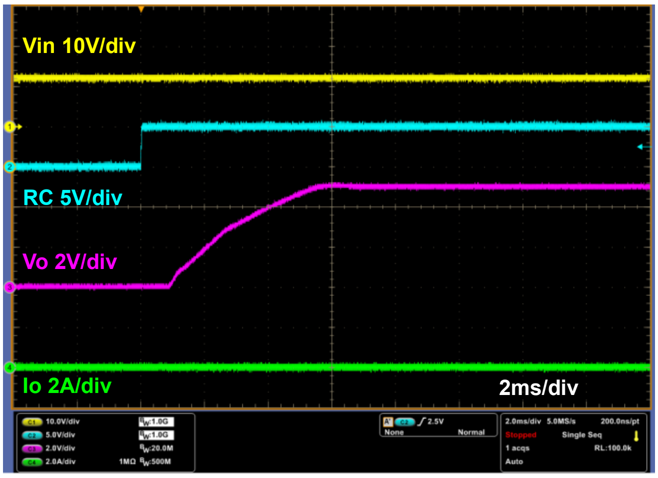



Figure 11-22. Startup Waveform
(Vin=12V, Vo=5V, Io=0A, RC=L→H)

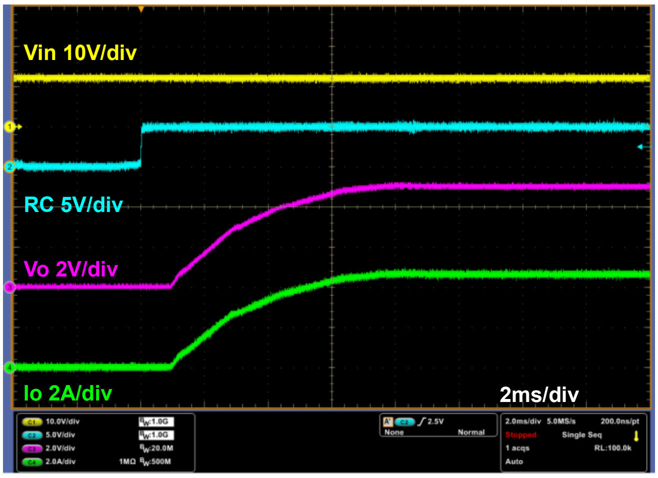



Figure 11-23. Startup Waveform
(Vin=12V, Vo=5V, Io=5A, RC=L→H)

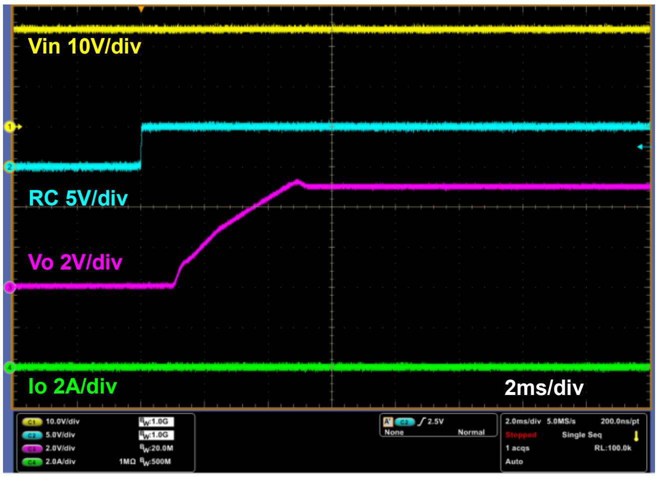



Figure 11-24. Startup Waveform
(Vin=24V, Vo=5V, Io=0A, RC=L→H)

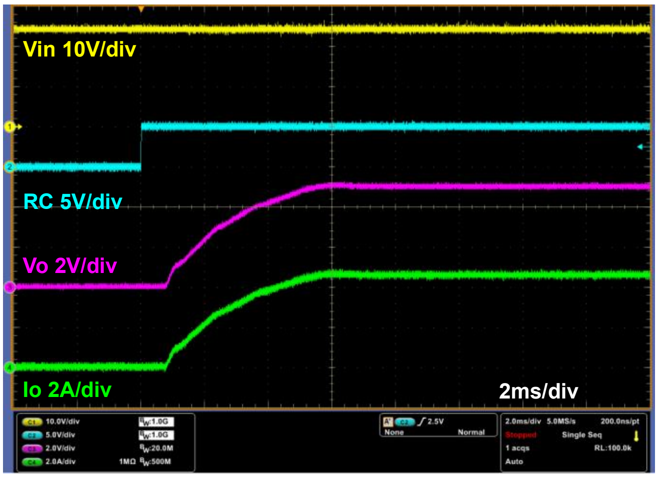



Figure 11-25. Startup Waveform
(Vin=24V, Vo=5V, Io=5A, RC=L→H)

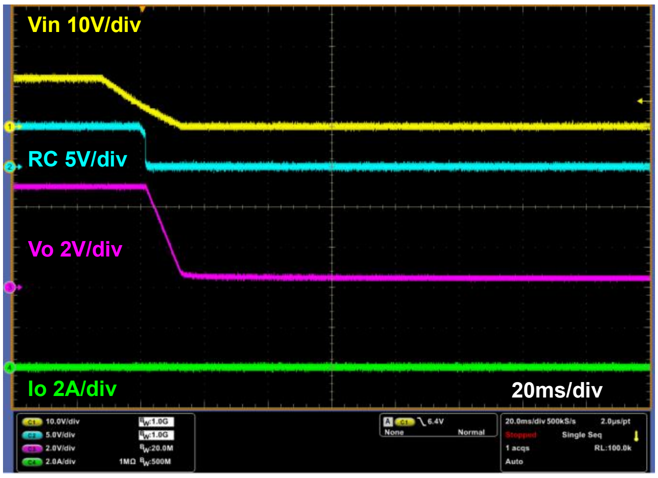



Figure 11-26. Stop Waveform
(Vin=12→0V, Vo=5V, Io=0A, RC=open)

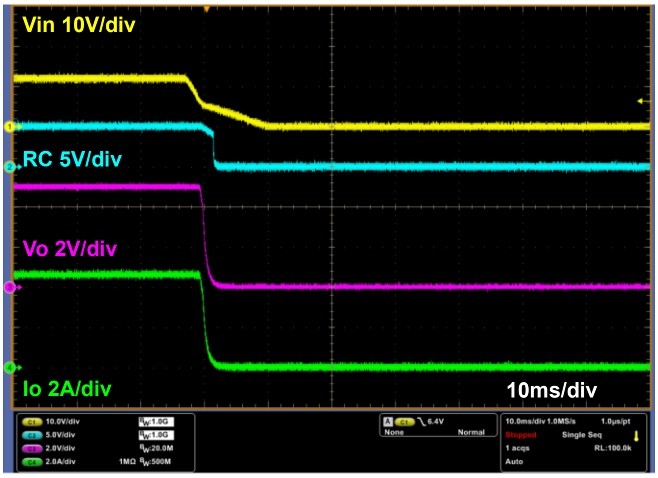



Figure 11-27. Stop Waveform
(Vin=12→0V, Vo=5V, Io=5A, RC=open)

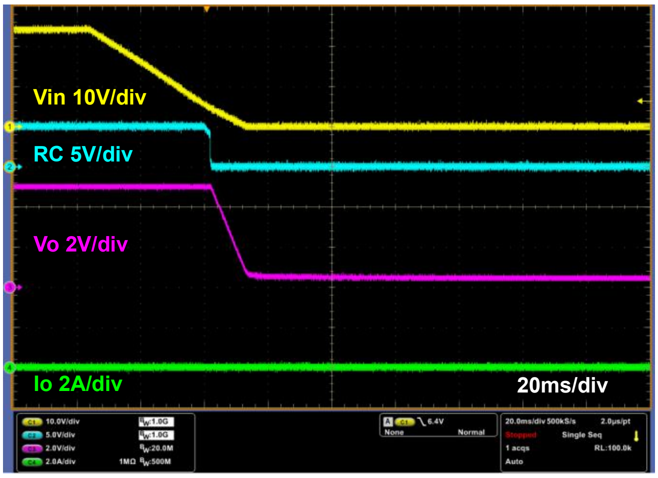



Figure 11-28. Stop Waveform
(Vin=24→0V, Vo=5V, Io=0A, RC=open)

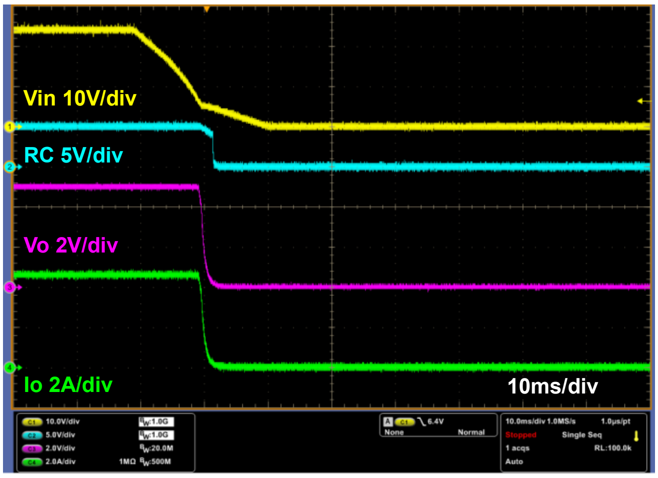



Figure 11-29. Stop Waveform
(Vin=24→0V, Vo=5V, Io=5A, RC=open)

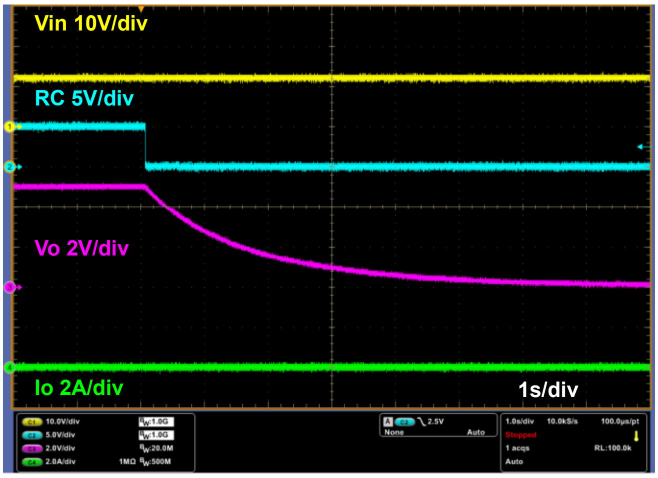



Figure 11-30. Stop Waveform
(Vin=12V, Vo=5V, Io=0A, RC=H→L)

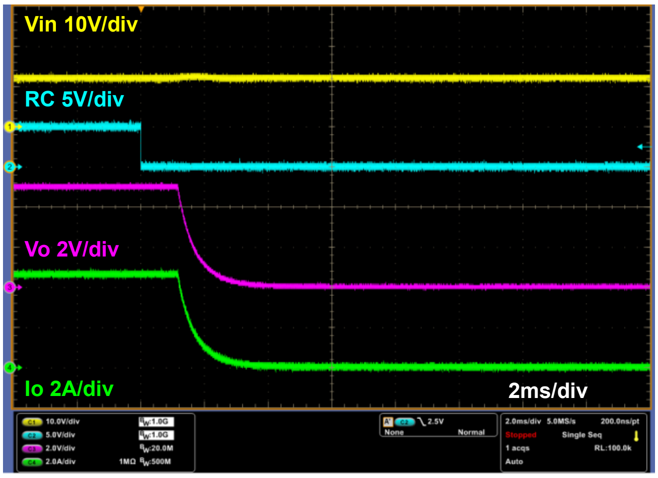



Figure 11-31. Stop Waveform
(Vin=12V, Vo=5V, Io=5A, RC=H→L)

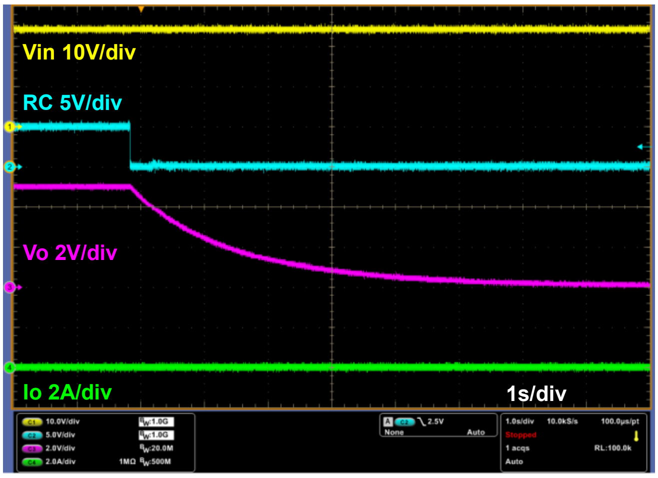



Figure 11-32. Stop Waveform
(Vin=24V, Vo=5V, Io=0A, RC=H→L)

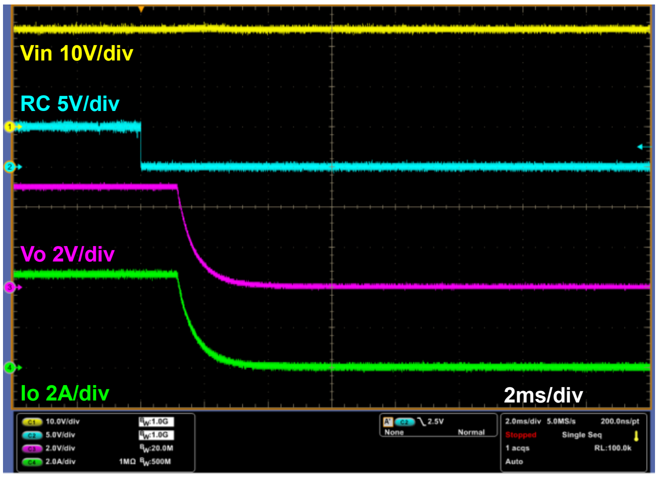



Figure 11-33. Stop Waveform
(Vin=24V, Vo=5V, Io=5A, RC=H→L)

## 12 References


[1] 66AN145E, Rev001, Analog-Digital hybrid control innovating switching power design

[2] FEDL62Q2045-01, ML62Q2033/2035/2043/2045 datasheet

[3] FEUL62Q2045-03, ML62Q2033/2035/2043/2045 User’s Manual

[4] 66AN147E, Rev.001, Operating system for switching power control MCU “RMOS”

[5] TSZ02201-0BDB0A400100-1-2 Rev.001, For Automotive 45V 150mA Fixed/Adjustable Output Nano Cap™ LDO Regulators BD9xxN1-C Series datasheet

[6] TSZ02201-0RAR0G200370-1-2 Rev.001, High Speed Low Voltage Operation CMOS Operational Amplifiers BU7481G BU7481SG datasheet

[7] TSZ02201-0Q2Q0A800840-1-2, Rev.002, High Frequency High-Side and Low-Side Driver BD2320EFJ-LA datasheet

[8] 66AN149E, Rev.001, Serial communication of RMOS and GUI developing manual

## Revision History

| Date | Revision Number | Description |
|---|---|---|
| 10. May.2024 | 001 | Initial release. |
| 31. Oct. 2024 | 002 | p.12 Add description of 4.14 LED indicator.<br>p.17 Add measurement condition and comment in Figure 11-2 and 11-3. |

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2) ROHM products are designed and manufactured for use in general electronic equipment and applications (such as Audio Visual equipment, Office Automation equipment, telecommunication equipment, home appliances, amusement devices, etc.) or specified in the datasheets. Therefore, please contact the ROHM sales representative before using ROHM products in equipment or devices requiring extremely high reliability and whose failure or malfunction may cause danger or injury to human life or body or other serious damage (such as medical equipment, transportation, traffic, aircraft, spacecraft, nuclear power controllers, fuel control, automotive equipment including car accessories, etc. hereafter referred to as Specific Applications). Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses, or losses incurred by you or third parties arising from the use of ROHM Products for Specific Applications.

3) Electronic components, including semiconductors, can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against physical injury, and damage to any property, which a failure or malfunction of products may cause.

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