LogiCoA™ Power Solutions

Analog-Digital Hybrid Power Supply Synchronous Buck DCDC Converter Operating Instructions

(12V→5V, 5A)

Introduction

LogiCoA™ Power is a solution adopting analog-digital hybrid control to a switching power supply. This application note describes LogiCoA001-EVK-001 as synchronous buck DCDC converters (buck converters) using LogiCoA™ power solutions.

This document first describes the features of LogiCoA™ power solution and the buck converter using analog-digital hybrid control. Next, we explain the operating conditions of LogiCoA001-EVK-001 and the operations of each block of that. We also explain how to control the power supply by software. For LogiCoA001-EVK-001, refer to the user's guide [1], too.

“LogiCoA™” is a trademark or a registered trademark of ROHM

Table of Contents

1 Overview of LogiCoA™ Power Solution

Figure 1-1 shows the overview of LogiCoA™ Power Solution. LogiCoA™ Power is a solution adopting analog-digital hybrid control to a switching power supply and consists of 3 elements, (1) Microcontroller for Power Supply Control (LogiCoA™ Microcontroller) ML62Q203x/ML62Q204x (hereinafter referred to ML62Q20xx group), (2) Operating System for Power Supply Control Microcontroller, RMOS, and (3) Power Supply Application. Refer to the explanation application note [2] for detail information of analog-digital hybrid control.

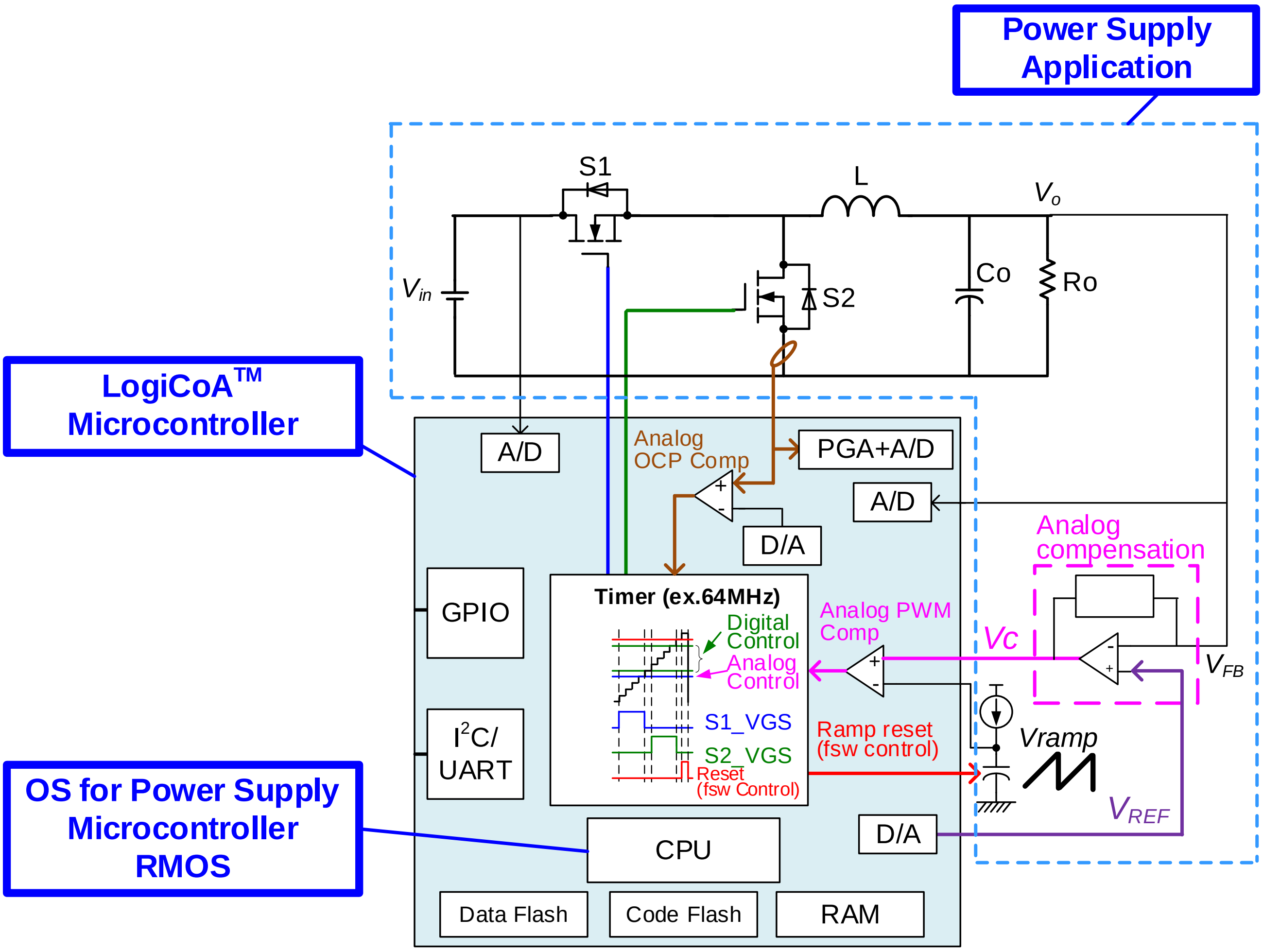

Figure 1-1. System overview of LogiCoA™ Power Solution

(1) Microcontrollers for Power Supply Control (LogiCoA™ Microcontroller)

LogiCoA™ Microcontrollers are suitable ones for power supply control with those analog-digital hybrid control is adopted and ML62Q2033/2035 and ML62Q2043/2045 are released. (at the time of this document's release) On LogiCoA001-EVK-001, ML62Q2035 is mounted. Refer to 4.2 MCU, the datasheet of ML62Q2033/2035/2043/2045 [3] and the user's manual of ML62Q2033/2035/2043/2045 [4] for more detail information about ML62Q2035.

(2) Operating System for Power Supply Control Microcontroller RMOS (**R**eal time **M**icro **O**perating **S**ystem)

RMOS is a multitask and real-time operating system developed to control switching power supplies and operates on ML62Q20xx group. Refer to the explanation application note [5] for more detail information about RMOS.

(3) Power Supply Application

Power Supply Applications are application circuits correspond to each power supply topology. On LogiCoA001-EVK-001, external components such as LDO, gate driver, operational amplifier, MOSFET, inductor and so on are mounted as an application circuit of buck converter.

2 Features of Analog-Digital Hybrid Control Buck Converter with LogiCoA™ MCU

Figure 2-1 shows the features of a buck converter with analog-digital hybrid control.

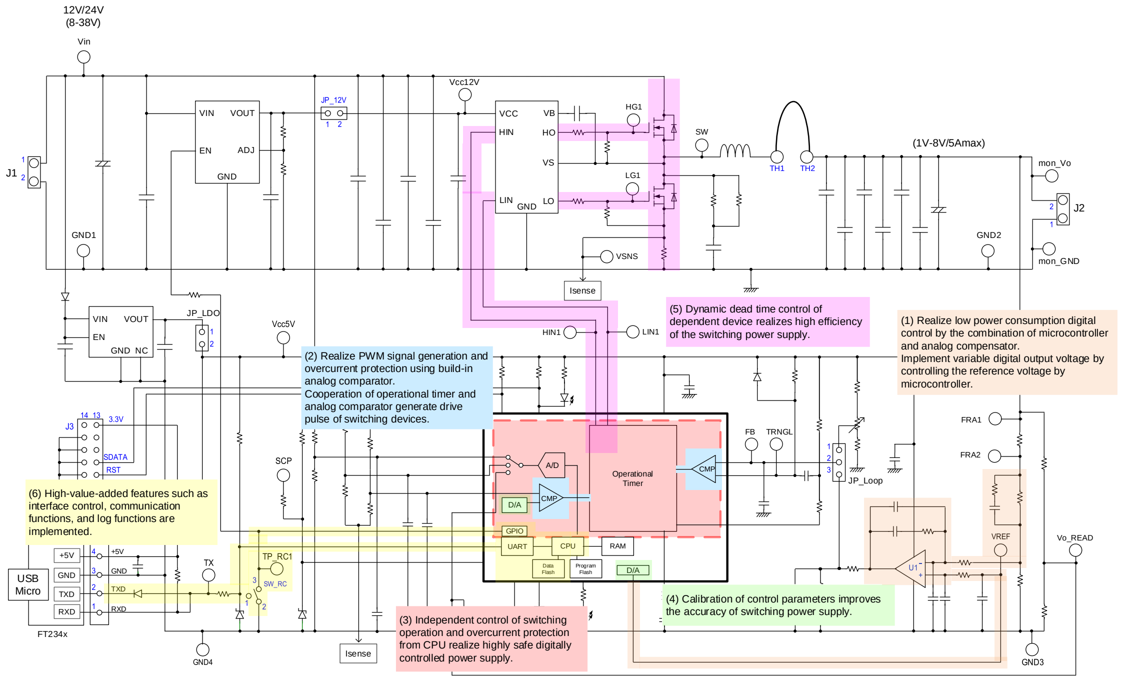

Figure 2-1. Features of Analog-Digital Hybrid Control Buck Converter

(1) Digital control and digital output voltage setting using an analog compensator and low-power microcontroller

The control circuit of switching power supply is configured using an analog compensator for output voltage control and with LogiCoA™ MCU ML62Q2035(CPU clock; 16MHz, timer clock; 64MHz). Since high power consumption devices such as DSP are not used, the power consumption of the control circuit can be reduced.

The output voltage control is performed by an analog compensator and the reference voltage VREF applied to the analog compensator is generated by the MCU D/A converter. Therefore, the output voltage setting of the switching power supply can be controlled by the MCU.

(2) Cooperation of built-in analog comparator and operational timer realizes switching device drive pulse generation and overcurrent protection

ML62Q2035 includes operational timers (10 outputs, controlling up to 10 power devices) optimized to generate gate drive signals for power devices, analog comparators (3 channels) those can be used for PWM signal generation and overcurrent protection circuit, and D/A converters (2 channels) those can be used as a reference voltage signal. The operational timer is configured to allow free setting of inter-timer coordination operation, timer-comparator coordination operation, timer-external inter-signal coordination operation, and phase tracking operation, allowing control of various power supply circuit topologies.

For PWM control signal, configure the built-in analog comparator in MCU to operate as a PWM comparator. PWM signal is generated by inputting a triangle wave to PWM comparator similar to analog control. The triangle wave can be generated using an operational timer to control the on-timing (switching frequency) of the switching device from MCU. In addition, since the ON Duty (pulse width of PWM signal) of the switching device is determined by analog control, the resolution of the switching pulse becomes infinite (in full digital control, the switching pulse has a finite resolution because it is determined by the resolution of the timer). Moreover, the maximum duty limit of the switching device can also be controlled from MCU.

For overcurrent protection, an analog comparator built-in the MCU is set to operate as an overcurrent protection comparator. By connecting a D/A converter built-in the MCU to the overcurrent protection comparator, the overcurrent protection setting can be controlled from the MCU.

(3) Switching operation and overcurrent protection independent from CPU realize highly safe digitally controlled power supply

Operational timers, comparators, and D/A converters and so on in the ML62Q2035 continue to operate independently of CPU after they are set once. So, even if CPU is stopped, protective operations such as overcurrent protection continue to operate, making it possible to create a highly safe digitally controlled power supply.

In analog-digital hybrid control, the output voltage control is controlled by an analog compensator. Therefore, even if CPU is stopped, the output voltage immediately before CPU is stopped is output.

(4) Calibration of control parameters improves the accuracy of switching power supply

ML62Q2035 controls various control parameters of the switching power supply with a microcontroller so that the change in characteristics due to "component variation" can be corrected by software.

【Control parameter example】

・Switching frequency	･･･ Controlled by the cycle setting of the operational timer
・Max. duty limit of switching device	･･･ Controlled by the pulse width setting of the operational timer
・Dead time of dependent device	･･･ Controlled by setting rise point of the operational timer
・Start/stop voltage	･･･ Controlled by acquiring input-voltage with A/D converters
・Preset output voltage	･･･ Controlled the reference voltage to the analog compensator by D/A converters.
・Overcurrent protection setting	･･･ Controlling the reference voltage to the comparator with D/A converters

(5) Dynamic dead time control of the dependent device realizes high efficiency of the switching power supply

The operational timer of ML62Q2035 has functions to detect the falling edge of the switching device, to start counting operation of the timer and to control the timing from the start of the timer counter until the timer output turns to the high level, so the dead time can be controlled. In addition, the microcontroller monitors the input voltage, the current of the switching device, the output voltage, etc., and can dynamically optimize the dead time for the state of the power supply, thus maximizing the efficiency of the power supply circuit. (At this moment of this document is released, dynamic dead time optimization is not implemented.)

(6) High-value-added features such as interface control, communication functions, and log functions

ML62Q2035 is a low-power microcontroller, but it has enough performances to realize high value-added functions such as interface control, communication functions, and log recording functions. In addition, an operating system for switching power supply control "RMOS" that realizes multitasking and real-time control is available for LogiCoA™ MCU. The communication and logging functions can be realized as standard functions of the operating system. (At this moment of this document is released, communication functions and log recording functions are not implemented.)

3 Operating Conditions

Following is the operating conditions of LogiCoA001-EVK-001.

(Unless otherwise specified Ta=25°C, Vin=12V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Voltage	Vin	7.5	12.0	38.0	V	
Control Block Supply Voltage(LDO)	Vcc5Vldo	4.9	5.0	5.1	V	Vcc5V=LDO Output
Control Block Supply Voltage(USB)	Vcc5Vusb	4.25	5.00	5.75	V	Vin=open, Vcc5V=USB VBUS Output
Driver Block Supply Voltage	Vcc12V	11.4	12.0	12.6	V	Vin>13V
Output Voltage	Vo	-	5.0	-	V	default setting, variable with serial communication
Output Voltage Range	Vo_r	1.0	-	8.0	V	variable with serial communication
Output Current	Io	-	-	5.0	A	
Switching Frequency	fsw	-	160	-	kHz	default setting
Switching Frequency Range	fsw_r	80	-	500	kHz	
Maximum Duty	Dmax	-	80	-	%	default setting
Soft Start Time	Tsstart	-	5	-	ms	Io=0A
Efficiency	η	-	92	-	%	Vo=5V, Io=5A
Startup Voltage	Vstart	-	9.0	-	V	Vin rise, default setting, variable with serial communication
Startup Voltage Range	Vstart_r	7.5	-	38.0	V	
Stop Voltage	Vstop	-	8.0	-	V	Vin fall, default setting, variable with serial communication
Stop Voltage Range	Vstop_r	7.5	-	38.0	V	
Startup Delay Time	Tstart	-	1000	-	ms	Vin rise, default setting
Startup Delay Time Range	Tstart_r	10	-	-	ms	
Input Voltage Protection	Vivp	-	38.0	-	V	default setting
Input Voltage Protection Range	Vivp_r	7.5	-	38.0	V	
Over Current Protection	Iocp	-	6.0	-	A	default setting
Over Current Protection Range	Iocp_r	2.5	-	8.0	A	
Output Low Voltage Protection	Vlvp	-	3.0	-	V	Vo fall, default setting
Output Low Voltage Protection Range	Vlvp_r	1.0	-	7.0	V	
Output Low Voltage Protection Mask Time	Tlvp	-	500	-	ms	Vo fall, default setting
Output Low Voltage Protection Mask Time Range	Tlvp_r	10	-	-	ms	
Output Over Voltage Protection	Vovp	-	6.0	-	V	Vo rise, default setting
Output Over Voltage Protection Range	Vovp_r	1.0	-	10.0	V	

4 Block Diagram and Description

Following pages describe the explanation for each block of LogiCoA001-EVK. In addition, the functions modified easily or tunable based on the firmware of this buck converter are picked up and described also. But note that the functional modifications described here is not always worked on the board of LogiCoA001-EVK-001.

4.1 Block Diagram

Figure 4-1 shows the application block diagram of LogiCoA001-EVK-001.

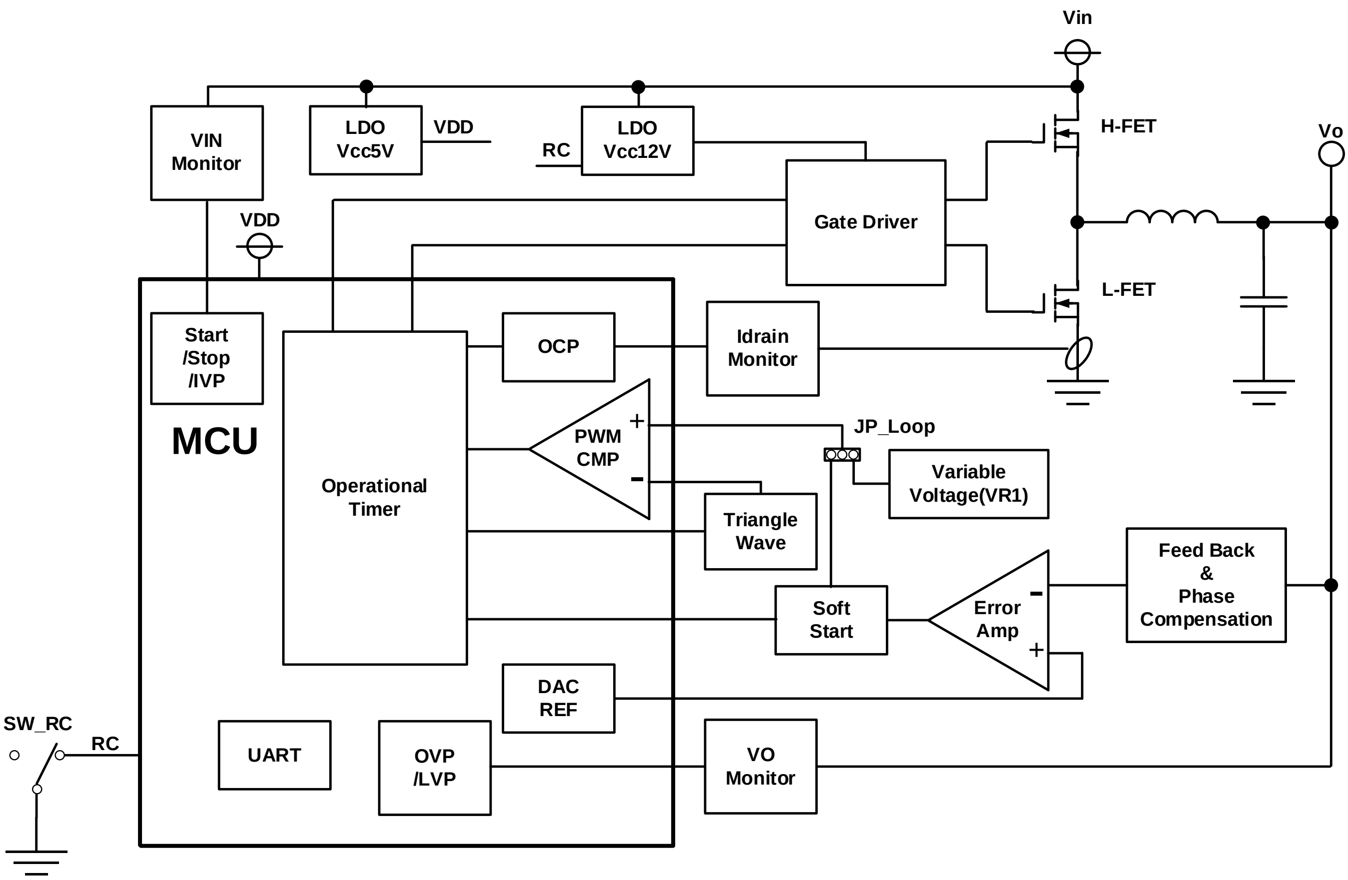

Figure 4-1. Application Block Diagram

4.2 MCU

On LogiCoA001-EVK-001, LogiCoA™ MCU ML62Q2035 is mounted as a power supply controller. VDD voltage of MCU is supplied from the control block power supply Vcc5V, and after supplied voltage becomes over 4.10V (typ) of the threshold voltage of POR, the microcontroller startup and RMOS starts its operation. Each pin's function of ML62Q2035 and selected function in LogiCoA001-EVK-001 is listed in Table 4-1.

Table 4-1. Pin list of ML62Q2035

Pin No.	Pin Name	1st Function	2nd Function	3rd Function	4th Function	5th Function	6th Function	7th Function	8th Function
		GPI/EXI	UART	I^2C	OTM	CMP/DAC	ADC	CMP	CMP/ADC
19	VDD	—	—	—	—	—	—	—	—
18	VSS	—	—	—	—	—	—	—	—
17	VDDL	—	—	—	—	—	—	—	—
16	P01	—	—	—	—	CMP0P	—	CMP0P /CMP1P	CMP0P
15	P02	—	—	—	OTO4B	CMP0M	—	CMP0M /CMP1M	CMP0M
14	P03	EXI0	—	—	OTO0A	—	—	—	—
13	P04	EXI1	—	—	OTO0B	—	—	—	—
12	P05	EXI1	—	—	OTO1A	—	—	—	—
11	P06	EXI2	—	—	OTO2A	—	—	—	—
10	P10	EXI3	RXD1, (/TXD1)	—	OTO3A	—	—	—	—
9	P11	—	—	—	OTO4A	CMP2P	—	CMP2P	CMP2P
8	P12	—	RXD0, (/TXD0)	SDAU0	OTO1B	—	—	—	—
7	P00/TEST0	EXI3	—	—	—	—	—	—	—
6	P13	EXI2	TXD0	SCLU0	OTO5B	—	AIN4	—	—
5	RESET_N	—	—	—	—	—	—	—	—
4	P14	—	—	—	—	CMP1P	AIN0	CMP1P /CMP2P	AIN0 /CMP1P
3	P15	—	—	—	—	CMP1M	AIN1	CMP1M /CMP2M	AIN1 /CMP1M
2	P16	—	—	—	—	CMP2M	AIN2	CMP2M	AIN2 /CMP2M
1	P17	EXI0	—	—	—	—	AIN3	—	—
20	P23	—	TXD1	—	OTO5A	DACOUT0	—	—	—

selected function in LogiCoA001-EVK-001

Table 4-2 listed the typical specifications of ML62Q2035. Refer to [3] and [4] for more detail information about ML62Q2035.

Table 4-2. Typical specifications of ML62Q2035

Part Number		ML62Q2035
CPU		16bit RISC CPU Core(nx-U16/100), Max operating frequency 16MHz
Memory		Code Flash: 32KB, Data Flash: 4KB(Erase Unit:128B), RAM: 2KB
Analog Comparator		3ch(asynchronous to clock), Response time: Max 100ns
Timer		16bit timer with PWM/Capture × 6 counters, 10 outputs
		Max 64MHz operation(Resolution 15.625ns)
AD Converter		12bit SA-ADC: 5ch
DA Converter		8bit, 2ch
Programmable Gain Amplifier		1ch, Gain Setting: 4 steps (×4/×8/×16/×32)
Serial I/F		I^2C×1, UART×2
I/O Port		I: 1, I/O: 15
External Interrupt		4
Other		Multiplication/Division Unit, Temperature Sensor, Power ON Reset
Clock	Low	Internal RC Oscillator: 32.768kHz ± 1.5%*
	High	PLL: 64MHz ± 1.5%*, CPU: 16MHz to 125kHz ± 1.5%*
		PWM/Capture: 64MHz to 500kHz ± 1.5%*
Current Consumption(CPU)		Stop: 80μA, Halt: 90μA, Active: 3.3mA@16MHz
Operating Supply Voltage		4.5V to 5.5V
Operating Temperature		Ta=-40°C to +105°C(Tj=115°C) (Absolute maximum ratings:Tjmax=125°C)
Package		TSSOP20

*: Ta=-20°C to +85°C

4.3 Control Block Power Supply

On LogiCoA001-EVK-001, a fixed 5V output LDO BD950N1WG-C is mounted as a power supply (Vcc5V) for control block (MCU and analog control circuit). BD950N1WG-C has standby control function, but in LogiCoA001-EVK-001, VIN pin and EN pin are shorted and so when Vin voltage is applied and VIN pin of BD950N1WG-C voltage is over UVLO rise voltage (typ 2.6V), Vcc5V turns on. Refer to the datasheet of BD9xxN1-C series [6] for more detail information about BD950N1WG-C.

4.4 Driver Block Power Supply

On LogiCoA001-EVK-001, a 12V output LDO BD900N1WG-C is mounted as a power supply (Vcc12V) of the gate driver to drive output FET. BD900N1WG-C has standby control function and can be controlled turning ON/OFF by a remote control switch described later. Refer to the datasheet of BD9xxN1-C series [6] for more detail information about BD900N1WG-C.

4.5 Remote Control Switch

LogiCoA001-EVK-001 has RC (RC: Remote Control) function for external turning ON/OFF control. DCDC operates as the setting below by turning the mechanical switch (SW_RC) connected P10 pin of ML62Q2035 to OPEN or short to GND. To avoid a false detection by noise, there are mask time of 150μs at RC=H detection and 1.25ms at RC=L. P10 pin is set as a GPIO with internal 40kΩ(typ) pulled-up. Refer to [3] about the threshold of operating state because it depends on input/output characteristics of ML62Q2035.

In the remote control switch block, ON/OFF logic of RC can be swapped by changing the firmware. Mask time is adjustable also. However, if ON/OFF logic of RC is swapped on LogiCoA001-EVK-001 board, DCDC does not operate because it reverses the standby control logic of the driver-part power supply Vcc12V.

Table 4-3. Operating state of Remote Control Switch

SW_RC	P10 pin	DCDC
OPEN	VDD	ON
GND SHORT	GND	OFF

4.6 Error Amplifier and Reference Voltage

Figure 4-2 shows the error amplifier and surrounding circuits. BU7481SG is mounted on as an error amplifier. As control block power supply Vcc5V is supplied, the error amplifier starts to operate but startup of the error amplifier output is controlled by the soft start circuit. Refer to the datasheet of that [7] for more detail information about BU7481SG.

The reference voltage of error amplifier Vo_REF is generated by the 8-bits DA converter built-in in the MCU (1.973V at VDD=5V). Output voltage Vo is calculated as following equation.

$$Vo = V_{O\_REF} \times \frac{R_{29} + R_{30} + R_{31}}{R_{31}}$$

Ex.) When Vo_REF=1.973V, R29=51Ω, R30=3.3kΩ and R31=2.2kΩ, output voltage is as below.

$$Vo = 1.973V \times \frac{51\Omega + 3.3k\Omega + 2.2k\Omega}{2.2k\Omega} \cong 4.9782V$$

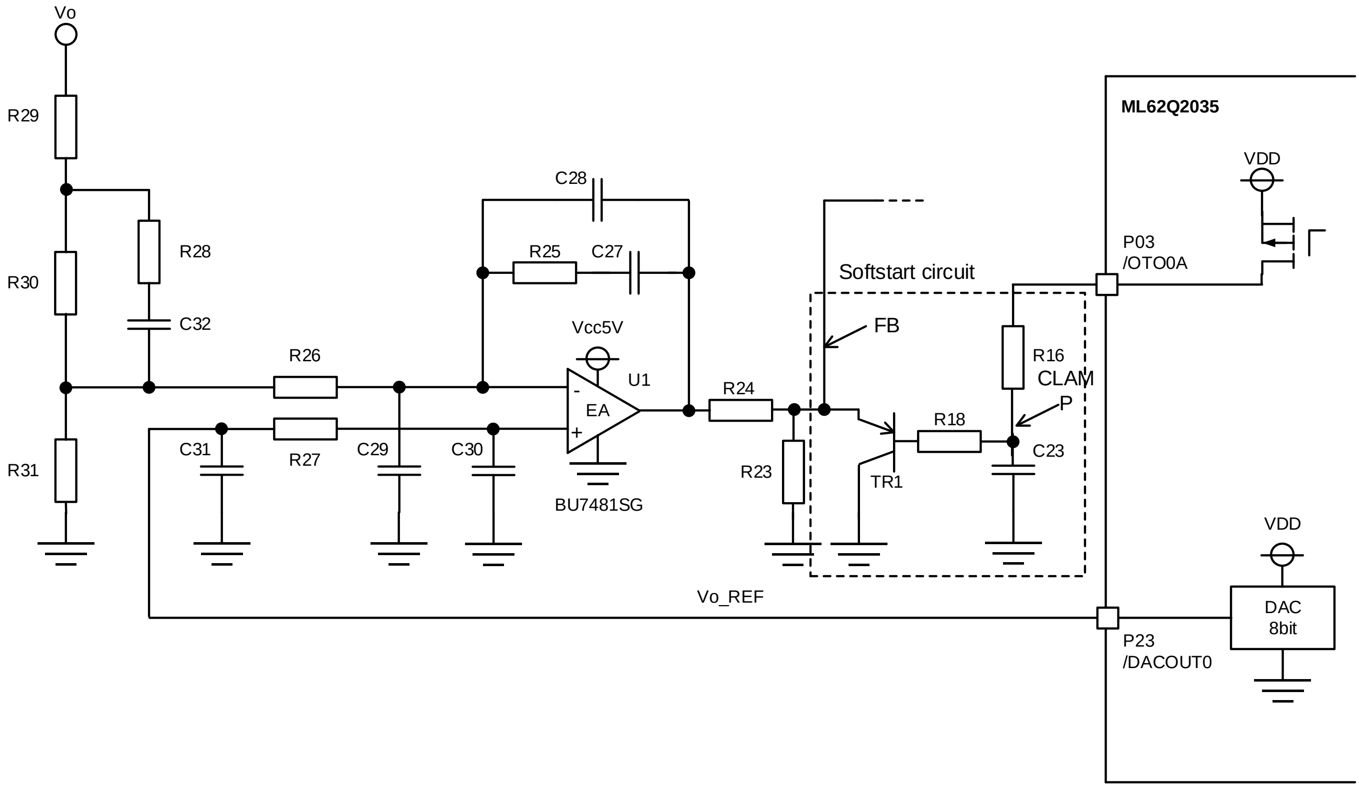

Figure 4-2. Error amplifier and surrounding circuits

Around the error amplifier block, the voltage of Vo_REF can be changed by changing the firmware. In LogiCoA001-EVK-001, the output voltage can be changed by changing the voltage of Vo_REF.

4.7 Soft Start

In LogiCoA001-EVK-001, to avoid an overshoot and rush current, output of the error amplifier (FB) is clamped while starting up, thus ramp up speed of DCDC output is controlled and starts softly.

The FB voltage is clamped by the CLAMP voltage + VBE of TR1 because the voltage generated at both ends of R18 can be considered minute due to R18=100Ω and TR1 base current. P03/OTO0A pin has been set as PMOS open drain, and while in startup, clamped voltage rise up slowly by controlling the ON duty of the PMOS. While the internal PMOS at P03/OTO0A pin is ON (outputting H), C23 is charged. While the PMOS is OFF, C23 remains uncharged and keep the voltage. For this reason, the rise rate of CLAMP is faster with higher ON Duty of PMOS and slower with lower ON Duty. At startup, ON Duty is stepwise decreased to gradually reduce CLAMP voltage (= FB voltage) rise rate and to suppress the steep rise of the output. In the steady state, the CLAMP voltage is equal to VDD and thus the FB voltage is not clamped.

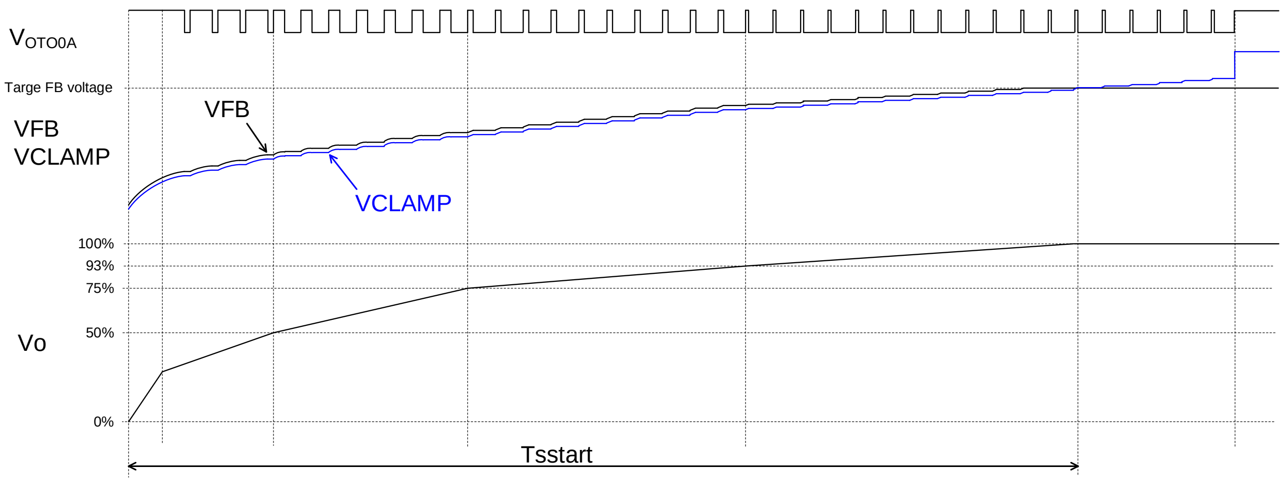

Figure 4-3. Soft start operation timing chart

In the soft start block, CLAMP voltage rise control (time/slope) can be changed by changing the firmware. In LogiCoA001-EVK-001, the soft start time can be changed by changing CLAMP rise control.

4.8 Triangle Waveform Generator and PWM Comparator

Figure 4-4 and 4-5 shows the triangle waveform generator and surrounding circuits, and timing chart. Triangle waveform is generated at P02/CMP0M pin by clock pulse output from P04/OTO0B pin. C26 is discharged when P04/OTO0B pin switches from the H output to the L output. While P04/OTO0B is outputting L, C26 is charged through R17 and TRNGL waveform rises. P01/CMP0P pin and P02/CMP0M pin have been set as an input of analog comparator and the build-in analog comparator operate as the PWM comparator to compare FB and TRNGL.

As shown in Figure 4-5, the frequency of clock pulse output from P04/OTO0B pin is the switching frequency of the DCDC converter fsw (160kHz typ). And while the output of the clock pulse is H, the voltage of TRNGL becomes also H, so the output of the PWM comparator is L. This leads that the L duty of the clock pulse is the Max Duty Dmax (80% typ) of the DCDC converter.

The triangle waveform generator can change the switching frequency and the maximum Duty of DCDC converters by changing the firmware.

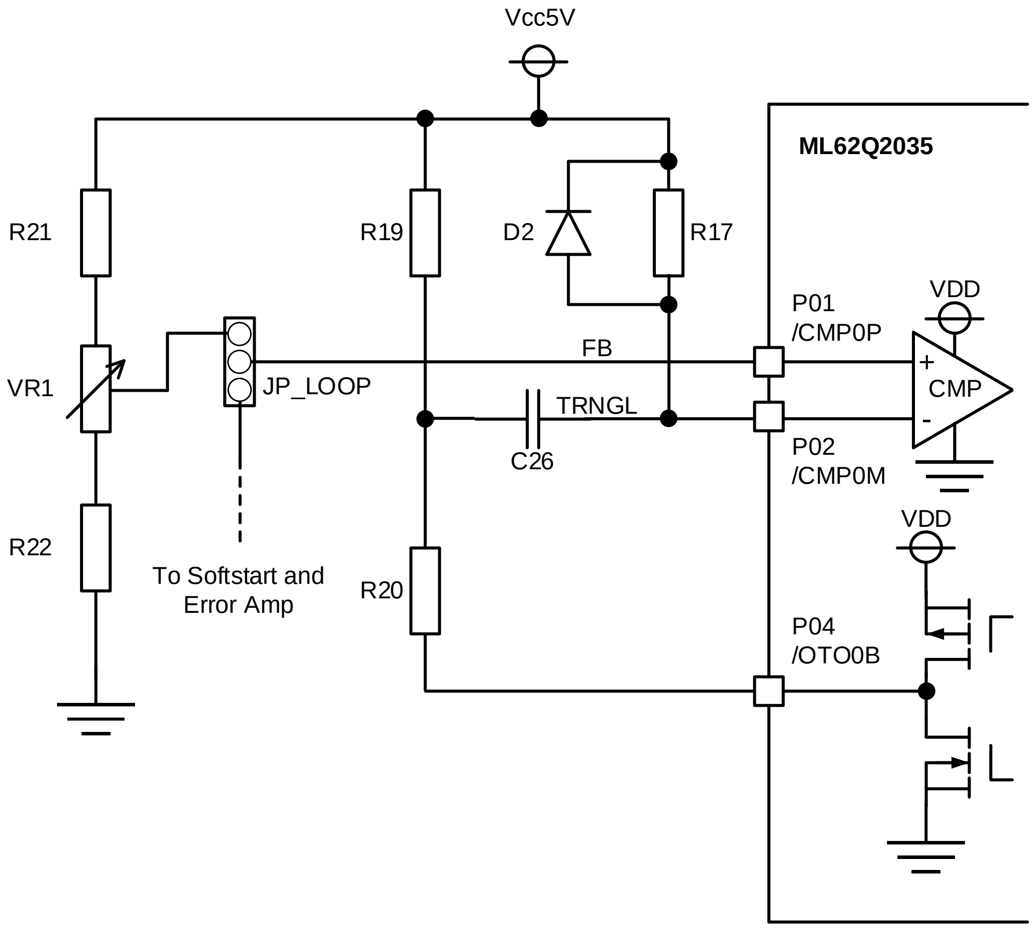

Figure 4-4. Triangle waveform generator and surrounding circuit

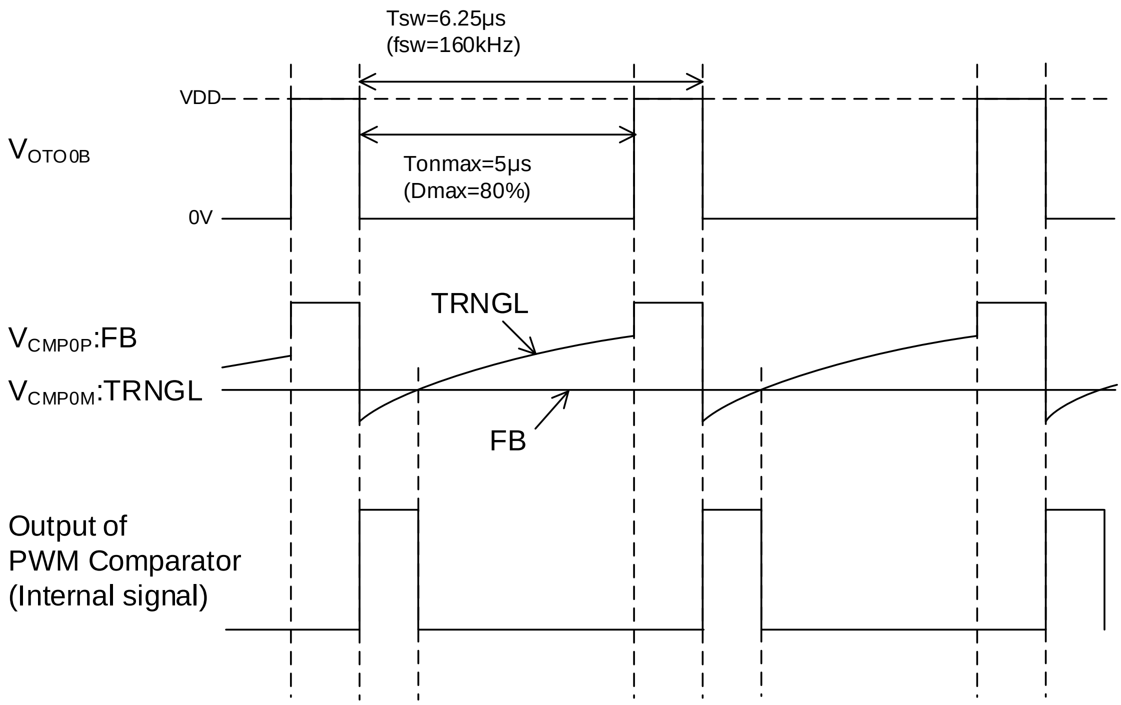

Figure 4-5. Triangle waveform generator timing chart

4.9 Volume Resistor for Open Loop Operation (for debug)

LogiCoA001-EVK-001 can be operated in open loop without feedback control for debugging. Open loop and closed loop operation can be exchanged by the jumper connection of JP_Loop (refer to Figure 4-1. Application Block Diagram and Figure 4-4. Triangle waveform generator and surrounding circuit.) When open loop operation is selected, the input voltage of the PWM comparator can be tuned using volume resistor VR1. The divided voltage from Vcc5V by R21 and 10kΩ volume resistor VR1 will be the FB voltage (0Ω is mounted on R22.)

4.10 Output Stage

In output stage, the control signals of H-side/L-side FET from the MCU level shifted by the gate driver drive output FETs, and stable voltage smoothed by the LC filter is supplied. BD2320EFJ-LA is mounted on as a gate driver. Refer to the datasheet of that [8] for more detail information of BD2320EFJ-LA.

4.11 Input Voltage Detection Block

Figure 4-6 shows the input voltage detection block. The divided Vin voltage by R6 and R7 is input to the P15/AIN1 pin of ML62Q2035, and the digital value of pin input voltage converted by the 12bits AD converter is obtained.

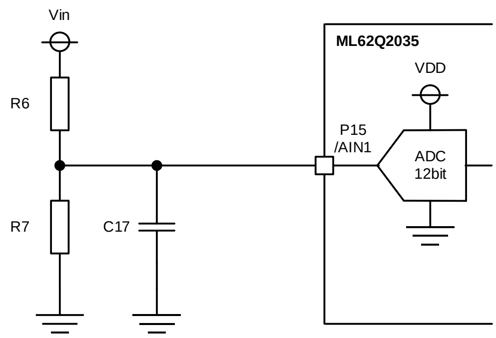

Figure 4-6. Input voltage detection block

4.11.1 Startup/Stop Voltage Check

In LogiCoA001-EVK-001, Vin input voltage is monitored by the input voltage detection block described above and when the voltage is over the startup voltage of 9V, DCDC startups after the 1s of the startup delay time. When the input voltage is below 8V, DCDC stops. For a noise reduction, there is a 150µs of mask time in voltage detection. When the input voltage falls below the start voltage, the count of the start voltage check mask time is reset. When the input voltage exceeds the stop voltage, the count of the stop voltage check mask time is reset.

In the start/stop voltage check block, the start and stop voltage threshold, mask time, and start delay time can be changed by changing the firmware.

4.11.2 Input Voltage Protection

LogiCoA001-EVK-001 has an input over voltage protection function (IVP: Input Voltage Protection). Vin input voltage is monitored by the input voltage detection block described above and when the voltage is over the detect voltage of 38V, the protection works and DCDC stops output switching. For a noise reduction, there is a 250µs of mask time in voltage detection. When the input voltage is below the detect voltage or the protection stops in the normal operation state, count of the mask time is reset. When protection works, DCDC stops latched, and restarts after turning on RC again in the condition that Vin input voltage is under the detection threshold voltage.

In the input voltage protection block, the threshold voltage and mask time of the detection can be changed by changing the firmware.

4.12 Output Voltage Detection Block

Figure 4-7 shows the output voltage detection block. The divided Vo voltage by R32 and R33 is input to the P14/AIN0 pin of ML62Q2035, and the digital value of pin input voltage converted by the 12bits AD converter is acquired.

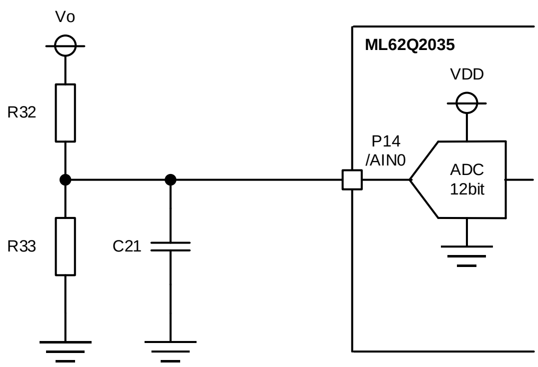

Figure 4-7. Output voltage detection block

4.12.1 Low Voltage Protection

LogiCoA001-EVK-001 has an output low voltage protection function (LVP: Low Voltage Protection). Vo output voltage is monitored by the output voltage detection block described above and when the voltage drops less than the detect voltage of 3.0V, timer count starts. When the output voltage remains below the detect voltage and 500ms has passed, protection works and DCDC stops output switching. The timer counter is incremented from the initial value by every 500µs, and when the output voltage becomes over the detect voltage while in timer counting, the counter value is decremented. When DCDC stops by the protection or RC, the timer counter is reset. When protection works, DCDC stops latched, and restart after turning on RC again.

In the low voltage protection block, the threshold voltage and mask time of the detection can be changed by changing the firmware.

4.12.2 Over Voltage Protection

LogiCoA001-EVK-001 has an output over voltage protection function (OVP: Over Voltage Protection). Vo output voltage is monitored by the output voltage detection block described above and when the voltage is over the detect voltage of 6.0V, the protection works, and DCDC stops output switching. For a noise reduction, there is a 250µs of mask time in voltage detection. When the output voltage drops less than the detect voltage in the normal operation state, count of the mask time is reset. When protection works the DCDC stops latched, and restart after turning on RC again.

In the over voltage protection block, the threshold voltage and mask time of the detection can be changed by changing the firmware.

4.13 Drain Current Detection Block

Figure 4-8 shows the drain current detection block. The drain current Id flows through low side FET, FET2, is converted to the voltage VSNS in the current sense resistor R5. VSNS divided from Vcc5V by R8, R9 and R10, R11, and added certain offset voltage to meet the input voltage range of AD converter/analog comparator, are input to P16/AIN2 pin and P11/CMP2P pin of ML62Q2035 each. By the built-in AD converter in P16/AIN2 pin, the digital value of the current is acquired and the built-in comparator in P11/CMP2P pin detect the overcurrent.

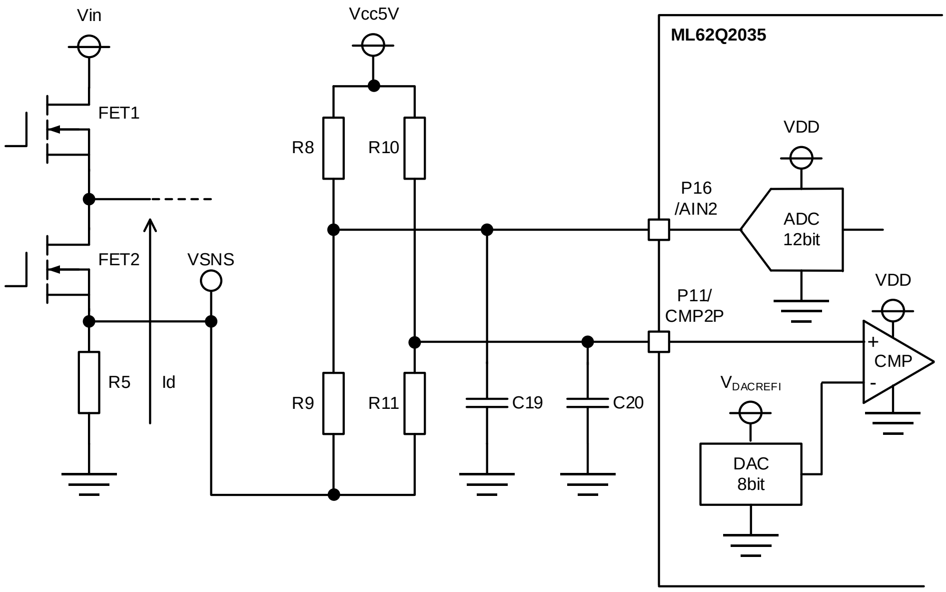

Figure 4-8. Drain current detection block

4.13.1 Over Current Protection

LogiCoA001-EVK-001 has a pulse-by-pulse over current protection function (OCP: Over Current Protection). The drain current of low side FET is monitored by the analog comparator in the drain current detection block described above. When the current exceeds the detect threshold value of 6.0A, protection works and turning off the FET. After the detection, DCDC restarts from protection automatically, but if the overload state continues, OCP is detected again.

In the over current protection block, the reference voltage of the analog comparator can be changed by changing the firmware. In LogiCoA001-EVK-001, the detected current can be changed by changing the reference voltage of the comparator.

5 Serial Communication

In LogiCoA001-EVK-001, modification of power supply control parameter and recording the operating log are capable of by a serial communication via the on-board USB-UART covert module from such as an external Windows PC. (Logging function is not implemented at the time of this document's release.) Refer to the explanation application note of communication function and GUI[9] for more detail information about the serial communication and communication commands.

6 Switching Power Supply Control by RMOS

In LogiCoA™ power supply solution, the operating system RMOS (RMOS; **R**eal time **M**icro **O**perating **S**ystem) for the switching power control microcontroller and the firmware described on RMOS for various power supply topologies are provided as a reference program, and the power supply is controlled by these softwares. The power control using RMOS is outlined below. For more information, refer to RMOS explanatory Application Notes [5].

6.1 State Transition Control

RMOS implements a function that controls the switching power supply using "state transition control." The operation states of switching power supplies can be classified into the following four operating states:

① Standby operation … The switching power supply is not outputting voltage (The input voltage is lower than the start voltage, and shalted by remote ON/OFF control)

② Start operation … A state in which the output voltage of the switching power supply rises from zero to a steady voltage

③ Normal operation … When the output voltage of the switching power supply outputs a steady voltage

④ Stop operation … State in which the output voltage of the switching power supply is stopped

Since the above operation states are independent in switching power supply operation, the control program can also be described independently for each operation state. Programs can be written without considering other operating states, so programs can be simplified and written. In addition, when describing a control program, the above operation state is further subdivided, and the program is modularized for the operation state of the power supply (state transition control module). Then, state transition control is performed to change (transition) the program module to be executed according to the state of the power supply.

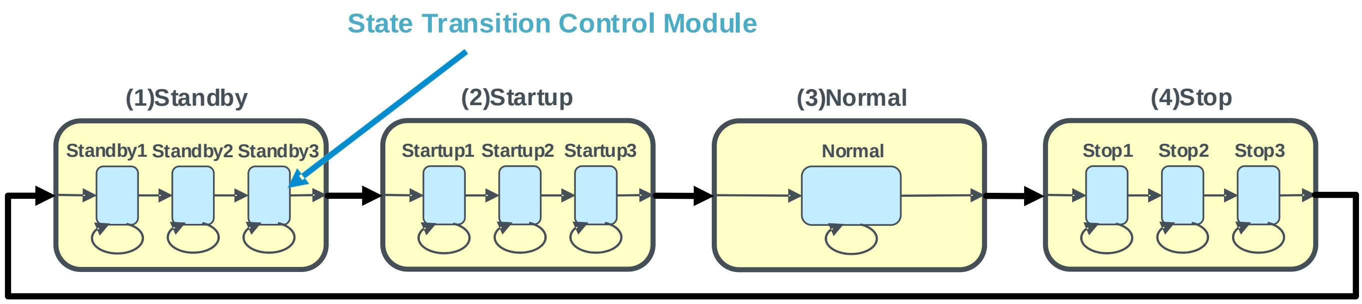

Figure 6-1. State transition control module

In RMOS, the state transition control module description area is prepared in advance (standby operation × 5, start operation × 5, normal operation × 2, stop operation × 5). The programmer can create a power control program by writing the program in RMOS status transition control module description area. One of the specified state transition control modules is executed every 50 μs in RMOS, and the state transition control module to be executed can be changed (transited) by issuing an instruction to RMOS according to the status of the power supply. RMOS also provides two sets of state transition control modules to control two types of switching power supplies simultaneously.

In RMOS, power supply control is performed by transitioning the execution of the state transition control module, so the configuration of the program is represented by the state transition diagram. The state transition diagram describes the operation, state transition conditions, and state transition destination of each state transition module. In developing a program, a state transition diagram is first created, and the operation of the power supply in each state is studied to prevent control missing or leakage.

6.2 State Transition Diagram of Buck Converter

Figure 6-2 shows the state transition diagram of LogiCoA001-EVK-001. As described in the section 6.1 “state transition control”, the operation state is divided into ① standby, ② start, ③ normal, and ④ stop. The top stage of Figure 6-2 is the ① standby, the second stage from the top is the ② start, the third stage is the ③ steady, and the bottom stage is the ④ stop. As shown in table 6-1, the standby, startup, and stop states have five state transition control modules, and the normal state has two modules, and one of the modules is executed in a cycle of 50μs. However, only for normal state operation, a module that is executed in a 50μs cycle and a module that is executed in a 500μs cycle operate in parallel. Each module judges and controls the transition to the next state or stagnation in the same state according to state variables and state flags such as input voltage, output voltage, and internal counter of the program dynamically acquired as described in the figure. State variables and state flags are listed in Section 6.3 "State Variables and State Flags".

Table 6-1. State transition control module group 0(PS0)

No.	Module Name	State
1	PS0_Standby_0	Standby
2	PS0_Standby_1	
3	PS0_Standby_2	
4	PS0_Standby_3	
5	PS0_Standby_4	
6	PS0_Startup_0	Startup
7	PS0_Startup_1	
8	PS0_Startup_2	
9	PS0_Startup_3	
10	PS0_Startup_4	
11	PS0_Normal_50u	Normal
12	PS0_Normal_500u	
13	PS0_Stop_0	Stop
14	PS0_Stop_1	
15	PS0_Stop_2	
16	PS0_Stop_3	
17	PS0_Stop_4	

※1) Control cycle : 50μs

※2) Any one module corresponding to the state of the power supply is executed. Only PS0_Normal_50u module PS0_Normal_500u module runs in parallel in normal state operation.

※3) "PS0" indicates that the module group is the first of the two sets of state transition control modules. (the other is PS1)

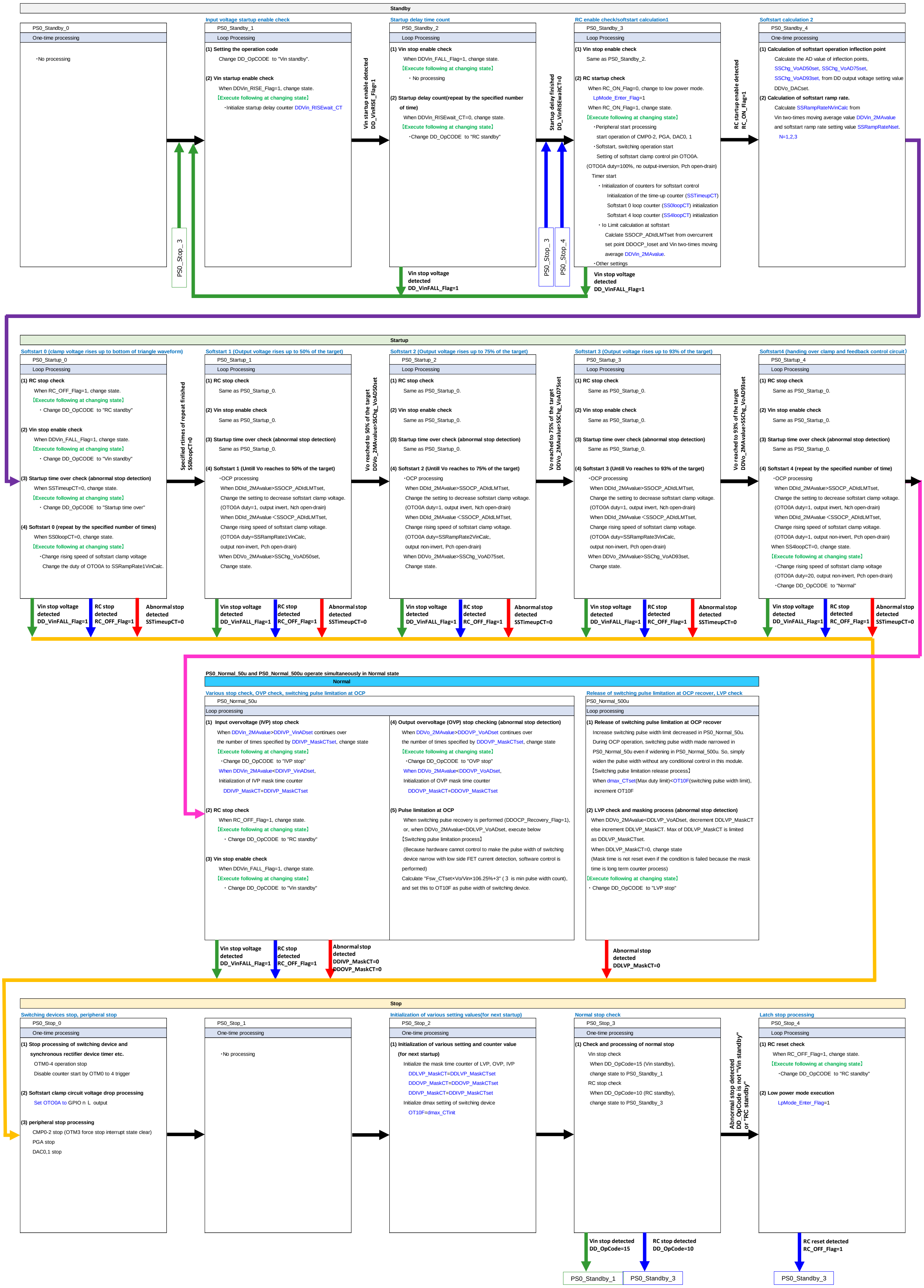

Figure 6-2. LogiCoA001-EVK-001 state transition diagram

6.3 List of State Variables and State Flags

Table 6-2 and 6-3 list the state variables and state flags that RMOS is processing and used for controlling the buck converter. Regarding the description of control program using state variables and state flags, refer to [5].

Table 6-2. State variables and state flags in RMOS

(1)Start/Stop

No.	Variable name・Flag name	Byte	Function	Symbole name for initial value setting	Default value	Comment
1	DDVin_RISEset	2	Startup input voltage setting value	DDVin_RISEsetinit	12880	Monitor cycle: 50μs
2	DDVin_RISE_Flag	Flag	Startup enable input voltage detection	–	–	
3	DDVin_RISEchk_CT	1	Noise rejection counter	DDVin_RISEchk_CTinit	3	
4	DDVin_FALLset	2	Stop input voltage setting value	DDVin_FALLsetinit	11456	
5	DDVin_FALL_Flag	Flag	Stop enable input voltage detection	–	–	
6	DDVin_FALLchk_CT	1	Noise rejection counter	DDVin_FALLchk_CTinit	3	

(2)Remote ON/OFF

No.	Variable name・Flag name	Byte	Function	Symbole name for initial value setting	Default value	Comment
1	RC_ON_Flag	Flag	Startup enable detection by RC pin	–	–	Monitor cycle: 50μs
2	RC_ONchk_CT	1	Noise rejection counter	RC_ONchk_CTinit	3	
3	RC_OFF_Flag	Flag	Stop enable detection by RC pin	–	–	
4	RC_OFFchk_CT	1	Noise rejection counter	RC_OFFchk_CTinit	25	
5	RClogic_Inv_Flag	Flag	RC pin input logic invert flag	–	–	

(3)Digital Filter

No	Variable name	Byte	Function	Reference variable name	Byte	Comment
1	DDVin_2MAvalue	2	Two-times moving average of input voltage AD value	DDVin_ADvalue	2	Calculation cycle: 25μs
2	DDVo_2MAvalue	2	Two-times moving average of output voltage AD value	DDVo_ADvalue	2	Calculation cycle: 25μs
3	DDId_2MAvalue	2	Two-times moving average of drain current AD value	DDId_ADvalue	2	Calculation cycle: 25μs

(4)Communication

No	Variable name	Byte	Function	Symbole name for initial value setting	Default value	Comment
1	PS_ADR	1	Communication address setting	PS_ADR_init	31	
2	RXD_CmdGr	1	Cmd group received by communication	–	–	
3	RXD_CmdNo	1	Cmd no. received by communication	–	–	
4	RXD_Data16	2	16bit data received by communication	–	–	

(5)Control of low power operation mode

No	Variable name	Byte	Function	Comment
1	LpMode_Enter_Flag	Flag	Enter the low power operation mode	
2	LpMode_Exit_Flag	Flag	Enter the normal operation mode	
3	LpMode_Use_RcReset_Flag	Flag	Enable RC reset process	

(6)System

No	Variable name	Byte	Function	Comment
1	DD_OpCode	1	Operation code of DCDC block	
2	DD_OpCode_FailRec	1	Operation code of DCDC block abnormal termination	
3	TaskCompChk_Flag	Flag	Check flag of task completion	

(7)LED blinking

No	Symbol name	Byte	Function	Comment
1	LED1FP_VinStby	–	Blink pattern of standby under startup voltage	
2	LED1FP_RcStby	–	Blink pattern of standby by RC	
3	LED1FP_NomOP	–	Blink pattern of normal operation	
4	LED1FP_FAIL	–	Blink pattern of abnormal termination	

Table 6-3. State variables and state flags for buck converter control

(1)Switching device・Synchronous rectifier device setting

No	Variable name	Byte	Function	Symbol name for initial value setting	Default value	Comment
1	Fsw_CTset	2	Switching frequency (OTM) setting	Fsw_CTinit	399	
2	dmax_CTset	2	Maximum duty (OTM) setting of switching device	dmax_CTinit	319	
3	DTimeHoffLon_CTset	2	Dead time (OTM) setting between switching device off and synchronous rectifier device on	DTimeHoffLon_CTinit	9	
4	DTimeLoffHon_CTset	2	Dead time (OTM) setting between synchronous rectifier device off and switching device on	DTimeLoffHon_CTinit	379	

(2)Startup delay

No.	Variable name	Byte	Function	Symbol name for initial value setting	Default value	Comment
1	DDVin_RISEwait_CTset	2	Startup delay setting	DDVin_RISEwait_CTinit	20000	Count cycle: 50μs
2	DDVin_RISEwait_CT	2	Startup delay counter	–	–	

(3)Softstart

No	Variable name	Byte	Function	Symbol name for initial value setting	Default value	Comment
1	SSRampRate1set	1	Softstart ramplate 1 setting	SSRampRate1init	50	
2	SSRampRate2set	1	Softstart ramplate 2 setting	SSRampRate2init	25	
3	SSRampRate3set	1	Softstart ramplate 3 setting	SSRampRate3init	12	
4	SSTimeupCTset	2	Startup time over detect time	SSTimeupCTinit	1000	
5	SS0loopCTset	1	Loop count before softstart	SS0loopCTinit	3	
6	SS4loopCTset	1	Loop count to normal operation	SS4loopCTinit	150	

(4)Output voltage setting

No	Variable name・Symbol name	Byte	Function	Symbol name for initial value setting	Default value	Comment
1	DDVo_DACset	1	DAC value for DCDC block output voltage	DDVo_DACinit	101	
2	DDVo_DAC_MaxLmt	–	DAC max limit value for DCDC block output voltage	(this variable is a sybol)	181	

(5)Protection

No	Variable name	Byte	Function	Symbol name for initial value setting	Default value	Comment
1	DDOCP_Ioset	2	Over current protection setting value for DCDC block	DDOCP_Ioinit	6000	
2	DDLVP_VoADset	2	Low voltage protection setting value for DCDC block	DDLVP_VoADinit	12528	Count cycle: 500μs
3	DDLVP_MaskCTset	2	Mask time (Noise rejection) setting	DDLVP_MaskCTinit	1000	
4	DDOVP_VoADset	2	Output over voltage protection setting valuefor DCDC block	DDOVP_VoADinit	25056	Count cycle: 50μs
5	DDOVP_MaskCTset	1	Mask time (Noise rejection) setting	DDOVP_MaskCTinit	5	
6	DDIVP_VinADset	2	Input over voltage protection setting valuefor DCDC block	DDIVP_VinADinit	54432	Count cycle: 50μs
7	DDIVP_MaskCTset	1	Mask time (Noise rejection) setting	DDIVP_MaskCTinit	5	

6.4 Firmware

For LogiCoA001-EVK-001, in addition to the evaluation board, the source code of RMOS and power supply control are supplied. And those can be downloaded from the URL below.

Table 6-4. RMOS download URL and the file name

Download URL	https://www.rohm.com/reference-designs/ref66009
Reference Program Name	LogiCoA™ Solution Buck Conveter Reference Program
File Name	RMOS100-PSFW001.zip

7 Debugger Connection and Development of the Program

In the LogiCoA001-EVK-001, the firmware is implemented, and evaluation can be carried out only with the board, but in addition to prepare following environment, a program of switching power supply control using RMOS can be developed or debugged.

① Integrated Development Environment LEXIDE-Ω
② RMOS project file (file to be read into LEXIDE-Ω and used)
③ Windows PC (Windows10 64bit version or Windows11 64bit version)
④ On-chip emulator EASE1000 V2
⑤ Microsoft Excel 64bit version (used to check the communication function and requires permission to use the macro function)

"Integrated Development Environment LEXIDE-Ω" is a software developed based on "Eclipse," an integrated development environment for open sources, and installed on a PC for use. The installers can be downloaded from our web website.

"RMOS project file" is provided in a zip compressed format and extracted to the any folder in the HDD (SSD) drive of Windows PC.

To use the on-chip emulator EASE1000 V2, connect EASE1000 V2 to USB terminal of the PC and to the debug pins of ML62Q203x/4x group. With EASE1000 V2 and LEXIDE-Ω, debug operation (such as writing to the MCU, execution, stop, stepping, internal memory reading and so on) can be carried out.

Refer to [5] for more detail information about developing or debugging of switching power supply control program with RMOS.

8 PWM Control Using Operational Timer (OTM)

8.1 Overview of Operational Timer

LogiCoA™ output solution uses an operational timer to control the outgoing FET of applications. The operational timer can perform various operations such as the logical product and trigger control between timers, and the logical product and trigger control of the timer and the built-in analog comparator output. Figure 8-1 is a schematic diagram of the operational timer function. (In the figure, only channel 0 is shown as a representative for simplification.)

The operational timer has six channels from OTM0 to OTM5, in which only OTM2 and OTM3 have one output and the other has two outputs. The two outputs can be PWM output at different Duty in the same cycle (PWM output: OTMn0 and OTMn1, n=0, 1, 4, 5, but only OTMn0 for n=2, 3). This PWM can be logical product with the timer signal/analog comparator output/external trigger input of other channels (output after logical product: OTMn0S and OTMn1S). In addition, two outputs are output from A/B 2 output terminals (ex. OTO0A and OTO0B), but one of the two outputs (output selection) can be set. Each output signal can be set to positive or negative logic (output logic selection).

In addition to the above selection of logical products, output signal selection, and output logic selection, the operational timer can control the timer count start/stop of various signals by using timer signals of other channels, analog comparator output, external trigger input, etc. This enables control such as linking ON/OFF of several output FET and stopping switching by the protection-detection comparator output.

The features of the operational timer are shown below. For details, refer to [3] and [4].

- The same period PWM with differing Duty can be output.
- Logical product with PWM output from other channels, external trigger, and analog comparator.
- External trigger input, timer interrupt request (event trigger), counter operation start/stop/counter clear by analog comparator output is possible
- An interrupt is generated when the pin output is forcibly stopped or stopped by the external trigger input or analog comparator output.
- Logical switching of timer output (positive logic/negative logic) is possible
- Capture /PWM with 16bit counters
- The count clock can be selected from 32kHz/16MHz/64MHz/ external trigger (divided by 1 to 128).
- Duty and cycle of the input-signal can be measured by the capture function.

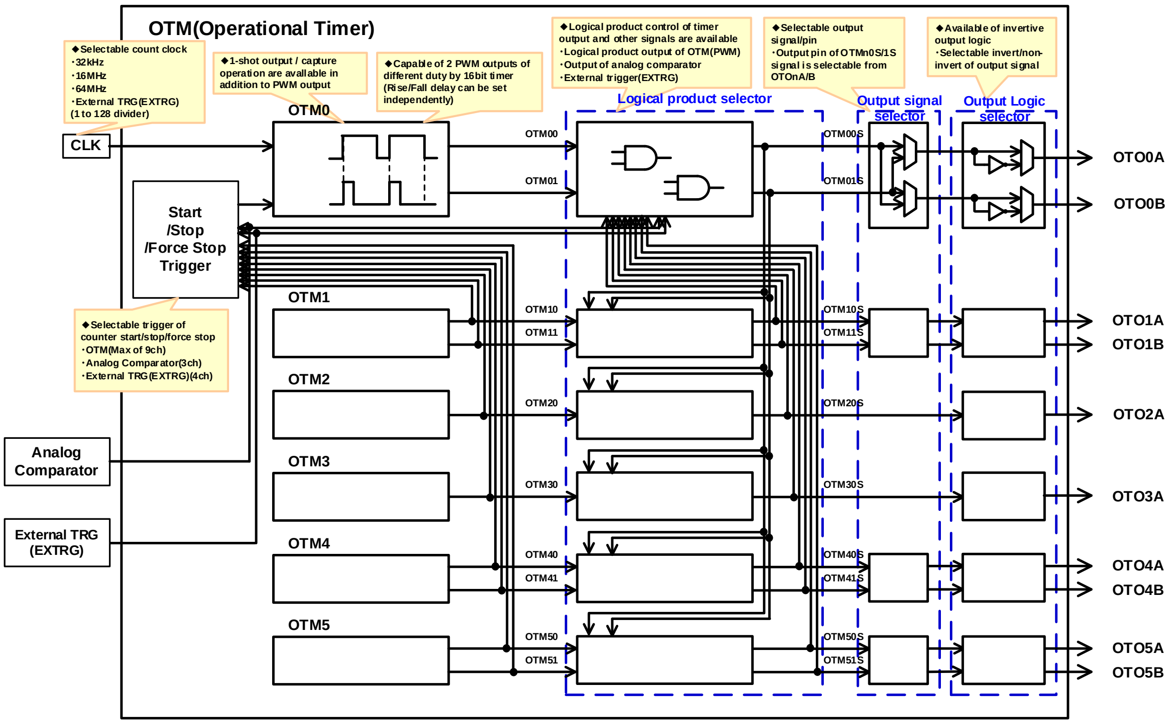

Figure 8-1. Schematic diagram of operational timer

8.2 PWM Control of the Buck Converter

This section describes PWM control of this buck converter. The timers have the roles shown in Table 8-1 and Figure 8-2. Output pins of respective timers are Table 5. Refer to the list of ML62Q2035 pins.

Table 8-1. Role of each operational timer

Channel	PWM Output	Internal Signal	Output Signal	
			OTOnA	OTOnB
OTM0	OTM00	Softstart Control	Softstart Control	-
	OTM01	Max Duty Clock	-	Max Duty Clock
OTM1	OTM10	-	H-side Gate Control	-
	OTM11	Not used	Not used	Not used
OTM2	OTM20	-	L-side Gate Control	
OTM3	OTM30	OCP	-	
OTM4	OTM40	L→H Deadtime Generate	Not used	Not used
	OTM41	Not used	Not used	Not used
OTM5	OTM50	Not used	Not used	Not used
	OTM51	Not used	Not used	Not used

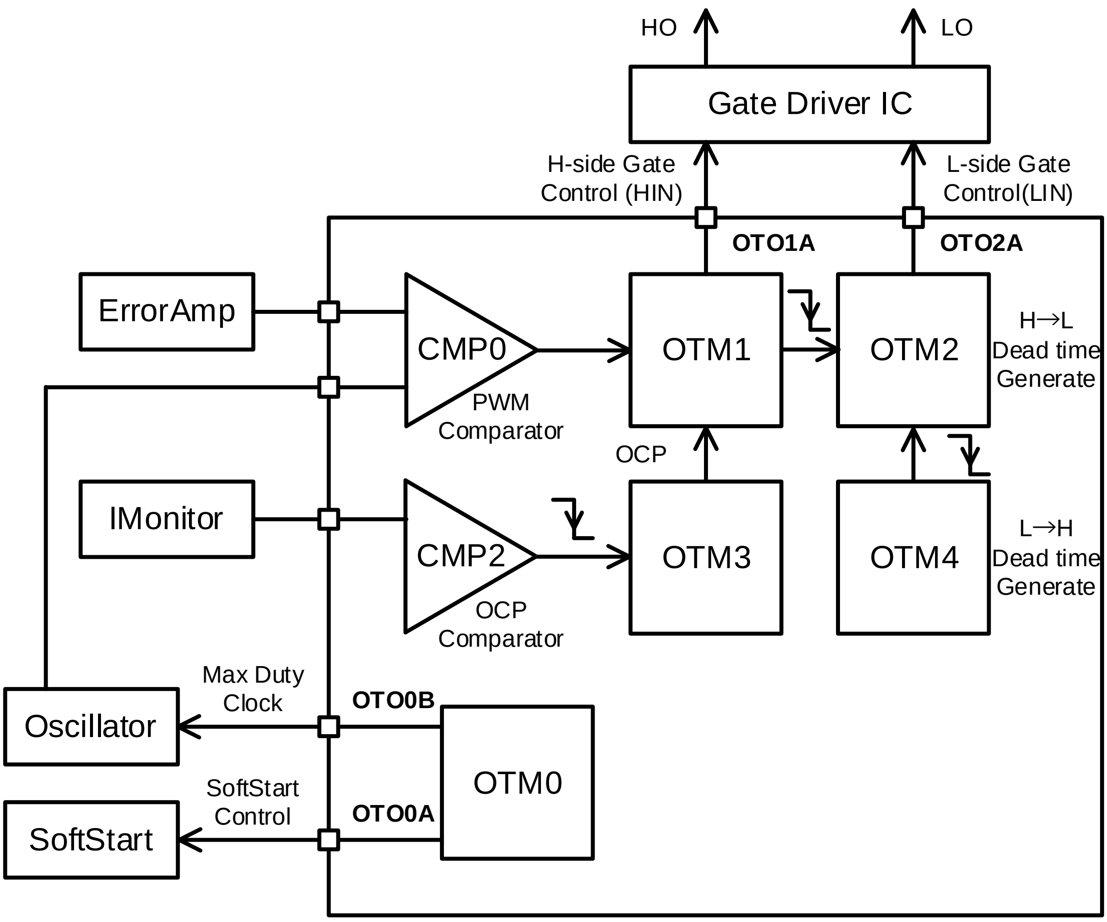

Figure 8-2. Role of each operational timer

The timing chart for PWM control of the buck converter is shown in Figure 8-3.

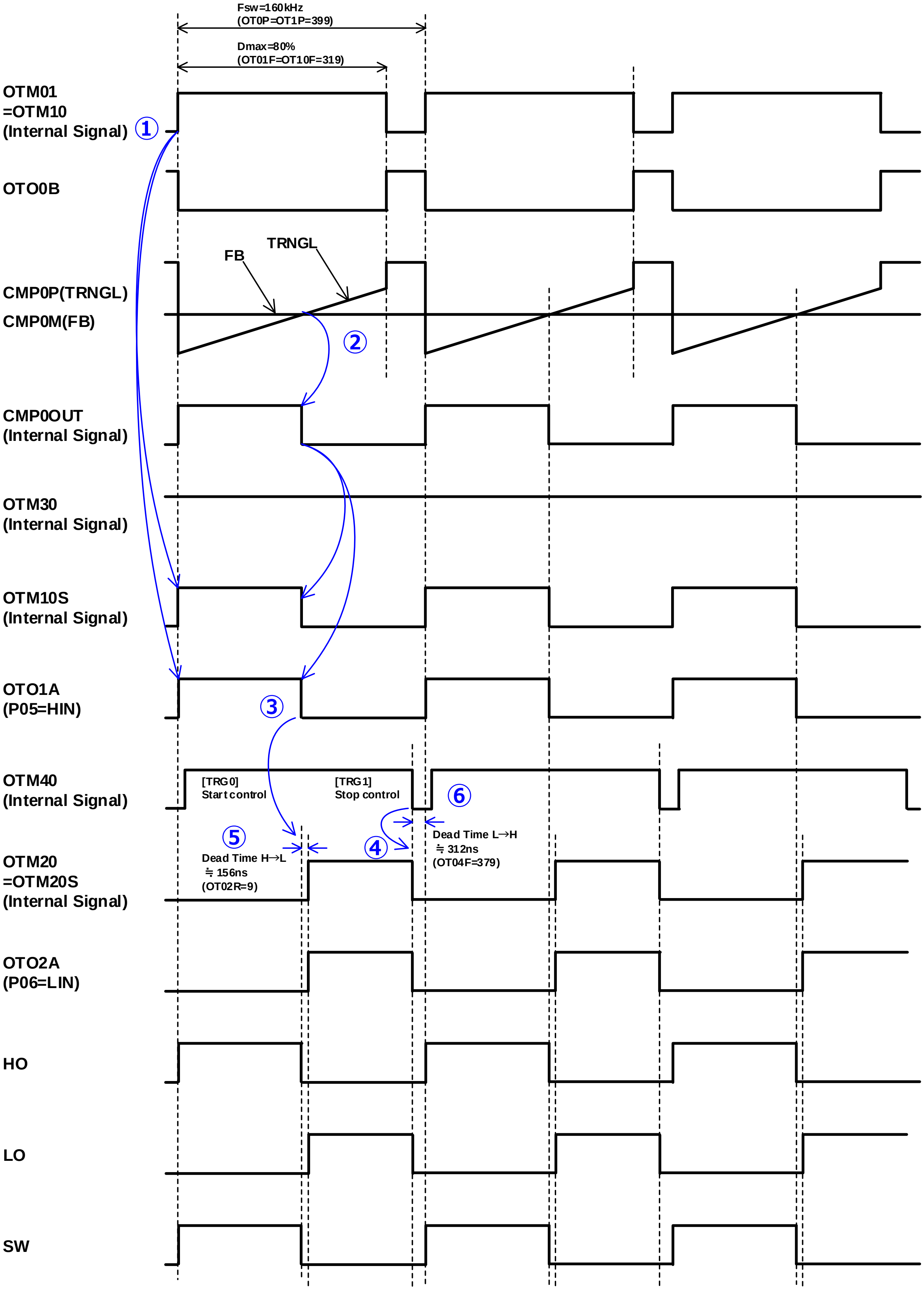

Figure 8-3. PWM control timing chart

The operation of each operational timer is described below.

OTM0: Softstart control is performed with the output signal OTO0A, and Max Duty clocks for triangle waveform generation are output with OTO0B.

Softstart control by OTO0A is not included in Figure 8-3 timing chart. Refer to 4.7 “Soft Start” together. As described in 4.7, the output is soft started by controlling ON Duty of PMOS inside the pin during startup (from state transition control module Startup_0 to Startup_4). OTO0A does not have a logical product with other signals and OTM00 = OTM00S is output. OTM00 operates in the switching frequency fsw.

For OTO0B, refer to 4.8 “Triangle Waveform Generator and PWM Comparator”. OTO0B does not take the logical product with other outputs, and the signal obtained by logically inverting OTM01=OTM01S (internal signal) of the switching-frequency fsw, Max Duty Dmax is output.

OTM1: The output signal OTO1A controls the high side FET.

OTO1A is OTM10S of the logical product of OTM10 (internal signal), its switching frequency is fsw and Max Duty is Dmax, and PWM comparator (CMP0) output CMP0OUT (internal signal) and OTM30 indicating OCP detection (H when the internal signal OCP is not detected). (For OTM30 behavior, see OTM3 section below) ① OTM10 outputs H from the beginning of the clock cycle (rising edge of OTM10) and the high side FET turns ON. ② When the voltage of TRNGL rises and exceeds FB voltage, CMP0OUT becomes L, and OTM10S that is the logical product also becomes L and the high-side FET is turned OFF.

OTO1B is unused.

OTM2: The output signal OTO2A controls the low side FET.

For OTO2A, OTM20=OTM20S is output without taking the logical product with other signals. OTM20 operates on the falling edge of the high side FET control signal OTO1A and the falling edge of the internal signal OTM40 for deadtime generating as triggers. ③ Timer count is started by the falling edge of OTO1A, and after the dead- ime (T_{deadHL}) setting time in the high side FET OFF to low side FET ON is counted, H is output to OTO2A, and ④ L is output by the falling edge of OTM40. ⑤ TdeadHL is determined by the delay between OTM20 timer count start and the rising edge timing. It is set by DTimeHoffLon_CTset (default of 9). T_{deadHL} can be calculated from DTimeHoffLon_CTset using the following equation.

$$T_{deadHL} = \frac{1}{f_{PLL}} \times (DTimeHoffLon\_CTset + 1) = \frac{1}{64MHz} \times (9 + 1) \cong 156ns$$

OTM3: The output signal is unused. Control is performed with the internal signal OTM30 during OCP operation.

OTO3A is unused. For the internal signal OTM30 indicating OCP detection, H is output during normal operation, but counting is forcibly stopped using the falling edge of OCP comparator (CMP2) output CMP2OUT (internal signal) as a trigger and L is output. The output OTO1A of OTM1 becomes L when an OCP is detected by taking the logical product with OTM30, and the output FET is turned OFF.

OTM4: The output signal is unused. Internal signal OTM40 generates dead time when low side FET OFF to high side FET ON.

OTO4A and OTO4B are not used. The switching frequency of OTM40 is fsw and has a dead time (L output interval) at the end of one clock cycle. A dead time (T_{deadLH}) in the low side FET OFF to high side FET ON can be provided by setting OTO2A output L at the falling edge of OTM40. ⑥ T_{deadLH} is determined by the delay between the falling timing of OTM40 and ON timing of high side FET at the beginning of the next clock. It is set by DTimeLoffHon_CTset (defaulted to 379). T_{deadLH} is the difference between the count number of the switching period and the count number of OTM40 falling timing. Using DTimeLoffHon_CTset, the following formula can be used:

$$T_{deadLH} = \frac{1}{f_{PLL}} \times (FswCTset - DTimeLoffHon\_CTset) = \frac{1}{64MHz} \times (399 - 379) \cong 312ns$$

OTM5: Not used for both output signals and internal signals.

9 Application Schematic

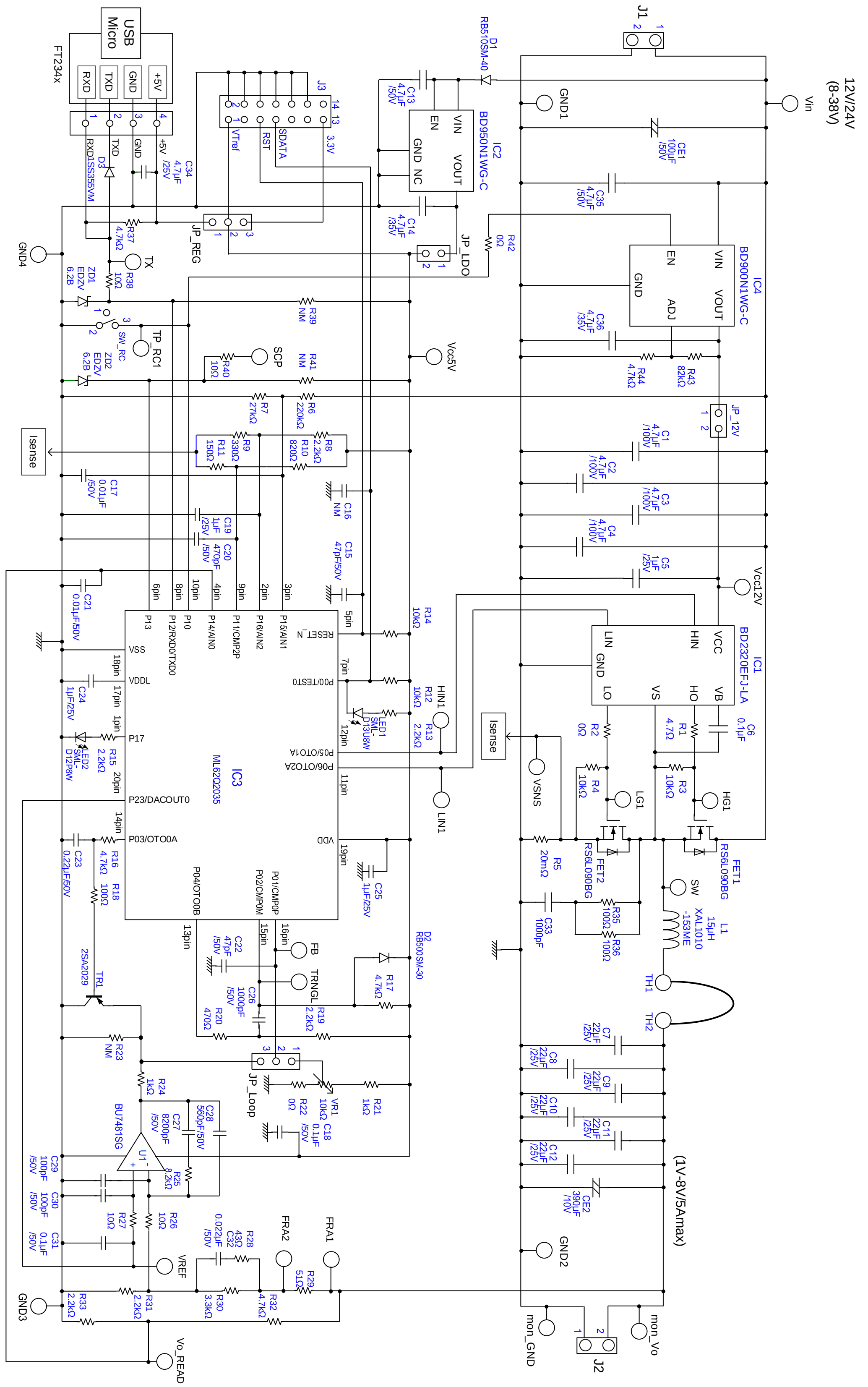

Figure 9-1. Buck Converter Application Schematic

10 References

[1] 66UG090E, Rev001, Synchronous Buck DCDC Converter Evaluation Board LogiCoA001-EVK-001

[2] 66AN145E, Rev001, Analog-Digital hybrid control innovating switching power design

[3] FEDL62Q2045-01, ML62Q2033/2035/2043/2045 datasheet

[4] FEUL62Q2045-03, ML62Q2033/2035/2043/2045 User's Manual

[5] 66AN147E, Rev.001, Operating system for switching power control MCU "RMOS"

[6] TSZ02201-0BDB0A400100-1-2, Rev.001, For Automotive 45V 150mA Fixed/Adjustable Output Nano Cap™ LDO Regulators BD9xxN1-C Series datasheet

[7] TSZ02201-0RAR0G200370-1-2, Rev.001, High Speed Low Voltage Operation CMOS Operational Amplifiers BU7481G BU7481SG datasheet

[8] TSZ02201-0Q2Q0A800840-1-2, Rev.001, High Frequency High-Side and Low-Side Driver BD2320EFJ-LA datasheet

[9] 66AN149E, Rev.001, Serial communication of RMOS and GUI developing manual

Revision History

Date	Revision Number	Description
1. Aug. 2024	001	Initial release.

Notice

1) The information contained in this document is intended to introduce ROHM Group (hereafter referred to asROHM) products. When using ROHM products, please verify the latest specifications or datasheets before use.

2) ROHM products are designed and manufactured for use in general electronic equipment and applications (such as Audio Visual equipment, Office Automation equipment, telecommunication equipment, home appliances, amusement devices, etc.) or specified in the datasheets. Therefore, please contact the ROHM sales representative before using ROHM products in equipment or devices requiring extremely high reliability and whose failure or malfunction may cause danger or injury to human life or body or other serious damage (such as medical equipment, transportation, traffic, aircraft, spacecraft, nuclear power controllers, fuel control, automotive equipment including car accessories, etc. hereafter referred to as Specific Applications). Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses, or losses incurred by you or third parties arising from the use of ROHM Products for Specific Applications.

3) Electronic components, including semiconductors, can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against physical injury, and damage to any property, which a failure or malfunction of products may cause.

4) The information contained in this document, including application circuit examples and their constants, is intended to explain the standard operation and usage of ROHM products, and is not intended to guarantee, either explicitly or implicitly, the operation of the product in the actual equipment it will be used. As a result, you are solely responsible for it, and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses, or losses incurred by you or third parties arising from the use of such information.

5) When exporting ROHM products or technologies described in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, such as the Foreign Exchange and Foreign Trade Act and the US Export Administration Regulations, and follow the necessary procedures in accordance with these provisions.

6) The technical information and data described in this document, including typical application circuits, are examples only and are not intended to guarantee to be free from infringement of third parties intellectual property or other rights. ROHM does not grant any license, express or implied, to implement, use, or exploit any intellectual property or other rights owned or controlled by ROHM or any third parties with respect to the information contained herein.

7) No part of this document may be reprinted or reproduced in any form by any means without the prior written consent of ROHM.

8) All information contained in this document is current as of the date of publication and subject to change without notice. Before purchasing or using ROHM products, please confirm the latest information with the ROHM sales representative.

9) ROHM does not warrant that the information contained herein is error-free. ROHM shall not be in any way responsible or liable for any damages, expenses, or losses incurred by you or third parties resulting from errors contained in this document.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

https://www.rohm.com/contactus