ROHM GROUP
LAPIS TECHNOLOGY

FEBL22Q573RB-03

RB-S22Q573MB30
User's Manual

Issue Date: October 14, 2021

ROHM SEMICONDUCTOR

Notes

1) The information contained herein is subject to change without notice.

2) When using LAPIS Technology Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples、etc.). Therefore LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) The Products are intended for use in general electronic equipment (AV/OA devices, communication, consumer systems, gaming/entertainment sets, etc.) as well as the applications indicated in this document. For use of our Products in applications requiring a high degree of reliability (as exemplified below), please be sure to contact a LAPIS Technology representative and must obtain written agreement: transportation equipment (cars, ships, trains, etc.), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us. Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc.

6) The Products specified in this document are not designed to be radiation tolerant.

7) LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Technology does not warrant that such information is error-free and LAPIS Technology shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

8) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

9) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act..

10) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

11) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) "LAPIS Technology" as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

Table of Contents

1. Overview

This instruction manual is for the RB-S22Q573MB30 which is the reference board for ML22Q573/ML2257X/ML22Q563/ML2256X/ML22Q553 (hereinafter referred to as "Speech Synthesis LSIs").

This board can be combined with Sound Device Control Board 3 (hereinafter referred to as "SDCB3") to do the following:

- Voice playback by ML22Q573/ML2257X/ML22Q563/ML2256X/ML22Q553.
- Writing sound code data into ML22Q573/ML22Q563/ML22Q553.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q573MB30.

- Turn off the power when attaching the RB-S22Q573MB30 to the SDCB3.
- Turn off the power when loading Speech Synthesis LSIs into the RB-S22Q573MB30. Pin 1 is the position of the board silk ▲ at the bottom left with respect to the socket opening. The Figure 1 shows the setting directions of Speech Synthesis LSIs.
- Use the RB-S22Q573MB30 with a power supply voltage of 5.0V.
- Connect JACK1 jack and JACK2 jack to the mono speaker.

- RB-S22Q573MB30 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q573MB30 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-S22Q573MB30 support. Replace only in case of initial failure.

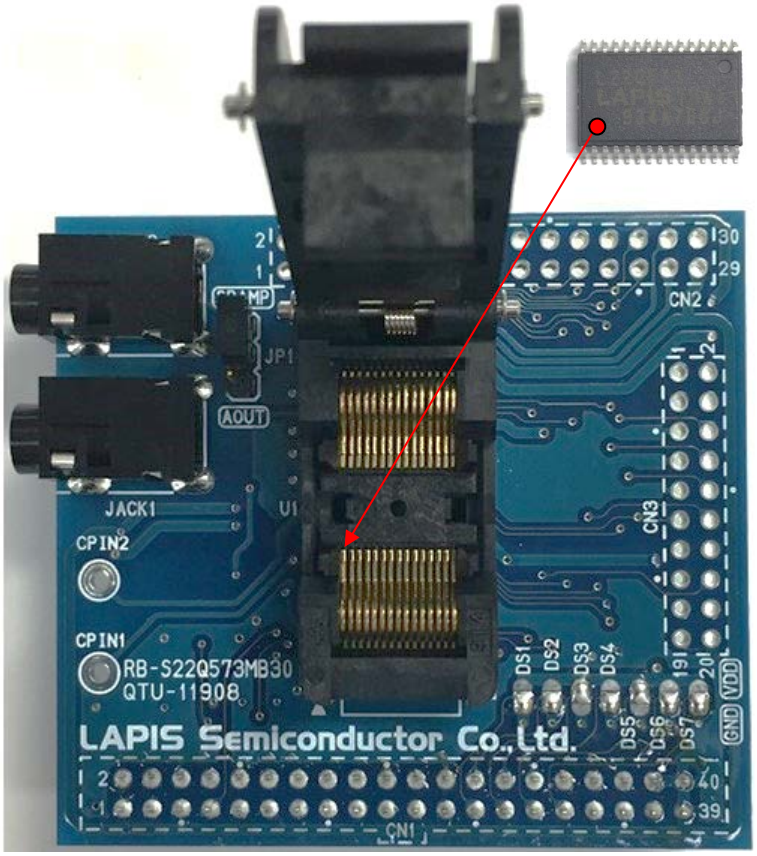


Figure 1 Outline Diagram

3. Specification

3.1. JP1 jumper pin

JP1 jumper pin is jumper pin that switch the connection of SPP pin of Speech Synthesis LSIs.

OUT	Contents
AOUT	SPP pin is connected to JACK1 jack.
SPAMP	SPP pin is connected to JACK2 jack.

3.2. JACK1 jack

JACK1 jack is a jack where the signal from SPP pins of Speech Synthesis LSIs is output via the speaker amplifier.
Set the JP1 jumper pin to AOUT when using JACK1 jack.
Connect a monaural speaker.

3.3. JACK2 jack

JACK2 jack is a jack where the signal from SPP,SPM pins of Speech Synthesis LSIs is output.
Set the JP1 jumper pin to SPAMP when using JACK2 jack.
Connect a monaural speaker.

3.4. CPIN1, CPIN2 through hall

CPIN1, CPIN2 through hole is used to input signals from an external source to the AIN pin of Speech Synthesis LSIs.
Input the speaker amplifier input signal to CPIN1, CPIN2 through hole.

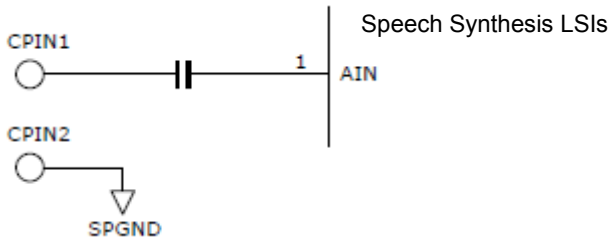


Figure 2 CPIN1, CPIN2 through hall

3.5. CN1 connector

CN1 connector is used to connect to SDCB3.

3.6. CN2 connector

CN2 connector is used to connect to the pins of Speech Synthesis LSIs.

CN2 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit
1	1	AIN	O	I
2	2	SG	O	O
3	3	VDDR	O	O
4	4,18	DVDD *	O	I
5	5,15	DGND	O	I
6	6	VDDL	O	O
7	7	DIPH	O	I
8	8	STATUS	O	O
9	9	ERR	O	O
10	10	CSB	O	I
11	11	SCK	O	I
12	12	SI	O	I
13	13	SO	O	O
14	14	CBUSYB	O	O
15	5,15	DGND	O	I
16	16	XTB	O	O
17	17	XT	O	O
18	4,18	DVDD *	O	I
19	-	-	-	-
20	20	RESETB	O	I
21	21	TESTI0 (MODE)	O	I
22	22	TESTI1 (nTRST)	O	I
23	23	TESTI2 (TMS)	O	I
24	24	TESTI3 (TDI)	O	I
25	25	TESTI4 (TCK)	O	I
26	26	TESTO (TDO)	O	O
27	27	SPM	O	O
28	28	SPP	O	O
29	29	SPGND	O	I
30	30	SPVDD *	O	I

*1 Do not supply DVDD,SPVDD from CN2 when connecting SDCB3.

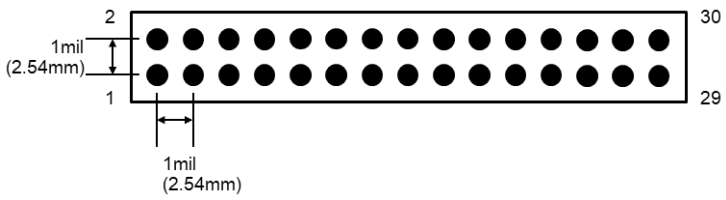


Figure 3 CN2 connectors hole pattern

3.7. CN3 connector

CN3 connector is used to connect to the serial audio interface pin of Speech Synthesis LSIs.

CN3 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit
1	-	-	-	-
2	4,18	DVDD	O	I
3	-	-	-	-
4	4,18	DVDD	O	I
5	5,15	DGND	O	I
6	25	TESTI4 (TCK)	O	I
7	5,15	DGND	O	I
8	24	TESTI3 (TDI)	O	I
9	5,15	DGND	O	I
10	26	TESTO (TDO)	O	O
11	23	TESTI2 (TMS)	O	I
12	22	TESTI1 (nTRST)	O	I
13	-	-	-	-
14	-	-	-	-
15	-	-	-	-
16	21	TESTI0 (MODE)	O	I
17	-	-	-	-
18	-	-	-	-
19	-	-	-	-
20	5,15	DGND	O	I

*1 Do not supply DVDD from CN3 when connecting SDCB3.

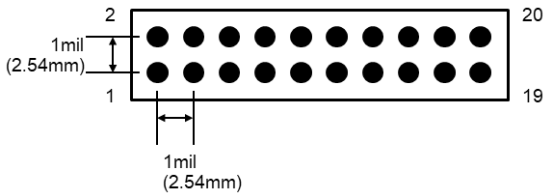


Figure 4 CN3 connectors hole pattern

4. Appendix

4.1. PCB layout

Figure 5 shows the RB-S22Q573MB30 PCB layout.

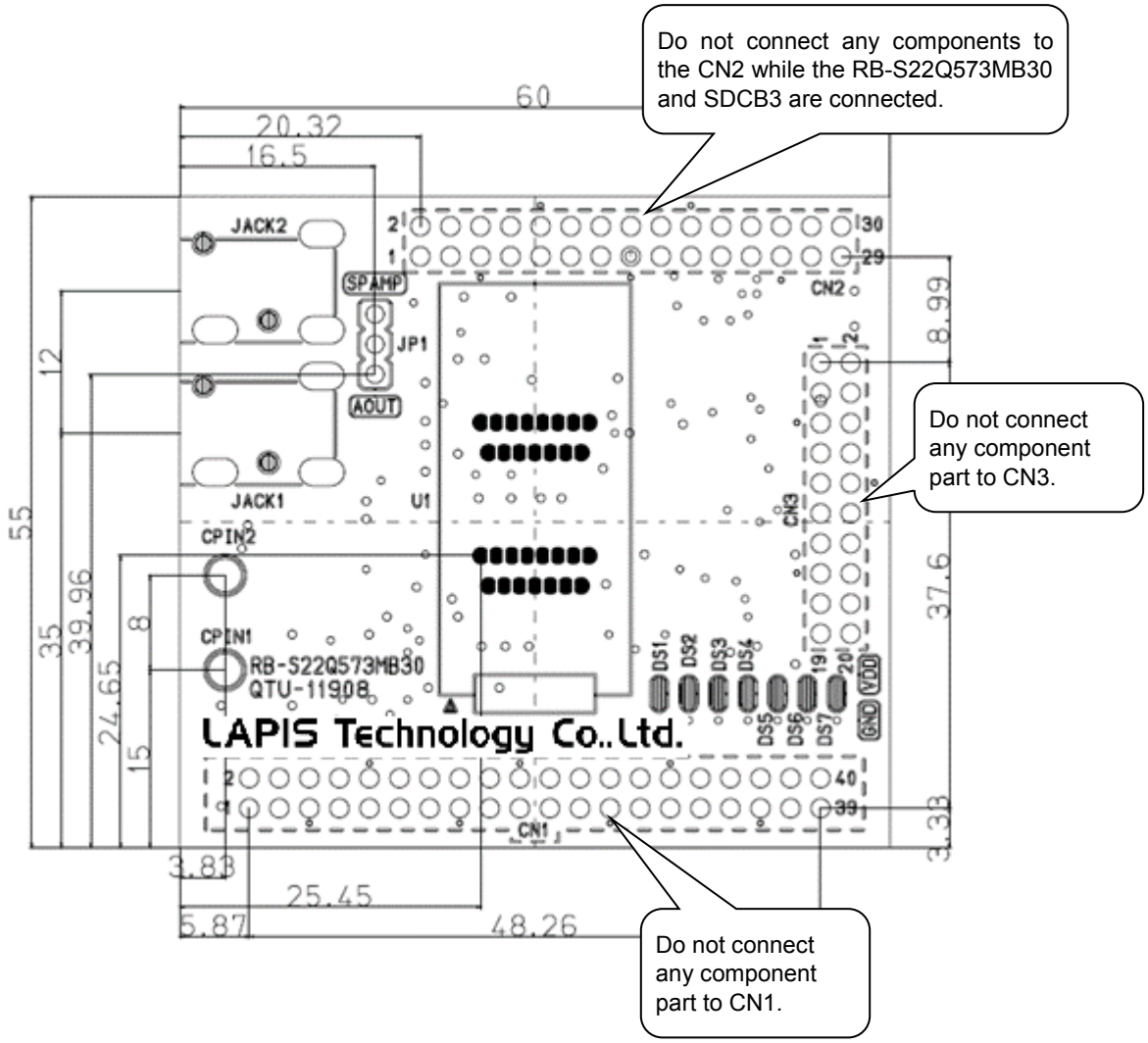
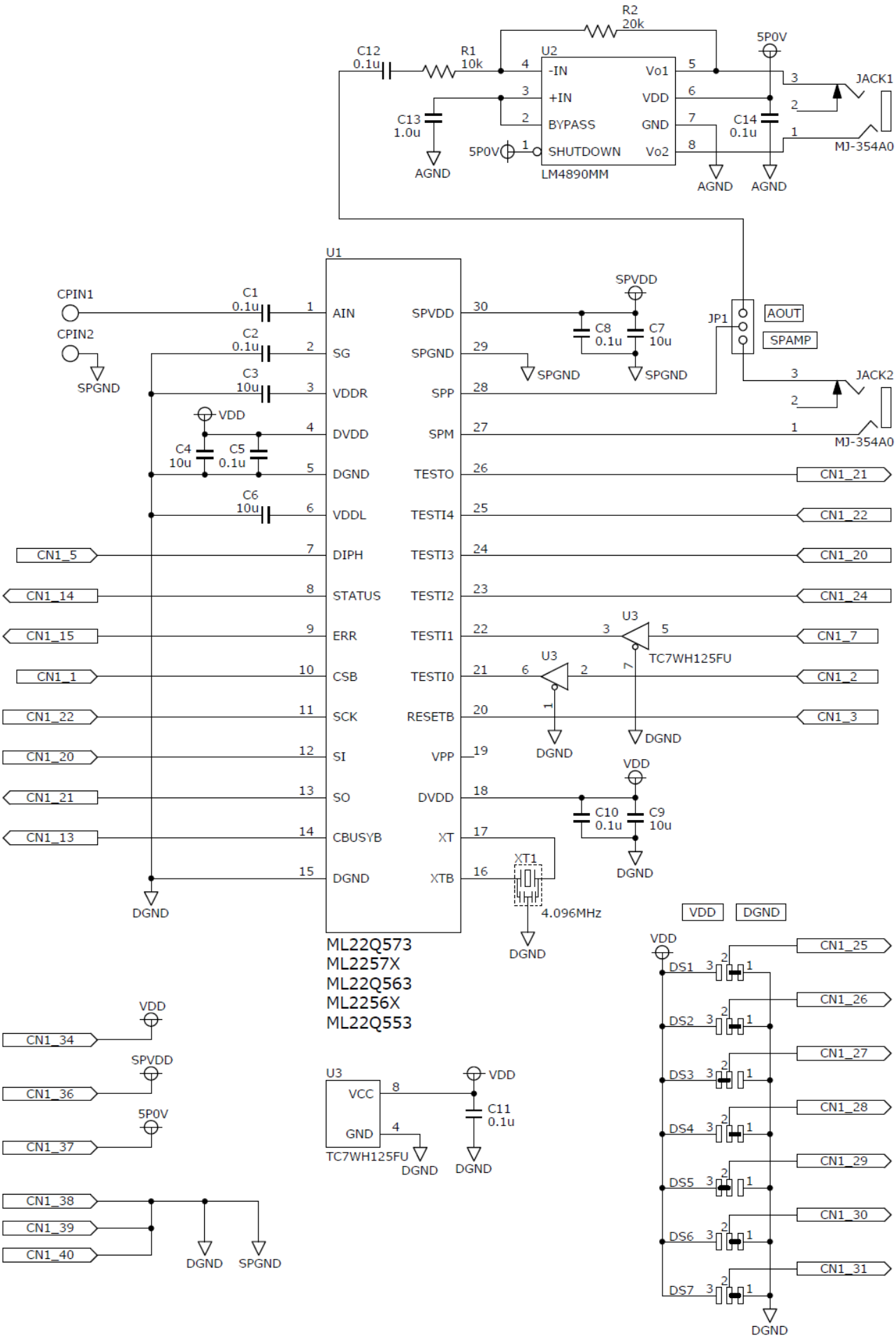


Figure 5 PCB layout

4.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11908	RB-S22Q573MB30	PCB	1	LAPIS Technology Co., Ltd.
2	CGA3E2X7R1E104K080AA	C1, C2, C5, C8, C10, C11, C12, C14	Ceramic Capacitor 0.1μF/25V X7R	8	TDK Corporation
3	CGA3E1X7R1C105K080AC	C13	Ceramic Capacitor 1.0μF/16V X7R	1	TDK Corporation
4	EMK212ABJ106KD-T	C3, C4, C6, C7, C9	Ceramic Capacitor 10uF/16V X5R	5	TAIYO YUDEN CO., LTD.
5	HIF3FB-40DA-2.54DSA(71)	CN1	HIF3FB-40DA-2.54DSA(71)	1	Hirose Electric Co., Ltd.
6	-	DS1, DS2, DS3, DS4, DS5, DS6, DS7	Select pad	7	-
7	MJ-354A0	JACK1, JACK2	2-Conductor Miniature Jack	2	MARUSHIN ELECTRIC MFG. CO., LTD.
8	A2-3PA-2.54DSA	JP1	3pin Pin Header	1	Hirose Electric Co., Ltd.
9	MCR03EZPJ103	R1	Resistor 10kΩ ±5%	1	Rohm Co., Ltd.
10	MCR03EZPJ203	R2	Resistor 20kΩ ±5%	1	Rohm Co., Ltd.
11	IC51-0302-914	U1	SSOP30 Socket	1	YAMAICHI ELECTRONICS Co., Ltd.
12	LM4890MM/NOPB	U2	Audio Power Amplifier	1	Texas Instruments Incorporated
13	TC7WH125FU	U3	Bus Buffer with 3-State Output	1	Toshiba Corporation
14	CSTCR4M09G55B-R0	XT1	Ceramic Resonators 4.096MHz 39pF	1	Murata Manufacturing Co., Ltd.
15	HIF3GA-2.54SP	-	Short Pin	1	Hirose Electric Co., Ltd.
16	-	CN2	Unmounted	1	-
17	-	CN3	Unmounted	1	-
18	-	CPIN1, CPIN2	Unmounted	2	-


R2
20k
C12
0.1u
R1
10k
U2
-IN
+IN
BYPASS
SHUTDOWN
Vo1
VDD
GND
Vo2
LM4890MM
5P0V
C13
1.0u
C14
0.1u
AGND
JACK1
MJ-354A0
U1
CPIN1
CPIN2
C1
C2
C3
C4
C5
C6
C7
C8
C10
C9
C11
SPVDD
SPGND
VDD
DGND
JP1
AOUT
SPAMP
JACK2
AIN
SG
VDDR
DVDD
DGND
VDDL
DIPH
STATUS
ERR
CSB
SCK
SI
SO
CBUSYB
DGND
SPVDD
SPGND
SPP
SPM
TESTO
TESTI4
TESTI3
TESTI2
TESTI1
TESTI0
RESETB
VPP
DVDD
XT
XTB
CN1_21
CN1_22
CN1_20
CN1_24
CN1_7
CN1_2
CN1_3
U3
TC7WH125FU
XT1
4.096MHz
ML22Q573
ML2257X
ML22Q563
ML2256X
ML22Q553
CN1_5
CN1_14
CN1_15
CN1_1
CN1_22
CN1_20
CN1_21
CN1_13
CN1_34
CN1_36
CN1_37
CN1_38
CN1_39
CN1_40
VCC
GND
DS1
DS2
DS3
DS4
DS5
DS6
DS7
CN1_25
CN1_26
CN1_27
CN1_28
CN1_29
CN1_30
CN1_31

5. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q573RB-01	March 19, 2020	–	–	First edition.
FEBL22Q573RB-02	Jury 30 2021	Notes	Notes	Change the description.
				Company name change.
		1	1	2. Operational notes Added to connect a monaural speaker to the JACK1 jack and JACK2 jack.
		-	2	3.1. JP1 jumper pin Changed chapter name.
				3.2. JACK1 jack Changed chapter number. Added SDCB Controller settings when using JACK1 jack. Added to connect a monaural speaker to the JACK1 jack.
				3.3. JACK2 jack Changed chapter number. Added SDCB Controller settings when using SP jack. Added to connect a monaural speaker to the JACK2 jack.
				3.5. CPIN1, CPIN2 through hall Changed chapter number. Changed chapter name. Added connection diagram.
		-	3	3.5. CN1 connector Changed chapter number.
				3.6. CN2 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.
		-	4	3.7. CN3 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.
				3.10. Ceramic resonator Deleted chapter.
		-	5	4. Appendix Added chapter.
				4.1. PCB layout Changed chapter number. Changed Figure 5.
		-	6	4.2. BOM list, Schematic Changed chapter number. Company name change.
		-	7	4.2. BOM list, Schematic Changed chapter number. Company name change.

FEBL22Q573RB-03	October 14 2021	7	7	4.2. BOM list, Schematic Fixed an error in the connection destination of 24pin of U1. Fixed an error in the connection destination of 25pin of U1. Fixed an error in the connection destination of 26pin of U1.