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FEUL610Q306-01

ML610Q305/306
User's Manual

Issue Date: Jun. 28, 2021

ROHM SEMICONDUCTOR

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610Q305/306.

The following manuals are also available. Read them as necessary.

■ nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications of CCU8.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ LEXIDE-U16 User's Manual
Description on the integrated development environment LEXIDE-U16.

■ EASE1000 V2 User's Manual
Description on the on-chip debug tool EASE1000 V2.

■ MWU16 Flash Writer Host Program User's Manual
Description on the Flash Multi Writer host program, MWU16.

Notation

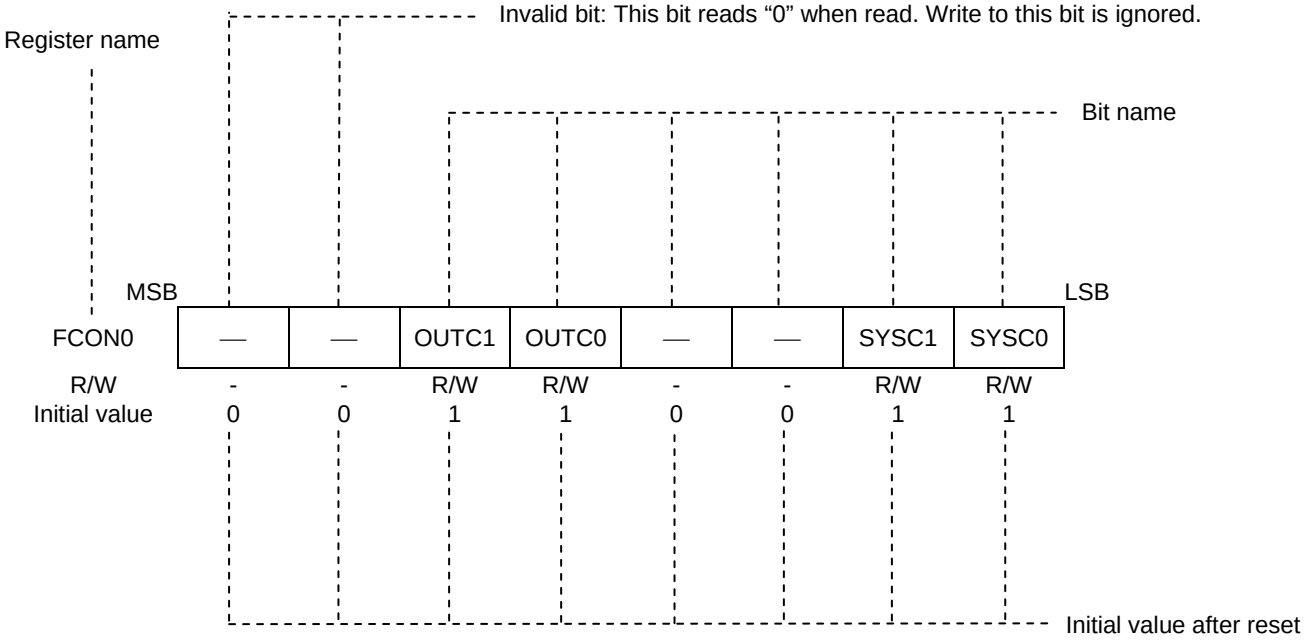
Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number.
	xxb	Indicates a binary number.
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.

MSB: The highest bit of 8-bit register

LSB: The lowest bit of 8-bit register



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Chapter 1

Overview

1. Overview

1.1 Features

Equipped with a 8-bit CPU nX-U8/100, the ML610Q305/306 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as timer, synchronous serial port, and voice output function. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture. The ML610Q305/306 is also equipped with a flash memory that has achieved low voltage and low power consumption (at read) equivalent to mask ROMs, so it is best suited to battery-driven applications such as alarm and portable devices. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 μs (@32.768kHz system clock)
    Approx 0.244 μs (@4.096 MHz system clock)@V_{DD}=2.0 to 5.5V
    Approx 0.122 μs (@8.192 MHz system clock)@V_{DD}=2.2 to 5.5V

- Internal memory
  - Has 96-Kbyte flash ROM(48K × 16-bits) built in. (1 K byte of test domain that it cannot be used is included)
  - Has 2-Kbyte flash ROM built in. (area in which self rewriting is possible (512byte × 4))
  - Internal 1Kbyte RAM (1K × 8 bits)

- Interrupt controller
  - 2 non-maskable interrupt sources
    Internal source: 1(Watchdog timer)
    External source: 1(NMI)
  - 24 maskable interrupt sources
    Internal source: 16(SSIO0, SSIO1, UART, I^2C bus master/slave interface, Timer 0, Timer 1, Timer 2, Timer 3, A/D converter, Voice sound reproduction, Speaker pin short detection, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External source: 8(P80, P81, P82, P83, P84, P85, P86, P87)

- Time base counter
  - Low-speed time base counter × 1 channel
  - High-speed time base counter × 1 channel

- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s@32.768kHz)

- Timers
  - 8 bits × 4ch (16-bit configuration available)

- Voice output function
  - Voice synthesis method: 4-bit ADPCM2 / non-linear PCM / straight 8-bit PCM / straight 16-bit PCM / HQ-ADPCM
  - Sampling frequency: 8/16/32 kHz; 10.7/21.3 kHz; 6.4/12.8/25.6 kHz

· Successive approximation type A/D converter
  - 10-bit A/D converter
  - Input: 3ch (ch0-2:External input) (for ML610Q305) /
    4ch (ch0-3:External input) (for ML610Q306)
  − Conversion time: 24.4 µs per channel at 4.096MHz V_{DD}≥2.2V
  − Conversion time: 12.2 µs per channel at 8.192MHz V_{DD}≥2.5V
  − Continuous conversion / Single conversion selectable
· Synchronous serial port
  - 2ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

· UART
  − Half-duplex × 1ch
  − TXD/RXD
  − Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  − Positive logic/negative logic selectable
  − Built-in baud rate generator

· I^2C bus interface
  - Master function: standard mode (100 kbps) and Fast mode (400 kbps)
  - Slave function: standard mode (100 kbps) and Fast mode (400 kbps)

· General-purpose ports
  - Input-only port ´ 1ch
  - Output-only port ´ 3ch (including secondary functions)
  - Input/output ´ 12ch (including secondary functions)
    (P40 to P42 uses also as an A/D converter input port.)(for ML610Q305) /
    ´ 15ch (including secondary functions)
    (P40 to P43 uses also as an A/D converter input port.) (for ML610Q306)

· Speaker amplifier(D-class) output power
  − 1.0W(at 5.0V)/0.45W(at 3.0V)
  − Disconnection detection circuit
  − Speaker pin short detection circuit

· Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - PLL oscillation stop detection reset
  - Low level detection (LLD) reset

· Clock
  - Low-speed clock
    Built-in RC oscillation (32.768 kHz)
  - High-speed clock
    Built-in PLL oscillation (Approx. 1.024MHz / 2.048MHz / 4.096MHz / 8.192MHz)

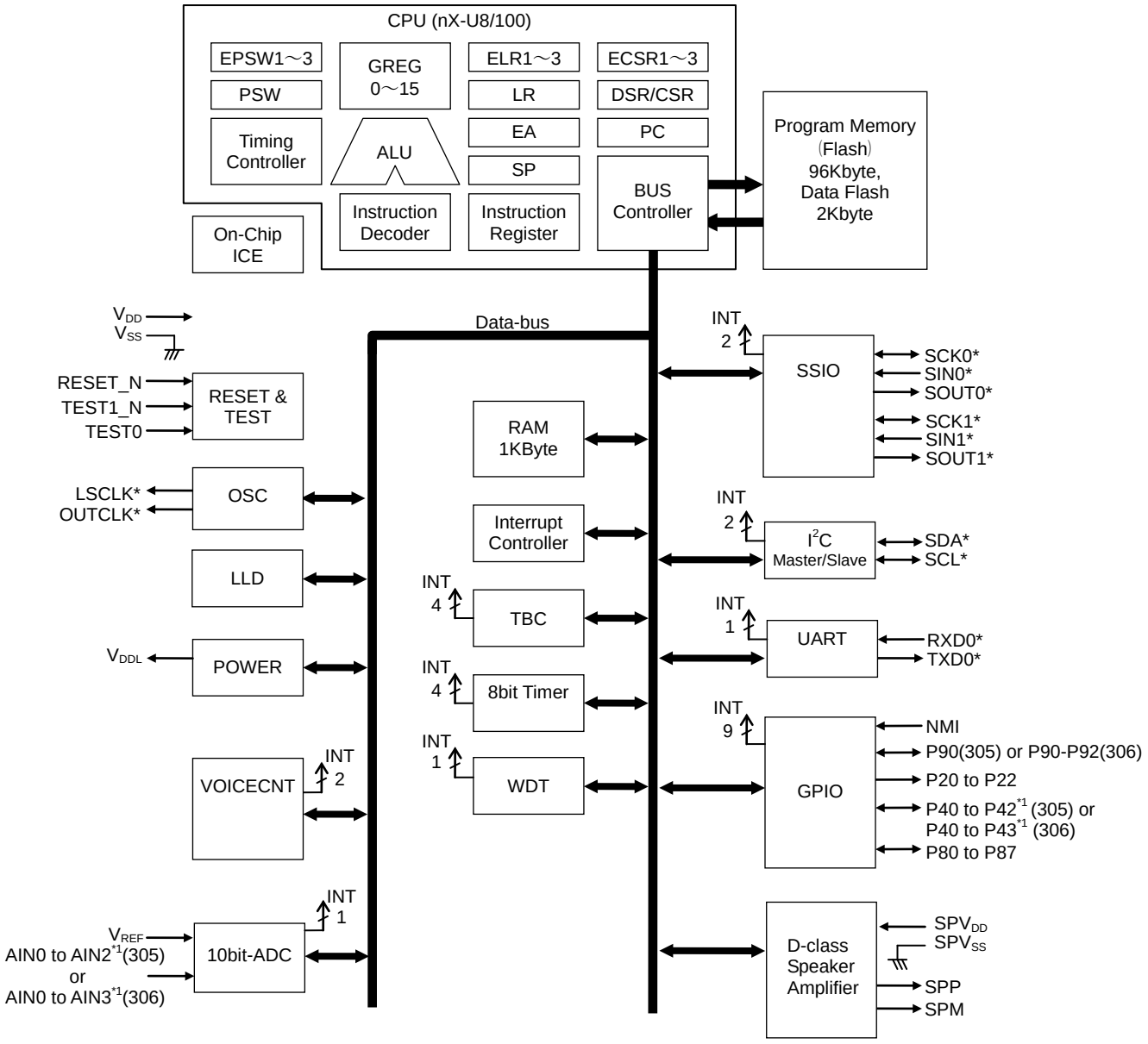
· Power management
  - STOP mode: Stop of oscillation (Operations of CPU and peripheral circuits are stopped.)
  − HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/2, 1/4, 1/8, or 1/16 of the oscillation clock)
  − Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

· Shipment
  - 32-pin WQFN
    ML610Q305-xxxGD (blank product: ML610Q305-NNNGD)
  - 32-pin TQFP
    ML610Q305-xxxTB (blank product: ML610Q305-NNNTB)
  - 36-pin WQFN
    ML610Q306-xxxGD (blank product: ML610Q306-NNNGD)
    xxx: ROM code number

· Guaranteed operating range
  - Operating temperature: - 40°C to 85°C
  - Operating voltage: V_{DD} = 2.0V to 5.5V, SPV_{DD} = 2.0V to 5.5V

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML610Q305/306



*: Secondary or tertiary function
*1: I/O port or A/D converter input terminal

Figure 1-1 Block Diagram of ML610Q305/306

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML610Q305 32-pin WQFN Package (TOP View)

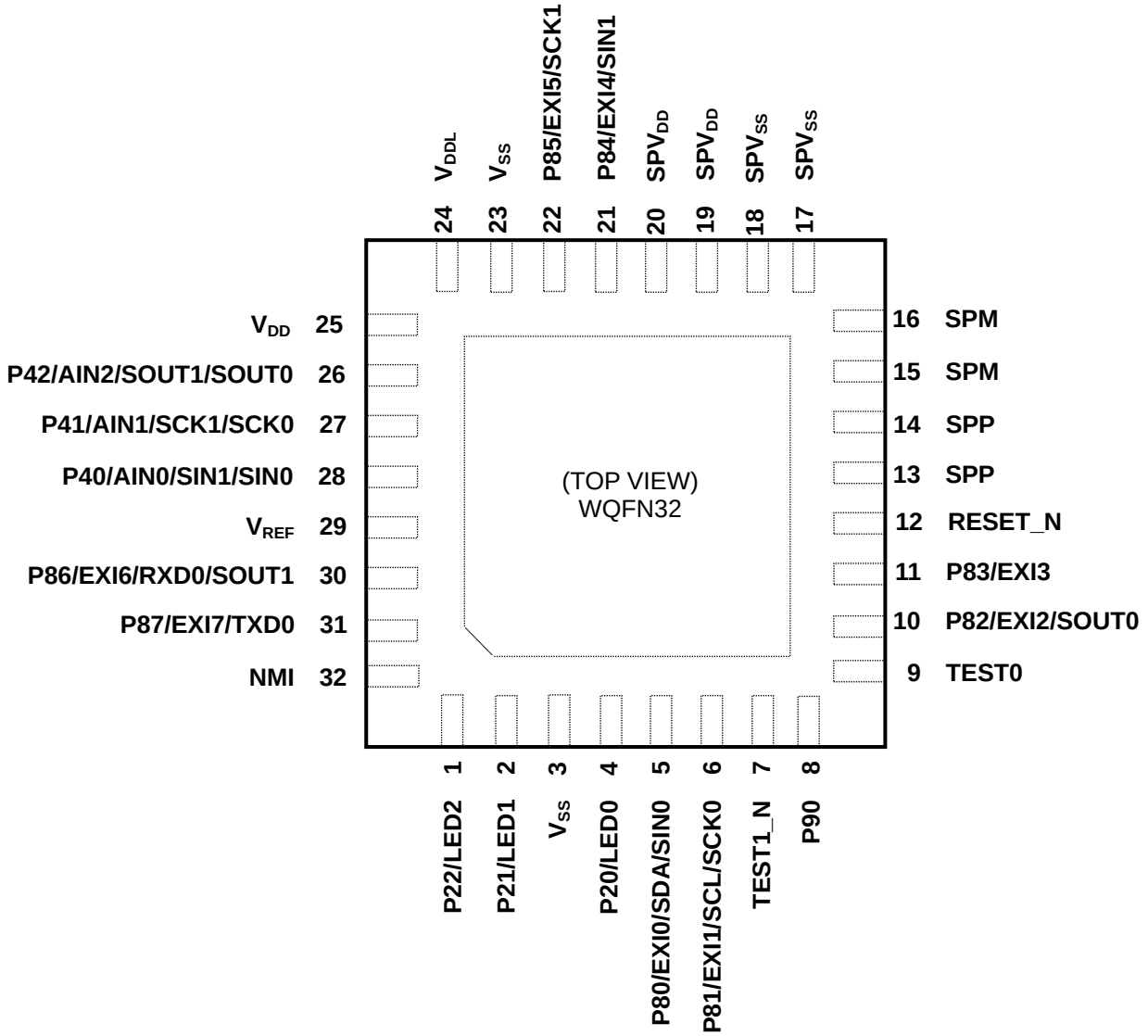


Figure 1-2 Pin Layout of 32-pin WQFN Package

1.3.1.2 Pin Layout of ML610Q305 32-pin TQFP Package (TOP View)

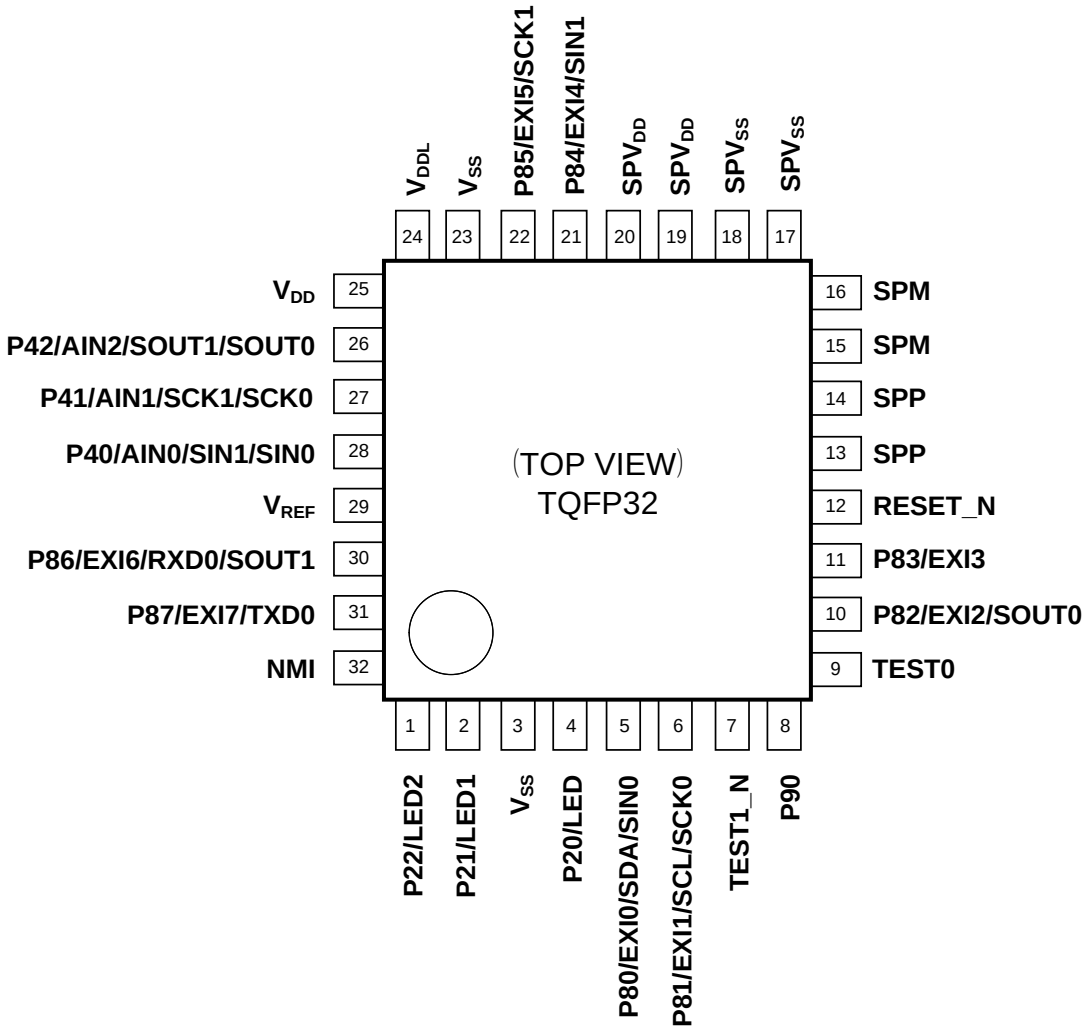


Figure 1-3 Pin Layout of 32-pin TQFP Package

1.3.1.3 Pin Layout of ML610Q306 36-pin WQFN Package (TOP View)

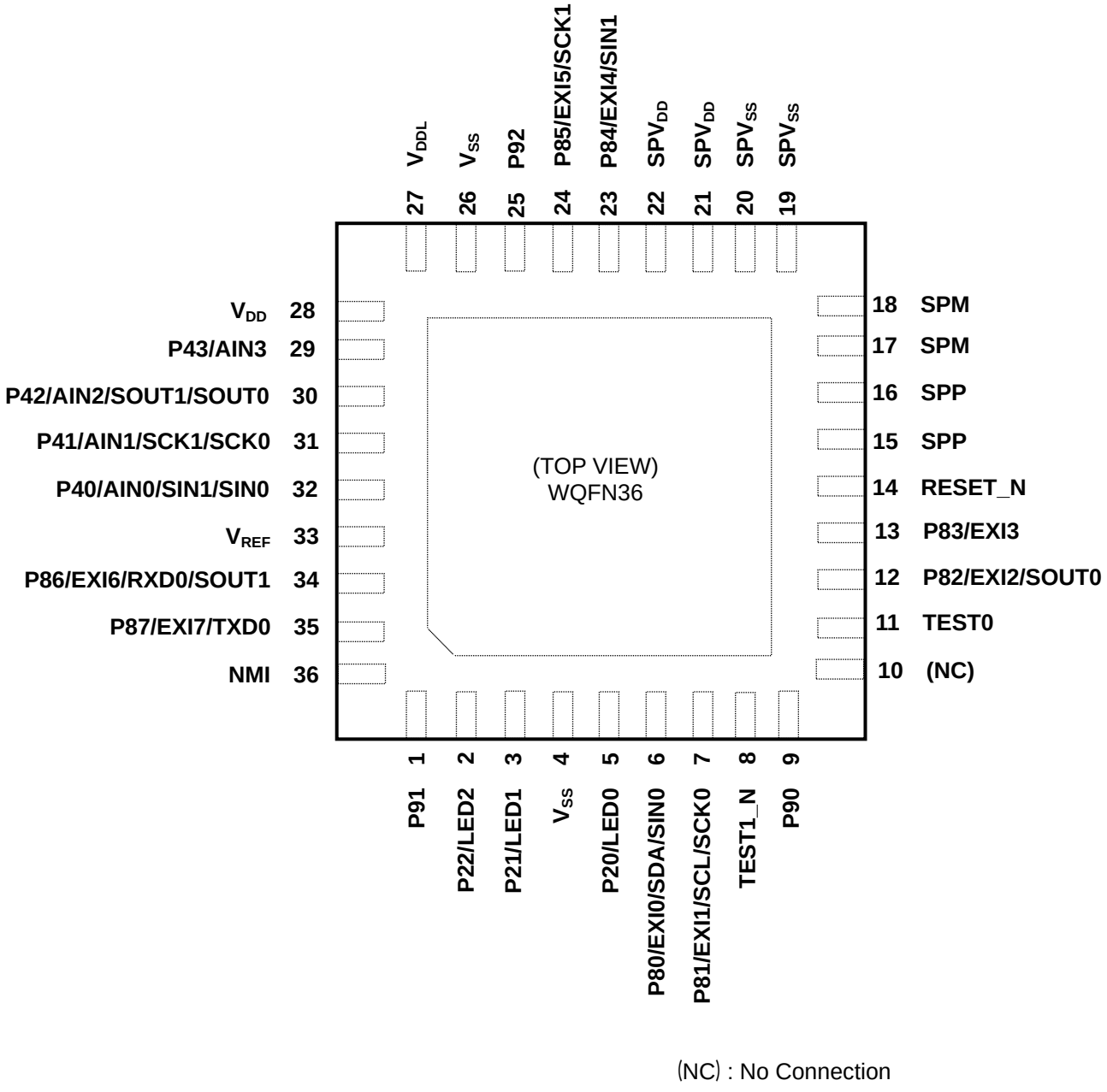


Figure 1-4 Pin Layout of 36-pin WQFN Package

1.3.2 List of Pins

Table 1-1 lists the pins of the ML610Q305/306. In the I/O column, "—" denotes an input pin (for primary functions only), "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Table 1-1 List of Pins

36pin WQFN	32pin WQFN /TQFP	Primary function			Secondary/Tertiary function			
		Pin name	I/O	Description	Secondary/ Tertiary	Pin name	I/O	Description
15, 16	13, 14	SPP	O	Positive output pin of the built-in speaker amplifier	¾	¾	¾	¾
17, 18	15, 16	SPM	O	Negative output pin of the built-in speaker	¾	¾	¾	¾
19, 20	17, 18	SPVss	¾	Negative power supply pin for built-in speaker amplifier	¾	¾	¾	¾
21, 22	19, 20	SPV_{DD}	¾	Positive power supply pin for built-in speaker amplifier	¾	¾	¾	¾
4, 26	3, 23	V_{SS}	¾	Negative power supply pin	¾	¾	¾	¾
27	24	V_{DDL}	¾	Power supply for internal logic (internally generated)	¾	¾	¾	¾
28	25	V_{DD}	¾	Positive power supply pin	¾	¾	¾	¾
33	29	V_{REF}	¾	Reference power supply pin for successive- approximation type ADC	¾	¾	¾	¾
14	12	RESET_N	I	Reset input pin	¾	¾	¾	¾
11	9	TEST0	I/O	Input/output pin for testing	¾	¾	¾	¾
8	7	TEST1_N	I	Input pin for testing	¾	¾	¾	¾
36	32	NMI	I	Input port, non-maskable interrupt	¾	¾	¾	¾
5	4	P20/LED0	O	Output port / LED port	Secondary	LSCLK	O	Low-speed clock output
3	2	P21/LED1	O	Output port / LED port	Secondary	OUTCLK	O	high-speed clock output
2	1	P22/LED2	O	Output port / LED port	¾	¾	¾	¾
9	8	P90	I/O	Input port/Output port	¾	¾	¾	¾
1	¾	P91	I/O	Input port/Output port	¾	¾	¾	¾
25	¾	P92	I/O	Input port/Output port	¾	¾	¾	¾
32	28	P40/AIN0	I/O	Input port/Output port /Successive-approximation type ADC input0	Secondary	SIN1	I	SSIO1 data input
					Tertiary	SIN0	I	SSIO0 data input
31	27	P41/AIN1	I/O	Input port/Output port /Successive-approximation type ADC input1	Secondary	SCK1	I/O	SSIO1 synchronous clock input/output
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
30	26	P42/AIN2	I/O	Input port/Output port /Successive-approximation type ADC input2	Secondary	SOUT1	O	SSIO1 data output
					Tertiary	SOUT0	O	SSIO0 data output
29	¾	P43/AIN3	I/O	Input port/Output port /Successive-approximation type ADC input3	¾	¾	¾	¾
6	5	P80/EXI0	I/O	Input port/Output port / External interrupt	Secondary	SDA	I/O	I^2C synchronous data input/ output
					Tertiary	SIN0	I	SSIO0 data input
7	6	P81/EXI1	I/O	Input port/Output port / External interrupt	Secondary	SCL	I/O	I^2C synchronous clock input/output
					Tertiary	SCK0	I/O	SSIO0 synchronous clock input/output
12	10	P82/EXI2	I/O	Input port/Output port / External interrupt	¾	¾	¾	¾
					Tertiary	SOUT0	O	SSIO0 data output
13	11	P83/EXI3	I/O	Input port/Output port / External interrupt	¾	¾	¾	¾
23	21	P84/EXI4	I/O	Input port/Output port / External interrupt	Tertiary	SIN1	I	SSIO1 data input
24	22	P85/EXI5	I/O	Input port/Output port / External interrupt	Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
34	30	P86/EXI6	I/O	Input port/Output port / External interrupt	Secondary	RXD0	I	UART0 data
					Tertiary	SOUT1	O	SSIO1 data
35	31	P87/EXI7	I/O	Input port/Output port / External interrupt	Secondary	TXD0	O	UART0 data output

Note:
The function which is not chosen is lost when either a secondary function or a tertiary function is chosen. However, when using it as an input, read-out of an input data is possible at a PnD.

1.3.3 Pin Description

Table 1-2 shows the pin description.
In the I/O column, "—" denotes an input pin, "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Table 1-2 Pin Description

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated) Connect a capacitor (C_L:1uF) between V_{DDL} and V_{SS} .	—	—
SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—
SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—
V_{REF}	—	Reference power supply pin for successive-approximation type ADC	—	—
Test				
TEST0	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
TEST1_N	I	Input pin for testing. Has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a "H" level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose Output port				
P20 to P22	O	General-purpose output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
General-purpose Input/output port				
P40 to P42	I/O	General-purpose input/output ports. Provided with a tertiary function. Cannot be used as ports if their tertiary function is used.	Primary	Positive
P43	I/O	General-purpose input/output port. (built into ML610Q306)	Primary	Positive
P80 to P87	I/O	General-purpose input/output ports. Provided with a secondary function or a tertiary function. Cannot be used as ports if their secondary function or tertiary function is used.	Primary	Positive
P90	I/O	General-purpose input/output ports.	Primary	Positive
P91 to P92	I/O	General-purpose input/output port. (built into ML610Q306)	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P80 pin. This pin has a Nch open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock output pin. This pin is used as the secondary function of the P81 pin. This pin has a Nch open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and P80 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin and P81 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin and P82 pin.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P84 pin and the secondary function of the P40 pin.	Secondary/ Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P85 pin and the secondary function of the P41 pin.	Secondary/ Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P86 pin and the secondary function of the P42 pin.	Secondary/ Tertiary	Positive
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P87 pin.	Secondary	Positive
RXD0	I	UART0 data input pin. Allocated to the secondary function of the P86 pin.	Secondary	Positive
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0 to 7	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P80 to P87 pins.	Primary	Positive/ Negative
LED drive				
LED0 to 2	O	Pins for LED driving. Allocated to the primary function of the P20 to P22 pins.	Primary	Positive/ Negative
Voice output function				
SPP	O	Positive output pin of the internal speaker amplifier.	—	—
SPM	O	Negative output pin of the internal speaker amplifier.	—	—
Successive-approximation type A/D converter				
AIN0 to 2	I	Analog inputs to Ch0 to Ch2 of the successive-approximation type A/D converter. Allocated to the primary function of the P40 to P42 pins.	Primary	—
AIN3	I	Analog inputs to Ch3 of the successive-approximation type A/D converter.(built into ML610Q306) Allocated to the primary function of the P43 pin.	Primary	—

1.3.4 Termination of Unused Pins

Table 1-3 shows the recommended termination of unused pins.

Table 1-3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST0	Open
TEST1_N	Open or connect to V_{DD}*
V_{REF}	Connect to V_{DD}
P40 to P42 (AIN0 to AIN2)	Open
P43(AIN3) (built into ML610Q306)	Open
SPV_{DD}	Connect to V_{DD}
SPV_{SS}	Connect to V_{SS}
SPP	Open
SPM	Open
P20 to P22	Open
P80 to P87	Open
P90	Open
P91 to P92(built into ML610Q306)	Open
NMI	Open or connect to V_{DD} *

*: TEST1_N pin (Typ.10kΩ) and NMI pin (Typ.100kΩ) have the built-in pull-up resistor. It is recommened to connect to V_{DD} or be pulled up by around 1kΩ resistor in a severe enviroment such as noise.

Notes:
· The unused input ports or unused input/output ports should not be configured as high-impedance inputs and left open. If the corresponding pins are configured as high-impedance inputs and left open, because the input buffer of both Nch and Pch MOS transistor turn on, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.
· When the power is turned on, the state of the general-purpose port is undefined. Therefore, there is a possibility of outputting high-level or low-level.If the undefined state at the power-on is a problem, take measures with the peripheral components on the user board.

Chapter 2

CPU and Memory Space

2. CPU and Memory Space

2.1 Overview

This LSI incorporates 8-bit CPU nX-U8/100, and a SMALL model is selected for the memory model.
For details of the CPU nX-U8/100, refer to the "nX-U8/100 Core Instruction Manual".

2.2 Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by 20 bits consisting of higher 4 bits as code segment register (CSR) and lower 16 bits as program counter (PC).
The ROM window area contains data having a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors. The software interrupt vectors area not to use can be used as program codes area.
The program memory space consists of 2 segments and has a total capacity of 96 Kbytes (48 Kwords).
Figure 2-1 shows the configuration of the program memory space.

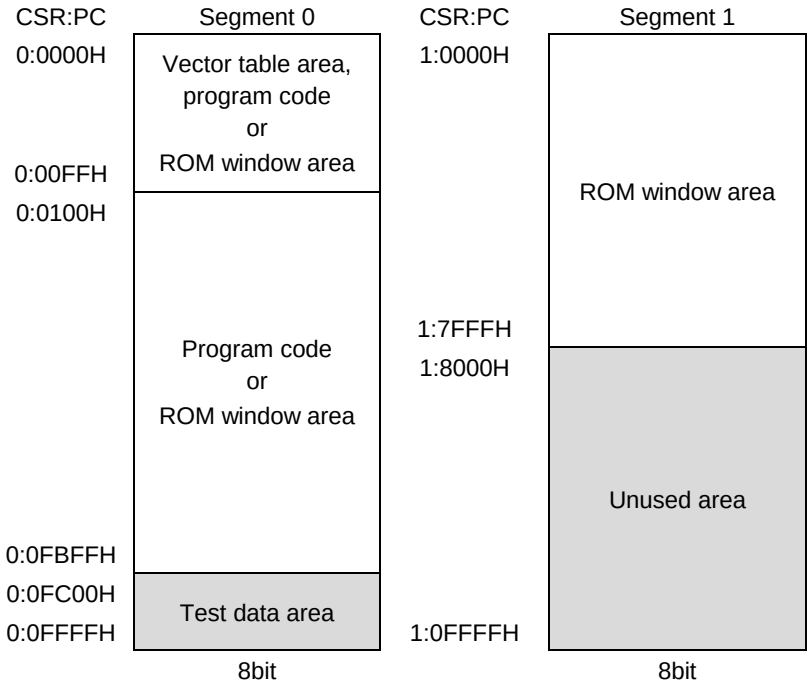


Figure 2-1 Configuration of Program Memory Space

Notes:
· The 1-Kbyte (512-word) test data area (0:0FC00H to 0:0FFFFH) of Segment 0 cannot be used as a program code area. In the test data area, the area 0:0FC00H to 0:0FDFFH is writable and erasable and the area 0:0FE00H to 0:0FFFFH is disabled for both write and erase. Set Code Options in the test data area 0:0FDE0H to 0:0FDE1H. Always write "0FFH" to the test data area 0:0FC00H to 0:0FDDFH and 0:0FDE2H to 0:0FDFFH for writable. If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code can not be guaranteed.
· Set "0FFH" data (BRK instruction) in the unused area of the program memory space for fail-safe reasons. It is possible using HTU8(program development support software). For details of the HTU8, refer to "HTU8 User's Manual". For details of BRK instruction, refer to "nx-U8/100 Core Instruction Manual".

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area, 1Kbyte RAM area, and SFR area of Segment 0, and the ROM reference area of Segment 1, and the data flash area of Segment 2, and the ROM reference area of Segment 8 to 9, and the data flash area of Segment A.
The data memory have a length of 8 bits and are specified by 20 bits consisting of higher 4 bits as DSR and lower 16 bits as addressing specified by instructions.
Figure 2-2 shows the configuration of the data memory space.

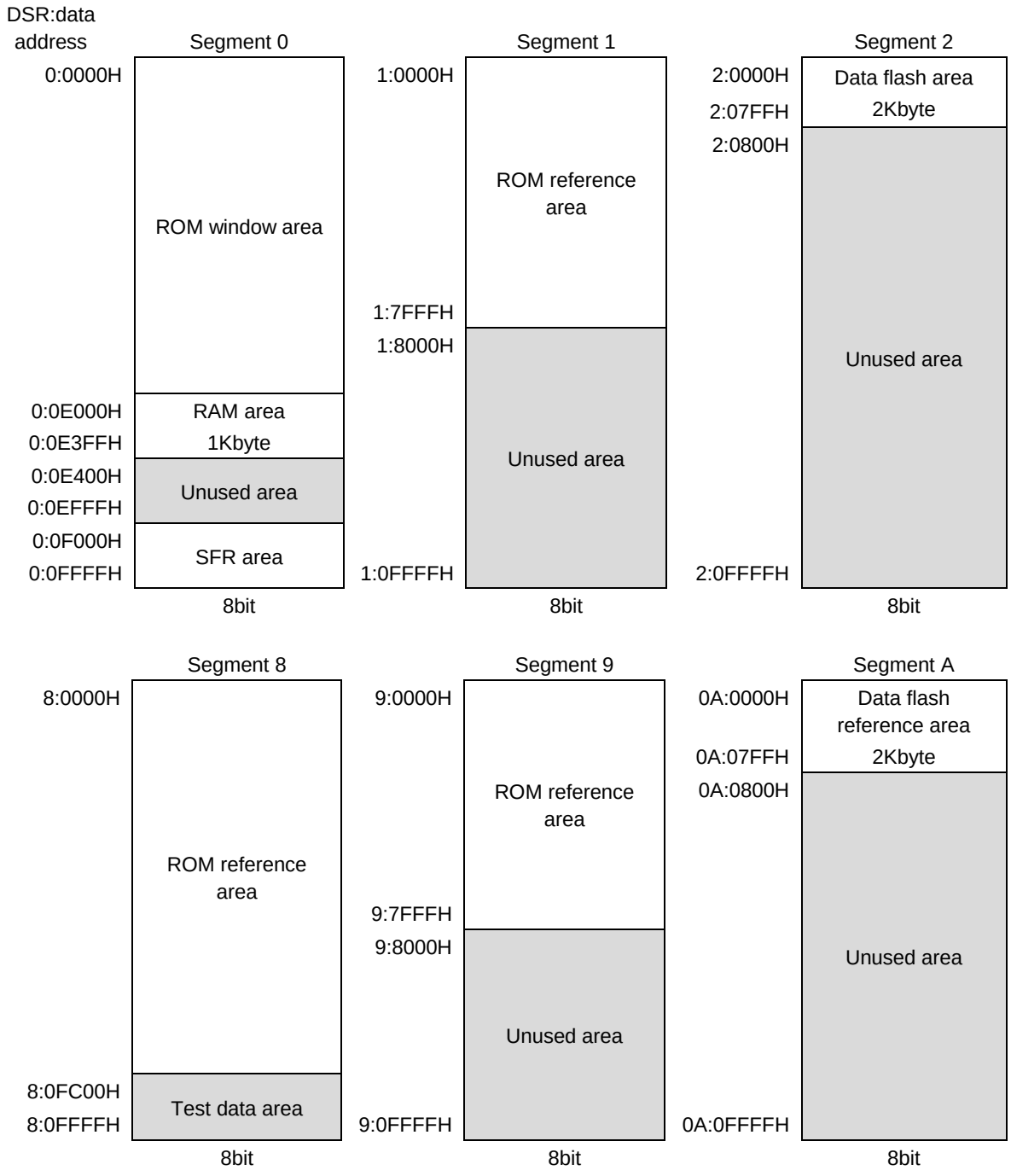


Figure 2-2 Configuration of Data Memory Space

Notes:
· The contents of the 1Kbyte RAM area are undefined at system reset. Initialize this area by software.
· Although Segment 0 of the program memory space and Segment 0 of the data memory space are separate spaces, the contents of Segment 0 of the program memory space can be read through the ROM window area of the data memory space. However, 0:0E000H to 0:0FFFFH cannot be read because it overlaps the RAM/SFR area. Read from the ROM reference area of Segment 8.
· The Segment 8 is the mirror area of Segment 0 in the program memory space. The contents of Segment 0 of the program memory space is read from the ROM reference area of Segment 8.
· The Segment 9 is the mirror area of Segment 1 in the program memory space. The contents of Segment 1 of the program memory space is read from the ROM reference area of Segment 9.
· The Segment A is the mirror area of Segment 2. The contents of Segment 2 of the data flash area is read from the data flash reference area of Segment A.

2.4 Instruction Length

One instruction has a length of 16 bits.

2.5 Data Type

The two data types of byte (8 bits) and word (16 bits) are supported.

2.6 Description of Registers

2.6.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	¾	R/W	8	00H

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	¾	¾	¾	¾	DSR3	DSR2	DSR1	DSR0
R/W	¾	¾	¾	¾	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) used to retain a data segment. For details of DSR, refer to the "nX-U8/100 Core Instruction Manual".

[Description of Bits]

· **DSR3 to DSR0** (bits 3 to 0)

DSR3	**DSR2**	**DSR1**	**DSR0**	Description
0	0	0	0	Data segment 0 (initial value)
0	0	0	1	Data segment 1
0	0	1	0	Data segment 2
0	0	1	1	Setting prohibited
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	Data segment 8
1	0	0	1	Data segment 9
1	0	1	0	Data segment A
1	0	1	1	Setting prohibited
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Chapter 3

Clock Generation Circuit

3. Clock Generation Circuit

3.1 Overview

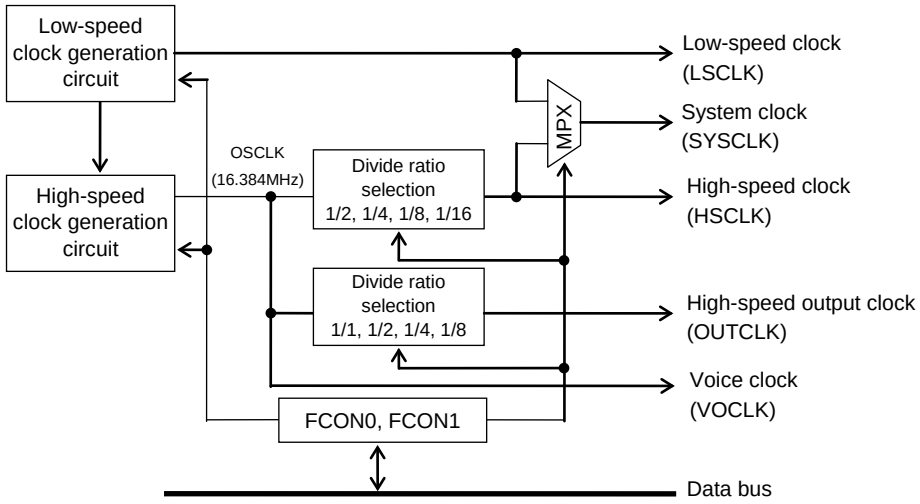
The clock generation circuit generates and supplies a low-speed clock (LSCLK), high-speed clock (HSCLK), system clock (SYSCLK), and high-speed output clock (OUTCLK). LSCLK and HSCLK operate as the time-base clocks for peripheral circuits, SYSCLK as the basic operating clock of the CPU, and OUTCLK and LSCLK as the clock to be output from ports.
For the output ports used for OUTCLK and LSCLK, see Chapter 6, "Port 2".
For the STOP mode mentioned in this chapter, see Chapter 5, "MCU Control Function".

3.1.1 Features

· Low-speed clock generation circuit:
  - Built-in RC oscillation
· High-speed clock generation circuit:
  - Built-in PLL oscillation

3.1.2 Configuration

Figure 3-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1

Figure 3-1 Configuration of Clock Generation Circuit

Note:
After power-on or a system reset, SYSCLK starts operating with the clock generated by dividing high-speed clock generation circuit output clock by 16. And HSCLK starts operating with the clock generated by dividing the OSCLK by 16. During initialization by software, set the FCON0 or FCON1 register so as to switch the clock to the required one.

3.1.3 Clock Configuration

Figure 3-2 shows the clock condiguration.

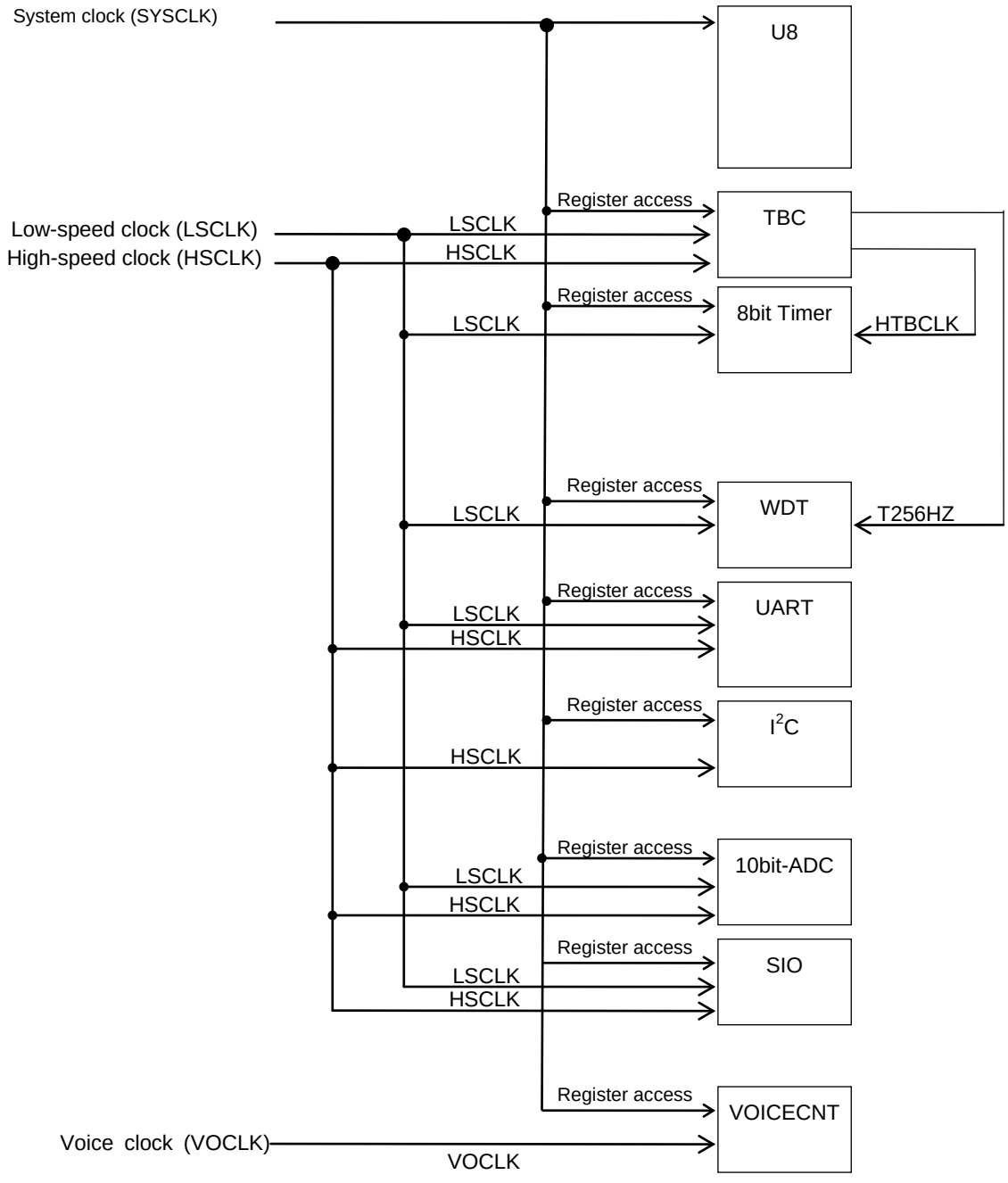


Figure 3-2 Clock Configuration

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	83H

3.2.2 Frequency Control Register 0(FCON0)

Address: 0F002H
Access: R/W
Access size: 8/16 bits
Initial value: 33H

	7	6	5	4	3	2	1	0
FCON0	¾	¾	OUTC1	OUTC0	¾	¾	SYSC1	SYSC0
R/W	-	-	R/W	R/W	-	-	R/W	R/W
Initial value	0	0	1	1	0	0	1	1

FCON0 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

· **SYSC1, SYSC0** (bits 1, 0)
The SYSC1 and SYSC0 bits are used to select the frequency of the system clock (SYSCLK) and high-speed clock (HSCLK). 1/2OSCLK, 1/4OSCLK, 1/8OSCLK, or 1/16OSCLK can be selected.
At system reset, 1/16OSCLK is selected.

SYSC1	SYSC0	Description	Frequency(PLL oscillation)(typ)
0	0	1/2OSCLK	8.192MHz(16.384MHz/2)
0	1	1/4OSCLK	4.096MHz(16.384MHz/4)
1	0	1/8OSCLK	2.048MHz(16.384MHz/8)
1	1	1/16OSCLK (Initial value)	1.024MHz(16.384MHz/16)

· **OUTC1, OUTC0** (bits 5, 4)
The OUTC1 and OUTC0 bits are used to select the frequency of the high-speed output clock which is output when the secondary function of the port is used.
OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.
At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description	Frequency(PLL oscillation)(typ)
0	0	OSCLK	16.384MHz
0	1	1/2OSCLK	8.192MHz
1	0	1/4OSCLK	4.096MHz
1	1	1/8OSCLK (Initial value)	2.048MHz

Note:
The maximum operating frequency guaranteed for the system clock (SYSCLK) of this LSI is 8.4 MHz.

3.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H
Access: R/W
Access size: 8 bits
Initial value: 83H

	7	6	5	4	3	2	1	0
FCON1	LPLL	¾	¾	¾	¾	¾	ENOSC	SYSCLK
R/W	R	-	-	-	-	-	R/W	R/W
Initial value	1	0	0	0	0	0	1	1

FCON1 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]

· **SYSCLK** (bit 0)
The SYSCLK bit is used to select system clock. It allows selection of the low-speed clock (LSCLK) or HSCLK (1/nOSCLK: n = 2, 4, 8, 16) selected by using the high-speed clock frequency select bit (SYSC1, 0) of FCON0.
When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK
1	HSCLK (initial value)

· **ENOSC** (bit 1)
The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator.

ENOSC	Description
0	Disables high-speed oscillation
1	Enables high-speed oscillation (initial value)

· **LPLL** (bit 7)
The LPLL bit is used as a flag to indicate the oscillation state of PLL oscillation.
When the LPLL bit is set to "1", this indicates that PLL oscillation can be used. When the LPLL bit is set to "0", this indicates that the PLL oscillation is inactive or the PLL oscillating clock is under count..
LPLL is a read-only bit.

LPLL	Description
0	The status which the PLL oscillation has stopped, or the status which a PLL oscillation clock is continuing counting.
1	The status which is carrying out the supply startup of the OSCLK after counting a PLL oscillation clock 16384 times. (initial value)

Note:
The LPLL flag is a reference flag.

3.3 Description of Operation

3.3.1 Low-Speed Clock

3.3.1.1 Low-Speed Clock Generation Circuit

Figure 3-3 shows the configuration of the low-speed clock generation circuit.
Supply of the low-speed oscillation clock (LSCLK) is started when the high-speed clock pulse count reaches 128.

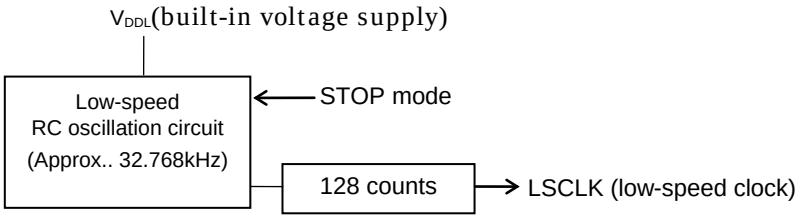


Figure 3-3 Low-speed clock generation circuit

3.3.1.2 Operation of the Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power ON reset.
A low-speed clock (LSCLK) is supplied to the peripheral circuits after the elapse of the low-speed oscillation start period (T_{XTL} : less than 10 LSCLK periods) and oscillation stabilization period of 128 low-speed RC oscillation clock counts after powered on.
The low-speed clock generation circuit stops the oscillation in STOP mode. When oscillation is resumed by releasing of the STOP mode by external interrupt, LSCLK is supplied to the peripheral circuits after the elapse of the low-speed oscillation start period (T_{XTL}) and low-speed clock (LSCLK) oscillation stabilization period (128 counts).
Figure 3-4 shows the waveforms of the low-speed clock generation circuit.

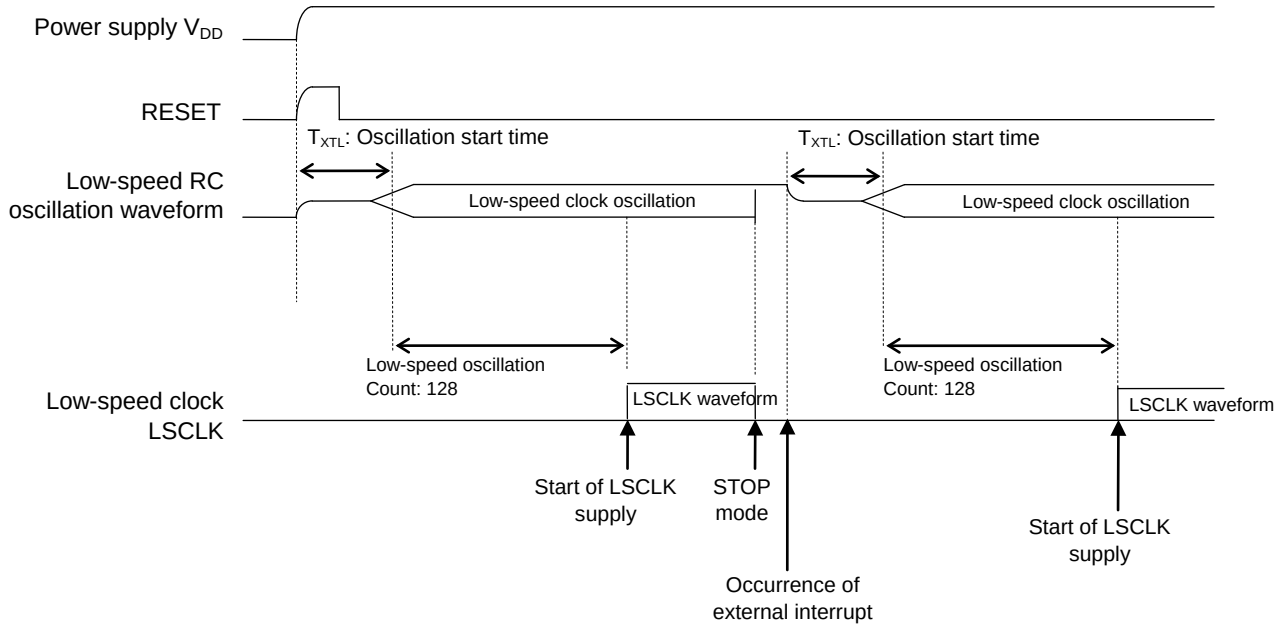


Figure 3-4 Operation of the Low-Speed Clock Generation Circuit

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3.3.2 High-Speed Clock

3.3.2.1 High-Speed Clock Generation Circuit

The PLL oscillation circuit on high-speed clock generation circuit generates a clock of 16.384 MHz multiplied low-speed clock by 500.
In built-in PLL oscillation mode, supply of OSCLK (high-speed oscillation clock) is started when PLL oscillation clock pulse count reaches 16384 after oscillation is enabled (ENOSC is set to "1").
Figure 3-5 shows the configuration of high-speed clock generation circuit.

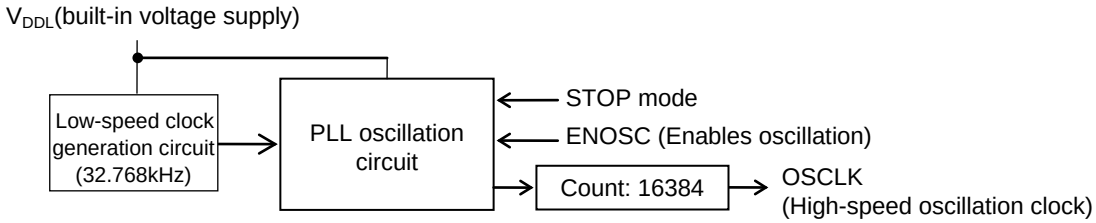


Figure 3-5 Configuration of High-Speed Clock Generation Circuit

3.3.2.2 Operation of High-Speed Clock Generation Circuit

The High-speed clock generation circuit is activated by the occurrence of power ON reset in a built-in PLL oscillation mode. As a result of the occurrence of a power-on reset, the circuit enters system reset mode and then shifts to program operating mode after a lapse of the high-speed oscillation start time (T_{XTH} : less than 1 LSCLK period) and the oscillation stabilization time (Count: 262144) of the high-speed oscillation clock (OSCLK) and at the same time, the high-speed clock (HSCLK) is supplied to the peripheral circuits.
Figure 3-6 shows the waveforms of the high-speed clock generation circuit at power-on.

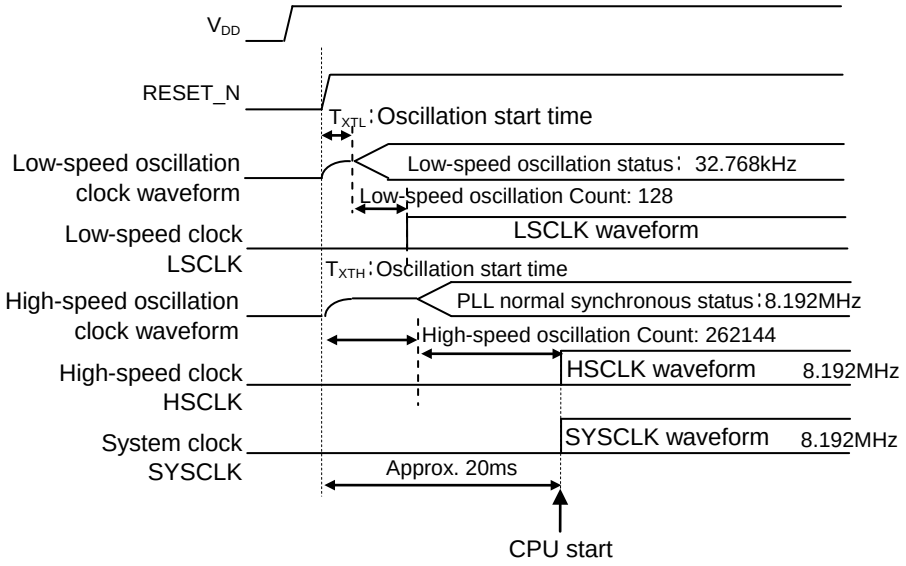


Figure 3-6 Operation of the High-Speed Clock Generation Circuit at Power-On

In High-Speed Clock Generation Circuit, the oscillation start/stop can be controlled by Frequency Control register 1(FCON1). When ENOSC bit of FCON1 is set to "1", high-speed oscillation is started. After the start of oscillation, HSCLK starts to be supplied to the peripheral circuits following a lapse of the high-speed oscillation start period (T_{XTH}: less than 1 LSCLK period) in each mode and the oscillation stabilization period of the high-speed oscillation clock.
The high-speed clock generation circuit stops oscillation when it enters STOP mode by software. It resumes oscillation when the STOP mode is released by an external interrupt. Then, HSCLK starts to be supplied to the peripheral circuits following a lapse of the high-speed oscillation start period (T_{XTH}) in each mode and the oscillation stabilization period of the high-speed clock (OSCLK). The oscillation stabilization period is the duration of 16384 clock pulses.
Figure 3-7 shows the waveforms of the high-speed clock generation circuit.

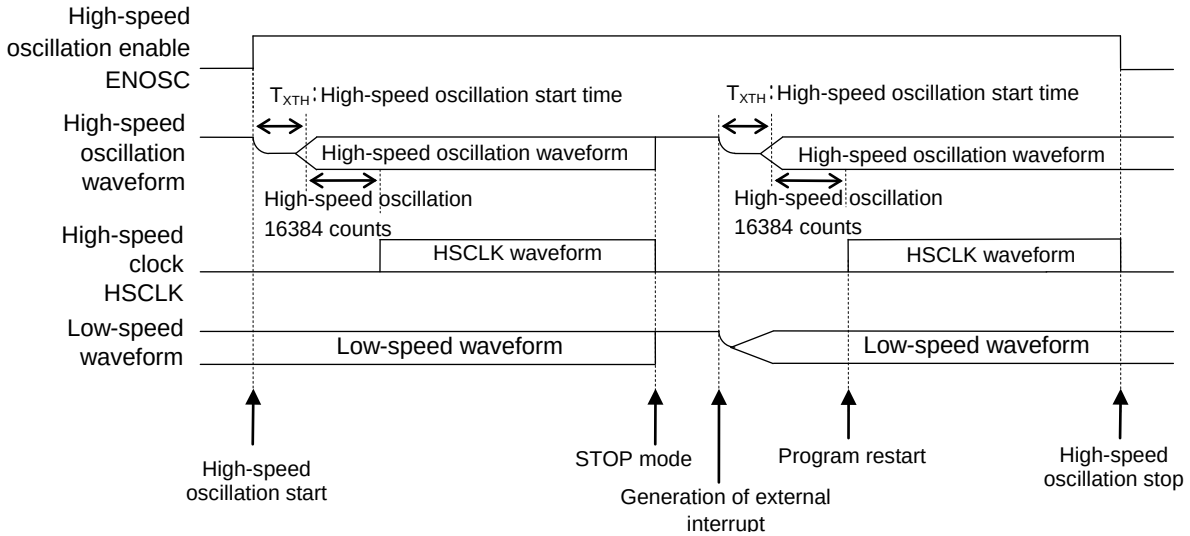


Figure 3-7 Operation of the High-Speed Clock Generation Circuit

3.3.3 Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 3-8 shows a flow of system clock switching processing (HSCLK® LSCLK) and Figure 3-9 shows a flow of system clock switching processing (LSCLK® HSCLK).

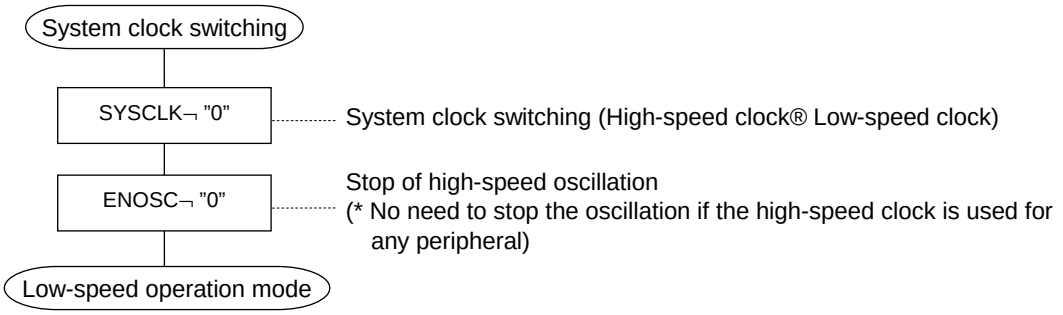


Figure 3-8 Flow of System Clock Switching Processing (HSCLK® LSCLK)

Note:
Immediately after the power-on or the return from the STOP mode, if the system clock is switched from HSCLK to LSCLK, the CPU becomes inactive until LSCLK starts clock supply to the peripheral circuits. Therefore, it is recommended to switch to LSCLK after confirming that the LSCLK is oscillating by checking that the time base counter interrupt request bit (128Hz interrupt request: Q128H) is "1" after the power-on or the recovery from the STOP mode.

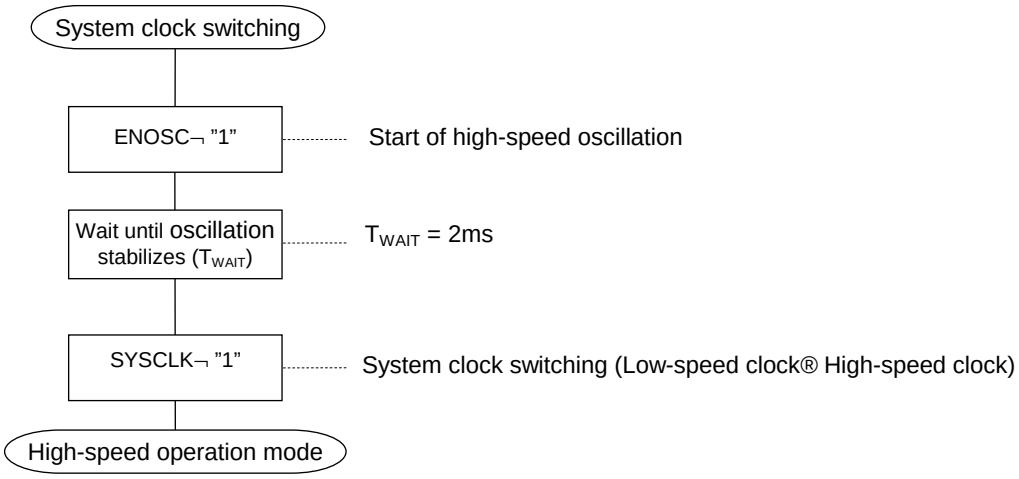


Figure 3-9 Flow of System Clock Switching Processing (LSCLK® HSCLK)

Note:
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

Chapter 4

Reset Function

4. Reset Function

4.1 Overview

This LSI has the five reset functions shown below. If any of the five reset conditions is satisfied, this LSI enters system reset mode.

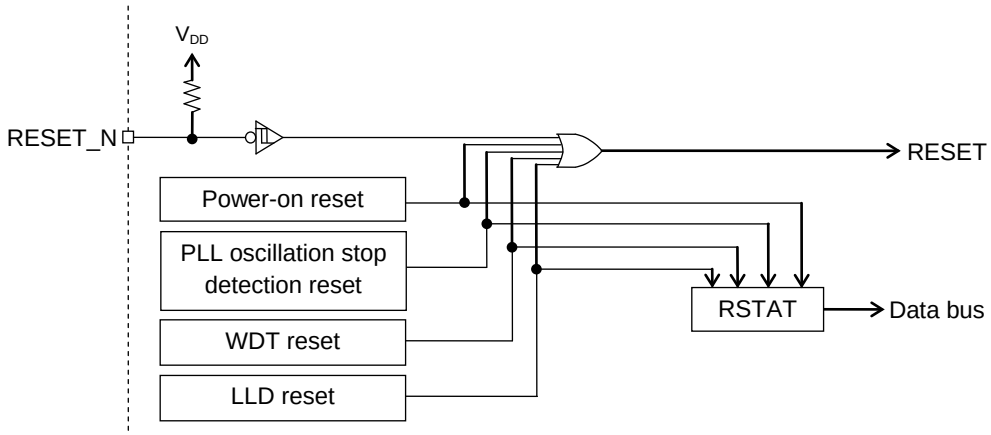
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd watchdog timer (WDT) overflow
- Reset by PLL oscillation stop detection
- Software reset by execution of the BRK instruction
- Low level detection (LLD) reset

4.1.1 Features

- The RESET_N pin has an internal pull-up resistor
- 125 ms, 500ms, 2 sec, or 8 sec can be selected as the watchdog timer (WDT) overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- PLL oscillation stop detection time(T_{STOP}) is Typ.19us(@4.096MHz)
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset)
- Low level detection (LLD) reset

4.1.2 Configuration

Figure 4-1 shows the configuration of the reset generation circuit.



RSTAT ：Reset status register

Figure 4-1 Configuration of Reset Generation Circuit

4.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F001H	Reset status register	RSTAT	–	R/W	8	—

4.2.2 Reset Status Register (RSTAT)

Address : 0F001H
Access : R/W
Access size : 8 bits
Initial value : Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	—	—	LLDR	—	WDTR	XSTR	POR
R/W	—	—	—	R/W	—	R/W	R/W	R/W
Initial value	0	0	0	0/1	0	0/1	0/1	0/1

RSTAT is a special function register (SFR) that indicates the causes by which the reset is generated.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the contents of RSTAT to "00H".

[Description of Bits]

· **POR** (bit 0)
The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not generated
1	Power-on reset generated

· **XSTR** (bit 1)
The XSTR bit is a flag that indicates that PLL oscillation stop detection reset is generated. When a PLL oscillation stops in the status of SPEN="1" in more than T_{STOP}, a device begins a reset processing. Please be sure to read the XSTR bit of RSTAT before starting a voice sound reproducing. When the PLL oscillation stop detection reset has occurred on that occasion, please set a XSTR bit to "0."

XSTR	Description
0	PLL oscillation stop detection reset not occurred
1	PLL oscillation stop detection reset occurred

· **WDTR** (bit 2)
The WTDR is a flag that indicates that the watchdog timer reset by 2nd overflow is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

· **LLDR** (bit 4)
The LLDR is a flag that indicates that the low level detection reset occurred.

LLDR	Description
0	Low level detection (LLD) reset not occurred
1	Low level detection (LLD) reset occurred

Notes:
· No flag is provided that indicates the occurrence of reset by the RESET_N pin.
· The POR bit may become "1" even if a power-on reset doesn't occur at power-on. When judging power on, it is recommended to use random value RAM at power-on. It can be judged by checking whether the value of the RAM that was written beforehand changed when the power was turned on.

4.3 Description of Operation

4.3.1 Operation of System Reset Mode

System reset has the highest priority among all the processings and any other processing being executed up to then is cancelled. The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by watchdog timer (WDT) overflow
- Reset by PLL oscillation stop detection
  (A reset processing is started when a speaker-amp carries out the PLL oscillation stop detection only of the ON status.(SPEN="1"))
- Software reset by the BRK instruction (only the CPU is reset)
- Low level detection (LLD) reset

In system reset mode, the following processing is performed.

(1) The power circuit is initialized, but not initialized by the reset by the BRK instruction execution. For the details of the power circuit, refer to Chapter 22, "Power Circuit".
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A "Registers" for the initial values of the SFRs.
(3) CPU is initialized.
   - All the registers in CPU are initialized.
   - The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
   - The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEVEL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U8/100 Core Instruction Manual".

Notes:
· In system reset mode, the contents of data memory(RAM) and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
· In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

Chapter 5

MCU Control Function

5. MCU Control Function

5.1 Overview

The operating states of this LSI are classified into the following 4 modes including system reset mode:

(1) System reset mode
(2) Program run mode
(3) HALT mode
(4) STOP mode

For system reset mode, see Chapter 4, "Reset Function".
And, this LSI has a block control function which enables reducing power consumption by shutting the unused operation (reset the register and stop the clock) of the function.

5.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where high-speed oscillation and low-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Built-in block control function, which shut the unused operation(reset the register and stop the clock) of the function.

5.1.2 Configuration

Figure 5-1 shows an operating state transition diagram.

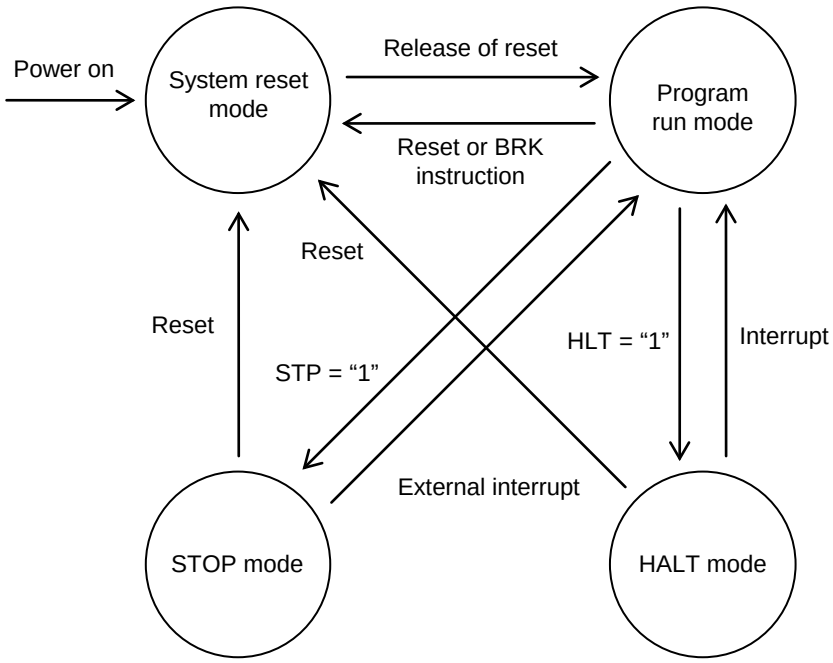


Figure 5-1 Operating State Transition Diagram

5.2 Description of Registers

5.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	¾	W	8	00H
0F009H	Standby control register	SBYCON	¾	W	8	00H
0F028H	Block control register 0	BLKCON0	¾	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	¾	R/W	8	00H
0F02BH	Block control register 3	BLKCON3	¾	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	¾	R/W	8	00H

5.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
STPACP	d7	d6	d5	d4	d3	d2	d1	d0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

STPACP is a write-only special function register (SFR) that enables a transition to the STOP mode.
When STPACP is read, "00H" is read.
When data is written to STPACP in the order of "5nH" and "0AnH"(n: an arbitrary value from 0H to 0FH), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to "1" in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes "5nH" to STPACP and the instruction that writes "0AnH", the stop code acceptor is enabled after "0AnH" is written. However, if data other than "0AnH" is written to STPACP after "5nH" is written, the "5nH" write processing becomes invalid so that data must be written again starting from "5nH".

As fail-safe, it is recommended to switch to the STOP mode with the interrupt used for canceling the STOP mode definitely set. For that purpose, it is recommended to set "1" to STP of STBYCON after setting the interrupt to be used for STOP mode cancellation, with the Stop code acceptor permitting the shift to STOP mode.
At system reset, transition to STOP mode is prohibited.

Note:
The stop code acceptor is not enabled on the condition that the master interruput enable flag(MIE) of nX-U8/100 core program status word(PSW) is "0", and both the interrupt enable flag and the interrupt request flag are "1".

5.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	¾	¾	¾	¾	¾	¾	STP	HLT
R/W	-	-	-	-	-	-	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control operating mode of MCU.

[Description of Bits]

· **HLT** (bit 0)
The HLT bit is used for setting a HALT mode. When the HLT bit is set to "1", the mode is changed to the HALT mode. When the non-maskable interrupt request, or enabled (the interrupt enable flag is "1") interrupt request is issued, the HLT bit is set to "0" and the mode is returned to program run mode.

· **STP** (bit 1)
The STP bit is used for setting the STOP mode. When the STP bit is set to "1" with the stop code adapter enabled by using STPACP, the mode is changed to the STOP mode. The STP bit can't be set to "1" when the transition to the STOP mode is prohibited.
When an interrupt occurs, the STP bit is set to "0" and returns to program operation mode. For the interrupt that can cancel the STOP mode, refer to 5.3.3 STOP mode.

STP	HLT	Description
0	0	Program run mode (initial value)
0	1	HALT mode
1	0	STOP mode
1	1	Prohibition of use

Notes:
· The mode can not be changed to HALT mode or STOP mode on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1" and master interrupt enable flag (MIE) of the program status word (PSW) in the nX-U8/100 core is "0".
· When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U8/100 core is "0", the STOP mode and the HALT mode are simply released and interrupt processing is not performed. Refer to the "nX-U8/100 Core Instruction Manual" for details of PSW.

5.2.4 Block Control Register 0 (BLKCON0)

Address: 0F028H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON0	¾	¾	¾	¾	DTM3	DTM2	DTM1	DTM0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON0 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

· **DTM0** (bit 0)
DTM0 controls the timer 0 operation.

DTM0	Description
0	Enables Timer 0 operation (initial value).
1	Disables Timer 0 operation.

· **DTM1** (bit 1)
DTM1 controls the timer 1 operation.

DTM1	Description
0	Enables Timer 1 operation (initial value).
1	Disables Timer 1 operation.

· **DTM2** (bit 2)
DTM2 controls the timer 2 operation.

DTM2	Description
0	Enables Timer 2 operation (initial value).
1	Disables Timer 2 operation.

· **DTM3** (bit 3)
DTM3 controls the timer 3 operation.

DTM3	Description
0	Enables Timer 3 operation (initial value).
1	Disables Timer 3 operation.

Notes:
· If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
· Refer to Chapter 12, "Timers" for details of the timer operation.

5.2.5 Block Control Register 2 (BLKCON2)

Address: 0F02AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	DI2C0	DI2C1	¾	¾	¾	DUA0	DSIO1	DSIO0
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

· **DSIO0** (bit 0)
DSIO0 controls the operation of the synchronous serial port 0.

DSIO0	Description
0	Enables the operation of SSIO0 (initial value).
1	Disables the operation of SSIO0.

· **DSIO1** (bit 1)
DSIO1 controls the operation of the synchronous serial port 1.

DSIO1	Description
0	Enables the operation of SSIO1(initial value).
1	Disables the operation of SSIO1.

· **DUA0** (bit 2)
DUA0 controls the operation of the UART0.

DUA0	Description
0	Enables the operation of UART0(initial value).
1	Disables the operation of UART0.

· **DI2C1** (bit 6)
DI2C1 controls the operation of the I^2C bus interface(slave).

DI2C1	Description
0	Enables the operation of I^2C bus interface (slave). (initial value).
1	Disables the operation of I^2C bus interface (slave).

· **DI2C0** (bit 7)
DI2C0 controls the operation of the I^2C bus interface(master).

DI2C0	Description
0	Enables the operation of I^2C bus interface (master). (initial value).
1	Disables the operation of I^2C bus interface (master).

Notes:
· If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
· Refer to Chapter 14, "Synchronous Serial Port" for details of the SSIO operation.
· Refer to Chapter 15, "UART" for details of the UART operation.
· Refer to Chapter 16, "I^2C Bus Interface (Master)" and Chapter 17, "I^2C Bus Interface (Slave)" for details of the I^2C operation.

5.2.6 Block Control Register 3 (BLKCON3)

Address: 0F02BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON3	¾	¾	¾	DVC0	¾	¾	¾	¾
R/W	-	-	-	R/W	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

BLKCON3 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

· **DVC0** (bit 0)
DVC0 controls audio playback operation.

DVC0	Description
0	Enables audio playback and speaker amplifier (initial value).
1	Disables audio playback and speaker amplifier

Notes:
· If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
· Refer to Chapter 19, "Audio Playback Function" and Chapter 20, "Speaker Amplifier" for details of the audio playback operation and speaker amplifier.

5.2.7 Block Control Register 4 (BLKCON4)

Address: 0F02CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	¾	¾	¾	¾	¾	¾	¾	DSAD
R/W	-	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) that controls the operation of the relevant block.

[Description of Bits]

· **DSAD** (bit 0)
DSAD controls the operation of the successive-approximation type A/D converter.

DSAD	Description
0	Enable the operation of the successive-approximation type A/D converter (initial value).
1	Disable the operation of the successive-approximation type A/D converter.

Notes:
· If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".
· Refer to Chapter 18, "Successive Approximation Type A/D Converter" for details of the successive approximation type A/D converter operation.

5.3 Description of Operation

5.3.1 Program Run Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, RESET_N pin reset, or WDT overflow reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt or NMI interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H.
For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 4, "Reset Function".

5.3.2 HALT Mode

The HALT mode is the state where the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the HALT mode is set.
When a non-maskable interrupt request or an interrupt request enabled by an interrupt enable register (IE1 to IE7) is issued, the HLT bit is set to "0" on the second falling edge of the system clock (SYSCLK) and the HALT mode is released and it returns to the program run mode.
Figure 5-2 shows the operation waveforms in HALT mode.

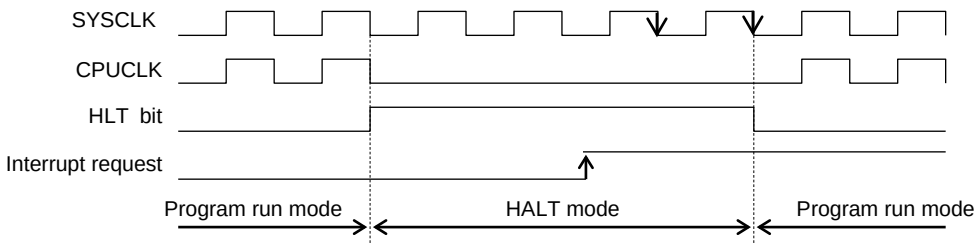


Figure 5-2 Operation Waveforms in HALT Mode

Note:
Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1". When the Master Interrupt Enable Flag(MIE) of Program Status Word(PSW) of nx-U16/100 core is "1", after the execution of two NOP instructions, an interrupt transition cycle is executed and instruction execution of the interrupt routine is started. When MIE is "0", afer executing two NOP instructions, it doesn't transition to interrupt and continues instruction execution after NOP instruction.

5.3.3 STOP Mode

The STOP mode is the state where oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by writing "5nH"(n: an arbitrary value of 0 to 0FH) and "0AnH"(n: an arbitrary value) to the stop code acceptor (STPACP) sequentially and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the stop code acceptor is disabled.
When an interrupt request shown below is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode. The interrupt requests which can release the STOP mode are shown below.

· Port P80 to P87pins interrupts

When an interrupt request is issued, the STOP mode is released after the elapse of the high-speed oscillation start time (T_{XTH} : less than 1 LSCLK period) and the high-speed clock (OSCLK) oscillation stabilization time (16384-pulse count), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.
For the high-speed oscillation start time (T_{XTH}), see the "Electrical Characteristics" Section in Appendix C.
Figure 5-3 shows the operation waveforms in STOP mode when CPU Operates with High-Speed Clock.

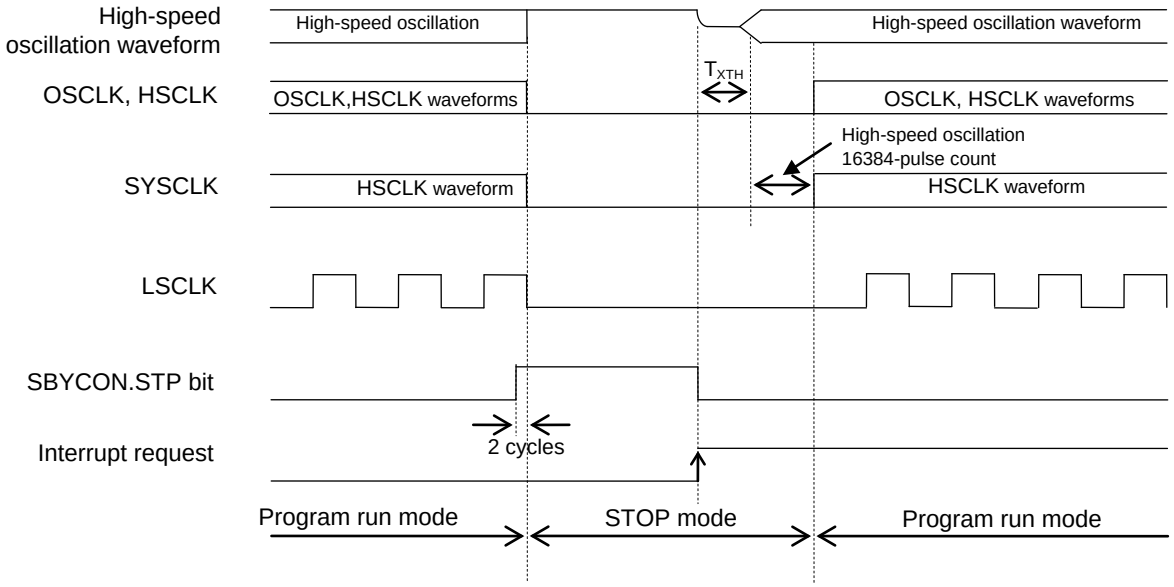


Figure 5-3 Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

Note:
Since up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the STP bit to "1". When the Master Interrupt Enable Flag(MIE) of Program Status Word(PSW) of nx-U16/100 core is "1", after the execution of two NOP instructions, an interrupt transition cycle is executed and instruction execution of the interrupt routine is started. When MIE is "0", afer executing two NOP instructions, it doesn't transition to interrupt and continues instruction execution after NOP instruction.

5.3.3.1 Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP mode and HALT mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE1 to IE7), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U8/100 Core Instruction Manual" and Chapter 9, "Interrupt", respectively.

Table 5-1 and Table 5-2 show the return operations from STOP/HALT mode.

Table 5-1 Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
Ô	Ô	¾	0	Not returned from STOP/HALT mode.
3	Ô	¾	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0, 1, 2	Ô	¾	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 5-2 Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
Ô	Ô	Ô	0	Not returned from STOP/HALT mode.
Ô	Ô	0	1	
Ô	0	1	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
2, 3	1	1	1	
0,1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

The interrupt level (ELEVEL) of the program status word (PSW) is a bit to shows CPU interrupt status. It is set by hardware when it goes to interrupt processing or it returns from interrupt processing.

- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither nonmaskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

5.3.4 Block control function

To use this block control function, supply current can be reduced more, by stopping completely operation of the unused function.
The initial value of each bit of each block control register is "0", and operation of each block is enabled. If the appropriate bit is set to "1" (operation disabled), the relevant block will be reset (all registers are initialized), and the clock of the relevant block will stop. When this bit is set to "1", the writing to all the registers of the relevant block will be invalid, an initial value is read when a register is read. To use the function of the relevant block, reset (enable operation) the appropriate bit of the block control register to "0".

BLKCON0 register controls (enables or disables) the operation of Timer .
BLKCON2 register controls (enables or disables) the operation of UART and SSIO and I^2C.
BLKCON3 register controls (enables or disables) audio playback.
BLKCON4 register controls (enables or disables) the operation of the successive-approximation type A/D converter.

Notes:
· If the appropriate bit of the block register is set to "1", all relevant registers are initialized.
· Refer to the relevant chapter for details of operation or notes of each block.

Chapter 6

Port 2

6. Port 2

6.1 Overview

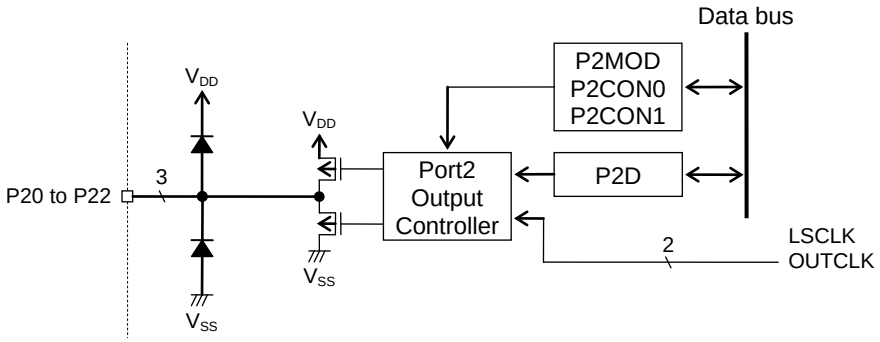
This LSI includes a 3-bit output-only port, Port 2 (P20 to P22).
Port 2 can output the low-speed clock (LSCLK) as the secondary function. See Chapter 3, "Clock Generation Circuit" for the clock output.

6.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit.
- Allows direct LED drive when the N-channel open drain output is selected.
- The low-speed clock (LSCLK) and high-speed clock (OUTCLK) can be output as the secondary function.

6.1.2 Configuration

Figure 6-1 shows the configuration of Port 2.



P2D : Port 2 data register
P2CON0 : Port 2 control register 0
P2CON1 : Port 2 control register 1
P2MOD : Port 2 mode register

Figure 6-1 Configuration of Port 2

6.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P20/LED0/LSCLK	O	Output port / LED direct drive*	Low-speed clock output (LSCLK)
P21/LED1/OUTCLK	O	Output port / LED direct drive*	High-speed clock output (OUTCLK)
P22/LED2	O	Output port / LED direct drive*	—

*When N-channel open drain output is selected.

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F210H	Port 2 data register	P2D	¾	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	¾	R/W	8	00H

6.2.2 Port 2 Data Register (P2D)

Address: 0F210H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2D	¾	¾	¾	¾	¾	P22D	P21D	P20D
R/W	¾	¾	¾	¾	¾	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2D is a special function register (SFR) to set the output value of Port 2. The value of this register is output to Port 2. The value written to P2D is readable.

[Description of Bits]

· **P22D to P20D** (bits 2 to 0)
The P22D to P20D bits is used to set the output value of the Port 2 pin.

P20D	Description
0	Output level of the P20 pin: "L"
1	Output level of the P20 pin: "H"

P21D	Description
0	Output level of the P21 pin: "L"
1	Output level of the P21 pin: "H"

P22D	Description
0	Output level of the P22 pin: "L"
1	Output level of the P22 pin: "H"

6.2.3 Port 2 control registers 0, 1 (P2CON0, P2CON1)

Address: 0F212H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON0	¾	¾	¾	¾	¾	P22C0	P21C0	P20C0
R/W	¾	¾	¾	¾	¾	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F213H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON1	¾	¾	¾	¾	¾	P22C1	P21C1	P20C1
R/W	¾	¾	¾	¾	¾	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2CON0 and P2CON1 are special function registers (SFRs) to select the output state of the output pin Port 2.

[Description of Bits]

· **P22C0 to P20C0, P22C1 to P20C1** (bits 2 to 0)
The P22C0 to P20C0 and P22C1 to P20C1 bits are used to select high-impedance output(*), P-channel open drain output, N-channel open drain output, or CMOS output.
To directly drive LEDs, select N-channel open drain output.

(*) High-impedance output means the status that both of "H" level output and "L" level output turn off.

P20C1	P20C0	Description
0	0	P20 pin: In high-impedance output mode (initial value)
0	1	P20 pin: In P-channel open drain output mode
1	0	P20 pin: In N-channel open drain output mode
1	1	P20 pin: In CMOS output mode

P21C1	P21C0	Description
0	0	P21 pin: In high-impedance output mode (initial value)
0	1	P21 pin: In P-channel open drain output mode
1	0	P21 pin: In N-channel open drain output mode
1	1	P21 pin: In CMOS output mode

P22C1	P22C0	Description
0	0	P22 pin: In high-impedance output mode (initial value)
0	1	P22 pin: In P-channel open drain output mode
1	0	P22 pin: In N-channel open drain output mode
1	1	P22 pin: In CMOS output mode

6.2.4 Port 2 Mode Register (P2MOD)

Address: 0F214H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD	¾	¾	¾	¾	¾	P22MD	P21MD	P20MD
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial value	¾	¾	¾	¾	¾	0	0	0

P2MOD is a special function register (SFR) to select the primary function or the secondary function of Port 2

[Description of Bits]

· **P20MD** (bit 0)
The P20MD bit is used to select the primary function or the secondary function of the P20 pin.

P20MD	Description
0	General-purpose output port function/ LED direct drive (initial value)
1	Low-speed output clock (LSCLK) output function

· **P21MD** (bit 1)
The P21MD bit is used to select the primary function or the secondary function of the P21 pin.

P21MD	Description
0	General-purpose output port function/ LED direct drive (initial value)
1	High-speed output clock (OUTCLK) output function

· **P22MD** (bit 2)
The P22MD bit is used to select the primary function or the secondary function of the P22 pin.

P22MD	Description
0	General-purpose output port function/ LED direct drive (initial value)
1	Prohibited

Note:
P2 (Port 2) is an output-only port and it does not have the register to select the input/output direction.

6.3 Description of Operation

6.3.1 Output Port Function

For each pin of Port 2, any one of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, and CMOS output mode can be selected by setting the Port 2 control registers 0, 1 (P2CON0, P2CON1). At a system reset, high-impedance output mode is selected as the initial status. To drive LEDs directly, select N-channel open drain output.
Depending of the value set in the Port 2 data register (P2D), a "L" level or "H" level signal is output to each pin of Port 2.

6.3.2 Secondary Function

The low-speed clock (LSCLK) and high-speed clock (OUTCLK) output are assigned to Port 2 as the secondary functions. The secondary function can be used by setting the P21MD to P20MD bits of the Port 2 mode register (P2MOD) to "1".

6.4 Register setup of the port

For use the clock output function, each related port register needs to be set up.

6.4.1 When use the High-speed clock (OUTCLK) output function using P21 pin.

The High-speed clock output is selected as the secondary function of the P21 pin by setting P21MD (P2MOD register: bit1) to "1" .

register	P2MOD register (Address:0F214H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	-	P22MD	**P21MD**	P20MD
value	-	-	-	-	-	0	**1**	*

The state of the P21 pin is selected as CMOS output mode by setting P21C1 bit (P2CON1 register:bit1) to "1", setting P21C0 bit (P2CON0 register:bit1) to "1".

register	P2CON1 register (Address: 0F213H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	-	P22C1	**P21C1**	P20C1
value	-	-	-	-	-	*	**1**	*

register	P2CON0 register (Address: 0F212H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	-	P22C0	**P21C0**	P20C0
value	-	-	-	-	-	*	**1**	*

As for P21D bit (P2D register:bit1), neither "0" nor "1" is problematic.

register	P2D register (Address: 0F210H)							
bit	7	6	5	4	3	2	**1**	0
bit name	-	-	-	-	-	P22D	**P21D**	P20D
value	-	-	-	-	-	*	******	*

- : not existing
* : no relation to the High-speed clock output function
** : Don't care

6.4.2 When use the Low-speed clock (LSCLK) output function using P20 pin.

The Low-speed clock output is selected as the secondary function of the P20 pin by setting P20MD (P2MOD register: bit0) to "1" .

register	P2MOD register (Address:0F214H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	-	P22MD	P21MD	**P20MD**
value	-	-	-	-	-	0	*	**1**

The state of the P20 pin is selected as CMOS output mode by setting P20C1 bit (P2CON1 register:bit0) to "1", setting P20C0 bit (P2CON0 register:bit0) to "1".

register	P2CON1 register (Address: 0F213H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	-	P22C1	P21C1	**P20C1**
value	-	-	-	-	-	*	*	**1**

register	P2CON0 register (Address: 0F212H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	-	P22C0	P21C0	**P20C0**
value	-	-	-	-	-	*	*	**1**

As for P20D bit (P2D register:bit0), neither "0" nor "1" is problematic.

register	P2D register (Address: 0F210H)							
bit	7	6	5	4	3	2	1	**0**
bit name	-	-	-	-	-	P22D	P21D	**P20D**
value	-	-	-	-	-	*	*	******

- : not existing
* : no relation to the Low-speed clock output function
** : Don't care

Chapter 7

Port 4

7. Port 4

7.1 Overview

This LSI includes a 3-bit or a 4-bit(*) input/output port, Port 4 (P40 to P42, P43(*)).
Port 4 can have the synchronous serial port functions as secondary or tertiary functions. For the synchronous serial port, see Chapter 14, "Synchronous Serial Port".

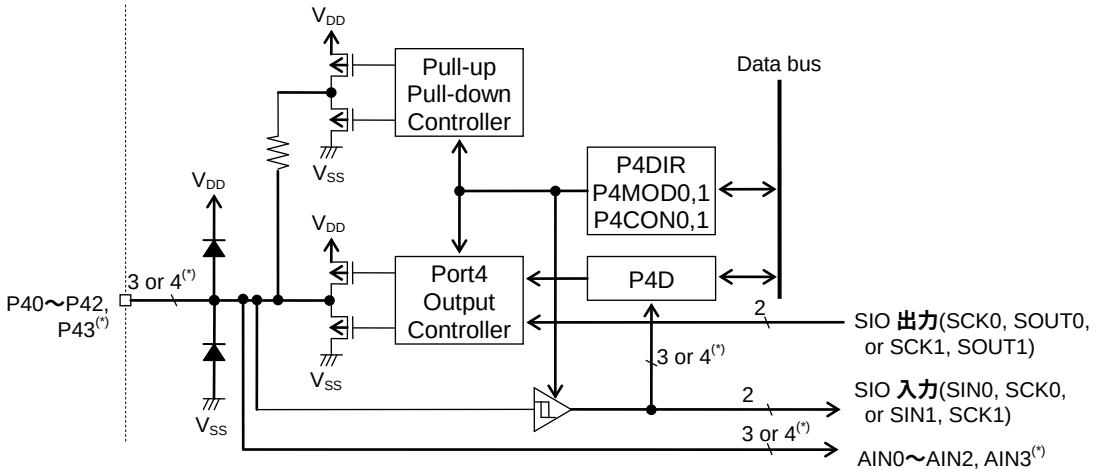
7.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The synchronous serial port pins (SIN0, SCK0, SOUT0) can be used as tertiary functions.
- The synchronous serial port pins (SIN1, SCK1, SOUT1) can be used as secondary functions.
- The P40 to P42 pins and P43(*) pin can be used as an analog input pin of the successive approximation type A/D converter.

(*) : P43 pin is built into ML610Q306.

7.1.2 Configuration

Figure 7-1 shows the configuration of Port 4.



P4D	: Port 4 data register
P4DIR	: Port 4 direction register
P4CON0	: Port 4 control register 0
P4CON1	: Port 4 control register 1
P4MOD0	: Port 4 mode register 0
P4MOD1	: Port 4 mode register 1

Figure 7-1 Configuration of Port 4

(*) : P43 pin, AIN3 input, and data width 4 bits are ML610Q306 only.

7.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P40/SIN0/AIN0	I/O	Input/output port /Successive-approximation type ADC input	SSIO1 data input	SSIO0 data input
P41/SCK0/AIN1	I/O	Input/output port /Successive-approximation type ADC input	SSIO1 synchronous clock input/output	SSIO0 synchronous clock input/output
P42/SOUT0/AIN2	I/O	Input/output port /Successive-approximation type ADC input	SSIO1 data output	SSIO0 data output
P43/AIN3 (*)	I/O	Input/output port /Successive-approximation type ADC input	¾	¾

Note:
P40 to P42 and P43(*) are assigned to the input of successive-approximation type ADC. When you use it as an analog input of successive-approximation type ADC, please set an applicable port as a high impedance output state.

(*) : P43/AIN3 pin is built into ML610Q306.

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F220H	Port 4 data register	P4D	¾	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	¾	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H

7.2.2 Port 4 Data Register (P4D)

Address: 0F220H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4D	¾	¾	¾	¾	P43D (*)	P42D	P41D	P40D
R/W	¾	¾	¾	¾	R/W (*)	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable. In input mode, the input level of the Port 4 pin is read when P4D is read. P4D can be written during input mode, and its value does not affect the port level.
Output mode or input mode is selected by using the port direction register (P4DIR) described later.

[Description of Bits]

· **P43D(*)**, **P42D to P40D** (bit 3(*), bits 2 to 0)
The P43D(*) and the P42D to P40D bits are used to set the output value of the Port 4 pin in output mode and to read the pin level of the Port 4 pin in input mode.

P40D	Description
0	Output or input level of the P40 pin: "L"
1	Output or input level of the P40 pin: "H"

P41D	Description
0	Output or input level of the P41 pin: "L"
1	Output or input level of the P41 pin: "H"

P42D	Description
0	Output or input level of the P42 pin: "L"
1	Output or input level of the P42 pin: "H"

P43D (*)	Description
0	Output or input level of the P43 pin: "L"
1	Output or input level of the P43 pin: "H"

Note:
When setting a value to the bit of the P4D by using bit operation instruction, input levels of the pin are written to the P4D if non-target bits are set as the input mode. Therefore, switch the mode to the output mode by the port 4 direction register (P4DIR) after setting the output value to the P4D when switching from the input mode to the output mode.
(*): The P43D is built into ML610Q306.

7.2.3 Port 4 Direction Register (P4DIR)

Address: 0F221H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4DIR	¾	¾	¾	¾	P43DIR(*)	P42DIR	P41DIR	P40DIR
R/W	¾	¾	¾	¾	R/W(*)	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

[Description of Bits]

· **P43DIR(*), P42DIR to P40DIR** (bit 3(*), bits 2 to 0)
The P43DIR(*) and the P42DIR to P40DIR pins are used to set the input/output direction of the Port 4 pin.

P40DIR	Description
0	P40 pin: Output (initial value)
1	P40 pin: Input

P41DIR	Description
0	P41 pin: Output (initial value)
1	P41 pin: Input

P42DIR	Description
0	P42 pin: Output (initial value)
1	P42 pin: Input

P43DIR(*)	Description
0	P43 pin: Output (initial value)
1	P43 pin: Input

(*): The P43DIR is built into ML610Q306.

7.2.4 Port 4 Control Registers 0, 1 (P4CON0, P4CON1)

Address: 0F222H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON0	¾	¾	¾	¾	P43C0(*2)	P42C0	P41C0	P40C0
R/W	¾	¾	¾	¾	R/W(*2)	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F223H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON1	¾	¾	¾	¾	P43C1(*2)	P42C1	P41C1	P40C1
R/W	¾	¾	¾	¾	R/W(*2)	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4CON0 and P4CON1 are special function registers (SFRs) to specify the input and output conditions of each pin of Port 4. The conditions differ between input mode and output mode. Input or output is selected by the P4DIR register.

[Description of Bits]

· **P43C1(*2), P42C1 to P40C1, P43C0(*2), P42C0 to P40C0** (bit 3(*2), bits 2 to 0)
The P43C1(*2), the P42C1 to P40C1 and the P43C0(*2), P42C0 to P40C0 bits are used to select high-impedance output(*1), P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

(*1) High-impedance output means the status that both of "H" level output and "L" level output turn off.

Setting of P40 pin		When output mode is selected (P40DIR bit = "0")	When input mode is selected (P40DIR bit = "1")
P40C1	**P40C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P41 pin		When output mode is selected (P41DIR bit = "0")	When input mode is selected (P41DIR bit = "1")
P41C1	**P41C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P42 pin		When output mode is selected (P42DIR bit = "0")	When input mode is selected (P42DIR bit = "1")
P42C1	**P42C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P43 pin		When output mode is selected (P43DIR bit = "0")	When input mode is selected (P43DIR bit = "1")
P43C1(*2)	**P43C0**(*2)	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

(*2) : The P43C1 and P43C0 are built into ML610Q306.

7.2.5 Port 4 Mode Registers 0, 1 (P4MOD0, P4MOD1)

Address: 0F224H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD0	¾	¾	¾	¾	¾	P42MD0	P41MD0	P40MD0
R/W	¾	¾	¾	¾	¾	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F225H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD1	¾	¾	¾	¾	¾	P42MD1	P41MD1	P40MD1
R/W	¾	¾	¾	¾	¾	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4MOD0 and P4MOD1 are special function registers (SFRs) used to select the primary, secondary, or tertiary function of Port 4.

[Description of Bits]

· **P40MD1, P40MD0** (bit 0)
The P40MD1 and P40MD0 bits are used to select the primary, secondary or tertiary function of the P40 pin.

P40MD1	P40MD0	Description
0	0	General-purpose input/output (initial value)
0	1	SSIO1 data input (SIN1)
1	0	SSIO0 data input (SIN0)
1	1	Prohibited

· **P41MD1, P41MD0** (bit 1)
The P41MD1 and P41MD0 bits are used to select the primary, secondary or tertiary functions of the P41 pin.

P41MD1	P41MD0	Description
0	0	General-purpose input/output (initial value)
0	1	SSIO1 clock input/output (SCK1)
1	0	SSIO0 clock input/output (SCK0)
1	1	Prohibited

· **P42MD1, P42MD0** (bit 2)
The P42MD1 and P42MD0 bits are used to select the primary, secondary or tertiary functions of the P42 pin.

P42MD1	P42MD0	Description
0	0	General-purpose input/output (initial value)
0	1	SSIO1 data output (SOUT1)
1	0	SSIO0 data output (SOUT0)
1	1	Prohibited

Note:
When the pin is set to "Prohibited" and the output mode is selected (by the Port 4 direction register), the Port 4 output pin state is fixed as follows regardless of the data of the port data register P4D.

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

7.3 Description of Operation

7.3.1 Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

7.3.2 Secondary and Tertiary Functions

Port 4 is assigned synchronous serial port 1 pins (SIN1, SCK1, SOUT1) and synchronous serial port 0 pins (SIN0, SCK0, SOUT0) as its secondary and tertiary functions. These pins can be used in secondary or tertiary functions mode by setting the P42MD0 to P40MD0 bits and the P42MD1 to P40MD1 bits of the Port 4 mode registers (P4MOD0, P4MOD1).

Note:
The P40 to P42 pins and P43 pin (built into ML610Q306) are assigned to the successive approximation type A/D converter input. To use them as the analog input of successive approximation type A/D converter input, set the appropriate port to the high-impedance output mode.

Chapter 8

Port 8

8. Port 8

8.1 Overview

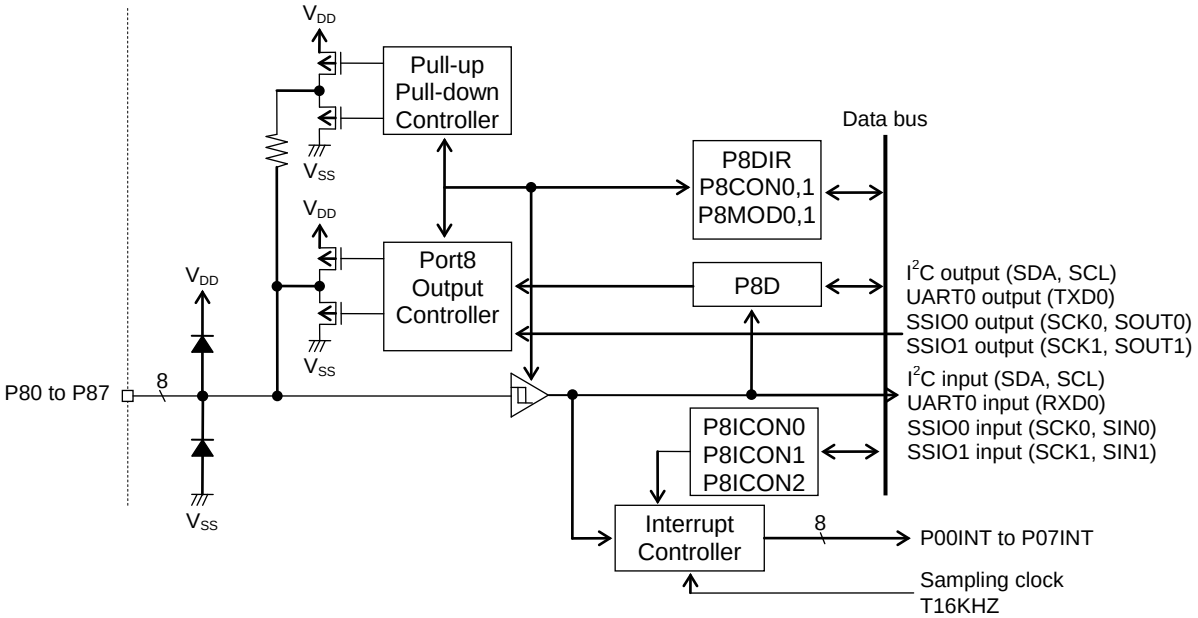
This LSI includes an 8-bit input/output port, Port 8 (P80 to P87).
Port 8 can use the I^2C communication pins (SDA, SCL), UART pins (TXD1, RXD1) and synchronous serial port pins (SIN0, SCK0, SOUT0 andSIN1, SCK1, SOUT1) as the secondary or tertiary function.
See Chapter 14, "Synchronous Serial Port" for the synchronous serial port, Chapter 15, "UART" for UART, Chapter 16, "I^2C Bus Interface (Master)" and Chapter 17, "I^2C Bus Interface (Slave)" for the I^2C bus.

8.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ)
- Allows selection of high-impedance output, a P-channel open drain output, a N-channel open drain output, and a CMOS output for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit.
- I^2C bus interface pins (SDA, SCL), UART pins (TXD0, RXD0) and Synchronous serial port pins (SIN0, SCK0, SOUT0 and SIN1, SCK1, SOUT1) can be used as the secondary or tertiary functions.

8.1.2 Configuration

Figure 8-1 shows the configuration of Port 8.



P8D	: Port 8 data register
P8DIR	: Port 8 direction register
P8CON0	: Port 8 control register 0
P8CON1	: Port 8 control register 1
P8ICON0	: Port 8 interrupt control register 0
P8ICON1	: Port 8 interrupt control register 1
P8ICON2	: Port 8 interrupt control register 2
P8MOD0	: Port 8 mode register 0
P8MOD1	: Port 8 mode register 1

Figure 8-1 Configuration of Port 8

8.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P80/EXI0	I/O	Input/output port, External 0 interrupt	I^2C synchronous data input/output (SDA)	SSIO0 data input (SIN0)
P81/EXI1	I/O	Input/output port, External 1 interrupt	I^2C synchronous clock input/output (SCL)	SSIO0 clock input/output (SCK0)
P82/EXI2	I/O	Input/output port, External 2 interrupt	¾	SSIO0 data output (SOUT0)
P83/EXI3	I/O	Input/output port, External 3 interrupt	¾	¾
P84/EXI4	I/O	Input/output port, External 4 interrupt	¾	SSIO1 data input (SIN1)
P85/EXI5	I/O	Input/output port, External 5 interrupt	¾	SSIO1 clock input/output (SCK1)
P86/EXI6	I/O	Input/output port, External 6 interrupt	UART0 data input(RXD0)	SSIO1 data output (SOUT1)
P87/EXI7	I/O	Input/output port, External 7 interrupt	UART0 data output(TXD0)	¾

8.2 Description of Registers

8.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F240H	Port 8 data register	P8D	¾	R/W	8	00H
0F241H	Port 8 direction register	P8DIR	¾	R/W	8	00H
0F242H	Port 8 control register 0	P8CON0	P8CON	R/W	8/16	00H
0F243H	Port 8 control register 1	P8CON1		R/W	8	00H
0F244H	Port 8 mode register 0	P8MOD0	P8MOD	R/W	8/16	00H
0F245H	Port 8 mode register 1	P8MOD1		R/W	8	00H
0F024H	Port 8 External interrupt control register 0	P8ICON0	¾	R/W	8	00H
0F025H	Port 8 External interrupt control register 1	P8ICON1	¾	R/W	8	00H
0F026H	Port 8 External interrupt control register 2	P8ICON2	¾	R/W	8	00H

8.2.2 Port 8 Data Register (P8D)

Address: 0F240H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8D	P87D	P86D	P85D	P84D	P83D	P82D	P81D	P80D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8D is a special function register (SFR) to set the value to be output to the Port 8 pin or to read the input level of the Port 8. In output mode, the value of this register is output to the Port 8 pin. The value written to P8D is readable. In input mode, the input level of the Port 8 pin is read when P8D is read. Output mode or input mode is selected by using the port mode register (P8DIR) described later.

[Description of Bits]

· **P87D to P80D** (bits 7 to 0)
The P87D to P80D bits are used to set the output value of the Port 8 pin in output mode and to read the pin level of the Port 8 pin in input mode.

P80D	Description
0	Output or input level of the P80 pin: "L"
1	Output or input level of the P80 pin: "H"

P81D	Description
0	Output or input level of the P81 pin: "L"
1	Output or input level of the P81 pin: "H"

P82D	Description
0	Output or input level of the P82 pin: "L"
1	Output or input level of the P82 pin: "H"

P83D	Description
0	Output or input level of the P83 pin: "L"
1	Output or input level of the P83 pin: "H"

P84D	Description
0	Output or input level of the P84 pin: "L"
1	Output or input level of the P84 pin: "H"

P85D	Description
0	Output or input level of the P85 pin: "L"
1	Output or input level of the P85 pin: "H"

P86D	Description
0	Output or input level of the P86 pin: "L"
1	Output or input level of the P86 pin: "H"

P87D	Description
0	Output or input level of the P87 pin: "L"
1	Output or input level of the P87 pin: "H"

Note:
When setting a value to the bit of the P8D by using bit operation instruction, input levels of the pin are written to the P8D if non-target bits are set as the input mode. Therefore, switch the mode to the output mode by the port 8 direction register (P8DIR) after setting the output value to the P8D when switching from the input mode to the output mode.

8.2.3 Port 8 Direction Register (P8DIR)

Address: 0F241H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8DIR	P87DIR	P86DIR	P85DIR	P84DIR	P83DIR	P82DIR	P81DIR	P80DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8DIR is a special function register (SFR) to select the input/output mode of Port 8.

[Description of Bits]

· **P87DIR to P80DIR** (bits 7 to 0)
The P87DIR to P80DIR pins are used to set the input/output direction of the Port 8 pin.

P80DIR	Description
0	P80 pin: Output (initial value)
1	P80 pin: Input

P81DIR	Description
0	P81 pin: Output (initial value)
1	P81 pin: Input

P82DIR	Description
0	P82 pin: Output (initial value)
1	P82 pin: Input

P83DIR	Description
0	P83 pin: Output (initial value)
1	P83 pin: Input

P84DIR	Description
0	P84 pin: Output (initial value)
1	P84 pin: Input

P85DIR	Description
0	P85 pin: Output (initial value)
1	P85 pin: Input

P86DIR	Description
0	P86 pin: Output (initial value)
1	P86 pin: Input

P87DIR	Description
0	P87 pin: Output (initial value)
1	P87 pin: Input

8.2.4 Port 8 Control Registers 0, 1 (P8CON0, P8CON1)

Address: 0F242H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8CON0	P87C0	P86C0	P85C0	P84C0	P83C0	P82C0	P81C0	P80C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F243H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8CON1	P87C1	P86C1	P85C1	P84C1	P83C1	P82C1	P81C1	P80C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8CON0 and P8CON1 are special function registers (SFRs) to specify the input and output conditions of each pin of Port 8. The conditions differ between input mode and output mode. Input or output is selected by the P8DIR register.

[Description of Bits]

· **P87C1 to P80C1, P87C0 to P80C0** (bits 7 to 0)
The P87C1 to P80C1 pins and the P87C0 to P80C0 pins are used to select high-impedance output (*), P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

(*) High impedance output means that both high-level output and low-level output are off.

Setting of P80 pin		When output mode is selected (P80DIR bit = "0")	When input mode is selected (P80DIR bit = "1")
P80C1	**P80C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P81 pin		When output mode is selected (P81DIR bit = "0")	When input mode is selected (P81DIR bit = "1")
P81C1	**P81C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P82 pin		When output mode is selected (P82DIR bit = "0")	When input mode is selected (P82DIR bit = "1")
P82C1	**P82C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P83 pin		When output mode is selected (P83DIR bit = "0")	When input mode is selected (P83DIR bit = "1")
P83C1	**P83C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P84 pin		When output mode is selected (P84DIR bit = "0")	When input mode is selected (P84DIR bit = "1")
P84C1	**P84C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P85 pin		When output mode is selected (P85DIR bit = "0")	When input mode is selected (P85DIR bit = "1")
P85C1	**P85C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P86 pin		When output mode is selected (P86DIR bit = "0")	When input mode is selected (P86DIR bit = "1")
P86C1	**P86C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P87 pin		When output mode is selected (P87DIR bit = "0")	When input mode is selected (P87DIR bit = "1")
P87C1	**P87C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

8.2.5 Port 8 Mode Registers 0, 1 (P8MOD0, P8MOD1)

Address: 0F244H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8MOD0	P87MD0	P86MD0	P85MD0	P84MD0	P83MD0	P82MD0	P81MD0	P80MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F245H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8MOD1	P87MD1	P86MD1	P85MD1	P84MD1	P83MD1	P82MD1	P81MD1	P80MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8MOD0 and P8MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 8.

[Description of Bits]

· **P80MD1, P80MD0** (bit 0)
The P80MD1 and P80MD0 bits are used to select the primary, secondary, or tertiary function of the P80 pin.

P80MD1	P80MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I2C bus data input/output pin (SDA)
1	0	SSIO0 data input pin (SIN0)
1	1	Prohibited

· **P81MD1, P81MD0** (bit 1)
The P81MD1 and P81MD0 bits are used to select the primary, secondary, or tertiary function of the P81 pin.

P81MD1	P81MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	I2C bus clock input/output pin (SCL)
1	0	SSIO0 clock input/output pin (SCK0)
1	1	Prohibited

· **P82MD1, P82MD0** (bit 2)
The P82MD1 and P82MD0 bits are used to select the primary, or tertiary function of the P82 pin.

P82MD1	P82MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	SSIO0 data output pin (SOUT0)
1	1	Prohibited

· **P83MD1, P83MD0** (bit 3)
The P83MD1 and P83MD0 bits are used to select the primary, secondary, or tertiary function of the P83 pin.

P83MD1	P83MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	Prohibited
1	1	Prohibited

· **P84MD1, P84MD0** (bit 4)
The P84MD1 and P84MD0 bits are used to select the primary, or tertiary function of the P84 pin.

P84MD1	P84MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	SSIO1 data input pin (SIN1)
1	1	Prohibited

· **P85MD1, P85MD0** (bit 5)
The P85MD1 and P85MD0 bits are used to select the primary, or tertiary function of the P85 pin.

P85MD1	P85MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Prohibited
1	0	SSIO1 clock input/output pin (SCK1)
1	1	Prohibited

· **P86MD1, P86MD0** (bit 6)
The P86MD1 and P86MD0 bits are used to select the primary, secondary, or tertiary function of the P86 pin.

P86MD1	P86MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data input (RXD0)
1	0	SSIO1 data output pin (SOUT1)
1	1	Prohibited

· **P87MD1, P87MD0** (bit 7)
The P87MD1 and P87MD0 bits are used to select the primary, or secondary function of the P87 pin.

P87MD1	P87MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data output (TXD0)
1	0	Prohibited
1	1	Prohibited

Note:
When the pin is set to "Prohibited" and the output mode is selected (by the Port 8 control register), the Port 8 output pin state is fixed as follows regardless of the data of the port data register P8D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

8.2.6 Port8 Interrupt Control Registers 0, 1 (P8ICON0, P8ICON1)

Address: 0F024H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8ICON0	P87E0	P86E0	P85E0	P84E0	P83E0	P82E0	P81E0	P80E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F025H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8ICON1	P87E1	P86E1	P85E1	P84E1	P83E1	P82E1	P81E1	P80E1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8ICON0 and P8ICON1 are special function registers (SFRs) to select an interrupt edge of Port 8.

[Description of Bits]

· **P87E0 to P80E0, P87E1 to P80E1** (bits 7 to 0)
The P87E0 to P80E0 bits and the P87E1 to P80E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The P8nE0 bit and the P8nE1 bit determine the interrupt mode of P8n (Example: When P82E0 = "0" and P82E1 = "1", P82 is in rising-edge interrupt mode).

P87E1 to P80E1	P87E0 to P80E0	Description
0	0	Interrupt disabled mode (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

8.2.7 Port8 Interrupt Control Register 2 (P8ICON2)

Address: 0F026H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P8ICON2	P87SM	P86SM	P85SM	P84SM	P83SM	P82SM	P81SM	P80SM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P8ICON2 is a special function register (SFR) to select detection of signal edge for interrupts with or without sampling.

[Description of Bits]

· **P87SM to P80SM** (bits 7 to 0)
The P87SM to P80SM bits are used to select detection of signal edge for Port 8 interrupts with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

P80SM	Description
0	Detects the input signal edge for a P80 interrupt without sampling (initial value).
1	Detects the input signal edge for a P80 interrupt with sampling.

P81SM	Description
0	Detects the input signal edge for a P81 interrupt without sampling (initial value).
1	Detects the input signal edge for a P81 interrupt with sampling.

P82SM	Description
0	Detects the input signal edge for a P82 interrupt without sampling (initial value).
1	Detects the input signal edge for a P82 interrupt with sampling.

P83SM	Description
0	Detects the input signal edge for a P83 interrupt without sampling (initial value).
1	Detects the input signal edge for a P83 interrupt with sampling.

P84SM	Description
0	Detects the input signal edge for a P84 interrupt without sampling (initial value).
1	Detects the input signal edge for a P84 interrupt with sampling.

P85SM	Description
0	Detects the input signal edge for a P85 interrupt without sampling (initial value).
1	Detects the input signal edge for a P85 interrupt with sampling.

P86SM	Description
0	Detects the input signal edge for a P86 interrupt without sampling (initial value).
1	Detects the input signal edge for a P86 interrupt with sampling.

P87SM	Description
0	Detects the input signal edge for a P87 interrupt without sampling (initial value).
1	Detects the input signal edge for a P87 interrupt with sampling.

Note:
In STOP mode, since the 16 kHz sampling clock stops, no sampling is performed regardless of the values set in P87SM to P80SM.

8.3 Description of Operation

8.3.1 Input/Output Port Functions

For each pin of Port 8, either output or input is selected by setting the Port 8 direction register (P8DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 8 control registers 0, 1 (P8CON0, P8CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 8 control registers 0, 1 (P8CON0, P8CON1).
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 8 depending on the value set by the Port 8 data register (P8D).
In input mode, the input level of each Port 8 pin can be read from the Port 8 data register (P8D).

8.3.2 Secondary and Tertiary Functions

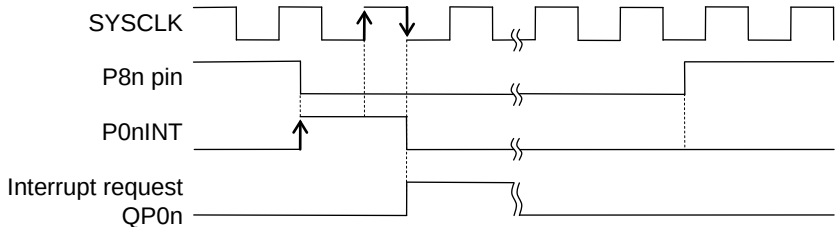
Port 8 is assigned I^2C bus pins (SDA, SCL) and synchronous serial port pins (SIN0, SCK0, SOUT0, and SIN1, SCK1, SOUT1) and UART pins (RXD0, TXD0) as its secondary and tertiary functions. These pins can be used in secondary or tertiary function mode by setting the P87MD0 to P80MD0 bits and the P87MD1 to P80MD1 bits of the Port 8 mode registers (P8MOD0, P8MOD1).

8.3.3 External Interrupt

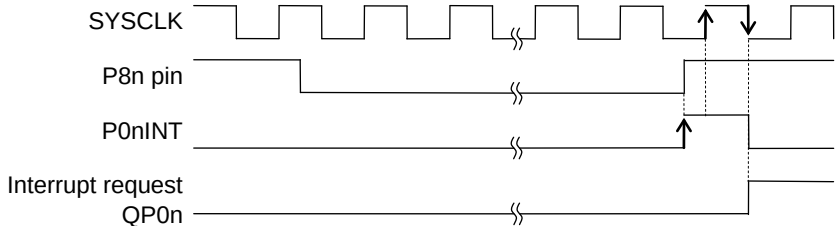
The Port 8 pins (P80 to P87) can be used for P80 to P87 interrupts (P00INT to P07INT). The P80 to P87 interrupts are maskable and interrupt enable or disable can be selected. For details of interrupts, see Chapter 9, "Interrupts".

8.3.4 Interrupt Request

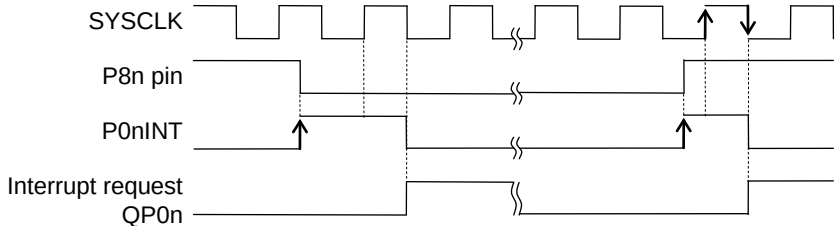
When an interrupt edge selected by the external interrupt control registers 0, 1, 2 (P8ICON0, P8ICON1, P8ICON2) occurs at a Port 8 pin, the corresponding maskable Pxx (P80 to P87) interrupt (P00INT to P07INT) occurs.
Figure 8-2 shows the P80 to P87 interrupt generation timing in rising-edge interrupt mode, falling-edge interrupt mode, and both-edges interrupt mode, each without sampling, and the P80 to P87 interrupt generation timing in rising-edge interrupt mode with sampling.



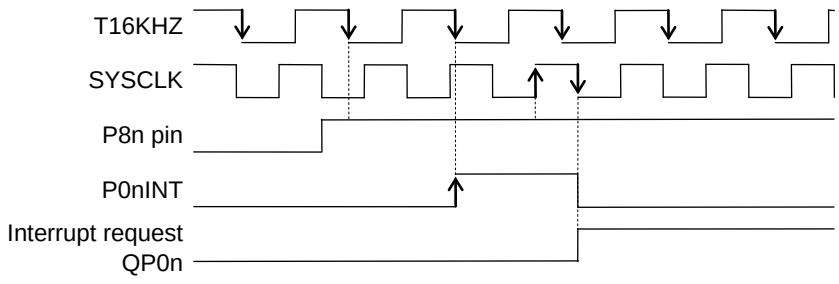
(a) When "falling-edge interrupt; without sampling" is selected



(b) When "rising-edge interrupt; without sampling" is selected



(c) When "both-edges interrupt; without sampling" is selected



n = 0 to 7

(d) When "rising-edge interrupt; with sampling" is selected

Figure 8-2 P80 to P87 Interrupt Generation Timing

Chapter 9

Interrupts (INTs)

9. Interrupts (INTs)

9.1 Overview

This LSI has 26 interrupt sources (External interrupts: 9 sources, Internal interrupts: 17 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

Chapter 8, "Port8"
Chapter 10, "NMI"
Chapter 11, "Time Base Counter"
Chapter 12, "Timer"
Chapter 13, "Watchdog Timer"
Chapter 14, "Synchronous Serial Port"
Chapter 15, "UART"
Chapter 16, "I^2C bus interface(master)"
Chapter 17, "I^2C bus interface(slave)"
Chapter 18, "Successive Approximation Type A/D Converter(SA-AD)"
Chapter 19, "Audio Playback Function"
Chapter 20, "Speaker Amplifier"

9.1.1 Features

- 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
- 24 maskable interrupt sources (Internal sources: 16, External sources: 8)
- Software interrupt (SWI): 64 sources max.
- External interrupts allow edge selection and sampling selection.

9.2 Description of Registers

9.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F011H	Interrupt enable register 1	IE1	¾	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	¾	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	¾	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	¾	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	¾	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	¾	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	¾	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	¾	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	¾	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	¾	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	¾	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	¾	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	¾	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	¾	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	¾	R/W	8	00H

9.2.2 Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	EP07	EP06	EP05	EP04	EP03	EP02	EP01	EP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

· **EP00** (bit 0)
EP00 is the enable flag for the input port P80 pin interrupt (P00INT).

EP00	Description
0	Disabled (initial value)
1	Enabled

· **EP01** (bit 1)
EP01 is the enable flag for the input port P81 pin interrupt (P01INT).

EP01	Description
0	Disabled (initial value)
1	Enabled

· **EP02** (bit 2)
EP02 is the enable flag for the input port P82 pin interrupt (P02INT).

EP02	Description
0	Disabled (initial value)
1	Enabled

· **EP03** (bit 3)
EP03 is the enable flag for the input port P83 pin interrupt (P03INT).

EP03	Description
0	Disabled (initial value)
1	Enabled

· **EP04** (bit 4)
EP04 is the enable flag for the input port P84 pin interrupt (P04INT).

EP04	Description
0	Disabled (initial value)
1	Enabled

· **EP05** (bit 5)
EP05 is the enable flag for the input port P85 pin interrupt (P05INT).

EP05	Description
0	Disabled (initial value)
1	Enabled

· **EP06** (bit 6)
EP06 is the enable flag for the input port P86 pin interrupt (P06INT).

EP06	Description
0	Disabled (initial value)
1	Enabled

· **EP07** (bit 7)
EP07 is the enable flag for the input port P87 pin interrupt (P07INT).

EP07	Description
0	Disabled (initial value)
1	Enabled

9.2.3 Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	EI2CM	EI2CS	¾	¾	¾	ESAD	ESIO1	ESIO0
R/W	R/W	R/W	—	—	—	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

[Description of Bits]

· **ESIO0** (bit 0)
ESIO0 is the enable flag for the synchronous serial port 0 interrupt (SIO0INT).

ESIO0	Description
0	Disabled (initial value)
1	Enabled

· **ESIO1** (bit 1)
ESIO1 is the enable flag for the synchronous serial port 1 interrupt (SIO1INT).

ESIO1	Description
0	Disabled (initial value)
1	Enabled

· **ESAD** (bit 2)
ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

· **EI2CS** (bit 6)
EI2CS is the enable flag for the I^2C bus(slave) interrupt (I2CSINT).

EI2CS	Description
0	Disabled (initial value)
1	Enabled

· **EI2CM** (bit 7)
EI2CM is the enable flag for the I^2C bus(master) interrupt (I2CMINT).

EI2CM	Description
0	Disabled (initial value)
1	Enabled

9.2.4 Interrupt Enable Register 3 (IE3)

Address: 0F013H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE3	¾	¾	ESD	EVC0	¾	¾	ETM1	ETM0
R/W	—	—	R/W	R/W	—	—	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE3 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE3 is not reset.

[Description of Bits]

· **ETM0** (bit 0)
ETM0 is the enable flag for the timer 0 interrupt (TM0INT).

ETM0	Description
0	Disabled (initial value)
1	Enabled

· **ETM1** (bit 1)
ETM1 is the enable flag for the timer 1 interrupt (TM1INT).

ETM1	Description
0	Disabled (initial value)
1	Enabled

· **EVC0** (bit 4)
EVC0 is the enable flag for the voice 0 interrupt (VC0INT).

EVC0	Description
0	Disabled (initial value)
1	Enabled

· **ESD** (bit 5)
ESD is the enable flag for the speaker short detection interrupt (SDINT).

ESD	Description
0	Disabled (initial value)
1	Enabled

9.2.5 Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	¾	¾	¾	¾	¾	¾	¾	EUA0
R/W	—	—	—	—	—	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

[Description of Bits]

· **EUA0** (bit 0)
EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

9.2.6 Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	¾	¾	ETM3	ETM2	¾	¾	¾	¾
R/W	—	—	R/W	R/W	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

[Description of Bits]

· **ETM2** (bit 4)
ETM2 is the enable flag for the timer 2 interrupt (TM2INT).

ETM2	Description
0	Disabled (initial value)
1	Enabled

· **ETM3** (bit 5)
ETM3 is the enable flag for the timer 3 interrupt (TM3INT).

ETM3	Description
0	Disabled (initial value)
1	Enabled

9.2.7 Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	E32H	¾	E128H	¾	¾	¾	¾	¾
R/W	R/W	—	R/W	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

[Description of Bits]

· **E128H** (bit 5)
E128H is the enable flag for the time base counter 128 Hz interrupt (T128HINT).

E128H	Description
0	Disabled (initial value)
1	Enabled

· **E32H** (bit 7)
E32H is the enable flag for the time base counter 32 Hz interrupt (T32HINT).

E32H	Description
0	Disabled (initial value)
1	Enabled

9.2.8 Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	¾	¾	¾	¾	E2H	¾	¾	E16H
R/W	—	—	—	—	R/W	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

[Description of Bits]

· **E16H** (bit 0)
E16H is the enable flag for the time base counter 16 Hz interrupt (T16HINT).

E16H	Description
0	Disabled (initial value)
1	Enabled

· **E2H** (bit 3)
E2H is the enable flag for the time base counter 2 Hz interrupt (T2HINT).

E2H	Description
0	Disabled (initial value)
1	Enabled

9.2.9 Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	¾	¾	¾	¾	¾	¾	QNMI	QWDT
R/W	—	—	—	—	—	—	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT) are non-maskable interrupts that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the master interrupt enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **QWDT** (bit 0)
QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

· **QNMI** (bit 1)
QNMI is the request flag for the NMI interrupt (NMINT).

QNMI	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with QWDT=0 or QWDT=1. When using Assembler language, describe with RB QWDT or SB QWDT.

9.2.10 Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	QP07	QP06	QP05	QP04	QP03	QP02	QP01	QP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **QP00** (bit 0)
QP00 is the request flag for the input port P80 pin interrupt (P00INT).

QP00	Description
0	No request (initial value)
1	Request

· **QP01** (bit 1)
QP01 is the request flag for the input port P81 pin interrupt (P01INT).

QP01	Description
0	No request (initial value)
1	Request

· **QP02** (bit 2)
QP02 is the request flag for the input port P82 pin interrupt (P02INT).

QP02	Description
0	No request (initial value)
1	Request

· **QP03** (bit 3)
QP03 is the request flag for the input port P83 pin interrupt (P03INT).

QP03	Description
0	No request (initial value)
1	Request

· **QP04** (bit 4)
QP04 is the request flag for the input port P84 pin interrupt (P04INT).

QP04	Description
0	No request (initial value)
1	Request

· **QP05** (bit 5)
QP05 is the request flag for the input port P85 pin interrupt (P05INT).

QP05	Description
0	No request (initial value)
1	Request

· **QP06** (bit 6)
QP06 is the request flag for the input port P86 pin interrupt (P06INT).

QP06	Description
0	No request (initial value)
1	Request

· **QP07** (bit 7)
QP07 is the request flag for the input port P87 pin interrupt (P07INT).

QP07	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with QP00=0 or QP00=1. When using Assembler language, describe with RB QP00 or SB QP00.

9.2.11 Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	QI2CM	QI2CS	¾	¾	¾	QSAD	QSIO1	QSIO0
R/W	R/W	R/W	—	—	—	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **QSIO0** (bit 0)
QSIO0 is the request flag for the synchronous serial port 0 interrupt (SIO0INT).

QSIO0	Description
0	No request (initial value)
1	Request

· **QSIO1** (bit 1)
QSIO1 is the request flag for the synchronous serial port 1 interrupt (SIO1INT).

QSIO1	Description
0	No request (initial value)
1	Request

· **QSAD** (bit 2)
QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT).

QSAD	Description
0	No request (initial value)
1	Request

· **QI2CS** (bit 6)
QI2CS is the request flag for the I^2C bus(slave) interrupt (I2CSINT).

QI2CS	Description
0	No request (initial value)
1	Request

· **QI2CM** (bit 7)
QI2CM is the request flag for the I^2C bus(master) interrupt (I2CMINT).

QI2CM	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with QSIO0=0 or QSIO0=1. When using Assembler language, describe with RB QSIO0 or SB QSIO0.

9.2.12 Interrupt Request Register 3 (IRQ3)

Address: 0F01BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ3	¾	¾	QSD	QVC0	¾	¾	QTM1	QTM0
R/W	—	—	R/W	R/W	—	—	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ3 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ3 request flag is set to "1" regardless of the IE3 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE3) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ3 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ3 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **QTM0** (bit 0)
QTM0 is the request flag for the timer 0 interrupt (TM0INT).

QTM0	Description
0	No request (initial value)
1	Request

· **QTM1** (bit 1)
QTM1 is the request flag for the timer 1 interrupt (TM1INT).

QTM1	Description
0	No request (initial value)
1	Request

· **QVC0** (bit 4)
QVC0 is the request flag for the voice 0 interrupt (VC0INT).

QVC0	Description
0	No request (initial value)
1	Request

· **QSD** (bit 5)
QSD is the request flag for the speaker short detection interrupt (SDINT).

QSD	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ3) or to the interrupt enable register (IE3), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with QTM0=0 or QTM0=1. When using Assembler language, describe with RB QTM0 or SB QTM0.

9.2.13 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	¾	¾	¾	¾	¾	¾	¾	QUA0
R/W	—	—	—	—	—	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **QUA0** (bit 0)
QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with QUA0=0 or QUA0=1. When using Assembler language, describe with RB QUA0 or SB QUA0.

9.2.14 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	¾	¾	QTM3	QTM2	¾	¾	¾	¾
R/W	—	—	R/W	R/W	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **QTM2** (bit 4)
QTM2 is the request flag for the timer 2 interrupt (TM2INT).

QTM2	Description
0	No request (initial value)
1	Request

· **QTM3** (bit 5)
QTM3 is the request flag for the timer 3 interrupt (TM3INT).

QTM3	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with QTM2=0 or QTM2=1. When using Assembler language, describe with RB QTM2 or SB QTM2.

9.2.15 Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	Q32H	¾	Q128H	¾	¾	¾	¾	¾
R/W	R/W	—	R/W	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **Q128H** (bit 5)
Q128H is the request flag for the time base counter 128 Hz interrupt (T128HINT).

Q128H	Description
0	No request (initial value)
1	Request

· **Q32H** (bit 7)
Q32H is the request flag for the time base counter 32 Hz interrupt (T32HINT).

Q32H	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with Q128H=0 or Q128H=1. When using Assembler language, describe with RB Q128H or SB Q128H.

9.2.16 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	¾	¾	¾	¾	Q2H	¾	¾	Q16H
R/W	—	—	—	—	R/W	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

· **Q16H** (bit 0)
Q16H is the request flag for the time base counter 16 Hz interrupt (T16HINT).

Q16H	Description
0	No request (initial value)
1	Request

· **Q2H** (bit 3)
Q2H is the request flag for the time base counter 2 Hz interrupt (T2HINT).

Q2H	Description
0	No request (initial value)
1	Request

Notes:
· When an interrupt is generated by the instruction to write to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the the interrupt shift cycle starts after the next 1 instruction is executed.
· When rewriting a specific bit of the interrupt request flag, write it with bit symbols. When using C-language, describe with Q16H=0 or Q16H=1. When using Assembler language, describe with RB Q16H or SB Q16H.

9.3 Description of Operation

With the exception of the watchdog timer interrupt (WDTINT) and the NMI interrupt (NMINT), interrupt enable/disable for 24 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1 to 7). WDTINT and NMIINT are non-maskable interrupts.
When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 9-1 lists the interrupt sources.

Table 9-1 Interrupt Sources

Priority	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
2	NMI interrupt	NMINT	000AH
5	P80 interrupt	P00INT	0010H
6	P81 interrupt	P01INT	0012H
7	P82 interrupt	P02INT	0014H
8	P83 interrupt	P03INT	0016H
9	P84 interrupt	P04INT	0018H
10	P85 interrupt	P05INT	001AH
11	P86 interrupt	P06INT	001CH
12	P87 interrupt	P07INT	001EH
13	Synchronous serial port 0 interrupt	SIO0INT	0020H
14	Synchronous serial port 1 interrupt	SIO1INT	0022H
15	Successive approximation type A/D converter interrupt	SADINT	0024H
19	I^2C bus slave interrupt	I2CSINT	002CH
20	I^2C bus master interrupt	I2CMINT	002EH
21	Timer 0 interrupt	TM0INT	0030H
22	Timer 1 interrupt	TM1INT	0032H
25	Voice 0 interrupt	VC0INT	0038H
26	Speaker short detection interrupt	SDINT	003AH
29	UART 0 interrupt	UA0INT	0040H
41	Timer 2 interrupt	TM2INT	0058H
42	Timer 3 interrupt	TM3INT	005AH
50	TBC128Hz interrupt	T128HINT	006AH
52	TBC32Hz interrupt	T32HINT	006EH
53	TBC16Hz interrupt	T16HINT	0070H
56	TBC2Hz interrupt	T2HINT	0076H

Notes:
· When multiple interrupts are generated concurrently, the interrupts are serviced according to this priority and processing of low-priority interrupts is pending.
· A watchdog timer interrupt(WDTINT) and NMI interrupt(NMINT) are non-maskable interrupt. When a non-maskable interrupt occurs during interrupt proccessing, non-maskable interrupts are processed with priority. (Interrupt processing is interrupted regardless of whether or not multiple interrupts are enabled/disabled.)
· Also define the unused interrupt vector for fail-safe reasons.If unused interrupts occur, there is a possibility that the CPU has run out of control. It is recommended to generate a watchdog timer reset using an infinite loop and initialize the CPU.

9.3.1 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW toEPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to"1".
(6) Load the interrupt start address into PC.

9.3.2 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2.
(2) Transfer CSR to ECSR2.
(3) Transfer PSW to EPSW2.
(4) Set the ELEVEL field to "2".
(5) Load the interrupt start address into PC.

9.3.3 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1.
(2) Transfer CSR to ECSR1.
(3) Transfer PSW to EPSW1.
(4) Set the MIE flag to "0".
(5) Set the ELEVEL field to "1".
(6) Load the interrupt start address into PC.

Reference:
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U8/100 Core Instruction Manual".

9.3.4 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

State A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine
- A-1-1: When multiple interrupts are disabled
  - – Processing immediately after the start of interrupt routine execution
    No specific notes.
  - – Processing at the end of interrupt routine execution
    Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.
- A-1-2: When multiple interrupts are enabled
  - – Processing immediately after the start of interrupt routine execution
    Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
  - – Processing at the end of interrupt routine execution
    Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW

Example of description: State A-1-1

```
Intrpt_A-1-1;          ; A-1-1 state
  DI                   ; Disable interrupt
  :
  :
  :
  RTI                  ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: State A-1-2

```
Intrpt_A-1-2;          ; Start
PUSH ELR, EPSW         ; Save ELR and EPSW at the
                         beginning
  EI                   ; Enable interrupt
  :
  :
  :
  :
  :
  POP PC, PSW          ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

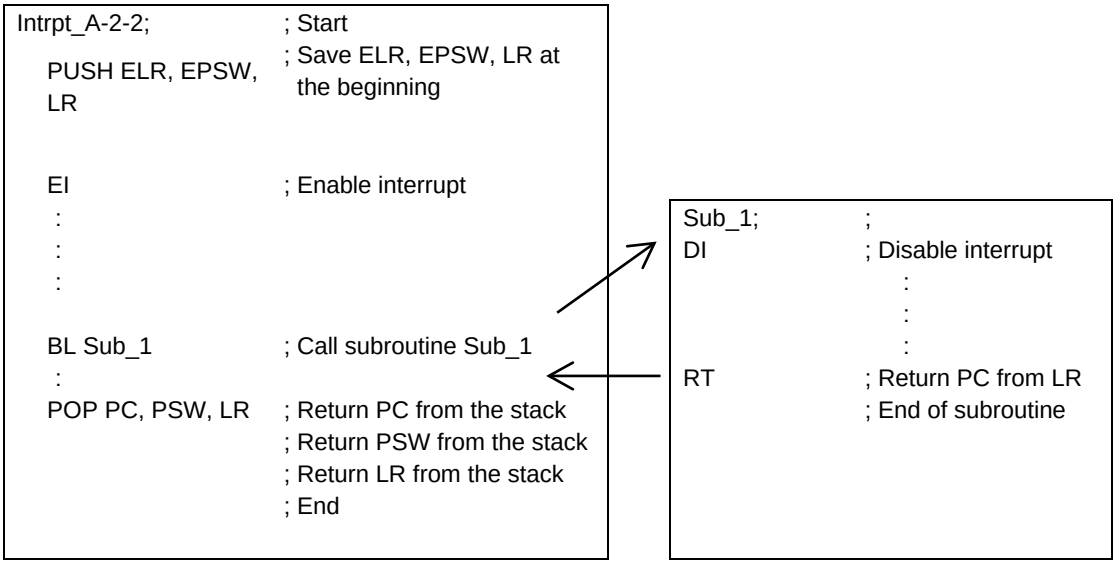
A-2-1: When multiple interrupts are disabled

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

- Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: A-2-2



State B: Non-maskable interrupt is being processed

B-1: When the interrupt processing is not executed in the interrupt routine.

- Processing immediately after the start of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to PC and those of the EPSW register to PSW.

B-2: When the interrupt processing is executed in the interrupt routine.

B-2-1: When a subroutine is not called by a program when the interrupt routine is executed.

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH ELR, EPSW" instruction to save the interrupt return address and the state of EPSW to the stack.
- Processing at the end of interrupt routine execution.
  Specify "POP PC, PSW" instead of the RTI instruction to return the saved data of the interrupt return address to PC, and the saved data of EPSW to PSW.

B-2-2: When a subroutine is called by a program when the interrupt routine is executed.

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR, ELR, EPSW" instruction to save the interrupt return address, the subroutine return address and the state of EPSW to the stack.
- Processing at the end of interrupt routine execution.
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: B-1

```
Intrpt_B-1;          ; State of B1
   RTI               ; Return PC from ELR
                     ; Return PSW from EPSW
                     ; End
```

Example of description: B-2-1

```
Intrpt_B-2-1:        ; Start
  PUSH  ELR, EPSW    ; Save ELR, EPSW
                       at the beginning
   :
   :
   :
  POP PC, PSW        ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

Example of description: B-2-2

```
Intrpt_B-2-2;        ; Start
   PUSH              ; Save ELR, EPSW, LR at
ELR, EPSW, LR        the beginning
    :
    :
    :
    BL Sub_1         ; Call subroutine Sub_1
:
   POP
   PC, PSW, LR       ; Return PC from the stack
                     ; Return PSW from the stack
                     ; Return LR from the stack
                     ; End
```

```
Sub_1;
                       :
                       :
                       :
RT                   ; Return PC from LR
                     ; End of subroutine
```

9.3.5 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1: Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine

When the interrupt conditions are satisfied in this section, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2: Between the DSR prefix instruction and the next instruction

When the interrupt conditions are satisfied in this section, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

Reference:
For the DSR prefix instruction, see "nX-U8/100 Core Instruction Manual".

Chapter 10

NMI Pin

10. NMI Pin

10.1 Overview

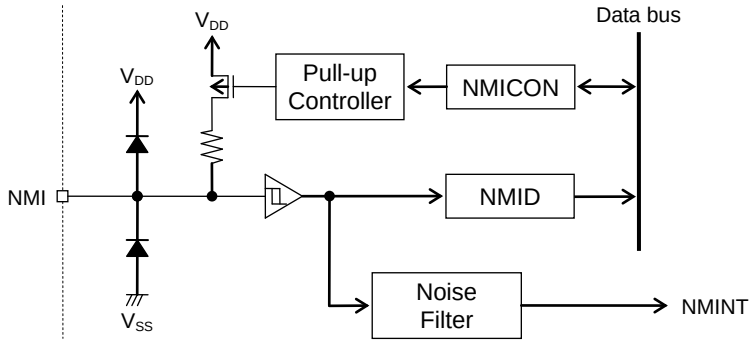
This LSI includes an input port (NMI) which generates a non-maskable interrupt.
For interrupts see Chapter 9, "Interrupts".

10.1.1 Features

- Non-maskable interrupt pin.
- Allows selection of an input with a pull-up resistor or a high-impedance input.
- Applies a noise filter to NMI interrupt (NMINT).

10.1.2 Configuration

Figure 10-1 shows the configuration of the NMI pin.



NMID : NMI data register
NMICON : NMI control register

Figure 10-1 Configuration of NMI Pin

10.1.3 List of Pins

Pin name	Input/output	Description
NMI	I	Non-maskable interrupt input port

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F200H	NMI data register	NMID	–	R	8	Depends on pin state
0F201H	NMI control register	NMICON	–	R/W	8	00H

10.2.2 NMI Data Register (NMID)

Address: 0F200H
Access: R
Access size: 8 bits
Initial value: Depends on the pin state

	7	6	5	4	3	2	1	0
NMID	—	—	—	—	—	—	—	NMI
R/W	—	—	—	—	—	—	—	R
Initial value	0	0	0	0	0	0	0	x

NMID is a read-only special function register (SFR) for reading the NMI pin level.

[Description of Bits]

- **NMI** (bit 0)
  The NMI bit is used to read the level of the NMI pin.

NMI	Description
0	"L" level
1	"H" level

10.2.3 NMI Control Register (NMICON)

Address：0F201H
Access：R/W
Access size：8 bits
Initial value：00H

	7	6	5	4	3	2	1	0
NMICON	—	—	—	—	—	—	—	NMIC
R/W	—	—	—	—	—	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

NMICON is a special function register (SFR) to select the input mode of the NMI pin.

[Description of Bits]

- **NMIC** (bit 0)
  The NMIC bit is used to select the input mode with or without a pull-up resistor.

NMIC	Description
0	Input mode with a pull-up resistor (initial value)
1	High-impedance input mode

10.3 Description of Operation

The non-maskable NMI interrupt (NMIINT) is assigned to the NMI pin.
The NMI pin allows selection of an input mode with a pull-up resistor or a high-impedance input mode by using the NMI control register (NMICON). At a system reset, the input mode with a pull-up resistor is selected.
The level of the NMI pin can be read by reading the NMI data register (MMID).

10.3.1 Interrupt Request

When a level change occurs at the NMI pin after the duration longer than the minimum NMI interrupt pulse width, a non-maskable interrupt which does not depend on the master interrupt enable flag (MIE) is generated.
Figure 10-2 shows the NMI interrupt generation timing.

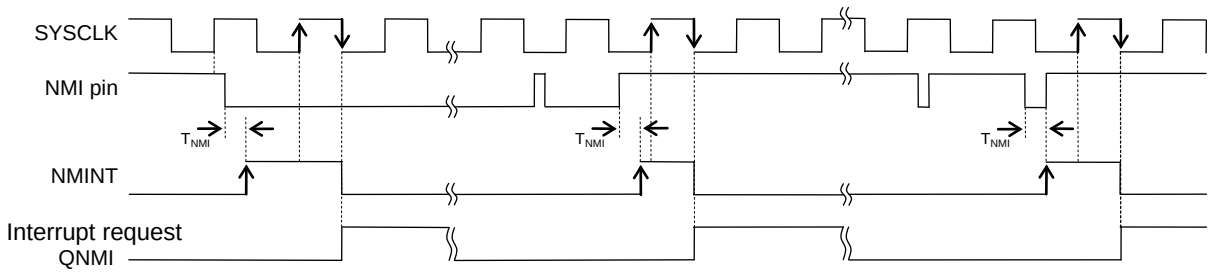


Figure 10-2 NMI Interrupt Generation Timing

Chapter 11

Time Base Counter

11. Time Base Counter

11.1 Overview

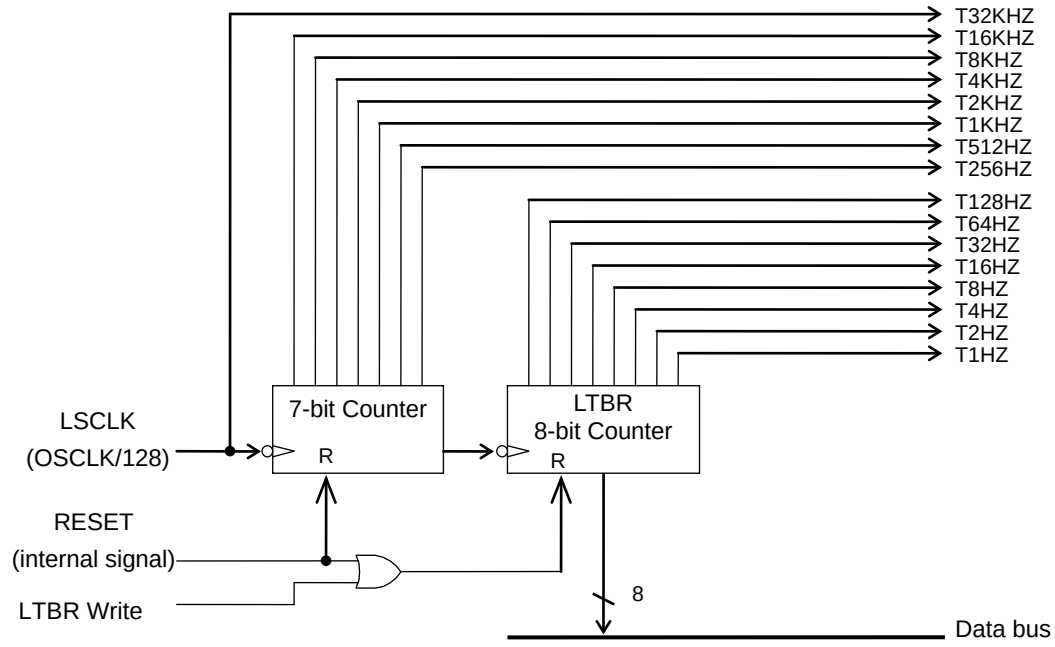
The time base counter generates base clocks for peripheral circuits and periodic interrupts. This LSI includes a low-speed time base counter (LTBC) and a high-speed time base counter (HTBC) that generate base clocks for peripheral circuits. By using the time base counter, it is possible to generate events periodically.
For input clocks, see Chapter 3, "Clock Generation Circuit". For interrupt permission, interrupt request flags, etc., described in this chapter, see Chapter 9, "Interrupts".

11.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK) frequency.
- HTBC generates HTB1 to HTB32 signals by dividing the high-speed clock (HSCLK) frequency.
- Capable of generating 128Hz , 32Hz , 16Hz , and 2Hz interrupts.

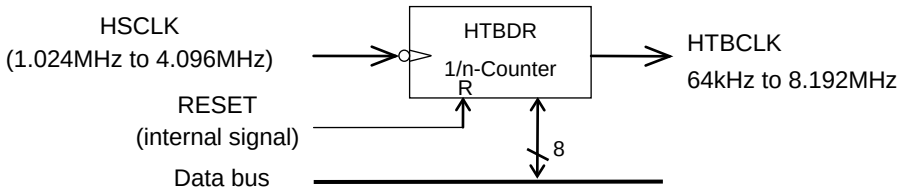
11.1.2 Configuration

Figure 11-1 and Figure 11-2 show the configuration of a low-speed time base counter and a high-speed time base counter, respectively.



LTBR: Low-speed time base counter register

Figure 11-1 Configuration of Low-Speed Time Base Counter (LTBC)



HTBDR: High-speed time base counter frequency divide register

Figure 11-2 Configuration of High-Speed Time Base Counter

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00AH	Low-speed time base counter register	LTBR	¾	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	¾	R/W	8	00H

11.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F00AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ to T1HZ outputs of the low-speed time base counter. The T128HZ to T1HZ outputs are set to "0" when write operation is performed for LTBR. Write data is invalid.

Note:
A TBC interrupt may occur depending on the LTBR write timing. Therefore, refer to the note on software programming in "11.3.1 Low-Speed Time Base Counter".

11.2.3 High-Speed Time Base Counter Divide Register (HTBDR)

Address: 0F00BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
HTBDR	¾	¾	¾	¾	HTD3	HTD2	HTD1	HTD0
R/W	¾	¾	¾	¾	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

HTBDR is a special function register (SFR) to set the divide ratio of the 4-bit, 1/n counter.

[Description of Bits]

· **HTD3 to HTD0** (bits 3 to 0)
The HTD3-HTD0 bits are used to set the frequency divide ratio of the 4-bit, 1/n counter. The frequency divide ratios selectable include 1/1 to 1/16.

HTD3	HTD2	HTD1	HTD0	Description	
				Divide ratio	Frequency of HTBCLK (*1)
0	0	0	0	´ 1/16 (initial value)	256 kHz
0	0	0	1	´ 1/15	273 kHz
0	0	1	0	´ 1/14	293 kHz
0	0	1	1	´ 1/13	315 kHz
0	1	0	0	´ 1/12	341 kHz
0	1	0	1	´ 1/11	372 kHz
0	1	1	0	´ 1/10	410 kHz
0	1	1	1	´ 1/9	455 kHz
1	0	0	0	´ 1/8	512 kHz
1	0	0	1	´ 1/7	585 kHz
1	0	1	0	´ 1/6	683 kHz
1	0	1	1	´ 1/5	819 kHz
1	1	0	0	´ 1/4	1024 kHz
1	1	0	1	´ 1/3	1365 kHz
1	1	1	0	´ 1/2	2048 kHz
1	1	1	1	´ 1/1	4096 kHz

*1: Indicates the frequency when the high-speed oscillation clock, HSCLK, is 4096 kHz.

11.3 Description of Operation

11.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
The T128HZ, T32HZ, T16HZ, and T2HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 11-3 shows an example of program to read LTBR.

```
volatile unsigned char tmp_LTBR_val = 0;

do {
tmp_LTBR_val = LTBR;                // 1st LTBR read
} while ( tmp_LTBR_val != LTBR );   // Comparison for 2nd LTBR read.
                                    // Repeat when this values don't coincide.
```

Figure 11-3 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". Write data is invalid. Since an interrupt occurs if a falling edge occurs in the T128Hz to T1Hz outputs during writing to LTBR, take care in software programming.
Figure 11-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.

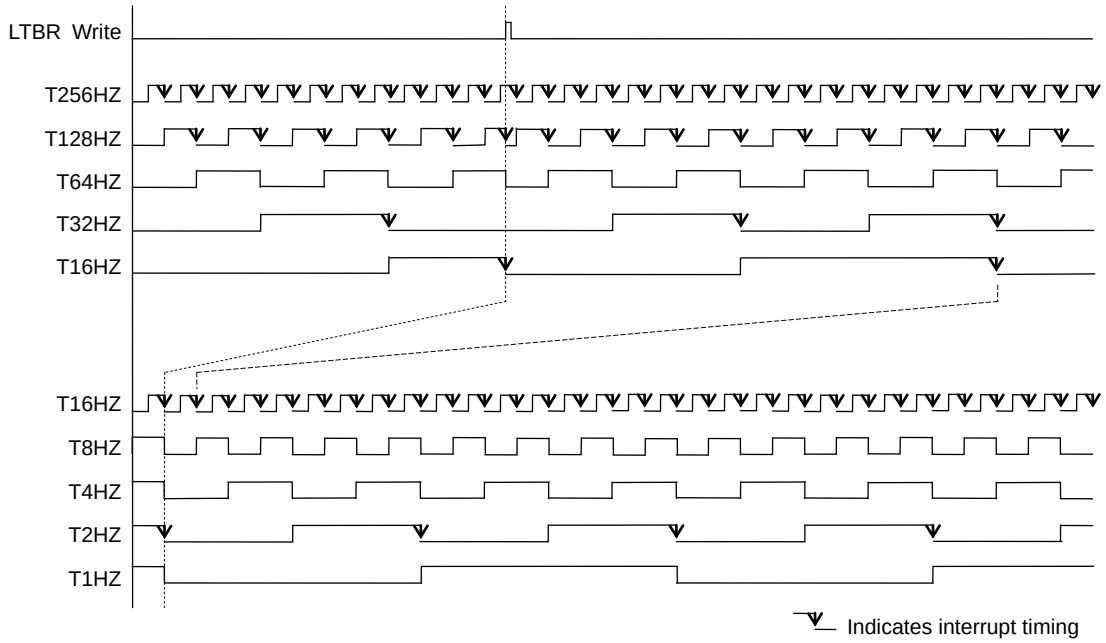


Figure 11-4 Interrupt Timing and Reset Timing by Writing to LTBR

11.3.2 High-Speed Time Base Counter

The high-speed time base counter is configured as a 4-bit 1/n counter (n = 1 to 16).
In the 4-bit 1/n counter, the divided clock (1/16´ HSCLK to 1/1´ HSCLK) selected by the high-speed time base counter divide register (HTBDR) is generated as HTBCLK. HTBCLK is used as a clock for the timer.
Figure 11-5 shows the output waveform of HTBCLK.

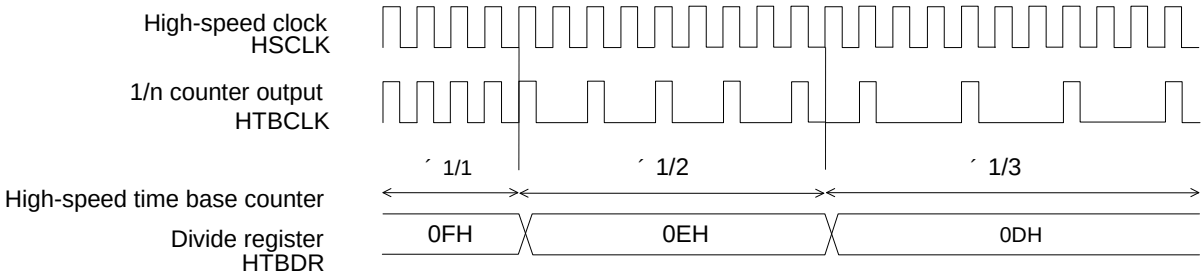


Figure 11-5 Output Waveform of HTBCLK

Chapter 12

Timers

12. Timers

12.1 Overview

This LSI has a 4-channels of 8-bit timers as Timer 0 to 3. Timers 0 to 3 operate only when the DTMn (n=0 to 3) bit of the block control register 0 (BLKCON0) is "0". When the DTMn bit is "1", every function of Timers n is in a reset state.

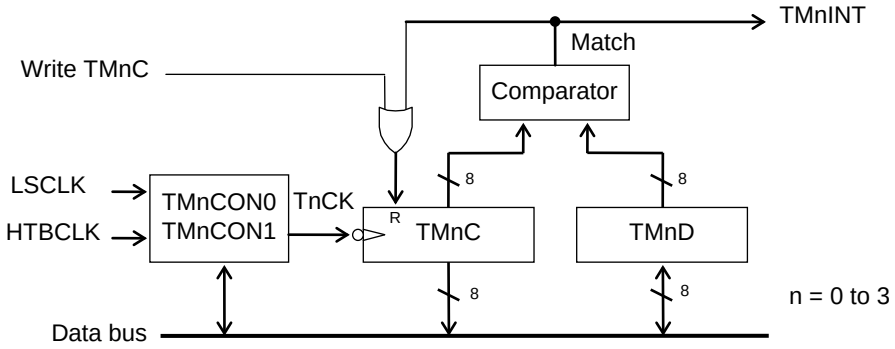
For the block control registers, see Chapter 5, "MCU Control Function". For input clocks, see Chapter 3, "Clock Generation Circuit".

12.1.1 Features

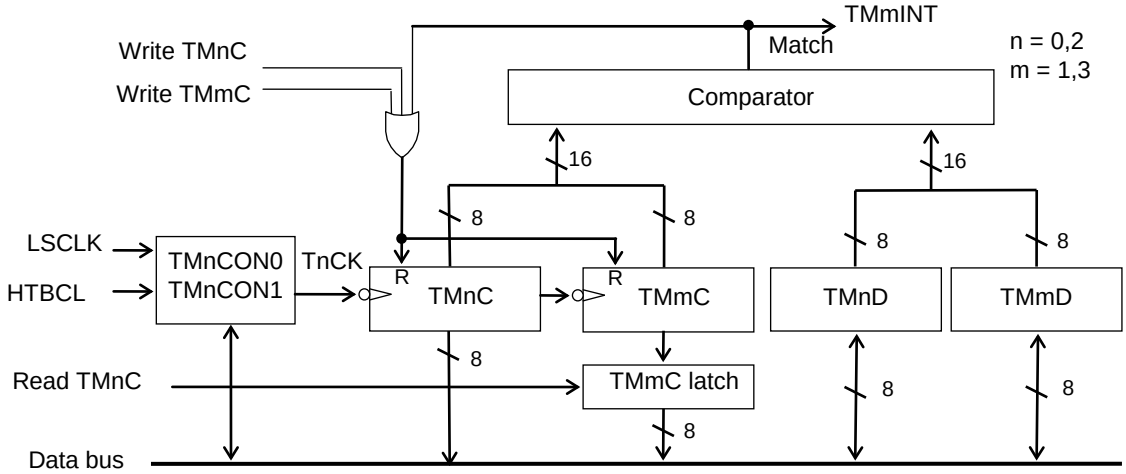
- The timer interrupt (TMnINT) is generated when the values of timer counter register (TMnC, n=0 to 3) and timer data register (TMnD) coincide.
- A timer configured by combining timer 0 and timer 1, timer 2 and timer 3 can be used as a 16-bit timer.
- For the timer clock, the low-speed clock (LSCLK) or high-speed time base clock (HTBCLK) can be selected.

12.1.2 Configuration

Figure 12-1 shows the configuration of the timers.



(a) 8-bit Timer Mode (Timers 0 to 3)



(b) 16-bit Timer Mode (Timers 0 to 3)

TMnCON0: Timer control register 0
TMnCON1: Timer control register 1
TMmD, TMnD: Timer data registers
TMmC, TMnC: Timer counter registers

Figure 12-1 Configuration of Timers

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F030H	Timer 0 data register	TM0D	TM0DC	R/W	8/16	0FFH
0F031H	Timer 0 counter register	TM0C		R/W	8	00H
0F032H	Timer 0 control register 0	TM0CON0	TM0CON	R/W	8/16	00H
0F033H	Timer 0 control register 1	TM0CON1		R/W	8	00H
0F034H	Timer 1 data register	TM1D	TM1DC	R/W	8/16	0FFH
0F035H	Timer 1 counter register	TM1C		R/W	8	00H
0F036H	Timer 1 control register 0	TM1CON0	TM1CON	R/W	8/16	00H
0F037H	Timer 1 control register 1	TM1CON1		R/W	8	00H
0F038H	Timer 2 data register	TM2D	TM2DC	R/W	8/16	0FFH
0F039H	Timer 2 counter register	TM2C		R/W	8	00H
0F03AH	Timer 2 control register 0	TM2CON0	TM2CON	R/W	8/16	00H
0F03BH	Timer 2 control register 1	TM2CON1		R/W	8	00H
0F03CH	Timer 3 data register	TM3D	TM3DC	R/W	8/16	0FFH
0F03DH	Timer 3 counter register	TM3C		R/W	8	00H
0F03EH	Timer 3 control register 0	TM3CON0	TM3CON	R/W	8/16	00H
0F03FH	Timer 3 control register 1	TM3CON1		R/W	8	00H

12.2.2 Timer 0 Data Register (TM0D)

Address: 0F030H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM0D	T0D7	T0D6	T0D5	T0D4	T0D3	T0D2	T0D1	T0D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM0D is a special function register (SFR) to set the value to be compared with the timer 0 counter register (TM0C) value.

Notes:
· Set TM0D while the timer 0 is stopped.
· In 8-bit timer mode, set "01H" to "0FFH" on TM0D. If "00H" is set, it behaves same as that "01H" is set.
· In 16-bit timer mode, set "0001H" to "0FFFFH" on TM1D, TM0D. If "0000H" is set, it behaves same as that "0001H" is set.

12.2.3 Timer 1 Data Register (TM1D)

Address: 0F034H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM1D	T1D7	T1D6	T1D5	T1D4	T1D3	T1D2	T1D1	T1D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM1D is a special function register (SFR) to set the value to be compared with the value of the timer 1 counter register (TM1C).

Notes:
· Set TM1D while the timer 1 is stopped.
· In 8-bit timer mode, set "01H" to "0FFH" on TM1D. If "00H" is set, it behaves same as that "01H" is set.
· In 16-bit timer mode, set "0001H" to "0FFFFH" on TM1D, TM0D. If "0000H" is set, it behaves same as that "0001H" is set.

12.2.4 Timer 2 Data Register (TM2D)

Address: 0F038H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM2D	T2D7	T2D6	T2D5	T2D4	T2D3	T2D2	T2D1	T2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM2D is a special function register (SFR) to set the value to be compared with the value of the timer 2 counter register (TM2C).

Notes:
· Set TM2D while the timer 2 is stopped.
· In 8-bit timer mode, set "01H" to "0FFH" on TM2D. If "00H" is set, it behaves same as that "01H" is set.
· In 16-bit timer mode, set "0001H" to "0FFFFH" on TM3D, TM2D. If "0000H" is set, it behaves same as that "0001H" is set.

12.2.5 Timer 3 Data Register (TM3D)

Address: 0F03CH
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM3D	T3D7	T3D6	T3D5	T3D4	T3D3	T3D2	T3D1	T3D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM3D is a special function register (SFR) to set the value to be compared with the value of the timer 3 counter register (TM3C).

Notes:
· Set TM3D while the timer 3 is stopped.
· In 8-bit timer mode, set "01H" to "0FFH" on TM3D. If "00H" is set, it behaves same as that "01H" is set.
· In 16-bit timer mode, set "0001H" to "0FFFFH" on TM3D, TM2D. If "0000H" is set, it behaves same as that "0001H" is set.

12.2.6 Timer 0 Counter Register (TM0C)

Address: 0F031H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0C	T0C7	T0C6	T0C5	T0C4	T0C3	T0C2	T0C1	T0C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM0C is performed, TM0C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM0C) or the higher counter (TM1C), both the lower and higher counters are set to "0000H".

During timer operation, the contents of TM0C may not be read depending on the conditions of the timer clock and the system clock.
Table 12-1 shows whether a TM0C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 12-1 TM0C Read Enable/Disable during Timer Operation

Timer clock T0CK	System clock SYSCLK	TM0C read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM0C twice until the last data coincides the previous data.
HTBCLK	HSCLK	Read enabled

12.2.7 Timer 1 Counter Register (TM1C)

Address: 0F035H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1C	T1C7	T1C6	T1C5	T1C4	T1C3	T1C2	T1C1	T1C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM1C is performed, TM1C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM0C) or the higher counter (TM1C), both the lower and higher counters are set to "0000H".
When reading TM1C in 16-bit timer mode, be sure to read TM0C first since the count value of TM1C is stored in the TM1C latch when TM0C is read.

During timer operation, the contents of TM1C may not be read depending on the conditions of the timer clock and the system clock.
Table 12-2 shows whether a TM1C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 12-2 TM1C Read Enable/Disable during Timer Operation

Timer clock T1CK	System clock SYSCLK	TM1C read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM1C twice until the last data coincides the previous data.
HTBCLK	HSCLK	Read enabled

Notes:
· When reading TM1C and TM0C in 16-bit timer mode, use the word-type instruction.
· When reading TM1C and TM0C by using the byte-type instruction, the counter of TM1C may count up before reading TM1C.

12.2.8 Timer 2 Counter Register (TM2C)

Address: 0F039H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2C	T2C7	T2C6	T2C5	T2C4	T2C3	T2C2	T2C1	T2C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM2C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM2C is performed, TM2C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM2C) or the higher counter (TM3C), both the lower and higher counters are set to "0000H".

During timer operation, the contents of TM2C may not be read depending on the conditions of the timer clock and the system clock.
Table 12-3 shows whether a TM2C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 12-3 TM2C Read Enable/Disable during Timer Operation

Timer clock T2CK	System clock SYSCLK	TM2C read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM2C twice until the last data coincides the previous data.
HTBCLK	HSCLK	Read enabled

12.2.9 Timer 3 Counter Register (TM3C)

Address: 0F03DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3C	T3C7	T3C6	T3C5	T3C4	T3C3	T3C2	T3C1	T3C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM3C is performed, TM3C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode, if a write operation is performed to either the lower counter (TM2C) or the higher counter (TM3C), both the lower and higher counters are set to "0000H".
When reading TM3C in 16-bit timer mode, be sure to read TM2C first since the count value of TM3C is stored in the TM3C latch when TM2C is read.

During timer operation, the contents of TM3C may not be read depending on the conditions of the timer clock and the system clock.
Table 12-4 shows whether a TM3C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 12-4 TM3C Read Enable/Disable during Timer Operation

Timer clock T3CK	System clock SYSCLK	TM3C read enable/disable
LSCLK	LSCLK	Read enabled
	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read consecutively TM3C twice until the last data coincides the previous data.
HTBCLK	HSCLK	Read enabled

Notes:
· When reading TM3C and TM2C in 16-bit timer mode, use the word-type instruction.
· When reading TM3C and TM2C by using the byte-type instruction, the counter of TM3C may count up before reading TM3C.

12.2.10 Timer 0 Control Register 0 (TM0CON0)

Address: 0F032H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON0	¾	¾	¾	¾	¾	T01M16	T0CS1	T0CS0
R/W	-	-	-	-	-	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON0 is a special function register (SFR) to control timer 0.
Rewrite TM0CON0 after TM0C is cleared by write operation on TM0C while the timer 0 is stopped (T0STAT of the TM0CON1 register is "0").

[Description of Bits]

· **T0CS1, T0CS0** (bits 1, 0)
The T0CS1 and T0CS0 bits are used for selecting the operation clock of timer 0. LSCLK or HTBCLK can be selected by these bits.

T0CS1	T0CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	Prohibited (timer does not operate)

· **T01M16** (bit 2)
The T01M16 bit is used for selecting the operating mode of timer 0 or timer 1.
In 8-bit timer mode, each timer 0 and timer 1 are operate as independent 8-bit timer.
In 16-bit timer mode, timer 0 and timer 1 are connected and they operate as a 16-bit timer.
In 16-bit timer mode, timer 1 is incremented by a timer 0 overflow signal. A timer 0 interrupt (TM0INT) is not generated.

T01M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

12.2.11 Timer 1 Control Register 0 (TM1CON0)

Address: 0F036H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON0	¾	¾	¾	¾	¾	¾	T1CS1	T1CS0
R/W	-	-	-	-	-	-	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON0 is a special function register (SFR) to control timer 1.
Rewrite TM1CON0 after TM1C is cleared by write operation on TM1C while timer 1 is stopped (T1STAT of the TM1CON1 register is "0").

[Description of Bits]

· **T1CS1, T1CS0** (bits 1, 0)
The T1CS1 and T1CS0 bits are used for selecting the operation clock of timer 1. LSCLK or HTBCLK can be selected by these bits.
In cases where the 16-bit timer mode has been selected by setting T01M16 of TM0CON to "1", the values of T1CS1 and T1CS0 are invalid.

T1CS1	T1CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	Prohibited (timer does not operate)

12.2.12 Timer 2 Control Register 0 (TM2CON0)

Address: 0F03AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2CON0	¾	¾	¾	¾	¾	T23M16	T2CS1	T2CS0
R/W	-	-	-	-	-	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM2CON0 is a special function register (SFR) to control timer 2.
Rewrite TM2CON0 after TM2C is cleared by write operation on TM2C while the timer 0 is stopped (T2STAT of the TM2CON1 register is "0").

[Description of Bits]

· **T2CS1, T2CS0** (bits 1, 0)
The T2CS1 and T2CS0 bits are used for selecting the operation clock of timer 0. LSCLK or HTBCLK can be selected by these bits.

T2CS1	T2CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	Prohibited (timer does not operate)

· **T23M16** (bit 2)
The T23M16 bit is used for selecting the operating mode of timer 2 or timer 3.
In 8-bit timer mode, each timer 2 and timer 3 are operate as independent 8-bit timer.
In 16-bit timer mode, timer 2 and timer 3 are connected and they operate as a 16-bit timer.
In 16-bit timer mode, timer 3 is incremented by a timer 2 overflow signal. A timer 2 interrupt (TM2INT) is not generated.

T23M16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

12.2.13 Timer 3 Control Register 0 (TM3CON0)

Address: 0F03EH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3CON0	¾	¾	¾	¾	¾	¾	T3CS1	T3CS0
R/W	-	-	-	-	-	-	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3CON0 is a special function register (SFR) to control timer 3.
Rewrite TM3CON0 after TM3C is cleared by write operation on TM3C while timer 3 is stopped (T3STAT of the TM3CON1 register is "0").

[Description of Bits]

· **T3CS1, T3CS0** (bits 1, 0)
The T3CS1 and T3CS0 bits are used for selecting the operation clock of timer 3. LSCLK or HTBCLK can be selected by these bits.
In cases where the 16-bit timer mode has been selected by setting T23M16 of TM2CON to "1", the values of T3CS1 and T3CS0 are invalid.

T3CS1	T3CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited (timer does not operate)
1	1	Prohibited (timer does not operate)

12.2.14 Timer 0 Control Register 1 (TM0CON1)

Address: 0F033H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM0CON1	T0STAT	¾	¾	¾	¾	¾	¾	T0RUN
R/W	R	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

TM0CON1 is a special function register (SFR) to control a timer 0.

[Description of Bits]

· **T0RUN** (bit 0)
The T0RUN bit is used for controlling count stop/start of timer 0.

T0RUN	Description
0	Stops counting
1	Starts counting

· **T0STAT** (bit 7)
The T0STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 0.

T0STAT	Description
0	Counting stopped
1	Counting in progress

12.2.15 Timer 1 Control Register 1 (TM1CON1)

Address: 0F037H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM1CON1	T1STAT	¾	¾	¾	¾	¾	¾	T1RUN
R/W	R	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

TM1CON1 is a special function register (SFR) to control timer 1.

[Description of Bits]

· **T1RUN** (bit 0)
The T1RUN bit is used for controlling count stop/start of timer 1.
In 16-bit timer mode, be sure to set this bit to "0". Timer 1 is incremented caused by a timer 0 overflow signal regardless of the value of T1RUN.

T1RUN	Description
0	Stops counting
1	Starts counting

· **T1STAT** (bit 7)
The T1STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 1.
In 16-bit timer mode, this bit will read "0".

T1STAT	Description
0	Counting stopped.
1	Counting in progress.

12.2.16 Timer 2 Control Register 1 (TM2CON1)

Address: 0F03BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2CON1	T2STAT	¾	¾	¾	¾	¾	¾	T2RUN
R/W	R	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

TM2CON1 is a special function register (SFR) to control a timer 2.

[Description of Bits]

· **T2RUN** (bit 0)
The T2RUN bit is used for controlling count stop/start of timer 2.

T2RUN	Description
0	Stops counting
1	Starts counting

· **T2STAT** (bit 7)
The T2STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 2.

T2STAT	Description
0	Counting stopped
1	Counting in progress

12.2.17 Timer 3 Control Register 1 (TM3CON1)

Address: 0F03FH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3CON1	T3STAT	¾	¾	¾	¾	¾	¾	T3RUN
R/W	R	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

TM3CON1 is a special function register (SFR) to control timer 3.

[Description of Bits]

· **T3RUN** (bit 0)
The T3RUN bit is used for controlling count stop/start of timer 3.
In 16-bit timer mode, be sure to set this bit to "0". Timer 3 is incremented caused by a timer 2 overflow signal regardless of the value of T3RUN.

T3RUN	Description
0	Stops counting
1	Starts counting

· **T3STAT** (bit 7)
The T3STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 3.
In 16-bit timer mode, this bit will read "0".

T3STAT	Description
0	Counting stopped.
1	Counting in progress.

12.3 Description of Operation

When the TnRUN bit of timer 0 to 3 control register 1 (TMnCON1) is set to "1", the timer counter (TMnC) is set to an operating state (TnSTAT is set to "1") on the first falling edge of the timer clock (TnCK) being selected by the Timer 0 to 3 control register 0 (TMnCON0). Then, the timer counter (TMnC) starts incrementing on the 2nd falling edge.

When the count value of TMnC and the timer 0 to 3 data register (TMnD) coincide, timer 0 to 3 interrupt (TMnINT) occurs on the next timer clock falling edge and at the same time, TMnC is reset to "00H" and continues incrementing.

When the TnRUN bit is set to "0", TMnC stops incrementing after counting the falling of the timer clock (TnCK) once. Confirm that TMnC has been stopped by checking that the TnSTAT bit of the Timer 0–3 control register 1 (TMnCON1) is "0". When the TnRUN bit is set to "1" again, TMnC restarts incrementing from the previous value. To initialize TMnC to "00H", perform a write operation to TMnC.
The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n = 0 \text{ to } 3)$$

TMnD: Timer 0 to 3 data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 0 to 3 control register 0 (TMnCON0)

After the TnRUN bit is set to "1", the timer is synchronized by the timer clock to start counting. Therefore, an error of a maximum of 1 clock period occurs until the first timer interrupt occurs. The timer interrupt periods from the second time onward are constant.
Figure 12-2 shows the operation timing diagram of Timer 0 to 3.

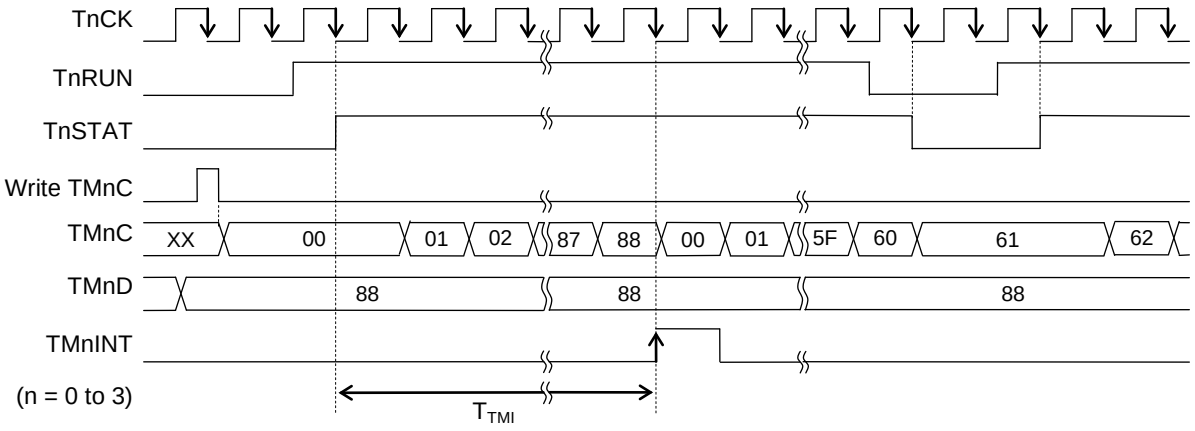


Figure 12-2 Operation Timing Diagram of Timer 0 to 3

Note:
Even if "0" is written to the TnRUN bit, counting operation continues up to the falling edge (the timer 0 to 3 status flag (TnSTA) is in a "1" state) of the next timer clock pulse. Therefore, the timer 0 to 3 interrupt (TMnINT) may occur.

Chapter 13

Watchdog Timer

13. Watchdog Timer

13.1 Overview

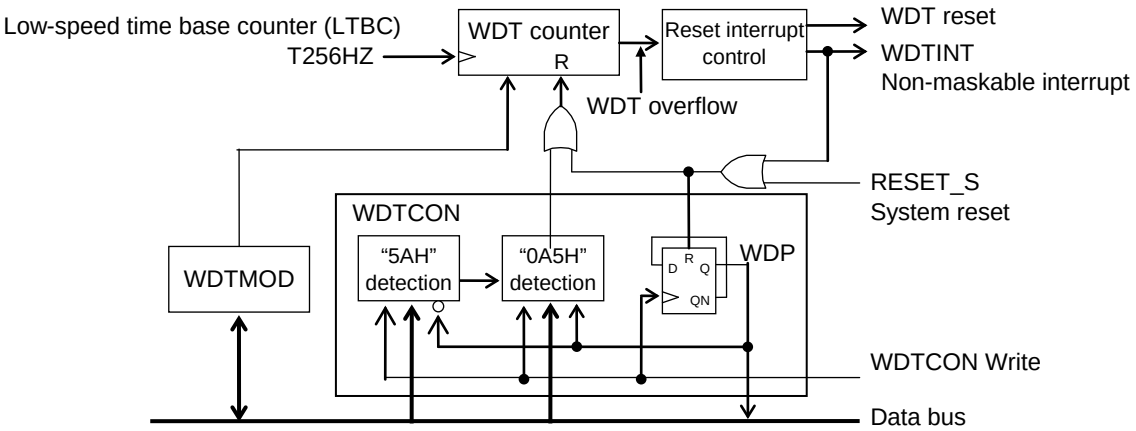
This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.
If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 9, "Interrupts," and for WDT interrupt see Chapter 4, "Reset Function".

13.1.1 Features

- Free running (cannot be stopped)
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable by software
- Non-maskable interrupt generated by the 1st overflow
- Reset generated by the 2nd overflow

13.1.2 Configuration

Figure 13-1 shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register

Figure 13-1 Configuration of Watchdog Timer

13.2 Description of Registers

13.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	–	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	–	R/W	8	02H

13.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	W	W	W	W	W	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to clear the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]

- **WDP/d0** (bit 0)
  The value of the internal pointer (WDP) is read from this bit. WDP is reset to "0" at system reset and when the WDT counter overflows, and is inverted each time awrite operation to WDTCON is performed.

- **d7～d0** (bits 7～0)
  This bit is used to write data to clear the WDT counter. The WDT counter can be cleared by writing "5AH" when the internal pointer(WDP) is "0" and then writing "0A5H" when the WDP is "1".

Note:
When a WDT interrupt(WDTINT) occurs due to the first overflow of the WDT counter, the WDT counter and internal pointer(WDP) are initialized for half the low speed clock(approx.15.26us). Therefore, writing to WDTCON during this time is invalid, and WDP is not inverted. When performing WDT clear process by WDT interrupt, in the state of high speed system clock, confirm that WDP has been inverted by writing to WDTCON. "13.3.1 Processing example when the watchdog timer is not used" shows an example of program description.

13.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: R/W
Access size: 8 bits
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	–	–	–	–	–	–	WDT1	WDT0
R/W	–	–	–	–	–	–	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the watchdog timer.

[Description of Bits]

- **WDT1～0** (bits 1～0)
  These bits are used to select an overflow period of the watchdog timer.
  The WDT1 and WDT0 bits set a overflow period (T_{WOV}) of the WDT counter. One of 125ms, 500ms, 2s, and 8s can be selected.

WDT1	WDT0	Description
0	0	125ms
0	1	500ms
1	0	2s (initial value)
1	1	8s

Note:
Clear the WDT counter before changing the overflow period.

13.3 Description of Operation

The WDT counter starts counting by low speed time base counter T256HZ after the system reset has been released and the low-speed clock oscillation start.
Write "5AH" when the internal pointer (WDP) is "0"and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to "0" at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a non-maskable watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (T_{WOV}) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 13-1.

Table 13-1 Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	125ms	Approx 121ms
0	1	500ms	Approx 496ms
1	0	2000ms	Approx 1996ms
1	1	8000ms	Approx 7996ms

Notes:
· A non-maskable watchdog timer interrupt is generated by the first overflow of the WDT, and a WDT reset is generated by the second overflow. The watchdog timer interrupt occurs at the first overflow as a warning. Use this interrupt to shut down the system or to restore the system safely.
· Even if the watchdog timer interrupt is not used, a watchdog timer occurs, so be sure to define a watchdog timer interrupt processing function.

Figure 13-2 shows an example of watchdog timer operation.

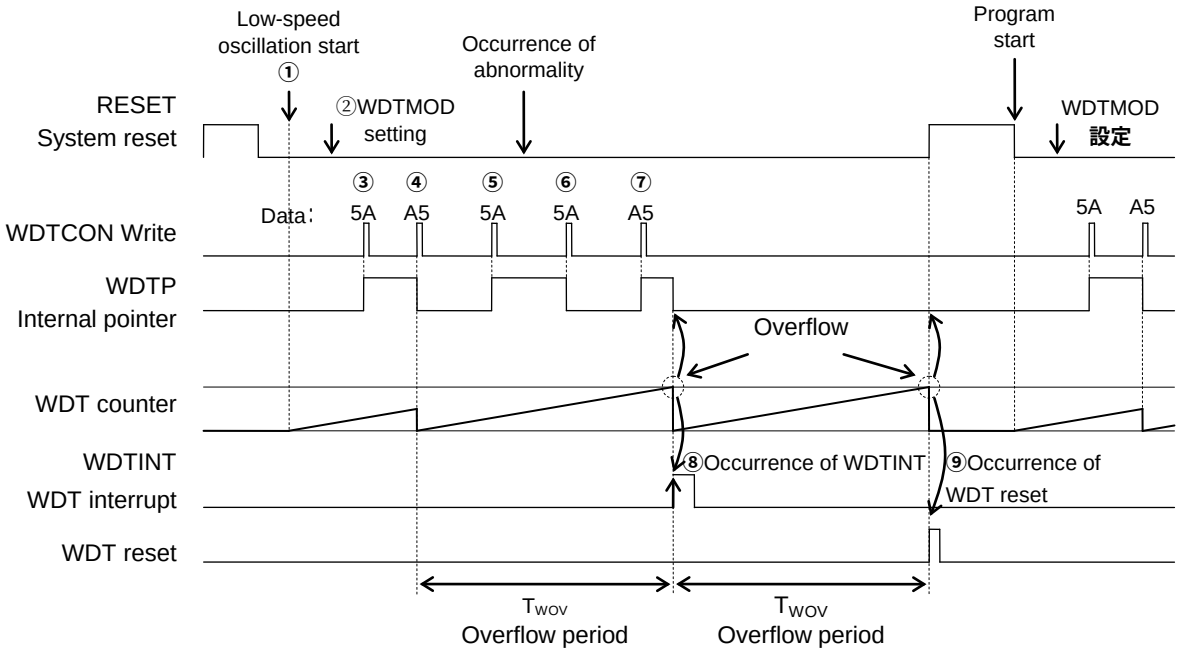


Figure 13-2 Example of Watchdog Timer Operation

j The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
k The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.
l "5AH" is written to WDTCON. (Internal pointer 0® 1)
m "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1® 0)
n "5AH" is written o WDTCON. (Internal pointer 0® 1)
o When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1® 0)
p Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in o. (Internal pointer 0® 1)
q The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. In this case, the WDT counter and internal pointer are initialized during a half cycle the low speed clock (Approx. 15.25us). (Internal pointer 0® 1)
r If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

Notes:
· In STOP mode, the watchdog timer operation also stops.
· In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
· The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

13.3.1 Handling example when not using the watchdog timer

The WDT counter is a free-run counter that starts counting up unconditionally when the low-speed clock(LSCLK) starts oscillating after a system reset is released. When the WDT counter overflows, a non-maskable interrupt or system reset occurs. Therefore, it is necessary to clear the WDT counter even if the WDT function is not used.
A program example for clearing the WDT counter in the WDT interrupt routine is as follows.

(program example)

```
__DI();          // Disable multiple interrupts
do
{
WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;
__EI();
```

Chapter 14

Synchronous Serial Port

14. Synchronous Serial Port

14.1 Overview

This LSI includes two channel of the 8/16-bit synchronous serial port (SSIO) as SSIO0 and SSIO1 and can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.
For the input clock, see Chapter 3, "Clock Generation Circuit".
When the synchronous serial port is used, the secondary functions of port 4 or tertiary functions of port 4 and port 8 must be set. For the secondary and tertiary functions of port 4, see Chapter 7, "Port 4", for the tertiary functions of port 8, see Chapter 8, "Port 8".
The synchronous serial port (SSIO0) operates only when the DSIO0 bit of the block control register 2 (BLKCON2) is "0". The synchronous serial port (SSIO1) operates only when the DSIO1 bit of the block control register 2 (BLKCON2) is "0". When the DSIO0 bit is "1", every function of SSIO0 is in a reset state. When the DSIO1 bit is "1", every function of SSIO1 is in a reset state.
For the block control registers, see Chapter 5, "MCU Control Function".

14.1.1 Features

- Master or slave selectable
- MSB first or LSB first selectable
- 8-bit length or 16-bit length selectable fro the data length
- Operation in SPI mode 0/3

14.1.2 Configuration

Figure 14-1 shows the configuration of the synchronous serial port 0 and 1.

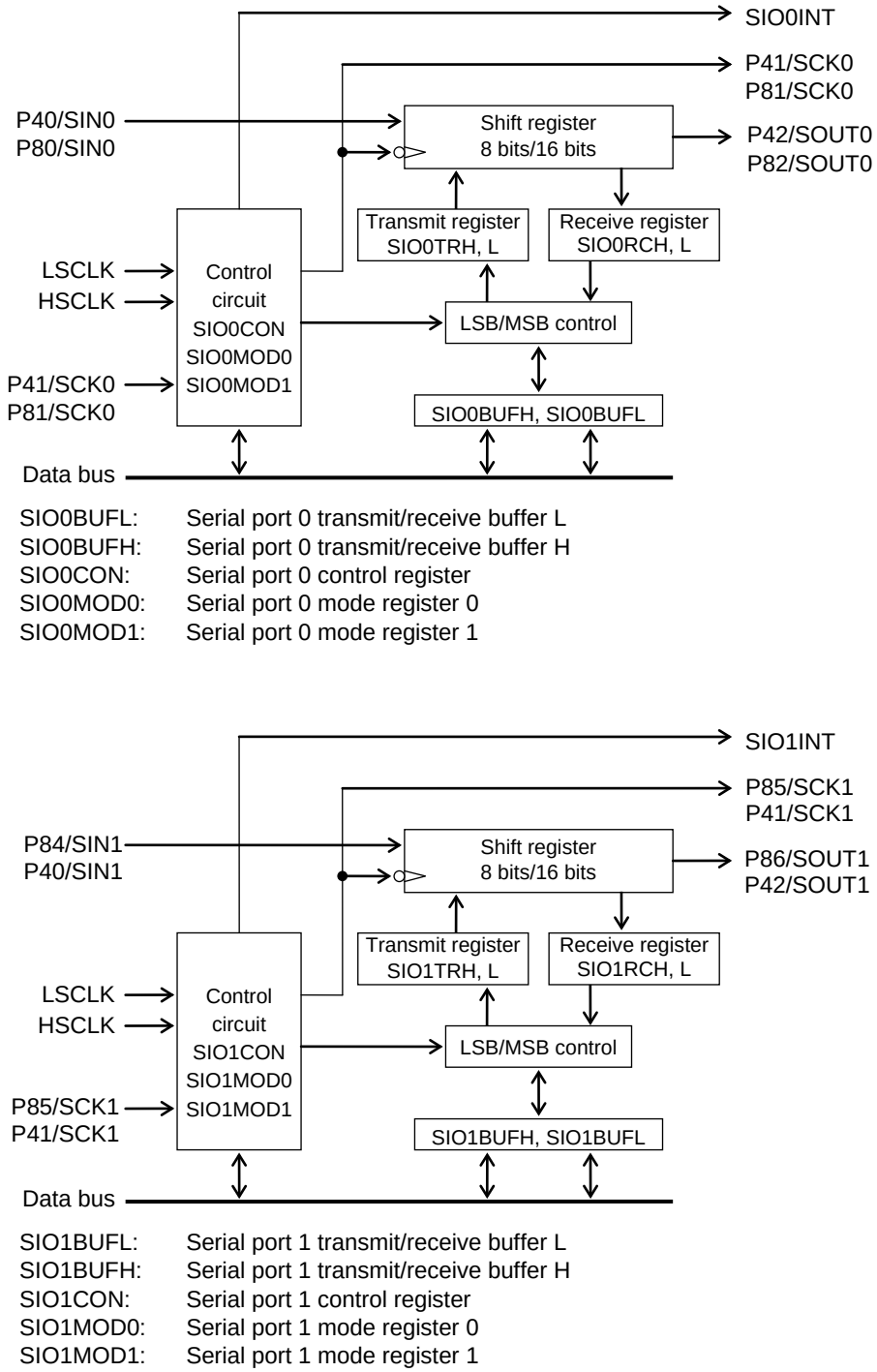


Figure 14-1 Configuration of Synchronous Serial Port 0 and 1

14.1.3 List of Pins

Pin name	I/O	Description
P40/SIN0	I	Receive data input. Used for the tertiary function of the P40 pin.
P41/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P41 pin.
P42/SOUT0	O	Transmit data output. Used for the tertiary function of the P42 pin.
P80/SIN0	I	Receive data input. Used for the tertiary function of the P80 pin.
P81/SCK0	I/O	Synchronous clock input/output. Used for the tertiary function of the P81 pin.
P82/SOUT0	O	Transmit data output. Used for the tertiary function of the P82 pin.
P84/SIN1	I	Receive data input. Used for the tertiary function of the P84 pin.
P85/SCK1	I/O	Synchronous clock input/output. Used for the tertiary function of the P85 pin.
P86/SOUT1	O	Transmit data output. Used for the tertiary function of the P86 pin.
P40/SIN1	I	Receive data input. Used for the secondary function of the P40 pin.
P41/SCK1	I/O	Synchronous clock input/output. Used for the secondary function of the P41 pin.
P42/SOUT1	O	Transmit data output. Used for the secondary function of the P42 pin.

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	¾	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F288H	Serial port 1 transmit/receive buffer L	SIO1BUFL	SIO1BUF	R/W	8/16	00H
0F289H	Serial port 1 transmit/receive buffer H	SIO1BUFH		R/W	8	00H
0F28AH	Serial port 1 control register	SIO1CON	¾	R/W	8	00H
0F28CH	Serial port 1 mode register 0	SIO1MOD0	SIO1MOD	R/W	8/16	00H
0F28DH	Serial port 1 mode register 1	SIO1MOD1		R/W	8	00H

14.2.2 Serial Port 0 Transmit/Receive Buffers (SIO0BUFL, SIO0BUFH)

Address: 0F280H
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFL	S0B7	S0B6	S0B5	S0B4	S0B3	S0B2	S0B1	S0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F281H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0BUFH	S0B15	S0B14	S0B13	S0B12	S0B11	S0B10	S0B9	S0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0BUFL and SIO0BUFH are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port 0.
When data is written in SIO0BUFL and SIO0BUFH, the data is written in the transmit registers (SIO0TRL and SIO0TRH) and when data is read from SIO0BUFL and SIO0BUFH, the contents of the receive registers (SIO0RCL and SIO0RCH) are read.

14.2.3 Serial Port 1 Transmit/Receive Buffers (SIO1BUFL, SIO1BUFH)

Address: 0F288H
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1BUFL	S1B7	S1B6	S1B5	S1B4	S1B3	S1B2	S1B1	S1B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F289H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1BUFH	S1B15	S1B14	S1B13	S1B12	S1B11	S1B10	S1B9	S1B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1BUFL and SIO1BUFH are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port 1.
When data is written in SIO1BUFL and SIO1BUFH, the data is written in the transmit registers (SIO1TRL and SIO1TRH) and when data is read from SIO1BUFL and SIO1BUFH, the contents of the receive registers (SIO1RCL and SIO1RCH) are read.

14.2.4 Serial Port 0 Control Register (SIO0CON)

Address: 0F282H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0CON	¾	¾	¾	¾	¾	¾	¾	S0EN
R/W	-	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0CON is a special function register (SFR) to control the synchronous serial port 0.

[Description of Bits]

· **S0EN** (bit 0)
The S0EN bit is used to specify start of synchronous serial port 0 communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated. The S0EN bit is set to "0" at a system reset.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

14.2.5 Serial Port 1 Control Register (SIO1CON)

Address: 0F28AH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1CON	¾	¾	¾	¾	¾	¾	¾	S1EN
R/W	-	-	-	-	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1CON is a special function register (SFR) to control the synchronous serial port 1.

[Description of Bits]

· **S1EN** (bit 0)
The S1EN bit is used to specify start of synchronous serial port 1 communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated. The S1EN bit is set to "0" at a system reset.

S1EN	Description
0	Stops communication. (Initial value)
1	Starts communication

14.2.6 Serial Port 0 Mode Register 0 (SIO0MOD0)

Address: 0F284H
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD0	¾	¾	¾	¾	S0LG	S0MD1	S0MD0	S0DIR
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD0 is a special function register (SFR) to set mode of the synchronous serial port 0.

[Description of Bits]

· **S0DIR** (bit 0)
The S0DIR is used to select LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

· **S0MD1, S0MD0** (bits 2, 1)
The S0MD1 and S0MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port 0.

S0MD1	S0MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

· **S0LG** (bit 3)
The S0LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.
The S0LG bit is set to "0" at a system reset.

S0LG	Description
0	8-bit length (initial value)
1	16-bit length

Notes:
· Please do not change any of the SIO0MOD0 register settings during transmission/reception.
· When the synchronous serial port 0 is used, the tertiary functions of Port 4 and Port 8 must be set. For the tertiary functions of Port 4, see Chapter 7, "Port 4", and for the tertiary functions of Port 8, see Chapter 8, "Port 8".

14.2.7 Serial Port 1 Mode Register 0 (SIO1MOD0)

Address: 0F28CH
Access: R/W
Access size: 8 bits /16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1MOD0	¾	¾	¾	¾	S1LG	S1MD1	S1MD0	S1DIR
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1MOD0 is a special function register (SFR) to set mode of the synchronous serial port 1.

[Description of Bits]

· **S1DIR** (bit 0)
The S1DIR is used to select LSB first or MSB first.

S1DIR	Description
0	LSB first (initial value)
1	MSB first

· **S1MD1, S1MD0** (bits 2, 1)
The S1MD1 and S1MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port 1.

S1MD1	S1MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

· **S1LG** (bit 3)
The S1LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.
The S1LG bit is set to "0" at a system reset.

S1LG	Description
0	8-bit length (initial value)
1	16-bit length

Notes:
· Please do not change any of the SIO1MOD0 register settings during transmission/reception.
· When the synchronous serial port 1 is used, the secondary functions of Port 4 or the tertiary functions of Port 8 must be set. For the secondary functions of Port 4, see Chapter 7, "Port 4", and for the tertiary functions of Port 8, see Chapter 8, "Port 8".

14.2.8 Serial Port 0 Mode Register 1 (SIO0MOD1)

Address: 0F285H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO0MOD1	¾	¾	S0NEG	S0CKT	S0CK3	S0CK2	S0CK1	S0CK0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD1 is a special function register (SFR) to set mode of the synchronous serial port 0.

[Description of Bits]

· **S0CK3 to S0CK0** (bits 3 to 0)
The S0CK3 to S0CK0 bits are used to select the transfer clock of the synchronous serial port 0. When the internal clock is selected, this LSI is set to master mode, and when the external clock is selected, it is set to slave mode.

S0CK3	S0CK2	S0CK1	S0CK0	Description
0	0	0	0	1/1 LSCLK (initial value)
0	0	0	1	1/2 LSCLK
0	0	1	0	1/4 HSCLK
0	0	1	1	1/8 HSCLK
0	1	0	0	1/16 HSCLK
0	1	0	1	1/32 HSCLK
0	1	1	0	External clock 0 (P41/SCK0)
0	1	1	1	External clock 0 (P81/SCK0)
1	0	0	0	1/1 HSCLK
1	0	0	1	1/2 HSCLK
1	0	1	Ú	Prohibited
1	1	Ú	Ú	Prohibited

· **S0CKT** (bit 4)
The S0CKT bit is used to select a tansfer clock output phase. When S0CKT is set to "0", it operates in SPI mode 3, and when S0CKT is set to "1", it operates in SPI mode 0. S0CKT setting is invalid in slave mode.

S0CKT	Description
0	Clock type 0: Clock is output with a "H" level being the default. (Initial value)
1	Clock type 1: Clock is output with a "L" level being the default.

· **S0NEG** (bit 5)
The S0NEG is a bit which chooses the positive logic or negative logic of a transfer clock output.

S0NEG	Description
0	Positive logic (Initial value)
1	Negative logic

Notes:
– Do not change the value of the SIO0MOD1 register during transmission or reception.
– Please set up not to exceed 4.2 MHz about S0CK0 to S0CK3 bits.

14.2.9 Serial Port 1 Mode Register 1 (SIO1MOD1)

Address: 0F28DH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SIO1MOD1	¾	¾	S1NEG	S1CKT	S1CK3	S1CK2	S1CK1	S1CK0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO1MOD1 is a special function register (SFR) to set mode of the synchronous serial port 1.

[Description of Bits]

· **S1CK3 to S1CK0** (bits 3 to 0)
The S1CK3 to S1CK0 bits are used to select the transfer clock of the synchronous serial port 1. When the internal clock is selected, this LSI is set to master mode, and when the external clock is selected, it is set to slave mode.

S1CK3	S1CK2	S1CK1	S1CK0	Description
0	0	0	0	1/1 LSCLK (initial value)
0	0	0	1	1/2 LSCLK
0	0	1	0	1/4 HSCLK
0	0	1	1	1/8 HSCLK
0	1	0	0	1/16 HSCLK
0	1	0	1	1/32 HSCLK
0	1	1	0	External clock 1 (P85/SCK1)
0	1	1	1	External clock 1 (P41/SCK1)
1	0	0	0	1/1 HSCLK
1	0	0	1	1/2 HSCLK
1	0	1	Ú	Prohibited
1	1	Ú	Ú	Prohibited

· **S1CKT** (bit 4)
The S1CKT bit is used to select a tansfer clock output phase. When S1CKT is set to "0", it operates in SPI mode 3, and when S1CKT is set to "1", it operates in SPI mode 0. S1CKT setting is invalid in slave mode.

S1CKT	Description
0	Clock type 0: Clock is output with a "H" level being the default. (Initial value)
1	Clock type 1: Clock is output with a "L" level being the default.

· **S1NEG** (bit 5)
The S1NEG is a bit which chooses the positive logic or negative logic of a transfer clock output.

S1NEG	Description
0	Positive logic (Initial value)
1	Negative logic

Notes:
– Do not change the value of the SIO1MOD1 register during transmission or reception.
– Please set up not to exceed 4.2 MHz about S1CK0 to S1CK3 bits.

14.3 Description of Operation

14.3.1 Transmit Operation

When "1" is written to the SnMD1 bit and "0" is written to the SnMD0 bit of the serial port n (n=0, 1) mode register (SIOnMOD0), this LSI is set to a transmit mode.
When transmit data is written to the serial port n transmit /receive buffer (SIOnBUFL and H) and the SnEN bit of the serial port n control register (SIOnCON) is set to "1", transmission starts. When transmission of 8/16-bit data terminates, a synchronous serial port n interrupt (SIOnINT) occurs and the SnEN bit is set to "0".
Transmit data is output from the secondary function pin (P42/SOUT1) or the tertiary function pins (P42/SOUT0, P82/SOUT0, P86/SOUT1) of GPIO.
When an internal clock is selected in the serial port n mode register (SIOnMOD1), the LSI is set to a master mode and when an external clock (P41/SCK0,P41/SCK1,P81/SCK0,P85/SCK1) is selected, the LSI is set to a slave mode.
The serial port n mode register (SIOnMOD0) enables selection of MSB first/LSB first.
The transmit data output pin (P42/SOUT0, P82/SOUT0, P86/SOUT1) and transfer clock input/output pin (P41/SCK0, P81/SCK0, P85/SCK1) must be set to the tertiary functions. The transmit data output pin (P42/SOUT1) and transfer clock input/output pin (P41/SCK1) must be set to the secondary functions.
Figures 14-2 and 14-3 show the transmit operation waveforms of the synchronous serial ports n for clock type 0 (SPI mode 3) and clock type 1 (SPI mode 0), respectively (8-bit length, LSB first).

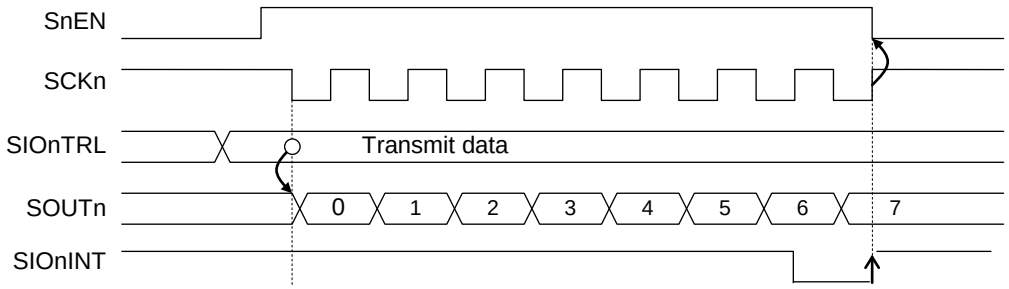


Figure 14-2 Transmit Operation Waveforms of Synchronous Serial Port n for Clock Type 0 (8-bit Length, LSB first, n=0,1)

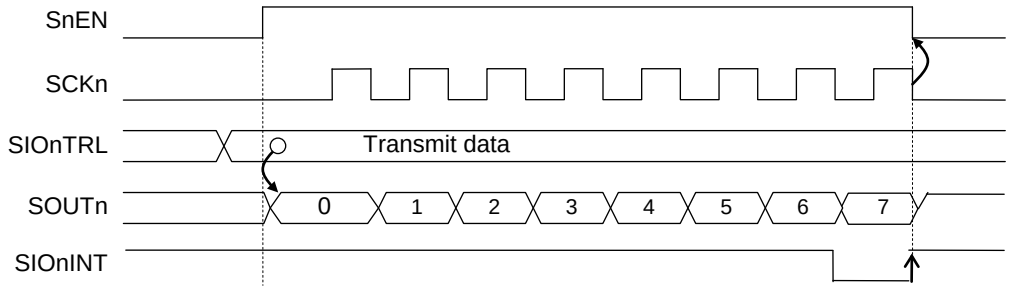


Figure 14-3 Transmit Operation Waveforms of Synchronous Serial Port n for Clock Type 1 (8-bit Length, LSB first, n=0,1)

14.3.2 Receive Operation

When "0" is written to the SnMD1 bit and "1" is written to the SnMD0 bit of the serial port n(n=0,1) mode register (SIOnMOD0), this LSI is set to a receive mode.
When the SnEN bit of the serial port n control register (SIOnCON) is set to "1", reception starts. When reception of 8/16-bit data terminates, a synchronous serial port n interrupt (SIOnINT) occurs and the SnEN bit is set to "0".
Receive data is input from the secondary function pin (P40/SIN1) or the tertiary function pin (P40/SIN0, P80/SIN0, P84/SIN1) of GPIO.
When an internal clock is selected in the serial port n mode register (SIOnMD1), the LSI is set to a master mode and when an external clock (P41/SCK0,P81/SCK0,P41/SCK1,P85/SCK1) is selected, the LSI is set to a slave mode.
The serial port n mode register (SIOnMOD0) enables selection of MSB first or LSB first.
The receive data input pin (P40/SIN0,P80/SIN0,P84/SIN1) and transfer clock input/output pin (P41/SCK0,P81/SCK0,P85/SCK1) must be set to the tertiary function. The receive data input pin (P40/SIN1) and transfer clock input/output pin (P41/SCK1) must be set to the secondary function.
Figures 14-4 and 14-5 show the receive operation waveforms of the synchronous serial port n for clock type 0 (SPI mode 3) and clock type 1 (SPI mode 0), respectively (8-bit length, MSB first).

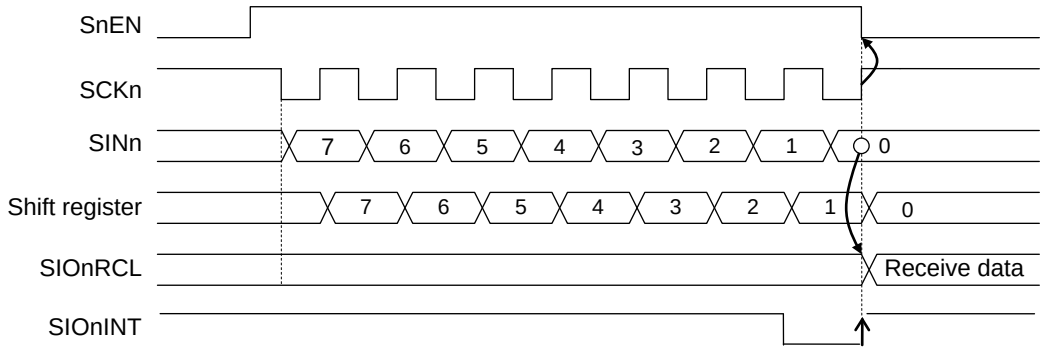


Figure 14-4 Transmit Operation Waveforms of Synchronous Serial Port n for Clock Type 0 (SPI mode 3) (8-bit Length, MSB first, n=0,1)

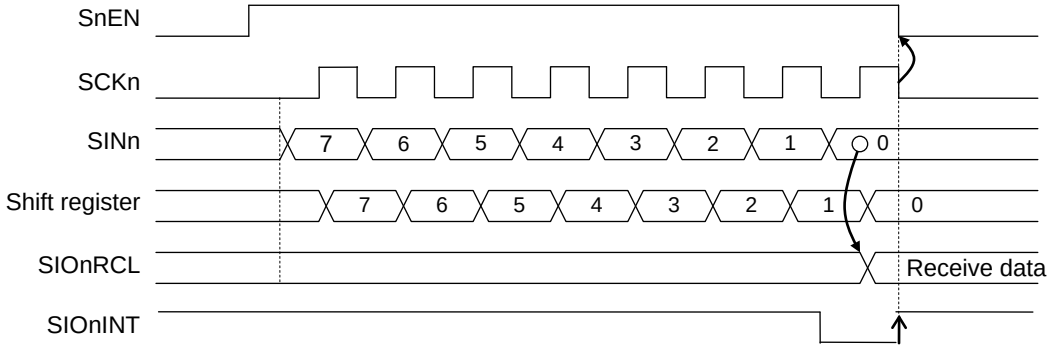


Figure 14-5 Transmit Operation Waveforms of Synchronous Serial Port n for Clock Type 1 (SPI mode 0) (8-bit Length, MSB first, n=0,1)

Note:
When the SOUTn pin is set to the secondary or tertiary function output in receive mode, a "H" level is output from the SOUTn output pin.

14.3.3 Transmit/Receive Operation

When "1" is written to the SnMD1 bit and "1" is written to the SnMD0 bit of the serial port n(n=0,1) mode register (SIOnMOD0), this LSI is set to a transmit/receive mode.
When the SnEN bit of the serial port n control register (SIOnCON) is set to "1", transmission/reception starts. When transmission/reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIOnINT) occurs and the SnEN bit is set to "0".
Receive data is input from the secondary function pin (P40/SIN1) or tertiary function pins (P40/SIN0, P80/SIN0, P84/SIN1) of GPIO, and transmit data is output from the secondary function pin (P42/SOUT1) or tertiary function pins (P42/SOUT0, P82/SOUT0, P86/SOUT1) of GPIO
When an internal clock is selected in the serial port n mode register (SIOnMD1), the LSI is set to a master mode and when an external clock (P41/SCK0,P81/SCK0, P41/SCK1,P85/SCK1) is selected, the LSI is set ot a slave mode.
The serial port n mode register (SIOnMOD0) enables selection of MSB first or LSB first.
The receive data input pin (P40/SIN0,P80/SIN0,P84/SIN1), the transmit data output pin (P42/SOUT0,P82/SOUT0,P86/SOUT1), and transfer clock input/output pin (P41/SCK0,P81/SCK0,P85/SCK1) must be set to the tertiary function. The receive data input pin (P40/SIN1), the transmit data output pin (P42/SOUT1), and transfer clock input/output pin (P41/SCK1) must be set to the secondary function.
Figure 14-6 shows the transmit/receive operation waveforms of the synchronous serial port n (16-bit length, LSB first, clock types 0(SPI mode 3)).

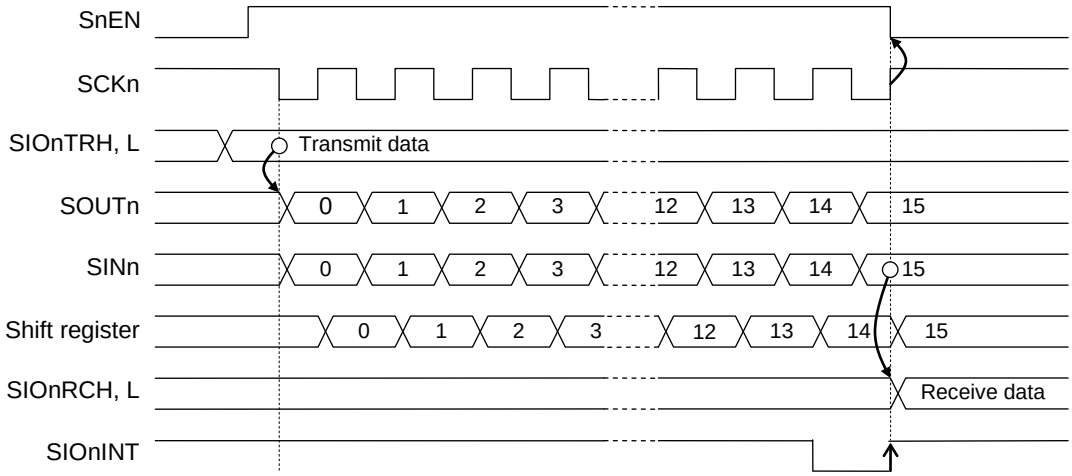


Figure 14-6 Transmit/Receive Operation Waveforms of Synchronous Serial Port n (16-bit Length, LSB first, Clock Type 0 (SPI mode 3), n=0,1)

14.4 Register setup of the port

For enable the SSIO function, each related port register needs to be set up. Refer to the Chapter 7, "Port 4" and Chapter 8, "Port 8" for details of each register.

14.4.1 When operating the SSIO0 function in master mode using P42 pin (SOUT0:output), P41 pin (SCK0:input/output), and P40 pin (SIN0:input).

SSIO is selected as the tertiary function of P42, P41, and P40 by setting P42MD1 to P40MD1 bit (P4MOD1 register: bits2 to 0) to "1" and setting P42MD0 to P40MD0 bit (P4MOD0 register: bit2s to 0) to "0".

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD1**	**P41MD1**	**P40MD1**
value	-	-	-	-	-	**1**	**1**	**1**

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD0**	**P41MD0**	**P40MD0**
value	-	-	-	-	-	**0**	**0**	**0**

The state of the P42 and P41 pin is selected as CMOS output mode by setting P42C1 to P41C1 bit (P4CON1 register:bits2 to 1) to "1" , setting P42C0 to P41C0 bit (P4CON0 register:bits2 to 1) to "1" and setting P42DIR to P41DIR bit (P4DIR register:bits2 to 1) to "0". Additionally, the P40 pin is selected as input pin by setting P40DIR bit (P4DIR register: bit0) to "1"
The setting value of P40C1 bit and P40C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the P40 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C1	**P42C1**	**P41C1**	**P40C1**
value	-	-	-	-	*	**1**	**1**	**$**

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C0	**P42C0**	**P41C0**	**P40C0**
value	-	-	-	-	*	**1**	**1**	**$**

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
value	-	-	-	-	*	**0**	**0**	**1**

As for P42D to P40D bit (P4D register:bits2 to 0), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43D	**P42D**	**P41D**	**P40D**
value	-	-	-	-	*	******	******	******

- : not existing * : no relation to the SSIO0 function **: Don't care $: Optional

14.4.2 When operating the SSIO0 function in slave mode using P42 pin (SOUT0:output), P41 pin (SCK0:input/output), and P40 pin (SIN0:input).

SSIO is selected as the tertiary function of P42, P41, and P40 by setting P42MD1 to P40MD1 bit (P4MOD1 register: bits2 to 0) to "1" and setting P42MD0 to P40MD0 bit (P4MOD0 register: bits2 to 0) to "0". It is the same setup as the case of master mode.

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD1**	**P41MD1**	**P40MD1**
value	-	-	-	-	-	**1**	**1**	**1**

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD0**	**P41MD0**	**P40MD0**
value	-	-	-	-	-	**0**	**0**	**0**

The state of the P42 pin is selected as CMOS output mode by setting P42C1 bit (P4CON1 register:bit2) to "1" , setting P42C0 bit (P4CON0 register:bit2) to "1" and setting P42DIR bit (P4DIR register:bit2) to "0". Additionally, the P41 and P40 pin is selected as input pin by setting P41DIR to P40DIR bit (P4DIR register: bits1 to 0) to "1"
The setting value of P41C1 to P40C1 bit and P41C0 to P40C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P41 and P40 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C1	**P42C1**	**P41C1**	**P40C1**
value	-	-	-	-	*	**1**	**$**	**$**

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C0	**P42C0**	**P41C0**	**P40C0**
value	-	-	-	-	*	**1**	**$**	**$**

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
value	-	-	-	-	*	**0**	**1**	**1**

As for P42D to P40D bit (P4D register:bits2 to 0), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43D	**P42D**	**P41D**	**P40D**
value	-	-	-	-	*	******	******	******

- : not existing * : no relation to the SSIO0 function **: Don't care $: Optional

14.4.3 When operating the SSIO0 function in master mode using P82 pin (SOUT0:output), P81 pin (SCK0:input/output), and P80 pin (SIN0:input).

SSIO is selected as the tertiary function of P82, P81, and P80 by setting P82MD1 to P80MD1 bit (P8MOD0 register: bits2 to 0) to "1" and setting P82MD0 to P80MD0 bit (P8MOD0 register: bits2 to 0) to "0".

register	P8MOD1 register (Address:0F245H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87MD1	P86MD1	P85MD1	P84MD1	P83MD1	**P82MD1**	**P81MD1**	**P80MD1**
value	*	*	*	*	*	**1**	**1**	**1**

register	P8MOD0 register (Address:0 F244H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87MD0	P86MD0	P85MD0	P84MD0	P83MD0	**P82MD0**	**P81MD0**	**P80MD0**
value	*	*	*	*	*	**0**	**0**	**0**

The state of the P82 and P81 pin is selected as CMOS output mode by setting P82C1 to P81C1 bit (P8CON1 register:bits2 to 1) to "1" , setting P82C0 to P81C0 bit (P8CON0 register:bits2 to 1) to "1" and setting P82DIR to P81DIR bit (P8DIR register:bits2 to 1) to "0". Additionally, the P80 pin is selected as input pin by setting P80DIR bit (P8DIR register: bit0) to "1"
The setting value of P80C1 bit and P80C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the P80 pin is connected.

register	P8CON1 register (Address:0F243H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87C1	P86C1	P85C1	P84C1	P83C1	**P82C1**	**P81C1**	**P80C1**
value	*	*	*	*	*	**1**	**1**	**$**

register	P8CON0 register (Address:0F242H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87C0	P86C0	P85C0	P84C0	P83C0	**P82C0**	**P81C0**	**P80C0**
value	*	*	*	*	*	**1**	**1**	**$**

register	P8DIR register (Address:0F241H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87DIR	P86DIR	P85DIR	P84DIR	P83DIR	**P82DIR**	**P81DIR**	**P80DIR**
value	*	*	*	*	*	**0**	**0**	**1**

As for P82D to P80D bit (P8D register:bits2 to 0), neither "0" nor "1" is problematic.

register	P8D register (Address:0F240H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87D	P86D	P85D	P84D	P83D	**P82D**	**P81D**	**P80D**
value	*	*	*	*	*	******	******	******

* : no relation to the SSIO0 function **: Don't care $: Optional

14.4.4 When operating the SSIO0 function in slave mode using P82 pin (SOUT1:output), P81 pin (SCK1:input/output), and P80 pin (SIN1:input).

SSIO is selected as the tertiary function of P82, P81, and P80 by setting P82MD1 to P80MD1 bit (P8MOD1 register: bits2 to 0) to "1" and setting P82MD0 to P80MD0 bit (P8MOD0 register: bits2 to 0) to "0". It is the same setup as the case of master mode.

register	P8MOD1 register (Address:0F245H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87MD1	P86MD1	P85MD1	P84MD1	P83MD1	**P82MD1**	**P81MD1**	**P80MD1**
value	*	*	*	*	*	**1**	**1**	**1**

register	P8MOD0 register (Address:0 F244H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87MD0	P86MD0	P85MD0	P84MD0	P83MD0	**P82MD0**	**P81MD0**	**P80MD0**
value	*	*	*	*	*	**0**	**0**	**0**

The state of the P82 pin is selected as CMOS output mode by setting P82C1 bit (P8CON1 register:bit2) to "1" , setting P82C0 bit (P8CON0 register:bit2) to "1" and setting P82DIR bit (P8DIR register:bit2) to "0". Additionally, the P81 and P80 pin is selected as input pin by setting P81DIR to P80DIR bit (P8DIR register: bits1 to 0) to "1"
The setting value of P81C1-P80C1 bit and P81C0 to P80C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P81 and P80 pin is connected.

register	P8CON1 register (Address:0F243H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87C1	P86C1	P85C1	P84C1	P83C1	**P82C1**	**P81C1**	**P80C1**
value	*	*	*	*	*	**1**	**$**	**$**

register	P8CON0 register (Address:0F242H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87C0	P86C0	P85C0	P84C0	P83C0	**P82C0**	**P81C0**	**P80C0**
value	*	*	*	*	*	**1**	**$**	**$**

register	P8DIR register (Address:0F241H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87DIR	P86DIR	P85DIR	P84DIR	P83DIR	**P82DIR**	**P81DIR**	**P80DIR**
value	*	*	*	*	*	**0**	**1**	**1**

As for P82D to P80D bit (P8D register:bits2 to 0), neither "0" nor "1" is problematic.

register	P8D register (Address:0F240H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	P87D	P86D	P85D	P84D	P83D	**P82D**	**P81D**	**P80D**
value	*	*	*	*	*	******	******	******

* : no relation to the SSIO0 function **: Don't care $: Optional

14.4.5 When operating the SSIO1 function in master mode using P86 pin (SOUT1:output), P85 pin (SCK1:input/output), and P84 pin (SIN1:input).

SSIO1 is selected as the tertiary function of P86, P85, and P84 by setting P86MD1 to P84MD1 bit (P8MOD1 register: bits6 to 4) to "1" and setting P86MD0 to P84MD0 bit (P8MOD0 register: bits6 to 4) to "0".

register	P8MOD1 register (Address:0F245H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87MD1	**P86MD1**	**P85MD1**	**P84MD1**	P83MD1	P82MD1	P81MD1	P80MD1
value	*	**1**	**1**	**1**	*	*	*	*

register	P8MOD0 register (Address:0 F244H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87MD0	**P86MD0**	**P85MD0**	**P84MD0**	P83MD0	P82MD0	P81MD0	P80MD0
value	*	**0**	**0**	**0**	*	*	*	*

The state of the P86 and P85 pin is selected as CMOS output mode by setting P86C1 to P85C1 bit (P8CON1 register:bits6 to 5) to "1" , setting P86C0 to P85C0 bit (P8CON0 register:bits6 to 5) to "1" and setting P86DIR to P85DIR bit (P8DIR register:bits6 to 5) to "0". Additionally, the P84 pin is selected as input pin by setting P84DIR bit (P8DIR register: bit4) to "1"
The setting value of P84C1 bit and P84C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the P84 pin is connected.

register	P8CON1 register (Address:0F243H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87C1	**P86C1**	**P85C1**	**P84C1**	P83C1	P82C1	P81C1	P80C1
value	*	**1**	**1**	**$**	*	*	*	*

register	P8CON0 register (Address:0F242H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87C0	**P86C0**	**P85C0**	**P84C0**	P83C0	P82C0	P81C0	P80C0
value	*	**1**	**1**	**$**	*	*	*	*

register	P8DIR register (Address:0F241H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87DIR	**P86DIR**	**P85DIR**	**P84DIR**	P83DIR	P82DIR	P81DIR	P80DIR
value	*	**0**	**0**	**1**	*	*	*	*

As for P86D to P84D bit (P8D register:bits6 to 4), neither "0" nor "1" is problematic.

register	P8D register (Address:0F240H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87D	**P86D**	**P85D**	**P84D**	P83D	P82D	P81D	P80D
value	*	******	******	******	*	*	*	*

* : no relation to the SSIO1 function **: Don't care $: Optional

14.4.6 When operating the SSIO1 function in slave mode using P86 pin (SOUT1:output), P85 pin (SCK1:input/output), and P84 pin (SIN1:input).

SSIO1 is selected as the tertiary function of P86, P85, and P84 by setting P86MD1 to P84MD1 bit (P8MOD1 register: bits6 to 4) to "1" and setting P86MD0 to P84MD0 bit (P8MOD0 register: bits6 to 4) to "0". It is the same setup as the case of master mode.

register	P8MOD1 register (Address:0F245H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87MD1	**P86MD1**	**P85MD1**	**P84MD1**	P83MD1	P82MD1	P81MD1	P80MD1
value	*	**1**	**1**	**1**	*	*	*	*

register	P8MOD0 register (Address:0 F244H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87MD0	**P86MD0**	**P85MD0**	**P84MD0**	P83MD0	P82MD0	P81MD0	P80MD0
value	*	**0**	**0**	**0**	*	*	*	*

The state of the P86 pin is selected as CMOS output mode by setting P86C1 bit (P8CON1 register:bit6) to "1" , setting P86C0 bit (P8CON0 register:bit6) to "1" and setting P86DIR bit (P8DIR register:bit6) to "0". Additionally, the P85 and P84 pin is selected as input pin by setting P85DIR to P84DIR bit (P8DIR register: bits5 to 4) to "1"
The setting value of P85C1 to P84C1 bit and P85C0 to P84C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P85 and P84 pin is connected.

register	P8CON1 register (Address:0F243H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87C1	**P86C1**	**P85C1**	**P84C1**	P83C1	P82C1	P81C1	P80C1
value	*	**1**	**$**	**$**	*	*	*	*

register	P8CON0 register (Address:0F242H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87C0	**P86C0**	**P85C0**	**P84C0**	P83C0	P82C0	P81C0	P80C0
value	*	**1**	**$**	**$**	*	*	*	*

register	P8DIR register (Address:0F241H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87DIR	**P86DIR**	**P85DIR**	**P84DIR**	P83DIR	P82DIR	P81DIR	P80DIR
value	*	**0**	**1**	**1**	*	*	*	*

As for P86D to P84D bit (P8D register:bits6 to 4), neither "0" nor "1" is problematic.

register	P8D register (Address:0F240H)							
bit	7	**6**	**5**	**4**	3	2	1	0
bit name	P87D	**P86D**	**P85D**	**P84D**	P83D	P82D	P81D	P80D
value	*	****	****	****	*	*	*	*

* : no relation to the SSIO1 function **: Don't care $: Optional

14.4.7 When operating the SSIO1 function in master mode using P42 pin (SOUT1:output), P41 pin (SCK1:input/output), and P40 pin (SIN1:input).

SSIO is selected as the secondary function of P42, P41, and P40 by setting P42MD1 to P40MD1 bit (P4MOD1 register: bits2 to 0) to "0" and setting P42MD0 to P40MD0 bit (P4MOD0 register: bits2 to 0) to "1".

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD1**	**P41MD1**	**P40MD1**
value	-	-	-	-	-	**0**	**0**	**0**

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD0**	**P41MD0**	**P40MD0**
value	-	-	-	-	-	**1**	**1**	**1**

The state of the P42 and P41 pin is selected as CMOS output mode by setting P42C1 to P41C1 bit (P4CON1 register:bits2 to 1) to "1" , setting P42C0 to P41C0 bit (P4CON0 register:bits2 to 1) to "1" and setting P42DIR to P41DIR bit (P4DIR register:bits2 to 1) to "0". Additionally, the P40 pin is selected as input pin by setting P40DIR bit (P4DIR register: bit0) to "1"
The setting value of P40C1 bit and P40C0 bit ($) is optional. Optional states are selected according to the state of the external circuit where the P40 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C1	**P42C1**	**P41C1**	**P40C1**
value	-	-	-	-	*	**1**	**1**	**$**

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C0	**P42C0**	**P41C0**	**P40C0**
value	-	-	-	-	*	**1**	**1**	**$**

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
value	-	-	-	-	*	**0**	**0**	**1**

As for P42D to P40D bit (P4D register:bits2 to 0), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43D	**P42D**	**P41D**	**P40D**
value	-	-	-	-	*	**	**	**

- : not existing * : no relation to the SSIO1 function **: Don't care $: Optional

14.4.8 When operating the SSIO1 function in slave mode using P42 pin (SOUT1:output), P41 pin (SCK1:input/output), and P40 pin (SIN1:input).

SSIO is selected as the secondary function of P42, P41, and P40 by setting P42MD1 to P40MD1 bit (P4MOD1 register: bits2 to 0) to "0" and setting P42MD0 to P40MD0 bit (P4MOD0 register: bits2 to 0) to "1". It is the same setup as the case of master mode.

register	P4MOD1 register (Address:0F225H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD1**	**P41MD1**	**P40MD1**
value	-	-	-	-	-	**0**	**0**	**0**

register	P4MOD0 register (Address:0F224H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	-	**P42MD0**	**P41MD0**	**P40MD0**
value	-	-	-	-	-	**1**	**1**	**1**

The state of the P42 pin is selected as CMOS output mode by setting P42C1 bit (P4CON1 register:bit2) to "1" , setting P42C0 bit (P4CON0 register:bit2) to "1" and setting P42DIR bit (P4DIR register:bit2) to "0". Additionally, the P41 and P40 pin is selected as input pin by setting P41DIR to P40DIR bit (P4DIR register: bits1 to 0) to "1"
The setting value of P41C1 to P40C1 bit and P41C0 to P40C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P41 and P40 pin is connected.

register	P4CON1 register (Address:0F223H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C1	**P42C1**	**P41C1**	**P40C1**
value	-	-	-	-	*	**1**	**$**	**$**

register	P4CON0 register (Address:0F222H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43C0	**P42C0**	**P41C0**	**P40C0**
value	-	-	-	-	*	**1**	**$**	**$**

register	P4DIR register (Address:0F221H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43DIR	**P42DIR**	**P41DIR**	**P40DIR**
value	-	-	-	-	*	**0**	**1**	**1**

As for P42D to P40D bit (P4D register:bits2 to 0), neither "0" nor "1" is problematic.

register	P4D register (Address:0F220H)							
bit	7	6	5	4	3	**2**	**1**	**0**
bit name	-	-	-	-	P43D	**P42D**	**P41D**	**P40D**
value	-	-	-	-	*	******	******	******

- : not existing * : no relation to the SSIO1 function **: Don't care $: Optional

Chapter 15

UART

15. UART

15.1 Overview

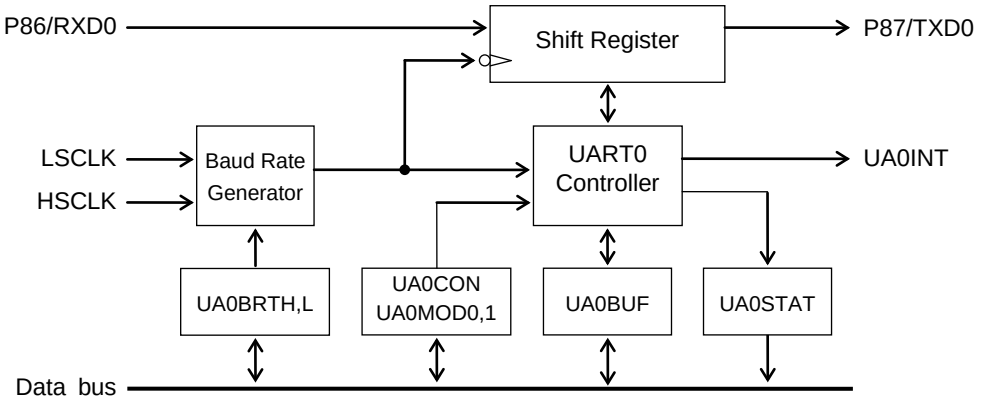
This LSI includes one channel of UART (Universal Asynchronous Receiver Transmitter) as UART0 which is an asynchronous serial interface of half-duplex communication.
For the input clock, see Chapter 3, "Clock Generation Circuit".
The use of UART0 requires setting of the secondary functions of Port 8. For setting of the secondary functions of Port 8, see Chapter 8, "Port 8".
The UART0 operates only when the DUA0 bit of the block control register 2 (BLKCON2) is "0". When the DUA0 bit are "1", every function of the UART0 is in a reset state.
For the block control registers, see Chapter 5, "MCU Control Function".

15.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable
- Odd parity, even parity, or no parity selectable
- 1 stop bit or 2 stop bits selectable
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic
- LSB first or MSB first selectable as a communication direction
- Communication speed: Settable within the range of 2400 bps to 115200 bps
- Built-in baud rate generator

15.1.2 Configuration

Figure 15-1 shows the configuration of the UART0.



UA0BUF:	UART0 transmit/receive buffer
UA0BRTH, L:	UART0 baud rate registers H, L
UA0CON:	UART0 control register
UA0MOD0, 1:	UART0 mode registers 0, 1
UA0STAT:	UART0 status register

Figure 15-1 Configuration of UART0

15.1.3 List of Pins

Pin name	I/O	Description
P86 / RXD0	I	UART0 data input pin Used for the secondary function of the P86 pin.
P87 / TXD0	O	UART0 data output pin Used for the secondary function of the P87 pin.

15.2 Description of Registers

15.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	¾	R/W	8	00H
0F291H	UART0 control register	UA0CON	¾	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	¾	R/W	8	00H

15.2.2 UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F290H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) to store the transmit/receive data of the UART.

In transmit mode (U0IO="0"), write the transmitted data to UA0BUF. To transmit data continuously, confirm the U0FUL bit of the UART0 status register (UA0STAT) becomes "0", then write the next transmitted data to UA0BUF. The UA0BUF is readable.

In receive mode (U0IO="1"), the received data is overwritten in UA0BUF in every reception completion. When the 5- to 7-bit data length is selected, unnecessary bits become "0". Writing to UA0BUF is invalid in the receive mode.

Note:
When using the transmit mode, select the transmit mode by setting "0" to U0IO bit of the UART0 mode register 0 (UA0MOD0), then set the transmit data to UA0BUF.

15.2.3 UART0 Control Register (UA0CON)

Address: 0F291H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	¾	¾	¾	¾	¾	¾	¾	U0EN
R/W	¾	¾	¾	¾	¾	¾	¾	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) to start/stop communication of the UART0.

[Description of Bits]

· **U0EN** (bit 0)

The U0EN bit is used to specify the UART0 communication operation start. In the transmit mode (U0IO="0"), transmission starts when writing the transmit data to the UART0 transmit/receive buffer (UA0BUF) and setting U0EN to "1". When the next transmission data is not written to UA0BUF and the transmission is completed, U0EN becomes "0" automatically. To terminate forcibly transmission/reception, set the U0EN bit to "0" by software.

In receive mode (U0IO="1"), the reception get enabled status when setting U0EN to "1". To terminate the reception, set the U0EN bit to "0" by the software.

U0EN	Description
0	Stop communication. (Initial value)
1	In transmit mode : Start communication In receive mode : Communication enabled

15.2.4 UART0 Mode Register 0 (UA0MOD0)

Address: 0F292H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	¾	¾	U0RSS	U0RSEL	¾	U0CK1	U0CK0	U0IO
R/W	¾	¾	R/W	R/W	¾	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) to set the transfer mode of the UART0.

[Description of Bits]

· **U0IO** (bit 0)
The U0IO bit is used to select transmit or receive mode.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

· **U0CK1, U0CK0** (bits 2, 1)
The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	Prohibited
1	*	HSCLK

· **U0RSEL** (bit 4)
The U0RSEL bit is used to select the receive data input pin for the UART0.

U0RSEL	Description
0	Selects the P86 pin. (Initial value)
1	Prohibited

· **U0RSS** (bit 5)
The U0RSS bit is used to select the receive data input sampling timing for the UART0.

U0RSS	Description
0	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 (Initial value)
1	Values-set-in-the-UA0BRTH-and-UA0BRTL-registers/2 - 1

Note:
Always set the UA0MOD0 register while communication is stopped, and do not rewrite it during communication.

15.2.5 UART0 Mode Register 1 (UA0MOD1)

Address: 0F293H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	¾	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	¾	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) to set the transfer mode of the UART0.

[Description of Bits]

· **U0LG1, U0LG0** (bits 1, 0)
The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART0.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

· **U0PT1, U0PT0** (bits 3, 2)
The U0PT1 and U0PT0 bits are used to select "even parity", odd parity", or "no parity" in the communication of the UART0.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

· **U0STP** (bit 4)
The U0STP bit is used to select the stop bit length in the communication of the UART0.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bits

· **U0NEG** (bit 5)
The U0NEG bit is used to select positive logic or negative logic in the communication of the UART0.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

· **U0DIR** (bit 6)
The U0DIR bit is used to select LSB first or MSB first in the communication of the UART0.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
Always set the UA0MOD1 register while communication is stopped, and do not rewrite it during communication.

15.2.6 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F294H
Access: R/W
Access size: 8/16 bits
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F295H
Access: R/W
Access size: 8 bits
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	¾	¾	¾	¾	U0BR11	U0BR10	U0BR9	U0BR8
R/W	¾	¾	¾	¾	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 15.3.2, "Baud Rate".

Note:
Always set the UA0BRTL and UA0BRTH registers while communication is stopped, and do not rewrite them during communication.

15.2.7 UART0 Status Register (UA0STAT)

Address: 0F296H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	¾	¾	¾	¾	U0FUL	U0PER	U0OER	U0FER
R/W	¾	¾	¾	¾	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART0. When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]

· **U0FER** (bit 0)
The U0FER bit is used to indicate occurrence of a framing error of the UART0.
When an error occurs in the start or stop bit, the U0FER bit is set to "1". This bit is updated each time reception is completed.
The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	Framing error

· **U0OER** (bit 1)
The U0OER bit is used to indicate occurrence of an overrun error of the UART0.
If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" unless the previous receive data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

· **U0PER** (bit 2)
The U0PER bit is used to indicate occurrence of a parity error of the UART0.
When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated after each reception is completed.
The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

· **U0FUL** (bit 3)
The U0FUL bit is used to indicate the state of the transmit/receive buffer of the UART0.
When transmit data is written in UA0BUF in transmit mode, this bit is set to "1" and when transmit data is transferred to the shift register, this bit is set to "0". To transmit data consecutively, write the next transmit data to UA0BUF after checking that the U0FUL flag has been set to "0".
The U0FUL bit is fixed to "0" in receive mode.

U0FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

15.3 Description of Operation

15.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and for the transfer direction, "LSB first" or "MSB first" are available for selection. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UART0 mode register 1 (UA0MOD1).
Figure 15-2 and Figure 15-3 show the positive logic input/output format and negative logic input/output format, respectively.

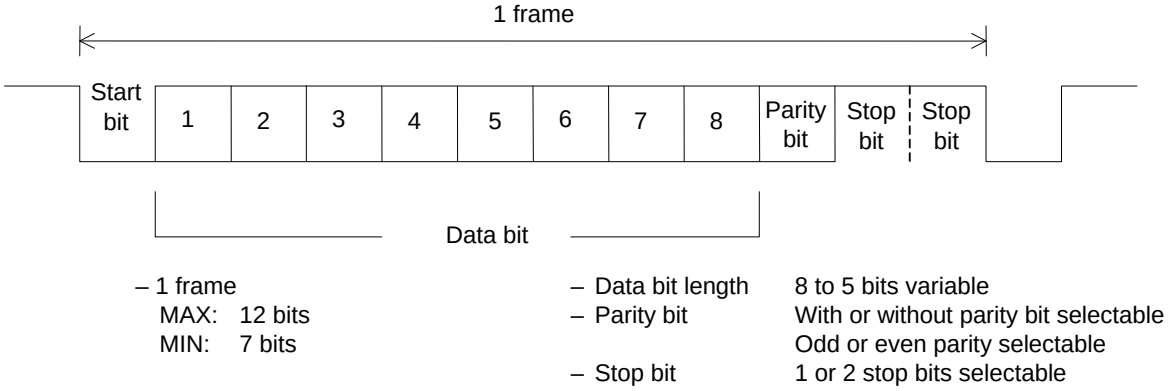


Figure 15-2 Positive Logic Input/Output Format

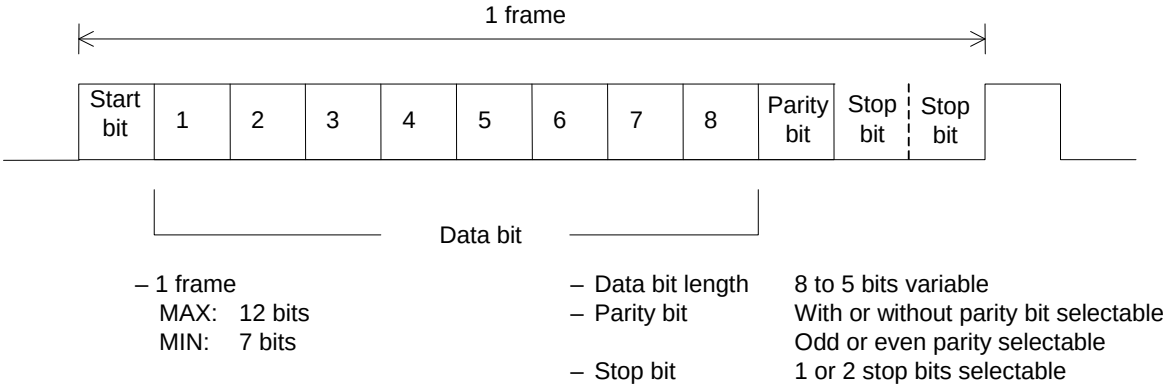


Figure 15-3 Negative Logic Input/Output Format

15.3.2 Baud Rate

Baud rates are generated by the baud generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (U0CK1, U0CK0) of the UART0 mode register 0 (UA0MOD0). The count value of the baud rate generator can be set by writing it in the UART0 baud rate register H or L (UA0BRTH, UA0BRTL). The maximum count is 4096.
The setting values of UA0BRTH and UA0BRTL are expressed by the following equation.

$$\text{UA0BRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 15-1 lists the count values for typical baud rates.

Table 15-1 Count Values for Typical Baud Rates

Baud rate	Baud rate generator clock selection	Count value of the baud rate generator				Error
	Baud rate clock	Count value	Period of 1 bit	UAnBRTH	UAnBRTL	
2400 bps	8.192MHz	3413	Approx. 417 ms	0DH	054H	0.01%
4800 bps		1707	Approx. 208 ms	06H	0AAH	-0.02%
9600 bps		853	Approx. 104 ms	03H	054H	0.04%
19200 bps		427	Approx. 52 ms	01H	0AAH	-0.08%
38400 bps		213	Approx. 26 ms	00H	0D4H	0.16%
57600 bps		142	Approx. 17.4 ms	00H	08DH	0.16%
115200 bps		71	Approx. 8.7 ms	00H	046H	0.16%

15.3.3 Transmit Data Direction

Figure 15-4 shows the relationship between the transmit/receive buffer and the transmit/receive data.

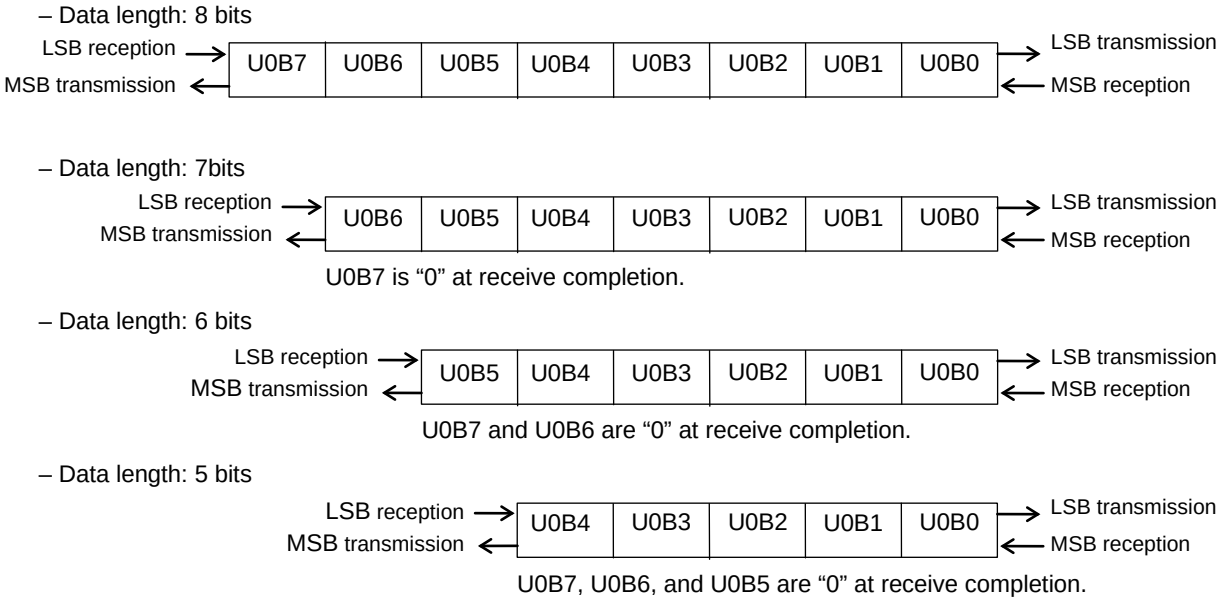


Figure 15-4 Relationship between Transmit/Receive Buffer and Transmit/Receive Data

Note:
When the TXD0 pin is set to serve the secondary function output in receive mode, "H" level is output from the TXD0 pin.

15.3.4 Transmit Operation

Transmission is started by setting the U0IO bit of the UART0 mode register 0 (UA0MOD0) to "0" to select transmit mode and setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 15-5 shows the operation timing for transmission.

When the transmit data is written in the UART0 transmit/receive buffer (UA0BUF), the U0FUL bit which indicates the state of the transmit/receive buffer of the UART0 status register (UA0STAT) becomes "1". Then, when the U0EN bit of UART0 control register (UA0CON) is set to "1" (j), the baud rate generator generates an internal transfer clock based on the setting baud rate, and starts the transmission.
When the transmission is started, the start bit is outputted to the TXD0 pin at the falling edge of the internal transfer clock (k), UART0 interrupt (UA0INT) is requested at the same time, then U0FUL bit of UA0STAT becomes "0".

In the UART0 interrupt routine, when the next transmission data is written in UART0 transmit/receive buffer (UA0BUF), U0FUL bit of UA0STAT is set to "1"(l).
Then, the transmit data, the parity bit and stop bit are outputted. The UART0 interrupt is requested at the falling edge(m) of the internal transfer clock after transmit of the stop bit. Then, when the stop bit is outputted in the state which the next transmit data is not written in UA0BUF (U0FUL bit is "0") (n), stop the transmission, U0EN-bit is reset to "0" and the UART0 interrupt is requested.

The valid period for the next transmit data to be written to the transmit/receive buffer (UA0BUF) is from the generation of an interrupt request (m) to the completion of stop bit transmission(n)(o).

Note:
Always start the transmission by setting the U0EN bit of the UART0 control register (UA0CON) to "1" after setting the transmit data to the UART0 transmit/receive buffer (UA0BUF) (U0FUL of UA0STAT is "1"). When the transmit data is not written to UA0BUF (U0FUL of UA0STAT is "0") and U0EN bit is set to "1", UART0 interrupt request is generated. However U0EN bit becomes "0" immediately and the transmission does not start.

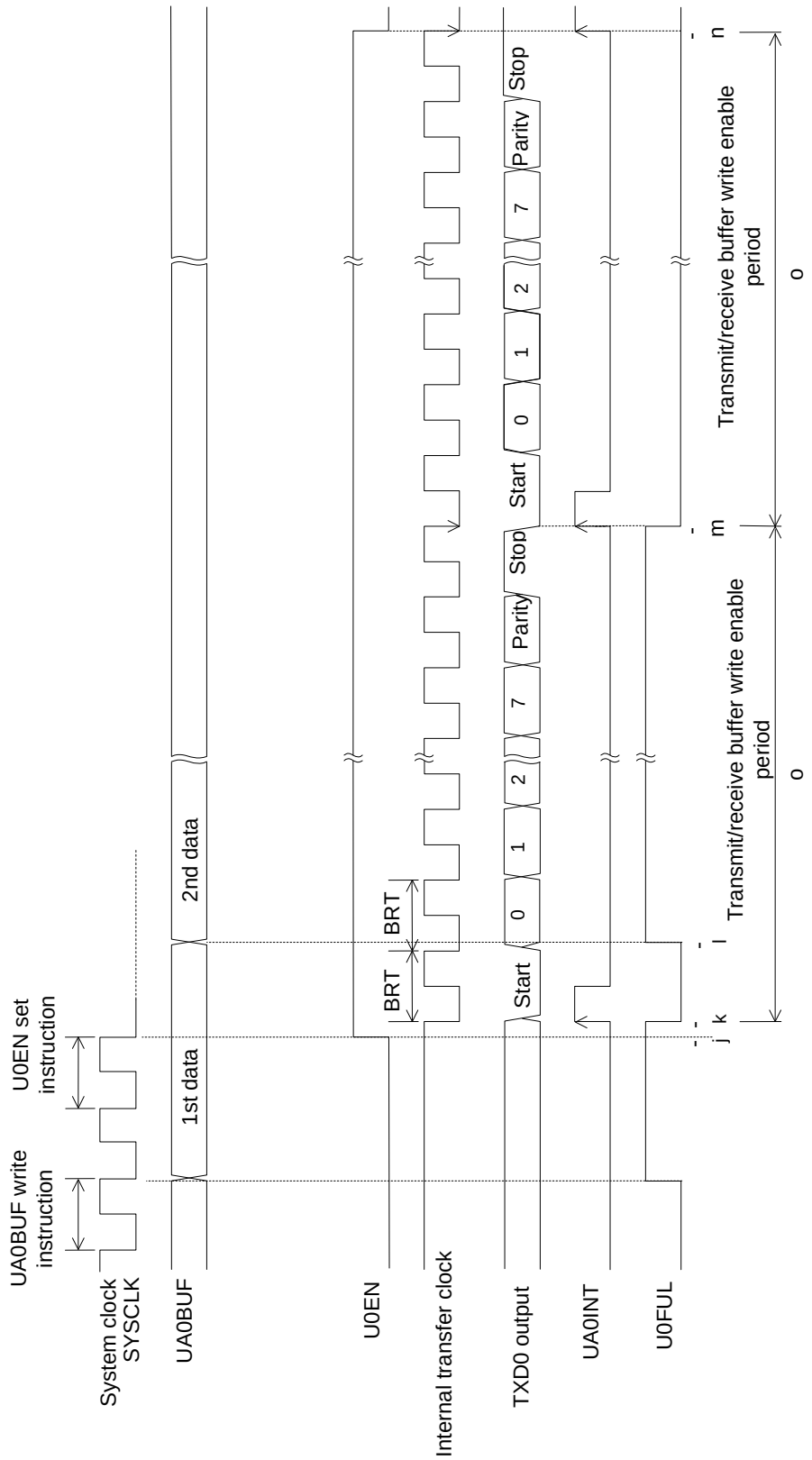


Figure 15-5 Operation Timing in Transmission

15.3.5 Receive Operation

Reception is started by selecting a receive data input pin using the U0RSEL bit of the UART0 mode register 0 (UA0MOD0), then setting the U0IO bit of UA0MOD0 to "1" to select receive mode, and then setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 15-6 shows the operation timing for reception.

When receive operation is enabled, the LSI checks the data sent to the input pin RXD0 and waits for the arrival of a start bit.
When detecting a start bit (k), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD0 on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the transmit/receive buffer (UA0BUF) concurrently with the falling edge of the internal transfer clock of l.
The LSI requests a UART0 interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (m) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UART0 status register (UA0STAT) to "1".

Parity error	: U0PER ="1"
Overrun error	: U0OER ="1"
Framing error	: U0FER ="1"

As shown in Figure 15-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the U0EN bit is reset to "0" by the software. When the U0EN bit is reset to "0" during reception, the received data may be destroyed. When the U0EN bit is reset to "0" during the "U0EN reset enable period" in Figure 15-6, the received data is protected.

Note:
U0OER becomes "1" when the next received data is overwritten before the reception data of the UART0 transmit/receive buffer (UA0BUF) is read. When the reception stops/restarts by U0EN bit, U0OER becomes "1" if the last received data (UA0BUF) is not read. Therefore, always read the UA0BUF even if the received data is unnecessary when the reception completed.

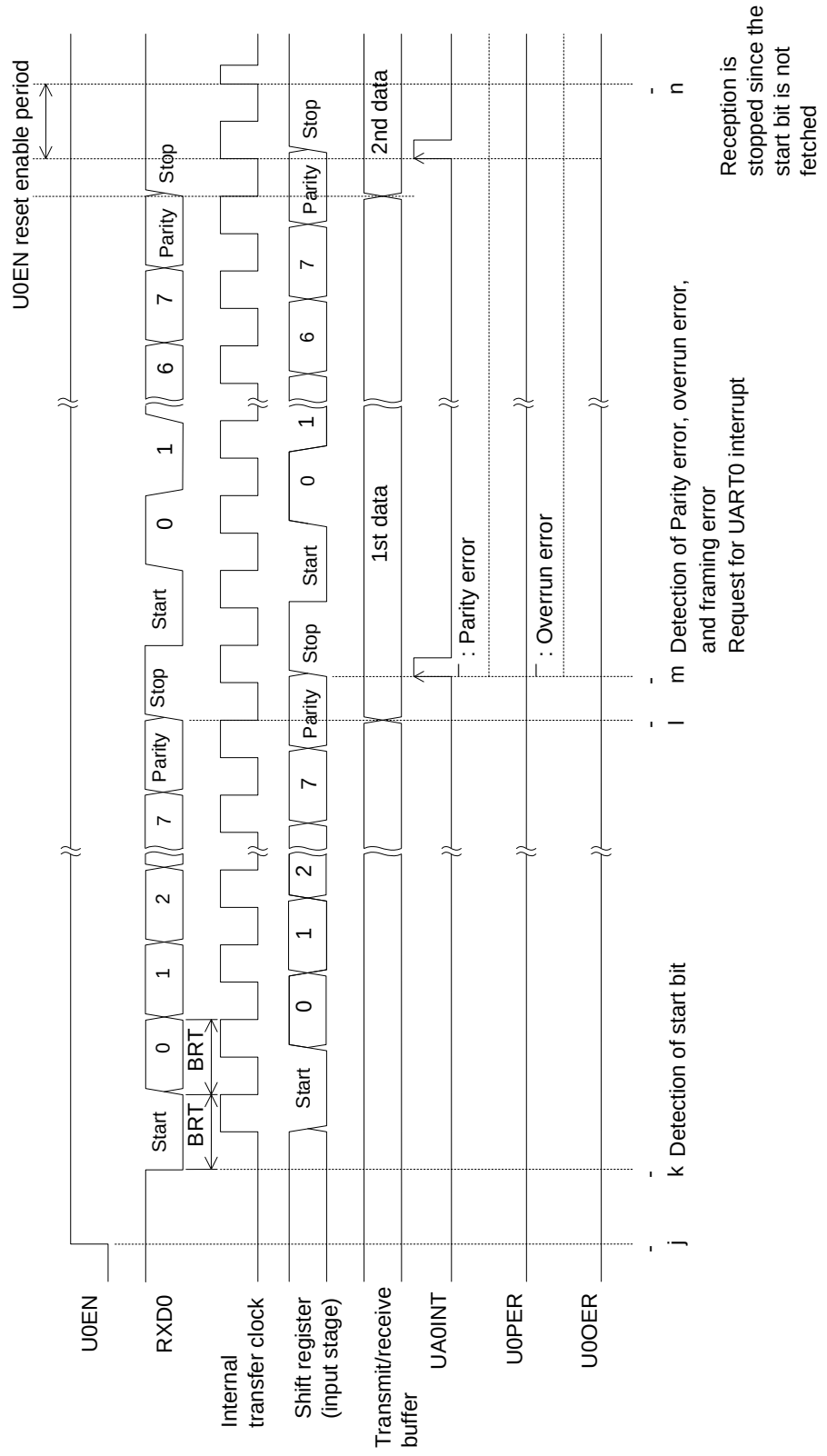


Figure 15-6 Operation Timing in Reception

15.3.5.1 Detection of Start bit

The start bit is sampled with the baud rate generator clock (LSCLK, HSCLK) which is selected by U0CK1, U0CK0 bits of UART0 mode register 0 (UA0MOD0). Therefore, there is a possibility that the start bit will be detected with a delay of a maximum of one cycle of the baud rate generator clock.
Figure 15-7 shows the start bit detection timing.

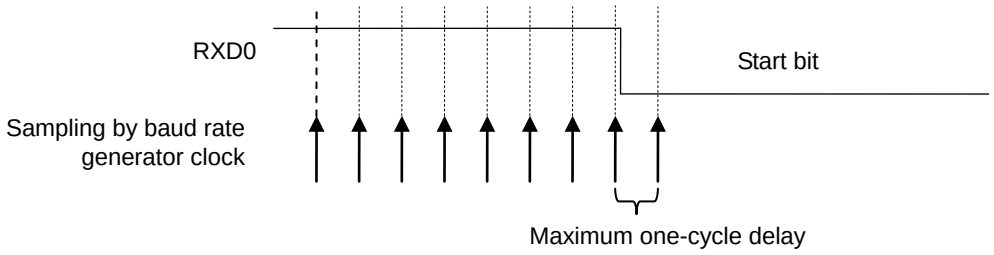
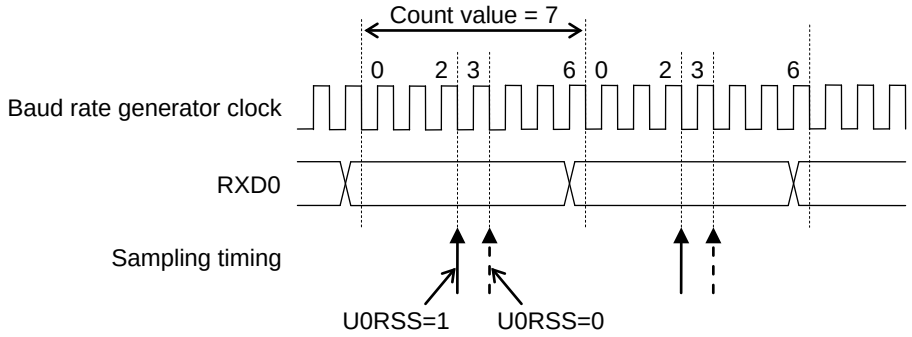


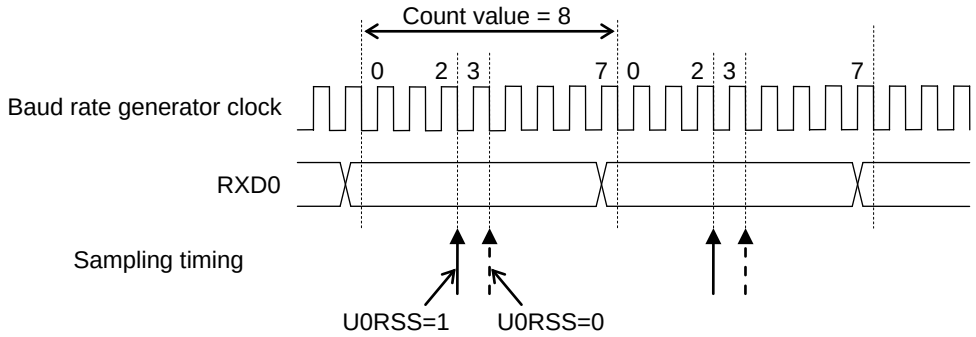
Figure 15-7 Start Bit Detection Timing (Positive Logic)

15.3.5.2 Sampling Timing

When the start bit is detected, the receive data that has been input to RXD0 is sampled roughly at the middle of the baud rate and shifted into the shift register.
This sampling timing, where the receive data is sampled to be shifted into the shift register, can be adjusted by one clock pulse of the baud rate generator clock by using the U0RSS bit of the UART0 mode register 0 (UA0MOD0). Figure 15-8 shows the relationship between the U0RSS bit and sampling timing.



(1) When the baud rate generator count value is "7" (odd number)



(2) When the baud rate generator count value is "8" (even number)

Figure 15-8 Relationship between U0RSS Bit and Sampling Timing

15.3.5.3 Reception Margin

If there are any errors between the baud rate on the transmitter side and the baud rate to be generated by the baud rate generator of the LSI, those errors will be accumulated until the last stop bit in one frame is shifted in, causing the reception margin to be reduced.
Figure 15-9 shows the waveform indicating baud rate errors and reception margin.

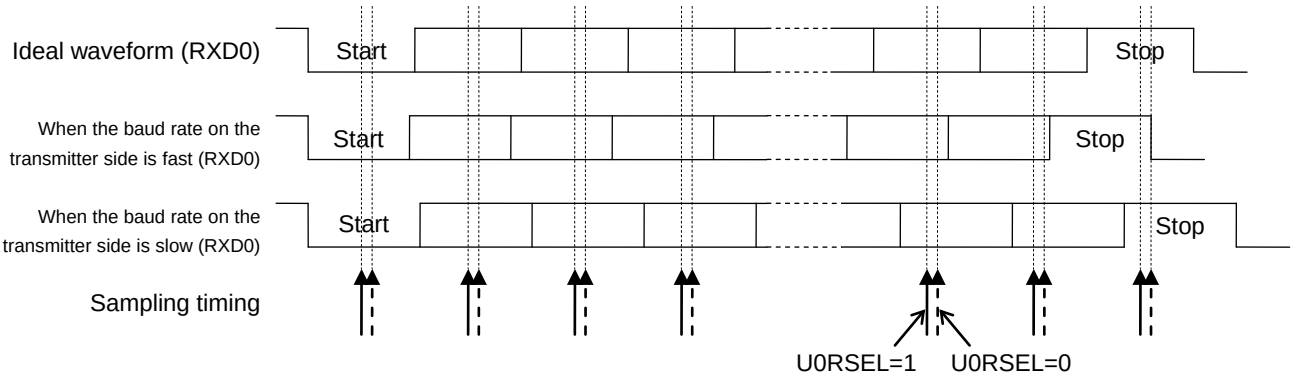


Figure 15-9 Baud Rate Errors and Reception Margin

Note:
When doing system design, ensure enough reception margin taking into account the effects of noise and receive data rounding as well as the difference in baud rate between the transmitter side and receiver side and a delay in the detection of start bit.

15.4 Register setup of the port

For operate the UART0 function, each related port register needs to be set up. Refer to the Chapter 8, "Port 8" for details of each register.

15.4.1 When operating the UART0 function using P87 pin (TXD0:output) and P86 pin (RDX0:input)

The UART0 is selected as the secondary function of the P87 pin and the P86 pin by setting P87MD1 to P86MD1 bit (P8MOD1 register: bits7 to 6) to "0" and setting P87MD0 to P86MD0 bit (P8MOD0 register: bits7 to 6) to "1".

register	P8MOD1 register (Address:0F245H)							
bit	**7**	**6**	5	4	3	2	1	0
bit name	**P87MD1**	**P86MD1**	-	-	-	-	-	-
value	**0**	**0**	-	-	-	-	-	-

register	P8MOD0 register (Address:0F244H)							
bit	**7**	**6**	5	4	3	2	1	0
bit name	**P87MD0**	**P86MD0**	-	-	-	-	-	-
value	**1**	**1**	-	-	-	-	-	-

The state of the P87 pin is selected as CMOS output mode by setting P87C1 bit (P8CON1 register:bit7) to "1", setting P87C0 bit (P8CON0 register:bit7) to "1" and setting P87DIR bit (P8DIR register:bit7) to "0". The P86 pin is selected as input pin by setting P86DIR bit (P8DIR register: bit6) to "1".
The setting value of P86C1 bit and P86C0 bit ($) is optional. Optional input modes are selected according to the state of the external circuit where the P86 pin is connected.

register	P8CON1 register (Address:0F243H)							
bit	**7**	**6**	5	4	3	2	1	0
bit name	**P87C1**	**P86C1**	-	-	-	-	-	-
value	**1**	**$**	-	-	-	-	-	-

register	P8CON0 register (Address:0F242H)							
bit	**7**	**6**	5	4	3	2	1	0
bit name	**P87C0**	**P86C0**	-	-	-	-	-	-
value	**1**	**$**	-	-	-	-	-	-

register	P8DIR register (Address:0F241H)							
bit	**7**	**6**	5	4	3	2	1	0
bit name	**P87DIR**	**P86DIR**	-	-	-	-	-	-
value	**0**	**1**	-	-	-	-	-	-

As for P87D to P86D bit (P8D register:bits7 to 6), neither "0" nor "1" is problematic.

register	P8D register (Address:0F240H)							
bit	**7**	**6**	5	4	3	2	1	0
bit name	**P87D**	**P86D**	-	-	-	-	-	-
value	******	******	-	-	-	-	-	-

* : no relation to the UART0 function **: Don't care $: Optional

Chapter 16

I^2C Bus Interface (Master)

16. I²C Bus Interface (Master)

16.1 Overview

This LSI includes 1 channel of I²C bus interface (master).
The secondary functions of Port 8 are assigned to the I²C bus interface data input/output pin and the I²C bus interface clock input/output pin. For Port8, see Chapter 8, "Port 8".

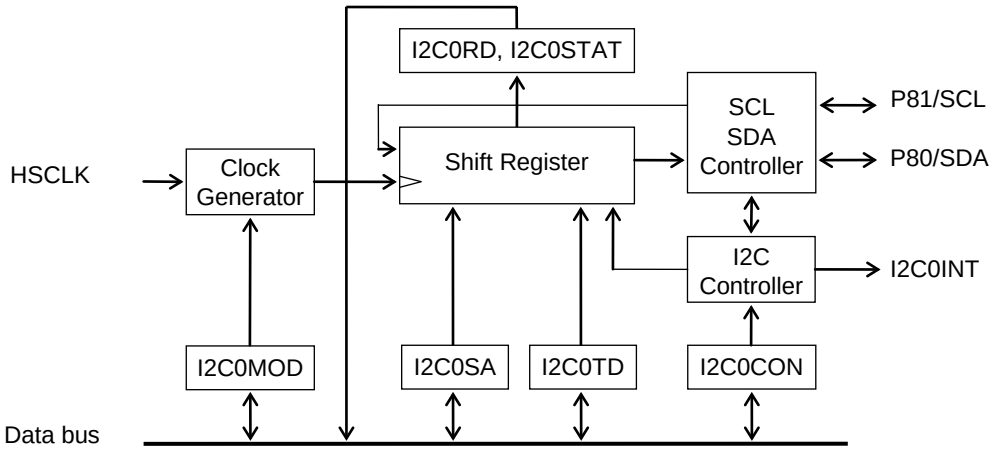
16.1.1 Features

- Master function
- Communication speeds supported include standard mode (100 kbps) and fast mode (400kbps).
- 7-bit address format (10-bit address can be supported)

Notes:
- This LSI does not support arbitration function (multi-master) and clock synchronization (handshake).
- Set HSCLK to 4.096MHz or 8.192MHz. At other frequencies, the communication speed is not 100kbps/400kbps.

16.1.2 Configuration

Figure 16-1 shows the configuration of the I²C bus interface.



I2C0RD : I²C bus 0 receive register
I2C0SA : I²C bus 0 slave address register
I2C0TD : I²C bus 0 transmit data register
I2C0CON : I²C bus 0 control register
I2C0MOD : I²C bus 0 mode register
I2C0STAT : I²C bus 0 status register

Figure 16-1 Configuration of I²C Bus Interface

16.1.3 List of Pins

Pin name	I/O	Description
P80/SDA	I/O	I^2C bus interface data input/output pin. Used for the secondary function of the P80 pin.
P81/SCL	I/O	I^2C bus interface clock input/output pin. Used for the secondary function of the P81 pin.

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2A0H	I^2C bus 0 receive register	I2C0RD	—	R	8	00H
0F2A1H	I^2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I^2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I^2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I^2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I^2C bus 0 status register	I2C0STAT	—	R	8	00H

16.2.2 I2C Bus 0 Receive Register (I2C0RD)

Address: 0F2A0H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0RD	I20R7	I20R6	I20R5	I20R4	I20R3	I20R2	I20R1	I20R0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C0RD is a read-only special function register (SFR) to store receive data.
I2C0RD is updated after completion of each reception.

[Description of Bits]

· **I20R7 to I20R0** (bits 7 to 0)
The I20R7 to I20R0 bits are used to store received data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since the SDA pin signal is received in synchronization with the rising edge of the SCL pin signal during slave address data transmission and data transmission in addition to data reception, it is possible to confirm whether the transmitted data has been reliably transmitted.

16.2.3 I2C Bus 0 Slave Address Register (I2C0SA)

Address: 0F2A1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0SA	I20A6	I20A5	I20A4	I20A3	I20A2	I20A1	I20A0	I20RW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0SA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

[Description of Bits]

· **I20RW** (bit 0)
The I20RW bit is used to select the data transmit mode (write) or data receive mode (read).

I20RW	Description
0	Data transmit mode (initial value)
1	Data receive mode

· **I20A6 to I20A0** (bits 7 to 1)
The I20A6 to I20A0 bits are used to set the address of the communication destination.

16.2.4 I2C Bus 0 Transmit Data Register (I2C0TD)

Address: 0F2A2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0TD	I20T7	I20T6	I20T5	I20T4	I20T3	I20T2	I20T1	I20T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0TD is a special function register (SFR) to set transmit data.

[Description of Bits]

· **I20T7 to I20T0** (bits 7 to 0)
The I20T7 to I20T0 bits are used to set transmit data.

16.2.5 I²C Bus 0 Control Register (I2C0CON)

Address: 0F2A3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0CON	I20ACT	—	—	—	—	I20RS	I20SP	I20ST
R/W	R/W	—	—	—	—	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

· **I20ST** (bit 0)
The I20ST bit is used to control the communication operation of the I²C bus interface. When the I20ST bit is set to "1", communication starts. When "1" is overwritten to the I20ST bit in a control register setting wait state after transmission/reception of acknowledgment, communication starts again. When the I20ST bit is set to "0", communication is stopped forcibly.
The I20ST bit can be set to "1" only when the I²C bus interface is in an operation enable state (I20EN = "1").
When the I20SP bit is set to "1", the I20ST bit is set to "0".

I20ST	Description
0	Stops communication (initial value)
1	Starts communication

· **I20SP** (bit 1)
The I20SP bit is a write-only bit used to request a stop condition. When the I20SP bit is set to "1", the I²C bus shifts to the stop condition and communication stops. When the I20SP bit is read, "0" is always read.

I20SP	Description
0	No stop condition request (initial value)
1	Stop condition request

· **I20RS** (bit 2)
The I20RS bit is a write-only bit used to request a repeated start. When this bit is set to "1" during data communication, the I²C bus shifts to the repeated start condition and communication restarts from the slave address. I20RS can be set to "1" only while communication is active (I20ST ="1"). When the I20RS bit is read, "0" is always read.

I20RS	Description
0	No repeated start request (initial value)
1	Repeated start request

· **I20ACT** (bit 7)
The I20ACT bit is used to set the acknowledge signal to be output at completion of reception.

I20ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

16.2.6 I²C Bus 0 Mode Register (I2C0MOD)

Address: 0F2A4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0MOD	—	—	—	I20SYN	I20DW1	I20DW0	I20MD	I20EN
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C0MOD is a special function register (SFR) to set operating mode.

[Description of Bits]

· **I20EN** (bit 0)
The I20EN bit is used to enable the operation of the I²C bus interface. Only when the I20EN bit is set to "1", the I20ST bit can be set and the I20BB flag starts operation. When the I20EN bit is set to "0", all the SFRs related to the I²C bus 0 are initialized.

I20EN	Description
0	Stops I²C operation. (Initial value)
1	Enables I²C operation.

· **I20MD** (bit 1)
The I20MD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected.

I20MD	Description
0	Standard mode (initial value)/ 100kbps
1	Fast mode / 400kbps

· **I20DW1, I20DW0** (bits 3, 2)
The I20DW1 and I20DW0 bits are used to set the communication speed reduction rate of the I²C bus interface. Set this bit so that the communication speed does not exceed 100kpbs/400kpbs.

I20DW1	I20DW0	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

· **I20SYN** (bit 4)
The I20SYN bit is used to select whether or not to use the clock synchronization function (handshake function). This LSI does not support the clock synchronization function or multi-master. Please always set the bit to "0".

I20SYN	Description
0	Clock synchronization is not used. (Initial value)
1	Prohibited

Note:
The I²C bus is set so that the communication speed may become 100kbps/400kbps when HSCLK is 4.096 MHz or 8.192MHz. The operation cannot be guaranteed if this register value is changed during I²C communication.

16.2.7 I2C Bus 0 Status Register (I2C0STAT)

Address: 0F2A5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C0STAT	—	—	—	—	—	I20ER	I20ACR	I20BB
R/W	—	—	—	—	—	R	R	R
Initial value:	0	0	0	0	0	0	0	0

I2C0STAT is a read-only special function register (SFR) to indicate the state of the I2C bus interface.

[Description of Bits]

· I20BB (bit 0)
The I20BB bit is used to indicate the state of use of the I2C bus interface. When the start condition is generated on the I2C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". The I20BB bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20BB	Description
0	I2C bus-free state (Initial value)
1	I2C bus-busy state

· **I20ACR** (bit 1)
The I20ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I20ACR bit is set to "0" when the I20EN bit of I2C0MOD is "0".

I20ACR	Description
0	Receives acknowledgment "0". (Initial value)
1	Receives acknowledgment "1".

· **I20ER** (bit 2)
The I20ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". The SDA pin remains the output until the subsequent byte data communication terminates even if I20ER is set to "1".
The I20ER bit is set to "0" when a write operation to I2C0CON is performed. The I20ER bit is set to "0" when the I20EN bit of I2C0MOD is set to "0".

I20ER	Description
0	No transmit error (initial value)
1	Transmit error

16.3 Description of Operation

16.3.1 Communication Operating Mode

Communication is started by start condition when communication mode is selected by using the I²C bus 0 mode register (I2C0MOD), the I²C function is enabled by using the I20EN bit, a slave address and a data communication direction are set in the I²C bus 0 slave address register, and "1" is written to the I20ST bit of the I²C bus 0 control register (I2C0CON).

16.3.1.1 Start Condition

When "1" is written to the I20ST bit of the I²C bus 0 control register ((I2C0CON) while communication is stopped (the I20ST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to slave address transmit mode.

16.3.1.2 Repeated Start Condition

When "1" is written to the I20RS and I20ST bits of the I²C bus 0 control register ((I2C0CON) during communication (the I20ST bit is "0"), the repeated start condition waveform is output to the SDA and SCL pins.
After execution of the repeated start condition, the LSI shifts to slave address transmit mode.

16.3.1.3 Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I²C bus 0 slave address register (I2C0SA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0SA output from the SDA pin is stored in I2C0RD.

16.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C0TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The value of I2C0TD output from the SDA pin is stored in I2C0RD.

16.3.1.5 Data Receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I20ACT bit of the I²C bus 0 control register (I2C0CON) is output as an acknowledge signal. At completion of acknowledgment transmission, the LSI shifts to the I²C bus 0 control register (I2C0CON) setting wait state (control register setting wait state).
The data received is stored in I2C0RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I20ACR bit of the I²C bus 0 status register (I2CSTAT).

16.3.1.6 Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I²C bus interface interrupt (I2C0INT) is generated.
In the control register setting wait state, the transmit flag (I20ER) of the I²C bus 0 status register (I2C0STAT) and acknowledgment receive data (I20ACR) are confirmed, and at data reception, the contents of I2C0RD are read in the CPU and the next operation mode is selected.
When "1" is written to the I20ST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I20SP bit, the LSI shifts to the stop condition. When "1" is written to the I20RS bit and I20ST bit, the operation shifts to the repeated start condition.

16.3.1.7 Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I²C bus interface interrupt (I2C0INT) is generated.

16.3.2 Communication Operation Timing

Figures 16-2 to 16-4 show the operation timing and control method for each communication mode.

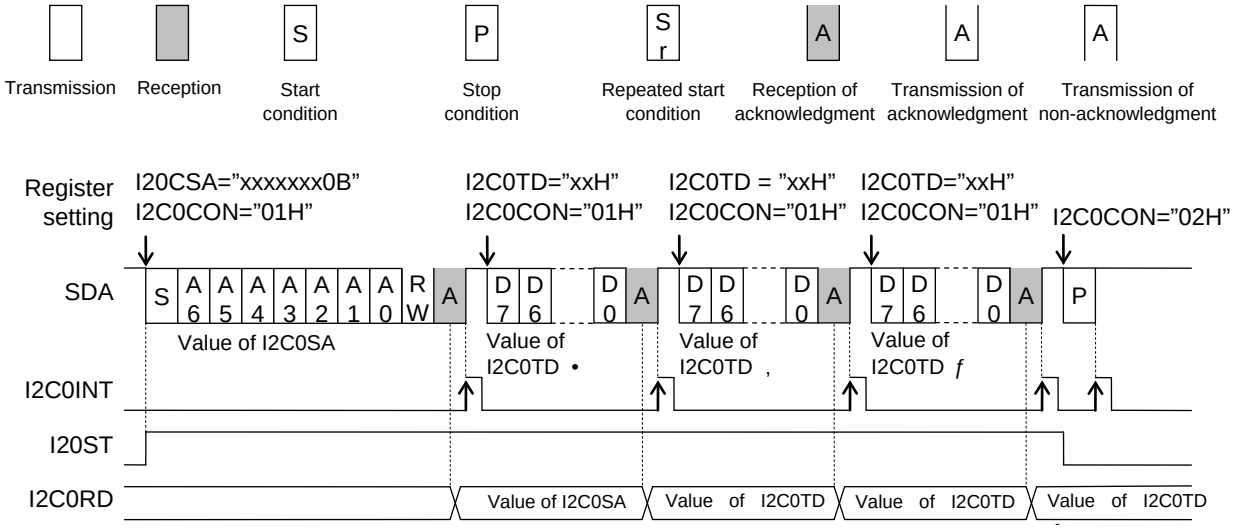


Figure 16-2 Operation Timing in Data Transmit (Write)

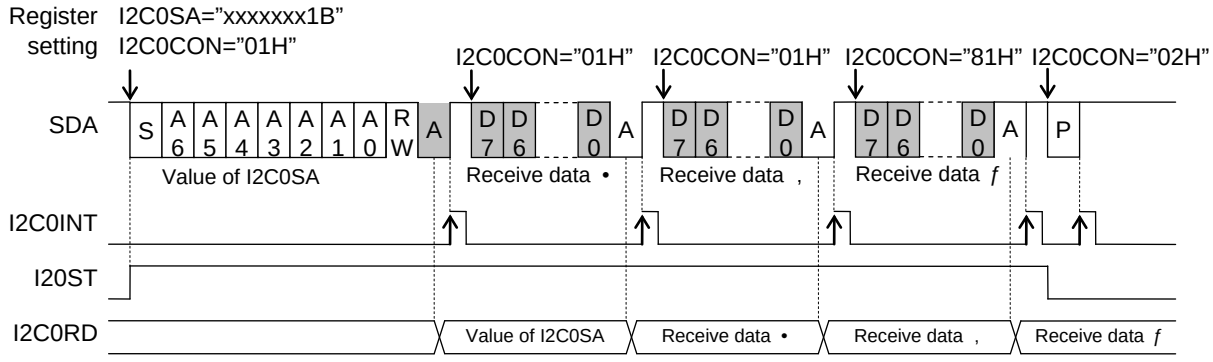


Figure 16-3 Operation Timing in Data Receive (Read)

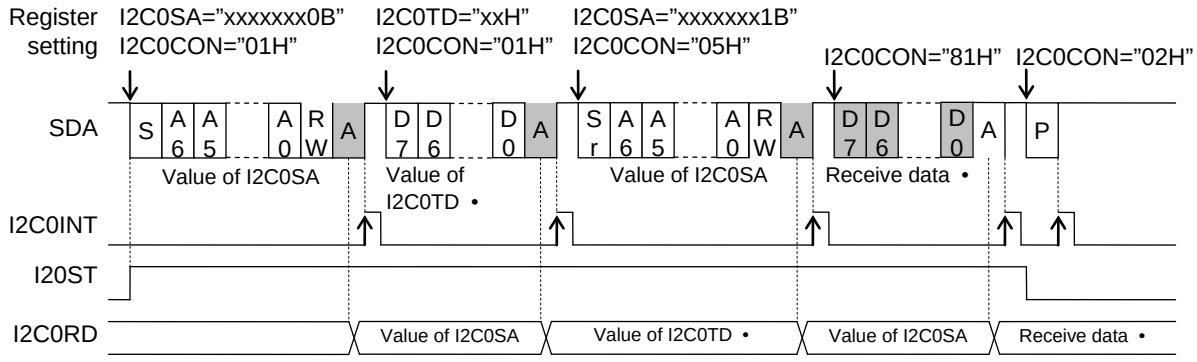


Figure 16-4 Operation Timing at Data Transmit/Receive (Write/Read) Switching

Figure 16-5 shows the operation timing and control method when an acknowledgment error occurs.

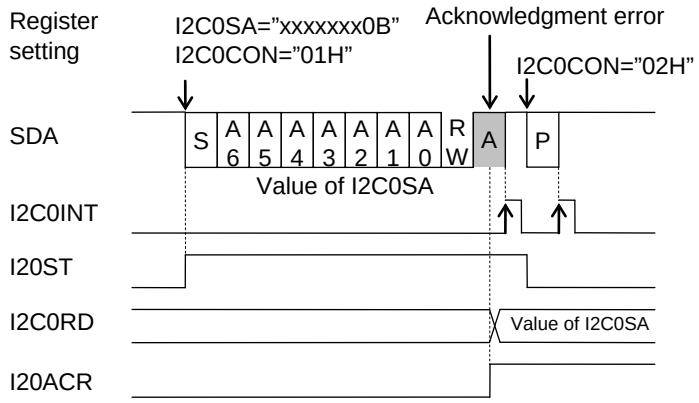


Figure 16-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide, the I20ER bit of the I²C bus 0 status register (I2C0STAT) is set to "1" and SDA pin output is prohibited until termination of the subsequent byte data communication. I20ER bit is initialized to "0" by writing I²C Bus 0 Control Register (I2C0CON).
Figure 16-6 shows the operation timing and control method when transmission fails.

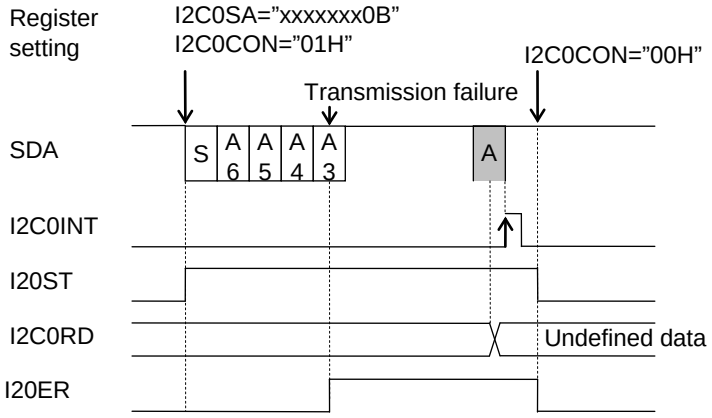


Figure 16-6 Operation Timing When Transmission Fails

16.3.3 Operation Waveforms

Figure 16-7 shows the operation waveforms of the SDA and SCL signals and the I20BB flag. Table 16-1 shows the relationship between communication speeds and HSCLK clock counts.

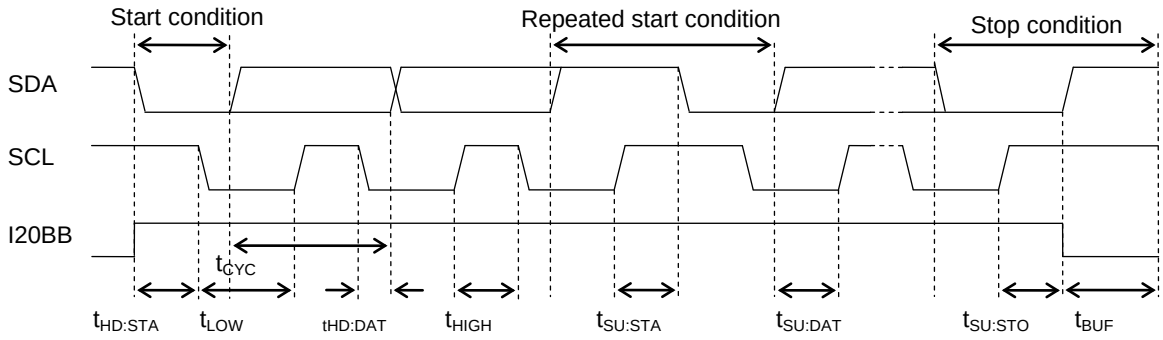


Figure 16-7 Operation Waveforms of SDA and SCL Signals and I20BB Flag

Table 16-1 Relationship between Communication Speeds and HSCLK Clock Counts

Communication speed (I20SP)	Speed reduction (I20DW1, 0)	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100 kbps	No reduction	80f	36f	44f	8f	36f	44f	36f	36f	44f
	10% reduction	88f	40f	48f	8f	40f	48f	40f	40f	48f
	20% reduction	96f	44f	52f	8f	44f	52f	44f	44f	52f
	30% reduction	104f	48f	56f	8f	48f	56f	48f	48f	56f
Fast mode 400 kbps	No reduction	20f	8f	12f	4f	8f	12f	8f	8f	12f
	10% reduction	22f	8f	14f	4f	8f	14f	10f	8f	14f
	20% reduction	24f	10f	14f	4f	10f	14f	10f	10f	14f
	30% reduction	26f	10f	16f	4f	10f	16f	12f	10f	16f

f : Period of high-speed clock (HSCLK)

Note:
The HSCLK clock count is set so that the communication speed may be set to 100kbps/400kbps when HSCLK is 4.096 MHz or 8.192MHz. When the high-speed clock frequency is not 4.096MHz or 8.192MHz, select an I2C0MOD communication speed reduction rate and an FCON0 HSCLK frequency so that the communication speed may not exceed 100kbps/400kbps.

16.4 Specifying Port Registers

To enable the I²C function, the applicable bit of each related port register needs to be set. See Chapter 8, "Port 8" for detail about the port registers.

Note:
Operation cannot be guaranteed if more than one port is set for one channel.

16.4.1 Functioning P81(SCL:output) and P80(SDA:input/output) as the I²C

Set P81MD1 to P80MD1 bit (bit1-bit0 of P8MOD1 register) to "0", and P81MD0 to P80MD0 bit (bit1 to bit0 of P4MOD0 register) to "1", for specifying the I²C as the secondary function of P81 and P80.

Reg. name	P8MOD1 register (Address: 0F245H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87MD1	P86MD1	P85MD1	P84MD1	P83MD1	P82MD1	**P81MD1**	**P80MD1**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P8MOD0 register (Address: 0F244H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87MD0	P86MD0	P85MD0	P84MD0	P83MD0	P82MD0	**P81MD0**	**P80MD0**
Data	*	*	*	*	*	*	**1**	**1**

Set P81C1 to P80C1 bit(bits1 to 0 of P8CON1 register) to "1", set P81C0 to P80C0 bit(bits1 to 0 of P8CON0 register) to "0", and set P81DIR to P80DIR bit(bits1 to 0 of P8DIR register) to "0", for specifying the P81 and P80 as Nch open-drain output. The pulled-up open-drain/open-collector outputs are required on the I²C bus line to avoid collision between H level and L level.

Reg. name	P8CON1 register (Address: 0F243H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87C1	P86C1	P85C1	P84C1	P83C1	P82C1	**P81C1**	**P80C1**
Data	*	*	*	*	*	*	**1**	**1**

Reg. name	P8CON0 register (Address: 0F242H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87C0	P86C0	P85C0	P84C0	P83C0	P82C0	**P81C0**	**P80C0**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P8DIR register (Address: 0F241H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87DIR	P86DIR	P85DIR	P84DIR	P83DIR	P82DIR	**P81DIR**	**P80DIR**
Data	*	*	*	*	*	*	**0**	**0**

Data of P81D to P80D bits (bits1 to 0 of P8D register) do not affect to the I²C function, so don't care the data for the function.

Reg. name	P8D register (Address: 0F240H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87D	P86D	P85D	P84D	P83D	P82D	**P81D**	**P80D**
Data	*	*	*	*	*	*	******	******

* : Bit not related to the I²C bus interface function
** : Don't care the data

Chapter 17

I^2C Bus Interface (slave)

17. I²C Bus Interface (slave)

17.1 Overview

This LSI includes 1 channel of I²C bus interface (slave).
The secondary functions of Port 8 are assigned to the I²C bus interface data input/output pin and the I²C bus interface clock input/output pin. For Port8, see Chapter 8, "Port 8".

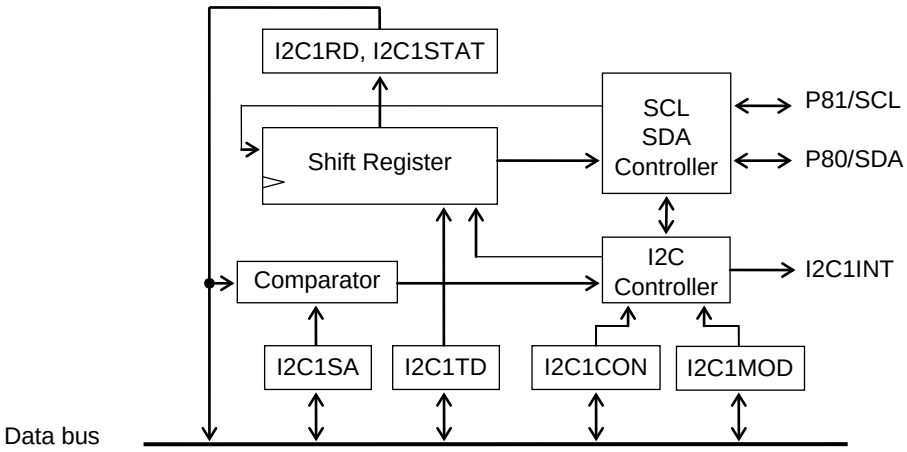
17.1.1 Features

- Slave function
- Communication speeds supported include standard mode (100 kbps) and fast mode (400kbps).
- Allows support for clock synchronization (handshake).

Notes:
- Set HSCLK to 4.096MHz or 8.192MHz. At other frequencies, the communication speed is not 100kbps/400kbps.
- If the power of this LSI is turned off in I²C slave mode, it disables communications of other devices on the I²C bus. If I²C slave function is used, remain the power of this LSI until the master devices power is turned off.

17.1.2 Configuration

Figure 17-1 shows the configuration of the I²C bus interface.



I2C1RD : I²C bus 1 receive register
I2C1SA : I²C bus 1 slave address register
I2C1TD : I²C bus 1 transmit data register
I2C1CON : I²C bus 1 control register
I2C1MOD : I²C bus 1 mode register
I2C1STAT : I²C bus 1 status register

Figure 17-1 Configuration of I²C Bus Interface

17.1.3 List of Pins

Pin name	I/O	Description
P80/SDA	I/O	I^2C bus interface data input/output pin. Used for the secondary function of the P80 pin.
P81/SCL	I/O	I^2C bus interface clock input/output pin. Used for the secondary function of the P81 pin.

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2A8H	I^2C bus 1 receive register	I2C1RD	—	R	8	00H
0F2A9H	I^2C bus 1 slave address register	I2C1SA	—	R/W	8	00H
0F2AAH	I^2C bus 1 transmit data register	I2C1TD	—	R/W	8	00H
0F2ABH	I^2C bus 1 control register	I2C1CON	—	R/W	8	00H
0F2ACH	I^2C bus 1 mode register	I2C1MOD	—	R/W	8	00H
0F2ADH	I^2C bus 1 status register	I2C1STAT	—	R	8	00H

17.2.2 I²C Bus 1 Receive Register (I2C1RD)

Address: 0F2A8H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1RD	I21R7	I21R6	I21R5	I21R4	I21R3	I21R2	I21R1	I21R0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2C1RD is a read-only special function register (SFR) to store receive data.
I2C1RD is updataed after completion of each reception.

[Description of Bits]

· **I21R7 to I21R0** (bits 7 to 0)
The I21R7 to I21R0 bits are used to store receive data. The signal input to the SDA pin is received at reception of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since, not only during data reception but during data transmission, SDA pin data is received synchronously at rising edge of SCL pin, it is possible to check whether transmit data has certainly been transmitted.

17.2.3 I²C Bus 1 Slave Address Register (I2C1SA)

Address: 0F2A9H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1SA	I21A6	I21A5	I21A4	I21A3	I21A2	I21A1	I21A0	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
Initial value	0	0	0	0	0	0	0	0

I2C1SA is a special function register (SFR) to set the address of the slave device.

[Description of Bits]

· **I21A6 to I21A0** (bits 7 to 1)
The I21A6 to I21A0 bits are used to set the address of the communication destination.

17.2.4 I2C Bus 1 Transmit Data Register (I2C1TD)

Address: 0F2AAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1TD	I21T7	I21T6	I21T5	I21T4	I21T3	I21T2	I21T1	I21T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2C1TD is a special function register (SFR) to set transmit data.

[Description of Bits]

· **I21T7 to I21T0** (bits 7 to 0)
The I21T7 to I21T0 bits are used to set transmit data.

17.2.5 I2C Bus 1 Control Register (I2C1CON)

Address: 0F2ABH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1CON	I21ACT	—	I21WT	—	—	—	—	—
R/W	R/W	—	W	—	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

I2C1CON is a special function register (SFR) to control transmit and receive operations.

[Description of Bits]

· **I21WT** (bit 5)
The I21WT bit is used to cancel the communication waiting state(The "L" level is output to the SCL pin). If "1" is written in into the communication waiting state, the communication waiting state is canceled(The "L" level output of the SCL pin is canceled). The I21WT bit is write-only bit. If this bit is read, "0" is always read from this bit.

I21WT	Description
0	Waiting state is not canceled (initial value)
1	Waiting state is canceled

· **I21ACT** (bit 7)
The I21ACT bit is used to set the acknowledge signal to be output at completion of reception.

I21ACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

17.2.6 I2C Bus 1 Mode Register (I2C1MOD)

Address: 0F2ACH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1MOD	—	I21SIE	I21PIE	—	—	—	—	I21EN
R/W	—	R/W	R/W	—	—	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

I2C1MOD is a special function register (SFR) to set operating mode.

[Description of Bits]

· **I21EN** (bit 0)
The I21EN bit is used to enable the operation of the I2C bus interface. When the I21EN bit is set to "1", the I2C bus operation is enabled. When the I20EN bit is set to "0", all the SFRs related to the I2C bus 1 are initialized.

I21EN	Description
0	Stops I2C operation. (Initial value)
1	Enables I2C operation.

· **I21PIE** (bit 5)
The I21PIE bit is used to select enable or disable of stop condition interrupt.

I21PIE	Description
0	Stop condition interrupt disable (Initial value)
1	Stop condition interrupt enable

· **I21SIE** (bit 6)
The I21PIE bit is used to select enable or disable of start condition interrupt.

I21SIE	Description
0	Start condition interrupt disable (Initial value)
1	Start condition interrupt enable

17.2.7 I2C Bus 1 Status Register (I2C1STAT)

Address: 0F2ADH
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2C1STAT	—	—	—	I21TR	I21SAA	I21ER	I21ACR	I21BB
R/W	—	—	—	R	R	R	R	R
Initial value:	0	0	0	0	0	0	0	0

I2C1STAT is a read-only special function register (SFR) to indicate the state of the I2C bus interface.

[Description of Bits]

· **I21BB** (bit 0)
The I21BB bit is used to indicate the state of use of the I2C bus interface. When the start condition is generated on the I2C bus, this bit is set to "1" and when the stop condition is generated, the bit is set to "0". The I21BB bit is set to "0" when the I21EN bit of I2C1MOD is "0".

I21BB	Description
0	I2C bus-free state (Initial value)
1	I2C bus-busy state

· **I21ACR** (bit 1)
The I21ACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I21ACR bit is set to "0" when the I21EN bit of I2C1MOD is "0".

I21ACR	Description
0	Receives acknowledgment "0". (Initial value)
1	Receives acknowledgment "1".

· **I21ER** (bit 2)
The I21ER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". If the I21ER bit is set to "1", the SDA pin output is disabled until the subsequent byte data communication terminates.
The I21ER bit is set to "0" when a write operation to I2C1CON is performed. The I21ER bit is set to "0" when the I21EN bit of I2C1MOD is set to "0".

I21ER	Description
0	No transmit error (initial value)
1	Transmit error

· **I21SAA** (bit 3)
The I21SAA bit is used to show that this device was specified as a slave address.
If the slave address which the master device output and the contents of the I21SA register is in equal, this bit is set to "1". When the I21EN bit of I2C1MOD is set to "0", I21SAA bit is set to "0".

I21SAA	Description
0	Not equal to the slave address (Initial value)
1	Equal to the slave address

· **I21TR** (bit 4)
The I21TR bit is used to indicate the state of the transmission/reception. When "1" is detected in the transmission direction specification bit, this bit is set to "1". When the stop condition detection, the start condition detection and "0" is detected in the transmission direction specification bit, this bit is set to "0". Additionally when the I21EN bit of I2C1MOD is set to "0", the I21TR bit is set to "0".

I21TR	Description
0	Reception state (Initial value)
1	Transmission state

17.3 Description of Operation

17.3.1 Communication Operating Mode

When the slave address is set to the I2C bus 1 slave address register (I2C1SA), and the interrupt of start condition and stop condition is enabled by the I2C bus 1 mode register (I2C1MOD), and I21EN bit is set to "1", then the receive operation is enabled..

17.3.1.1 Start Condition

When the start condition waveform is input to the SDA and SCL pins, the I21BB bit of I2C bus 1 status register is set to "1", then reception operation is started.
After execution of the start condition, the LSI shifts to slave address receiving mode.
When start condition interruption is enabled by the I21SIE bit of I2C bus 1 mode register (I2C1MOD), I2C bus 1 interface interrupt (I2C1INT) occurs.

17.3.1.2 Slave Address Receive Mode

In slave address receive mode, the values (slave address and data communication direction) of the SDA pin is received synchronizing with the rising edge of the serial clock output to the SCL pin.
If the value of the slave address and the value of the I2C bus 1 slave address register (I2C1SA) are in equal, the I21SAA bit of the I2C bus 1 status register (I2C1STAT) is set to "1", and next, the value of the received data direction is stored in the I21TR bit of the I2C1STAT, and finally, the acknowledgment signal ("L" level) is output, and after falling edge detection of the SCL pin under acknowledgment signal transmission, the LSI shifts to the communication waiting state, I2C bus interface interrupt is generated simultaneously.
If the value of the slave address and the value of the I2C bus 1 slave address register (I2C1SA) are not in equal, the I21SAA bit hold "0", storing in the I21TR bit is not performed, acknowledgment signal is not output, and the LSI does not shift to the communication waiting state. Additionally, I2C bus interface interrupt (I2C1INT) is not generated.

17.3.1.3 Communication waiting state

In the communication waiting state, the SCL pin is fixed to the "L" level and communication is changed into a waiting state. In the data reception mode, when preparation of the next data reception is completed, the I21WT bit of I2C bus 1 controll register (I2C1CON) is set to "1", the communication waiting state is canceled. In the data transmitting mode, after setting the next transmitting data to I2C bus 1 transmitting register (I2C1RD), the I21WT bit of I2C bus 1 controll register (I2C1CON) is set to "1", the communication waiting state is canceled.

17.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2C1TD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I21ACR bit of the I2C bus 1 status register (I2C1STAT).
After falling edge detection of the SCL pin under acknowledgment signal reception, the LSI shifts to the communication waiting state, I2C bus interface interrupt (I2C1INT) is generated simultaneously.
The value of I2C1TD output from the SDA pin is stored in I2C1RD.

17.3.1.5 Data Receive Mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I21ACT bit (acknowledgment) of the I2C bus 1 control register (I2C1CON) is output.
After falling edge detection of the SCL pin under acknowledgment signal reception, the LSI shifts to the communication waiting state, I2C bus 1 interface interrupt (I2C1INT) is generated simultaneously.
The data received is stored in I2C1RD after the acknowledgment signal is output. The acknowledgment signal output is received in the I21ACR bit of the I2C bus 1 status register (I2C1STAT).

17.3.1.6 Stop Condition

When the stop condition waveform is input to the SDA and SCL pins, the I21BB bit of I2C bus 1 status register (I2CSTAT) is set to "0", reception operation stops. If the I21PIE bit of I2C bus 1 mode register (I2C1MOD) is enabled, the I2C bus 1 interface interrupt (I2C1INT) is generated.

17.3.2 Communication Operation Timing

Figures 17-2 to 17-4 show the operation timing and control method for each communication mode.

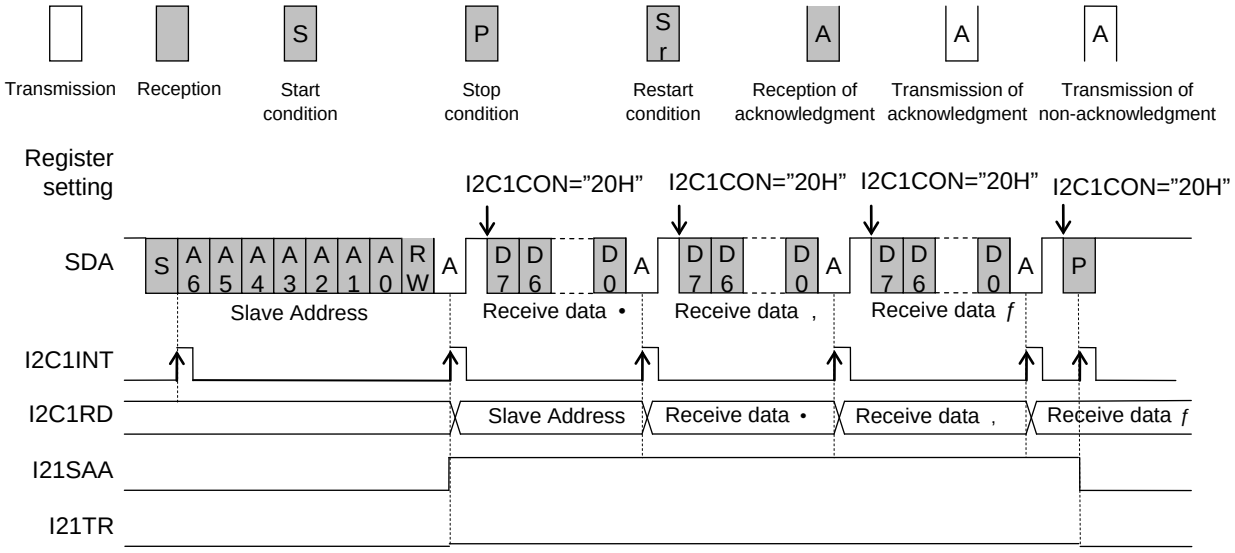


Figure 17-2 Operation Timing in Data Receive Mode

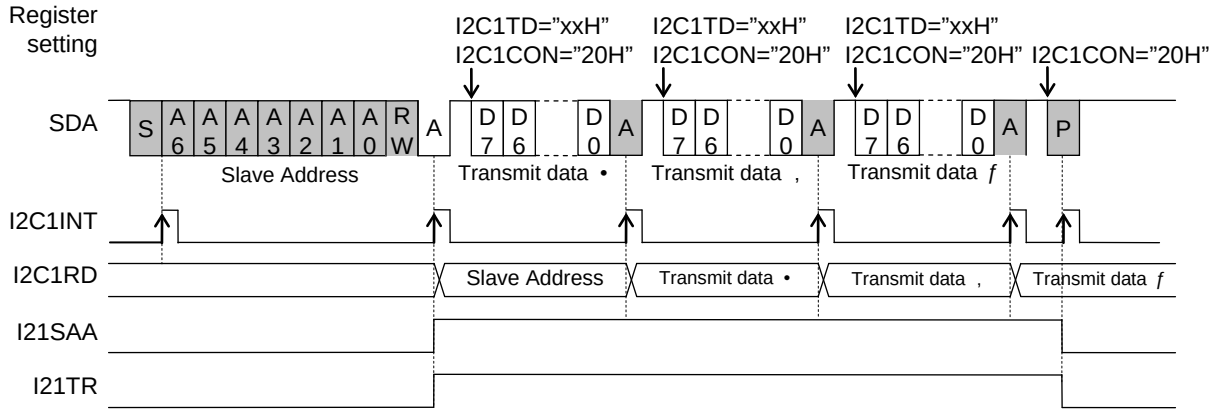


Figure 17-3 Operation Timing in Data Transmit Mode

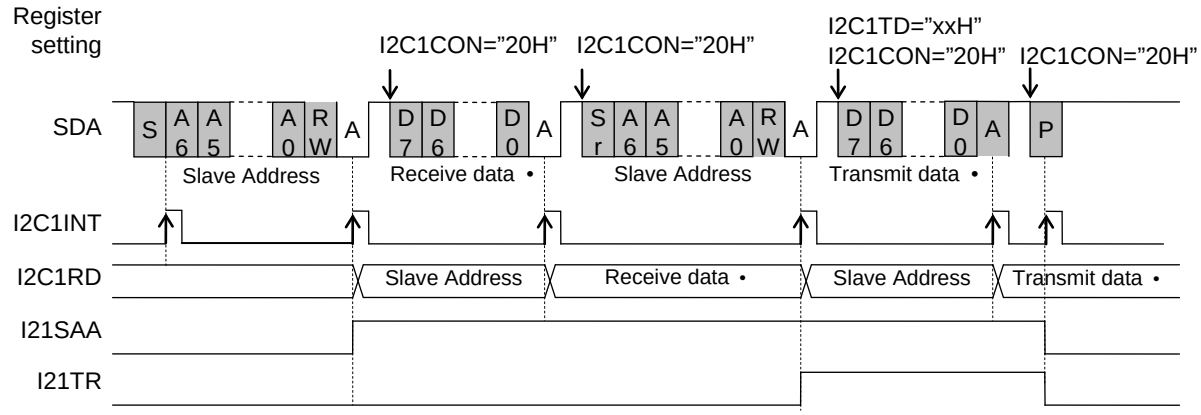


Figure 17-4 Operation Timing at Data Transmit/Receive Mode Switching

When the values of the transmitted bit and the SDA pin do not coincide, the I21ER bit of the I²C bus 1 status register (I2C1STAT) is set to "1" and SDA pin output is prohibited until termination of the subsequent byte data communication.
Figure 17-5 shows the operation timing and control method when transmission fails.

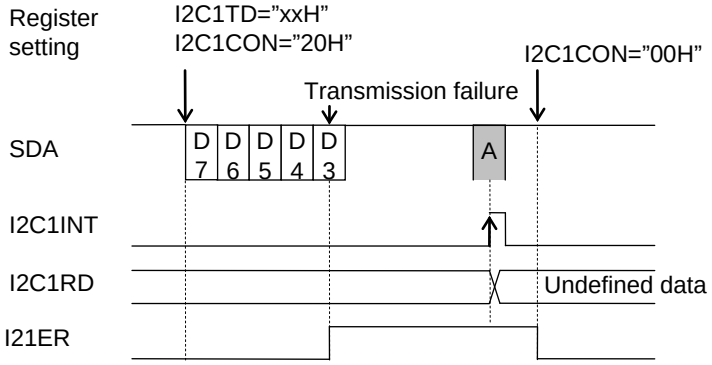


Figure 17-5 Operation Timing When Transmission Fails

17.3.3 Operation Waveforms

Figure 17-6 shows the operation waveforms of the SDA and SCL signals and the I21BB flag.

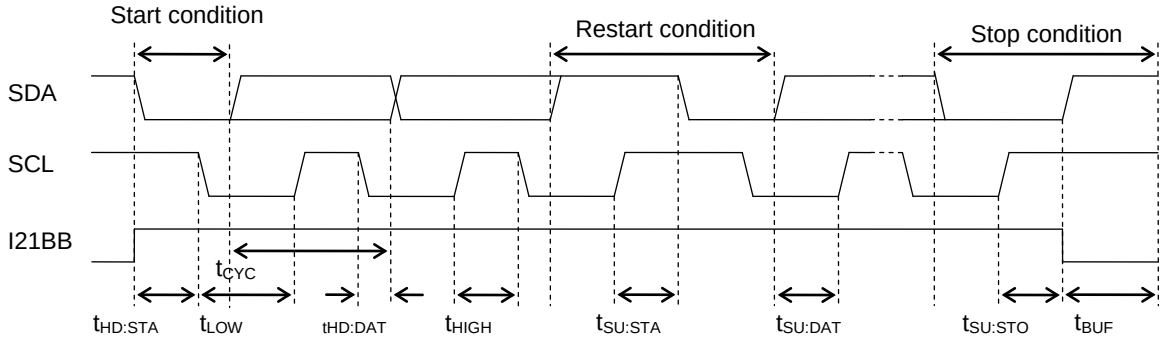


Figure 17-6 Operation Waveforms of SDA and SCL Signals and I21BB Flag

17.4 Specifying Port Registers

When you want to make sure the I²C function is working, please check related port registers are specified. See Chapter 8, "Port 8" for detail about the port registers.

17.4.1 Functioning P81(SCL:input/output) and P80(SDA:input/output) as the I²C

Set P81MD1 to P80MD1 bits(bits1 to bit0 of P8MOD1 register) to "0" and set P81MD0 to P80MD0(bit1 to bit0 of P8MOD0 register) to "1", for specifying the I²C as the secondary function of P81 and P80.

Reg. name	P8MOD1 register (Address: 0F245H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87MD1	P86MD1	P85MD1	P84MD1	P83MD1	P82MD1	**P81MD1**	**P80MD1**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P8MOD0 register (Address: 0F244H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87MD0	P86MD0	P85MD0	P84MD0	P83MD0	P82MD0	**P81MD0**	**P80MD0**
Data	*	*	*	*	*	*	**1**	**1**

Set P81C1 to P80C1 bit(bits1 to 0 of P8CON1 register) to "1", set P81C0 to P80C0 bit(bits1 to 0 of P8CON0 register) to "0", and set P81DIR to P80DIR bit(bits1 to 0 of P8DIR register) to "0", for specifying the P81 and P80 as Nch open-drain output. The pulled-up open-drain/open-collector outputs are required on the I²C bus line to avoid collision between H level and L level.

Reg. name	P8CON1 register (Address: 0F243H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87C1	P86C1	P85C1	P84C1	P83C1	P82C1	**P81C1**	**P80C1**
Data	*	*	*	*	*	*	**1**	**1**

Reg. name	P8CON0 register (Address: 0F242H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87C0	P86C0	P85C0	P84C0	P83C0	P82C0	**P81C0**	**P80C0**
Data	*	*	*	*	*	*	**0**	**0**

Reg. name	P8DIR register (Address: 0F241H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87DIR	P86DIR	P85DIR	P84DIR	P83DIR	P82DIR	**P81DIR**	**P80DIR**
Data	*	*	*	*	*	*	**0**	**0**

Data of P81D to P80D bits (bits1 to 0 of P8D register) do not affect to the I²C function, so don't care the data for the function.

Reg. name	P8D register (Address: 0F240H)							
Bit	7	6	5	4	3	2	**1**	**0**
Bit name	P87D	P86D	P85D	P84D	P83D	P82D	**P81D**	**P80D**
Data	*	*	*	*	*	*	******	******

* : Bit not related to the I²C(using P81 and P80) function
** : Don't care the data

Chapter 18

Successive Approximation Type A/D Converter

18. Successive Approximation Type A/D Converter (SA-ADC)

18.1 Overview

This LSI has a built-in 3-channel or 4-channel(*1) successive approximation type A/D converter (SA-ADC).
The SA-ADC operates only when the DSAD bit of the block control register 4 (BLKCON4) is "0" and high speed clock oscillation is enabled. When the DSAD bit is "1", every function of the SA-ADC is in a reset state.
For the block control registers, see Chapter 5, "MCU Control Function".
(*1): built into ML610Q306.

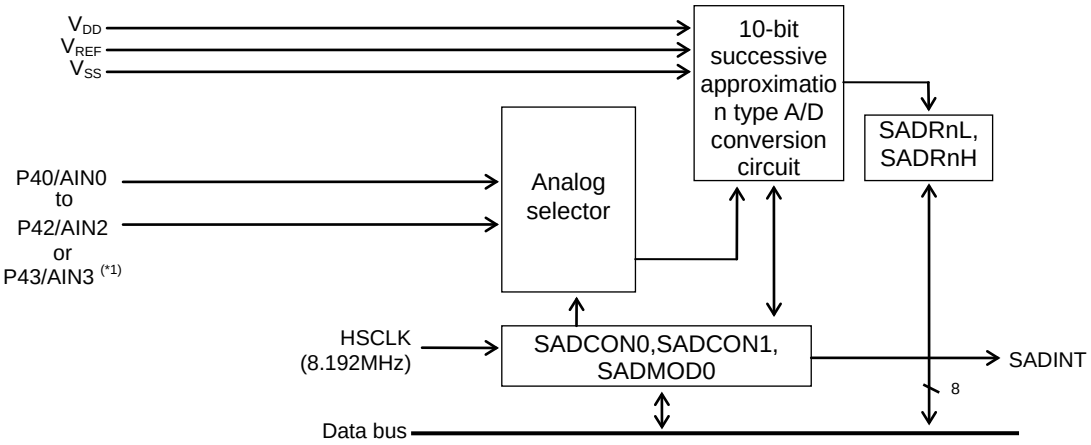
18.1.1 Features

- Built-in sample/hold 10-bit successive approximation type A-D converter
- Three channels or four channels(*1) analog inputs can be selected.
- Conversion time : Approx. 12.75us/ch (PLL oscillation mode)
- Continuous conversion / single conversion can be selected.

(*1): built into ML610Q306.

18.1.2 Configuration

Figure 18-1 shows the configuration of SA-ADC.



SADRnL : SA-ADC result register nL
SADRnH : SA-ADC result register nH

SADCON0 : SA-ADC control register 0
SADCON1 : SA-ADC control register 1
SADMOD0 : SA-ADC mode register 0 n: 0 to 2 or 3(*1)

Figure 18-1 Configuration of SA-ADC

(*1): built into ML610Q306.

18.1.3 List of Pins

Pin name	I/O	Description
V_{DD}	¾	Positive power supply pin for the successive approximation type A/D converter
V_{REF}	¾	Reference power supply pin for the successive approximation type A/D converter
V_{SS}	¾	Negative power supply pin for the successive approximation type A/D converter
P40/AIN0	I	successive approximation type A/D converter input pin 0
P41/AIN1	I	successive approximation type A/D converter input pin 1
P42/AIN2	I	successive approximation type A/D converter input pin 2
P43/AIN3(*1)	I	successive approximation type A/D converter input pin 3

Note:
When P40-P42 and P43(*1) is used as the input of successive approximation type A/D converter, set them to High-impedance output mode.

(*1): built into ML610Q306.

18.2 Description of Registers

18.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F2D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F2D6H	SA-ADC result register 3L(*1)	SADR3L	SADR3	R	8/16	00H
0F2D7H	SA-ADC result register 3H(*1)	SADR3H		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	—	R/W	8	00H

(*1): built into ML610Q306.

18.2.2 SA-ADC Result Register 0L (SADR0L)

Address: 0F2D0H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0L	SAR03	SAR02	¾	¾	¾	¾	¾	¾
R/W	R	R	¾	¾	¾	¾	¾	¾
Initial value	0	0	0	0	0	0	0	0

SADR0L is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0L is updated after A/D conversion.

[Description of Bits]

· **SAR03 to SAR02** (bits 7 to 6)
The SAR03 to SAR02 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 0.

18.2.3 SA-ADC Result Register 0H (SADR0H)

Address: 0F2D1H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR0H	SAR0B	SAR0A	SAR09	SAR08	SAR07	SAR06	SAR05	SAR04
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR0H is a special function register (SFR) used to store SA-ADC conversion results on channel 0.
SADR0H is updated after A/D conversion.

[Description of Bits]

· **SAR0B to SAR04** (bits 7 to 0)
The SAR0B3 to SAR04 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 0.

18.2.4 SA-ADC Result Register 1L (SADR1L)

Address: 0F2D2H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1L	SAR13	SAR12	¾	¾	¾	¾	¾	¾
R/W	R	R	¾	¾	¾	¾	¾	¾
Initial value	0	0	0	0	0	0	0	0

SADR1L is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1L is updated after A/D conversion.

[Description of Bits]

· **SAR13 to SAR12** (bits 7 to 6)
The SAR13 to SAR12 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 1.

18.2.5 SA-ADC Result Register 1H (SADR1H)

Address: 0F2D3H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR1H	SAR1B	SAR1A	SAR19	SAR18	SAR17	SAR16	SAR15	SAR14
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR1H is a special function register (SFR) used to store SA-ADC conversion results on channel 1.
SADR1H is updated after A/D conversion.

[Description of Bits]

· **SAR1B to SAR14** (bits 7 to 0)
The SAR1B to SAR14 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 1.

18.2.6 SA-ADC Result Register 2L (SADR2L)

Address: 0F2D4H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2L	SAR23	SAR22	¾	¾	¾	¾	¾	¾
R/W	R	R	¾	¾	¾	¾	¾	¾
Initial value	0	0	0	0	0	0	0	0

SADR2L is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2L is updated after A/D conversion.

[Description of Bits]

· **SAR23 to SAR22** (bits 7 to 6)
The SAR23 to SAR22 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 2.

18.2.7 SA-ADC Result Register 2H (SADR2H)

Address: 0F2D5H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR2H	SAR2B	SAR2A	SAR29	SAR28	SAR27	SAR26	SAR25	SAR24
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR2H is a special function register (SFR) used to store SA-ADC conversion results on channel 2.
SADR2H is updated after A/D conversion.

[Description of Bits]

· **SAR2B to SAR24** (bits 7 to 0)
The SAR2B to SAR24 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 2.

18.2.8 SA-ADC Control Register 0 (SADCON0)

Address: 0F2F0H
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON0	¾	¾	¾	¾	¾	¾	¾	SALP
R/W	¾	¾	¾	¾	¾	¾	¾	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

· **SALP** (bit 0)
This bit is used to select whether A/D conversion is performed once only for each channel or continuously . When this bit is set to "0", A/D conversion is performed once only for each channel and when it is set to "1", A/D conversion is performed continuously.

SALP	Description
0	Single A/D conversion (Initial value)
1	Continuous A/D conversion

Note:
Set SA-ADC Control Register 0 before A/D conversion is started.

18.2.9 SA-ADC Control Register 1 (SADCON1)

Address: 0F2F1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	¾	¾	¾	¾	¾	¾	¾	SARUN
R/W	¾	¾	¾	¾	¾	¾	¾	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON1 is a special function register (SFR) used to control the operation of the SA-ADC.

[Description of Bits]

· **SARUN** (bit 0)

The SARUN bit is used to start or stop SA-ADC conversion. Setting this bit to "1" starts A/D conversion and setting it to "0" stops A/D conversion.

When SALP of SADCON0 is "0" and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to "0".

SARUN	Description
0	Stops conversion. (Initial value)
1	Starts conversion.

Notes:

· Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).

· Do not start A/D conversion with all of bit-3 (SACH3)(*) and bit-2 (SACH2) to bit-0 (SACH0) of the SA-ADC mode register 0. If A/D conversion is started in this state, the SARUN remains "0" and no A/D conversion is carried out. Start conversion after setting the SACH3(*) and SACH2-SACH0 of SA-ADC mode register 0(SADMOD0).

(*): built into ML610Q306.

18.2.10 SA-ADC Mode Register 0 (SADMOD0)

Address: 0F2F2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADMOD0	¾	¾	¾	¾	SACH3(*)	SACH2	SACH1	SACH0
R/W	¾	¾	¾	¾	R/W(*)	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADMOD0 is a special function register (SFR) used to choose A/D conversion channel(s).

[Description of Bits]
The SACH3(*) and SACH2 to SACH0 bits are used to select channel(s) on which A/D conversion is performed.
If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.

· **SACH0** (bit 0)

SACH0	Description
0	Stops conversion on channel 0. (Initial value)
1	Performs conversion on channel 0.

· **SACH1** (bit 1)

SACH1	Description
0	Stops conversion on channel 1. (Initial value)
1	Performs conversion on channel 1.

· **SACH2** (bit 2)

SACH2	Description
0	Stops conversion on channel 2. (Initial value)
1	Performs conversion on channel 2.

· **SACH3** (bit 3) (*)

SACH3(*)	Description
0	Stops conversion on channel 3. (Initial value)
1	Performs conversion on channel 3.

Note:
Do not start A/D conversion in the state that all the bits of the bit 3 (SACH3) (*) and bit 2 (SACH2) to the bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) are "0". If A/D conversion is started in this state, the SARUN remains "0" and no A/D conversion is carried out. Start conversion after setting the SACH3(*) and SACH2-SACH0 of SA-ADC mode register 0(SADMOD0).

(*): built into ML610Q306.

18.2.11 SA-ADC Result Register 3L (SADR3L)

Address: 0F2D6H
Access: R
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3L	SAR33	SAR32	¾	¾	¾	¾	¾	¾
R/W	R	R	¾	¾	¾	¾	¾	¾
Initial value	0	0	0	0	0	0	0	0

SADR3L is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3L is updated after A/D conversion. This register is built into ML610Q306.

[Description of Bits]

· **SAR33 to SAR32** (bits 7 to 6)
The SAR33 to SAR32 bits are used to store the values of bit 1 to bit 0 of A/D conversion results (10 bits) on channel 3.

18.2.12 SA-ADC Result Register 3H (SADR3H)

Address: 0F2D7H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADR3H	SAR3B	SAR3A	SAR39	SAR38	SAR37	SAR36	SAR35	SAR34
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SADR3H is a special function register (SFR) used to store SA-ADC conversion results on channel 3.
SADR3H is updated after A/D conversion. This register is built into ML610Q306.

[Description of Bits]

· **SAR3B to SAR34** (bits 7 to 0)
The SAR3B to SAR34 bits are used to store the values of bit 9 to bit 2 of A/D conversion results (10 bits) on channel 3.

18.3 Description of Operation

18.3.1 Setup of the A/D conversion channel

By setup of the SA-ADC mode register 0 (SADMOD0), as shown in the following table, A/D conversion operation is performed, and the A/D conversion result is stored in the SA-ADC result register.

SA-ADC mode register 0/1				SA-ADC result register				Remarks
SACH3(*)	SACH2	SACH1	SACH0	SADR3(*)	SADR2	SADR1	SADR0	
0	0	0	0					Prohibition of use
0	0	0	1				AIN0	
0	0	1	0			AIN1		
0	0	1	1			AIN1	AIN0	
0	1	0	0		AIN2			
0	1	0	1		AIN2		AIN0	
0	1	1	0		AIN2	AIN1		
0	1	1	1		AIN2	AIN1	AIN0	
1	0	0	0	AIN3				
1	0	0	1	AIN3			AIN0	
1	0	1	0	AIN3		AIN1		
1	0	1	1	AIN3		AIN1	AIN0	
1	1	0	0	AIN3	AIN2			
1	1	0	1	AIN3	AIN2		AIN0	
1	1	1	0	AIN3	AIN2	AIN1		
1	1	1	1	AIN3	AIN2	AIN1	AIN0	

(*): built into ML610Q306.

The value of the result register of a slash part does not change.
Do not start A/D conversion in the state that all the bits of the bit 3 (SACH3) (*) and the bit 2 (SACH2) to the bit 0 (SACH0) of the SA-ADC mode register 0 (SADMOD0) are "0". If A/D conversion is started in this state, the SARUN remains "0" and no A/D conversion is carried out. Start conversion after setting the SACH3(*) and SACH2-SACH0 of SA-ADC mode register 0(SADMOD0).
(*): built into ML610Q306.
Figure 18-2 shows the A/D conversion pins and the conversion range.

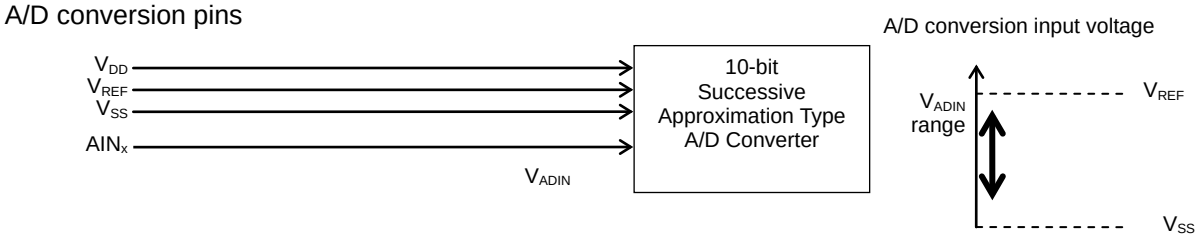


Figure 18-2 The A/D conversion pins and the conversion range

18.3.2 Operation of Successive Approximation Type A/D Converter

Use the following procedure to operate the SA-ADC:

1. Before starting the SA-ADC, start oscillation of the high-speed clock (HSCLK) and wait until the oscillation stabilizes.
2. Set the input port for A/D conversion to High-impedance output mode.
3. Set DSAD bit "0" in Block Control Register 4(BLKCON4).
4. Select the ADC conversion channel on SA-ADC mode register 0 (SADMOD0).
5. Select single A/D conversion or continuous A/D conversion on SA-ADC Control Register 0(SADCON0).
6. When bit 0 (SARUN) of SA-ADC control register 1 (SADCON1) is set to "1", the SA-ADC circuit becomes active and performs A/D conversion from the lower channel number that is selected in the SA-ADC mode register (SADMOD0).
7. A/D conversion results are stored in the applicable SA-ADC result registers (SADRnL, SADRnH), and when A/D conversion of the largest channel number that is selected is terminated, an SA-ADC conversion termination interrupt (SADINT) is generated.
   If bit 0 of SADCON0 register(SALP) is "0", SARUN bit is automatically cleared when the last channel of A/D conversion is finished.
   If bit 0 of SADCON0 register(SALP) is "1", A/D conversion is started again. Therefore, after A/D conversion is finished , set SARUN bit "0" and stop the A/D conversion by the software.
8. If A/D conversion is required again, repeat the step from 4 to 7.

Even if a channel is switched during A/D conversion, the channel that was selected at the start of A/D conversion is used until an A/D conversion termination interrupt occurs.

Figure 18-3 shows the SA-ADC operation timing when channel 0 and channel 1 are selected.

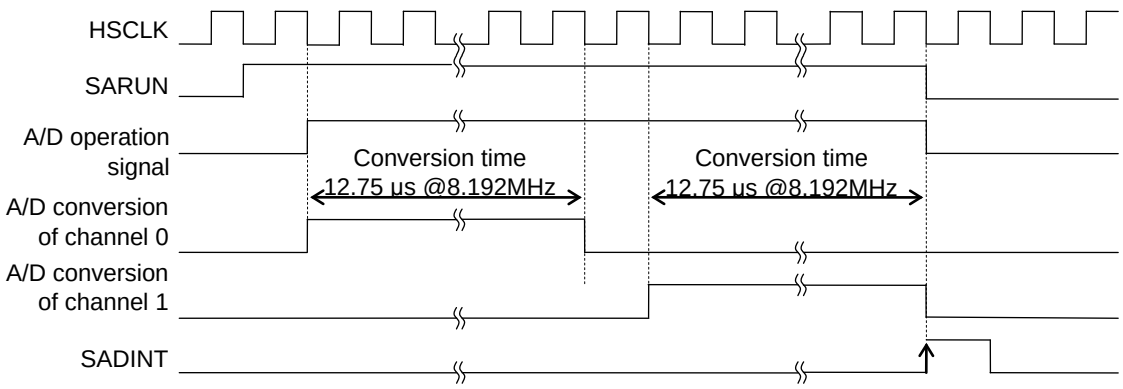


Figure 18-3 SA-ADC Operation Timing

Notes:
· When the input of successive approximation type A/D converter is set to High-impedance input mode, a current may flow through input buffer depending on the analog voltage to be converted. Therefore, set the input to High-impedance output mode.
· SA-ADC has a built-in about 19pF capacitance. To complete charging this 19pF capacitance within about 7.3us sampling time, the output impedance of the signal source connected to the analog input(AINn) should be 5k ohms or less. When the output impedance cannot be 5k ohms or less, connect 0.1uF capacitance between the analog input(AINn) and V_{SS}.
· When no capacitance is connected between analog input(AINn) and V_{SS}, at the start of A/D conversion, the charge remaining in the built-in 19pF capacitance is released to analog input(AINn). And the voltage of analog input(AINn) may fluctuate momentarily. When the output impedance is within 5k ohms or less, it dose not affect the A/D conversion result.

Chapter 19

Audio Playback Function

19. Audio Playback Function

19.1 Overview

This LSI has an audio playback function.
The audio playback function is enabled only when the DVC0 bit of the block control register 3 (BLKCON3) is "0". If the DVC0 bit is "1", the audio playback function is in a reset state. For the block control registers, see Chapter 5, "MCU Control Function".

19.1.1 Features

The built-in Class D speaker amplifier integrates all the functions required for audio playback into one chip, enabling audio output simply by connecting a speaker.

• Audio playback time: (e.g. for control program 16Kbyte)

ROM Capacity (bits)	Maximum playback time (sec.) (Sampling Frequency: 8.0kHz)		
	4-bit ADPCM2	16-bit PCM	HQ-ADPCM
630K	20.1	5.1	25.2

- Sampling frequency: Selectable from among 8/16/32 kHz; 10.7/21.3 kHz; 6.4/12.8/25.6 kHz in each phrase
- Allows audio operations using the following voice synthesis algorithms: 4-bit ADPCM2, 8-bit non-linear PCM, 8-bit straight PCM, and 16-bit straight PCM, and HQ-ADPCM.
- Volume adjustment function: The volume can be set at 32 levels (including off-state).
- Editing ROM function: Continuous playback of multiple phrases is possible
  The memory capacity of the audio code data can be used efficiently. For details, refer to section 19.3.5, Editing ROM Function.

19.1.2 Configuration

19.1.2.1 Block Configuration

Figure 19-1 shows the configuration of the audio playback function.

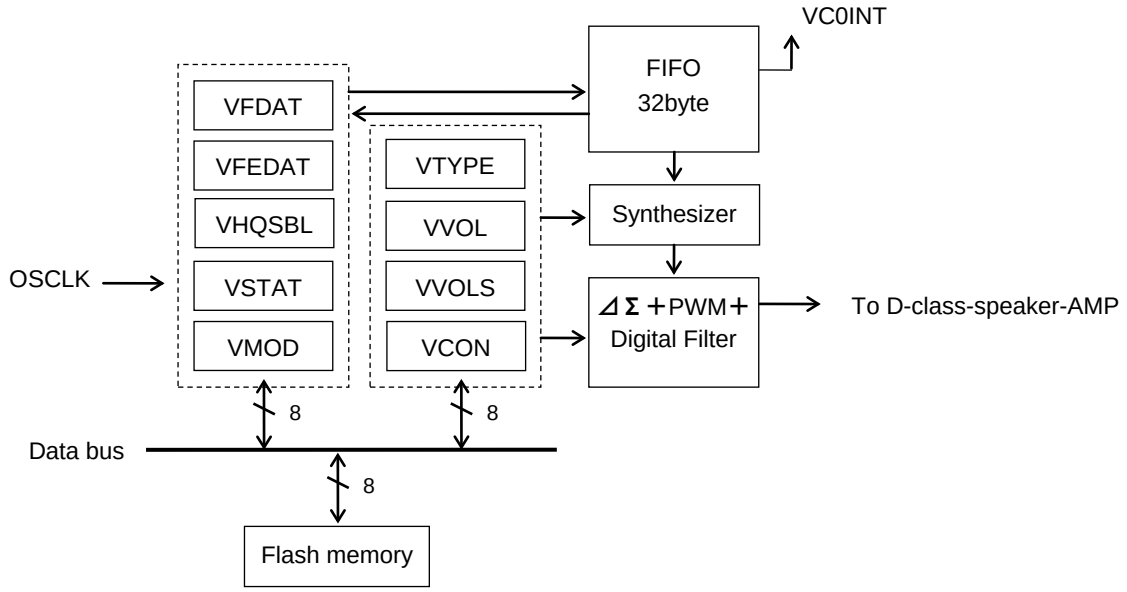


Figure 19-1 Configuration of the Audio Playback Function

The operation principle of audio playback is as follows.

(1) Original sound data (WAV file) is converted into audio code data (binary data, Motorola S format) by Speech LSI Utility tools (audio phrase creation, voice synthesis method, sampling frequency, etc.). The data is placed in the flash memory as audio code data.
(2) Audio data placed in the flash memory is transferred to the voice synthesis circuit via the CPU
(3) Voice synthesizes is carried out while storing audio data in a FIFO, and reproduces the sound close to the original sound with digital filters.
(4) PWM signal is output from a digital filter and amplified by a built-in class-D speaker amplifier for audio reproduction.

Note:
When using the audio playback function, set the system clock setting to high-speed clock in the frequency control register 1 (FCON1).

HQ-ADPCM is audio compression technology featuring high-quality sound. It was developed by "Ky's". "Ky's" is a registered trademark of Kyushu Institute of Technology, one of the national universities in Japan.

19.1.2.2 Placement of audio code data

Audio code data can be placeed in the whole area of segment 1 and the free area of segment 0.
Figure 19-2 shows the placement of audio code data.
The audio code data is arranged from 0x0000 address of segment 1, and audio code data exceeding the capacity of segment 1 is placed in segment 0.

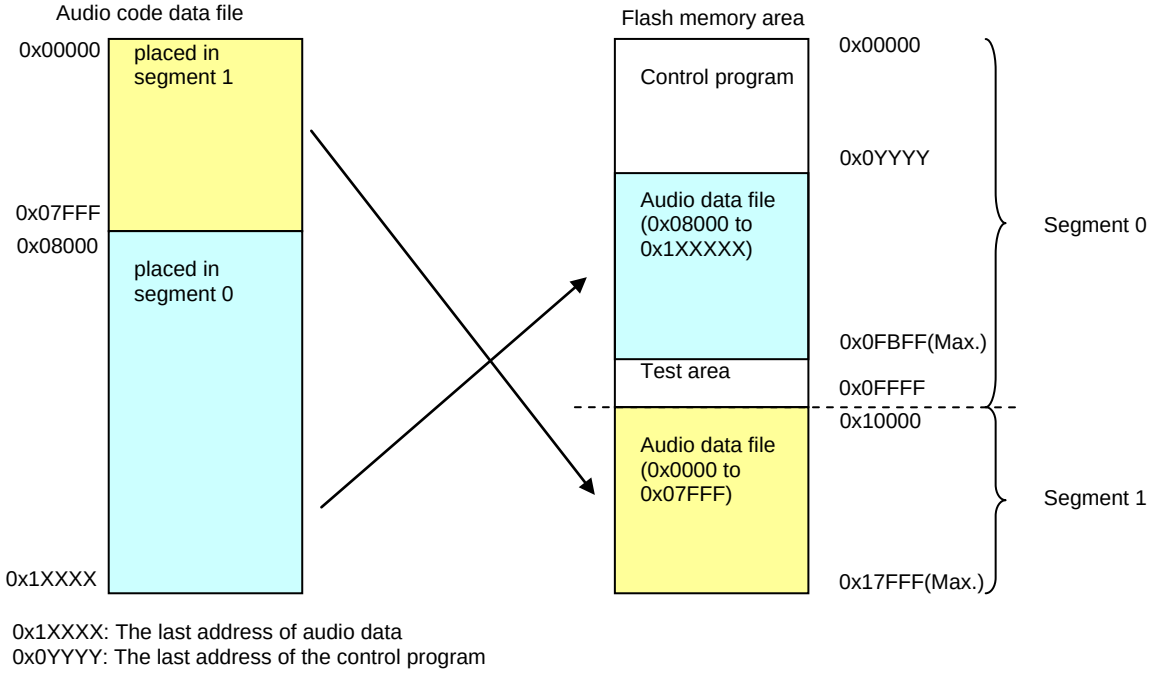


Figure 19-2 Placement of audio code data

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2B0H	Audio FIFO data register	VFDAT	—	W	8	00H
0F2B1H	Audio FIFO phrase end data register	VFEDAT	—	W	8	00H
0F2B2H	HQ phrase stop-bit length register	VHQSBL	—	R/W	8	00H
0F2B3H	Audio status register	VSTAT	—	R	8	11H
0F2B4H	Audio mode register	VMOD	—	R/W	8	00H
0F2B5H	Audio data type register	VTYPE	—	R/W	8	41H
0F2B6H	Volume setting register	VVOL	—	R/W	8	09H
0F2B7H	Audio playback control register	VCON	—	R/W	8	00H
0F2C0H	Volume status register	VVOLS	—	R	8	09H

19.2.2 Audio FIFO Data Register (VFDAT)

Address: 0F2B0H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VFDAT	VFDAT7	VFDAT6	VFDAT5	VFDAT4	VFDAT3	VFDAT2	VFDAT1	VFDAT0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

VFDAT is a special function register (SFR) used to store audio data.
The audio data area stores the audio data of each voice synthesis method.

The audio data placement format for each voice synthesis method is shown below.

(1) 4-bit ADPCM2
Each 4-bit data is placed from the MSB side.

Audio data	MSB	LSB
1st byte	Data 1	Data 2
2nd byte	Data 3	Data 4
3rd byte	Data 5	Data 6
.....		

(2) 8-bit Straight PCM
The 8-bit data is placed as is.

Audio data	MSB LSB
1st byte	Data 1
2nd byte	Data 2
3rd byte	Data 3
.....	

(3) 16-bit Straight PCM
The data is placed in 16-bit units in the order of the lower 8-bit data and the higher 8-bit data.

Audio data	MSB LSB
1st byte	Data 1 (lower 8 bits)
2nd byte	Data 1 (higher 8 bits)
3rd byte	Data 2 (lower 8 bits)
4th byte	Data 2 (higher 8 bits)
.....	

(4) HQ-ADPCM

The stop-bit length data (E4–E0) of HQ-ADPCM are stored in the 1st byte, and the actual audio data is placed in the 2nd and subsequent bytes. The data length is variable and averages 3.2bits. When playing the HQ-ADPCM phrase, store E4–E0 in the HQ phrase stop-bit length register (VHQSBL).

Audio data	MSB							LSB
1st byte	E4	E3	E2	E1	E0	0	0	0
2nd byte	Data 1							
3rd byte	Data 2							
4th byte	Data 3							
5th byte	Data 4							
……								

19.2.3 Audio FIFO Phrase End Data Register (VFEDAT)

Address: 0F2B1H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VFEDAT	VFEDAT7	VFEDAT6	VFEDAT5	VFEDAT4	VFEDAT3	VEFDAT2	VEFDAT1	VEFDAT0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

VFEDAT is a special function register (SFR) used to store the final data of a phrase.
Since the final data of a phrase will be identified in audio playback operation, store the final data of a phrase in this register.

19.2.4 Audio Status Register (VSTAT)

Address: 0F2B3H
Access: R
Access size: 8 bits
Initial value: 11H

	7	6	5	4	3	2	1	0
VSTAT	VERR	¾	¾	VAEND	VDEND	VFUL	VMID	VEMP
R/W	R	-	-	R	R	R	R	R
Initial value	0	0	0	1	0	0	0	1

VSTAT is a special function register (SFR) that indicates the status of the audio playback function.
Since an audio data request interrupt occurs when any of the following interrupt causes is generated, check the cause of the interrupt request by reading this register.

- VMID bit goes to "0" from "1"(When the audio data in FIFO is less than the number of byte specified in VMOD.)
- VDEND bit goes to "1"(When the final audio data is output to the digital filter.)
- VAEND bit goes to "1"(While PWM-voice circuit is powered down.)
- VERR bit goes to "1"(When there is an error in reading audio data.)

[Description of Bits]

· **VEMP** (bit 0)
VEMP indicates the status (EMPTY) of the FIFO that stores audio data.

VEMP	Description
0	Status of the FIFO that stores audio data ¹ EMPTY
1	Status of the FIFO that stores audio data = EMPTY (initial value)

· **VMID** (bit 1)
VMID indicates the status (MIDDLE)of the FIFO that stores audio data.
Uses the FIFO interrupt request level set by the FIFO interrupt control register (VMOD) as the MIDDLE position to make status judgment.

VMID	Description
0	Status of the FIFO that stores audio data < MIDDLE (initial value)
1	Status of the FIFO that stores audio data ³ MIDDLE

· **VFUL** (bit 2)
VFUL indicates the status (FULL)of the FIFO that stores audio data (32byte).

VFUL	Description
0	Status of the FIFO that stores audio data ¹ FULL (initial value)
1	Status of the FIFO that stores audio data = FULL

· **VDEND** (bit 3)
VDEND is a bit that indicates that the final data was output from the digital filter.
The VDEND bit goes to "1" when the final data written to the FIFO phrase end data register (VFEDAT) is taken into the digital filter and then output from it with the FIFO kept EMPTY.
If either any data is written to the FIFO data register (where the FIFO is no longer EMPTY) or VCEN bit = "0", VDEND goes to "0".

VDEND	Description
0	Final data was not output from the digital filter (initial value).
1	Final data was output from the digital filter.

· **VAEND** (bit 4)
VAEND is a bit that indicates that the PWM-voice circuit is in the power-down state.
Setting the VCEN bit of the audio playback control register (VCON) to "1" from "0" puts the PWM-voice circuit into the power-up state and VAEND goes to "0". Setting the VCEN bit to "0" from "1" puts the PWM-voice circuit tinto the power-down state. When returned from the PWM-voice circuit power-down state, the VAEND bit is set to "1".

VAEND	Description
0	PWM-voice circuit is in the power-up state.
1	PWM-voice circuit is in the power-down state (initial value).

· **VERR** (bit 7)
VERR is a bit that indicates an audio data read error.
The audio operation circuit reads the audio data written to the FIFO every sampling period according to the voice synthesis method; however, if an error occurs in the audio data, the VERR bit is set to "1".

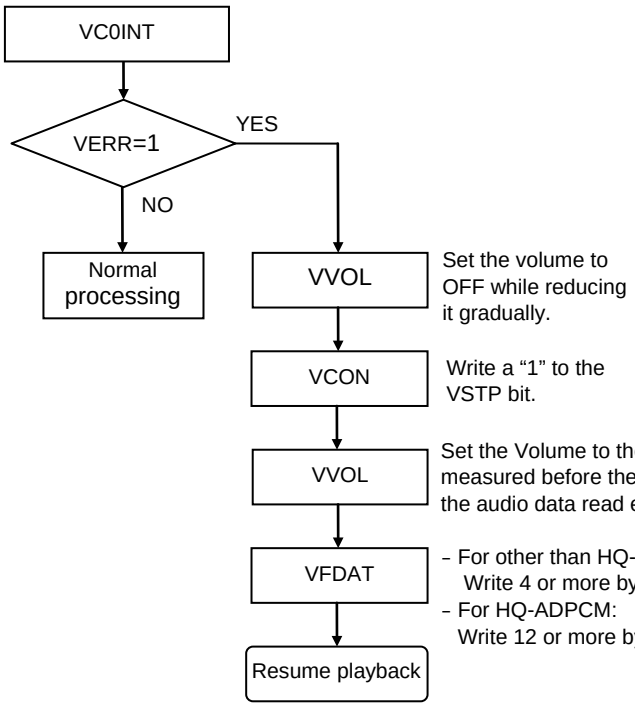
An audio data read is determined as a read error if the following conditions are met:

16-bit Straight PCM : When the audio operation circuit reads audio data in a state where the size of the audio data in FIFO is 1 byte
HQ-ADPCM : When the audio operation circuit reads audio data in a state where the size of the audio data in FIFO is 1 to 3 bytes (excluding the final data)

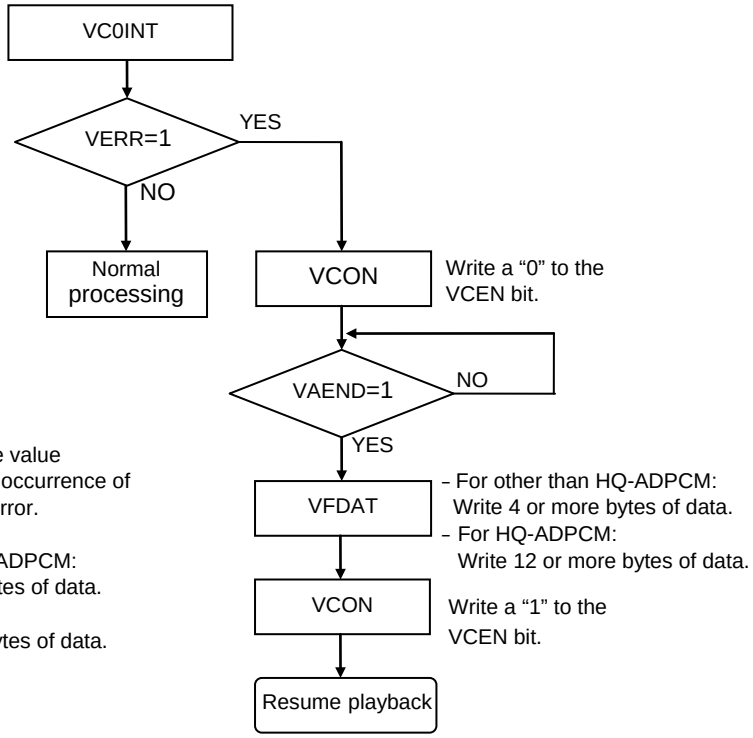
VERR	Description
0	No audio data read error detected (initial value)
1	Audio data read error detected

Note:
If VERR goes to "1", perform either of the following processing units:

j Processing using VCON's VSTP bit
Initialize the FIFO and audio operation circuit with the PWM-voice circuit being in a power-up state.



k Processing using VCON's VCEN bit
Put the PWM-voice circuit into the power-down state, and then resume processing from power-up processing.



19.2.5 Audio Mode Register (VMOD)

Address: 0F2B4H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VMOD	VVOLPS	¾	¾	¾	¾	VFMD2	VFMD1	VFMD0
R/W	R/W	-	-	-	-	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

· **VFMD2, VFMD1, VFMD0** (bits 2 to 0)
VFMD2, VFMD1 and VFMD0 are bits that select the interrupt request level for the FIFO that stores audio data. When the audio data in FIFO becomes less than the number of remaining byte specified by VFMD2, VFMD1,VFMD0, VMID bit of the audio status register (VSTAT) is set to "0".

VFMD2	VFMD1	VFMD0	Interrupt request level
0	0	0	1 byte (initial value)
0	0	1	10 bytes
0	1	0	4 bytes
0	1	1	8 bytes
1	0	0	12 bytes
1	0	1	16 bytes
1	1	0	20 bytes
1	1	1	24 bytes

· **VVOLPS** (bit 7)
The VVOLPS is a bit that selects the timing at which the setting of the volume setting register (VVOL) is reflected.
When set to "0", the VVOL setting value is immediately reflected in the playback sound.
When set to "1", the VVOL setting value is reflected synchronously when the phrase playback is started. Even if the VVOL setting is changed during audio playback, it will not be reflected in the playback sound. It is used to change the volume in sychronization with the playback after the data of the next phrase (The next data after the data written to VFEDAT) during continuous playback.

VVOLPS	Description
0	The volume setting register (VVOL) setting is immediately reflected in the playback sound (initial value).
1	The volume setting register (VVOL) setting is reflected synchronously when the phrase playback is started.

Note:
In the case of HQ-ADPCM, a single voice synthesis operation may use 12 bytes of data.
(When HQ-ADPCM(1/5) is selected by the audio data type register, the average audio data size is 16 bits/5 @3.2 bits.)

19.2.6 Audio Data Type Register (VTYPE)

Address: 0F2B5H
Access: R/W
Access size: 8 bits
Initial value: 41H

	7	6	5	4	3	2	1	0
VTYPE	¾	VSYN2	VSYN1	VSYN0	VSMP3	VSMP2	VSMP1	VSMP0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	1	0	0	0	0	0	1

VTYPE is a special function register (SFR) used to specify the voice synthesis algorithm and sampling frequency.

[Description of Bits]

· **VSMP3**, **VSMP2, VSMP1, VSMP0** (bits 3 to 0)
VSMP3, VSMP2, VSMP1, and VSMP0 are bits used to select the sampling frequency.

VSMP3	VSMP2	VSMP1	VSMP0	Sampling frequency
0	0	0	0	Setting prohibited
0	0	0	1	8.0 kHz (initial value)
0	0	1	0	16.0 kHz
0	0	1	1	32.0 kHz
0	1	0	0	Setting prohibited
0	1	0	1	10.7 kHz
0	1	1	0	21.3 kHz
0	1	1	1	Setting prohibited
1	0	0	0	6.4 kHz
1	0	0	1	12.8 kHz
1	0	1	0	25.6 kHz
1	0	1	1	Setting prohibited
1	1	*	*	Setting prohibited

· **VSYN2**, **VSYN1, VSYN0** (bits 6 to 4)
VSYN2, VSYN1, and VSYN0 are bits used to select the voice synthesis algorithm. 4-bit ADPCM2, 8-bit nonlinear PCM, 8-bit straight PCM or 16-bit straight PCM, or HQ-ADPCM can be selected.

VSYN2	VSYN1	VSYN0	Voice synthesis algorithm
0	0	0	Setting prohibited
0	0	1	4-bit ADPCM2
0	1	0	8-bit Nonlinear PCM
0	1	1	8-bit straight PCM
1	0	0	16-bit straight PCM (initial value)
1	0	1	HQ-ADPCM(1/5)
1	1	0	Setting prohibited
1	1	1	Setting prohibited

19.2.7 Volume Setting Register (VVOL)

Address: 0F2B6H
Access: R/W
Access size: 8 bits
Initial value: 09H

	7	6	5	4	3	2	1	0
VVOL	¾	¾	¾	VVOL4	VVOL3	VVOL2	VVOL1	VVOL0
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	0	0	1

VVOL is a special function register (SFR) used to set the volume value.

[Description of Bits]

· **VVOL4**, **VVOL3**, **VVOL2, VVOL1, VVOL0** (bits 4 to 0)
VVOL4, VVOL3, VVOL2, VVOL1, and VVOL0 are bits used to select the value of volume.

VVOL4	VVOL3	VVOL2	VVOL1	VVOL0	Volume [dB]
0	0	0	0	0	+2.98
0	0	0	0	1	+2.70
0	0	0	1	0	+2.40
0	0	0	1	1	+2.10
0	0	1	0	0	+1.78
0	0	1	0	1	+1.45
0	0	1	1	0	+1.11
0	0	1	1	1	+0.76
0	1	0	0	0	+0.39
0	1	0	0	1	+0.00 (initial value)
0	1	0	1	0	- 0.41
0	1	0	1	1	- 0.83
0	1	1	0	0	- 1.28
0	1	1	0	1	- 1.75
0	1	1	1	0	- 2.25
0	1	1	1	1	- 2.77
1	0	0	0	0	- 3.34
1	0	0	0	1	- 3.94
1	0	0	1	0	- 4.58
1	0	0	1	1	- 5.28
1	0	1	0	0	- 6.04
1	0	1	0	1	- 6.87
1	0	1	1	0	- 7.79
1	0	1	1	1	- 8.82
1	1	0	0	0	- 9.99
1	1	0	0	1	- 11.34
1	1	0	1	0	- 12.94
1	1	0	1	1	- 14.90
1	1	1	0	0	- 17.44
1	1	1	0	1	- 21.04
1	1	1	1	0	- 27.31
1	1	1	1	1	OFF

19.2.8 Audio Playback Control Register (VCON)

Address: 0F2B7H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VCON	¾	¾	¾	VSTP	¾	¾	¾	VCEN
R/W	-	-	-	W	-	-	-	R/W
Initial value	0	0	0	0	0	0	0	0

VCON is a special function register (SFR) that controls playback.

[Description of Bits]

· **VCEN** (bit 0)
VCEN is a bit that controls stopping/starting the audio playback function.

VCEN	Description
0	Stops the audio playback function (initial value).
1	Starts the audio playback function.

· **VSTP** (bit 4)
VSTP controls stopping playback during audio playback.

Writing a "1" to this bit stops audio playback and sets the audio operation results to a fixed value of 0000H.
At this time, FIFO is cleared as well. To restart playback, store 4 or more bytes (12 or more bytes when HQ-ADPCM is selected) of audio data in the FIFO data register (VFDAT).

19.2.9 HQ Phrase Stop-Bit Length Register (VHQSBL)

Address: 0F2B2H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
VHQSBL	VHQSBL 4	VHQSBL 3	VHQSBL 2	VHQSBL 1	VHQSBL 0	¾	¾	¾
R/W	R/W	R/W	R/W	R/W	R/W	-	-	-
Initial value	0	0	0	0	0	0	0	0

VHQSBL is a special function register (SFR) used to store the bit length of the final data of a phrase for when HQ-ADPCM is selected.
If the phrase of HQ-ADPCM is generated using the audio code data creation tool, the stop-bit length data (E4–E0) of HQ-ADPCM is stored in the 1st byte of the each HQ-ADPCM waveform data in the audio area. Store that stop bit length data in VHQSBL.

19.2.10 Volume Status Register (VVOLS)

Address: 0F2C0H
Access: R
Access size: 8 bits
Initial value: 09H

	7	6	5	4	3	2	1	0
VVOLS	¾	¾	¾	VVOLS4	VVOLS3	VVOLS2	VVOLS1	VVOLS0
R/W	-	-	-	R	R	R	R	R
Initial value	0	0	0	0	1	0	0	1

VVOLS is a special function register (SFR) that indicates the status of VVOL being reflected during audio playback. The VVOLS read value changes according to the setting of VVOLPS of the audio mode register (VMOD). When VVOLPS is set to "0", the same value as the volume setting register (VVOL) is read. When VVOLPS is set to "1", by comparing VVOLS and VVOL read values, the status can be judged as shown below.

VVOLPS	Description
0	The same value as the VVOL is read from VVOLS (initial value).
1	In case the VVOL and VVOLS read values match: The VVOL setting is reflected in the audio being played. In case the VVOL and VVOLS read values do not match: The VVOL setting is not yet reflected in the audio being played. The next audio playback has not started yet.

19.3 Description of Operation

19.3.1 Audio Playback Operation

When the VCEN bit of the audio playback control register (VCON) is set to "1", the D/A converter enters an operating state. Then, voice synthesis processing and audio data request interrupt processing start.
If there exist 4 or more byes (12 or more bytes when HQ-ADPCM is selected) of audio data to be operated in the FIFO data register (VFDAT) with the VCEN bit set to "1", audio operation starts according to the voice synthesis algorithm and volume selected by the audio data type register (VTYPE) and volume setting register (VVOL).
The audio data request interrupt (VC0INT) occurs when the byte count of audio data becomes smaller than the interrupt request level set by the audio mode register (VMOD). In addition, after the final data of the phrase is stored in the FIFO phrase end data register (VFEDAT), if that final data is fetched into the audio operation circuit, the FIFO becomes enmpty. When the final data is output from teh digital filter with FIFO empty, the audio data request interrupt occurs and the audio status register (VSTAT)'s VDEND bit is set to "1".

To identify the final data of the phrase, store it into VFEDAT. After the final data is operated, the audio operation circuit is initialized and, at the same time, if there exist 4 or more byes (12 or more bytes when HQ-ADPCM is selected) of audio data to be operated in VFDAT, data is updated to the voice synthesis algorithm and sampling furequency stored in VTYPE and playback is started again. At this time, in the case of VVOL setting value is reflected synchronously when the next phrase playback is started, set VVOLPS in the VMOD to "1". In the case of "0", the VVOL setting is immediately reflected.

Figure 19-3 shows the flowchart of audio playback, Figure 19-4 the flowchart of continuous playback, Figures 19-5 to 19-6 the operation timing of audio playback, and Figures 19-7 to 19-8 power-up/power-down timing.

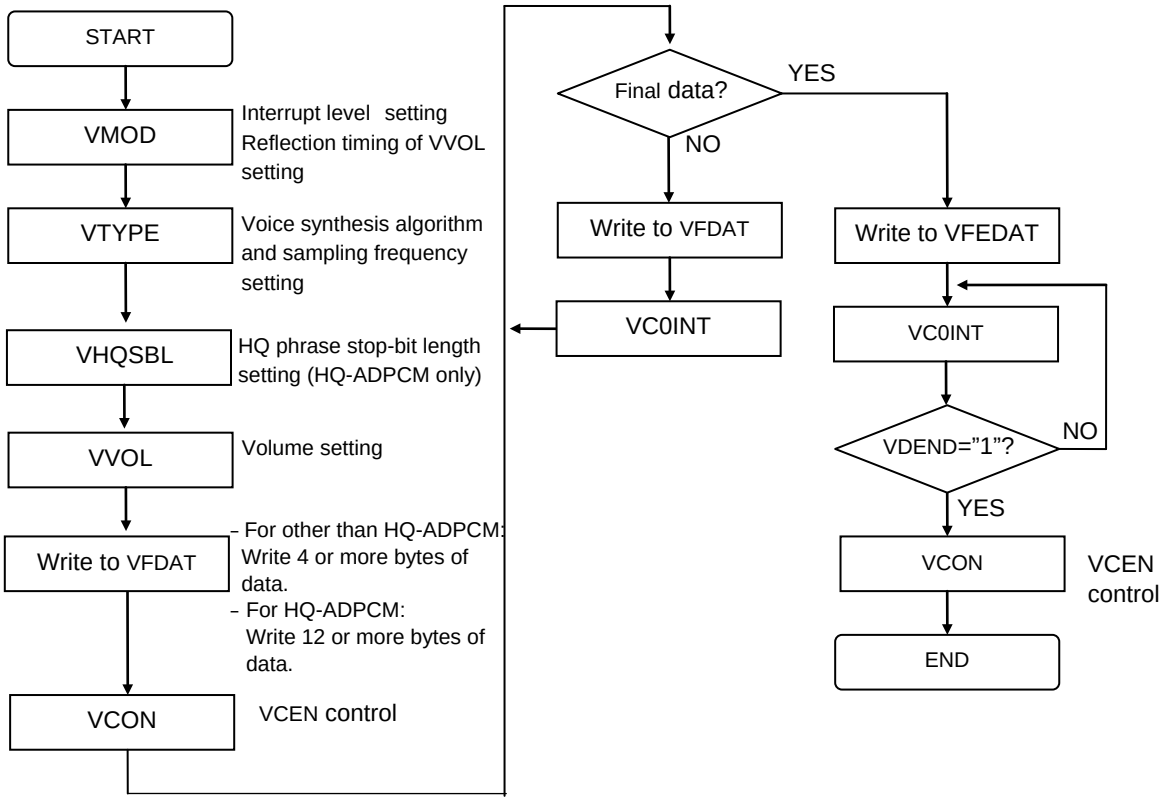
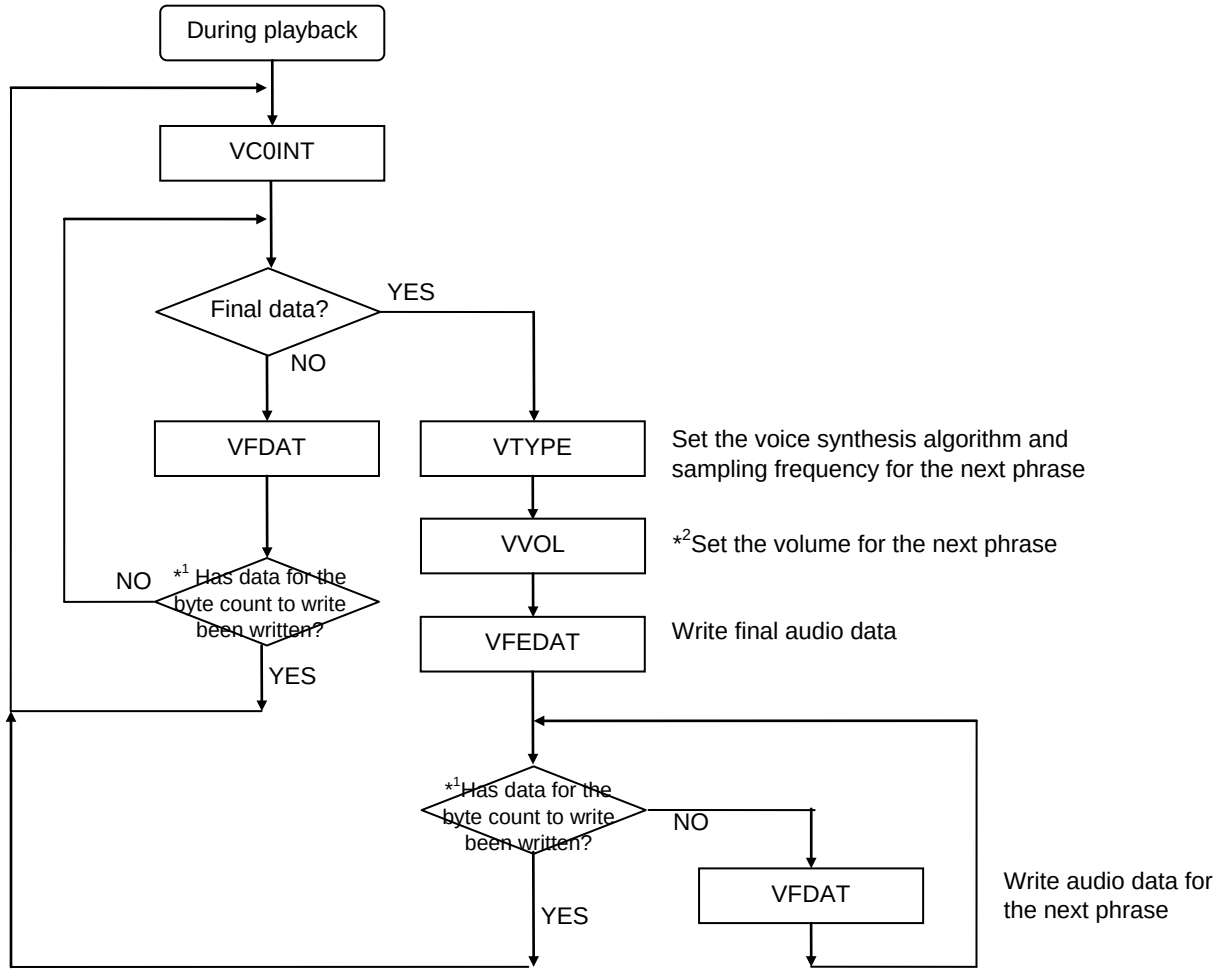


Figure 19-3 Flow of Audio Playback



*1For the byte count to write, determine an arbitrary number of bytes according to the FIFO capacity and the FIFO interrupt request level set by the VFMD1,0 bits of the VMOD register.
*2In the case of VVOL setting value is reflected synchronously when the next phrase playback is started, set VVOLPS in the VMOD to "1". In the case of "0", the VVOL setting is immediately reflected.

Figure 19-4 Flow of Continuous Playback

19.3.2 Timing of Audio Playback Operation

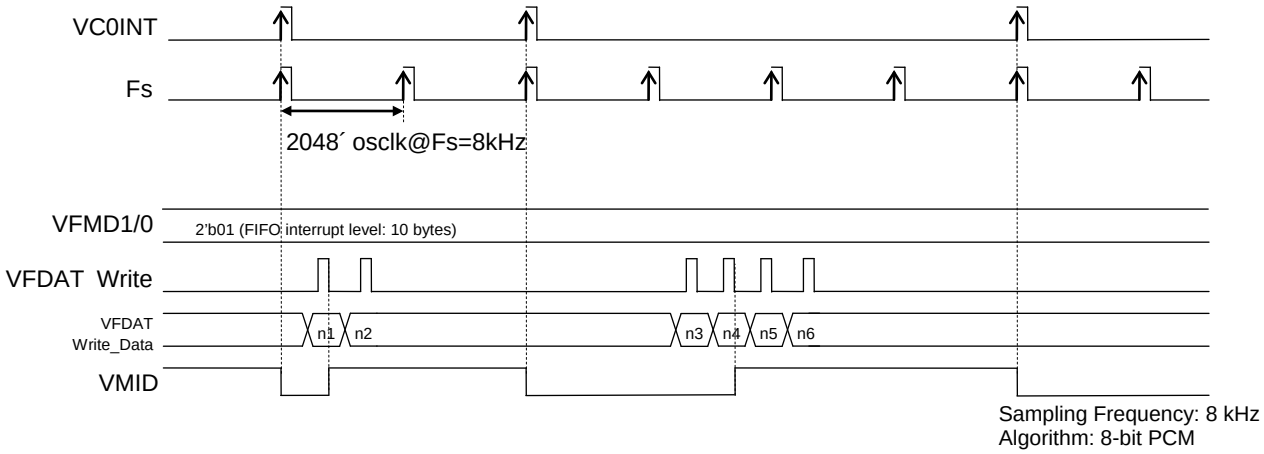


Figure 19-5 Basic Operation Timing of Audio Playback

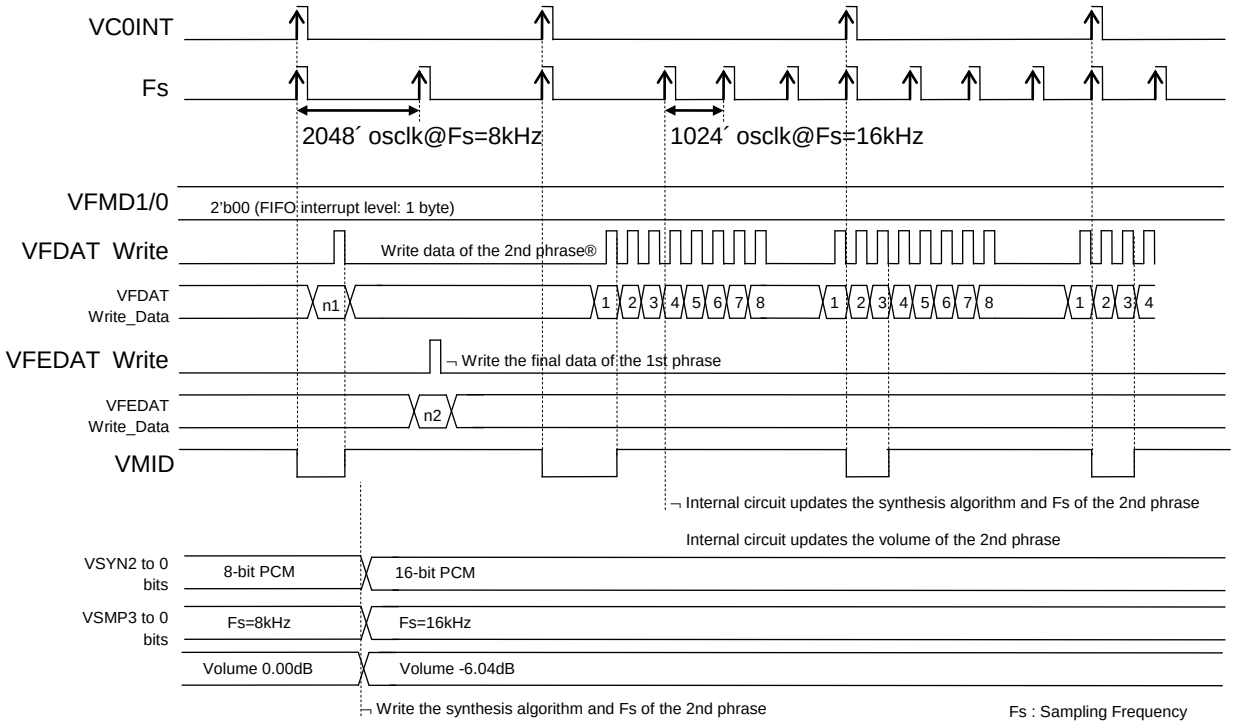


Figure 19-6 Operation Timing of Continuous Playback

Note:
Store the final data of the 1st phrase into the FIFO phrase end data register (VFEDAT).

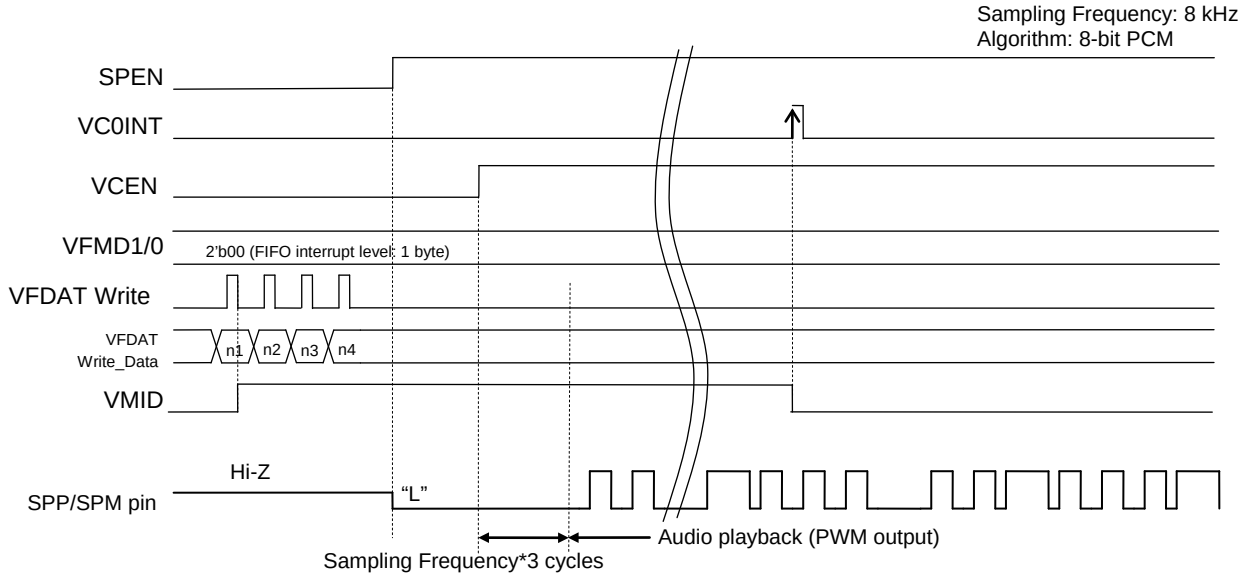


Figure 19-7 Power-Up Timing

If, after the SPEN bit of the speaker amplifier control register (SPCON) is set to "1", and the VCEN bit of the audio playback control register (VCON) is set to "1", there exist 4 or more byes (12 or more bytes when HQ-ADPCM is selected) of audio data to be operated in the FIFO data register (VFDAT) after a lapse of the (Sampling Frequency)*3 cycles, audio operation starts (sequentially from n1 in the figure above) according to the voice synthesis algorithm selected by the audio data type register (VTYPE).

Note:
For the speaker amplifier control, see Chapter 20.

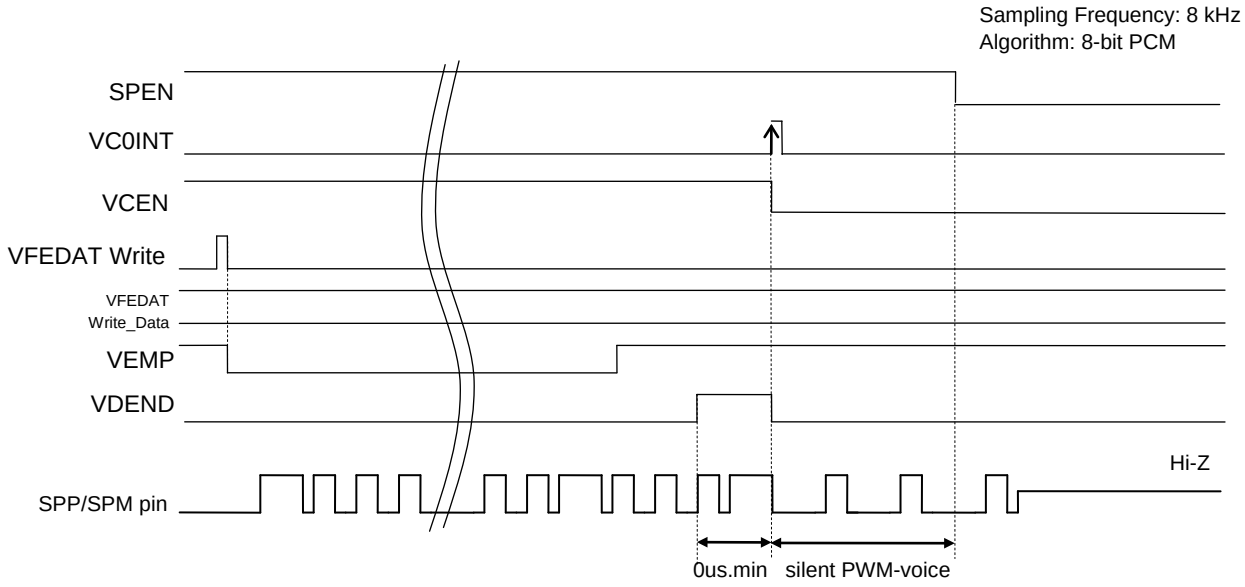


Figure 19-8 Power-Down Timing

Write the final data to the FIFO phrase end data register (VFEDAT). Then, after the VDEND bit of the FIFO status register (VSTAT) goes to "1", set the VCEN bit of the audio playback control register (VCON) to "0".

Note:
For the speaker amplifier control, see Chapter 20.

19.3.3 Audio Code Data Configuration and Audio Data Creation Methods

The data of the audio code consists of the audio management area, the audio area, and the editing ROM area.
The audio management area is an area that manages the phrase information of the code data. It stores data that controls the start address, stop address, and use/unuse of the editing ROM function of the audio data for the specified phrase (phrase address).
The audio area stores actual waveform data.
Editing ROM area stores data for efficient use of audio data. For details, refer to section 19.3.5, Editing ROM Function.
When the editing ROM is not used, the editing ROM area does not exist.

We use our Speech LSI Utility tools to create audio code data. For more information, see Speech LSI Utility User's Manual.

Audio Code Data Configuration

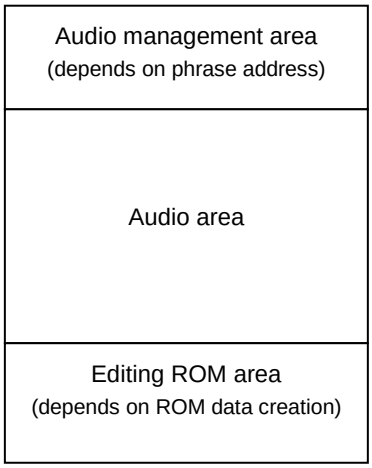


Figure 19-9 Configuration Diagram of Audio Code Data

19.3.4 Playback time and memory capacity

The playback time depends on the memory capacity, sampling frequency, and playback method. The relationship is shown below. However, this is the playback time when the editing ROM function is not used.

$$\text{Playback time} = \frac{1.024 \times ((\text{Audio memory capacity}) - (\text{Audio management area}) - (\text{Audio editing ROM area}))\ (\text{kbit})}{(\text{Sampling frequency(kHz)}) \times (\text{bit length})}\ (\text{sec.})$$

(Bit length of 4-bit ADPCM2, 8-bit PCM and 16-bit PCM is 4, 8, and 16, respectively. 3.2bits for HQ-ADPCM.)

When the 16 Kbyte control program, 16kHz sampling frequency, 4-bit ADPCM2 method, 32 phrases, and editing ROM function are not used, the playback time is about 20.1 seconds. (Unavailable test area 1K byte)

Audio memory capacity = 96 (K bytes)-16 (K bytes)-1 (K bytes) = 79 (K bytes) = 632 (K bits)
Audio management area = 32 (phrase) × 8 (byte) = 256 (byte) = 2 (K bit)

$$\text{Playback time} = \frac{1.024 \times (632-2)(\text{kbit})}{8(\text{kHz}) \times 4(\text{bit})} = 20.1\ (\text{sec.})$$

The playback time of one phrase should be 20ms or more.
The HQ-ADPCM method has an average bit length of 3.2 bits, and under the same conditions, the playback time is approximately 25.2 seconds.

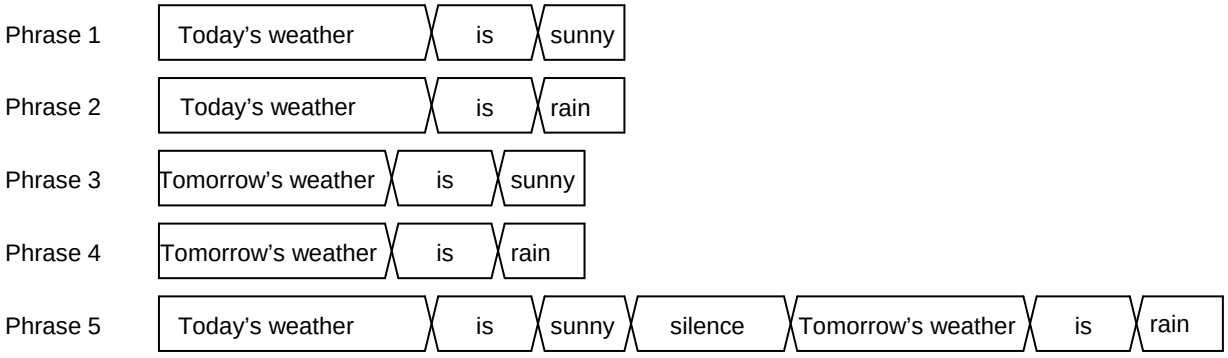
19.3.5 Editing ROM function

Editing ROM function is a function that enables continuous playback of multiple phrases. The following functions can be set using the editing ROM function.

• Continuous playback (The specified number of continuous playback is unlimited. It depends on the flash memory capacity.)
• Silence insertion function (4ms to 1,024ms)

By using the editing ROM function, the flash memory capacity of the audio code data can be used efficiently.
Figure 19-10 shows an example of audio code data configuration when the editing ROM function is used.

Example 1; Phrase configuration when editing ROM function is used



Example 2: Example of data when Example 1 is converted to audio code data

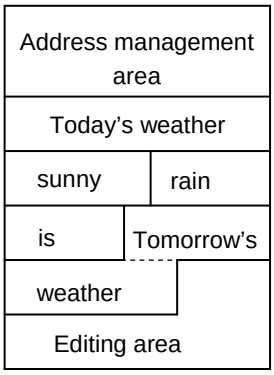


Figure 19-10 Configuration Diagram of Editing ROM Data

Chapter 20

Speaker Amplifier

20. Speaker Amplifier

20.1 Overview

This LSI includes one channel of a mono D-Class speaker amplifier.

20.1.1 Features

· D-Class Speaker amplifier
A high-efficiency D-Class speaker amplifier (1.0W@5.0V) with minimal losses due to LSI heat generation.

· Disconnection detection function
This function detects disconnection of the speaker wiring connected to the speaker amplifier. For example of an alerm device, in order to prevent the speaker from breaking because of disconnection of the speaker wiring, the system can maintain reliability as an alarm device by periodically detecting disconnection.

· Speaker pin short detection function
This function detects a short between the SPP and SPM pins and a short between SPP/SPM pin and GND during audio playback. This function also prevents the current between the SPP and SPM pins when an error occurs in the internal PWM and the PWM is fixed at "H" level. When the short circuit of the speaker pin or the fixation of the "H" level of the internal PWM is detected, the LSI automatically stops audio playback. The speaker pin short detection function prevents excessive current through the speaker amplifier.

20.1.2 Configuration

Figure 20-1 shows the configuration of the speaker amplifier.

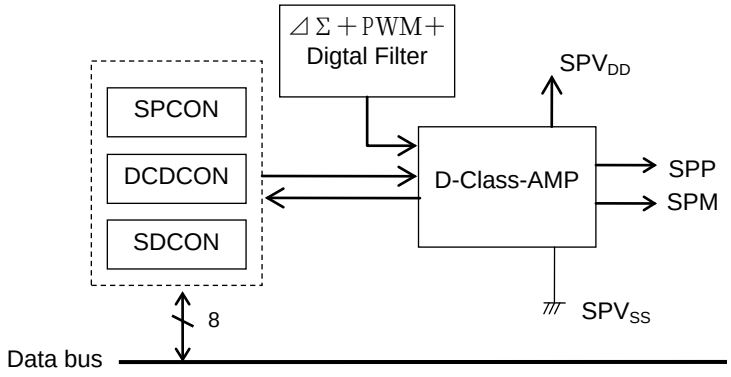


Figure 20-1 Speaker Amplifier Configuration

20.2 Description of Registers

20.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2BCH	Speaker amplifier control register	SPCON	-	R/W	8	00H
0F2BFH	Disconnection detection control register	DCDCON	-	R/W	8	00H
0F2C8H	Speaker pin short detection control register	SDCON	-	R/W	8	00H

20.2.2 Speaker Amplifier Control Register (SPCON)

Address: 0F2BCH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SPCON	¾	¾	¾	¾	¾	¾	SPGAIN	SPEN
R/W	¾	¾	¾	¾	¾	¾	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SPCON is a special function register (SFR) that controls the speaker amplifier.

[Description of Bits]

· **SPEN** (bit 0)
SPEN is a bit that controls the SPP pin and SPM pin.

SPEN	Description
0	SPP/SPM pin: Hi-z output (initial value)
1	SPP/SPM pin: The speaker amplifier starts operating.

· **SPGAIN** (bit 1)
SPGAIN is bit that select input gain of the delta-sigma.

DSGGAIN	Description
0	Gain: 1 time (initial value)
1	Gain: 1.11 time

20.2.3 Disconnection Detection Control Register (DCDCON)

Address: 0F2BFH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DCDCON	DCDF	¾	¾	¾	¾	¾	¾	DCDEN
R/W	R	¾	¾	¾	¾	¾	¾	R/W
Initial value	0	0	0	0	0	0	0	0

DCDCON is a special function register (SFR) that controls the disconnection detection circuit.

[Description of Bits]

· **DCDEN** (bit 0)
DCDEN is a bit that controls ON/OFF of the disconnection detection circuit.
Setting this bit to "1" turns the disconnection detection circuit ON and setting the bit to "0" turns the circuit OFF.

DCDEN	Description
0	Turns the disconnection detection circuit OFF (initial value).
1	Turns the disconnection detection circuit ON.

· **DCDF** (bit 7)
DCDF is a flag that indicates the judgment results by the disconnection detection circuit.
This bit is set to "1" if disconnection has been detected, and "0" if not.

DCDF	Description
0	Disconnection has not been detected (initial value).
1	Disconnection has been detected.

20.2.4 Speaker Pin Short Detection Control Register (SDCON)

Address: 0F2C8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SDCON	SDF	SDA2	SDA1	SDA0	SDD2	SDD1	SDD0	SDEN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SDCON is a special function register (SFR) that controls PWM "H" level fixation detection and the SPP pin and SPM pin short detection circuit.

[Description of Bits]

· **SDEN** (bit 0)

SDEN is a bit that controls ON/OFF of PWM "H" level fixation detection and the SPP pin and SPM pin short detection circuit.

Setting this bit to "1" turns PWM "H" level fixation detection and the speaker pin short detection circuit ON and setting the bit to "0" turns the circuit OFF.

SDEN	Description
0	Turns PWM "H" level fixation detection and the SPP pin and SPM pin short detection circuit OFF (initial value).
1	Turns PWM "H" level fixation detection and the SPP pin and SPM pin short detection circuit ON. Just before this setting is done, be sure to set address "0:0F2C9H" to "04H". Except the value "04H" is set, the operation can not be guaranteed.

Note:
The speaker pin short detection circuit operates during for the playback. The register setting of playback is as follow. PWM "H" level fixation detection and the short detection circuitry of PWM become effective in the state of SPEN="1" and VCEN="1".

Register	SPCON register (Adderss: 0F2BCH)							
bit	7	6	5	4	3	2	1	**0**
bit name	¾	¾	¾	¾	¾	¾	SPGAIN	**SPEN**
value	*	*	*	*	*	*	*	**1**

Register	VCON register (Adderss: 0F2B7H)							
bit	7	6	5	4	3	2	1	**0**
bit name	¾	¾	¾	VSTP	¾	¾	¾	**VCEN**
value	*	*	*	*	*	*	*	**1**

· **SDD0 to 2** (bit 1 to 3)
SDD0 to 2 are bits which sets up interval time of the PWM "H" level fixation detection.

SDD2	SDD1	SDD0	Description	
			SPGAIN = 0	SPGAIN = 1
0	0	0	62.5µs (initial value)	8ms
0	0	1	125µs	12ms
0	1	0	250µs	16ms
0	1	1	500µs	24ms
1	0	0	1ms	32ms
1	0	1	2ms	48ms
1	1	0	4ms	64ms
1	1	1	PWM "H" level fixation detection disable	

· **SDA0 to 2** (bit 4 to 6)
SDA0 to 2 are bits which sets up count of detection of the SPP pin and SPM pin short detection.

SDD2	SDD1	SDD0	Description
0	0	0	initial value, When SDEN is set to "1", change SDA2 to SDA0 value to SDA2=SDA1=1, SDA0=0 (64-time detection) or SDA2=SDA1=SDA0 = 1 (short detection disable).
1	1	0	64-time detection
1	1	1	The SPP pin and SPM pin short detection disable
Others			Prohibited

"C
For "64-time detection", while the short detection circuit is on (SDEN=1), the presence/absence of a short is checked at a sampling cycle of 2us, and when 64 times of consecutive short detection occurs, audio playback stops and the SDF bit is set to "1".

· **SDF** (bit 7)
SDF is a bit that shows the result of the judgement of PWM "H" level fixation detection and the SPP pin and SPM pin short detection.
When PWM "H" level fixation or the SPP pin and SPM pin short is detected, SDF is turnd "H" level. When the SPP pin and SPM pin short is not detected, SDF is turnd "L" level.
If SDF is turned "H" level, the speaker pin short detection interrupt occurs, then PWM circuit is reset.

SDF	Description
0	PWM "H" level fixation detection or the SPP pin and SPM pin short detection is not operating. (initial value).
1	PWM "H" level fixation detection or the SPP pin and SPM pin short detection is operating

Note:
When short detection circuit is enabled (SDEN=1), be sure to select either 64-time detection (SDA2=SDA1=1, SDA0=0) or short detection disable (SDA2=SDA1=SDA0=1).

20.3 Description of Operation

20.3.1 Speaker Amplifier

The speaker amplifier circuit is turned on or off by the SPEN bit of the speaker amplifier control register (SPCON). SPEN is an enable control bit for the SPP/SPM pin of the speaker amplifier. Setting SPEN to "1" turns on the speaker amplifier circuit.

When a PLL oscillation stops in the status of SPEN="1" in more than T_{STOP}, a device begins a reset processing. Please be sure to read the XSTR bit of RSTAT before starting a voice sound reproducing. When the PLL oscillation stop detection reset has occurred on that occasion, please set a XSTR bit to "0."

Setting SPEN to "0" puts the SPP/SPM pin into a Hi-Z state and the supply current of the speaker amplifier circuit becomes zero.

Figure 20-2 shows an example of operation timing.

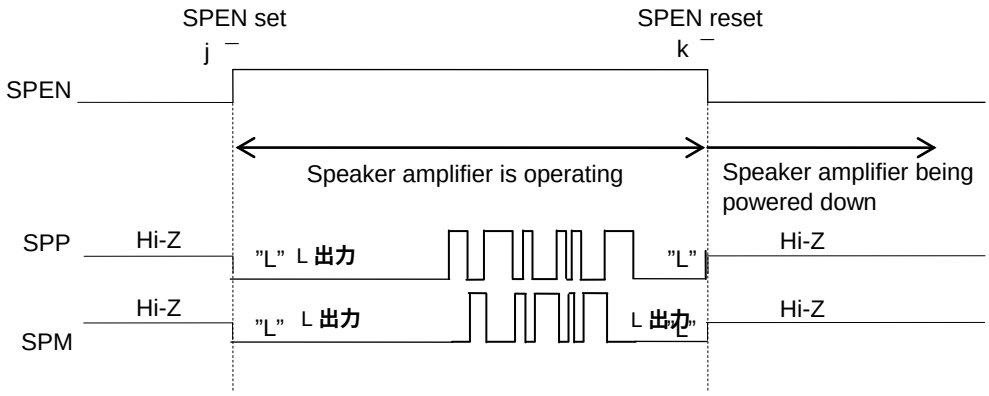


Figure 20-2 Example of Operation Timing

The operation in Figure 20-2 is described below.

j Set SPEN to "1" to turn on the speaker amplifier.
The speaker amplifier starts operating.

k Set SPEN to "0" to turn off the speaker amplifier.
The speaker amplifier stops operating.

20.3.2 Disconnection Detection Circuit

The disconnection detection circuit is turned on or off by the DCDEN bit of the disconnection detection control register (DCDCON). It outputs disconnection detection results to the DCDF bit of DCDCON.
DCDEN is an enable control bit for the disconnection detection circuit. Setting DCDEN to "1" turns on the disconnection detection circuit, and setting it to "0" turns off the circuit, when the supply current of the circuit becomes zero.
DCDF is a flag that indicates the judgment results. When DCDF is "1", it indicates that disconnection has been detected and when "0", it indicates that no disconnection has been detected.
The disconnection detection circuit takes time to stabilize. Read the DCDF bit at least 1 ms after setting DCDEN to "1".
Figure 20-4 shows an example of operation timing.

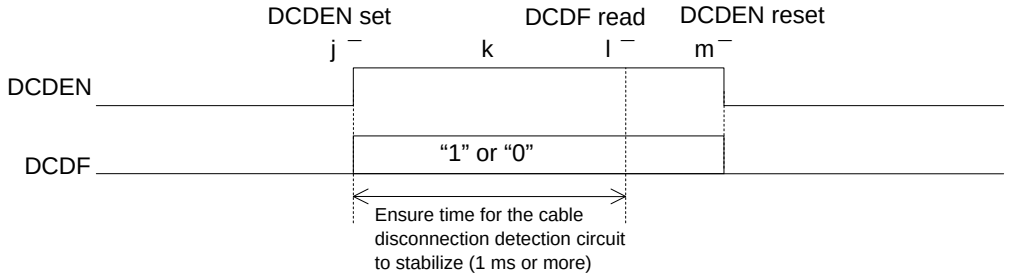


Figure 20-4 Example of Operation Timing

The operation in Figure 20-4 is described below.

- j Set DCDEN to "1" to turn on the disconnection detection circuit.
- k Ensure time for the disconnection detection circuit to stabilize (1 ms or more).
- l Read the judgment result flag (DCDF).
- m Set DCDEN to "0".

Note:
Operate the disconnection detection circuit when the SPEN bit of the speaker amplifier control register (SPCON) is at "0".

20.3.3 Speaker Pin Short Detection Circuit

20.3.3.1 PWM "H" level fixation detection circuit operation

PWM "H" level fixation detection circuit is turned on or off by the SDEN bit of the speaker pin short detection control register (SDCON). It outputs PWM "H" level fixation detection results to the SDF bit of SDCON.
SDEN is an enable control bit for PWM "H" level fixation detection circuit. Setting SDEN to "1" turns on the PWM "H" level fixation detection circuit. SDF is a flag that indicates the judgment results. When SDF is "1", it indicates that PWM "H" level fixation has been detected and when "0", it indicates that PWM "H" level fixation has been detected.
Judgment time of the PWM "H" level fixation detection can be set up by the SDD2 to SDD0 bits.
Figure 20-5 shows an example of operation timing.

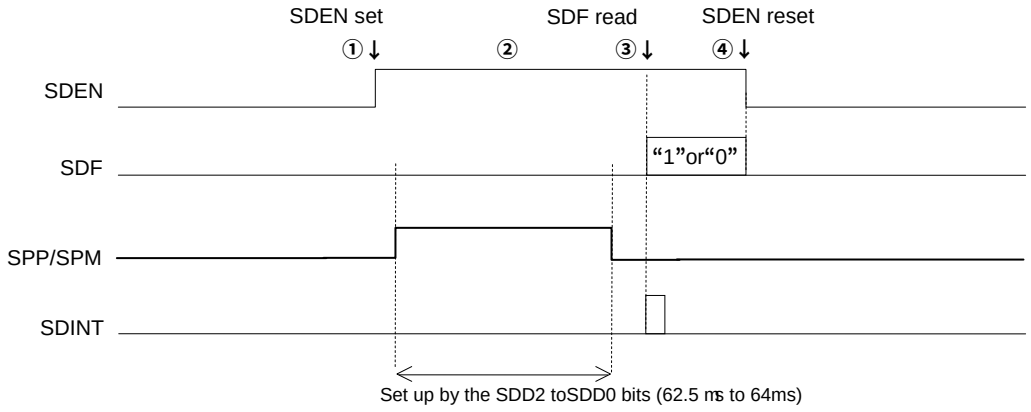


Figure 20-5 Example of Operation Timing

The operation in Figure 20-5 is described below.

j Set SDEN to "1" to turn on the PWM "H" level fixation detection circuit.
k When the PWM "H" level fixation is detected, SDF bit turn "1" after the time whitch was set up by the SDD2 to SDD0 bits.
l Read the judgment result flag (SDF).
m Set SDEN to "0" to turn off the PWM "H" level fixation detection circuit.

20.3.3.2 SPP and SPM terminal of speaker Pin Short Detection Circuit operation

This LSI has a short detection circuit for the SPP pin and SPM pin. This prevents current from SPP/SPM pin to the GND when SPP/SPM pin is short-circuited with GND. when the short of SPP/SPM is detected, the audio playback automatically stopped.
The speaker pin(SPP,SPM) short detection circuit is turned on or off by the SDEN bit of the speaker pin short detection control register (SDCON). It outputs speaker pin short detection results to the SDF bit of SDCON.
SDEN is an enable control bit for the speaker pin short detection circuit. Setting SDEN to "1" turns on the speaker pin short detection circuit, and setting it to "0" turns off the circuit, when the supply current of the circuit becomes zero.
SDF is a flag that indicates the judgment results. When SDF is "1", it indicates that speaker pin short has been detected and when "0", it indicates that speaker pin no short has been detected.
Judgment time of the speaker pin short detection can be set up by the SDA2 to SDA0 bits.
Figure 20-6 shows an example of operation timing.

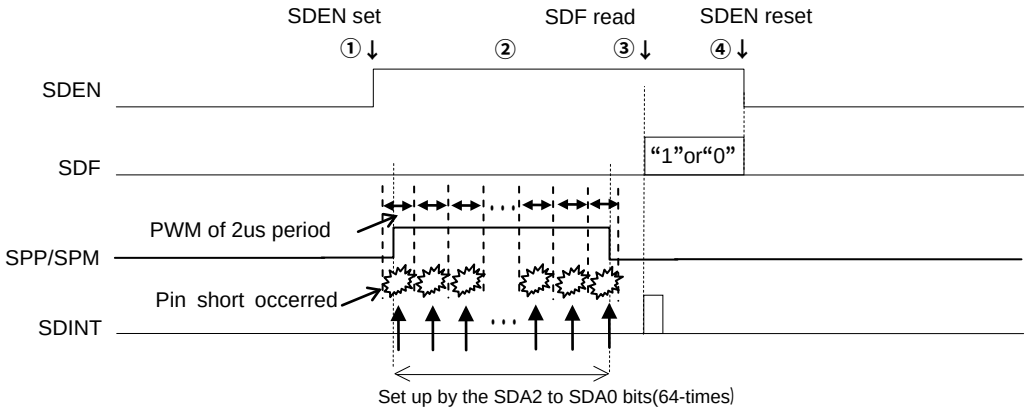


Figure 20-6 Example of Operation Timing

The operation in Figure 20-6 is described below.

j Set SDEN to "1" to turn on the speaker pin short detection circuit.
k When the speaker pin short is detected, SDF bit turn "1" after the count of detection whitch was set up by the SDA2 to SDA0 bits.
l Read the judgment result flag (SDF).
m Set SDEN to "0" to turn off the speaker pin short detection circuit.

Note:
Speaker short detection prevents IC destruction, but the detection circuit is effective to prevent destruction caused by sudden accidents, and is not intended for use in the condition like short detection occurs continuously. Speaker short is detected by monitoring the short current from SPP/SPM terminals. Even if either SPP/SPM terminal is in short condition, in case the SPP/SPM wire impedance is so large that it prevents the short current flows, and the volume setting is so small that the short current is small, SPP/SPM terminal current may NOT cross the threshold of the short detection voltage and the speaker short may NOT be detected. Therefore, please make sure to evaluate and use it in the usage conditions and environment.

Chapter 21

Flash memory self rewriting function

21. Flash memory self rewriting function

21.1 Overview

This LSI includes the flash memory self rewriting function that rewrites the content of the flash memory (Data memory space (2K bytes : 512 bytes * 4 sectors)) using special functional register (SFR) programmatically.

21.1.1 Features

- Maximum rewrite count : 10000 times V_{DD}=2.2V to 5.5V@-40 to 70℃
- Sector erase : 256 words (512bytes) erase
- Block erase : 1K words (2K bytes) erase
- Data writing : 1-word writing

21.2 Description of Registers

21.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0E0H	Flash address register L	FLASHAL	FLASHA	R/W	8/16	00H
0F0E1H	Flash address register H	FLASHAH		R/W	8	00H
0F0E2H	Flash data register L	FLASHDL	FLASHD	R/W	8/16	00H
0F0E3H	Flash data register H	FLASHDH		R/W	8	00H
0F0E4H	Flash control register	FLASHCON	−	W	8	00H
0F0E5H	Flash accepter	FLASHACP	−	W	8	00H
0F0E6H	Flash segment register	FLASHSEG	−	R/W	8	00H
0F0E7H	Flash self register	FLASHSLF	−	R/W	8	00H
0F0E8H	Flash protection register	FLASHPRT	−	R/W	8	00H

21.2.2 Flash address register L,H (FLASHAL,H)

Address: 0F0E0H
Access: R/W
Access size: 8 bits/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHAL	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

Address: 0F0E1H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHAH	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHAL and FLASHAH are the special function registers (SFRs) that set the flash memory rewriting address.

[Description of Bits]

- **FA7 to FA0** (bits 7 to 0)
  The FA7 to FA0 bits are used to set the lower address for 1-word write.
  Note that the bit 0 is fixed to 0 and cannot be written.

- **FA15 to FA8** (bits 7 to 0)
  The FA15 to FA8 bits are used to set the upper address for block erase, or sector erase, or 1-word write.
  The block specified by the flash segment register (FSEG0, FSEG1) and the FA15 to FA8 bits is erased.
  Table21-1 show the address setting values for sector erase.
  Table21-2 show the address setting values for block erase.

Table 21-1 Address Setting Values for Sector Erase.

Sector erase area		FLASHSEG		FLASHAH							
Segment	address	FSEG1	FSEG0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 2	0000H to 01FFH	1	0	0	0	0	0	0	0	0	0
	0200H to 03FFH	1	0	0	0	0	0	0	0	1	0
	0400H to 05FFH	1	0	0	0	0	0	0	1	0	0
	0600H to 07FFH	1	0	0	0	0	0	0	1	1	0

Table 21-2 Address Setting Values for Block Erase.

Block erase area		FLASHSEG		FLASHAH							
Segment	address	FSEG1	FSEG0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 2	0000H to 07FFH	1	0	0	0	0	0	0	0	0	0

21.2.3 Flash Data Register L,H (FLASHDL,H)

Address: 0F0E2H
Access: R/W
Access size: 8 bits/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHDL	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F0E3H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHDH	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHDL and FLASHDH are special function registers (SFRs) that set the flash memory write data.

Description of Bits

- **FD7 to FD0** (bits 7 to 0)
  The FD7 to FD0 bits are used to set the lower write data for 1-word write.

- **FD15 to FD8** (bits 7 to 0)
  The FD15 to FD8 bits are used to set the upper write data for 1-word write.
  Writing to FD15 to FD8 starts the 1-word write.
  The CPU stops instructions during a flash memory write operation. After the completion of writing, the CPU restarts from the next instruction.

Notes:
· Erase the memory of the target addresses in advance. The memory of an overwritten address is not guaranteed.
· Writing to FLASHDH starts the 1-word write. Write data to FLASHDL and FLASHDH in this order.
During writing to flash memory, the peripheral circuits continue an operation and the interrupts are on hold.

21.2.4 Flash Control Register (FLASHCON)

Address: 0F0E4H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHCON	—	—	—	—	—	—	FSERS	FERS
R/W	—	—	—	—	—	—	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHCON is a write-only special function register (SFR) to control the block erase or the sector erase for the flash memory rewrite.

Description of Bits

- **FERS** (bit 0)
  The FERS bit is used to start the block erase.
  Setting the FERS bit to "1" erases the block specified by the FLASHSEG register and FLASHAH register. This bit is automatically set to "0" after completing the erase.
  The CPU stops executing instructions during a flash memory erase operation. After the completion of erasing, the CPU restarts executing from the next instruction.

- **FSERS** (bit 1)
  The FSERS bit is used to start the sector erase.
  Setting the FSERS bit to "1" erases the block specified by the FLASHSEG register and FLASHAH register. This bit is automatically set to "0" after completing the erase.
  The CPU stops executing instructions during a flash memory erase operation. After the completion of erasing, the CPU restarts executing from the next instruction.

FSERS	FERS	Description
0	0	Erase function is not started (initial value)
0	1	Start block erase
1	0	Start sector erase
1	1	Start block erase

Note:
During the block erase and sector erase operation, the peripheral circuits continue an operation and the interrupts are on hold.

21.2.5 Flash Acceptor (FLASHACP)

Address: 0F0E5H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHACP	fac7	fac6	fac5	fac4	fac3	fac2	fac1	fac0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHACP is a write-only special function register (SFR) to control the block erase and the sector erase for the flash memory rewrite or enable/disable the 1-word write operation.

Description of Bits

- **fac7 to fac0** (bits 7 to 0)
  The fac7 to fac0 bitsrs are used to restrict the erase operation or 1-word write operation in order to prevent an unintended operation.
  Writing "0FAH" and "0F5H" to FLASHACP in this order enables a one-time erase or 1-word write. For subsequent block erases or sector erases or 1-word writes, "0FAH" and "0F5H" must be written to FLASHACP each time.
  Even if another instruction is inserted between "0FAH" and "0F5H" written to FLASHACP, the erase operation or 1-word write is enabled. Note that, if data other than "0F5H" is written to FLASHACP after "0FAH" is written, the "0FAH" write processing becomes invalid. So, "0FAH" must be rewritten at first.

21.2.6 Flash Segment Register (FLASHSEG)

Address: 0F0E6H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSEG	—	—	—	—	—	—	FSEG1	FSEG0
R/W	—	—	—	—	—	—	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSEG is a special function register (SFR) that sets the flash memory rewrite segment address.

Description of Bits

- **FSEG1, FSEG0** (bits 1 to 0)
  The FSEG0 and FSEG1 bits are used to set the flash segment address.
  Thease bits are used to specify a flash memory address for block erase, sector erase or 1-word write in combination with flash address registers (FLASHAL, FLASHAH).

FSEG1	FSEG0	Description
0	0	Invalid (initial value)
0	1	Invalid
1	0	Select segment 2
1	1	Invalid

21.2.7 Flash Self Register (FLASHSLF)

Address: 0F0E7H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSLF	—	—	—	—	—	—	—	FSELF
R/W	—	—	—	—	—	—	—	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSLF is a special function register (SFR) that controls the flash memory self rewrite function.

Description of Bits

- **FSELF** (bit 0)
  Setting the FSELF bit to "1" the flash self rewriting function is enabled.

FSELF	Description
0	Flash-memory self rewriting function: Disenable (initial value)
1	Flash-memory self rewriting function: Enable

21.2.8 Flash Protection Register (FLASHPRT)

Address: 0F0E8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHPRT	—	—	—	—	FPRT3	FPRT2	FPRT1	FPRT0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHPRT is a special function register (SFR) that controls sector erase, block erase and 1-word writing of 0000H to 01FFH, 0200H to 03FFH, 0400H to 05FFH, 0600H to 07FFH in the segment 2.

Description of Bits

- **FPRT0** (bit 0)
  FPRT0 is the bit that controls sector erase and the 1-word writing of 0000H to 01FFH in the segment 2. When "1" is written in FPRT0, FPRT0 is set to "1" and sector erase of 0000H to 01FFH in the subsequent segments 2, block erase and 1-word writing become invalid. It is not set to "0", although "0" is written in FPRT0 after writing "1" in FPRT0.

FPRT0	Description
0	Sector erase of 0000H to 01FFH in the segment 2, block erase and 1 word writing: Enable (initial value)
1	Sector erase of 0000H to 01FFH in the segment 2, block erase and 1 word writing: Disenable

- **FPRT1** (bit 1)
  FPRT1 is the bit that controls sector erase and the 1-word writing of 0200H to 03FFH in the segment 2. When "1" is written in FPRT1, FPRT1 is set to "1" and sector erase of 0200H to 03FFH in the subsequent segments 2, block erase and 1-word writing become invalid. It is not set to "0", although "0" is written in FPRT1 after writing "1" in FPRT1.

FPRT1	Description
0	Sector erase of 0200H to 03FFH in the segment 2, block erase and 1 word writing: Enable (initial value)
1	Sector erase of 0200H to 03FFH in the segment 2, block erase and 1 word writing: Disenable

- **FPRT2**(bit 2)
  FPRT2 is the bit that controls sector erase and the 1-word writing of 0400H to 05FFH in the segment 2. When "1" is written in FPRT2, FPRT2 is set to "1" and sector erase of 0400H to 05FFH in the subsequent segments 2, block erase and 1-word writing become invalid. It is not set to "0", although "0" is written in FPRT2 after writing "1" in FPRT2.

FPRT2	Description
0	Sector erase of 0400H to 05FFH in the segment 2, block erase and 1 word writing: Enable (initial value)
1	Sector erase of 0400H to 05FFH in the segment 2, block erase and 1 word writing: Disenable

· **FPRT3**(bit 3)
FPRT3 is the bit that controls sector erase and the 1-word writing of 0600H to 07FFH in the segment 2. When "1" is written in FPRT3, FPRT3 is set to "1" and sector erase of 0600H to 07FFH in the subsequent segments 2, block erase and 1-word writing become invalid. It is not set to "0", although "0" is written in FPRT3 after writing "1" in FPRT3.

FPRT3	Description
0	Sector erase of 0600H to 07FFH in the segment 2, block erase and 1 word writing: Enable (initial value)
1	Sector erase of 0600H to 07FFH in the segment 2, block erase and 1 word writing: Disenable

Note:
After writing "1" in any one bit of flash protection register (FLASHPRT), block erase to 0000H to 07FFH of the segment 2 becomes invalid.

21.3 Description of Operation

When using the flash memory self rewrite function, prepare the program for rewrite in advance on a program code area with addresses that are not used for sector erase, block erase or 1-word write.
The flash memory self rewrite function includes the sector erase function that erases 512 bytes, the block erase function that erases 2K bytes and the 1-word write function that writes by 1 word (2 bytes).
It also includes the flash rewrite acceptor function which restricts the flash memory rewrite operation, to prevent an improper rewriting of the flash memory. Writing "0FAH" and "0F5H" to the flash acceptor (FLASHACP) in this order enables a one-time block erase or sector erase or 1-word write.
The flash memory rewrite operation is not supported when the system clock is low-speed clock.
The note of the system clock during rewriting the flash memory is shown below Table 21-2.
Table 21-2 shows the specification of flash memory rewriting.

Table 21-2 Specification of flash memory rewriting

Item		Specification
Maximum rewrite count (Data memory space (512bytes * 4 sectors))		10000 times
Operating temperature		-40℃ to 70℃
Operating voltage	V_{DD}	2.2V to 5.5V
Sector blanking time		(Max.) 50ms
Block blanking time		(Max.) 50ms
1 word (16bits) writing		(Max.) 40μs

Note:
Please use it, where High-speed clock (HSCLK) oscillation of Frequency control register(FCON1) is enabled and HSCLK is chosen as a system clock.

21.3.1 Sector Erase Function

This function erases the flash memory data by the sector (512 bytes).
Erase operation becomes enabled by writing "01H" to the flash self register. Write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the block address in the flash segment register (FLASHSEG) and the flash address register H (FLASHAH). Then, write "1" to the FERS bit of the flash control register (FLASHCON) to erase the data in the block (512 bytes) specified by FLASHSEG and FLASHAH.
During the erase, the CPU is stopped. When the erase is completed, the program is restarted from the instruction following the one that set the FERS bit of the FLASHCON to "1".

Figure 21-1 shows the sector erase flow.

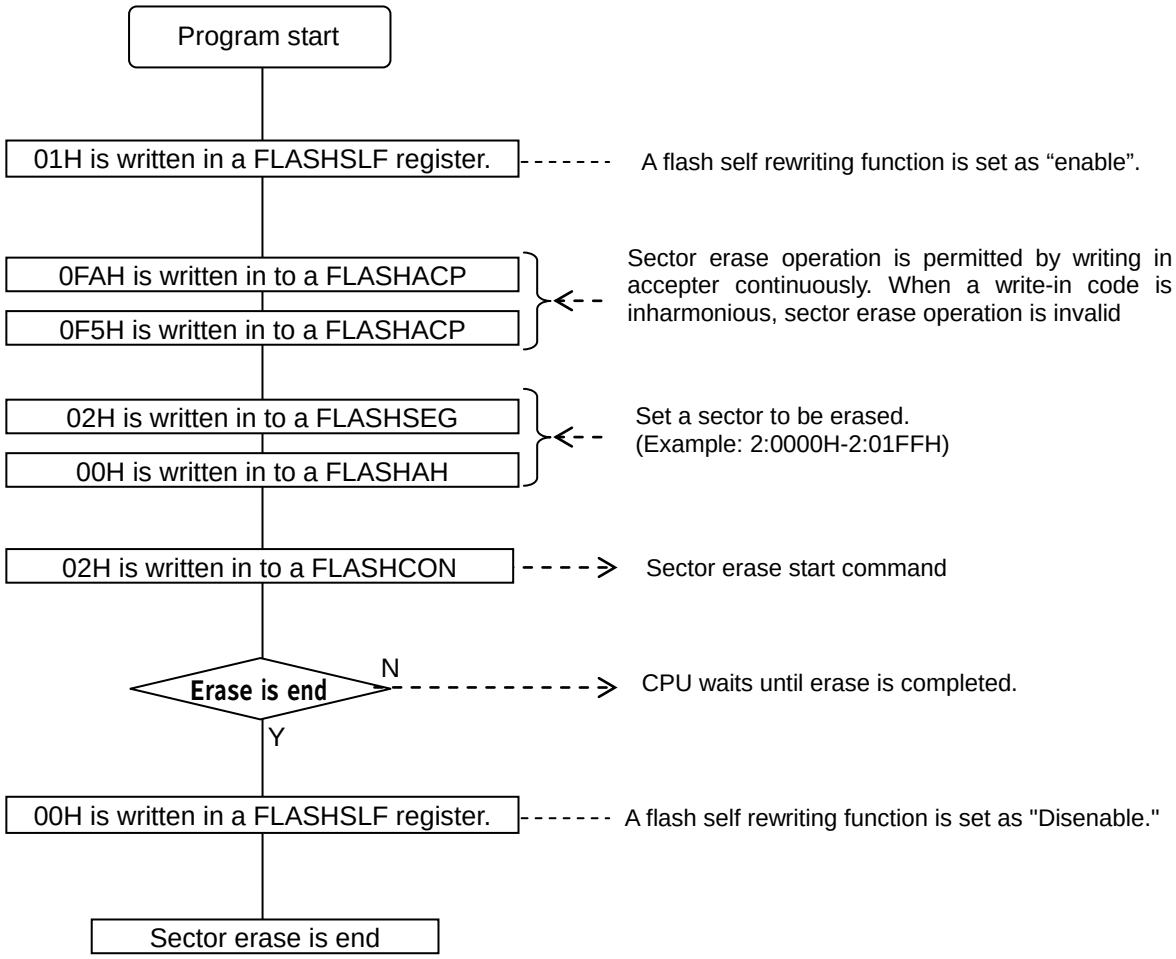


Figure 21-1 Sector erase flow

Figure 21-2 shows a sample program of sector erase.

```
LEA     offset FLASHAH          ; EA¬ FLASHAH address
MOV     R0,   #0FAH             ; Flash acceptor enable data
MOV     R1,   #0F5H             ; Flash acceptor enable data
MOV     R4,   #(offset FLASHACP)&0FFH
MOV     R5,   #(offset FLASHACP)>>8     ; ER4¬ FLASHACP address
  :
(Set the erase start sector address in R9)
  :
SB      FSELF                   ; Enable flash self rewritting

ST      R0,   [ER4]             ; Enable flash acceptor
ST      R1,   [ER4]             ; Enable flash acceptor

    MOV     R2,   #02H          ; Segment setting data (example:segment 2)
    ST      R2,   FLASHSEG      ; Set segment

ST      R9,   [EA]              ; Set sector address

MOV     R2,   #02H              ; Sector erase setting data
ST      R2,   FLASHCON          ; Start sector erase
NOP                             ; * Always set
NOP                             ; * Always set

RB      FSELF                   ; Disenable flash self rewritting
```

Figure 21-2 Sample Program of Sector Erase

Notes:

· If you erase data being used by the running program, the program would malfunction. Erase a sector unrelated to the operation of the program.

· Be sure to set the NOP instruction twice or more, following the sector erase start instruction.

· Use it with high-speed clock oscillation (HSCLK) enabled by setting the ENOSC bit and the SYSCLK bit of the frequency control register (FCON1) to "1", and with HSCLK selected as system clock.

· During sector erase, the CPU is in a wait state for max.85ms. Clear the WDT counter in a proper timing, because the peripheral circuits continue to work.

· After writing "1" in FPRT0 bit of flash protection register (FLASHPRT), sector erase to 0000H to 01FFH of the segment 2 becomes invalid.

· After writing "1" in FPRT1 bit of flash protection register (FLASHPRT), sector erase to 0200H to 03FFH of the segment 2 becomes invalid.

· After writing "1" in FPRT2 bit of flash protection register (FLASHPRT), sector erase to 0400H to 05FFH of the segment 2 becomes invalid.

· After writing "1" in FPRT3 bit of flash protection register (FLASHPRT), sector erase to 0600H to 07FFH of the segment 2 becomes invalid.

21.3.2 Block Erase Function

This function erases the flash memory data by the block (2K bytes).
Erase operation becomes enabled by writing "01H" to the flash self register.Write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the block address in the flash segment register (FLASHSEG) and the flash address register H (FLASHAH). Then, write "1" to the FERS bit of the flash control register (FLASHCON) to erase the data in the block (2K bytes) specified by FLASHSEG and FLASHAH.
During the erase, the CPU is stopped. When the erase is completed, the program is restarted from the instruction following the one that set the FERS bit of the FLASHCON to "1".
Figure 21-3 shows the block erase flow.

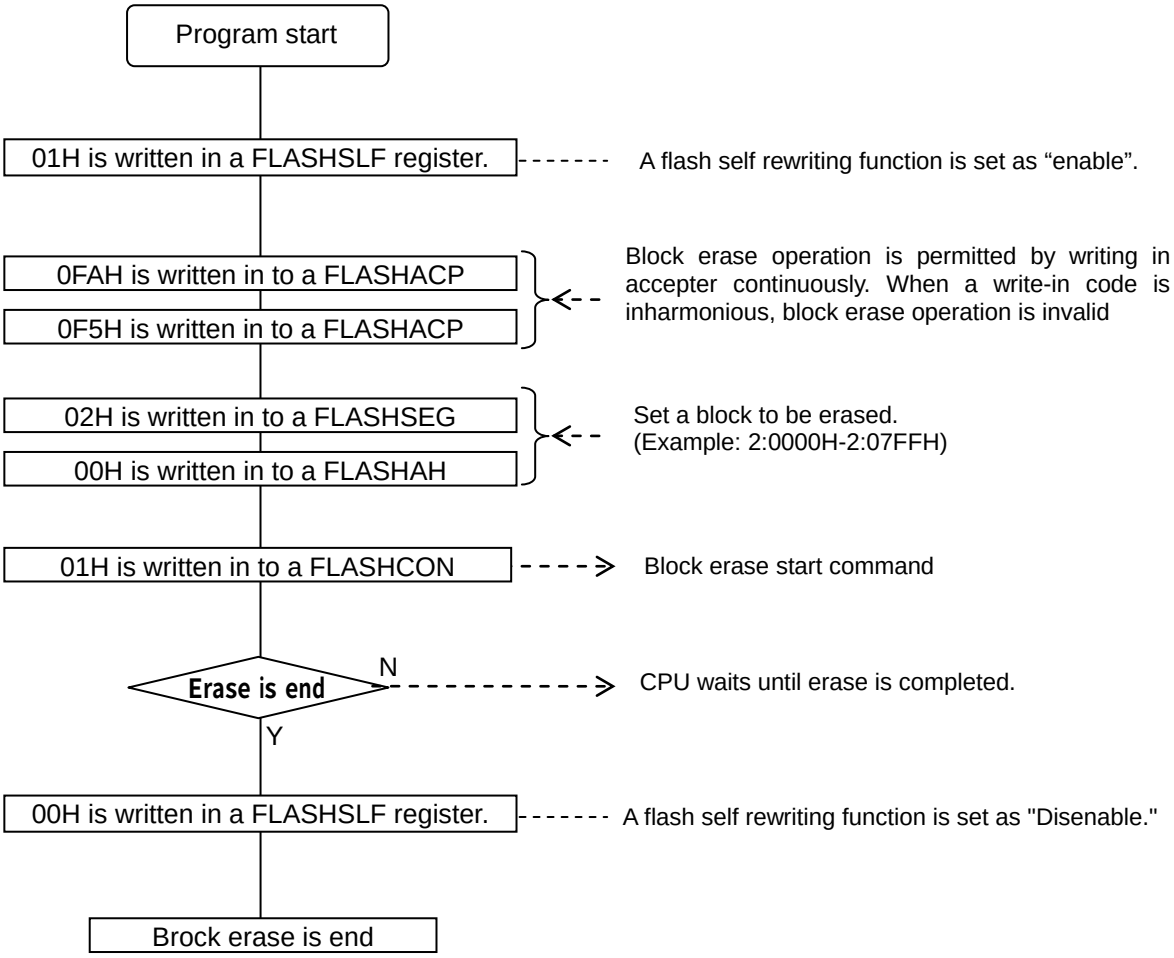


Figure 21-3 Block erase flow

Figure 21-4 shows a sample program of block erase.

```
LEA     offset FLASHAH          ; EA¬ FLASHAH address
MOV     R0,   #0FAH         ; Flash acceptor enable data
MOV     R1,   #0F5H         ; Flash acceptor enable data
MOV     R4,   #(offset FLASHACP)&0FFH
MOV     R5,   #(offset FLASHACP)>>8     ; ER4¬ FLASHACP address
  :
(Set the erase start block address in R9)
  :
SB      FSELF                       ; Enable flash self rewritting

ST      R0,   [ER4]             ; Enable flash acceptor
ST      R1,   [ER4]             ; Enable flash acceptor

MOV     R2,   #02H              ; Segment setting data (example:segment 2)
ST      R2,   FLASHSEG          ; Set segment

ST      R9,   [EA]              ; Set block address

MOV     R2,   #01H              ; Block erase setting data
ST      R2,   FLASHCON          ; Start block erase
NOP                                 ; * Always set
NOP                                 ; * Always set
RB      FSELF                       ; Disenable flash self rewritting
```

Figure 21-4 Sample Program of Block Erase

Notes:

· If you erase data being used by the running program, the program would malfunction. Erase a block unrelated to the operation of the program.

· Be sure to set the NOP instruction twice or more, following the block erase start instruction.

· Use it with high-speed clock oscillation (HSCLK) enabled by setting the ENOSC bit and the SYSCLK bit of the frequency control register (FCON1) to "1", and with HSCLK selected as system clock.

· During block erase, the CPU is in a wait state for max.85ms. Clear the WDT counter in a proper timing, because the peripheral circuits continue to work.

· After writing "1" in any one bit of FPRT0 to FPRT3 in flash protection register (FLASHPRT), block erase to 0000H to 07FFH of the segment 2 becomes invalid.

21.3.3 1-word Write Function

This function writes data to the flash memory by the one word (2 bytes).
Write operation becomes enabled by writing "01H" to the flash self register. Write "0FAH" and "0F5H" to the flash acceptor (FLASHACP) and set the address in the flash segment register (FLASHSEG) and the flash address register L, H (FLASHAL,H). Then, write data to the flash data register L, H (FLASHDL,H) to write the data in the address specified by FLASHSEG and FLASHAL, H.
During the 1-word write, the CPU is stopped. When the write is completed, the program is restarted from the instruction following the write to FLASHDH instruction.
For an example of estimation for writing time (Figure 21-6), data preparation and verify need to take about 4µs per one-word(two bytes) write when the CPU runs at high-speed (8.192MHz) and wait time for writing Flash memory is max.40µs, therefore it takes about (4µs+40µs) x 10 = 440µs at maximum for writing 10 words(20 bytes).
Fig. 21-5 shows a 1-word write flow.

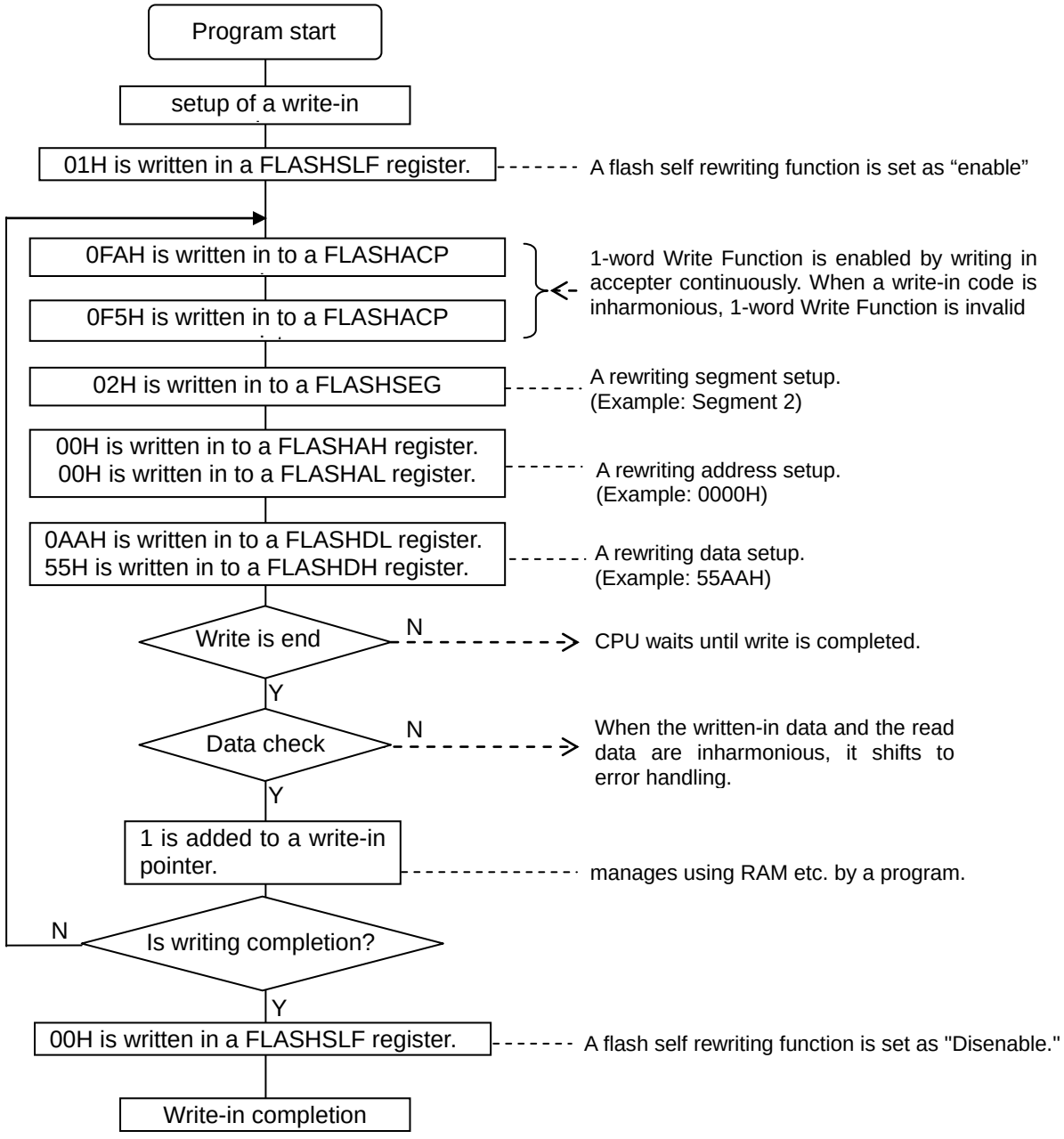


Figure 21-5 1-word Write flow

Figure 21-6 shows a sample program of 1-word write.

```
        LEA     offset FLASHAL              ; EA¬ FLASHAL address
        MOV     R0,   #0FAH             ; Flash acceptor enable data
        MOV     R1,   #0F5H             ; Flash acceptor enable data
        MOV     R2,   #02H              ; Address increment data
        MOV     R3,   #01H
        MOV     R4,   #(offset FLASHACP)&0FFH
        MOV     R5,   #(offset FLASHACP)>>8         ; ER4¬ FLASHACP address
        :
        (Set the write start address in ER8)
        (Set the write end address in ER12)
        :
        SB      FSELF                       ; Enable flash self rewritting
MARK:
        :
        (Set the write data in ER10)
        :
        ST      R0,   [ER4]             ; Enable flash acceptor
        ST      R1,   [ER4]             ; Enable flash acceptor
        MOV     R2,   #02H              ; Segment setting data (example:segment 2)
        ST      R2,   FLASHSEG          ; Set segment
        ST      XR8,    [EA]                ; Set address and data, start 1-word write
        NOP                                 ; * Always set
        NOP                                 ; * Always set

        L       ER14,   [ER8]               ; Load data
        CMP     ER14,   ER10                ; Check data
        BNE     ERROR                       ; Go to error routine on error

        ADD     ER8,    ER2                 ; Increment address
        CMP     ER8,    ER12
        BLE     MARK                        ; Compare addresses

        RB      FSELF                       ; Disenable flash self rewritting
```

Figure 21-6 Sample Program of 1-word Write

Notes:

· If you erase data being used by the running program, the program would malfunction. Erase a block unrelated to the operation of the program.

· Be sure to set the NOP instruction twice or more, following the write to FLASHDH instruction.

· Use it with high-speed clock oscillation (HSCLK) enabled by setting the ENOSC bit and the SYSCLK bit of the frequency control register (FCON1) to "1", and with HSCLK selected as system clock.

· During 1-word write, the CPU is in a wait state for max.40μs. Clear the WDT counter in a proper timing, because the peripheral circuits continue to work.

· After writing "1" in FPRT0 bit of flash protection register (FLASHPRT), 1-word Write Function to 0000H to 01FFH of the segment 2 becomes invalid.

· After writing "1" in FPRT1 bit of flash protection register (FLASHPRT), 1-word Write Function to 0200H to 03FFH of the segment 2 becomes invalid.

· After writing "1" in FPRT2 bit of flash protection register (FLASHPRT), 1-word Write Function to 0400H to 05FFH of the segment 2 becomes invalid.

· After writing "1" in FPRT3 bit of flash protection register (FLASHPRT), 1-word Write Function to 0600H to 07FFH of the segment 2 becomes invalid.

21.3.4 Notes in Use

In case an instantaneous power failure happened or the operation is terminated forcibly by a reset during block erase or sector erase or 1-word write, the flash memory data can not be guaranteed. Erase the block or the sector and rewrite the block or the sector.
In case the LSI did not start up by the failures that an instantaneous or a forced power failure happened, during rewriting of block or sector containing 0:0000H in the program area, rewrite the program by using the on-chip debug emulator (EASE1000 V2).

Chapter 22

Power Supply Circuit

22. Power Supply Circuit

22.1 Overview

This LSI incorporates a regulated power supply circuit for the internal logic and oscillation circuit (VRL).
For the circuit configuration of the power supplies for the speaker circuit (SPV_{DD}, SPV_{SS}), see Chapter 20, "Speaker Amplifier".

22.1.1 Features

· VRL outputs the operating voltage, V_{DDL}, of the internal logic, oscillation circuit (PLL oscillation, RC oscillation), program memory, data memory.

22.1.2 Configuration

Figure 22-1 shows the configuration of the power supply circuit.

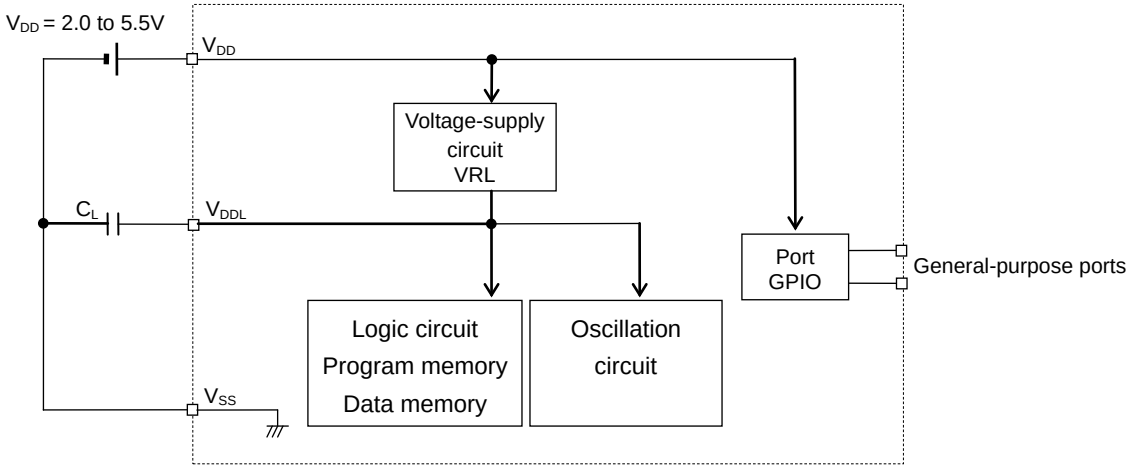


Figure 22-1 Configuration of Power Supply Circuit

22.1.3 List of Pins

Pin name	I/O	Description
V_{DDL}	¾	Positive power supply pin for the internal logic circuits

22.2 Description of Operation

After power on, V_{DDL} reaches approx. 1.55V in every operation mode.

Figure 22-2 shows the operation waveforms of the power supply circuit.

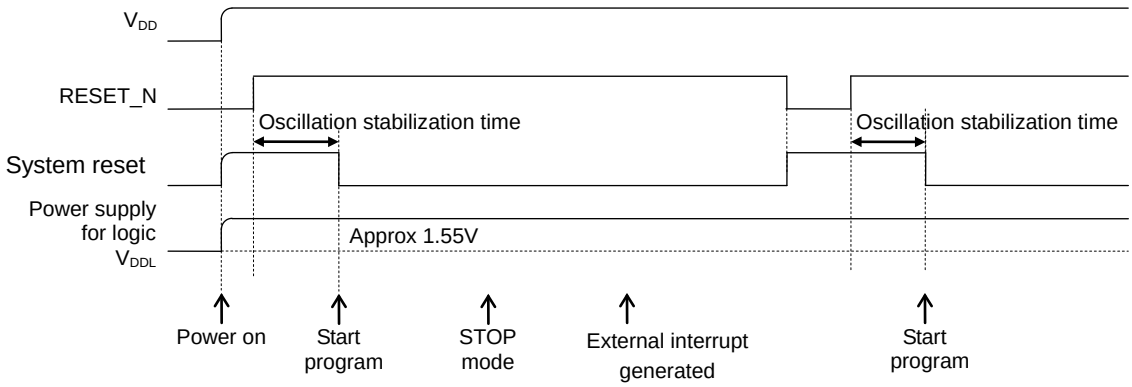


Figure 22-2 Waveforms of Power Supply Circuit Operation

Chapter 23

On-Chip Debug Function

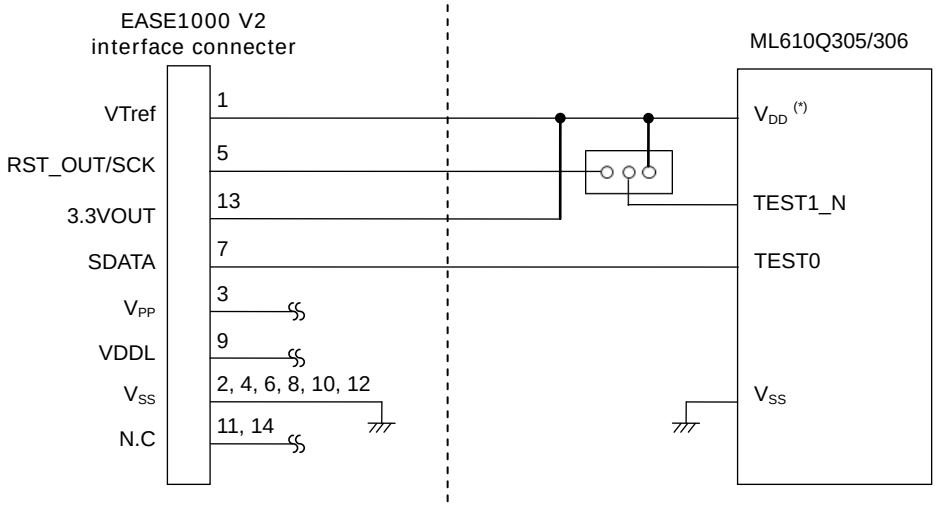
23. On-Chip Debug Function

23.1 Overview

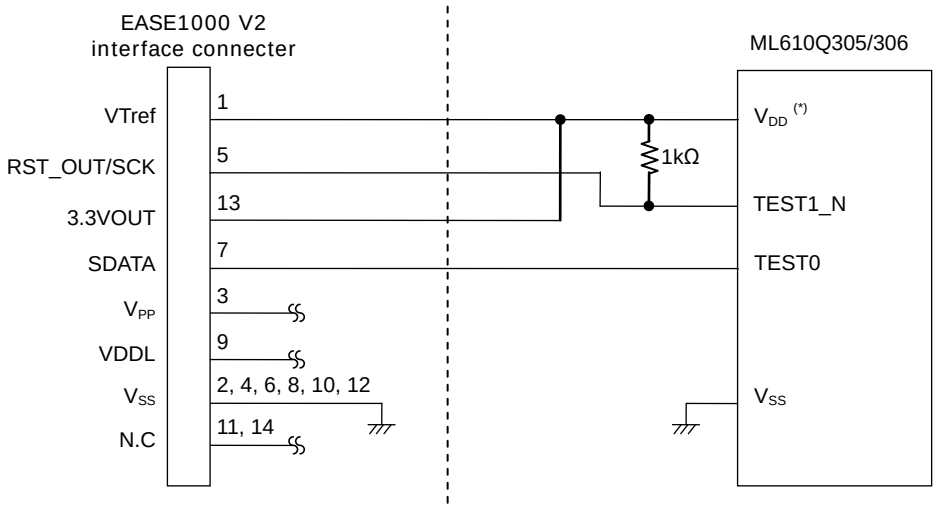
This LSI has an on-chip debug function that enables flash memory reprogramming.
To use the on-chip debug function, connect the LSI to the on-chip debug emulator (EASE1000 V2).
For the on-chip debug emulator, refer to the "EASE1000 V2 User's Manual."

23.2 How to Connect the On-Chip Debug Emulator

Figure 23-1 shows EASE1000 V2 Connections when 3.3VOUT power from EASE1000 V2 is used for V_{DD}.
Figure 23-2 shows EASE1000 V2 Connections when the power from customer's power circuit is used for V_{DD}.
Please make that either TEST1_N pin can be connected to VDD with a jumper pin when the on-chip debug emulator is not used or TEST1_N pin is pulled up to V_{DD} with around 1kΩ resistor.



In case TEST1_N is connected to VDD with a jumper pin



In case TEST1_N is pulled up to V_{DD} with 1kΩ resistor

Figure 23-1 EASE1000 V2 Connections when 3.3VOUT power from EASE1000 V2 is used for V_{DD}

(*) Connect the capacitor C_V externally between V_{DD} and V_{SS} described in recommended operating conditoins of Appendix C.

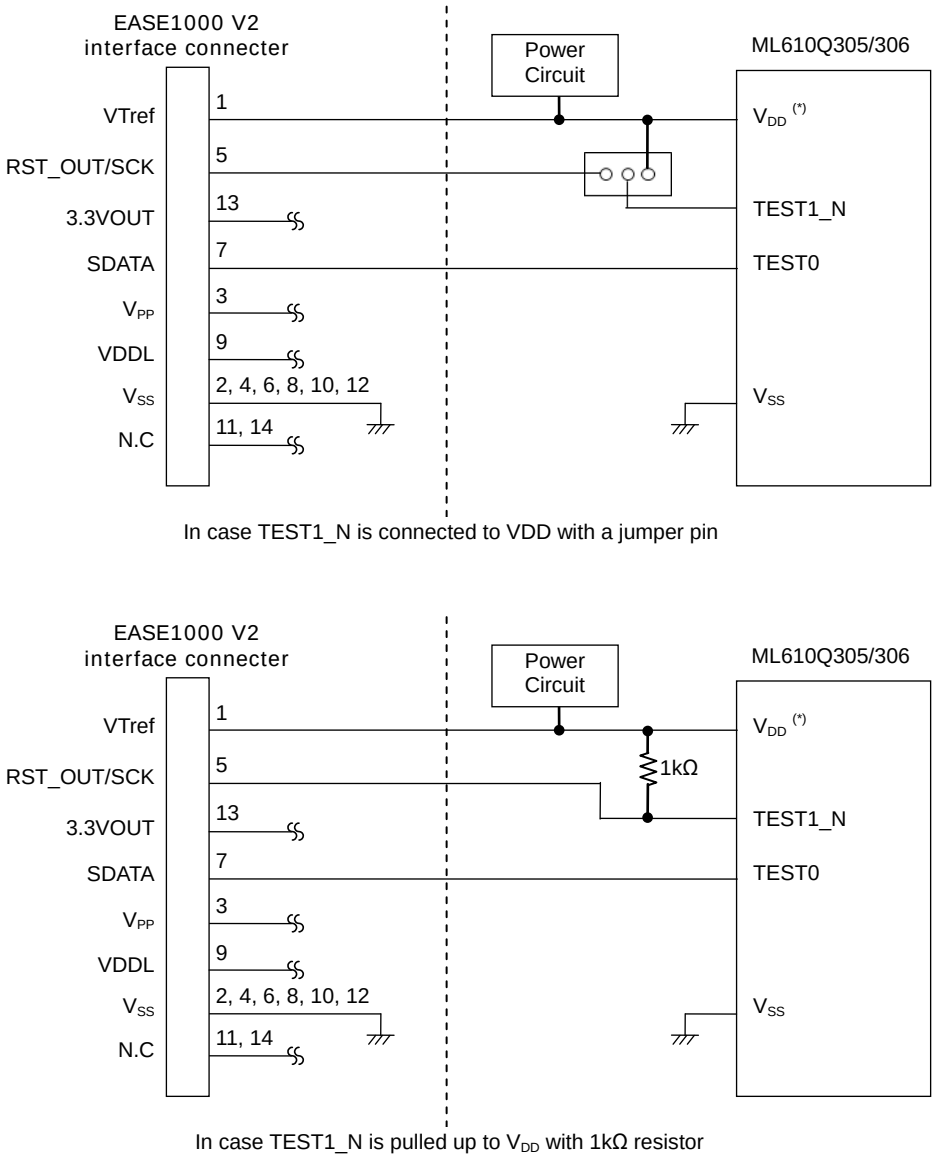


Figure 23-2 EASE1000 V2 Connections when the power from customer's power circuit is used for V_{DD}

(*) Connect the capacitor C_V externally between V_{DD} and V_{SS} described in recommended operating conditoins of Appendix C.

Notes:
· Do not use LSI used for debugging as a mass-production article.
· When using the on-chip debug function or flash memory reprogramming function after mounting the LSI on the board, design the board so that the four pins of V_{DD}, V_{SS}, ,TEST1_N, and TEST0, which are required for connection to the on-chip debug emulator, are capable of connection. For details, refer to the "EASE1000 V2 User's Manual".
· When software debugging with the on-chip debug emulator (EASE1000 V2), select "ML610305" or "ML610306" as a target chip on it.

Chapter 24

Port 9

24. Port 9

24.1 Overview

This LSI includes an 1-bit or 3-bit(*) input/output port, Port 9 (P90, P91(*), P92(*)).

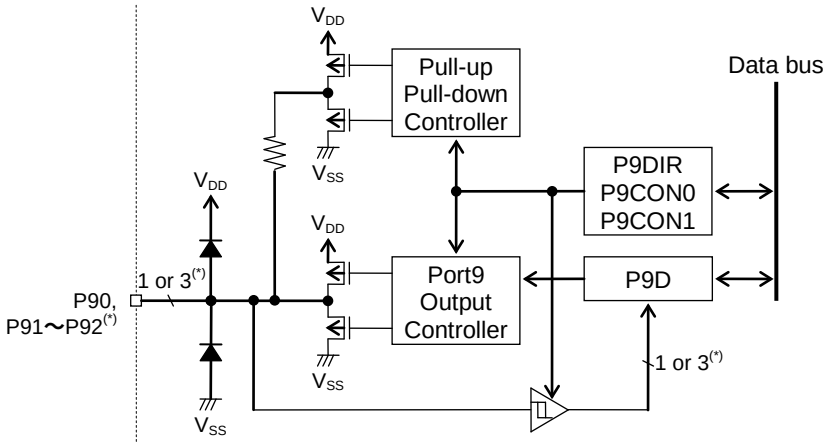
24.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for a bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for a bit in input mode.

(*): built into ML610Q306.

24.1.2 Configuration

Figure 24-1 shows the configuration of Port 9.



P9D	: Port 9 data register
P9DIR	: Port 9 direction register
P9CON0	: Port 9 control register 0
P9CON1	: Port 9 control register 1

Figure 24-1 Configuration of Port 9

(*) : P91 to P92 pin, and data width 3 bits are ML610Q306 only.

24.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function
P90	I/O	Input/output port	¾	¾
P91(*)	I/O	Input/output port	¾	¾
P92(*)	I/O	Input/output port	¾	¾

(*): built into ML610Q306.

24.2 Description of Registers

24.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F248H	Port 9 data register	P9D	¾	R/W	8	00H
0F249H	Port 9 direction register	P9DIR	¾	R/W	8	00H
0F24AH	Port 9 control register 0	P9CON0	P9CON	R/W	8/16	00H
0F24BH	Port 9 control register 1	P9CON1		R/W	8	00H

24.2.2 Port 9 Data Register (P9D)

Address: 0F248H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9D	¾	¾	¾	¾	¾	P92D(*)	P91D(*)	P90D
R/W	¾	¾	¾	¾	¾	R/W(*)	R/W(*)	R/W
Initial value	0	0	0	0	0	0	0	0

P9D is a special function register (SFR) to set the value to be output to the Port 9 pin or to read the input level of the Port 9. In output mode, the value of this register is output to the Port 9 pin. The value written to P9D is readable. In input mode, the input level of the Port 9 pin is read when P9D is read. P9D can be written during input mode, and its value does not affect the port level.
Output mode or input mode is selected by using the port direction register (P9DIR) described later.

[Description of Bits]

· **P92D to P91D(*), P90D** (bits 2 to 0(*), bit 0)
The P92D to P91D bits(*) and the P90D bit are used to set the output value of the Port 9 pin in output mode and to read the pin level of the Port 9 pin in input mode.

P90D	Description
0	Output or input level of the P90 pin: "L"
1	Output or input level of the P90 pin: "H"

P91D(*)	Description
0	Output or input level of the P91 pin: "L"
1	Output or input level of the P91 pin: "H"

P92D(*)	Description
0	Output or input level of the P92 pin: "L"
1	Output or input level of the P92 pin: "H"

Note:
When setting a value to the bit of the P9D by using bit operation instruction, input levels of the pin are written to the P9D if non-target bits are set as the input mode. Therefore, switch the mode to the output mode by the port 9 direction register (P9DIR) after setting the output value to the P9D when switching from the input mode to the output mode.

(*): The P92D to P91D are built into ML610Q306.

24.2.3 Port 9 Direction Register (P9DIR)

Address: 0F249H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9DIR	¾	¾	¾	¾	¾	P92DIR(*)	P91DIR(*)	P90DIR
R/W	¾	¾	¾	¾	¾	R/W(*)	R/W(*)	R/W
Initial value	0	0	0	0	0	0	0	0

P9DIR is a special function register (SFR) to select the input/output mode of Port 9.

[Description of Bits]

· **P92DIR to P91DIR(*), P90DIR** (bits 2 to 0(*), bit 0)
The P92DIR to P91DIR bits(*) and the P90DIR bit are used to set the input/output direction of the Port 9 pin.

P90DIR	Description
0	P90 pin: Output (initial value)
1	P90 pin: Input

P91DIR(*)	Description
0	P91 pin: Output (initial value)
1	P91 pin: Input

P92DIR(*)	Description
0	P92 pin: Output (initial value)
1	P92 pin: Input

(*): The P92DIR to P91DIR are built into ML610Q306.

24.2.4 Port 9 Control Registers 0, 1 (P9CON0, P9CON1)

Address: 0F24AH
Access: R/W
Access size: 8/16 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9CON0	¾	¾	¾	¾	¾	P92C0(*2)	P91C0(*2)	P90C0
R/W	¾	¾	¾	¾	¾	R/W(*2)	R/W(*2)	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F24BH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P9CON1	¾	¾	¾	¾	¾	P92C1(*2)	P91C1(*2)	P90C1
R/W	¾	¾	¾	¾	¾	R/W(*2)	R/W(*2)	R/W
Initial value	0	0	0	0	0	0	0	0

P9CON0 and P9CON1 are special function registers (SFRs) to specify the input and output conditions of a pin of Port 9. The conditions differ between input mode and output mode. Input or output is selected by the P9DIR register.

[Description of Bits]

· **P92C1 to P91C1(*2), P90C1, P92C0 to P91C0(*2), P90C0** (bits 2 to 1(*2), bit 0)
The P92C1 to P91C1(*2), the P90C1 and the P92C0 to P91C0(*2), the P90C0 bits are used to select high-impedance output(*1), P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

(*1) High-impedance output means the status that both of "H" level output and "L" level output turn off.

Setting of P90 pin		When output mode is selected (P90DIR bit = "0")	When input mode is selected (P90DIR bit = "1")
P90C1	**P90C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P91 pin		When output mode is selected (P91DIR bit = "0")	When input mode is selected (P91DIR bit = "1")
P91C1	**P91C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P92 pin		When output mode is selected (P92DIR bit = "0")	When input mode is selected (P92DIR bit = "1")
P92C1	**P92C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

(*2): The P92C1 to P91C1 and the P92C0 to P91C0 are built into ML610Q306.

24.3 Description of Operation

24.3.1 Input/Output Port Functions

For a pin of Port 9, either output or input is selected by setting the Port 9 direction register (P9DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 9 control registers 0 and 1 (P9CON0 and P9CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 9 control registers 0 and 1 (P9CON0 and P9CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to a pin of Port 9 depending on the value set by the Port 9 data register (P9D).
In input mode, the input level of a pin of Port 9 can be read from the Port 9 data register (P9D).

Chapter 25

Code option

25. Code-Option

25.1 Overview

This LSI includes code option function.
Allows selection of detection voltage of Low Level Detector (LLD) by setting the Code-Option Data in the test data area of program memory

25.1.1 Features

· Allows selection of detection voltage of Low Level Detector (LLD).

25.2 The Setting Method of the Code-Option Data

25.2.1 Code-Option Data Format

The Code-Option data set the test data area 0:0FDE0H of program memory.

Address	7	6	5	4	3	2	1	0
See above	—*	—*	—*	—*	—*	—*	LLD1	LLD0

Address	15	14	13	12	11	10	9	8
See above	—*	—*	—*	—*	—*	—*	—*	—*

*: Set to "0"

The LLD1 and LLD0 bits are used to set the detection voltage of Low Level Detector (LLD)

LLD1	**LLD0**	Detection Voltage V_{TH}	Hysteresis Width Ta=25°C
1	1	1.9V	100mV (Typ.)
1	0	2.1V	
0	1	2.3V	
0	0	2.5V	

25.2.2 Code-Option Programming Method

Figure 25-1 shows an example program of the Code-Option data.

example
The detection voltage of LLD is 2.3V

```
;-------------------------------------------------------
;       Setting the code-option data
;-------------------------------------------------------
        cseg at 0:0fde0h        ; Setting address
        dw      0001h           ; Setting of LLD
```

Figure 25-1 Example program of the Code-Option data

Note:
Set "0FFH" data for the test data area other than the Code-Option data.

25.3 The Method to refer the Code-Option Data

The Code-Option data can be read from Segment 8 address (8:0fde0h) in the data memory space, which is mirror address of Segment 0 address (0:0fde0h) in the program memory area, where the code option data is set. The software program examples of reading Code-Option data are shown below.

Example of assembler program

```
L       R0,8:0FDE0h;   loading 8:0FDE0h address data
AND     R0, #03h;
CMP     R0, #02h;
BEQ     < function when LLD detection voltage is 2.1V>;
```

Example of C program

```
#define CODEOP (*(volatile unsigned int __far *)0x8FDE0)

if(CODEOP & 0x03 == 0x02) function_when_LLD_detection_voltage_is_2.1V();
```

Appendixes

Appendix A Registers

Contents of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	¾	R/W	8	00H
0F001H	Reset status register	RSTAT	¾	R/W	8	Undefined
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	83H
0F008H	Stop code acceptor	STPACP	¾	W	8	00H
0F009H	Standby control register	SBYCON	¾	W	8	00H
0F00AH	Low-speed time base counter register	LTBR	¾	R/W	8	00H
0F00BH	High-speed time base counter divide register	HTBDR	¾	R/W	8	00H
0F00EH	Watchdog timer control register	WDTCON	¾	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	¾	R/W	8	02H
0F011H	Interrupt enable register 1	IE1	¾	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	¾	R/W	8	00H
0F013H	Interrupt enable register 3	IE3	¾	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	¾	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	¾	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	¾	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	¾	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	¾	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	¾	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	¾	R/W	8	00H
0F01BH	Interrupt request register 3	IRQ3	¾	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	¾	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	¾	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	¾	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	¾	R/W	8	00H
0F024H	Port 8 interrupt control register 0	P8ICON0	¾	R/W	8	00H
0F025H	Port 8 interrupt control register 1	P8ICON1	¾	R/W	8	00H
0F026H	Port 8 interrupt control register 2	P8ICON2	¾	R/W	8	00H
0F028H	Block control register 0	BLKCON0	¾	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	¾	R/W	8	00H
0F02BH	Block control register 3	BLKCON3	¾	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	¾	R/W	8	00H
0F030H	Timer 0 data register	TM0D	TM0DC	R/W	8/16	0FFH
0F031H	Timer 0 counter register	TM0C		R/W	8	00H
0F032H	Timer 0 control register 0	TM0CON0	TM0CON	R/W	8/16	00H
0F033H	Timer 0 control register 1	TM0CON1		R/W	8	00H
0F034H	Timer 1 data register	TM1D	TM1DC	R/W	8/16	0FFH
0F035H	Timer 1 counter register	TM1C		R/W	8	00H
0F036H	Timer 1 control register 0	TM1CON0	TM1CON	R/W	8/16	00H
0F037H	Timer 1 control register 1	TM1CON1		R/W	8	00H
0F038H	Timer 2 data register	TM2D	TM2DC	R/W	8/16	0FFH
0F039H	Timer 2 counter register	TM2C		R/W	8	00H

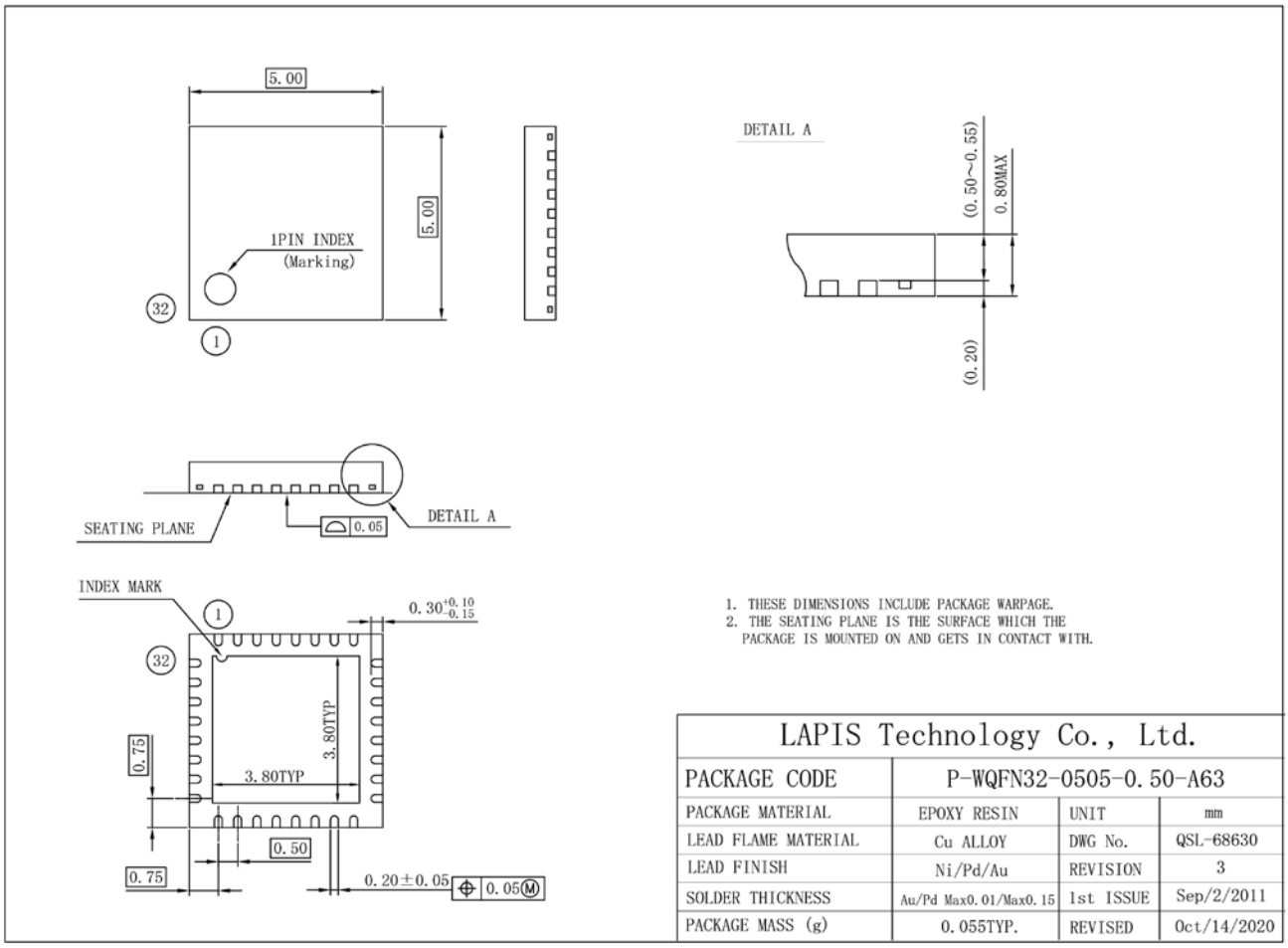
Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F03AH	Timer 2 control register 0	TM2CON0	TM2CON	R/W	8/16	00H
0F03BH	Timer 2 control register 1	TM2CON1		R/W	8	00H
0F03CH	Timer 3 data register	TM3D	TM3DC	R/W	8/16	0FFH
0F03DH	Timer 3 counter register	TM3C		R/W	8	00H
0F03EH	Timer 3 control register 0	TM3CON0	TM3CON	R/W	8/16	00H
0F03FH	Timer 3 control register 1	TM3CON1		R/W	8	00H
0F0E0H	Flash address register L	FLASHAL	FLASHA	R/W	8/16	00H
0F0E1H	Flash address register H	FLASHAH		R/W	8	00H
0F0E2H	Flash data register L	FLASHDL	FLASHD	R/W	8/16	00H
0F0E3H	Flash data register H	FLASHDH		R/W	8	00H
0F0E4H	Flash control register	FLASHCON	¾	W	8	00H
0F0E5H	Flash accepter	FLASHACP	¾	W	8	00H
0F0E6H	Flash segment register	FLASHSEG	¾	R/W	8	00H
0F0E7H	Flash self register	FLASHSLF	¾	R/W	8	00H
0F0E8H	Flash protection register	FLASHPRT	¾	R/W	8	00H
0F200H	NIMI data register	NMID	¾	R	8	Undefined
0F201H	NIMI control register	NIMICON	¾	R/W	8	00H
0F210H	Port 2 data register	P2D	¾	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	¾	R/W	8	00H
0F220H	Port 4 data register	P4D	¾	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	¾	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H
0F240H	Port 8 data register	P8D	¾	R/W	8	00H
0F241H	Port 8 direction register	P8DIR	¾	R/W	8	00H
0F242H	Port 8 control register 0	P8CON0	P8CON	R/W	8/16	00H
0F243H	Port 8 control register 1	P8CON1		R/W	8	00H
0F244H	Port 8 mode register 0	P8MOD0	P8MOD	R/W	8/16	00H
0F245H	Port 8 mode register 1	P8MOD1		R/W	8	00H
0F248H	Port 9 data register	P9D	¾	R/W	8	00H
0F249H	Port 9 direction register	P9DIR	¾	R/W	8	00H
0F24AH	Port 9 control register 0	P9CON0	P9CON	R/W	8/16	00H
0F24BH	Port 9 control register 1	P9CON1		R/W	8	00H
0F280H	Serial port 0 transmit/receive buffer L	SIO0BUFL	SIO0BUF	R/W	8/16	00H
0F281H	Serial port 0 transmit/receive buffer H	SIO0BUFH		R/W	8	00H
0F282H	Serial port 0 control register	SIO0CON	¾	R/W	8	00H
0F284H	Serial port 0 mode register 0	SIO0MOD0	SIO0MOD	R/W	8/16	00H
0F285H	Serial port 0 mode register 1	SIO0MOD1		R/W	8	00H
0F288H	Serial port 1 transmit/receive buffer L	SIO1BUFL	SIO1BUF	R/W	8/16	00H
0F289H	Serial port 1 transmit/receive buffer H	SIO1BUFH		R/W	8	00H
0F28AH	Serial port 1 control register	SIO1CON	¾	R/W	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F28CH	Serial port 1 mode register 0	SIO1MOD0	SIO1MOD	R/W	8/16	00H
0F28DH	Serial port 1 mode register 1	SIO1MOD1		R/W	8	00H
0F290H	UART0 transmit/receive buffer	UA0BUF	–	R/W	8	00H
0F291H	UART0 control register	UA0CON	–	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	–	R/W	8	00H
0F2A1H	I^2C bus 0 slave address register	I2C0SA	—	R/W	8	00H
0F2A2H	I^2C bus 0 transmit data register	I2C0TD	—	R/W	8	00H
0F2A3H	I^2C bus 0 control register	I2C0CON	—	R/W	8	00H
0F2A4H	I^2C bus 0 mode register	I2C0MOD	—	R/W	8	00H
0F2A5H	I^2C bus 0 status register	I2C0STAT	—	R	8	00H
0F2A8H	I^2C bus 1 receive register	I2C1RD	¾	R	8	00H
0F2A9H	I^2C bus 1 slave address register	I2C1SA	¾	R/W	8	00H
0F2AAH	I^2C bus 1 transmit data register	I2C1TD	¾	R/W	8	00H
0F2ABH	I^2C bus 1 control register	I2C1CON	¾	R/W	8	00H
0F2ACH	I^2C bus 1 mode register	I2C1MOD	¾	R/W	8	00H
0F2ADH	I^2C bus 1 status register	I2C1STAT	¾	R	8	00H
0F2B0H	Audio FIFO data register	VFDAT	¾	W	8	00H
0F2B1H	Audio FIFO phrase end data register	VFEDAT	¾	W	8	00H
0F2B2H	HQ phrase stop-bit length register	VHQSBL	¾	R/W	8	00H
0F2B3H	Audio status register	VSTAT	¾	R	8	11H
0F2B4H	Audio mode register	VMOD	¾	R/W	8	00H
0F2B5H	Audio data type register	VTYPE	¾	R/W	8	41H
0F2B6H	Volume setting register	VVOL	¾	R/W	8	09H
0F2B7H	Audio playback control register	VCON	¾	R/W	8	00H
0F2BCH	Speaker amplifier control register	SPCON	¾	R/W	8	00H
0F2BFH	Disconnection detection control register	DCDCON	¾	R/W	8	00H
0F2C0H	Volume status register	VVOLS	¾	R	8	09H
0F2C8H	Speaker pin short detection control register	SDCON	¾	R/W	8	00H
0F2D0H	SA-ADC result register 0L	SADR0L	SADR0	R	8/16	00H
0F2D1H	SA-ADC result register 0H	SADR0H		R	8	00H
0F2D2H	SA-ADC result register 1L	SADR1L	SADR1	R	8/16	00H
0F2D3H	SA-ADC result register 1H	SADR1H		R	8	00H
0F2D4H	SA-ADC result register 2L	SADR2L	SADR2	R	8/16	00H
0F2D5H	SA-ADC result register 2H	SADR2H		R	8	00H
0F2D6H	SA-ADC result register 3L (*1)	SADR3L	SADR3	R	8/16	00H
0F2D7H	SA-ADC result register 3H (*1)	SADR3H		R	8	00H
0F2F0H	SA-ADC control register 0	SADCON0	SADCON	R/W	8/16	00H
0F2F1H	SA-ADC control register 1	SADCON1		R/W	8	00H
0F2F2H	SA-ADC mode register 0	SADMOD0	¾	R/W	8	00H

(*1) : built into ML610Q306.

Appendix B Package Dimensions

Package Dimensions (32-pin WQFN)



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN32-0505-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68630
LEAD FINISH	Ni/Pd/Au	REVISION	3
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/2/2011
PACKAGE MASS (g)	0.055TYP.	REVISED	Oct/14/2020

Notes for Mounting the Surface Mount Type Package

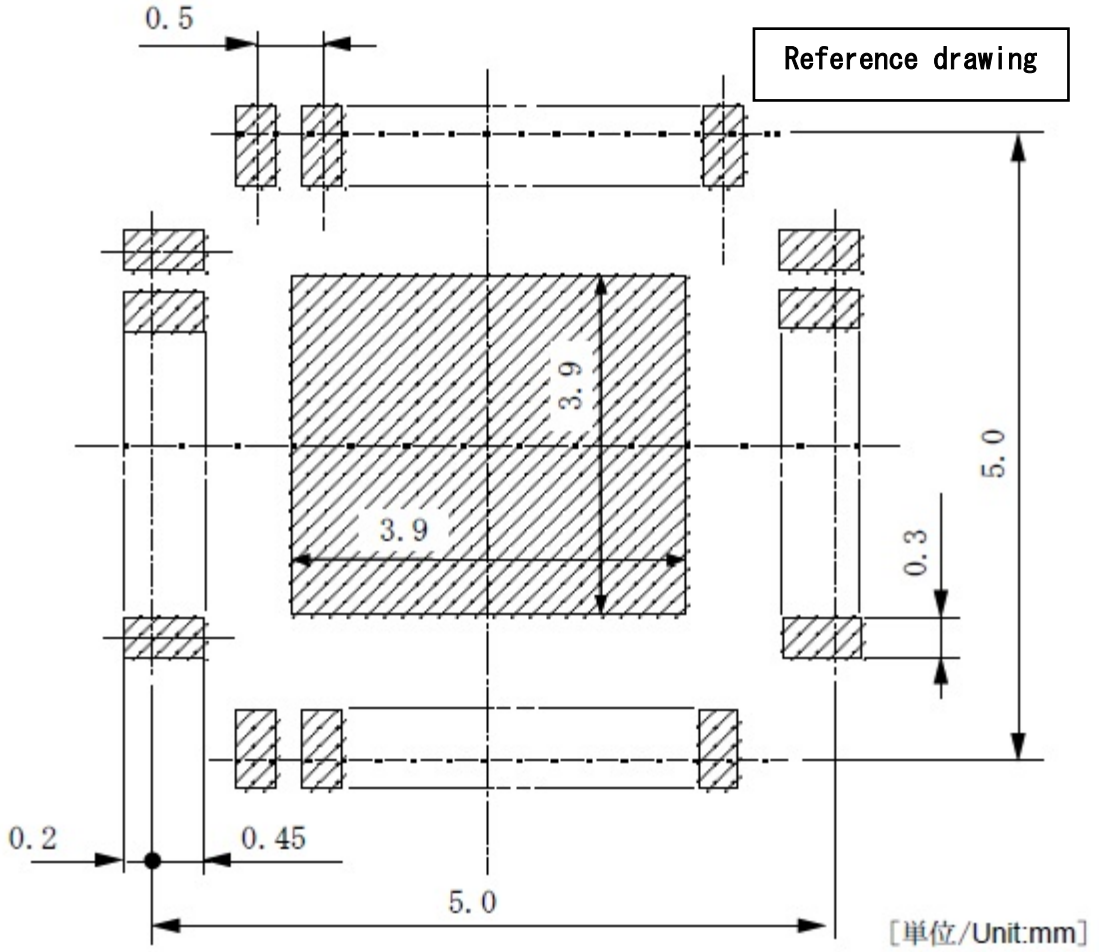
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=76.2 / 114.3 / 1.6(mm)
PCB Layer	JEDEC 4layers
Air cooling conditions	Calm(0m/sec)
Heat resistance(θJa)	32.2[°C/W] (back diepad contact)
Power consumption of Chip PMax	0.300[W]

TjMax of this LSI is 110 °C. TjMax is expressed with the following formulas.
TjMax = TaMax + θJa × PMax

Figure of soldering department terminal existence range (32-pin WQFN)

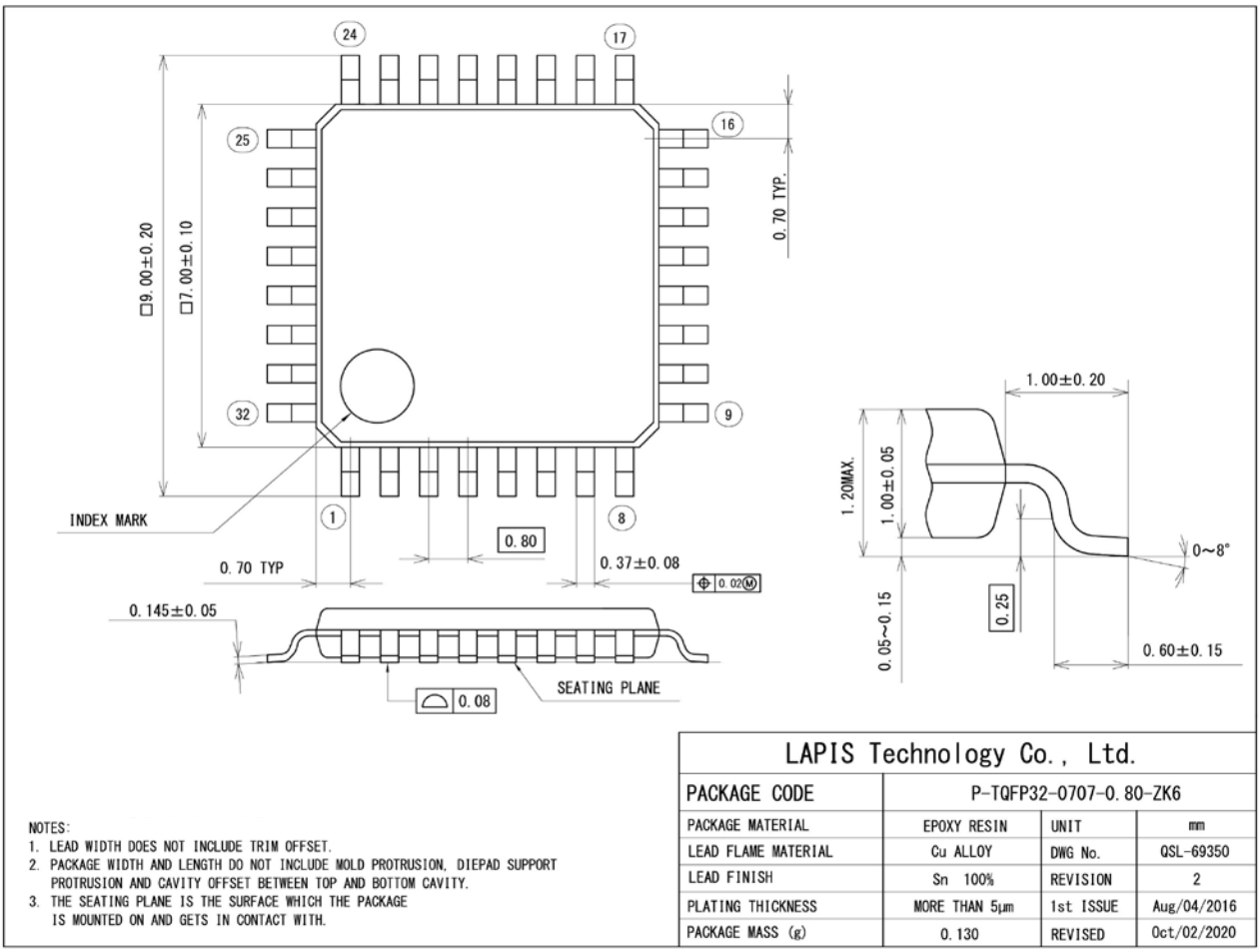


Attention of the layout of a mounting board

Please take into consideration enough that there are not ease of a mounting, the reliability of contact, leading about of a wiring, and a solder bridge generate in the case of layout of the foot pattern of a mounting board.

The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

Package Dimensions (32-pin TQFP)



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP32-0707-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69350
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Aug/04/2016
PACKAGE MASS (g)	0.130	REVISED	Oct/02/2020

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

Notes for Mounting the Surface Mount Type Package

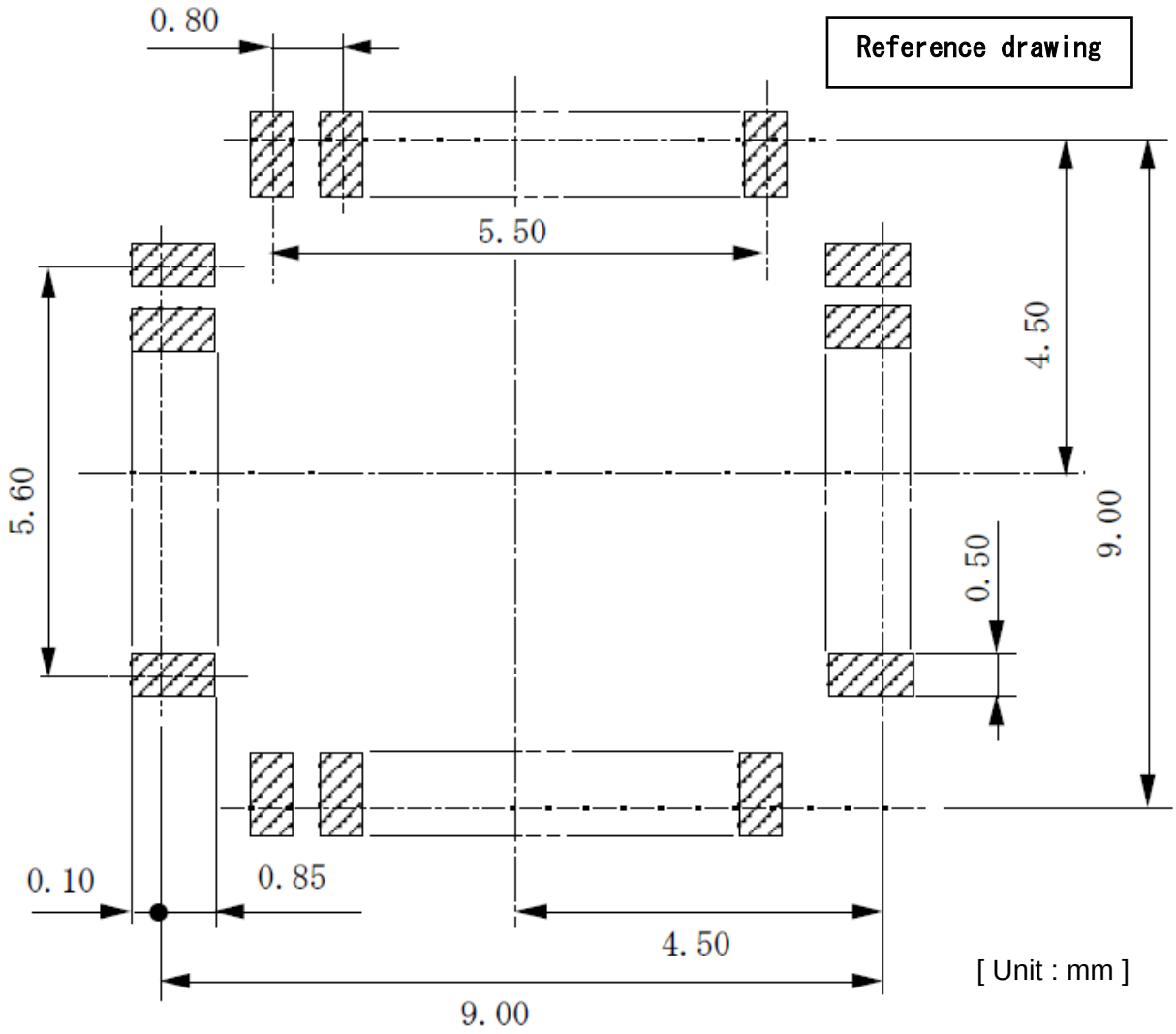
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=76.2 / 114.3 / 1.6(mm)
PCB Layer	JEDEC 4layers
Air cooling conditions	Calm(0m/sec)
Heat resistance(θJa)	58.5 [°C/W]
Power consumption of Chip PMax	0.300[W]

TjMax of this LSI is 110 °C. TjMax is expressed with the following formulas.
TjMax = TaMax + θJa × PMax

Figure of soldering department terminal existence range (32-pin TQFP)

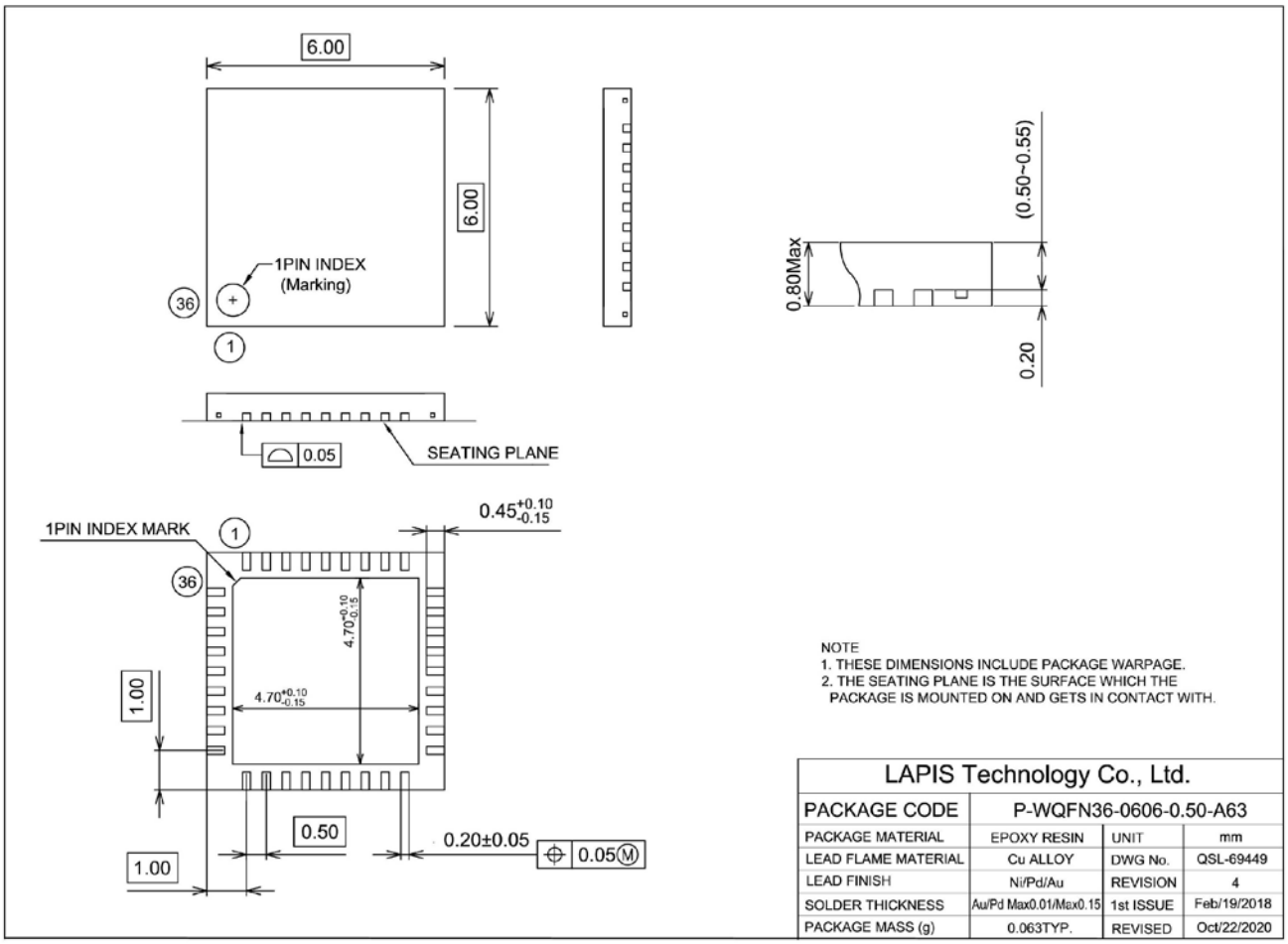


Attention of the layout of a mounting board

Please take into consideration enough that there are not ease of a mounting, the reliability of contact, leading about of a wiring, and a solder bridge generate in the case of layout of the foot pattern of a mounting board.

The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

Package Dimensions (36-pin WQFN)



Notes for Mounting the Surface Mount Type Package

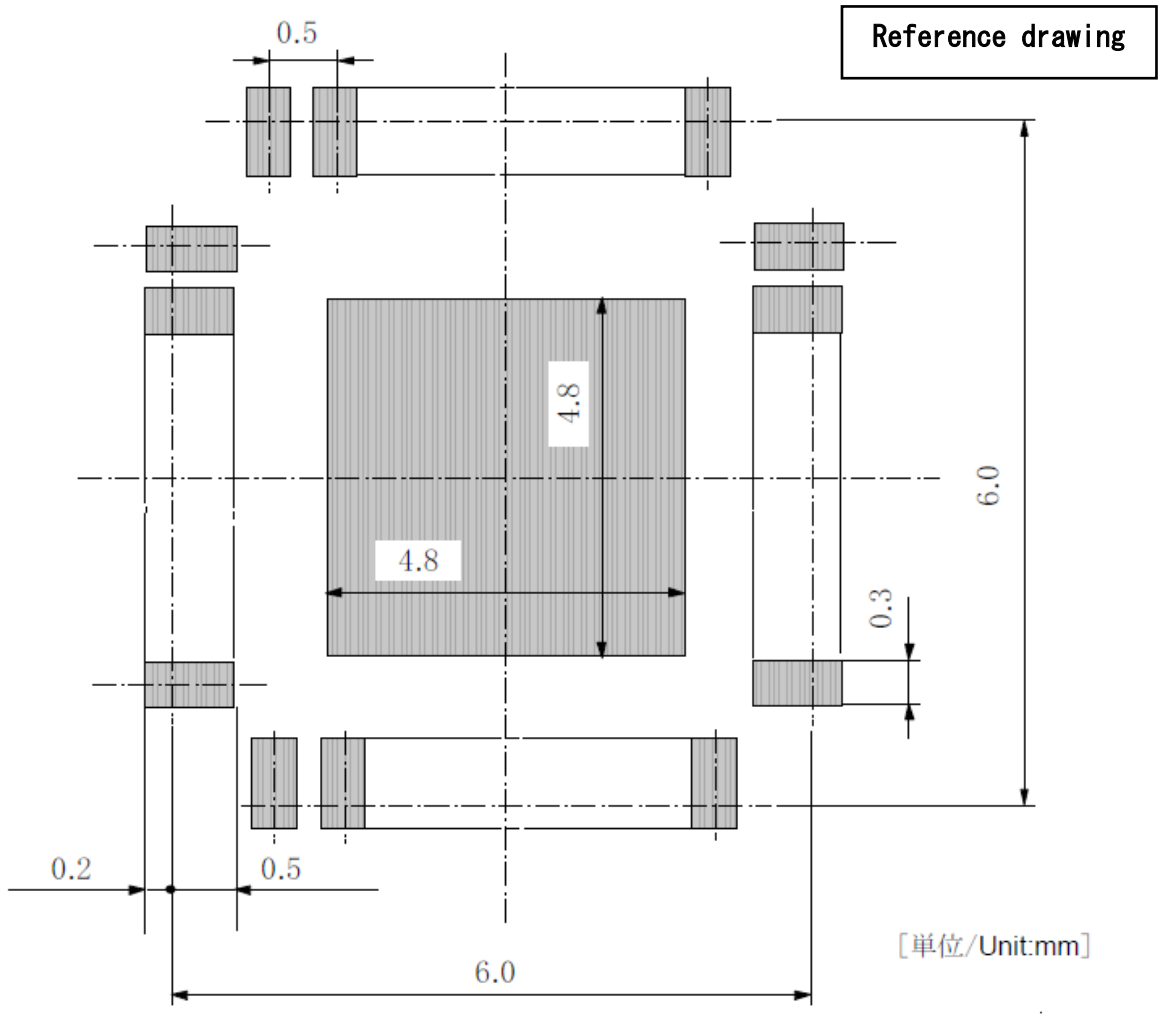
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=76.2 / 114.3 / 1.6（mm）
PCB Layer	JEDEC 4layers
Air cooling conditions	Calm（0m/sec）
Heat resistance（θJa）	30.0 [°C/W] (back diepad contact)
Power consumption of Chip PMax	0.300[W]

TjMax of this LSI is 110 °C. TjMax is expressed with the following formulas.
TjMax = TaMax + θJa × PMax

Figure of soldering department terminal existence range (36-pin WQFN)



Attention of the layout of a mounting board

Please take into consideration enough that there are not ease of a mounting, the reliability of contact, leading about of a wiring, and a solder bridge generate in the case of layout of the foot pattern of a mounting board.

The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

Appendix C Electrical Characteristics

● Absolute Maximum Ratings

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	- 0.3 to +6.5	V
Power supply voltage 2	SPV_{DD}	Ta=25°C	- 0.3 to +6.5	V
Power supply voltage 3	V_{DDL}	Ta=25°C	- 0.3 to +2.0	V
Reference supply voltage	V_{REF}	Ta=25°C	- 0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta=25°C	- 0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	- 0.3 to V_{DD}+0.3	V
Output current 1 (P40 to P42, P43[*1], P80 to P87, P90, P91 to P92[*1])	I_{OUT1}	Ta=25°C	- 12 to +11	mA
Output current 2 (P20 to P22)	I_{OUT2}	Ta=25°C When setting Nch open drain mode	- 12 to +20	mA
Power dissipation	PD	Ta=25°C	1.0	W
Storage temperature	T_{STG}	—	- 55 to +150	°C

[*1] :P43, P91 to P92 are built into ML610Q306

● Recommended Operating Conditions

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	- 40 to +85	°C
Operating voltage	V_{DD}	—	2.0 to 5.5	V
	SPV_{DD}	—	2.0 to 5.5	
Reference supply voltage	V_{REF}	$V_{DD} \geqq V_{REF}$	2.2 to V_{DD}	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 2.0 to 5.5V	27k to 4.2M	Hz
		V_{DD} = 2.2 to 5.5V	4.2M to 8.4M	Hz
Capacitor externally connected to V_{DD} pin	C_V	—	More than 1.0±30%	mF
Capacitor externally connected to V_{DDL} pin	C_L	—	1.0±30%	mF

● Operating Conditions of Flash Memory

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	At write/erase (Data flash area)		-40 to +70	°C
		At write/erase (Program code area)		0 to +40	
Operating voltage	V_{DD}	At write/erase		2.2 to 5.5	V
Maximum rewrite count *1	C_{EPD}	Data flash area (512Byte x 4)		10,000	cycles
	C_{EPP}	Program code area		100	
Erase unit	—	Chip erase		All program and data area	—
	—	Block erase	Program area	16	KB
			Data area	2	
	—	Sector erase		512	B
Erase time(Maximum)	—	Chip/Block/Sector erase		50	ms
Program unit	—	—		1word (2Bytes)	—
Program time(Maximum)	—	1word (2Bytes)		40	µs
Write cycles	Y_{DR}	—		15	years

*1: It means one erase and one program. Even when erasing is interrupted, it counts as one time.

● DC Characteristics (Supply Current)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta≦+50°C	—	0.5	3.0	mA	1
			Ta≦+85°C	—	0.5	8.0		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WDT: Operating) High-speed oscillation: Stopped	Ta≦+50°C	—	2.0	5.0		
			Ta≦+85°C	—	2.0	10		
Supply current 3	IDD3	CPU: Running at 32.768 kHz*1 High-speed oscillation: Stopped		—	15	30		
Supply current 4	IDD4	CPU: Running at 4.096MHz CR oscillating mode	V_{DD}=SPV_{DD}= 3.0V	—	1.0	2.5	mA	
			V_{DD}=SPV_{DD}= 5.0V	—	1.0	2.5		
		CPU: Running at 8.192MHz CR oscillating mode	V_{DD}=SPV_{DD}= 3.0V	—	2.0	3.5		
			V_{DD}=SPV_{DD}= 5.0V	—	2.0	3.5		
Supply current 5	IDD5	CPU: Running at 4.096MHz CR oscillating mode During voice playback of 1KHz,2.98db,SIN-wave (no output load)	V_{DD}=SPV_{DD}= 3.0V	—	2.0	5.0		
			V_{DD}=SPV_{DD}= 5.0V	—	4.0	8.0		
		CPU: Running at 8.192MHz CR oscillating mode During voice playback of 1KHz,2.98db,SIN-wave (no output load)	V_{DD}=SPV_{DD}= 3.0V	—	3.0	6.0		
			V_{DD}=SPV_{DD}= 5.0V	—	5.0	9.0		

*1: Case when the CPU operating rate is 100% (no HALT state).

● DC Characteristics (VOHL, IOHL, IIHL)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P22) (P40 to P42, P43[*1]) (P80 to P87) (P90, P91 to P92[*1])	VOH1	IOH1=- 0.5mA (When one Port output mode is selected)		V_{DD} - 0.5	—	—	V	2
	VOL1	IOL1=+0.5mA (When one Port output mode is selected)		—	—	0.5		
Output voltage 2 (P20 to P22)	VOL2	(When one port is selected as Nch open drain mode)	IOL2=+5mA $V_{DD} \geqq 2.2V$	—	—	0.5		
			IOL2=+8mA $V_{DD} \geqq 2.3V$	—	—	0.5		
Output voltage 3 (P80 to P81)	VOL3	IOL3=+3mA (I^2C bus input/output mode. When one port is selected as output)		—	—	0.4		
Output leakage (P20 to P22) (P40 to P42, P43[*1]) (P80 to P87) (P90, P91 to P92[*1])	IOOH	VOH=V_{DD} (in high-impedance state)		—	—	1.0	mA	3
	IOOL	VOL=V_{SS} (in high-impedance state)		- 1.0	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1=V_{DD}		0	—	1.0	mA	4
	IIL1	VIL1=V_{SS}		- 1500	- 300	- 20		
Input current 2 (NMI) (P40 to P42, P43[*1]) (P80 to P87) (P90, P91 to P92[*1])	IIH2	VIH2=V_{DD} (when pulled-down)		2	30	250		
	IIL2	VIL2=V_{SS} (when pulled-up)		- 250	- 30	- 2		
	IIH2Z	VIH2=V_{DD} (in high-impedance state)		—	—	1.0		
	IIL2Z	VIL2=V_{SS} (in high-impedance state)		- 1.0	—	—		
Input current 3 (TEST0)	IIH3	VIH3=V_{DD}		20	300	1500		
	IIL3	VIL3=V_{SS}		- 1.0	—	—		

[*1] :P43, P91 to P92 are built into ML610Q306

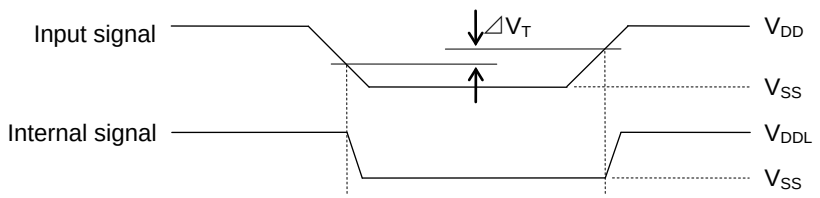
● DC Characteristics (VIHL)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (NMI) (P40 to P42, P43[*1]) (P80 to P87) (P90, P91 to P92[*1])	VIH1	—	0.7´ V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3´ V_{DD}		
Hysteresis width (RESET_N) (TEST0) (TEST1_N) (NMI) (P40 to P42, P43[*1]) (P80 to P87) (P90, P91 to P92[*1])	ΔV_T	—	0.05´ V_{DD}	—	0.4´ V_{DD}		
Input pin capacitance (NMI) (P40 to P42, P43[*1]) (P80 to P87) (P90, P91 to P92[*1])	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	10	pF	—

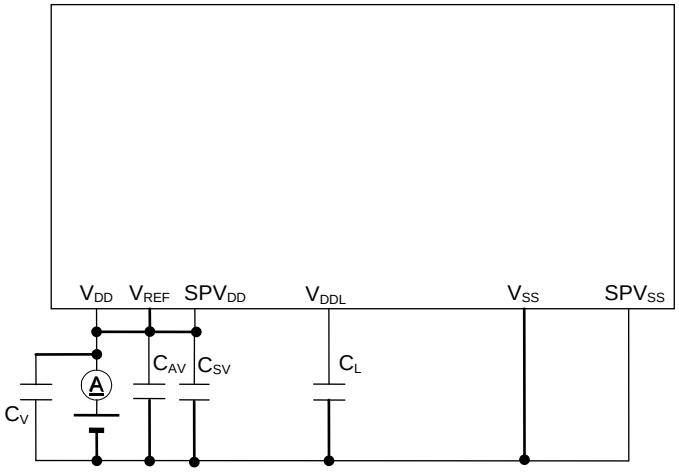
[*1] :P43, P91 to P92 are built into ML610Q306

● Hysteresis Width



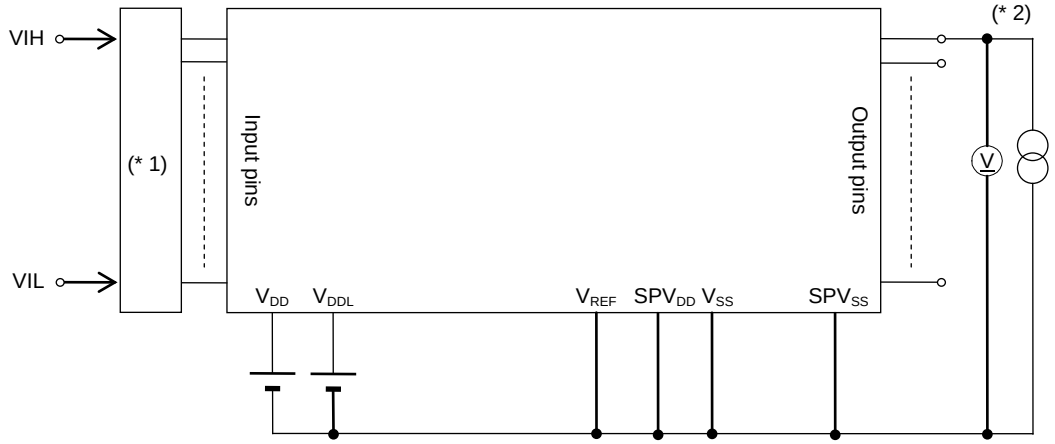
● Measuring Circuit

Measuring Circuit 1



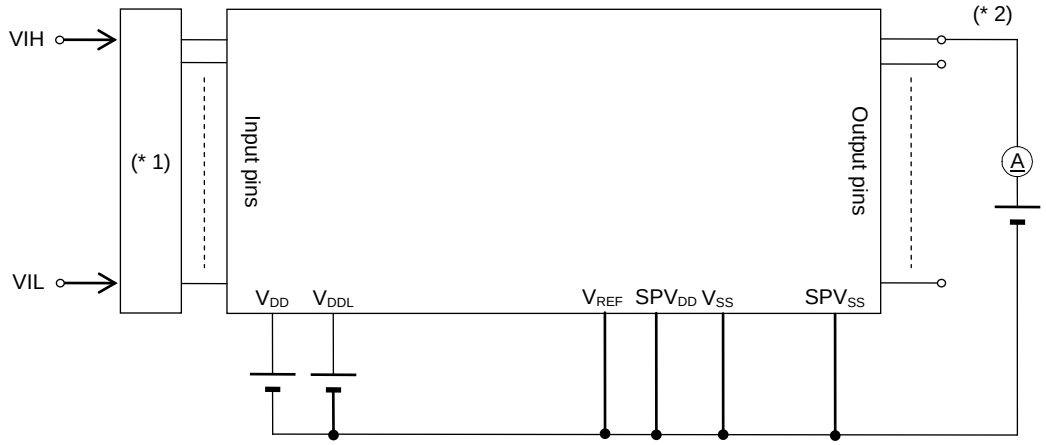
C_V : 1.0µF
C_{SV} : 1.0µF
C_{AV} : 1.0µF
C_L : 1.0µF

Measuring Circuit 2



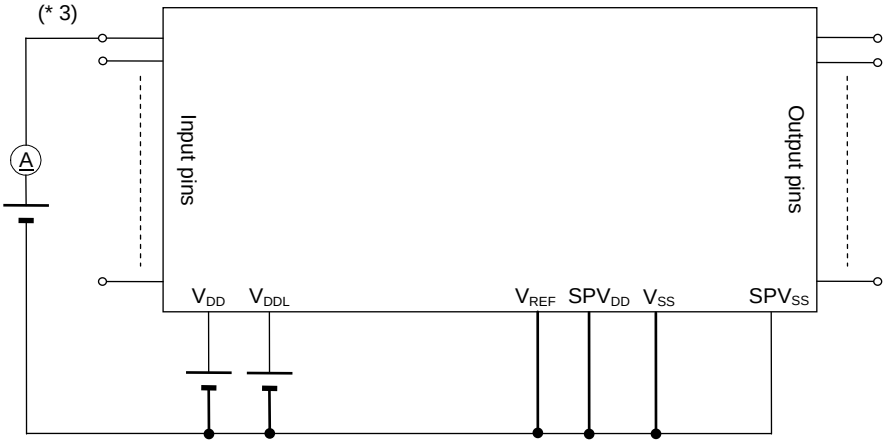
(* 1) Input logic circuit to determine the specified measuring conditions.
(* 2) Measured at the specified output pins.

Measuring Circuit 3



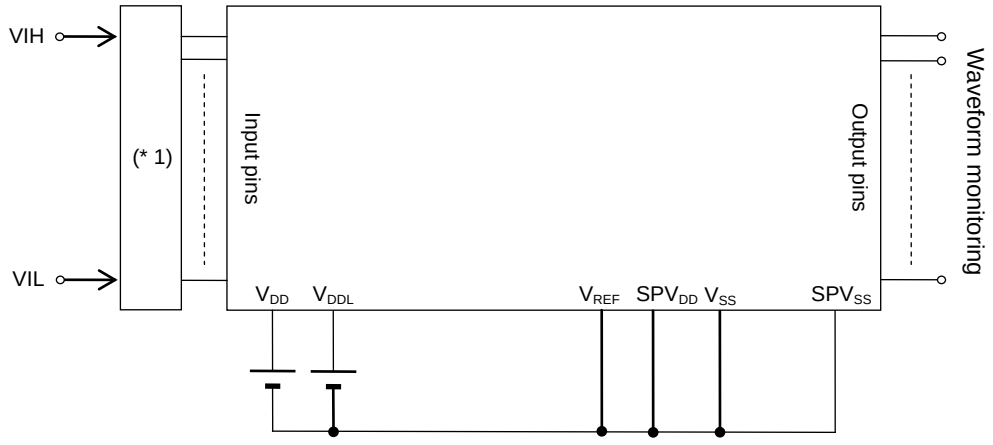
(* 1) Input logic circuit to determine the specified measuring conditions.
(* 2) Measured at the specified output pins.

Measuring Circuit 4



(* 3) Measured at the specified input pins.

Measuring Circuit 5



(* 1) Input logic circuit to determine the specified measuring conditions.

● AC Characteristics (Oscillation Circuit)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Built-in RC oscillation frequency	f_{LCR}	Ta = - 10 to +50°C	Typ -1.5%	32.768	Typ +1.5%	kHz	1
		Ta = - 40 to +85°C	Typ -3.0%		Typ +3.0%		
PLL oscillation frequency	f_{HPLL}	Ta = - 10 to +50°C	Typ -1.5%	4.096 or 8.192	Typ +1.5%	MHz	
		Ta = - 40 to +85°C	Typ -3.0%		Typ +3.0%		

● AC Characteristics (Speaker amp)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

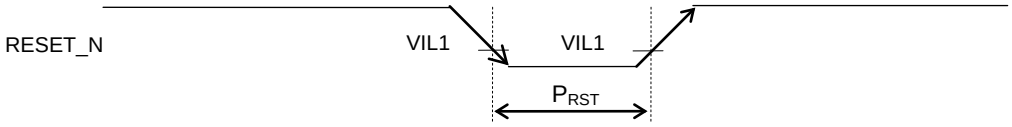
Parameter	Symbol	Condition	Rating			Unit	
			Min.	Typ.	Max.		
SPM, SPP output load resistance	R_{LSP}	—	6.4	8	—	W	
Speaker amp output power	P_{SPO1}	SPV_{DD}=3.0V, f=1kHz R_{SPO}=8W, THD³ 10%	—	0.45	—	W	
	P_{SPO2}	SPV_{DD}=5.0V, f=1kHz R_{SPO}=8W, THD³ 10%	—	1.0	—	W	

● AC Characteristics (Power on, Reset Sequence)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Time until it starts SPV_{DD} after starting V_{DD}	t_{VDD}	—	0	—	—	ns	1
Reset [*1] pulse width	P_{RST}	—	100	—	—	ms	
Reset [*1] noise elimination pulse width	P_{NRST}	—	—	—	0.4	ms	
Power-on rising slope	S_{POR}	—	0.1	—	—	V/ms	

[*1] : reset from RESET_N pin



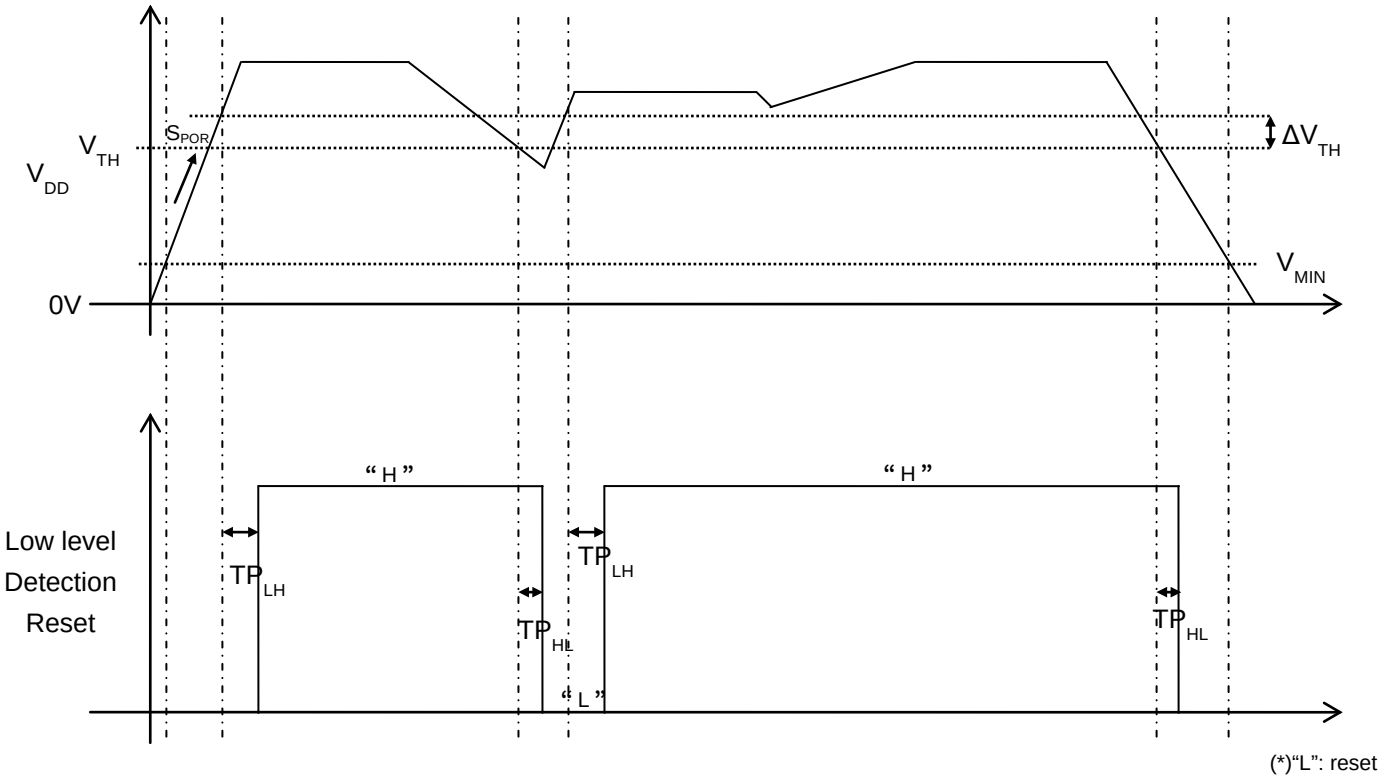
RESET_N Pin Reset

Power-on rising slope

● AC Characteristics (Low Level Detection Reset)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Detection voltage	V_{TH}	LLD1-0=3H	Typ. -5%	1.9	Typ. +5%	V	1
		LLD1-0=2H	Typ. -5%	2.1	Typ. +5%		
		LLD1-0=1H	Typ. -5%	2.3	Typ. +5%		
		LLD1-0=0H	Typ. -5%	2.5	Typ. +5%		
Hysteresis width	Δ_{TH}	—	0.05	0.1	0.15	V	
Output delay when power rising	TP_{LH}	—	—	10	200	ms	
Output delay when power falling	TP_{HL}	—	—	10	200	ms	
Low level detection reset operating voltage	V_{MIN}	—	1.0	—	—	V	

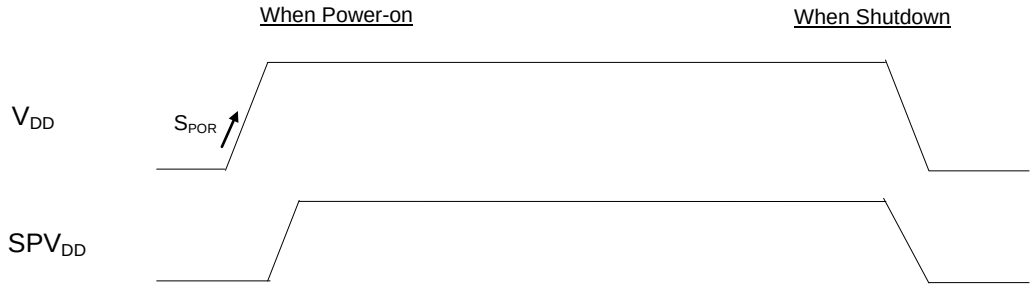


(*)"L": reset

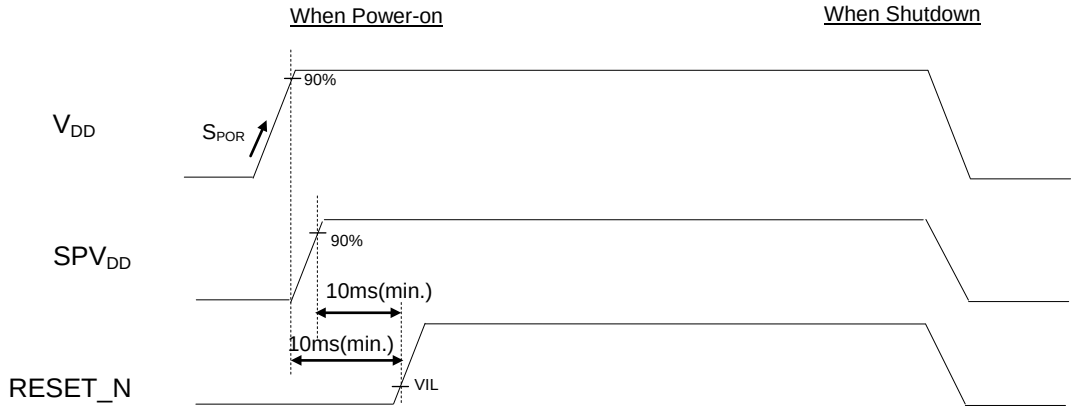
Note:
When the detection voltage of Low Level Detection Reset (V_{TH}) is set to 1.9V(LLD1-0=3H), Low Level Detection Reset is not asserted in the voltage lange from lower minimum recommended operating volatge (V_{DD}=2.0V) to upper detection voltage (V_{TH}=1.9V). During power shutdown sequence, if this voltage lange is kept, depending on the LSI operationg condition, the internal regulated power supply circuit (VRL) can not keep the operationg votage, and the program may NOT operate properly. Therefore, please take measures, such as, setting Low Level Detection Reset (V_{TH}) to except 1.9V (LLD1-0 =3H), and reset generation from RESET_N pin for fail-safe

● Power-on/Shutdown Sequence

・When the power-on rising slope is 0.1V/ms(Min.) or more



・When the power-on rising slope is less than 0.1V/ms(Min.)



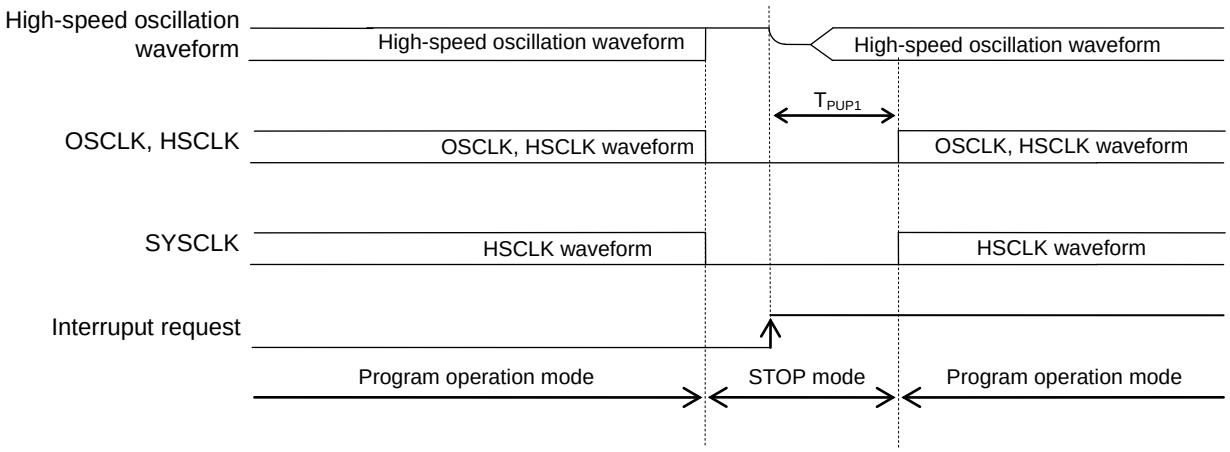
Recommended power-on/shutdown sequence
There are no ristrictions of order, slope time, time lag in turnning on/off V_{DD} and SPV_{DD}.

Notes:
· When the power is turned on, the state of the general-purpose port is undefined. Therefore, there is a possibility of outputting high-level or low-level.If the undefined state at the power-on is a problem, take measures with the peripheral components on the user board.
· When power-on reset is generated because of instantaneous power failure etc., or, when the glitch which is narrower than output delay when power falling (TP_{HL}) is generated on V_{DD} power, or, When V_{DD} power is decreased below low level detection reset operating voltage (V_{MIN}) before output delay when power falling (TP_{HL}) is passed, the LSI may NOT get reset, and the program may NOT operate properly. Therefore, please take measures, such as, power voltage drop prevention by bypass capacitors, and reset generation from RESET_N pin for fail-safe.

● AC Characteristics (Oscillation stable time after STOP release)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

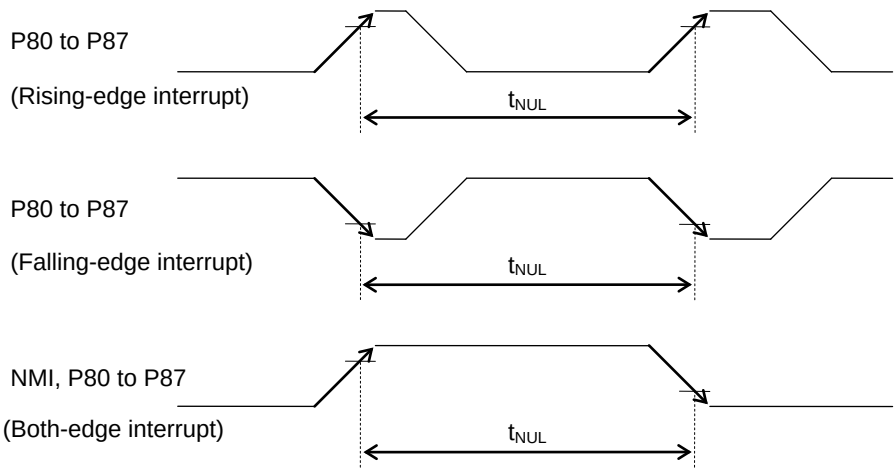
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation stable time after STOP release	T_{PUP1}	—	—	—	2	ms



● AC Characteristics (External Interrupt)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE=1) CPU: NOP operation	2.5´ sysclk	—	3.5´ sysclk	ns

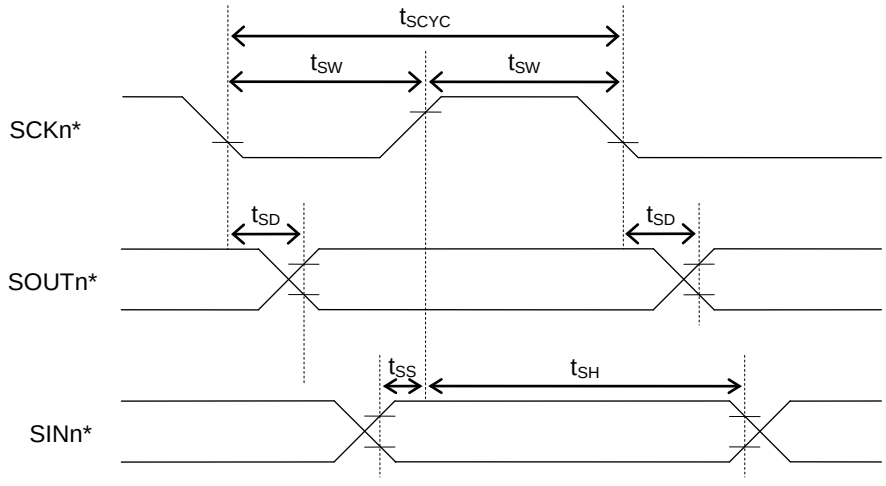


● AC Characteristics (Synchronous Serial Port)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	ms
		When high-speed oscillation is active	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	VDD≧2.4V	—	4	—	MHz
		VDD≧2.0V	—	2	—	
SCK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	ms
		When high-speed oscillation is active	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK*1 ´ 0.4	SCK*1 ´ 0.5	SCK*1 ´ 0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIOnMOD1). (n=0,1)



*: Indicates the secondary/tertiary function of the port. n=0,1

● AC Characteristics (I^2C Bus Interface: Standard Mode 100kbps)

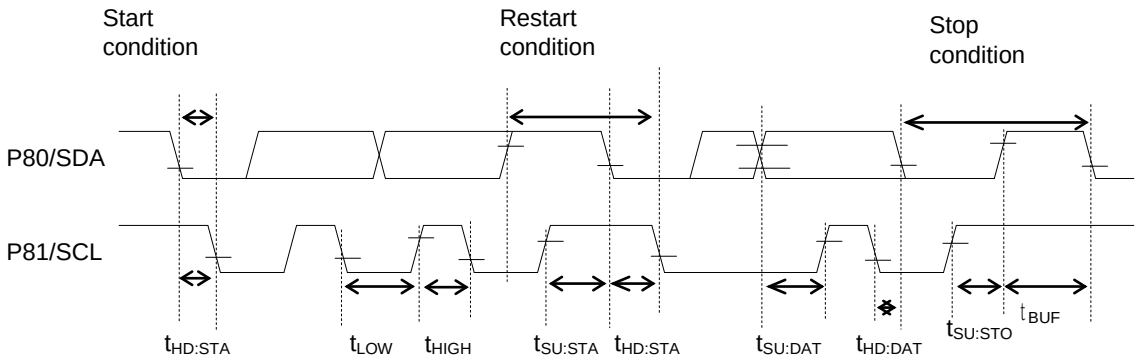
(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	¾	0	¾	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	¾	4.0	¾	¾	ms
SCL "L" level time	t_{LOW}	¾	4.7	¾	¾	ms
SCL "H" level time	t_{HIGH}	¾	4.0	¾	¾	ms
SCL setup time (restart condition)	$t_{SU:STA}$	¾	4.7	¾	¾	ms
SDA hold time	$t_{HD:DAT}$	¾	0	¾	¾	ms
SDA setup time	$t_{SU:DAT}$	¾	0.25	¾	¾	ms
SDA setup time (stop condition)	$t_{SU:STO}$	¾	4.0	¾	¾	ms
Bus-free time	t_{BUF}	¾	4.7	¾	¾	ms

● AC Characteristics (I^2C Bus Interface: Fast Mode 400kbps)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	¾	0	¾	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	¾	0.6	¾	¾	ms
SCL "L" level time	t_{LOW}	¾	1.3	¾	¾	ms
SCL "H" level time	t_{HIGH}	¾	0.6	¾	¾	ms
SCL setup time (restart condition)	$t_{SU:STA}$	¾	0.6	¾	¾	ms
SDA hold time	$t_{HD:DAT}$	¾	0	¾	¾	ms
SDA setup time	$t_{SU:DAT}$	¾	0.1	¾	¾	ms
SDA setup time (stop condition)	$t_{SU:STO}$	¾	0.6	¾	¾	ms
Bus-free time	t_{BUF}	¾	1.3	¾	¾	ms

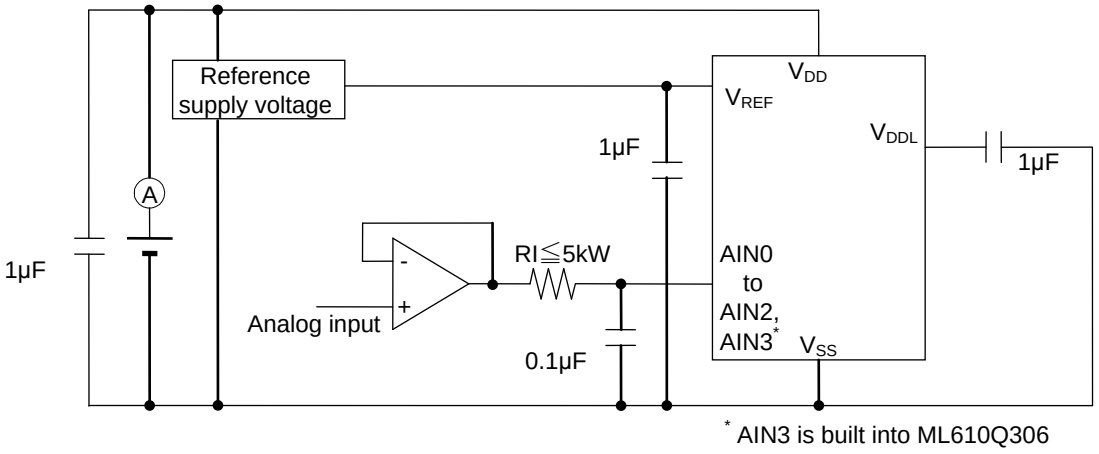


● Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD}=SPV_{DD}=2.2 to 5.5V, V_{REF}=2.2 to 5.5V, V_{SS}=SPV_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	10	bit
Integral non-linearity error	IDL	2.7V≤V_{REF}≤5.5V	- 4	—	+4	LSB
		2.2V≤V_{REF}＜2.7V	- 5	—	+5	
Differential non-linearity error	DNL	2.7V≤V_{REF}≤5.5V	- 3	—	+3	
		2.2V≤V_{REF}＜2.7V	- 4	—	+4	
Zero-scale error	V_{OFF}	R_I≤5kΩ	- 4	—	+4	
Full-scale error	FSE	R_I≤5kΩ	- 4	—	+4	
Prefilter resistance	R_I	—	—	—	5k	Ω
Reference supply voltage	V_{REF}	—	2.2		V_{DD}	V
Conversion time	t_{CONV}	HSCLK=4M to 8.4MHz	—	102	—	f /CH

f : Period of high-speed clock (HSCLK)



* AIN3 is built into ML610Q306

Appendix D The example of an application circuit

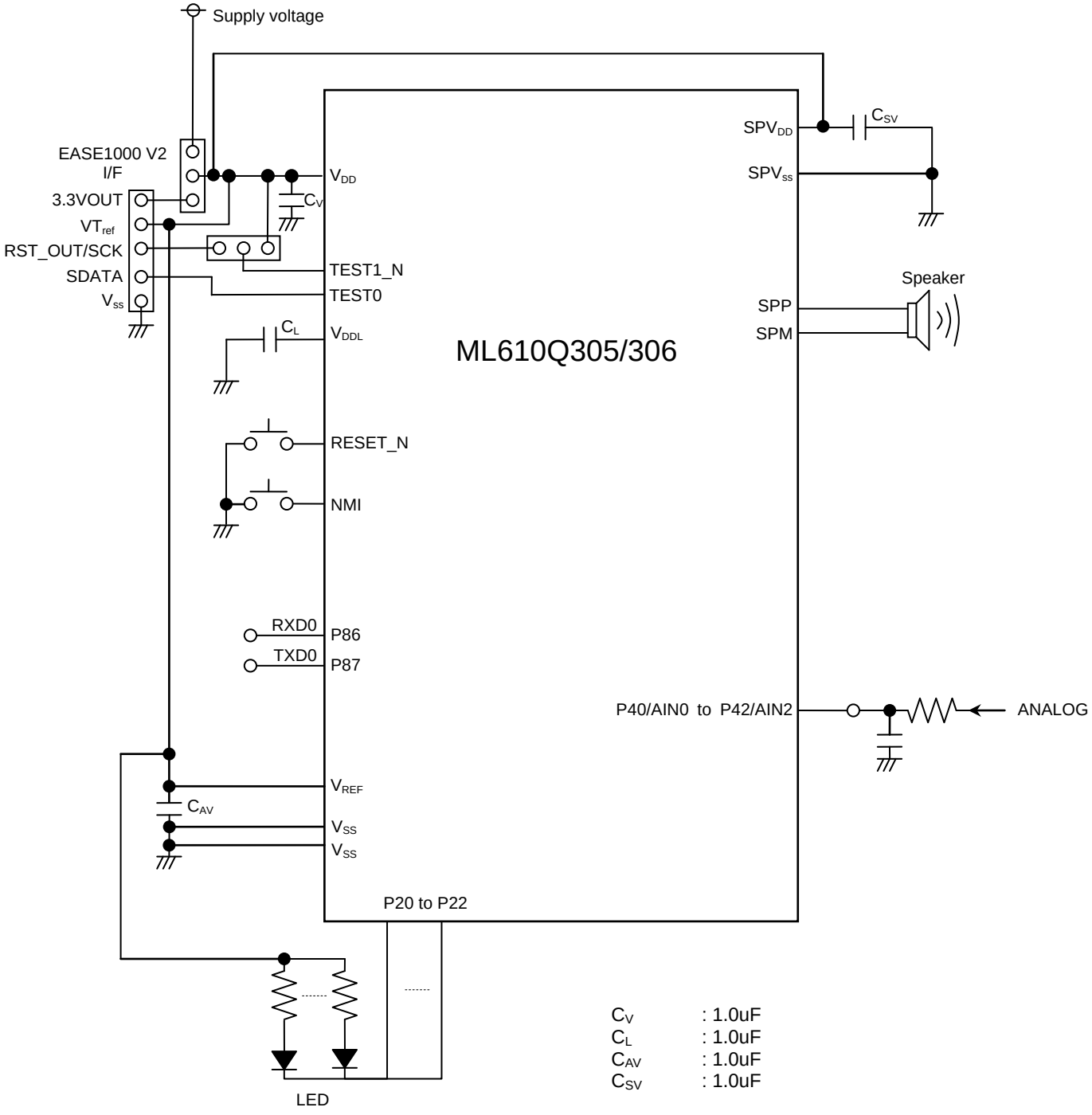


Figure 1 V_{DD} and SPV_{DD} are supplied from same power supply

Note:
Design the PCB layout having the shortest wiring distance between V_{DDL} pin and V_{DDL} pin's external capacitor (C_L), and between V_{DDL} pin's external capacitor (C_L) and V_{SS} for noise reduction purpose.

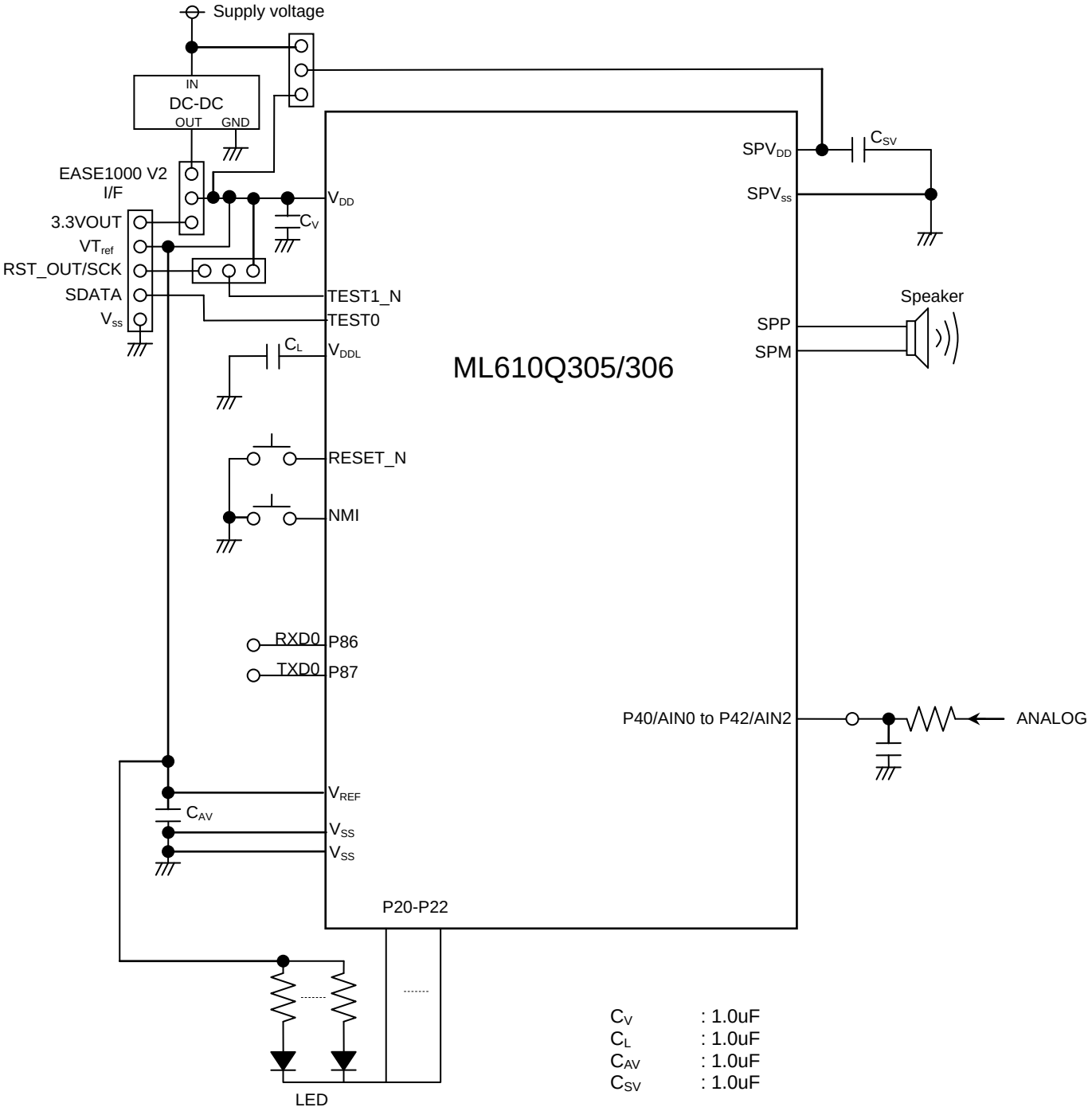


Figure 2 V_{DD} is supplied through DC-DC converter from SPV_{DD}

Note:
Design the PCB layout having the shortest wiring distance between V_{DDL} pin and V_{DDL} pin's external capacitor (C_L), and between V_{DDL} pin's external capacitor (C_L) and V_{SS} for noise reduction purpose.

Appendix E Check List

This Check List has notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware features of the MCU. Check each note listed up chapter by chapter while coding the program or evaluating it using the MCU.

Chapter 1 Overview

•About unused pins

[ ] Please confirm how to handle the unused pins(Please refer to Section 1.3.4 in the user's manual).

[ ] The unused input ports or unused input/output ports should not be configured as high-impedance inputs and left open. If the corresponding pins are configured as high-impedance inputs and left open, because the input buffer of both Nch and Pch MOS transistor turn on, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

[ ] When the power is turned on, the state of the general-purpose port is undefined. Therefore, there is a possibility of outputting high-level or low-level.If the undefined state at the power-on is a problem, take measures with the peripheral components on the user board.

Chapter 2 CPU and Memory Space

•Program Code size

[ ] 97,280 Byte (0:0000H to 0:0FBFFH, 1:0000H to 1:7FFFH)

•Data Memory size

[ ] 100,352 Byte (0:0000H to 1:7FFFH, 2:0000H to 2:07FFH)

•Data RAM size

[ ] 1,024 Byte (0:0E000H to 0:0E3FFH)

•Unused area

[ ] Please fill test area 0:FC00H to 0:FDDFH and 0:0FDE2H to 0:0FDFFH with BRK instruction code "0FFH" (Refer to a startup file "ML610305.asm" / "ML610306.asm" for programming in the source code).

[ ] Set code options in the test area 0:0FDE0H to 0:0FDE1H.

[ ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH". We will fill the area with the code "0FFH" at LAPIS Semiconductor's factory programming.

•RAM initialization

[ ] The hardware reset does not initialize RAM. Please initialize RAM by the software.

Chapter 3 Clock Generation Circuit

•Initial System clock

[ ] At power up or system reset, the 16.384MHz PLL clock oscillates and 1.024MHz clock which is 1/16 of 16.384MHz is supplied to CPU as the system clock.

•Switching high-speed clock operation mode to low-speed clock operation mode

[ ] When switching the high-speed clock to the low-speed clock after the recovery from the STOP mode, make sure the low-speed clock is oscillating checking to see the low-speed time base counter's interrupt request (128Hz interrupt request: Q128H) bit becomes "1".

•Port secondary function setting

[ ] Specify the secondary function for the port when driving a clock to the pin.

Chapter 4 Reset Function

•Reset activation pulse width

[ ] Minimum 100us (Please refer to Appendix C-8 in the user's manual)

[ ] No flag is provided that indicates the occurrence of reset by the RESET_N pin (Please refer to section 4.2.2. in the user's manual).

•Power-on reset activation power rise time

[ ] Maximum 10ms (Please refer to Appendix C-8 in the User`s Manual).

•BRK instruction reset

[ ] In system reset by the BRK instruction, no special function register (SFR) is initialized either. Therefore, initialize the SFRs by your software (Please refer to Section 4.3.1 in the User's Manual).

Chapter 5 MCU Control Function

•STOP mode

[ ] When the MIE flag is "0", the stop code acceptor (STPACP) cannot be enabled under the condition where both the interrupt enable and request flags become "1" (Refer to Sections 5.2.2 and 5.2.3. in the user's manual).

[ ] Place two NOP instructions next to the instruction that sets the STP bit to "1" (Please refer to Section 5.3.3. in the user's manual).

•HALT mode

[ ] Place two NOP instructions next to the instruction that sets the HLT bit to "1" (Please refer to Section 5.3.2. in the user's manual).

•BLKCON register

[ ] BLKCON registers enable or disable corresponsive each peripheral (Please refer to Section 5.2.4 - 5.2.7. in the user's manual).

[ ] When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.

Chapters 6 to 8, and 24 Port

•Pin Handling

[ ] Don't leave Hi-impedance Input ports in floating state.

[ ] When using P40-P42 and P43(*) as the analog input of the successive approximation A/D converter, set to the high impedance state.

•Port secondary/tertiary Function

[ ] Specify properly PnCON0/1 and PnMOD0/1 registers for each port.

(*) : P43 pin is built into ML610Q306.

Chapter 9 Interrupts(INTs)

•Unused interrupt vector table

[ ] Please define all unused interrupt vector tables for fail safe.

•Non-maskable interrupt

[ ] The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that does not depend on MIE flag (Please refer to Sections 9.2.9. and 9.3 in the User's Manual).

Chapter 11 Time Base Counter

•HTBCLK

[ ] When using the HTBCLK for a timer, set an arbitrary dividing ratio in the high-speed side time base counter frequency divide register (HTBDR register) (Please refer to Section 11.2.3. in the User's Manual).

•How to read LTBC

[ ] Read consecutively LTBC(Low-speed Time Base Counter) twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock (Please refer to Section 11.3.1 in the user's manual).

Chapter 12 Timers

•How to read the timer counter registers

[ ] Check notes for reading the timer counter registers while counting up (Please refer to Sections 12.2.6 to 12.2.9 in the user's manual).

Chapter 13 Watchdog Timer

•Overflow period

Clear WDT during the selected overflow period:

[ ] 125ms, [ ] 500ms, [ ] 2s, [ ] 8s

•WDP

[ ] Check the WDP content before writing to the WDTCON register, then determine writing whether "5AH" or "0A5H" (Please refer to Section 13.2.2. in the user's manual).

Chapter 14 Synchronous Serial Port

•Pins used

[ ] P40(SIN0), P41(SCK0) and P42(SOUT0) are used.

[ ] P80(SIN0), P81(SCK0) and P82(SOUT0) are used.

[ ] P40(SIN1), P41(SCK1) and P42(SOUT1) are used.

[ ] P84(SIN1), P85(SCK1) and P86(SOUT1) are used.

•Port secondary/tertiary function setting

[ ] Specify the secondary or tertiary Function for the port(Please refer to Section 14.4 in the user's manual).

Chapter 15 UART

•Pins used

[ ] P86(RXD0) is used.

[ ] P87(TXD0) is used.

•Port secondary function setting

[ ] Specify the secondary Function for the port(Please refer to Section 15.4 in the user's manual).

Chapter 16 I²C Bus Interface(master)

•Pins used

[ ] P80(SDA) pin and P81(SCL) pin used.

•Port secondary function setting

[ ] Specify the secondary Function for the port(Please refer to Section 16.4 in the user's manual).

Chapter 17 I²C Bus Interface(slave)

•Pins used

[ ] P80(SDA) pin and P81(SCL) pin used.

•Port secondary function setting

[ ] Specify the secondary Function for the port(Please refer to Section 17.4 in the user's manual).

Chapter 18 Successive Approximation Type A/D Converter

•Operating Conditions

[ ] Please confirm voltage of operation.
V_{DD}=2.2V to 5.5V，HSCLK=3MHz～8.4MHz

[ ] Use the SA-ADC with high-speed clock oscillation (HSCLK) enabled in the frequency control register (FCON0).

[ ] When using P40-P42 and P43(*) as the analog input of the successive approximation A/D converter, set to the high impedance state.

[ ] Do not start A/D conversion with all of bits SACH2 to SACH0 and bit SACH3(*) of the SA-ADC mode register 0 (SADMOD0) and the SA-ADC mode register 1 (SADMOD1) set to "0". (Please refer to clause 18.2.9 in the user's manual.)

[ ] SA-ADC has a built-in sample-and-hold capacitance. It is required to complete charging this capacitance within sampling time. The output impedance of the signal source connected to the analog input(AINn) should be 5k ohms or less. When the output impedance cannot be 5k ohms or less, connect 0.1uF capacitance between the analog input(AINn) and V_{SS}.

[ ] When no capacitance is connected between analog input(AINn) and VSS, at the start of A/D conversion, the charge remaining in the built-in sample-and-hold capacitance is released to analog input(AINn). And the voltage of analog input(AINn) may fluctuate momentarily. When the output impedance is within 5k ohms or less, it does not affect the A/D conversion result.

(*): P43 pin and bit SACH3 are built into ML610Q306.

Chapter 19 Audio Playback Function

•Operating Conditions

[ ] When using the audio playback function, set the system clock setting to high-speed clock in the frequency control register 1 (FCON1). (Please refer to Section 19.1.2 in the user's manual)

•Error processing

[ ] When VEER becomes "1", take an appropriate step (Please refer to Section 19.2.4 in the user's manual).

•Description

[ ] Store the last data of the phrase to FIFO phrase end data register (VFEDAT) (Please refer to Section 19.3 in the user's manual).

Chapter 20 Speaker Amplifier

•Operating Conditions

[ ] The speaker pin short detection circuit operates during for the playback. Operate the speaker pin short detection circuit when the SPEN bit of the speaker amplifier control register (SPCON) is at "1" and the VCEN bit of audio playback control register (VCON). (Please refer to Section 20.2.4 in the user's manual.)

[ ] Just before SDEN bit of Speaker Pin Short Detection Control Register (SDCON) is set to "1", be sure to set address "0:0F2C9H" to "04H". Except the value "04H" is set, the operation can not be guaranteed (Please refer to Section 20.2.4 in the user's manual).

[ ] When SDEN bit of Speaker Pin Short Detection Control Register (SDCON) is set to "1", be sure to select either 64-time detection (SDA2=SDA1=1, SDA0=0) or short detection disable (SDA2=SDA1=SDA0=1) (Please refer to Section 20.2.4 in the user's manual).

[ ] Operate the disconnection detection circuit when the SPEN bit of the speaker amplifier control register (SPCON) is at "0" (Please refer to Section 20.3.2 in the user's manual).

Chapter 21 Flash memory self rewriting function

• Operating Conditions

[ ] Erase the contents of the target addresses in advance. The content of an overwritten address is not guaranteed (Please refer to Section 21.2.3 in the user's manual).

[ ] Writing to FLASHDH starts the 1-word write. Write data to FLASHDL and FLASHDH in this order (Please refer to Section 21.2.3 in the user's manual).

[ ] Use it in the state that chose HSCLK as system clock after having admitted high-speed clock (HSCLK) oscillation of frequency control register (FCON1) (Please refer to Section 21.3 to 21.3.3 in the user's manual).

[ ] Be sure to set the NOP instruction twice or more, following the block/sector erase instruction and the write in command to FLASHDH (Please refer to Section 21.3.1 to 21.3.3 in the user's manual).

[ ] Please clear the WDT counter of WDT suitably (Please refer to Section 21.3.1 to 21.3.2 in the user's manual).
[ ] After writing "1" in FPRT0 to FPRT3 bit of flash protection register (FLASHPRT), block erase to 0000H to 07FFH of the segment 2 becomes invalid (Please refer to Section 21.2.8 in the user's manual).

Chapter 22 Power Supply Circuit
•External capacitor
[ ] C_L = 1uF (for V_{DDL} pin) (Please refer to Section 22.1.2 in the user's manual.)

Chapter 23 On-Chip Debug Function
• Operating Conditions
[ ] When using the on-chip debug function or flash memory reprogramming function after mounting the LSI on the board, design the board so that the four pins of V_{DD}, V_{SS}, TEST1_N, and TEST0, which are required for connection to the on-chip debug emulator, are capable of connection. Also, apply 2.0 to 5.5 V to V_{DD}. (Please refer to Section 23.2 in the user's manual.)
[ ] Please do not apply LSIs being used for debugging to mass production.
[ ] Please validate the ROM code on your production board without on-chip debug tool EASE1000 V2.

Appendix A SFR (Specific Function Registers)
•Initial value
[ ] Please confirm there are some SFRs have undefined initial value at reset (Please refer to Appendix A in the user's manual).

Appendix B Package Dimensions
•TjMax
[ ] Heat resistance (θ Ja) changes by the size and the number of layers of a substrate.(The example is shown about the heat resistance of LSI.)
TjMax of this LSI is 110 degrees. (Please refer to Appendix B in the user's manual.)

Appendix C Electrical Characteristics
•External capacitors for Power circuits
[ ] C_L=1uF （connected to V_{DDL} pin）, [ ] C_V =1uF (connected to V_{DD} pin）
[ ] C_{AV}=1uF （connected to V_{REF} pin）, [ ] C_{SV} =1uF (connected to SPV_{DD} pin）
•Operating voltage
[ ] 2.0V to 5.5V
•Operating temperature
[ ] -40'C to +85'C

<u>The code last confirm environment</u>
[ ] A confirm of a program cord of operation is on a user's mass production board, and please confirm it in the condition that disconnect on-chip debug tool EASE1000 V2 of our company.

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL610Q306-01	Jun. 28,2021	–	–	Formal edition 1