Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5204

Analog Front-End IC for 4 to 5-Serial-Cell Lithium-Ion Rechargeable Battery Protection

■ General Description

The ML5204 is an analog front-end type battery monitoring LSI for a host controller in 4- to 5-cell Li-ion rechargeable battery packs. It outputs individual analog cell voltages and pack current equivalent voltage, while cell balancing, overvoltage/undervoltage detection, and overcurrent detection functions are integrated for configuring high-precision/high-reliability battery management systems.

■ Features

- Supported number of cells: 4 to 5 cells
- Analog cell voltage output: Individual analog cell voltage is divided by 2 and output on the VMON pin.
- Analog pack current output: The voltage across the shunt resistor is amplified by x12 or x24 and output on the IMON pin
- Cell balancing function: Built-in cell balancing switches with a 6Ω (typ) ON resistance
- Overvoltage/undervoltage detection function:
  - Overvoltage detection accuracy : ±20 mV (25 °C)
  - 2nd overvoltage detection accuracy : ±35 mV (25 °C)
  - Undervoltage detection accuracy : ±50 mV (25 °C)
  - Zero voltage (0-V) charge inhibit detection accuracy : ±50 mV (25 °C)
- Charge/discharge overcurrent detection function
  - Discharge overcurrent detection accuracy : ±10 mV (25 °C)
  - Charge overcurrent detection accuracy : ±10 mV (25 °C)
- Short-Circuit detection function:
  - Short-circuit detection accuracy : ±10 mV (25 °C)
- Wake-up detection function: Asserts an interrupt signal to the external MCU when a predefined discharge current is detected.
- Cell count, detection thresholds and delay times can be redefined and supplied under a separate product code
- MCU interface: I2C compatible serial interface
- Low current consumption
  - Cell voltage/current monitor active : 14 µA (typ), 50 µA (max)
  - Cell voltage/current monitor inactive : 6 µA (typ), 10 µA (max)
- High voltage supply input : +53 V (absolute maximum rating)
- Operating power supply range : +3.3 V to +42 V
- Operating temperature : -40 °C to +85 °C
- Package : 20-pin TSSOP

■ Application

・Power tools and Garden tools
・Cordless Cleaner

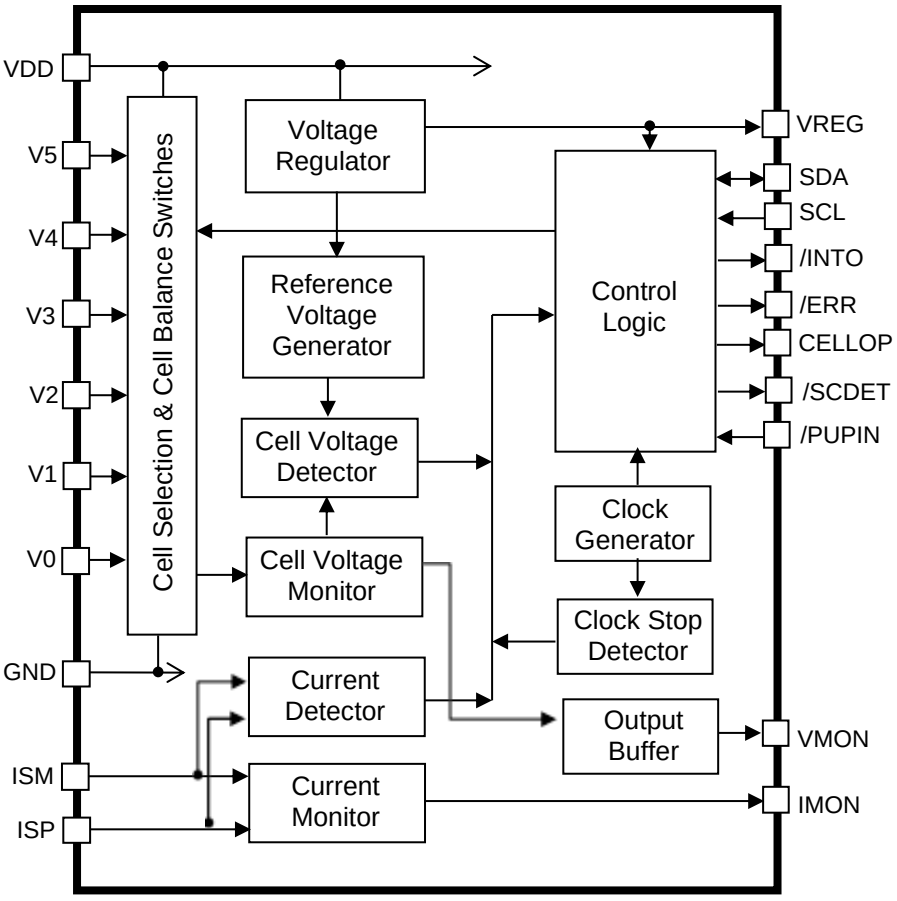
■ Part number

ML5204-001TD

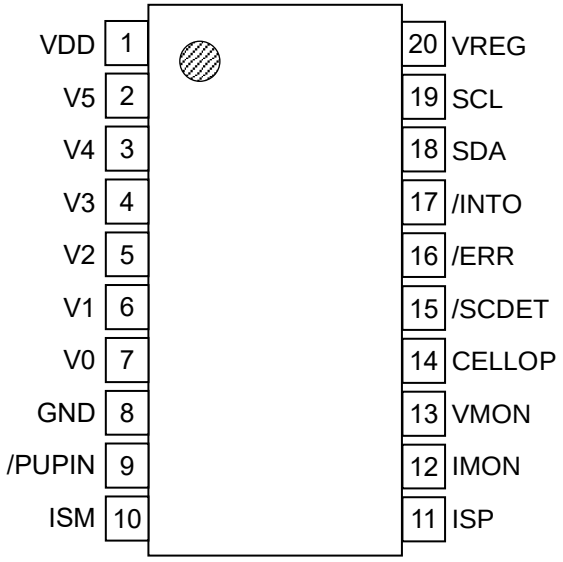
.

ROHM SEMICONDUCTOR

■ Block Diagram



■ Pin Configuration (Top View)



■ Pin Description

Pin No.	Pin name	I/O	Description
1	VDD	—	Power supply. Configure an external CR noise filter circuit.
2	V5	I	Cell 5 positive input.
3	V4	I	Cell 5 negative input and Cell 4 positive input.
4	V3	I	Cell 4 negative input and Cell 3 positive input.
5	V2	I	Cell 3 negative input and Cell 2 positive input.
6	V1	I	Cell 2 negative input and Cell 1 positive input.
7	V0	I	Cell 1 negative input.
8	GND	I	Ground pin.
9	/PUPIN	I	Power-up trigger input. The device wakes up with an "L" level input. Internally pulled up to VDD through a 1 MΩ resistor. Connect a 0.1 μF capacitor between this pin and GND.
10	ISM	I	Current sense negative input. Connected to the negative terminal of the lowest battery cell.
11	ISP	I	Current sense positive input. The ISP pin level should be higher than the ISM pin level in discharge state.
12	IMON	O	Analog current monitor output. The input voltage difference between the ISP and ISM pins is amplified by 12-/24-fold on output.
13	VMON	O	Analog cell voltage output. The specified cell voltage is divided by 2 on output.
14	CELLOP	O	2nd overvoltage alarm output. Output type is NMOS open drain, and the "L" level is asserted at 2nd overvoltage conditions.
15	/SCDET	O	Short-circuit alarm output. Output type is NMOS open drain, and the "L" level is asserted if short-circuit is detected.
16	/ERR	O	Error state alarm output. Output type is NMOS open drain, and the "L" level is asserted if any error is detected.
17	/INTO	O	Interrupt signal to an external MCU. Output type is NMOS open drain, and the "L" level is asserted when an interrupt request occurs.
18	SDA	IO	Serial data input/output pin. Connect an external pull-up resistor.
19	SCL	I	Serial clock input pin. Connect an external pull-up resistor.
20	VREG	O	Internal 3.3 V regulator output pin. Connected to GND through a 1 μF or larger capacitor. Do not use as a power supply for external circuit.

■ Absolute Maximum Ratings

GND= 0 V, Ta = +25 °C

Item	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD pin	-0.3 to +53	V
Input voltage	V_{IN1}	Applied to V5 to V0 pins Voltage difference between Vn+1 and Vn pins (Note 1)	-0.3 to +6.5	V
	V_{IN2}	Applied to /PUPIN pin	-0.3 to V_{DD}+0.3	V
	V_{IN3}	Applied to ISM and ISP pins	-0.3 to V_{REG}+0.3	V
	V_{IN4}	Applied to SCL and SDA pins	-0.3 to +6.5	V
Output voltage	V_{OUT1}	Applied to /SCDET, CELLOP, /ERR, /INTO, SDA, VREG pins	-0.3 to +6.5	V
	V_{OUT2}	Applied to VMON and IMON pins	-0.3 to V_{REG}+0.3	V
Cell balancing current	I_{CB}	Per cell balancing switch	200	mA
Power dissipation	P_D	—	1.0	W
Short-circuit output current	I_{OS}	Applied to /SCDET, CELLOP, /ERR, /INTO, SDA, VREG, VMON, IMON pins	10	mA
Storage temperature	T_{STG}	—	-55 to +150	°C

Note 1: When connecting or removing a battery cell, the Vn+1-to-Vn pin voltage may exceed the specified rating, leading to destruction of the device. Make a full and detailed evaluation before usage.

■ Recommended Operating Conditions

GND= 0 V

Item	Symbol	Conditions	Range	Unit
Supply voltage	V_{DD}	Applied to VDD pin	3.3 to 42	V
Operating temperature	T_{OP}	—	-40 to +85	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD}=3.3 V to 42 V, GND=0 V, Ta=-40 to +85 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage (Note 1)	V_{IH}	—	0.7×V_{REG}	—	3.6	V
"L" input voltage (Note 1)	V_{IL}	—	0	—	0.3×V_{REG}	V
"H" input current (Note 1)	I_{IH}	V_{IH} = 3.3 V	—	—	2	µA
"L" input current (Note 1)	I_{IL}	V_{IL} = GND	–2	—	—	µA
Cell voltage monitor pin input current 1	I_{INV1}	In normal operation Cell voltage monitor inactive Cell balancing switch OFF	—	0.1	1.5	µA
Cell voltage monitor pin input current 2	I_{INV2}	Each cell voltage = 4 V Cell voltage monitor active Cell balancing switch OFF	–0.5	—	3.5	µA
Cell voltage monitor pin input leakage current	I_{ILVC}	In power-down	–0.5	—	0.5	µA
"L" output voltage (Note 2)	V_{OL}	I_{OL} = 1 mA	—	—	0.2	V
Output leakage current (Note 2)	I_{OLK}	V_{OUT}= 0 V to 4 V	–2	—	2	µA
/PUPIN pin "H" input voltage	V_{IHP}	—	0.8×V_{DD}	—	V_{DD}	V
/PUPIN pin "L" input voltage	V_{ILP}	—	0	—	0.2×V_{DD}	V
/PUPIN pin "H" input current	I_{IHP}	V_{IH} = V_{DD}	—	—	5	µA
/PUPIN pin "L" input current	I_{ILP}	VDD=18 V V_{IL} = GND	–36	–18	–9	µA
VREG pin output voltage	V_{REG1}	VDD=5 V to 42 V Output load current < 0.5 mA	3.0	3.3	3.6	V
	V_{REG2}	VDD=3.3 V to 5 V Output load current < 100 µA	3.0	3.3	3.6	V
Cell balancing switch ON resistance	R_{CB}	VDD=15 V to 42 V VDS=0.6 V	3	6	12	Ω

Note 1: Applied to SCL and SDA pins.
Note 2: Applied to SDA, /SCDET, CELLOP, /ERR, /INTO pins.

● Supply Current Characteristics

V_{DD} = 3.3 to 42 V, GND = 0 V, Ta = -40 to +85 °C, no output load, /PUPIN = "H"

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current during operation 1	I_{DD1}	Cell voltage/current monitor output active Ta=0 to +60 °C	—	14	50	µA
Supply current during operation 2	I_{DD2}	Cell voltage/current monitor output inactive Ta=0 to +60 °C	—	6	10	µA
Current consumption during powered-down	I_{DDS}	—	—	0.1	1.0	µA

● Code 001: Detection Threshold Characteristics (Ta = 25 °C)

V_{DD}=18 V, GND=0 V, Ta=+25 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.205	4.225	4.245	V
Overvoltage release threshold	V_{OVR}	—	3.975	4.025	4.075	V
2nd overvoltage detection threshold	V_{SOV}	—	4.265	4.30	4.335	V
Undervoltage detection threshold	V_{UV}	—	1.55	1.6	1.65	V
Undervoltage release threshold	V_{UVR}	—	2.925	3.000	3.075	V
0-V charge inhibit threshold	V_{CNG}	—	0.95	1.00	1.05	V
Discharge overcurrent detection threshold	V_{OCU}	—	110	120	130	mV
Charge overcurrent detection threshold	V_{OCO}	—	-50	-40	-30	mV
Short-circuit detection threshold	V_{SC}	—	190	200	210	mV
Wake-up detection threshold	V_{WK}	When current monitoring is stopped	2.5	5	7.5	mV

● Code 001: Detection Threshold Characteristics (Ta = 0 to 60 °C)

V_{DD}=18 V, GND=0 V, Ta=0 °C to +60 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	Ta=10 °C to 45 °C	4.200	4.225	4.250	V
Overvoltage release threshold	V_{OVR}	—	3.955	4.025	4.095	V
2nd overvoltage detection threshold	V_{SOV}	—	4.25	4.30	4.35	V
Undervoltage detection threshold	V_{UV}	—	1.5	1.6	1.7	V
Undervoltage release threshold	V_{UVR}	—	2.9	3.0	3.1	V
0-V charge inhibit threshold	V_{CNG}	—	0.95	1.00	1.05	V
Discharge overcurrent detection threshold	V_{OCU}	—	105	120	135	mV
Charge overcurrent detection threshold	V_{OCO}	—	-55	-40	-25	mV
Short-circuit detection threshold	V_{SC}	—	185	200	215	mV
Wake-up detection threshold	V_{WK}	When current monitoring is stopped	2	5	8	mV
VREG drop threshold	V_{UREG}	—	2.2	2.5	2.8	V
VREG recovery threshold	V_{RREG}	—	2.4	2.7	3.0	V

● Code 001: Detection/Release Delay Time Characteristics (Ta = 25 °C)

V_{DD}=18 V, GND=0 V, Ta=+25 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cell voltage monitor cycle	t_{DET}		0.32	0.40	0.48	sec
Overvoltage detection delay time (Note)	t_{OV}	—	3.8	4.8	5.8	sec
Overvoltage release delay time (Note)	t_{OVR}	—	0.6	0.8	1.0	sec
2nd overvoltage detection delay time (Note)	t_{SOV}	—	12.8	16	19.2	sec
Undervoltage detection delay time (Note)	t_{UV}	—	3.8	4.8	5.8	sec
Undervoltage release delay time (Note)	t_{OVR}	—	0.6	0.8	1.0	sec
0-V charge inhibit delay time (Note)	t_{CNG}	—	6.9	8	9.5	sec
0-V charge enable delay time (Note)	t_{CNGR}	—	0.6	0.8	1.0	sec
Discharge overcurrent detection delay time	t_{OCU}	—	40	50	60	ms
Discharge overcurrent release delay time	t_{OCUR}	—	80	100	120	ms
Charge overcurrent detection delay time	t_{OCO}	—	20	25	30	ms
Charge overcurrent release delay time	t_{OCOR}	—	80	100	120	ms
Short-circuit detection delay time	t_{SC}	—	60	100	180	µs
Short-circuit release delay time	t_{SCR}	—	80	100	120	ms
Wake-up detection delay time	t_{WK}	—	1.6	2	2.6	ms

(Note) The actual detection delay time may include the time lag incorporated by the cell voltage monitor cycle.

● Code 001: Detection/Release Delay Time Characteristics (Ta = 0 to 60 °C)

V_{DD}=18 V, GND=0 V, Ta=0 to +60 °C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cell voltage monitor cycle	t_{DET}		0.3	0.4	0.5	sec
Overvoltage detection delay time (Note)	t_{OV}	—	3.6	4.8	6.0	sec
Overvoltage release delay time (Note)	t_{OVR}	—	0.6	0.8	1.0	sec
2nd overvoltage detection delay time (Note)	t_{SOV}	—	12	16	20	sec
Undervoltage detection delay time (Note)	t_{UV}	—	3.6	4.8	6.0	sec
Undervoltage release delay time (Note)	t_{OVR}	—	0.6	0.8	1.0	sec
0-V charge inhibit delay time (Note)	t_{CNG}	—	6.6	8	9.8	sec
0-V charge enable delay time (Note)	t_{CNGR}	—	0.6	0.8	1.0	sec
Discharge overcurrent detection delay time	t_{OCU}	—	37	50	63	ms
Discharge overcurrent release delay time	t_{OCUR}	—	74	100	126	ms
Charge overcurrent detection delay time	t_{OCO}	—	18	25	32	ms
Charge overcurrent release delay time	t_{OCOR}	—	74	100	126	ms
Short-circuit detection delay time	t_{SC}	—	50	100	200	µs
Short-circuit release delay time	t_{SCR}	—	74	100	126	ms
Wake-up detection delay time	t_{WK}	—	1.4	2	2.8	ms

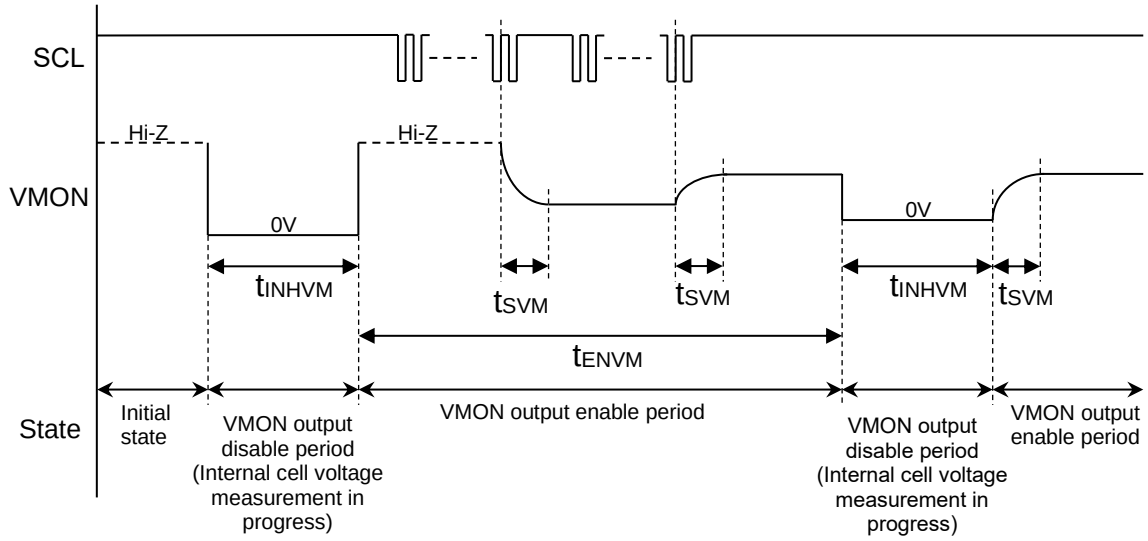
(Note) The actual detection delay time may include the time lag incorporated by the cell voltage monitor cycle.

● Cell Voltage Monitor Output Characteristics (Ta = 0 to 60 °C)

V_{DD} = 18 V, GND = 0 V, Ta = 0 to +60 °C, no VMON output load

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cell voltage monitor range	V_{VMR}	—	0.1	—	4.5	V
VMON output voltage	V_{CELO4}	When cell voltage = 4 V	1.96	2.00	2.04	V
	V_{CELO1}	When cell voltage = 1 V	0.4	0.5	0.6	V
Cell voltage measurement error (Note)	V_{ECEL4}	When cell voltage = 4 V	-25	—	+25	mV
	V_{ECEL1}	When cell voltage = 1 V	-30	—	+30	mV
VMON output current	I_{OVM}	—	-100	—	+100	µA
VMON output disable period	t_{INHVM}	—	40	50	65	ms
VMON output enable period	t_{ENVM}	—	290	350	450	ms
VMON output stabilization time	t_{SVM}	No output load	—	—	1	ms

(Note) Cell voltage is corrected in the following formula with the VGAIN and OFFSET register values:
Corrected cell voltage = VGAIN × [VMON output voltage] + OFFSET

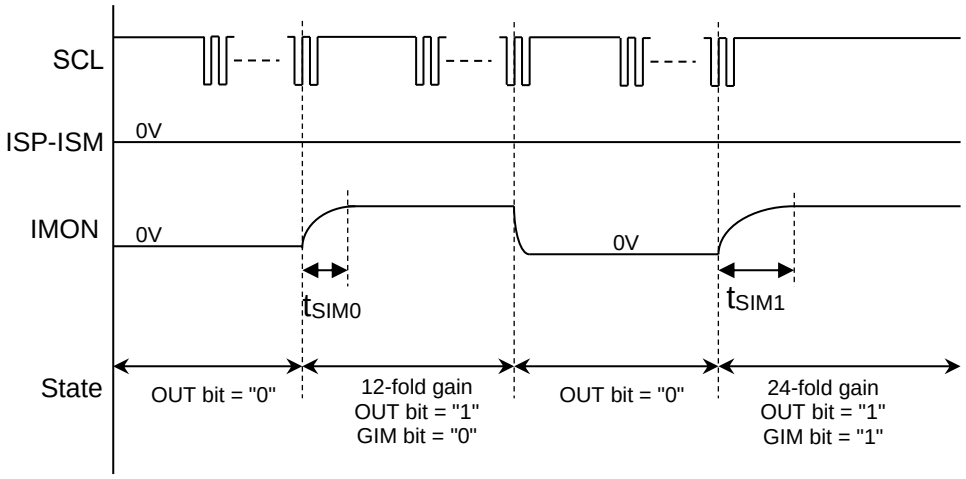


● Code 001: Current Monitor Output Characteristics (Ta = 0 to 60 °C)

V_{DD} = 18 V, GND = 0 V, Ta = 0 to +60 °C, no IMON output load

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
IMON output voltage	V_{IMON0}	ISP-to-ISM voltage difference = 0 V GIM bit = "0"	0.5	0.6	0.7	V
	V_{IMON1}	ISP-to-ISM voltage difference = 0 V GIM bit = "1"	0.4	0.6	0.8	V
IMON output gain (Note)	G_{IM0}	GIM bit = "0"	11.4	12	12.6	V/V
	G_{IM1}	GIM bit = "1"	22.8	24	25.2	V/V
Current measurement range (Note)	R_{IM0}	GIM bit = "0" Shunt resistor R_{IS} = 0.5 mΩ	-365	—	+63	A
	R_{IM1}	GIM bit = "1" Shunt resistor R_{IS} = 0.5 mΩ	-174	—	+23	A
IMON output current	I_{OIM}	—	-100	—	+100	µA
ISP and ISM pin input current (Note)	I_{IS}	ISP=ISM=0 V OUT bit = "1" GIM bit = "0"	0.25	0.46	0.8	µA
IMON output stabilization time	t_{SIM0}	GIM bit = "0"	—	—	1	ms
	t_{SIM1}	GIM bit = "1	—	—	3	ms

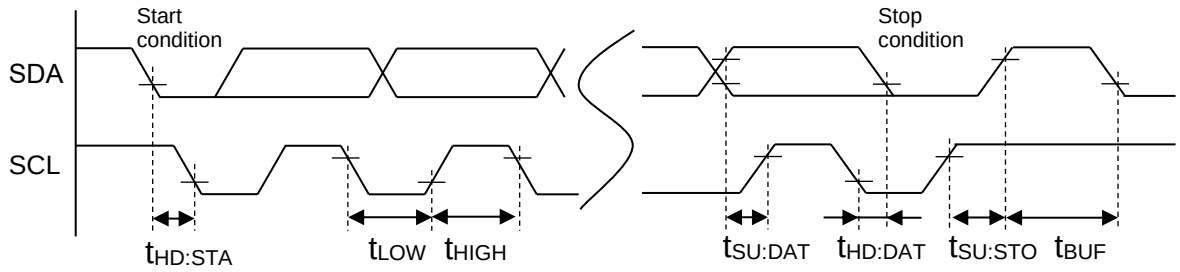
(Note) A shunt resistor is connected to the ISP and ISM pins via a 1 kΩ resistor each.



● I2C Compatible Serial Interface

V_{DD}=3.3 to 42 V, GND=0 V, Ta=-40 to +85 °C

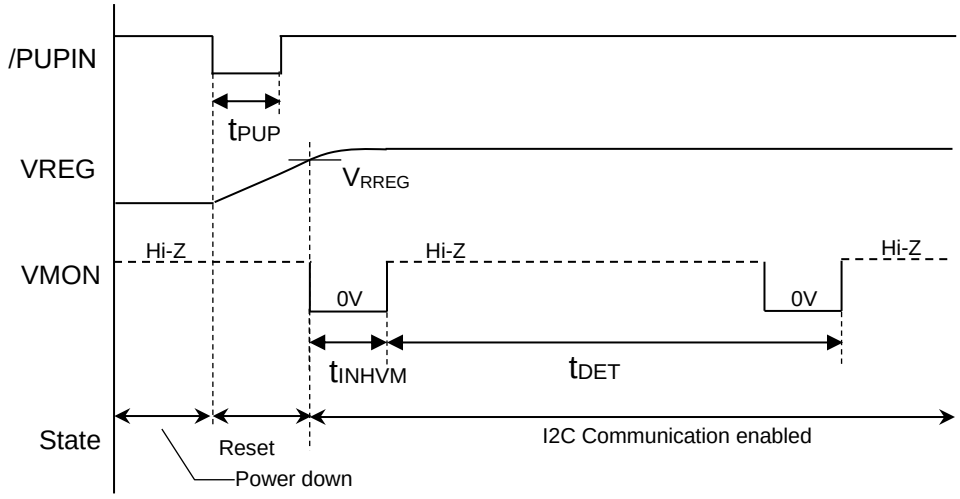
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	—	—	400	kHz
SCL hold time (Start condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" hold time	t_{LOW}	—	1.3	—	—	µs
SCL "H" hold time	t_{HIGH}	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (Stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus free time	t_{BUF}	—	1.3	—	—	µs



● Power-up Timing

V_{DD}=3.3 to 42 V, GND=0 V, Ta=-40 to +85 °C

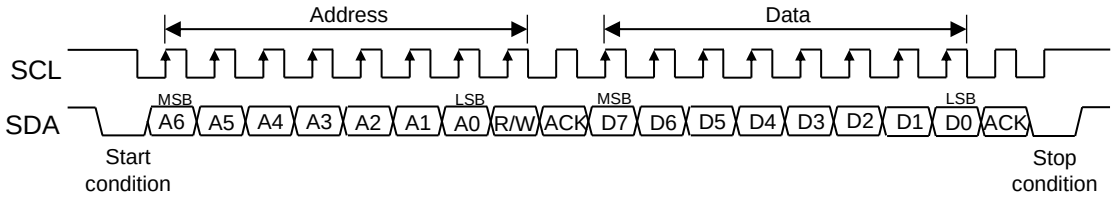
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
/PUPIN "L" pulse width	t_{PUP}	—	1	—	—	ms



■ Functional Description

● I2C Compatible Serial Interface

The ML5204 is equipped with an I2C compatible serial interface.
Configurations can be done by reading/writing corresponding addresses in the control register.



Set the RW bit to "0" for data write or "1" for data read.

● Control Register

The control register map is shown below.

Address	Register name	R/W	Default	Description
00H	NOOP	R/W	00H	No function is assigned.
01H	VMON	R/W	00H	Cell voltage monitor control
02H	IMON	R/W	00H	Current monitor control
03H	CBAL	R/W	00H	Cell balancing switch control
04H	POWER	R/W	00H	Power-down/Wake-up control
05H	INTREQ	R	00H	Interrupt request flags
06H	ERROR	R	02H	Error state flags
07H	VGAIN	R	—	VMON output voltage gain
08H	OFFSET	R	—	VMON output voltage offset
09H	TEST	R/W	00H	Detection delay time reduction for tests CELLOP state control
Others	NOT_USE	R/W	00H	Reserved for IC production test (Do not use)

1. NOOP Register (Adrs = 00H)

Bit	7	6	5	4	3	2	1	0
	NO7	NO6	NO5	NO4	NO3	NO2	NO1	NO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

No function is assigned to the NOOP register. Read/write access to this register does not change the LSI state. The written data can be read as it is.

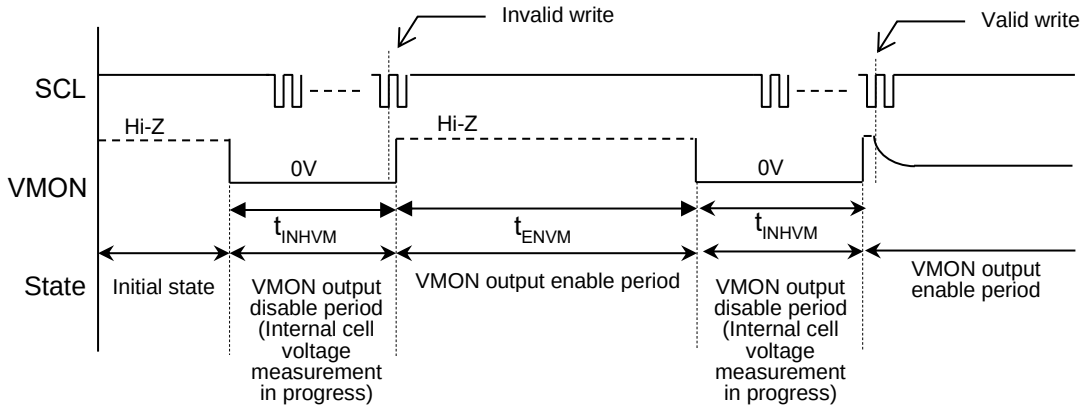
2. VMON Register (Adrs = 01H)

Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	CN2	CN1	CN0
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The VMON register specifies the battery cell to monitor on the VMON pin.
The CN0, CN1, and CN2 bits select the battery cell.

CN2	CN1	CN0	Selected cell
0	0	0	None (default) VMON output = Hi-Z
0	0	1	V1 cell (lowermost)
0	1	0	V2 cell
0	1	1	V3 cell
1	0	0	V4 cell
1	0	1	V5 cell (uppermost)
1	1	0	None VMON output = Hi-Z
1	1	1	

Data write to the VMON register during the VMON output disable period is ignored, thus the present register value is kept.



3. IMON Register (Adrs = 02H)

Bit	7	6	5	4	3	2	1	0
	—	—	—	OUT	—	—	ZERO	GIM
R/W	R	R	R	R/W	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

The IMON register specifies various conditions for pack current monitor output.
The GIM bit selects the voltage gain of the current amplifier.

GIM	Voltage gain G_{IM}
0	12 times (default)
1	24 time

The ZERO bit selects input levels on the ISP and ISM pins to perform zero current compensation on the current amplifier.

ZERO	ISP pin input level	ISM pin input level
0	Pin input level	Pin input level
1	GND level	GND level

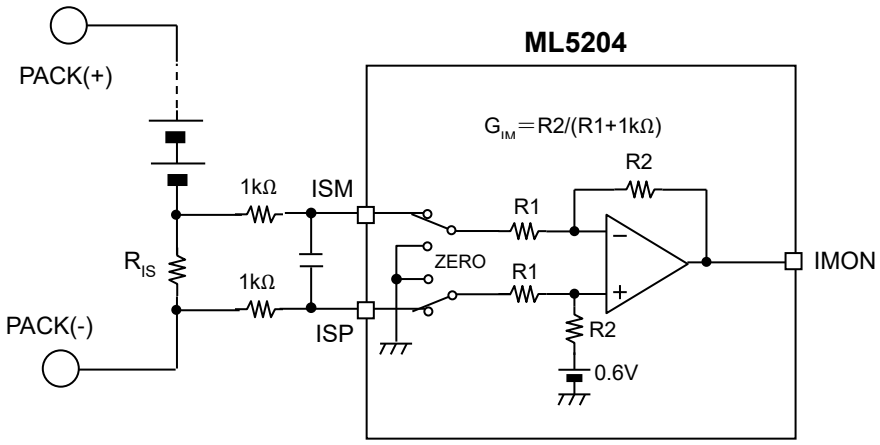
The OUT bit enables the current amplifier output on the IMON pin. The OUT bit should be set to "1" when zero current compensation is performed as well.

OUT	IMON pin output level
0	0V(default)
1	Current amplifier output

Pack current is obtained as the voltage across the current sensing shunt resistor R_{IS}, which is tied to the ISP and ISM pins.
The voltage difference between the ISP and ISM pins is converted and centered to 0.6 V (typ), which is asserted on the IMON pin. The IMON pin output voltage V_{IMON} is given by the following formula using the shunt resistance R_{IS} and the pack current I_{SENSE}:

$$V_{IMON} = (I_{SENSE} \times R_{IS}) \times G_{IM} + 0.6$$

The circuit configuration of the current amplifier is shown below.



V_{IMON} = 0.6 V for zero current, V_{IMON} > 0.6 V for discharge current, and V_{IMON} < 0.6 V for charge current.
When ZERO bit = "1", the ISM and ISP pins are fixed to the GND level inside the device so that the input voltage difference of the current amplifier becomes zero. By using this IMON level as the

reference for zero current, internal reference deviation from 0.6 V and offset of the current amplifier can be corrected.
The charge/discharge overcurrent, short-circuit, wake-up detection characteristics are irrelevant to IMON register values.

4. CBAL Register (Adrs = 03H)

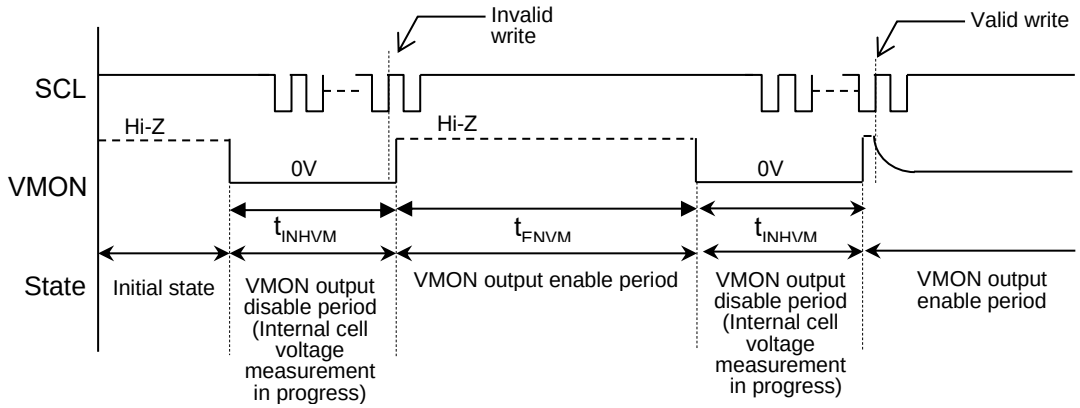
Bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	SW2	SW1	SW0
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The CBAL register controls cell balancing switches.
The SW0, SW1, and SW2 bits select the cell balancing switch to turn ON.
When changing switches, all switches should be turned OFF first, then select a new switch to turn ON.

SW2	SW1	SW0	Switched ON cell
0	0	0	All OFF (default)
0	0	1	V1 cell (lowermost)
0	1	0	V2 cell
0	1	1	V3 cell
1	0	0	V4 cell
1	0	1	V5 cell
1	1	0	All OFF
1	1	1	

During the VMON output disable period, all the cell balancing switches are autonomously turned OFF regardless of the CBAL register setting. During the VMON output enable period, the cell balancing switch specified with the CBAL register is turned ON. Data write to the CBAL register during the VMON output disable period is ignored, thus the present register value is kept.

If a cell balancing switch is kept turned ON all the way along, it is autonomously turned OFF at the beginning of the VMON output disable period. But if the time constant of the RC input filter is too large, cell voltage recovery may be slow enough to create a false overvoltage or undervoltage condition. It is thus recommended that RCELL and CCELL values are carefully selected so that the time constant of the RC filter is 1.5 ms or shorter.



5. POWER Register (Adrs = 04H)

Bit	7	6	5	4	3	2	1	0
	PUPIN	—	—	PD	—	—	—	WKUP
R/W	R	R	R	R/W	R	R	R	R/W
Default	0	0	0	0	0	0	0	0

The POWER register specifies wake-up detection and power-down conditions.
The WKUP bit starts or stops the wake-up detection circuit. It is autonomously reset to “0” when a wake-up condition is detected.

WKUP	Wake-up circuit operation
0	Inactive (default)
1	Active

The PD bit controls transition to the power-down state. In the power-down state, all circuit operations are halted for reducing current consumption.

PD	Power-down control
0	None (Default)
1	Transition to Power-down

The PUPIN bit indicates the /PUPIN pin input level.

PUPIN	/PUPIN pin input level
0	"H"
1	"L"

If the PD bit is set to "1" while the /PUPIN pin input level is "L", transition to the power-down state is not enabled until the /PUPIN pin input level becomes "H". Therefore, make sure that the /PUPIN pin level is “H” by reading the PUPIN bit before writing “1” to the PD bit.

Writing “0” to the PD bit during power-down does not power up the device. For power-up, assert the "L" level on the /PUPIN pin.

6. INTREQ Register (Adrs = 05H)

Bit	7	6	5	4	3	2	1	0
	QWK	QSC	QOCC	QOCD	QSOV	QZV	QUV	QOV
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The INTREQ register shows the existing interrupt requests to MCU. The INTREQ register is cleared by reading it, and the /INTO output autonomously returns to “Hi-Z”.
Data write to the INTREQ register is ignored.

QOV	Overvoltage IRQ
0	None (default)
1	Present

QUV	Undervoltage IRQ
0	None (default)
1	Present

QZV	0-V charge inhibit IRQ
0	None (default)
1	Present

QSOV	2nd overvoltage IRQ
0	None (default)
1	Present

QOCD	Discharge overcurrent IRQ
0	None (default)
1	Present

QOCC	Charge overcurrent IRQ
0	None (default)
1	Present

QSC	Short-circuit IRQ
0	None (default)
1	Present

QWK	Wake-up IRQ
0	None (default)
1	Present

All bits are set to "1" when clock halt is detected.

7. ERROR Register (Adrs = 06H)

Bit	7	6	5	4	3	2	1	0
	CKER	SC	OCC	OCD	SOV	ZV	UV	OV
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	1	0

The ERROR register indicates present error states. If any one bit is set to "1", the "L" level is asserted on the /ERR pin. Each bit is autonomously reset to "0" when corresponding error condition is resolved. The /ERR pin output becomes “Hi-Z” when all the bits are "0". Data write to the ERROR register is ignored.

OV	Overvoltage condition
0	Not detected (default)
1	Detected

UV	Undervoltage condition
0	Not detected
1	Detected (default)

ZV	0-V charge inhibit condition
0	Not detected (default)
1	Detected

SOV	2nd overvoltage condition
0	Not detected (default)
1	Detected

OCD	Discharge overcurrent condition
0	Not detected (default)
1	Detected

OCC	Charge overcurrent condition
0	Not detected (default)
1	Detected

SC	Short-circuit condition
0	Not detected (default)
1	Detected

CKER	Clock halt condition
0	Not detected (default)
1	Detected

The "L" level is asserted on the CELLOP pin at 2nd overvoltage condition.

SOV	2nd overvoltage state	CELLOP pin level
0	Not detected (default)	“Hi-Z”
1	Detected	"L"

The "L" level is asserted on the /SCDET pin at short-circuit condition.

SC	Short-circuit state	/SCDET pin level
0	Not detected (default)	“Hi-Z”
1	Detected	"L"

8. VGAIN Register (Adrs = 07H)

Bit	7	6	5	4	3	2	1	0
	—	VG6	VG5	VG4	VG3	VG2	VG1	VG0
R/W	R	R	R	R	R	R	R	R
Default	—	—	—	—	—	—	—	—

The VGAIN register specifies a calibrated gain value for VMON output.
Calibrated cell voltage is given by the following equation using an A/D converted value of analog VMON output:

Cell voltage = VGAIN × [VMON output voltage] + OFFSET

, where VGAIN is a calibrated gain, and OFFSET is a deviation from zero voltage.

The following table shows the relationship between the VGAIN register value and the calibrated gain.

Register value [Hex]	Calibrated Gain	Register value [Hex]	Calibrated Gain
00	2.000	40	1.936
01	2.001	41	1.937
02	2.002	42	1.938
03	2.003	43	1.939
04	2.004	44	1.940
05	2.005	45	1.941
06	2.006	46	1.942
07	2.007	47	1.943
…	…	…	…
0F	2.015	4F	1.951
10	2.016	50	1.952
…	…	…	…
1F	2.031	5F	1.967
20	2.032	60	1.968
…	…	…	…
2F	2.047	6F	1.983
30	2.048	70	1.984
…	…	…	…
3F	2.063	7F	1.999

9. OFFSET Register (Adrs = 08H)

Bit	7	6	5	4	3	2	1	0
	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
R/W	R	R	R	R	R	R	R	R
Default	—	—	—	—	—	—	—	—

The OFFSET register specifies the voltage offset on the VMON output. Calibrated cell voltage is given by the following equation using an A/D converted value of analog VMON output:

Cell voltage = VGAIN × [VMON output voltage] + OFFSET

, where VGAIN is a calibrated gain, and OFFSET is a deviation from zero voltage.

The following table shows the relationship between the VOFFSET register value and the offset value.

Register value [Hex]	Offset [mV]
00	+0
01	+1
02	+2
03	+3
…	…
7F	+127
80	-128
81	-127
82	-126
83	-125
…	…
FD	-3
FE	-2
FF	-1

10. TEST Register (Adrs = 09H)

Bit	7	6	5	4	3	2	1	0
	OPC	—	—	RCVD	SOVD	ZVD	UVD	OVD
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The TEST register controls detection delay times. Production test time can be reduced significantly in battery pack assembly.

The OVD bit selects overvoltage detection delay time.

OVD	Overvoltage detection delay time
0	4.8 second (default)
1	100 ms (internal timer used)

The UVD bit selects undervoltage detection delay time.

UVD	Undervoltage detection delay time
0	4.8 second (default)
1	100 ms (internal timer used)

The ZVD bit selects 0-V charge inhibit delay time.

ZVD	0-V charge inhibit delay time
0	16 second (default)
1	100 ms (internal timer used)

The SOVD bit selects 2nd overvoltage detection delay time.

SOVD	2nd overvoltage detection delay time
0	16 second (default)
1	100 ms (internal timer used)

The RCVD bit selects recovery delay time from the overvoltage, undervoltage and 0-V charge inhibit states.

RCVD	Recovery delay time
0	0.8 second (default)
1	100 ms (internal timer used)

The OPC bit resets the 2nd overvoltage detection state. Writing data "1" to the OPC bit resets the SOV bit of the ERROR register to "0", with resetting the CELLOP pin output to Hi-Z as well.

OPC	2nd overvoltage state reset
0	None (default)
1	Reset

(Note) After writing data "1" to the OPC bit, it is autonomously restored to the ‘0’ level. You do not have to write ‘0’ again.

● Power-on/Power-off Sequence

Battery cells can be connected in any order, but the recommend sequence is connecting the GND and VDD pins first, followed by Vn pins from the bottom to the top of the battery cell stack. When disconnecting cells the opposite sequence is recommended, in which Vn pins are disconnected from the top to the bottom of the cell stack, and then cut off VDD and GND. If this sequence is not observed, the Vn+1-to-Vn pin voltage may exceed the absolute maximum rating, resulting in destruction of the device. This is also true in performing evaluation or inspection with battery simulators, where the power-on/power-off sequence should be observed so that the Vn+1-to-Vn pin voltage does not exceed the absolute maximum rating.

For surge protection, a 150 Ω or higher external input resistor R_{CELL} is recommended. Battery cells should be stacked before connected to Vn pins. Never try to connect single battery cells one-by-one, because the Vn+1-to-Vn pin voltage may exceed the absolute maximum rating.

There are no restrictions on the power supply voltage rise time at power-on and power-off, and power supply voltage fall time at power-off.

● False Overvoltage Conditions at Power-up

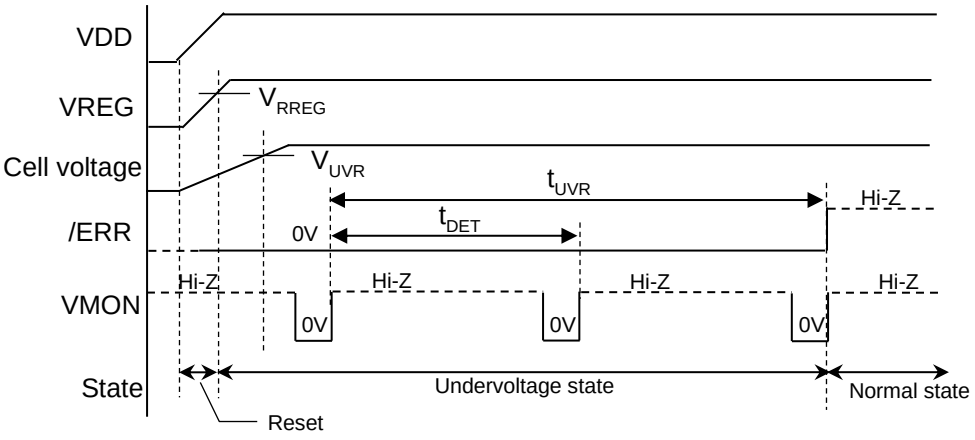
Immediately after the power-on sequence, the ML5204 usually enters the normal state. But due to chattering noise or other reasons at power-up, it may enter the power-down state. The power-down state is cleared by asserting the "L" level on the /PUPIN pin.

During battery pack assembly, overvoltage or 2nd overvoltage condition may be detected if battery pack assembly is not completed soon enough. After completing pack assembly, the overvoltage state is released autonomously, while the 2nd overvoltage state needs to be reset by one of the following methods.
To reset the 2nd overvoltage state, you can either:

(1)Set the OPC bit of the TEST register to "1", and then the CELLOP pin is restored to Hi-Z.
(2)Set the PD bit of the POWER register to "1" to transition to the power-down state, and then assert “L” on the /PUPIN pin to power up. This procedure resets the ML5204 so the CELLOP output is restored to Hi-Z accordingly.
(3)Assert a voltage which is lower than the VREG drop detection threshold V_{UREG} for 100 ms or longer on the VREG pin. It resets the ML5204 and the CELLOP pin output is restored to Hi-Z.

● Cell Voltage Monitor Function

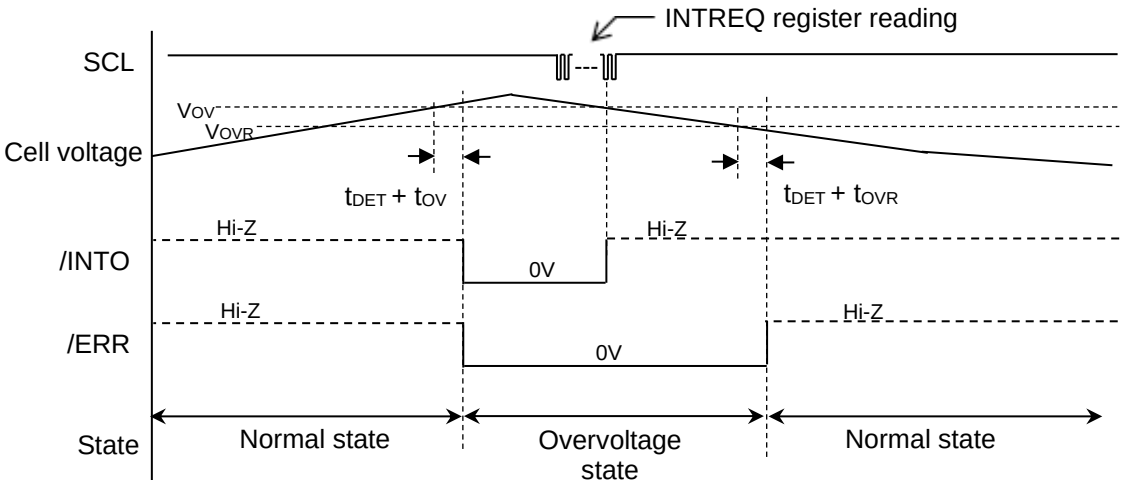
During battery pack assembly if VREG pin voltage reaches the VREG recovery threshold V_{RREG}, cell voltage monitoring is started at an interval t_{DET} of 0.4 sec. Because the initial state of the device is the undervoltage state by default, the UV bit of the ERROR register is "1", and "L" is asserted on the /ERR pin. After battery pack assembly is completed, if all the cell voltages exceed the undervoltage release threshold V_{UVR} for longer than the undervoltage release delay time t_{UVR}, the UV bit is set to "0" and the /ERR pin level becomes Hi-Z, transitioning to the normal state.



After VREG recovery if battery pack assembly is not completed within the corresponding detection delay time, an overvoltage or 2nd overvoltage condition may be detected. In this case, the /INTO pin output becomes "L" asserting an interrupt signal to the microcontroller. Confirm the interrupt requests by reading the INTREQ register and control the device accordingly.

1. Overvoltage Detection and Release

Overvoltage detection and release timing is shown in the following diagram.

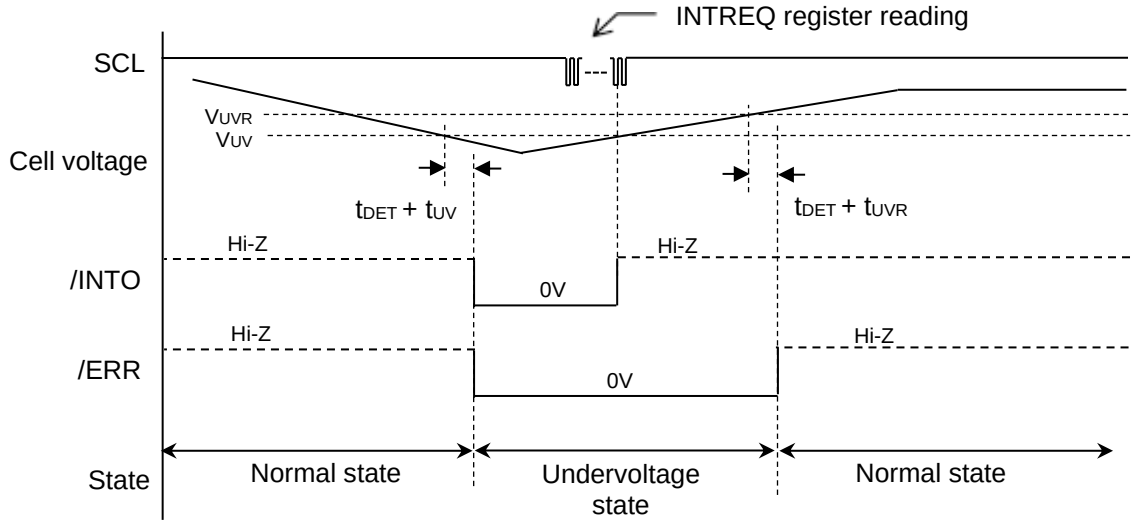


If one or more battery cell voltage exceeds the overvoltage detection threshold V_{OV} for longer than the overvoltage detection delay time t_{OV}, the ML5204 enters the overvoltage state and the "L" level is asserted on the /INTO pin to interrupt the microcontroller. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QOV bit "1" denotes overvoltage condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin level is set to Hi-Z. In parallel, the OV bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin to notify the microcontroller of the error.

If all the battery cell voltages fall below the overvoltage release voltage V_{OVR} for longer than the overvoltage release delay time t_{OVR}, the ML5204 returns to the normal state. The /ERR pin level returns to Hi-Z if no other errors are present. When returning to the normal state, no interrupt signal is asserted on the /INTO pin.

2. Undervoltage Detection and Release

Undervoltage detection and release timing is shown in the following diagram.



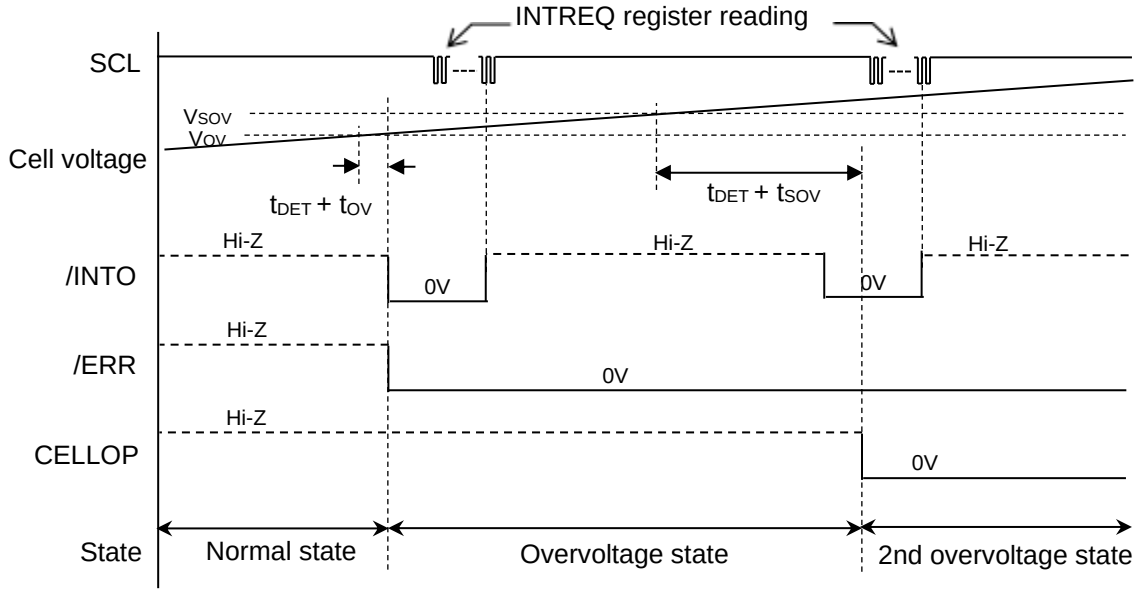
If one or more battery cell voltage falls below the undervoltage detection threshold V_{UV} for longer the undervoltage detection delay time t_{UV}, the ML5204 enters the undervoltage state and the "L" level is asserted on the /INTO pin to interrupt the microcontroller. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QUV bit "1" denotes undervoltage condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin level is set to Hi-Z. In parallel, the UV bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin to notify the microcontroller of the error.

If all the battery cell voltages exceed the undervoltage release threshold V_{UVR} for longer than the undervoltage release delay time t_{UVR}, the ML5204 returns to the normal state. The /ERR pin level returns to Hi-Z, if no other errors are present. When returning to the normal state, no interrupt signal is asserted on the /INTO pin.

The ML5204 does not transition to the power-down state autonomously even if it detects an undervoltage condition. To enter the power-down state, set the PD bit of the POWER register to "1". Refer to the POWER register section for details.

3. 2nd Overvoltage Detection

2nd overvoltage detection timing is shown in the following diagram.



If one or more battery cell voltage exceeds the 2nd overvoltage detection threshold V_{SOV} for longer than the 2nd overvoltage detection delay time t_{SOV}, the ML5204 enters the 2nd overvoltage state and the "L" level is asserted on the CELLOP pin to notify the microcontroller of the 2nd overvoltage state. In parallel, the SOV bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin. Also, the "L" level is asserted on the /INTO pin as well. By reading the INTREQ register, the microcontroller can confirm the interrupt requests, where the QSOV bit s "1" denotes 2nd overvoltage condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin level is set to Hi-Z.

If 2nd overvoltage is detected, a permanent failure is suspected where charge current cannot be turned off due to C-FET breakdown, for example. Fuse the current path immediately to permanently disable the battery pack.

Even if all the battery cell voltages come back to the normal range, the 2nd overvoltage state is held. To reset the 2nd overvoltage state, you can either:

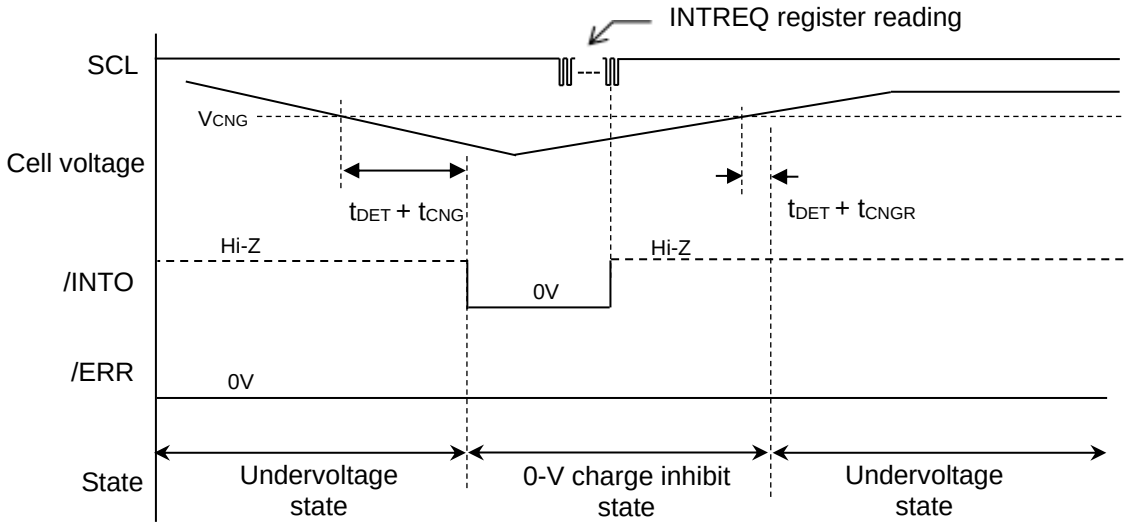
(1)Set the OPC bit of the TEST register to "1", and the CELLOP output is restored to Hi-Z.

(2)Set the PD bit of the POWER register to "1" to transition to the power-down state, and then assert “L” on the /PUPIN pin to power up. This procedure resets the ML5204 so the CELLOP output is restored to Hi-Z accordingly.

(3)Assert a voltage which is lower than the VREG drop detection threshold V_{UREG} for 100 ms or longer on the VREG pin. It resets the ML5204 and the CELLOP pin output is restored to Hi-Z.

4. 0-V Charge Inhibit and Enable

0-V charge inhibit and enable timing is shown in the following diagram.

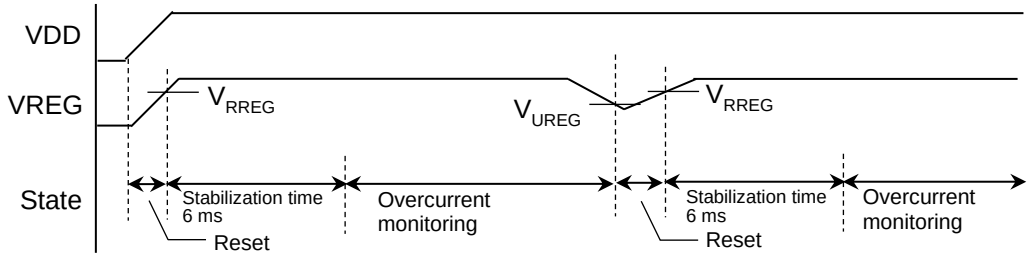


If one or more battery cell voltage falls below the 0-V charge inhibit threshold V_{CNG} for longer than the 0-V charge inhibit delay time t_{CNG}, the ML5204 enters the 0-V charge inhibit state and the "L" level is asserted on the /INTO pin to interrupt the microcontroller. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QZV bit "1" denotes 0-V charge inhibit condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin is set to Hi-Z. In parallel, the ZV bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin to notify the microcontroller of the error.

If all the battery cell voltages exceed the 0-V charge inhibit threshold V_{CNG} for longer than the 0-V charge enable delay time t_{CNGR}, the 0-V charge inhibit state is released, and the ZV bit of the ERROR register is reset to "0". Immediately after 0-V charge enable, the cell voltage is usually below the undervoltage threshold, thus undervoltage condition is remaining and the /ERR level is still "L". If 0-V charge inhibit condition is cleared, no interrupt signals are asserted on the /INTO pin.

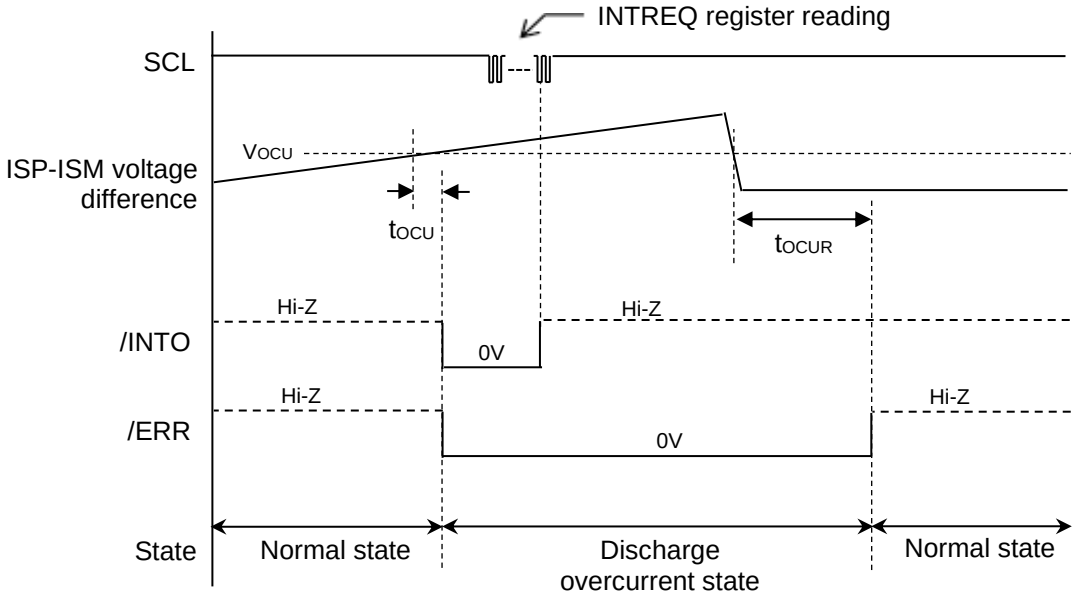
● Current Monitor Function

If the VREG pin voltage exceeds the VREG recovery threshold V_{RREG}, overcurrent monitor is initiated after a 6 ms stabilization time, where voltage difference between the ISP and ISM pins is analyzed for overcurrent detection. Overcurrent monitor is always running except in the power-down state, the VREG drop state and the stabilization time after the VREG recovery, regardless of the analog current monitor configurations on the IMON register.



1. Discharge Overcurrent Detection and Release

Discharge overcurrent detection and release timing is shown in the following diagram.

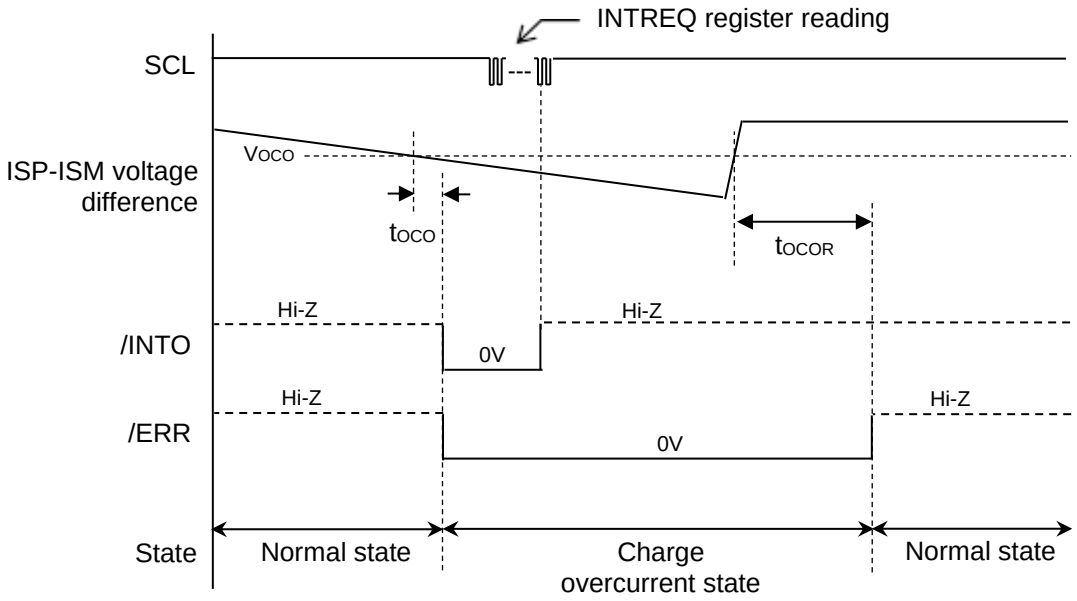


When a load is connected to the battery pack, if the ISP-to-ISM voltage exceeds the discharge overcurrent detection threshold V_{OCU} for longer than the discharge overcurrent detection delay time t_{OCU}, the ML5204 enters into the discharge overcurrent state and asserts the "L" level on the /INTO pin to interrupt the microcontroller, regardless of cell voltage monitoring. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QOCU bit "1" denotes discharge overcurrent condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin level is set to Hi-Z. In parallel, the OCU bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin to notify the microcontroller of the error.

If the ISP-to-ISM pin voltage falls below the discharge overcurrent detection threshold V_{OCU} for longer than the discharge overcurrent release delay time t_{OCUR}, the discharge overcurrent state is released, and the OCU bit of the ERROR register is reset to "0". The /ERR pin returns to the Hi-Z state if no other errors are present. When returning to the normal state, no interrupt signals are asserted on the /INTO pin.

2. Charge Overcurrent Detection and Release

Charge overcurrent detection and release timing is shown in the following diagram.

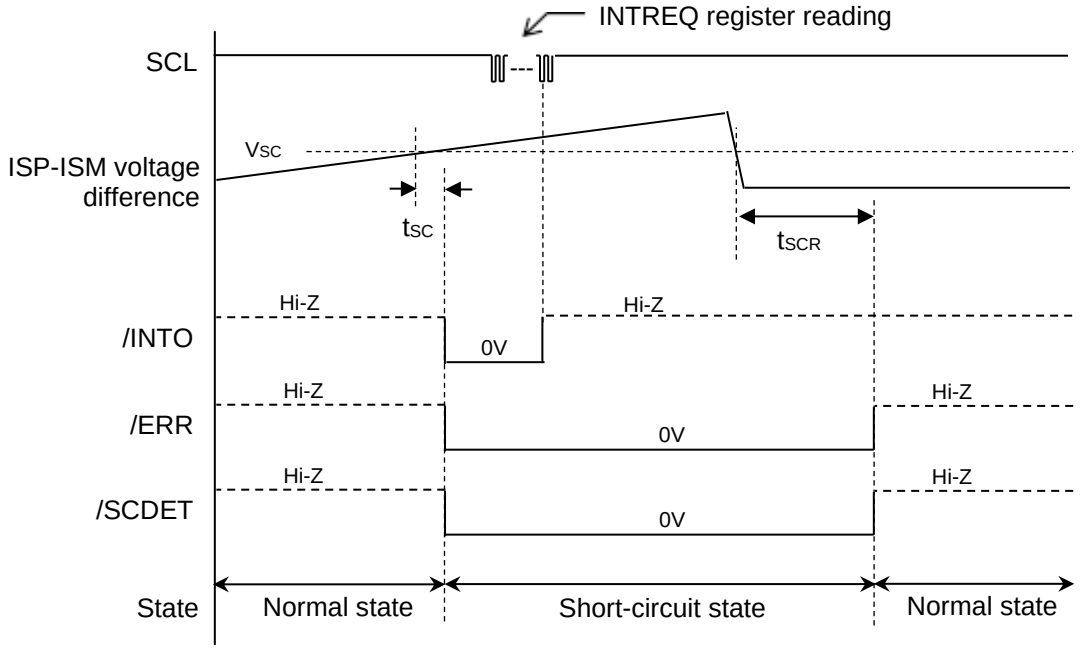


When a charger is connected to the battery pack, if the ISP-to-ISM pin voltage exceeds the charge overcurrent detection threshold V_{OCO} for longer than the charge overcurrent detection delay time t_{OCO}, the ML5204 enters into the charge overcurrent state, and asserts the "L" level on the /INTO pin to interrupt the microcontroller, regardless of cell voltage monitoring. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QOCO bit "1" denotes charge overcurrent condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin level is set to Hi-Z. In parallel, the OCO bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin to notify the microcontroller of the error.

If the ISP-to-ISM pin voltage falls below the charge overcurrent detection threshold V_{OCO} for longer than the charge overcurrent release delay time t_{OCOR}, the charge overcurrent state is released, and the OCO bit of the ERROR register is reset to "0". The /ERR pin returns to the Hi-Z state if no other errors are present. When returning to the normal state, no interrupt signals are asserted on the /INTO pin.

3. Short-Circuit Detection and Release

Short-circuit detection and release timing is shown in the following diagram.

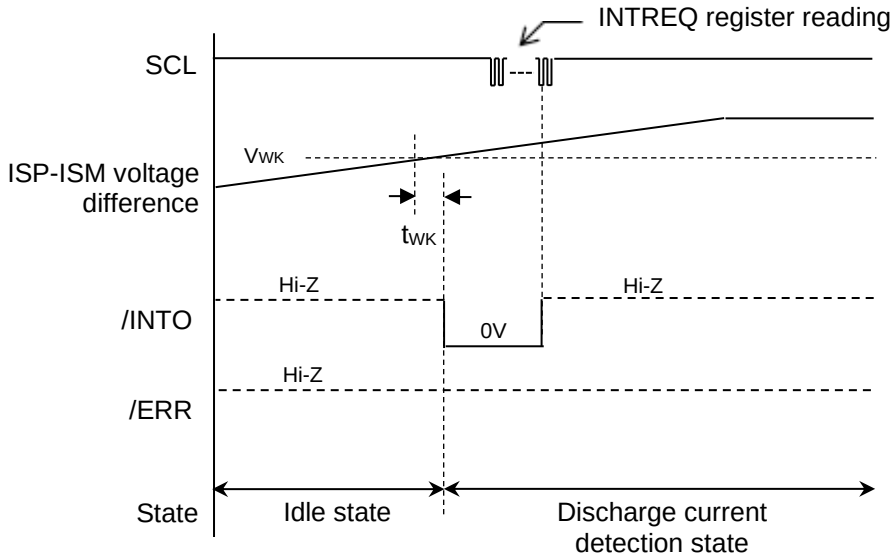


When a heavy load is connected to the battery pack, if the ISP-to-ISM pin voltage exceeds the short-circuit detection threshold V_{SC} for longer than the short-circuit detection delay time t_{SC}, the ML5204 enters the short-circuit state and asserts the "L" level on the /SCDET pin to interrupt the microcontroller, regardless of cell voltage monitoring. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QSC bit "1" denotes short-circuit condition. The INTREQ register is autonomously cleared after readout, and the /INTO pin level is set to Hi-Z. In parallel, the SC bit of the ERROR register is set to "1", and the "L" level is asserted on the /ERR pin. Also, the "L" level is asserted on the /INTO pin.

If the ISP-to-ISM pin voltage falls below the short-circuit detection threshold V_{SC} for longer than the short-circuit release delay time t_{SCR}, the short-circuit state is released, and the SC bit of the ERROR register is reset to "0". The /ERR pin returns to the Hi-Z state if no other errors are present. When returning to the normal state, no interrupt signals are asserted on the /INTO pin.

● Wake-up Detection

If the VREG pin voltage reaches the VREG recovery threshold V_{RREG}, wake-up detection is available after a 6ms stabilization time, where voltage difference between the ISP and ISM pins is analyzed for wake-up detection. Wake-up detection is controlled by the WKUP bit of the POWER register. Refer to the POWER register section for details.

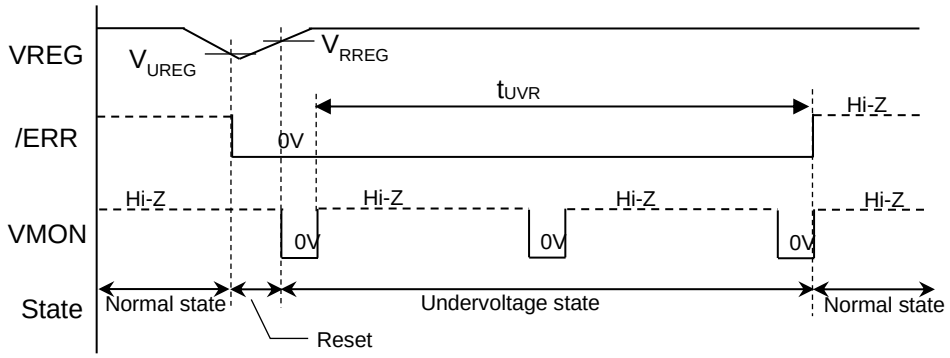


When wake-up detection is enabled, if a load is connected and the ISP-to-ISM pin voltage exceeds the wake-up detection threshold for longer than the wake-up detection delay time t_{WK}, the "L" level is asserted on the /INTO pin to interrupt the microcontroller. By reading the INTREQ register, the microcontroller can confirm the interrupt request, where the QWKUP bit "1" denotes wake-up condition and presence of discharge current. The INTREQ register is autonomously cleared by readout, and the /INTO pin level is restored to Hi-Z. Wake-up detection does not change the /ERR pin or the ERROR register state.

● VREG Drop Detection

If the VREG pin voltage falls below VREG drop threshold V_{UREG}, ML5204 internal state is initialized, in which the UV bit of the ERROR register is set to “1”, and the "L" level is asserted on the /ERR pin. At this time, the /INTO pin output level is Hi-Z and no interrupt signals are asserted.

If the VREG voltage exceeds the VREG recovery threshold V_{RREG}, individual cell voltage monitoring is started. If all the battery cell voltages exceed the undervoltage release threshold V_{UVR} for longer than the undervoltage release delay time t_{UVR}, the UV bit is reset to "0", making the /ERR pin level Hi-Z.



● Handling VDD Pin and V0 to V5 Pins

Since the VDD pin is power supply input, a noise elimination RC filter is recommended for stability.
The V0 to V5 pins are cell voltage sense inputs. Connect each battery cell via a noise elimination RC filter to prevent false alarms. For surge protection, 150 Ω or larger value is recommended for the external resistance R_{CELL}.

● Handling VREG Pin

The VREG pin outputs internally regulated power, which is also used for internal circuits. Connect a 1 µF or larger capacitor between this pin and GND for stability. Do not source power to external circuits since supply capacity of the internal regulator is limited.

● Unused Pins Treatment

The following table shows how to handle unused pins.

Unused pins	Recommended treatment
V0	Connected to GND
ISM, ISP	Connected to GND
VMON	Open
IMON	Open
SCL, SDA	Connected to VREG
/SCDET	Open
CELLOP	Open
/INTO	Open
/ERR	Open
/PUPIN	Connected to GND through a 0.1 µF or larger capacitor
VREG	Connected to GND through a 1 µF or larger capacitor

● Supported Cell Counts

Supported serial cell count is 4 or 5.
In a 4-cell system, the V0 input pin should not be used and should be tied to GND.

● Redefinition of Detection Thresholds

Detection thresholds are selectable and can be redefined in the range and step shown in the following table. Some combinations may not be available due to conflicts.

Detection threshold	Settable range	Step voltage
Overvoltage detection threshold	3.65 V to 4.35 V	25 mV
Overvoltage release threshold	3.5 V to 4.25 V	25 mV
2nd overvoltage detection threshold	3.65 V to 4.35 V	25 mV
Undervoltage detection threshold	1.6 V to 3 V	100 mV
Undervoltage release threshold	2.3 V to 3.6 V	100 mV
0-V charge inhibit threshold	0.1 V to 1.2 V	50 mV
Discharge overcurrent threshold	50 mV to 200 mV	10 mV
Charge overcurrent threshold	-60 mV to -20 mV	10 mV
Short-circuit detection threshold (Note 1)	100 mV to 500 mV	10 mV
Wake-up detection threshold	5 mV to 10 mV	2.5 mV

(Note 1) Detection accuracy is aggravated twice for a threshold value exceeding 200 mV.

● Redefinition of Detection Delays

Detection delay times are selectable and can be redefined in the range shown below.

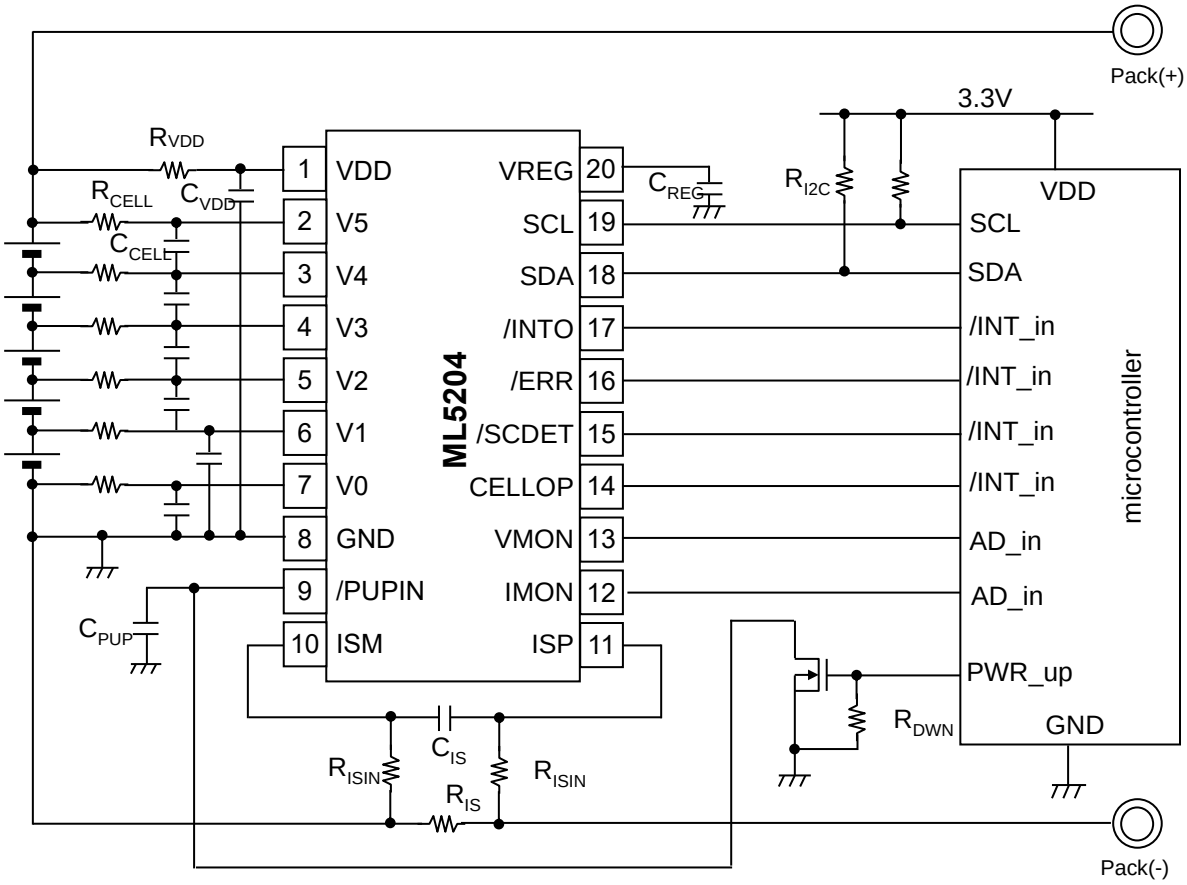
Detection delay time	Configurable time							Unit
Overvoltage detection delay time	1.6	3.2	4.8	6.4	8	9.6	11.2	sec
Overvoltage release delay time	0.4	0.8	1.6	–	–	–	–	sec
2nd overvoltage detection delay time	6.4	11.2	12.8	14.4	16	17.6	19.2	sec
Undervoltage detection delay time	1.6	3.2	4.8	6.4	8	9.6	11.2	sec
Undervoltage release delay time	0.4	0.8	1.6	–	–	–	–	sec
0-V charge inhibit delay time	1.6	3.2	4.8	6.4	8	9.6	11.2	sec
0-V charge enable delay time	0.4	0.8	1.6	–	–	–	–	sec
Discharge overcurrent detection delay time	12.5	25	50	100	200	–	–	ms
Discharge overcurrent release delay time	25	50	100	200	–	–	–	ms
Charge overcurrent detection delay time	12.5	25	50	100	200			ms
Charge overcurrent release delay time	25	50	100	200	–	–	–	ms
Short-circuit detection delay time	100	200	400	800	–	–	–	μs
Short-circuit release delay time	25	50	100	200	–	–	–	ms
Wake-up detection delay time	2	4	8	16	–	–	–	ms

● Redefinition of Current Amplifier Gain/IMON Level at Zero Current

Current amplifier gain and IMON Level at zero current are selectable and can be redefined in the range shown below. Some combinations may not be available due to conflicts.

Item	Configurable value					Unit
Gain (GIM = 0)	8	10	12	14	16	Factor
Gain (GIM = 1)	16	20	24	28	32	Factor
IMON level at zero current	0.4	0.5	0.6	0.7	0.8	V

■ Application Circuit Example



■ Recommended Values for External Components

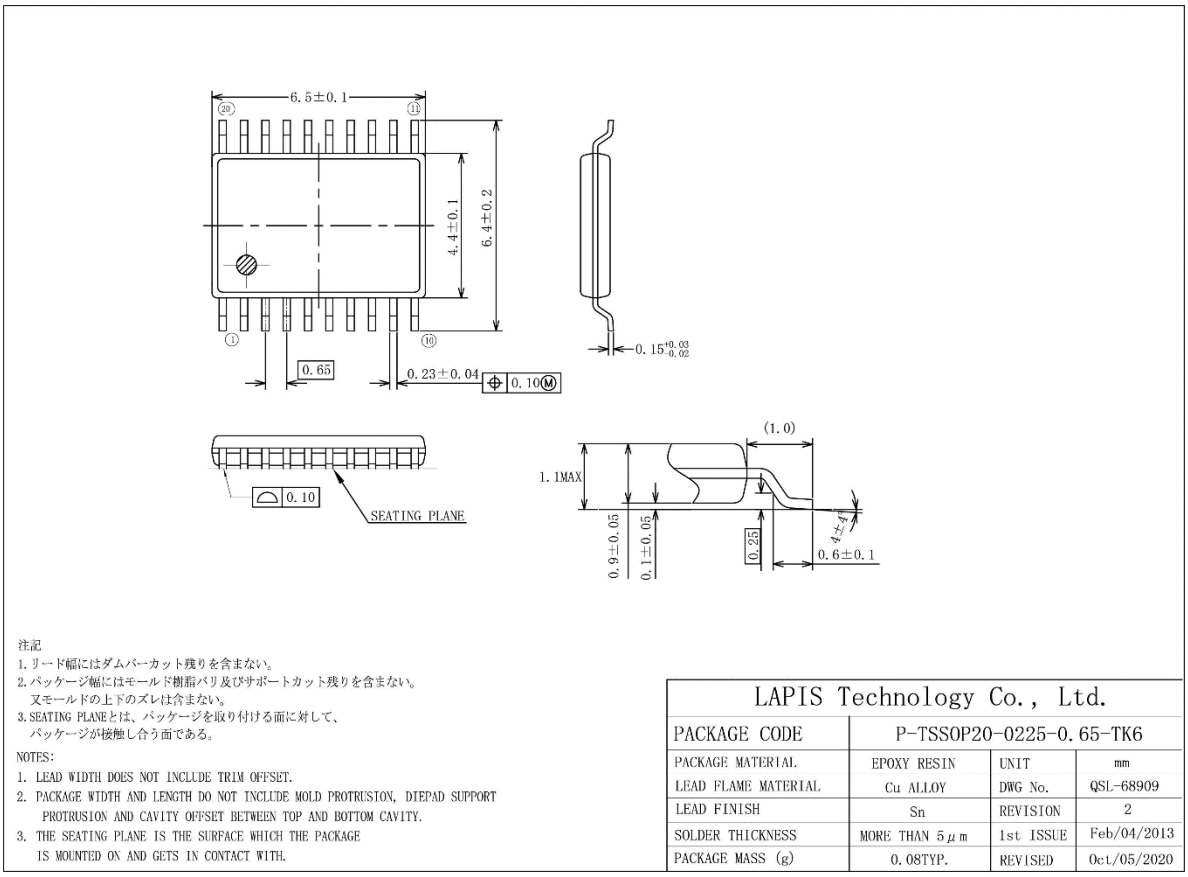
Component	Recommended value
R_{VDD}	510 Ω
C_{VDD}	2.2 µF or larger
R_{CEL}	150 Ω to 10 kΩ
C_{CEL}	0.1 µF or larger
C_{REG}	1 µF
C_{PUP}	0.1 µF

Component	Recommended value
R_{IS}	0.5 mΩ
R_{ISIN}	1 kΩ
C_{IS}	10 nF
R_{I2C}	5.1 kΩ to 47 kΩ
R_{DWN}	100 kΩ

(Note 1) When cell balancing is performed, false overvoltage and/or undervoltage conditions may be detected if the time constant of RC input filter is too large. It is thus recommended that R_{CELL} and C_{CELL} are carefully selected so that the time constant is 1.5 ms or shorter.

(Note 2) Example of application circuit and the recommended values to parts list shall not guarantee performance under all conditions. Full and detailed tests are suggested on your actual application.

■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	2
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	Oct/05/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to applied heat in solder reflow or moisture absorption during storage. Please contact your local ROHM sales representative for the recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

■ Revision History

Document No.	Issue date	Page		Revision description
		Before revision	After revision	
FEDL5204-01	30 Oct, 2017	-	-	Initial release
FEDL5204-02	1 Dec, 2020	-	-	Changed Company name
		36	36	Changed “Notes”
FEDL5204-03	Jan. 9, 2024	1	1	Add Application Part number, Delete notes
		36	36	Add Notes

Notes

1) When using LAPIS Technology Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings*1, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore, LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) LAPIS Technology intends our Products to be used in a way indicated in this document. Please be sure to contact a ROHM sales office if you consider the use of our Products in different way from original use indicated in this document. For use of our Products in medical systems, please be sure to contact a LAPIS Technology representative and must obtain written agreement. Do not use our Products in applications which may directly cause injuries to human life, and which require extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us without our prior written consent.

6) All information contained in this document is subject to change for the purpose of improvement, etc. without any prior notice. Before purchasing or using LAPIS Technology Products, please confirm the latest information with a ROHM sales office. LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document, however, LAPIS Technology shall have no responsibility for any damages, expenses or losses arising from inaccuracy or errors of such information.

7) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

8) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

9) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

10) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) “LAPIS Technology” as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.
2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

LTSZ08023・01・002