Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5236

Analog Front-End IC for 14-Serial-Cell Lithium-Ion Rechargeable Battery Protection

■ General Description

The ML5236 is an analog front-end IC intended for 14-cell Li-ion rechargeable battery protection systems. With integrated individual cell voltage monitor and charge/discharge current monitor functions, it protects cell overvoltage, cell undervoltage, and pack over-current working with an external microcontroller (MCU). Also, it is equipped with the short-circuit protection function, which autonomously turns off the external charge/discharge Nch-FETs on the high-side power rail without the external MCU.

■ Features

- 5- to 14-cell high-precision cell voltage measurement function
  Built-in 12-bit successive approximation type ADC
  Cell voltage measurement precision: ±10mV (typ) at cell voltage 4V
  Cell voltage measurement time: 2ms per cell (typ)
- Charge/discharge current measurement function
  The potential differential between the ISP and ISM pins amplified by 12- or 60-fold, then digitized with the 12-bit ADC.
  (A single ADC module is shared in cell voltage measurement and pack current measurement.)
- Short-circuit protection function
  Variable detection threshold between ISP and ISM pins: 50mV/100mV/150mV/200mV (typ)
  Detection delay time adjustable using an external capacitor
- Built-in cell balancing switch on each cell: Switch ON resistance 6Ω (typ)
- External charge/discharge FET control: Built-in gate driver for highside Nch-FET
- Temperature sensor measurement function: Two thermistor inputs
- Overvoltage protection function: Overvoltage protection tripped by comparing each A/D converted cell voltage value with the detection threshold defined in the control register
- MCU interface: SPI serial interface (mode 0)
  Dedicated power supply pin VSPI allows 5V interface
- Built-in 3.3V regulator for an external MCU: 10mA (max) output current
  Current boost circuitry configurable with an external Pch-FET
- Low current consumption
  Normal operation : 330µA(typ), 700µA (max)
  Power-save : 120µA(typ), 200µA (max)
  Power-down : 0.1µA(typ), 1µA(max)
- Power supply voltage : +8V to +64V
- Operating temperature range : -40°C to +85°C
- Package : 44-Pin TQFP

■ Application

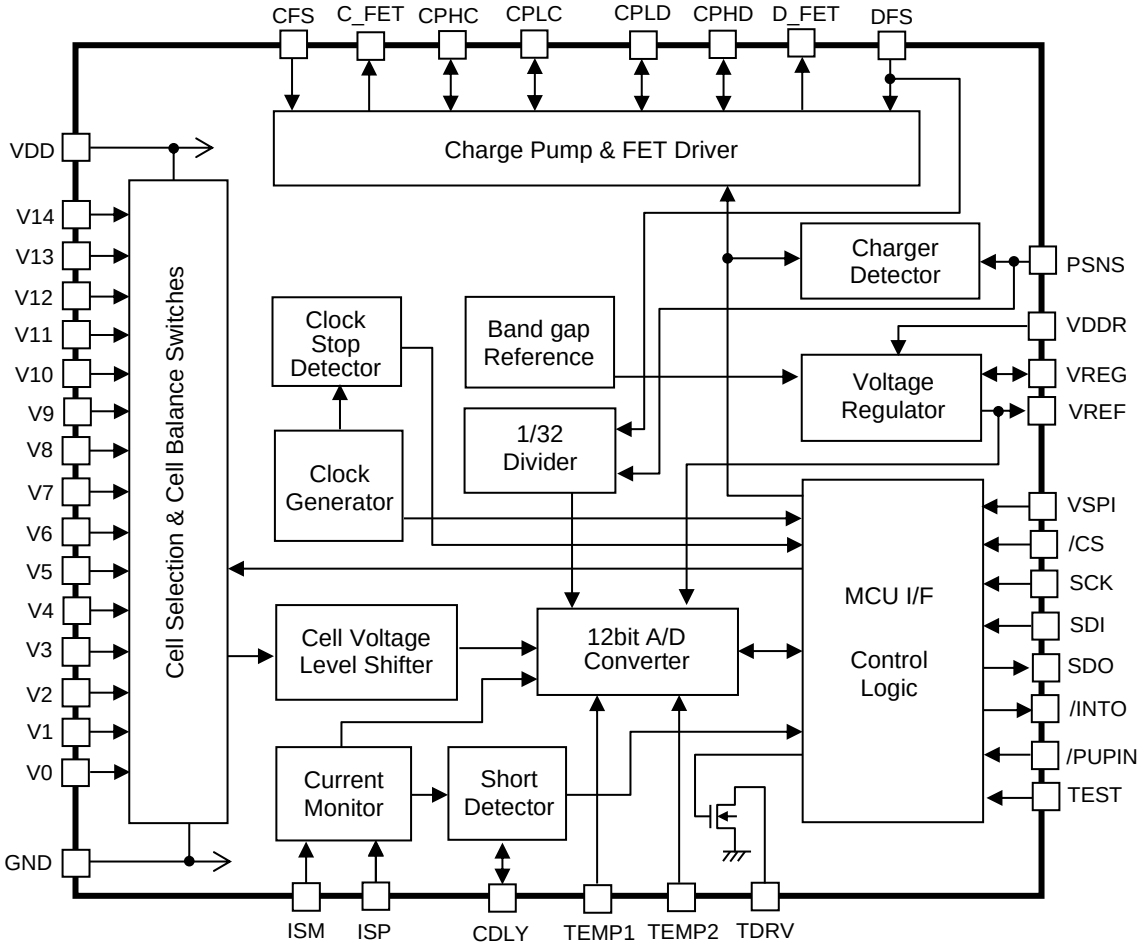
・Power tools and Garden tools
・E-Bike and Electric assisted bicycle
・Uninterruptible Power Supplies (UPS)
・Energy Storage Systems (ESS)

■ Part number

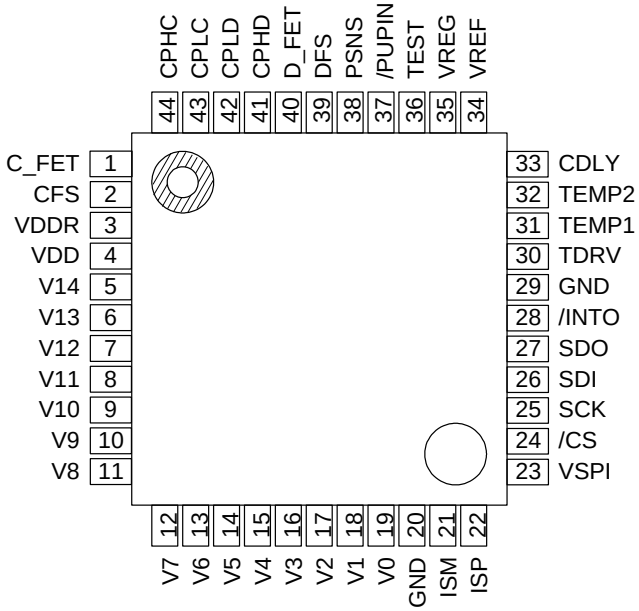
ML5236TB

ROHM SEMICONDUCTOR

■ Block Diagram



■ Pin Configuration (Top View)



■ Pin Description

Pin No.	Pin name	I/O	Description
1	C_FET	O	Charge FET gate drive. Connected to the gate pin of the external Nch-FET. In the ON state, the CFS level +12V (typ) is asserted, while the CFS level is asserted in the OFF state.
2	CFS	I	Reference voltage input for the C_FET drive charge pump. Connected to the source pin of the charge FET.
3	VDDR	—	Power supply for the internal regulator. Configure an external CR noise filter circuit.
4	VDD	—	Power supply. Configure an external CR noise filter circuit.
5	V14	I	Cell 14 positive input.
6	V13	I	Cell 14 negative input and Cell 13 positive input.
7	V12	I	Cell 13 negative input and Cell 12 positive input.
8	V11	I	Cell 12 negative input and Cell 11 positive input.
9	V10	I	Cell 11 negative input and Cell 10 positive input.
10	V9	I	Cell 10 negative input and Cell 9 positive input.
11	V8	I	Cell 9 negative input and Cell 8 positive input. For the 5-cell applications, connected to GND.
12	V7	I	Cell 8 negative input and Cell 7 positive input. For the 5- to 6-cell application, connected to GND.
13	V6	I	Cell 7 negative input and Cell 6 positive input. For the 5- to 7-cell applications, connected to GND.
14	V5	I	Cell 6 negative input and Cell 5 positive input. For the 5- to 8-cell applications, connected to GND.
15	V4	I	Cell 5 negative input and Cell 4 positive input. For the 5- to 9-cell applications, connected to GND.
16	V3	I	Cell 4 negative input and Cell 3 positive input. For the 5- to 10-cell applications, connected to GND.
17	V2	I	Cell 3 negative input and Cell 2 positive input. For the 5- to 11-cell applications, connected to GND.
18	V1	I	Cell 2 negative input and Cell 1 positive input. For the 5- to 12-cell applications, connected to GND.
19	V0	I	Cell 1 negative input. For the 5- to 13-cell applications, connected to GND.
20	GND	—	Ground pin.
21	ISM	I	Current sense negative input. Connected to the negative terminal of the most negative battery cell.
22	ISP	I	Current sense positive input. The ISP pin level should be higher than the ISM pin level in discharge state.
23	VSPI	—	Serial MCU interface power supply. Tied to the external MCU power supply.
24	/CS	I	Serial MCU interface chip select input. Serial MCU interface is enabled with L-level input.

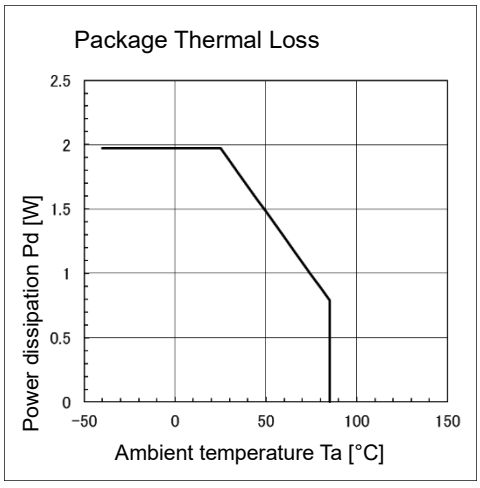
Pin No.	Pin name	I/O	Description
25	SCK	I	Serial MCU interface clock input. SDI input is captured at the rising edge of the SCK clock, while SDO output should be read at the falling edge of the SCK.
26	SDI	I	Serial MCU interface data input.
27	SDO	O	Serial MCU interface data output. If /CS input is “H” level, SDO is fixed to Hi-Z state.
28	/INTO	O	Interrupt signal output to an external MCU, NMOS open drain. Should be pulled up externally so that “L” level is asserted when an interrupt occurs.
29	GND	—	Ground.
30	TDRV	O	Ground for thermistors. 0V is asserted during temperature measurement, or fixed to the Hi-Z state otherwise.
31	TEMP1	I	Thermistor inputs. Connected to TDRV through an NTC thermistor, and also pulled up to VREF via a resistor.
32	TEMP2	I	
33	CDLY	IO	Short circuit detection delay time configuration pin. Connected to GND through a capacitor.
34	VREF	O	2.5V reference level output for the internal ADC. Connected to GND through a 4.7μF capacitor.
35	VREG	O	Built-in 3.3V regulator output. Connected to GND through a 4.7μF capacitor. Can power the external MCU.
36	TEST	I	Device test enable input. Should be fixed to GND.
37	/PUPIN	I	Power-up trigger input. The device wakes up with the ”L” level input. Internally pulled up to VDD through a 1MΩ resistor.
38	PSNS	I	Charger presence detection input at power-down. The device is powered-up when the PSNS level becomes 1/2VDD or higher during power-down. The ADC can measure 1/32-fold voltage of the PSNS level.
39	DFS	I	Reference voltage input for the D_FET drive charge pump. Connected to the source pin of the discharge FET. The ADC can measure 1/32-fold voltage of the DFS level.
40	D_FET	O	Discharge FET gate drive. Connected to the gate pin of the external Nch-FET. In the ON state, the DFS level +12V (typ) is asserted, while the DFS level is asserted in the OFF state.
41	CPHD	O	Charge pump capacitor input for D_FET drive. Connect a capacitor with approximately twice the gate capacitance of the discharge FET between the CPHD and CPLD pins.
42	CPLD	O	
43	CPLC	O	Charge pump capacitor input for C_FET drive. Connect a capacitor with approximately twice the gate capacitance of the charge FET between the CPHC and CPLC pins.
44	CPHC	O	

■ Absolute Maximum Ratings

GND=0V, Ta=25°C

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Applied to VDD and VDDR pins	-0.3 to +86.5	V
Input voltage	V_{IN1}	Applied to V14 to V0 pins Voltage difference between Vn+1 and Vn pins (note)	-0.3 to +6.5	V
	V_{IN2}	Applied to CFS, DFS, and PSNS pins	-0.3 to +86.5	V
	V_{IN3}	Applied to /PUPIN pin	-0.3 to V_{DD}+0.3	V
	V_{IN4}	Applied to TEMP1, TEMP2, ISM, and ISP pins	-0.3 to V_{REG}+0.3	V
	V_{IN5}	Applied to /CS, SCK, and SDI pins	-0.3 to V_{SPI}+0.3	V
Output voltage	V_{OUT1}	Applied to D_FET pin V_{DFS}=DFS pin voltage	V_{DFS}-0.3 to +86.5	V
	V_{OUT2}	Applied to C_FET pin V_{CFS}=CFS pin voltage	V_{CFS}-0.3 to +86.5	V
	V_{OUT3}	Applied to /INTO ,TDRV and CDLY pins	-0.3 to +6.5	V
	V_{OUT4}	Applied to SDO pin	-0.3 to V_{SPI}+0.3	V
Short circuit output current	I_{OS}	VDD=50V, Applied to VREG, VREF, SDO, /INTO, TDRV, CDLY, C_FET, and D_FET pins	20	mA
Cell balancing current	I_{CB}	Per cell balancing switch	100	mA
Power dissipation	P_D	Ta=25°C	1.9	W
Junction temperature	Tj_{MAX}	—	125	°C
Package thermal resistance	θja	JEDEC double-side board mounted	50.7	°C/W
Storage temperature	T_{STG}	—	-55 to +150	°C

Note : When connecting and disconnecting battery cells, voltage exceeding the absolute maximum rating may be applied between the adjacent Vn+1 and Vn inputs, resulting in permanent damage on the LSI. Make a full and detailed evaluation before usage.



Package thermal loss tolerance decreases with increased ambient temperature Ta as in the left diagram. Make sure that the thermal loss tolerance is not exceeded especially when the output current on the VREG pin is high.

■ Recommended Operating Conditions

(GND= 0 V)

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	Applied to VDD and VDDR pins	8 to 64	V
	V_{SPI}	Applied to VSPI pin	2.7 to 5.5	V
Operating temperature	Ta	No VREG output load	-40 to +85	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (*1)	V_{IH}	—	0.8×V_{SPI}	—	V_{SPI}	V
Digital "L" input voltage (*1)	V_{IL}	—	0	—	0.2×V_{SPI}	V
/PUPIN pin "H" input voltage	V_{IHP}	—	0.8×V_{DD}	—	V_{DD}	V
/PUPIN pin "L" input voltage	V_{ILP}	—	0	—	0.2×V_{DD}	V
Digital "H" input current (*1)	I_{IH}	V_{IH} = V_{SPI}	—	—	2	µA
Digital "L" input current (*1)	I_{IL}	V_{IL} = GND	–2	—	—	µA
/PUPIN pin "H" input current	I_{IHP}	V_{IH} = V_{DD}	—	—	2	µA
/PUPIN pin "L" input current	I_{ILP}	V_{DD}=64V, V_{IL} = GND	–128	-64	-32	µA
Digital "H" output voltage (*2)	V_{OH}	I_{OH}=-100µA	V_{SPI}-0.2	—	V_{SPI}	V
Digital "L" output voltage (*3)	V_{OL}	I_{OL}=1mA	0	—	0.2	V
Digital output leakage current (*3)	I_{OLK}	V_{OH}= V_{SPI} V_{OL}=0V	–2	—	2	µA
Cell voltage monitor pin Input current (*4)	I_{INVC}	Cell voltage being measured	-5	—	15	µA
Cell voltage monitor pin Input leakage current (*4)	I_{ILVC}	Cell voltage not being measured	-5	—	5	µA
FET "H" output voltage (*5)	V_{OHF}	I_{OH}=-1µA V_{DD}=V_S=18V to 64V V_S: CFS and DFS pin voltage	V_S+8	V_S+12	V_S+16	V
FET "L" output voltage (*5)	V_{OLF}	I_{OL} = 1µA V_{DD}=V_S=18V to 64V V_S: CFS and DFS pin voltage	V_S	—	V_S+0.3	V
VREG output voltage	V_{REG1}	V_{DD}=10V to 64V Output load current < 10mA	3.0	3.3	3.6	V
	V_{REG2}	V_{DD}=8V to 10V Output load current < 5mA	3.0	3.3	3.6	V
VREF output voltage	V_{REF1}	Ta=0 to 60°C Output load current < 1mA	2.48	2.50	2.54	V
	V_{REF2}	Ta=-40 to 85°C Output load current < 1mA	2.45	2.50	2.55	V
Cell balancing switch ON resistance	R_{BL}	Internal balancing FET V_{DS}=0.6V, V_{DD}=18V to 64V	3	6	30	Ω

(*1) Applied to /CS, SCK, and SDI pins.
(*2) Applied to SDO pin.
(*3) Applied to SDO, /INTO, and TDRV pins.
(*4) Applied to V14 to V0 pins.
(*5) Applied to C_FET and D_FET pins.

- Supply Current Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG and VREF output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage measurement state current consumption	I_{DD1}	No output load	—	330	700	μA
Power-save state current consumption	I_{DD2}	No output load	—	120	200	μA
Power-down state current consumption	I_{DDS}	No output load	—	0.1	1.0	μA
VSPI pin static current consumption	I_{VSPI}	No output load Without SPI communication	—	—	10	μA

(Note) The above current consumption values are defined by the total current on the VDD and VDDR pins.

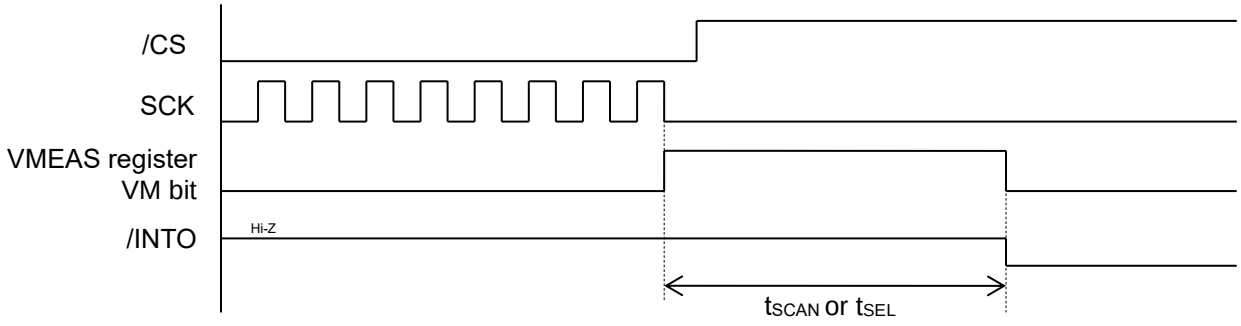
- Cell Voltage Measurement Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage measurement range	V_{VMR}	(*1)	0.1	—	4.5	V
Cell voltage measurement error (*2)	V_{ER1T}	Cell voltage = 3.8 to 4.3V Ta = 25°C	-15	—	15	mV
	V_{ER2T}	When cell voltage = 1V Ta = 25°C	-50	—	50	mV
	V_{ER1}	Cell voltage = 3.8 to 4.3V Ta = 0°C to 60°C	-20	—	20	mV
	V_{ER2}	When cell voltage = 1V Ta = 0°C to 60°C	-70	—	70	mV
Cell voltage measurement step	V_{LSB}	—	—	5000/4095	—	mV
Cell voltage measurement time	t_{SCAN}	14-cell scan	22	28	36	ms
	t_{SEL}	Individual cell select	1.6	2	2.6	ms

(*1) The power supply voltage VDD should be greater than 8V.
(*2) The measurement error within 1.0-to-3.8V cell voltage range is obtained by linear extrapolation.

Cell voltage measurement timing diagram



- Current Measurement Characteristics

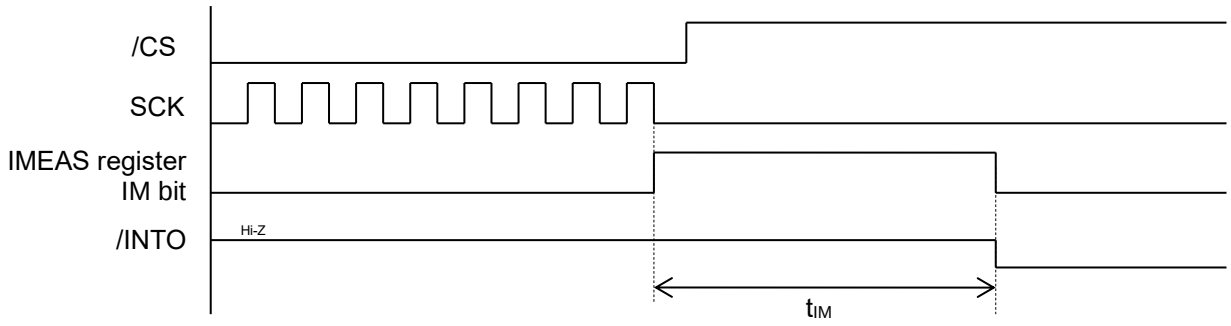
V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, shunt resistor=1mΩ, no VREG output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current measurement range	I_{MR1}	GIM bit = ”0”	-150	—	30	A
	I_{MR2}	GIM bit = ”1”	-25	—	5	A
Current measurement amplifier gain (*1)	G_{IM0}	GIM bit = ”0” Ta = 0°C to 60°C	11.4	12	12.6	Factor
	G_{IM1}	GIM bit = ”1” Ta = 0°C to 60°C	57	60	63	Factor
Current measurement A/D conversion value at zero current	V_{ZIM1}	GIM bit = ”0” Ta = 0°C to 60°C	2B84	3333	3AE1	Hex
	V_{ZIM2}	GIM bit = ”1” Ta = 0°C to 60°C	28F5	3333	3D70	Hex
Current measurement error (*2)	I_{ER1}	GIM bit = ”0” Ta = 0°C to 60°C -50A measurement	-2.5	—	2.5	A
	I_{ER2}	GIM bit = ”1” Ta = 0°C to 60°C -10A measurement	-0.5	—	0.5	A
Current measurement step	I_{LSB1}	GIM bit = ”0”	—	3.1790	—	mA
	I_{LSB2}	GIM bit = ”1”	—	0.6358	—	mA
Current measurement setup stabilization time	t_{STB}	When changing GIM and ZERO bits	—	—	2	ms
Current measurement time (*3)	t_{IM}	—	0.8	1.0	1.3	ms

(*1) The both ends of the shunt resistor should be tied to the ISP and ISM pins via a 1kΩ resistor respectively .

(*2) Assuming a 1mΩ shunt resistor without resistance error, the A/D conversion value at zero current flow is compensated. The given values include errors in the amplification gain factor of 12- or 60-fold. (*3) Stabilization time for current measurement amplifier gain switching is not included.

Current measurement timing diagram

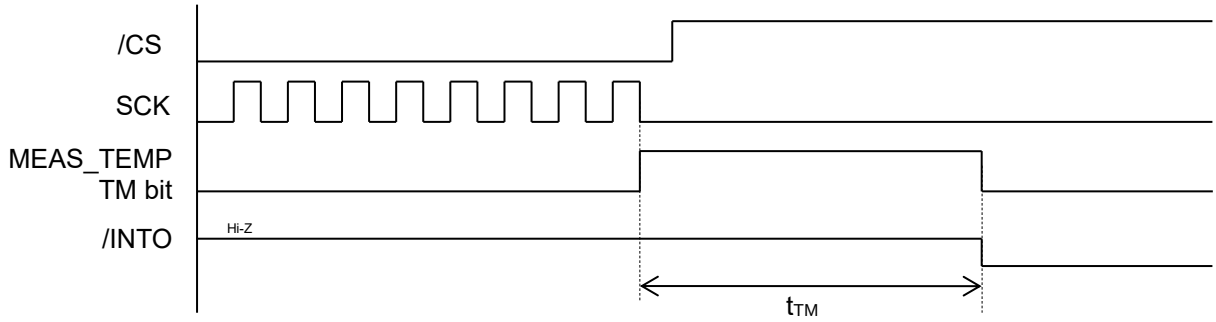


- Temperature Sensor Measurement Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load .

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TEMP1 and TEMP2 pins input current	I_{TEMP}	V_{IN}=0V to V_{REG}	-2	—	2	µA
TEMP1 and TEMP2 pins input voltage measurement error	V_{TER}	TEMP input = 0.3 to 2.3V	-25	—	25	mV
Temperature sensor measurement step	V_{TLSB}	—	—	2500/4095	—	mV
Temperature sensor measurement time	t_{TEMP}	—	0.8	1.0	1.3	ms

Temperature sensor measurement timing diagram

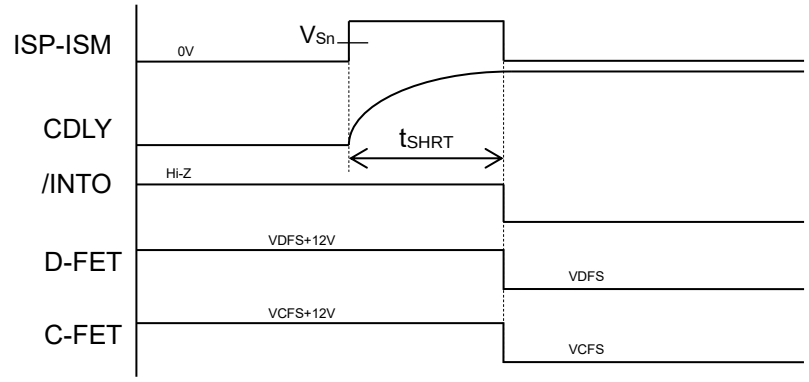


- Short circuit Detection and VREG Threshold Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Short circuit detection threshold	V_{S0T}	SC1 and SC0 bits = (0,0) Ta = 25°C	30	50	70	mV
	V_{S1T}	SC1 and SC0 bits = (0,1), Ta = 25°C	75	100	125	mV
	V_{S2T}	SC1 and SC0 bits = (1,0), Ta = 25°C	120	150	180	mV
	V_{S3T}	SC1 and SC0 bits = (1,1), Ta = 25°C	160	200	240	mV
	V_{S0}	SC1 and SC0 bits = (0,0)	25	50	75	mV
	V_{S1}	SC1 and SC0 bits = (0,1)	65	100	135	mV
	V_{S2}	SC1 and SC0 bits = (1,0)	110	150	190	mV
	V_{S3}	SC1 and SC0 bits = (1,1)	140	200	260	mV
Short circuit detection delay time	t_{SHRT}	C_{DLY}=1nF	50	100	180	µs
VREG drop threshold	V_{RD}	—	2.3	2.45	2.6	V
VREG recovery threshold	V_{RR}	—	2.5	2.75	2.9	V

Short current detection timing diagram



- PSNS-and-DFS-Pins Voltage Measurement and Charger Detection Threshold Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

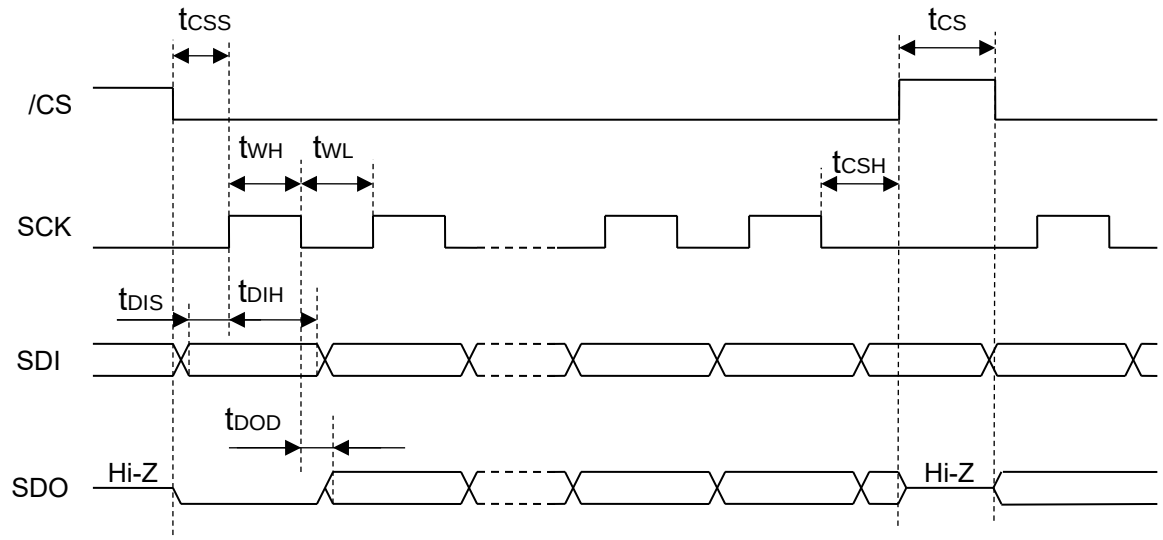
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PSNS and DFS pins input voltage measurement error	V_{ERS}	Input voltage = 64V	-5	—	5	V
PSNS and DFS pins input voltage measurement step	V_{SLSB}	—	—	19.536	—	mV
PSNS and DFS pins input voltage measurement time	t_{SM}	—	1.6	2.0	2.6	ms
Charger detection PSNS pin threshold	V_{PC}	When powered-up from the power down state	V_{DD}X0.2	V_{DD}X0.5	V_{DD}X0.8	V
PSNS pull-down resistance	R_{PD}	PSNS pin voltage is not being measured	200	500	1000	KΩ
DFS pull-up resistor	R_{PU}	DFS pin voltage is not being measured	0.5	2	4	MΩ
Pull-down resistance during voltage measurement on PSNS and DFS pins	R_{DM}	Pull-down/pull-up resistor released	8	20	50	MΩ
PSNS input leakage current	I_{LPS}	Pull-down resistor released PSNS pin voltage is not being measured	-2	—	2	µA
DFS input leakage current	I_{LFS}	Pull-up resistor released D-FET turned OFF DFS pin voltage is not being measured	-2	—	2	µA

- AC Characteristics

V_{DD} = 8 to 64V, V_{SPI} = 2.7 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
/CS-SCK setup time	t_{CSS}	—	100	—	—	ns
SCK-/CS hold time	t_{CSH}	—	100	—	—	ns
SCK “H” pulse width	t_{WH}	—	500	—	—	ns
SCK “L” pulse width	t_{WL}	—	500	—	—	ns
SCK-SDI setup time	t_{DIS}	—	50	—	—	ns
SCK-SDI hold time	t_{DIH}	—	50	—	—	ns
SCK-SDO output delay time	t_{DOD}	—	—	—	400	ns
/CS “H” pulse width	t_{CS}	—	500	—	—	ns
/PUPIN “L” pulse width	t_{PUP}	—	1	—	—	ms

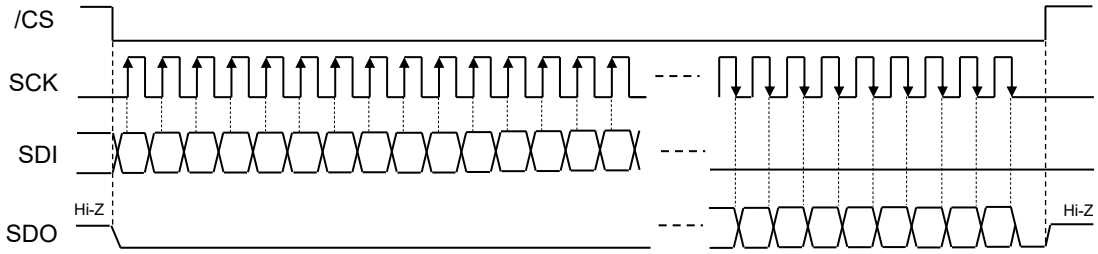
Serial interface timing diagram



■ Functional Description

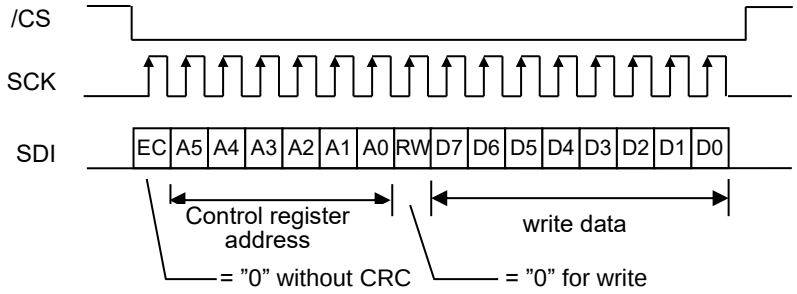
● MCU Interface

The ML5236 is equipped with the SPI interface.
The SPI interface is enabled by asserting the /CS pin to the ”L” level. It takes in the MSB-first input data on the SDI pin synchronous to the rising edges of SCK clock. Output- data is supplied on the SDO pin in the MSB-first order synchronous to the falling edges of SCK clock. The SPI interface is disabled with the ”H” level input on the /CS pin and returns to the initial state. The /CS pin should be fixed to the ”H” level every time after one data write/read operation is completed.

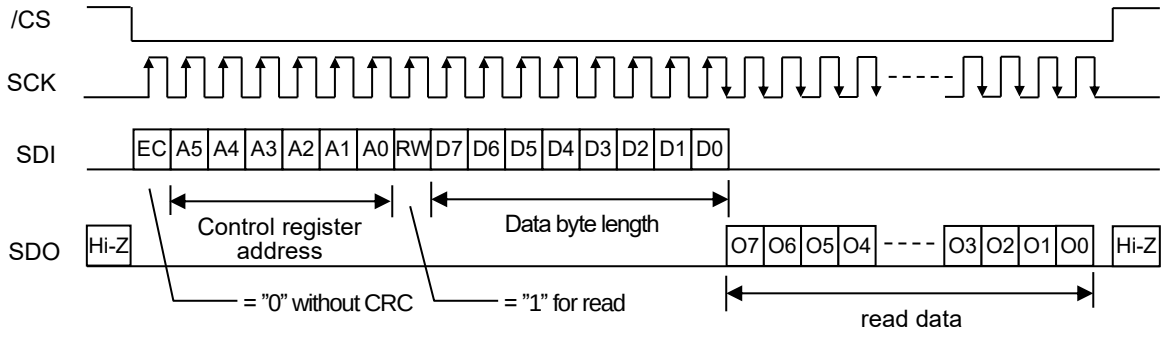


Configurations and controls can be done by reading/writing corresponding addresses in the control register. Write data is one-byte length, while read data length is specified in read commands. Set the RW bit to ”0” for data write and ”1” for data read. Also, set the EC bit to ”1” if the CRC code for detecting a communication error is required, or to ”0” otherwise.
When using by applying an external voltage to the VSPI pin, set the /CS pin level at power down to "H" level.

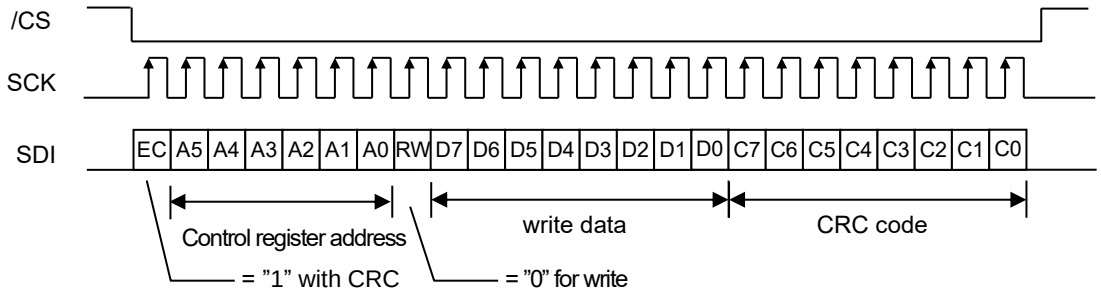
1. Data Write Communication Format without CRC



2. Data Read Communication Format without CRC

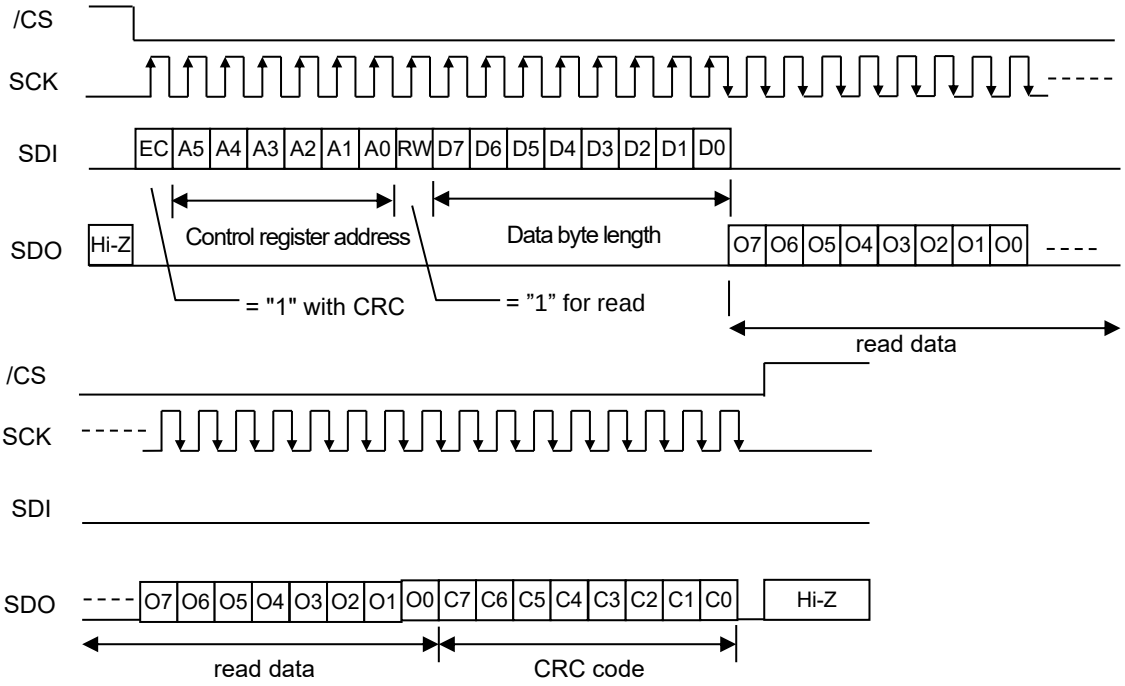


3. Data Write Communication Format with CRC



If the EC bit is enabled, 1-byte CRC (Cyclic Redundancy Code) is generated according to an X^8+X^2+X+1 equation, and added at the end of each communication data. Set the /CS pin to the "H" level to initialize CRC computation to the default FF [h].
Data write is performed on the specified control register only if the result from CRC computation matches the received CRC. Otherwise, data write is not performed. When a CRC error is detected, the CRC error flag is set, allowing the interrupt signal to the external MCU to be asserted on the /INTO pin. For details, refer to the INT_EN and INT_REQ registers description.

4. Data Read Communication Format with CRC



The CRC computation is also performed for each transmitted/received data during data read operation and the result is appended at the end of the read data. The external MCU can detect any communication errors by comparing the CRC computation result and the received CRC. The CRC code is not included in the data byte length.

- Control Register

The control register map is shown below.

Address	Register name	R/W	Default	Description
00H	NOOP	R/W	00H	User register
01H	INT_EN1	R/W	00H	Interrupt enable 1
02H	INT_EN2	R/W	00H	Interrupt enable 2
03H	INT_REQ1	R/W	00H	Interrupt request 1
04H	INT_REQ2	R/W	00H	Interrupt request 2
05H	VMEAS	R/W	00H	Cell voltage measurement control
06H	IMEAS	R/W	00H	Current measurement control
07H	TMEAS	R/W	00H	Temperature measurement control
08H	SMEAS	R/W	00H	PSNS/DFS pin voltage measurement control
09H	FET	R/W	00H	FET control
0AH	CBALL	R/W	00H	Cell balancing control (lower 8 cells)
0BH	CBALH	R/W	00H	Cell balancing control (higher 8 cells)
0CH	POWER	R/W	00H	Power-save/power-down control
0DH	STATUS	R	00H	Status register
0EH	SCWDT	R/W	00H	Short circuit detection threshold/watchdog timer control
0FH	SETOV	R/W	00H	Overvoltage alarm control
10H	OVDETL	R/W	FFH	Overvoltage threshold (low-order 8 bits)
11H	OVDETH	R/W	0FH	Overvoltage threshold (high-order 4 bits)
12H	VCELL1L	R	00H	Cell 1 voltage measurement result (low-order 8 bits)
13H	VCELL1H	R	00H	Cell 1 voltage measurement result (high-order 4 bits)
14H	VCELL2L	R	00H	Cell 2 voltage measurement result (low-order 8 bits)
15H	VCELL2H	R	00H	Cell 2 voltage measurement result (high-order 4 bits)
16H	VCELL3L	R	00H	Cell 3 voltage measurement result (low-order 8 bits)
17H	VCELL3H	R	00H	Cell 3 voltage measurement result (high-order 4 bits)
18H	VCELL4L	R	00H	Cell 4 voltage measurement result (low-order 8 bits)
19H	VCELL4H	R	00H	Cell 4 voltage measurement result (high-order 4 bits)
1AH	VCELL5L	R	00H	Cell 5 voltage measurement result (low-order 8 bits)
1BH	VCELL5H	R	00H	Cell 5 voltage measurement result (high-order 4 bits)
1CH	VCELL6L	R	00H	Cell 6 voltage measurement result (low-order 8 bits)
1DH	VCELL6H	R	00H	Cell 6 voltage measurement result (high-order 4 bits)
1EH	VCELL7L	R	00H	Cell 7 voltage measurement result (low-order 8 bits)
1FH	VCELL7H	R	00H	Cell 7 voltage measurement result (high-order 4 bits)
20H	VCELL8L	R	00H	Cell 8 voltage measurement result (low-order 8 bits)
21H	VCELL8H	R	00H	Cell 8 voltage measurement result (high-order 4 bits)

Address	Register name	R/W	Default	Description
22H	VCELL9L	R	00H	Cell 9 voltage measurement result (low-order 8 bits)
23H	VCELL9H	R	00H	Cell 9 voltage measurement result (high-order 4 bits)
24H	VCELL10L	R	00H	Cell 10 voltage measurement result (low-order 8 bits)
25H	VCELL10H	R	00H	Cell 10 voltage measurement result (high-order 4 bits)
26H	VCELL11L	R	00H	Cell 11 voltage measurement result (low-order 8 bits)
27H	VCELL11H	R	00H	Cell 11 voltage measurement result (high-order 4 bits)
28H	VCELL12L	R	00H	Cell 12 voltage measurement result (low-order 8 bits)
29H	VCELL12H	R	00H	Cell 12 voltage measurement result (high-order 4 bits)
2AH	VCELL13L	R	00H	Cell 13 voltage measurement result (low-order 8 bits)
2BH	VCELL13H	R	00H	Cell 13 voltage measurement result (high-order 4 bits)
2CH	VCELL14L	R	00H	Cell 14 voltage measurement result (low-order 8 bits)
2DH	VCELL14H	R	00H	Cell 14 voltage measurement result (high-order 4 bits)
2EH	CURL	R	00H	Current measurement result (low-order 8 bits)
2FH	CURH	R	00H	Current measurement result (high-order 8 bits)
30H	TEMP1L	R	00H	Temperature 1 measurement result (low-order 8 bits)
31H	TEMP1H	R	00H	Temperature 1 measurement result (high-order 4 bits)
32H	TEMP2L	R	00H	Temperature 2 measurement result (low-order 8 bits)
33H	TEMP2H	R	00H	Temperature 2 measurement result (high-order 4 bits)
34H	SNSL	R	00H	PSNS/DFS measurement result (low-order 8 bits)
35H	SNSH	R	00H	PSNS/DFS measurement result (high-order 4 bits)

1. NOOP Register (Adrs = 00H)

	7	6	5	4	3	2	1	0
Bit name	NO7	NO6	NO5	NO4	NO3	NO2	NO1	NO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

No function is assigned to the NOOP register. Read/write access to this register does not change the LSI status. The written data can be read as it is.

2. INT_EN1 Register (Adrs = 01H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	ESM	ETM	EIM	EVM
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The INT_EN1 register enables or disables the interrupt signal output on the /INTO pin.

The EVM bit enables or disables the interrupt signal output at the completion of cell voltage measurement.

EVM	Cell voltage measurement complete interrupt
0	Disabled (default)
1	Enabled

The EIM bit enables or disables the interrupt signal output at the completion of current measurement.

EIM	Current measurement complete interrupt
0	Disabled (default)
1	Enabled

The ETM bit enables or disables the interrupt signal output at the completion of temperature sensor measurement.

ETM	Temperature sensor measurement complete interrupt
0	Disabled (default)
1	Enabled

The ESM bit enables or disables the interrupt signal output at the completion of PSNS/DFS pin voltage measurement.

ESM	PSNS/DFS pin voltage measurement complete interrupt
0	Disabled (default)
1	Enabled

3. INT_EN2 Register (Adrs = 02H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	EWDT	ECKSP	ECRC	ESC	EOV
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The INT_EN2 register enables or disables the interrupt signal output on the /INTO pin.

The EOV bit enables or disables the interrupt signal output at overvoltage detection.

EOV	Overvoltage detection interrupt
0	Disabled (default)
1	Enabled

The ESC bit enables or disables the interrupt signal output at short circuit detection.

ESC	Short circuit detection interrupt
0	Disabled (default)
1	Enabled

The ECRC bit enables or disables the interrupt signal output at CRC error detection.

ECRC	CRC error interrupt
0	Disabled (default)
1	Enabled

The ECKSP bit enables or disables the interrupt signal output when the internal clock is halted.

ECKSP	Internal clock halt interrupt
0	Disabled (default)
1	Enabled

The EWDT bit enables or disables the interrupt signal output when a watchdog timer overflow occurs.

EWDT	WDT overflow interrupt
0	Disabled (default)
1	Enabled

4. INT_REQ1 Register (Adrs = 03H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	QSM	QTM	QIM	QVM
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The INT_REQ1 register contains interrupt request flags. Each request flag is set to "1" when the corresponding interrupt request is generated, regardless of the INT_EN1 register configuration. Only if the generated interrupt is enabled by the INT_EN1 register, the “L” level is asserted on the /INTO pin. An interrupt request flag can be cleared by writing data “0” to the corresponding data bit. Since writing data “1” is ignored, if you want to clear one specific interrupt request flag, fill in data "1" to the other bits. When all the enabled interrupt request flags are cleared, the /INTO pin is set to the "Hi-Z" level.

The QVM bit indicates the interrupt request generated on completion of cell voltage measurement.

QVM	Cell voltage measurement complete interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QIM bit indicates the interrupt request generated on completion of current measurement.

QIM	Current measurement complete interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QTM bit indicates the interrupt request generated on completion of temperature measurement.

QTM	Temperature measurement complete interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QSM bit indicates the interrupt request generated on completion of PSNS/DFS pin voltage measurement.

QSM	PSNS/DFS pin voltage measurement complete interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

5. INT_REQ2 Register (Adrs = 04H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	QWDT	QCKSP	QCRC	QSC	QOV
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The INT_REQ2 register contains interrupt request flags. Each request flag is set to "1" when the corresponding interrupt request is generated, regardless of the INT_EN2 register configuration. Only if the generated interrupt is enabled by the INT_EN2 register, the “L” level is asserted on the /INTO pin. An interrupt request flag can be cleared by writing data “0” to the corresponding data bit. Since writing data “1” is ignored,if you want to clear one specific interrupt request flag, fill in data "1" to the other bits. When all enabled interrupt request flags are cleared, the /INTO pin is set to the "Hi-Z" level.

The QOV bit indicates the interrupt request generated at overvoltage detection.

QOV	Overvoltage detection interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QSC bit indicates the interrupt request generated at short circuit detection.

QSC	Short circuit detection interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QCRC bit indicates the interrupt request generated at CRC error detection.

QCRC	CRC error interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QCKSP bit indicates the interrupt request generated when the internal clock stop is halted.

QCKSP	Internal clock halt interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

The QWDT bit indicates the interrupt request generated when a watchdog timer overflow occurs.

QWDT	WDT overflow interrupt request
0	No interrupt request (default)
1	An interrupt request is generated

6. VMEAS Register (Adrs = 05H)

	7	6	5	4	3	2	1	0
Bit name	VM	—	—	SCAN	VC3	VC2	VC1	VC0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The VMEAS register configures the cell voltage measurement conditions.

Configure the SCAN bit and the V0 to V3 bits to select the measurement mode and the battery cell(s) to measure.

SCAN	VC3	VC2	VC1	VC0	Cell voltage measurement
0	0	0	0	0	Cell 1 selected
0	0	0	0	1	Cell 2 selected
0	0	0	1	0	Cell 3 selected
0	0	0	1	1	Cell 4 selected
0	0	1	0	0	Cell 5 selected
0	0	1	0	1	Cell 6 selected
0	0	1	1	0	Cell 7 selected
0	0	1	1	1	Cell 8 selected
0	1	0	0	0	Cell 9 selected
0	1	0	0	1	Cell 10 selected
0	1	0	1	0	Cell 11 selected
0	1	0	1	1	Cell 12 selected
0	1	1	0	0	Cell 13 selected
0	1	1	0	1	Cell 14 selected
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	
1	0	0	0	1	Cell 13 to cell 14 scanned
1	0	0	1	0	Cell 12 to cell 14 scanned
1	0	0	1	1	Cell 11 to cell 14 scanned
1	0	1	0	0	Cell 10 to cell 14 scanned
1	0	1	0	1	Cell 9 to cell 14 scanned
1	0	1	1	0	Cell 8 to cell 14 scanned
1	0	1	1	1	Cell 7 to cell 14 scanned
1	1	0	0	0	Cell 6 to cell 14 scanned
1	1	0	0	1	Cell 5 to cell 14 scanned
1	1	0	1	0	Cell 4 to cell 14 scanned
1	1	0	1	1	Cell 3 to cell 14 scanned
1	1	1	0	0	Cell 2 to cell 14 scanned
1	1	1	0	1	Cell 1 to cell 14 scanned
1	1	1	1	0	
1	1	1	1	1	

The VM bit starts or stops cell voltage measurement operation and indicates the cell voltage measurement status at the same time. The cell voltage measurement results are stored in the VCELLnL and VCELLnH registers (12H to 2DH).

Write		Read	
VM	Cell voltage measurement	VM	Cell voltage measurement
0	Stop (default)	0	Completed/stopped (default)
1	Start	1	Being measured

If the value “0” is written to the VM bit in the middle of cell voltage measurement, the on-going measurement is completed before measurement is stopped. The VM bit value continues to be “1” until the end of measurement, and it is reset to “0” when the measurement stops.
Any changes to the SCAN and VC3 to VC0 bits are ignored during measurement (while the VM bit is “1”).
Also, writing the value “1” to the VM bit during current measurement, temperature measurement, or PSNS/DFS pin voltage measurement is ignored.

7. IMEAS Register (Adrs = 06H)

	7	6	5	4	3	2	1	0
Bit name	IM	—	—	ENIM	—	—	ZERO	GIM
R/W	R/W	R	R	R/W	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

The IMEAS register controls current measurement and its conditions.
The GIM bit selects the voltage gain of the current measurement amplifier.

GIM	Voltage gain G_{IM}
0	12 times (default)
1	60 times

The ZERO bit executes zero current compensation of the current measurement amplifier. Because the compensated values may differ for different voltage gains of the current measurement amplifier or different temperatures, periodic compensations are suggested for each voltage gain.

ZERO	ISP input	ISM input	State
0	Pin input level	Pin input level	Current measurement enabled
1	GND level	GND level	Zero current compensation enabled

The ENIM bit runs and stops the current measurement amplifier.

ENIM	Current measurement amplifier
0	Stop (default)
1	Run

If the value “1” is written to the IM bit, current measurement is repeated for 16 times. For zero current compensation, if the value “1” is written to both the ZERO bit and IM bit , zero current compensation is repeated for 16 times. When the ENIM bit is “0”, writing “1” to the IM bit does not execute current measurement or compensation.
Current measurement status can be obtained by reading the IM bit.
The 16-times repeated measurement results are summed up and stored as a 16-bit data to the CURL and CURH registers (2EH to 2FH).

Write		Read	
IM	Current measurement	IM	Current measurement
0	Not being measured (default)	0	Completed (default)
1	Start	1	Being measured

After the current measurement is started, writing “0” to the IM bit does not stop the current measurement in progress. Also, writing “1” to the IM bit during cell voltage measurement, temperature measurement, or PSNS/DFS pin voltage measurement is ignored.

8. TMEAS Register (Adrs = 07H)

	7	6	5	4	3	2	1	0
Bit name	TM	—	—	—	—	—	TSEL	TDRV
R/W	R/W	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

The TMEAS register controls temperature measurement and its conditions. The input voltage on the TEMP1 and TEMP2 pins can be measured.

The TDRV bit specifies the TDRV pin output status.
The temperature measurement should be performed after the input voltages on the TEMP1 and TEMP2 pins are stabilized.

TDRV	TDRV pin status
0	Hi-Z (default)
1	0V

The TSEL bit selects the input pin to be measured.

TSEL	TEMP pin to be measured
0	TEMP1 pin (default)
1	TEMP2 pin

Writing “0” to the TM bit executes temperature measurement. The temperature measurement result is stored in the TEMPnL and TEMPnH registers (30H to 33H).

Write		Read	
TM	TEMP pin measurement	TM	TEMP pin measurement
0	Not being measured (default)	0	Completed (default)
1	Start	1	Being measured

After temperature measurement is started, writing “0” to the TM bit does not stop the temperature measurement in progress. Also, writing “1” the TM bit during cell voltage measurement, current measurement, or PSNS/DFS pin voltage measurement is ignored.

9. SMEAS Register (Adrs = 08H)

	7	6	5	4	3	2	1	0
Bit name	SM	—	—	ENSM	—	SSEL	PU	PD
R/W	R/W	R	R	R/W	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The SMEAS register controls voltage measurement on the PSNS and DFS pins, configures the pull-down resistor on the PSNS pin and the pull-up resistor on the DFS pin. The 1/32-fold voltage of the input levels on the PSNS and DFS pins can be measured.

The PD bit specifies the connection of a pull-down resistor on the PSNS pin.

PD	PSNS pin status
0	Pull-down resistor not connected (default)
1	500kΩ pull-down resistor connected

The PU bit specifies the connection of a pull-up resistor on the DFS pin.

PU	DFS pin status
0	Pull-up resistor not connected (default)
1	2MΩ pull-up resistor connected

The SSEL bit selects the input pin to be measured.

SSEL	Pin to be measured
0	PSNS pin (default)
1	DFS pin

The ENSM bit runs and stops the PSNS/DFS pin voltage measurement circuit.

ENSM	Measurement circuit
0	Stop (default)
1	Run

Writing "1" to the SM bit executes voltage measurement on the PSNS or DFS pin. The measurement result is stored in the SNSL and SNSH registers (34H to 35H). When the ENSM bit is set to "0", writing "1" to the SM bit does not execute measurement.

Write		Read	
SM	Pin voltage measurement	SM	Pin voltage measurement
0	Not being measured (default)	0	Completed (default)
1	Start	1	Being measured

After voltage measurement is started, writing "0" to the SM bit does not stop the measurement in progress. Also, writing "1" to the SM bit during cell voltage measurement, current measurement, or temperature measurement is ignored.

10. FET Register (Adrs = 09H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	CF	DF
R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

The FET register turns on or turns off the C-FET and D-FET pins, and the C-/D-FET output status can be obtained by reading it.

The DF bit specifies the D-FET pin output status. When short circuit is detected, the DF bit is automatically reset to "0". Note that it is not automatically set to "1" even after the short circuit detection state is restored to the normal state. It is required to turn on the DF pin using the external MCU.

DF	Discharge-FET status	D-FET pin output level
0	OFF (default)	DFS pin level V_{DFS}
1	ON	V_{DFS}+12V(typ)

The CF bit specifies the C-FET pin output status. When short circuit is detected, the CF bit is automatically reset to "0". Note that it is not automatically set to "1" even after the short circuit detection state is restored to the normal state. It is required to turn on the CF pin using the external MCU.

CF	Charge–FET status	C_FET pin output level
0	OFF (default)	CFS pin level V_{CFS}
1	ON	V_{CFS}+12V(typ)

11. CBALL Register (Adrs = 0AH)

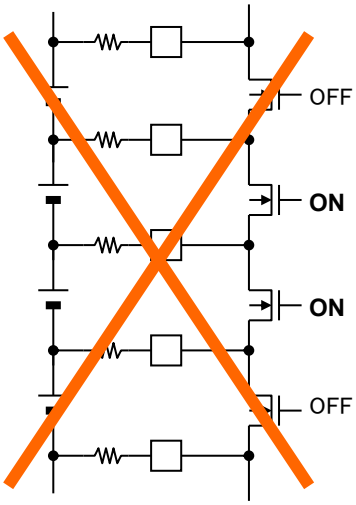
	7	6	5	4	3	2	1	0
Bit name	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

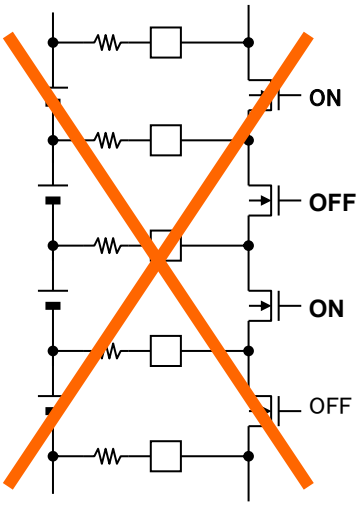
The CBALL register turns ON or turns OFF the cell balancing switches for the lower 8 cells.
Use the SW8 to SW1 bits to control the respective cells.

SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	Switch ON/OFF
0	0	0	0	0	0	0	0	Lower 8 cells turned OFF (default)
0	0	0	0	0	0	0	1	V1-to-V0 switch turned ON
0	0	0	0	0	0	1	0	V2-to-V1 switch turned ON
0	0	0	0	0	1	0	0	V3-to-V2 switch turned ON
0	0	0	0	1	0	0	0	V4-to-V3 switch turned ON
0	0	0	1	0	0	0	0	V5-to-V4 switch turned ON
0	0	1	0	0	0	0	0	V6-to-V5 switch turned ON
0	1	0	0	0	0	0	0	V7-to-V6 switch turned ON
1	0	0	0	0	0	0	0	V8-to-V7 switch turned ON

Multiple switches can be turned ON simultaneously, but the following configurations are inhibited, because they may damage the built-in cell balancing switches.

(1) Do not turn on adjacent cell balancing switches.
(2) Do not turn on cell balancing switches simultaneously on both sides of a cell balancing switch that is turned OFF.





The cell balancing current and the ON-resistance of cell balancing switch generate heat. Configure the number of turned-on switches and the turned-on duration so that the total power loss in the cell balancing switches does not exceed the power dissipation limit.

12. CBALH Register (Adrs = 0BH)

	7	6	5	4	3	2	1	0
Bit name	—	—	SW14	SW13	SW12	SW11	SW10	SW9
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

The CBALH register turns ON or turns OFF the cell balancing switches for the higher 6 cells. Use the SW14 to SW9 bits to control the respective cells.

SW14	SW13	SW12	SW11	SW10	SW9	Switch ON/OFF
0	0	0	0	0	0	Higher 6 cells turned OFF (default)
0	0	0	0	0	1	V9-to-V8 switch turned ON
0	0	0	0	1	0	V10-to-V9 switch turned ON
0	0	0	1	0	0	V11-to-V10 switch turned ON
0	0	1	0	0	0	V12-to-V11 switch turned ON
0	1	0	0	0	0	V13-to-V12 switch turned ON
1	0	0	0	0	0	V14-to-V13 switch turned ON

The same restrictions apply to the switch ON configurations as the CBALL register.

13. POWER Register (Adrs = 0CH)

	7	6	5	4	3	2	1	0
Bit name	PUPIN	—	—	PDWN	—	—	—	PSV
R/W	R	R	R	R/W	R	R	R	R/W
Default	0	0	0	0	0	0	0	0

The POWER register controls the power-save and power-down operation states.

The PSV bit enables the power-save state.

PSV	Power-save state
0	Normal state (default)
1	Power-save

In the power-save state, only the circuits required for the VREG and VREF outputs are activated, and the measurement circuits for cell voltage or pack current are halted so as to reduce the current consumption. Even in the middle of measurement, the power-save state is enabled right away and halts the measurement in progress. Note that a measurement complete interrupt request flag is set, in this case. All cell balancing switches are initialized to OFF condition at the transition to the power-save state, while other settings are maintained in the power-save state.
The FET drive circuit and short current detection circuit continue to operate even in the power-save state.
However, operating frequency of charge pump circuit for FET drive is reduced to 1/4 of normal state for the purpose of saving current consumption. Therefore, in the power-save state turning on the C-FET or D-FET takes longer than in the normal state. It is thus recommended to turn on the FETs after transitioning to the normal state.
The power-save state can be restored to the normal state by resetting the PSV bit to “0”.

The PDWN bit enables the power-down state.

PDWN	Power-down state
0	Normal state (default)
1	Power-down

If the PDWN bit is set to “1”, a 500kΩ pull-down resistor is automatically connected to the PSNS pin and all circuit operations are halted.
Before setting the PDWN bit to “1”, both the C-FET and D-FET pins should be turned off, and confirm that a charger is not present by measuring the PSNS pin level. If the /PUPIN pin input is “L”level, the power-down state is not enabled until the /PUPIN pin input becomes “H” level, even after the PDWN bit is set to “1”. As the /PUPIN pin status can be read from the PUPIN bit, check that the /PUPIN pin status is not “L” level before setting the PDWN bit to “1”.

PUPIN	/PUPIN pin status
0	“H” level
1	“L” level

The power-down state is cleared with a charger detection through the PSNS pin or with the “L” level input on the /PUPIN pin.
At the recovery from the power-down state, all required configurations need to be initialized after the VREG output becomes valid.

14. STATUS Register (Adrs = 0DH)

	7	6	5	4	3	2	1	0
Bit name	INT	CKSP	WDT	OV	CBAL	PSV	CF	DF
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The STATUS register indicates status information.

The DF bit indicates the D-FET pin output status.

DF	D-FET pin status
0	OFF (default)
1	ON

The CF bit indicates the C-FET pin output status.

CF	C-FET status
0	OFF (default)
1	ON

The PSV bit indicates the power-save state.

PSV	Power-save
0	Normal operation (default)
1	Power-save

The CBAL bit indicates the ON state of cell balancing switches.

CBAL	Cell balancing switch ON state
0	All OFF (default)
1	One or more are ON

The OV bit indicates overvoltage detection state.

OV	Overvoltage detection state
0	Not detected (default)
1	Overvoltage detected

The WDT bit indicates the watchdog timer overflow state.

WDT	WDT overflow state
0	Not detected (default)
1	Overflow detected

The CKSP bit indicates the clock halt detection state.

CKSP	Clock halt detection state
0	Not detected (default)
1	Clock halted

The INT bit indicates the /INTO pin output status.

INT	/INTO pin output state
0	No interrupt (default)
1	An interrupt signal generated

15. SCWDT Register (Adrs = 0EH)

	7	6	5	4	3	2	1	0
Bit name	ENWD	—	WDT1	WDT0	ENSC	—	SC1	SC0
R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

The SCWDT register configures the short circuit detection threshold and the watchdog timer overflow period, and controls operations of these functions.

The SC0 and SC1 bits select the short circuit detection threshold corresponding to the shunt resistance. Do not change these values during the measurement operation.

SC1	SC0	Short detection threshold (ISP-to-ISM pin voltage)	Equivalent current Shunt resistance = 1mΩ
0	0	50mV (default)	50A
0	1	100mV	100A
1	0	150mV	150A
1	1	200mV	200A

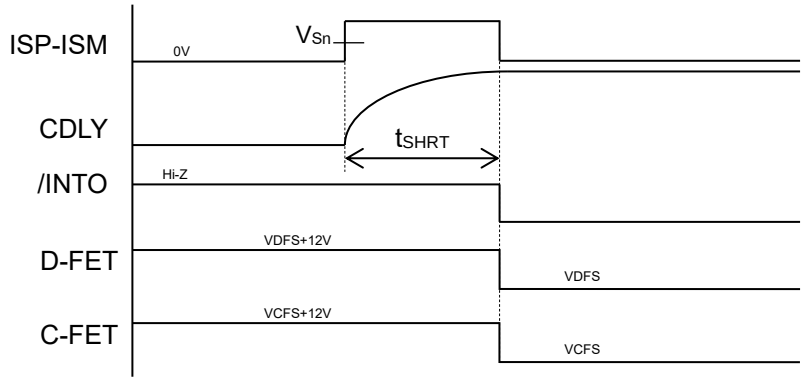
The ENSC bit runs or stops the short circuit detection operation.

ENSC	Short circuit detection operation state
0	Stop (default)
1	Run

Short circuit detection timing is shown in the below diagram.
If the ISP-to-ISM pin voltage difference is equal to or larger than the short circuit detection threshold (V_{Sn}), the delay timer capacitor on the CDLY pin starts charging. If the CDLY pin level is equal to or larger than a specific threshold, the DF and CF bits of the FET register are automatically reset to “0” and charge/discharge is disabled. In this case, if the ESC bit of the INT_EN2 register is set to “1”, the “L” level is asserted on the /INTO pin and a short circuit alarm is notified to the external MCU.

If the short circuit state is cleared while the delay timer capacitor is being charged, charge is discontinued, and the CDLY pin is fixed to the GND level.

Short current detection timing diagram



The short circuit detection delay (t_{SHRT}) depends on the charge time of the delay capacitor (C_{DLY}) on the CDLY pin, which is described as follows:

Short circuit detection delay t_{SC} [μs] = C_{DLY} [nF] x 100

The WDT0 and WDT1 bits configure the overflow period. Do not change these values while the watchdog timer is in operation.

WDT1	WDT0	Overflow period
0	0	1 second (default)
0	1	2 seconds
1	0	4 seconds
1	1	8 seconds

If writing/reading data to the control register is not performed for longer than the overflow period, the QWDT bit of the INT_REQ2 register is set to “1”, and the “L” level is asserted on the /INTO pin.
If WDT overflow is detected twice consecutively, the DF and CF bits of the FET register are automatically set to “0” and charge/discharge is disabled.

The ENWD bit runs or stops the watchdog timer.

ENWD	WDT operation state
0	Stop (default)
1	Run

16. SETOV Register (Adrs = 0FH)

	7	6	5	4	3	2	1	0
Bit name	ENOV	—	SLT1	SLT0	—	CN2	CN1	CN0
R/W	R/W	R	R/W	R/W	R	R	R/W	R/W
Default	0	0	0	0	0	0	0	0

The SETOV register configures the various overvoltage detection conditions.

The CN0 to CN2 bits define the number of consecutive overvoltage detections in scan measurements, which is required to determine an overvoltage alarm. Do not change these values in the middle of measurement.

CN2	CN1	CN0	Number of scan measurements
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Cell voltage measurements in the scan measurement mode are controlled with the VMEAS register. If one or more cell voltage continues to exceed the overvoltage detection threshold for more than the specified number of scan measurements, an overvoltage alarm is tripped, and the QOV bit of the INT_REQ2 register and the OV bit of the STATUS register are set with the CF bit of the FET register is reset to “0” for charge inhibition. Since the CF bit of the FET register is not automatically initialized to “1” after recovery to the normal state, it is necessary to turn on the charge FET using an external MCU.

The SLT0 and SLT1 bits configure the interval time between the cell voltage scan measurements in the power-save state. Do not change these values during the scan measurement operation.

SLT1	SLT0	Interval time
0	0	1 second (default)
0	1	2 seconds
1	0	4 seconds
1	1	8 seconds

In the power-save state, scan measurement is performed for all 14 cells including unused cells at the specified interval time. Fix the unused cell input pins to GND.

The ENOV bit runs and stops overvoltage detection operation.

ENOV	Overvoltage detection operation state
0	Stop (default)
1	Run

17. OVDETL Register (Adrs = 10H)

	7	6	5	4	3	2	1	0
Bit name	OVD7	OVD6	OVD5	OVD4	OVD3	OVD2	OVD1	OVD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	1	1	1	1	1	1	1

The OVDETL register defines the low-order 8 bits of the overvoltage detection threshold. Set this value before initiating overvoltage monitor. Do not change this value in the middle of overvoltage monitor.

18. OVDETH Register (Adrs = 11H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	OVD11	OVD10	OVD9	OVD8
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	1	1	1

The OVDETH register defines the high-order 4 bits of the overvoltage detection threshold. Set this value before initiating overvoltage monitor. Do not change this value during overvoltage monitor.

19. VCELLnL Register (Adrs = even number addresses between 12H and 2CH)

	7	6	5	4	3	2	1	0
Bit name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The VCELLnL register (n = 1 to 14) stores the low-order 8-bit for the A/D conversion result of the individual cell voltages.

20. VCELLnH Register (Adrs = odd number addresses between 13H and 2DH)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	AD11	AD10	AD9	AD8
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The VCELLnH register (n = 1 to 14) stores the high-order 4-bit for the A/D conversion result of the individual cell voltages.

21. CURL Register (Adrs = 2EH)

	7	6	5	4	3	2	1	0
Bit name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The CURL register stores the low-order 8-bit for the A/D conversion result of pack current measurement.

22. CURH Register (Adrs = 2FH)

	7	6	5	4	3	2	1	0
Bit name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The CURH register stores the high-order 8-bit for the A/D conversion result of pack current measurement.

23. TEMPnL Register (Adrs = 30H, 32H)

	7	6	5	4	3	2	1	0
Bit name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The TEMPnL register (n = 1, 2) stores the low-order 8-bit for the A/D conversion result of the TEMP1 and TEMP2 levels

24. TEMPnH Register (Adrs = 31H, 33H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	AD11	AD10	AD9	AD8
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The TEMPnH register (n = 1 or 2) stores the high-order 4-bit for the A/D conversion result of the TEMP1 and TEMP2 levels.

25. SNSL Register (Adrs = 34H)

	7	6	5	4	3	2	1	0
Bit name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The SNSL register stores the low-order 8-bit for the A/D conversion result of the PSNS or DFS level.

26. SNSH Register (Adrs = 35H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	AD11	AD10	AD9	AD8
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

The SNSH register stores the high-order 4-bit for the A/D conversion result of the PSNS or DFS level.

- Cell Connection Table

Cells should be connected to voltage sense pins according to the following table when the series cell count is 13 or less.

Number of connected cells	V14 to V9 pins	V8 pin	V7 pin	V6 pin	V5 pin	V4 pin	V3 pin	V2 pin	V1 pin	V0 pin
13	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	GND
12	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	GND	GND
11	Cell	Cell	Cell	Cell	Cell	Cell	Cell	GND	GND	GND
10	Cell	Cell	Cell	Cell	Cell	Cell	GND	GND	GND	GND
9	Cell	Cell	Cell	Cell	Cell	GND	GND	GND	GND	GND
8	Cell	Cell	Cell	Cell	GND	GND	GND	GND	GND	GND
7	Cell	Cell	Cell	GND	GND	GND	GND	GND	GND	GND
6	Cell	Cell	GND	GND	GND	GND	GND	GND	GND	GND
5	Cell	GND	GND	GND	GND	GND	GND	GND	GND	GND

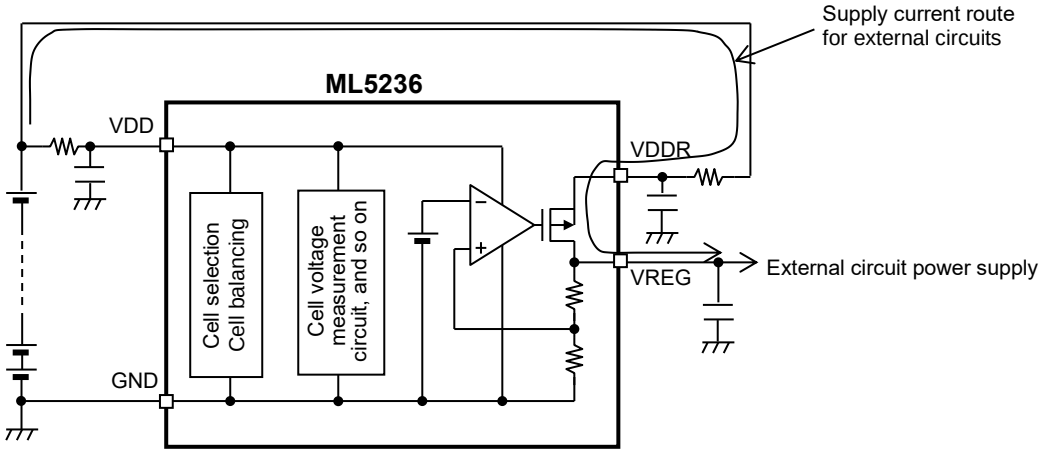
- Handling of Unused Pins

The following table shows how to handle unused pins.

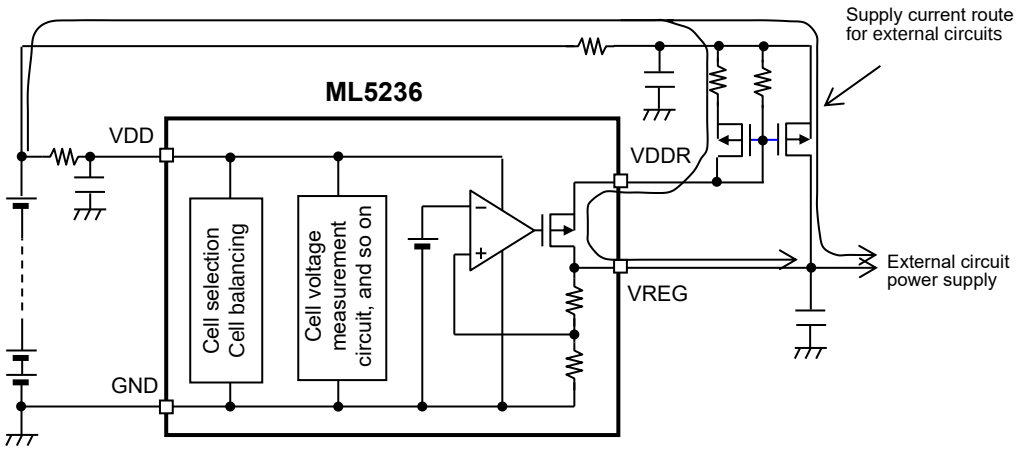
Unused pins	Recommended pin handling
V0 to V8	Tied to GND.
TDRV	Left open or tied to GND .
TEMP1,TEMP2	Tied to GND.
/INTO	Open

- Handling of VDDR and VDD Power Supplies

The VDDR pin is power supply dedicated for the built-in regulator output (VREG). If the regulator output current is high, the RC noise filter should be configured so that the voltage drop across the resistor is 1V or less.
The VDD pin supplies power to all the other circuits except the built-in regulator.

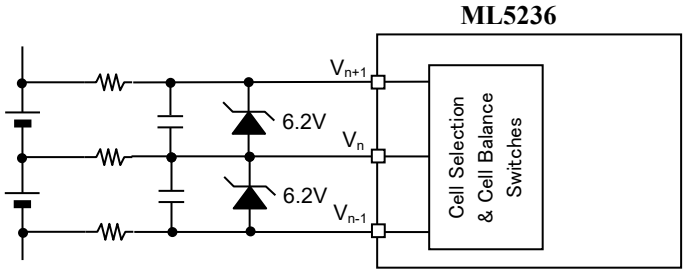


The maximum output current of the built-in regulator (VREG output) is 10mA. If the consumption current of the external circuits exceeds 10mA, configure an external current boost circuit with Pch-FET as in the diagram below.



- Power-on/Power-off Sequence

The recommended sequence of cell connection at power-on is as follows. Tie the GND pin first. Then connect the VDD and VDDR pins. Finally connect the cell voltage monitor pins from the most negative level to the most positive level.
When this sequence is not observed, voltage exceeding the absolute maximum rating may be applied between the adjacent Vn+1 and Vn inputs, resulting in permanent damage on the LSI.
The recommended sequence of cell connection at power-off is as follows. Disconnect cell voltage monitor pins from the most positive level to the most negative level, then disconnect the VDD, VDDR pins, and finally disconnect the GND pin.
Also during tests and evaluation using a battery simulator, cell connection or disconnection sequence should be observed so that voltage exceeding the absolute maximum rating is not applied between the adjacent Vn+1 and Vn inputs.
As shown in the below diagram, a TVS diode for protection is recommended between adjacent cell monitor input pins, which also requires full and detailed evaluation.

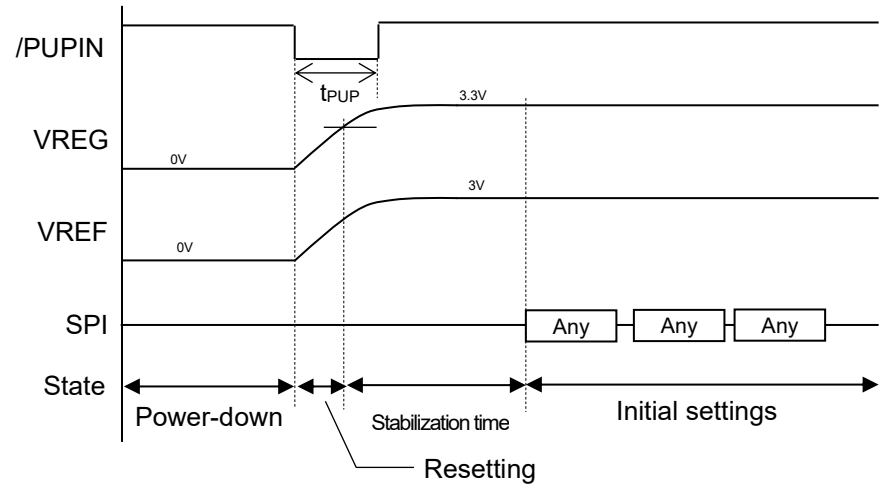


Battery cell should be stack in a series before connected to the V_n pins.
Connecting separate battery cells to the V_n pins is forbidden because the input level between the adjacent V_{n+1} and V_n pins may exceed the absolute maximum rating, resulting in permanent damage on the LSI.

There are no restrictions on the power supply voltage rise time at power-on, power-off sequence, and power supply voltage fall time at power-off.
The operation state after power-on is the normal operation state, but it may be the power-down state due to chattering noise during power-on sequence. Power up the LSI either by asserting a voltage greater than the charger detection threshold (V_{PC}) on the PSNS pin or by asserting the "L" level on the /PUPIN pin.
After the power-on or power-up, wait until the VREG and VREF output levels are stabilized before measuring cell voltages, pack current and temperature. Confirm the VREG and VREF output stabilization times on your actual applications because these values depend on the output load capacitance and other conditions.

The following timing diagram shows the power-up operation.

Power-up operation timing diagram

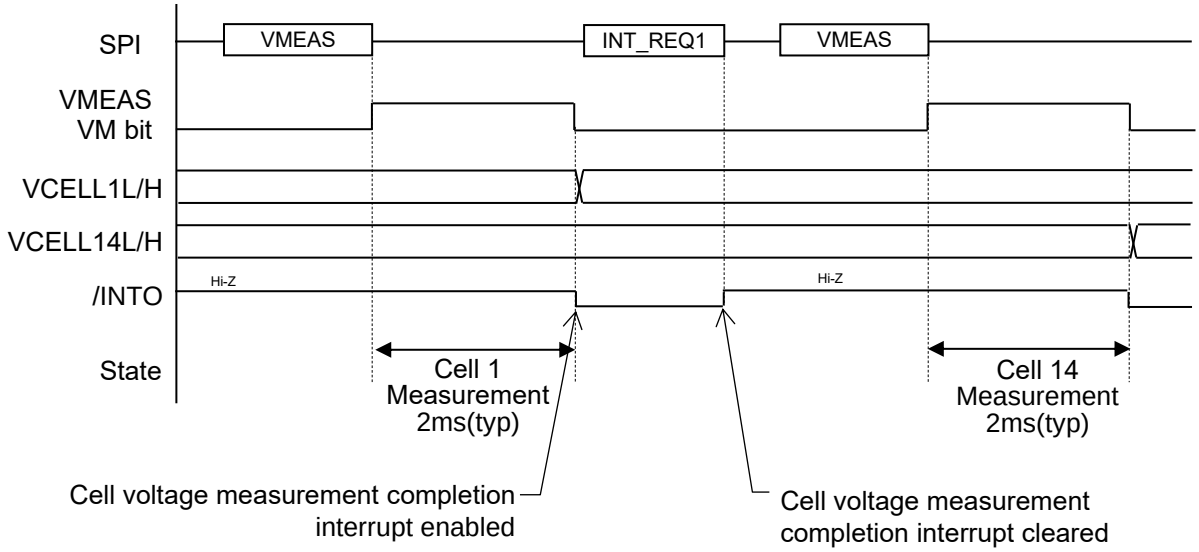


- Cell Voltage Measurement

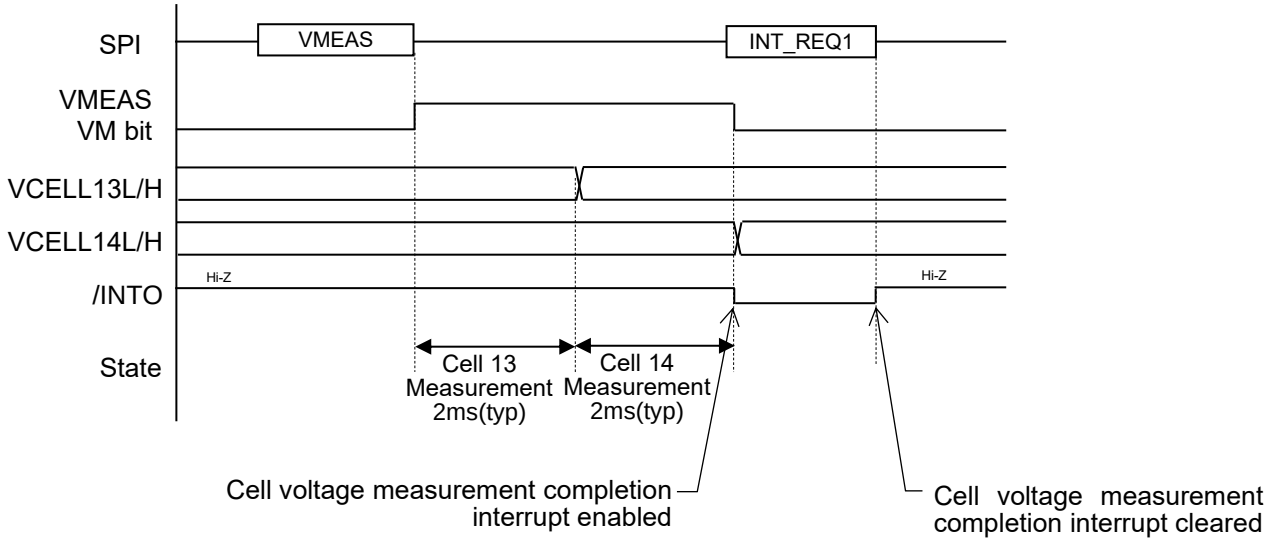
There are two modes in cell voltage measurement, the select mode and the scan mode. The select mode measures the voltage of a selected cell, while the scan mode continuously measures the voltages of selected multiple cells.
The VMEAS register configures the cell voltage measurement conditions and controls measurement operation. For details, see the VMEAS register section.

The following timing diagrams show the cell voltage measurement operation in each measurement mode.

Select measurement timing diagram (Cell 1 and Cell 14 selected)

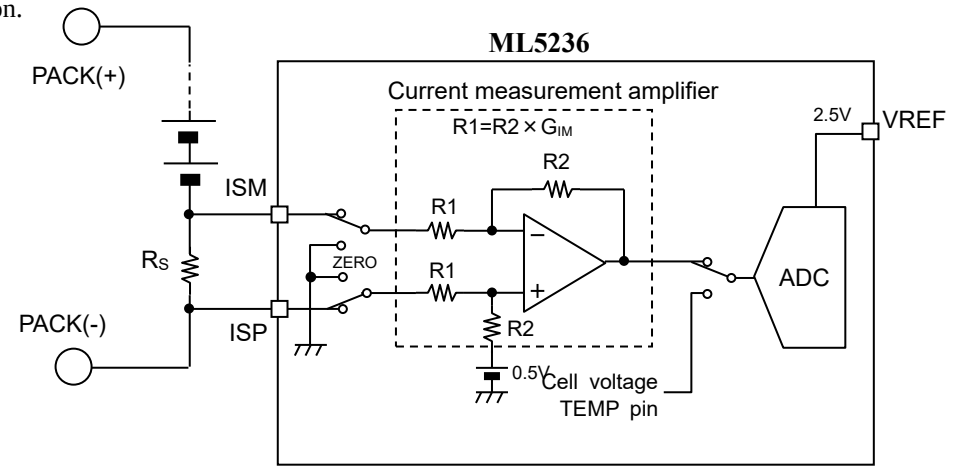


Scan measurement timing diagram (Cell 13 to Cell 14 scanned)



- Current Measurement

A shunt resistor R_S is connected between the ISP and ISM pins, and the input level difference between these pins is amplified and supplied to the A/D converter. The circuit configuration of the current measurement amplifier is shown below.
The IMEAS register configures current measurement conditions. For details, see the IMEAS register section.



The A/D conversion result is 3333H (typ) at zero current, greater than 3333H (typ) during discharge, and less than 3333H (typ) during charge.
The current value can be derived from the A/D conversion result AD_{IM} by the following calculation formula, where the shunt resistor is R_S, the amplifier gain G_{IM}, and the zero current flow compensation value AD_{ZERO}:

$$\text{Current [A]} = (AD_{ZERO} - AD_{IM}) \times (2.5 / 65535) / G_{IM} / R_S$$

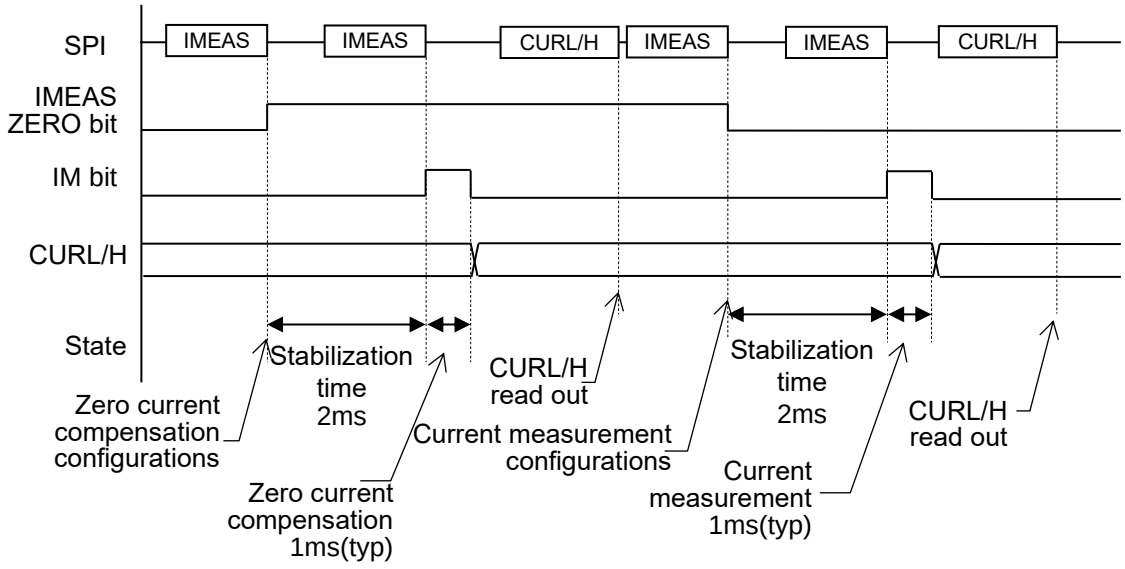
For 12-fold gain with the current measurement result = 3600H, where the zero current compensation value = 3300H, and the shunt resistance = 1mΩ:

Current [A] = (3300H - 3600H) x 2.5/65535/12/1e-3 = -768 x 2.5/65535/12/1e-3 = -2.4414[A]

Since the current amplification gain G_{IM} values may vary between devices, it is recommended to measure G_{IM} on each device for reducing current measurement errors.

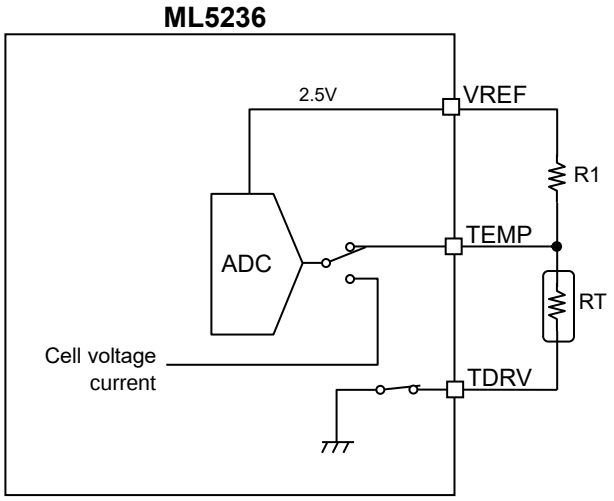
The following timing diagram shows current measurement operation with the zero current compensation performed at 12-fold current amplification gain. Interrupt output on the /INTO pin is not enabled.

Current measurement timing diagram (zero current compensation and current measurements at 12-fold gain)

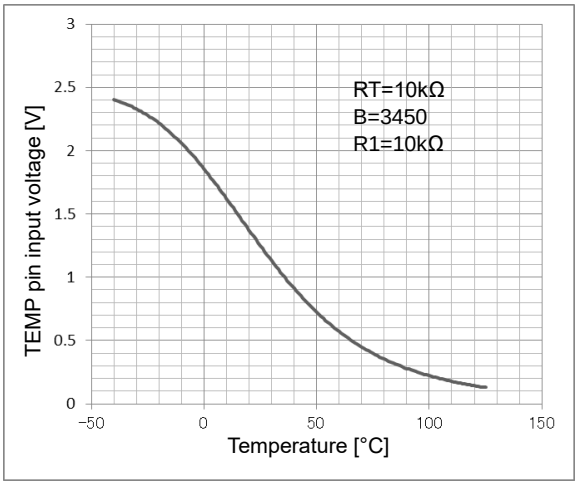


- Temperature Sensor Measurement

Below is an example of the temperature sensor (NTC thermistor) configuration.

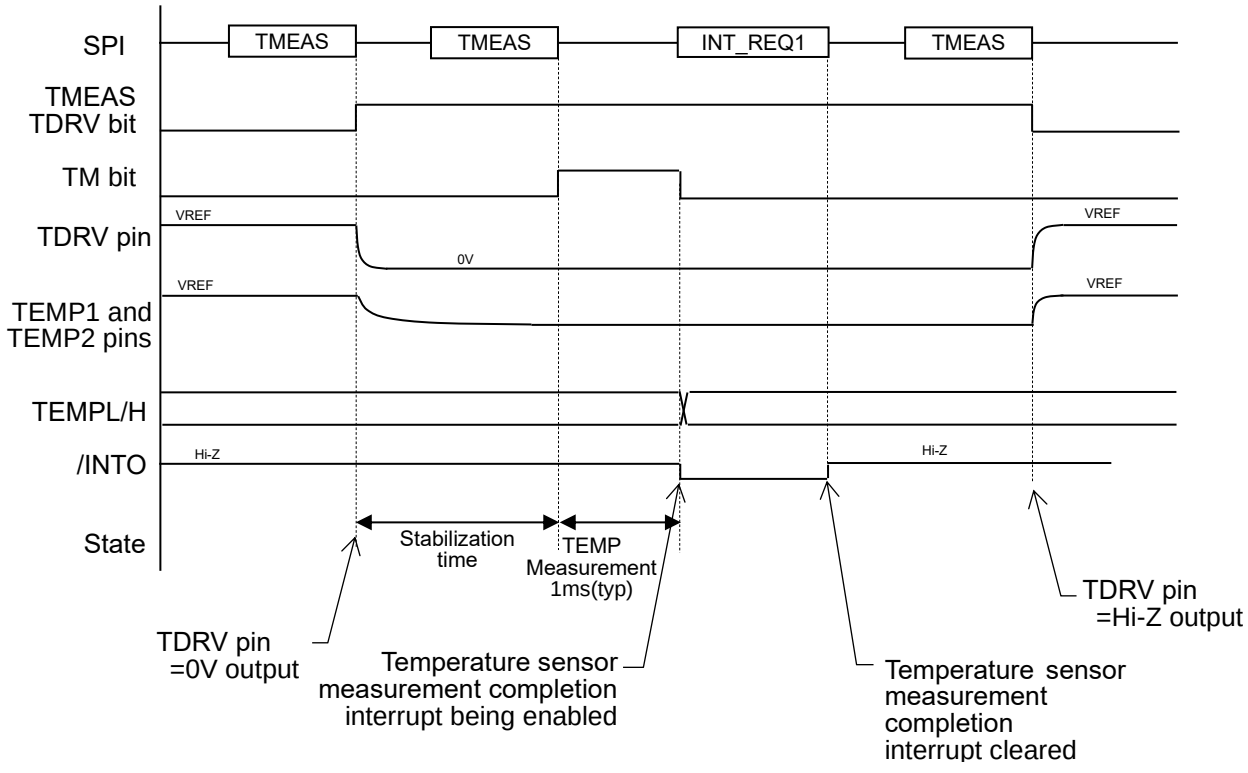


Example of TEMP input level versus temperature



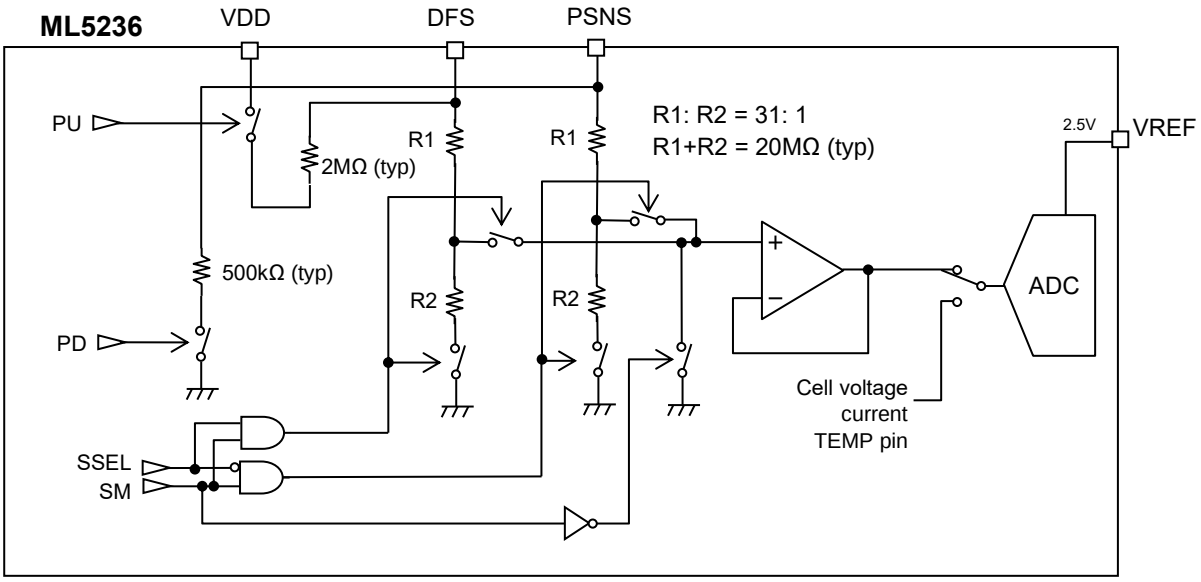
The TMEAS register configures temperature sensor measurement conditions. For details, see the TMEAS register section.
Assert 0V on the TDRV pin and wait until the TEMP1 or TEMP2 pin input level stabilizes before starting measurement. After temperature sensor measurement is completed, asserting the TDRV pin to the Hi-Z state is recommended for reducing current consumption and minimizing VREF output voltage drop.
The following timing diagram shows the temperature sensor measurement operation.

Temperature sensor measurement timing diagram



- PSNS and DFS Voltage Measurement

The PSNS or DFS input level is divided to the 1/32-fold and is measured with the A/D converter. Below is the regarding voltage measurement circuit.

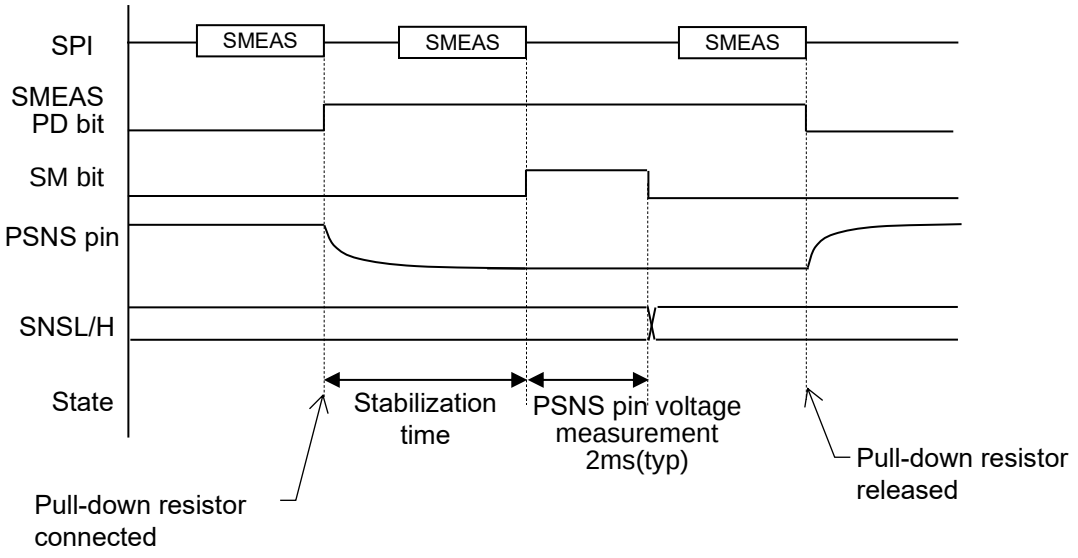


The SMEAS register configures the PSNS and DFS input voltage measurement conditions. For details, see the SMEAS register section.

Writing data "1" to the SM bit of the SMEAS register the 1/32-voltage dividing resistor is connected to the PSNS or DFS pin and A/D conversion is performed after internal voltage stabilization time of about 1ms. If you connect a pull-down or pull-up resistor to the PSNS or DFS pin, set the PD bit/PU bit to "1" first, then wait until the PSNS or DFS pin input voltage stabilizes before writing data "1" to the SM bit to start voltage measurement. After measurement is finished, release the pull-down/pull-up resistor by configuring the PD/PU bits, otherwise it continues to be connected.

The following timing diagram shows the PSNS pin voltage measurement sequence when the PSNS pin is pulled-down.

PSNS pin voltage measurement timing diagram



- Power-save Function

The ML5236 is equipped with the power-save function, which reduces current consumption by halting cell voltage measurement circuits and others.
The PSV bit of the POWER register controls transition to/from the power-save state.
Write data "1" to the PSV bit of the POWER register to transition to the power-save state.
If the PSV bit is "1" during measurement on cell voltages or others, the measurement in progress is canceled and transitions to the power-save state. In this case, invalid values may be saved to the measurement result registers, wait until all measurements are completed before transitioning to the power-save state.

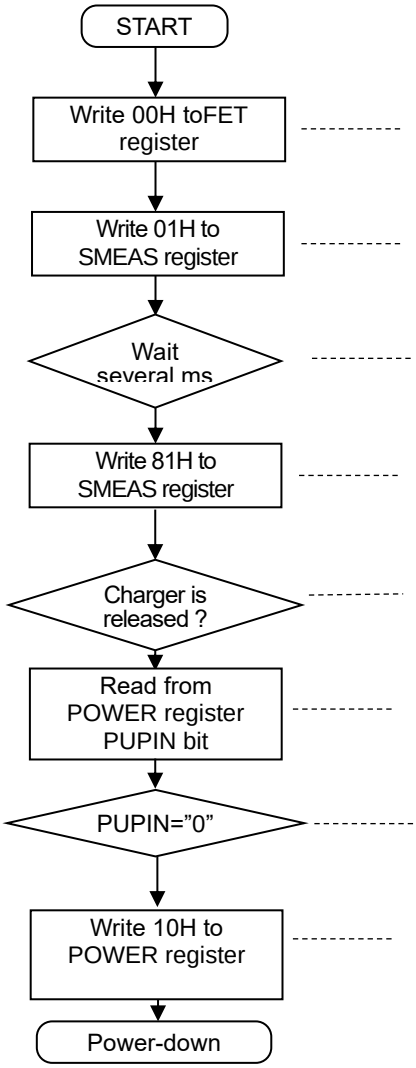
The following table shows the operation state of each function during the power-save state.

Function	Operation state during power-save
VREG pin output	Outputs 3.3V (typ) as the normal state.
VREF pin output	Outputs 2.5V (typ) as the normal state.
MCU serial interface	Can normally read/write registers as the normal state, but the measurement and cell balance configurations are ignored.
Cell voltage measurement	Halted.
Pack current measurement	Halted.
Temperature sensor measurement	Halted.
PSNS and DFS voltage measurement	Halted.
Cell balancing	Halted.
Short circuit detection	Operates as the normal state.
Charge/discharge control FET driver	Operating frequency of the charge pump circuit is reduced to 1/4 of the normal state.
Overvoltage detection	Operates at the defined interval time.
Watchdog timer	Halted.
Internal clock halt detection circuit	Operates as the normal state .

Write data "0" to the PSV bit of the POWER register to recover from the power-save state and start the measurement circuits . Various measurements should be conducted after 1ms (max) operation stabilization time.

- Power-down Function

The ML5236 is equipped with the power-down function, which halts all circuits to reduce the current consumption to zero. Write data "1" to the PDWN bit of the POWER register to transition to the power-down state.
Below is an example of the control flow for transitioning to the power-down state.



Charge/discharge FETs are turned off.

The PSNS pin is pulled-down with a 500kΩ (typ) resistor to monitor release of the charger .

Wait until the PSNS pin voltage stabilizes.

The PSNS pin voltage is measured to confirm that the charger is released.

The SNSL and SNSH registers are evaluated to confirm the PSNS pin level to be lower than 1/2 VDD. If it is higher than 1/2 VDD, the device is powered-up again immediately after transitioning to the power-down state. Wait until the PSNS pin voltage becomes lower than 1/2 VDD.

Check the PUPIN bit to confirm that the /PUPIN pin level is "H"

If the PUPIN bit is "1", the device is powered-up again immediately after transitioning to the power-down state. Wait until the PUPIN bit becomes "0".

Write data "1" to the PDWN bit to transition to the power-down state. All circuits are halted and all registers are initialized.
PSNS is internally pulled-down with a 500kΩ (typ) resistor and presence of a charger is monitored.

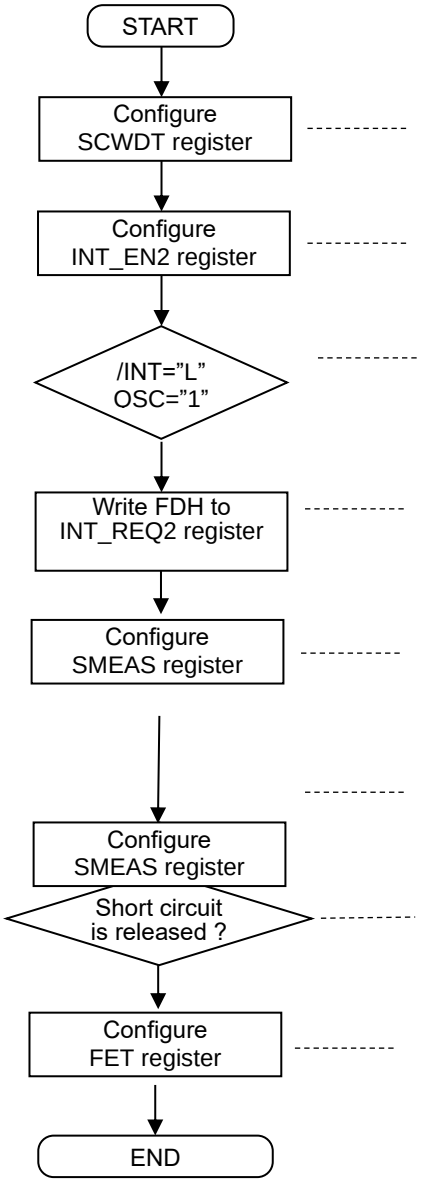
The following table shows the output level on each pin in the power-down state.

Pin name	Output level during power-down
VREG	0V
VREF	0V
/INTO	Hi-Z
SDO	Hi-Z
C_FET	Equals to the CFS level
D_FET	Equals to the DFS level
CDLY	0V

The power-down state is cleared if a charger is detected through the PSNS pin, or if the "L" level is asserted on the /PUPIN pin.
At recovery from the power-down state, the initial configurations should be made after the VREG and VREF outputs have risen.

- Short Circuit Detection Function

The ML5236 is equipped with the short circuit detection function, which autonomously turns off the charge/discharge FETs when a short circuit condition is detected. The SCWDT register configures the short circuit conditions. For details, see the SCWDT register section.
Below is an example of short circuit detection configurations and the system control flow.



Configure the short circuit detection threshold with the SC0 and SC1 bits, and set the ENSC bit to "1" to start short circuit monitor.

Set the ESC bit to "1" to enable the short circuit detection interrupt.

If the "L" level is asserted on the /INTO pin, read the INT_REQ2 register to confirm the requested interrupt. (QSC is assumed here.)

Write "0" to the QSC bit to clear the interrupt request.

Set the PU bit of the SMEAS register to "1" to pull-up the DFS pin.
If the short circuit state is continued, the DFS pin level remains to be the GND level. Otherwise, it is brought up to a level close to VDD by the pull-up resistor.

To measure the DFS pin voltage, set the SSEL and SM bits of the SMEAS register to "1".

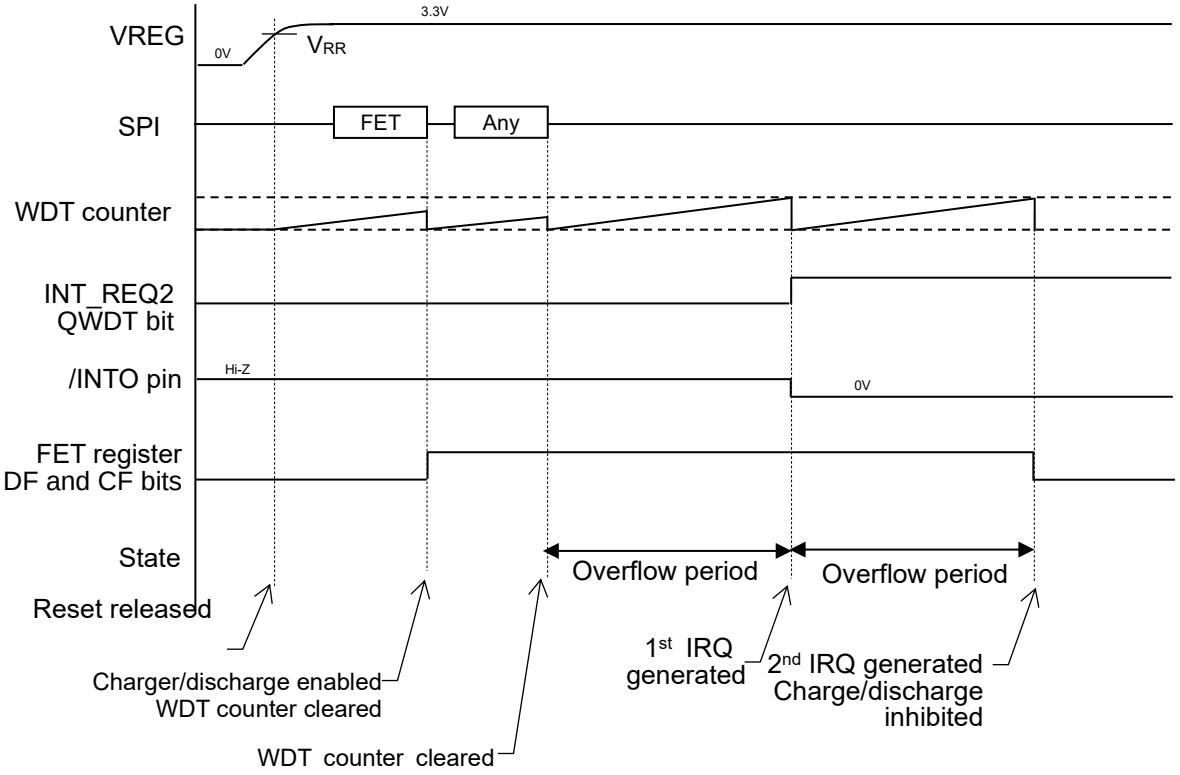
Read the SNSL and SNSH registers to confirm that the DFS pin level is close to VDD. If the DFS pin level is GND, it means that the short circuit state is continued. Wait until the DFS pin level reaches VDD.

If the cell voltages are in the normal range, set the DF and CF bits of the FET register to "1" to enable charge/discharge.

- Watchdog Timer Function

The ML5236 is equipped with the watchdog timer function, which triggers an alarm when writing/reading data to/from the control register is not executed for a specific time period. The SCWDT register configures the watchdog timer conditions. For details, see the SCWDT register section.
Below is an example of the watchdog timer operation.

Example of watchdog timer operation



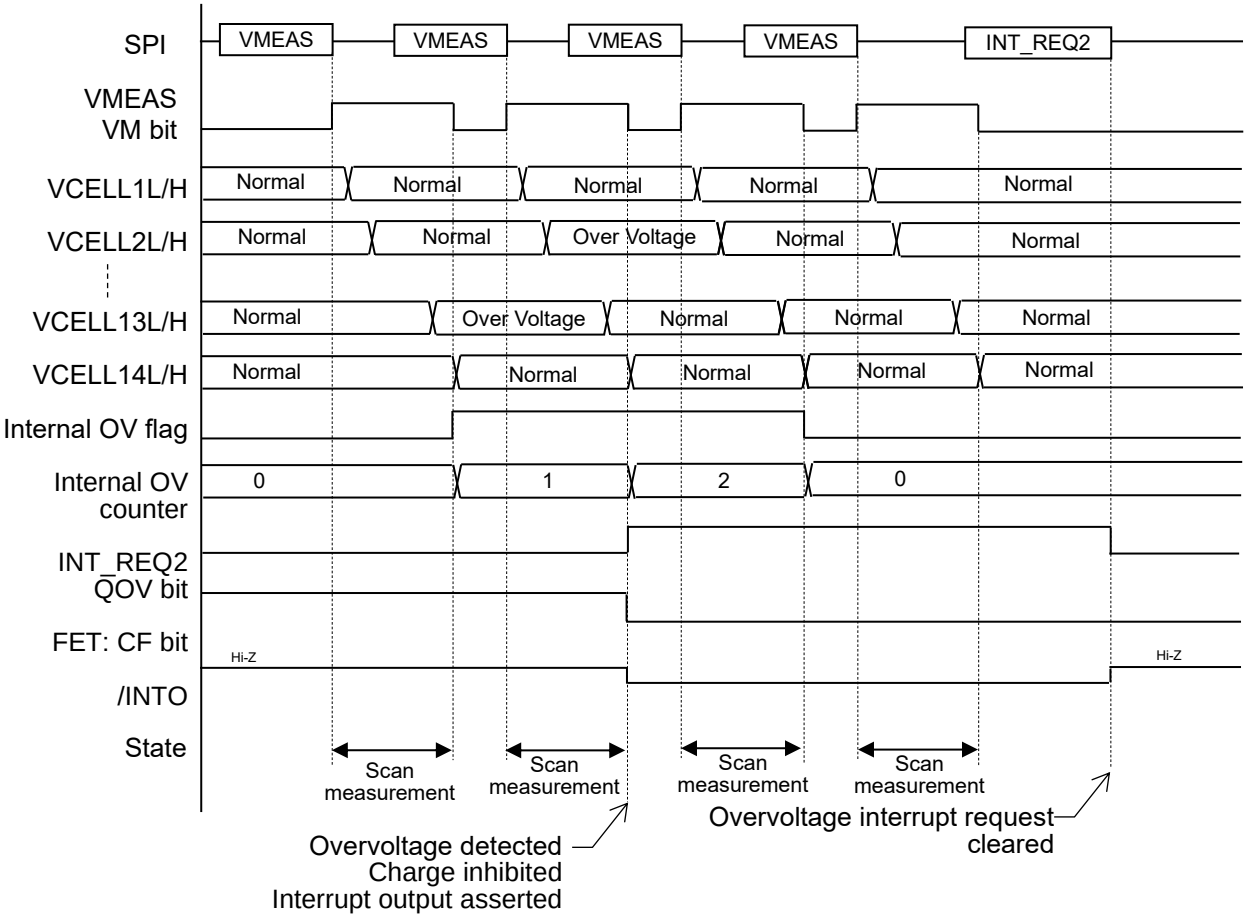
If writing/reading data to the control register is not performed for longer than the overflow period, the QWDT bit of the INT_REQ2 register is set to "1", and the "L" level is asserted on the /INTO pin. If a CRC error occurs during the CRC mode, the watchdog timer counter is not cleared.
If the overflow is detected twice consecutively, the DF and CF bits of the FET register are automatically set to "0" to disable charge/discharge. Since these bits will not be reset automatically after recovery to the normal state, they should be reconfigured using the external MCU.

- Overvoltage Detection Function

The ML5236 is equipped with the overvoltage detection function, which compares the register values of cell voltage measurement results with the overvoltage threshold value defined in the OVDETL/H register to monitor overvoltage.
The SETOV and OVDETL/H registers configure the overvoltage detection conditions. For details, refer to the SETOV and OVDETL/H registers.

The following timing diagram shows the overvoltage monitor in the normal state with the number of consecutive overvoltage detection delays in scan measurements being 2.

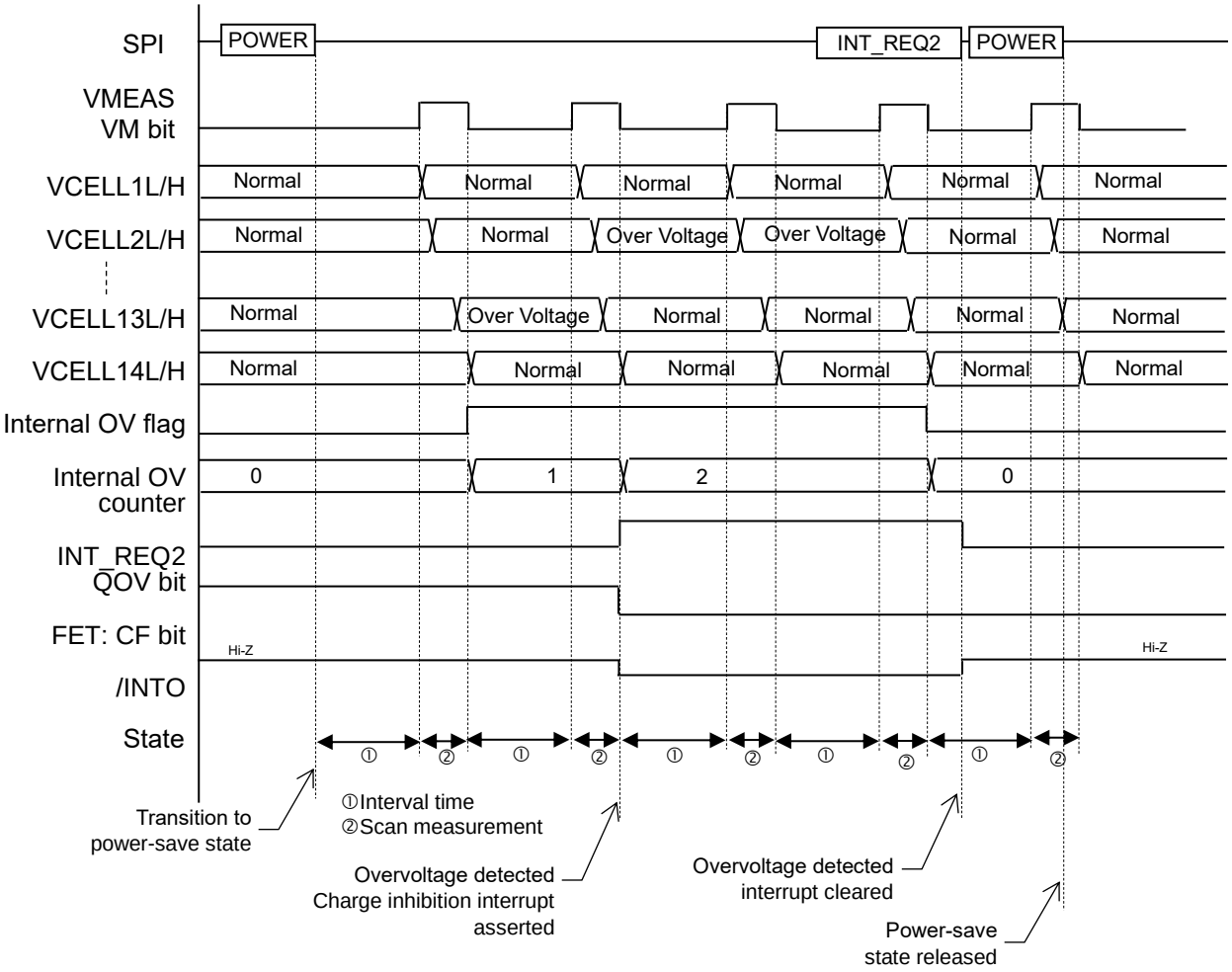
Overvoltage detection timing diagram (normal state, number of detection delays in scan measurement = 2)



If any one VCELLnL/H register value is greater than the OVDETL/H register value on completion of each scan measurement, the internal OV flag is set, and the internal OV counter for detection delays is incremented.
If an overvoltage condition is detected on a different cell at the next scan measurement, the internal OV flag is maintained and the OV counter is incremented.
If the number of overcharge detection delay threshold defined in the CN0 to CN2 bits of the SETOV register is equal to the OV counter value, the QOV bit of the INT_REQ2 register and the OV bit of the STATUS register are set to “1”, and the CF bit of the FET register is reset to “0” for charge inhibition.
Since the CF bit of the FET register is not automatically set to “1” after recovery to the normal state, they should be reconfigured to turn-on condition using the external MCU.

While in the power-save state, all the cells from Cell 1 to Cell 14 are scanned for voltage measurement automatically at the interval time specified in the SLT0 and SLT1 bits of SETOV register. Since unused cells are scanned, tie the corresponding cell monitor pins to GND. The following timing diagram shows the overvoltage monitor operation in the power-save state.

Overvoltage detection timing diagram (power-save state, number of detection delays in scan measurement = 2)



If a scan measurement is in progress when the PSV bit of POWER register is set to "0" to recover from the power-save to the normal state, the scan in progress continues until the last cell is scanned. Therefore, after the restoration from the power-save to the normal state, make sure that the VM bit of the VMEAS register is not "1".

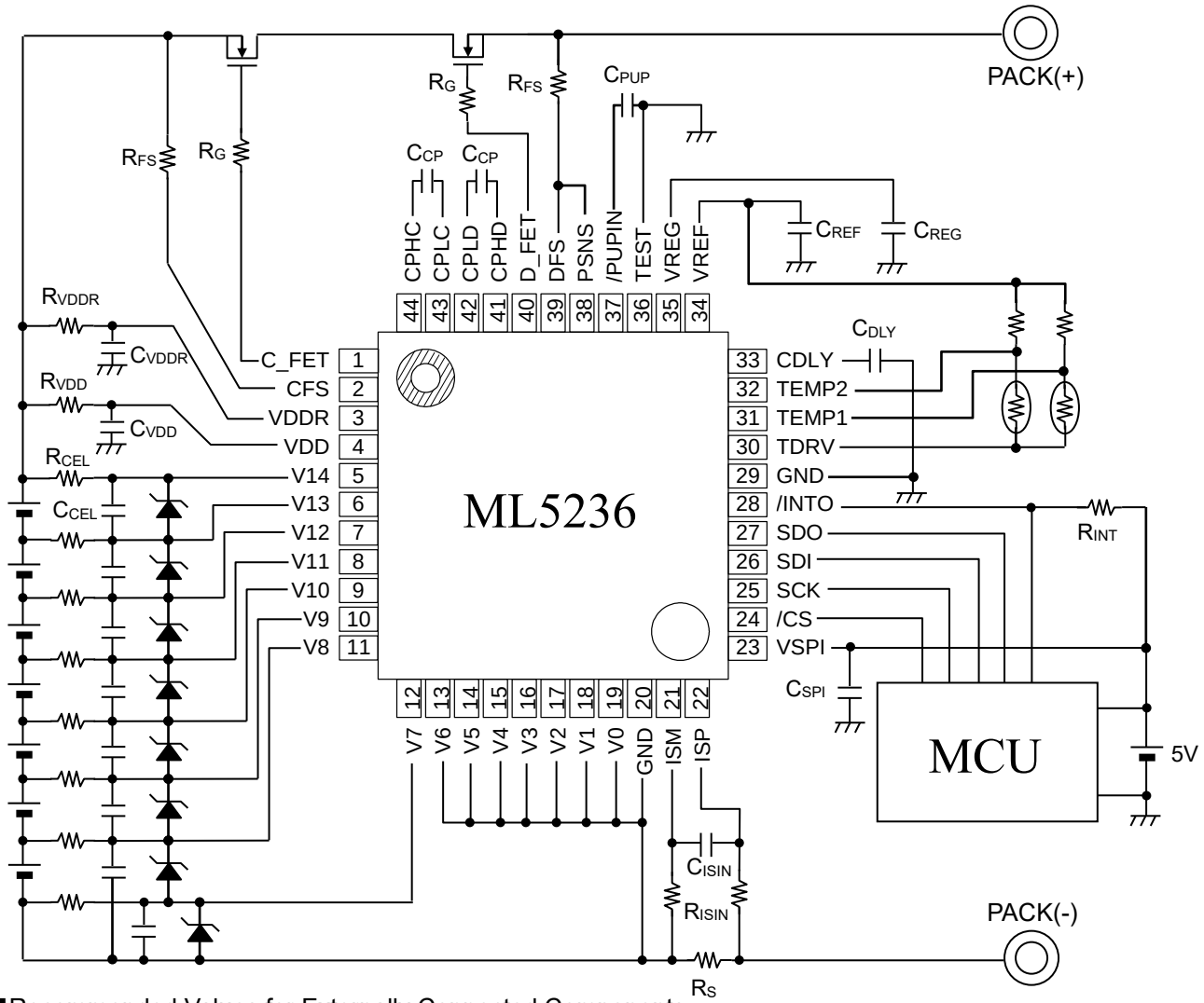
The scan measurement completion interrupt flag will be set during the power-save state. Reset the EVM bit of the INT_EN1 register to "0" before transitioning to the power-save state to disable the cell voltage measurement completion interrupt request.

- Interrupt Output Function

Interrupt signal is asserted on the /INTO pin to notify the external MCU at the completed measurements and error detections.
The INT_EN1 and INT_EN2 registers enables various interrupt outputs, while the INT_REQ1 and INT_REQ2 registers are read/written to check and clear generated interrupt requests.
The following table shows interrupt requests, generation conditions, and states after generation.

Interrupt request	Interrupt generation condition	State after interrupt
Cell voltage measurement completion	The VM bit of the VMEAS register is set to “1”, subsequently the cell voltage measurement is completed.	The measurement result is stored in the VCELLnL/H register.
Current measurement completion	The IM bit of the IMEAS register is set to “1”, subsequently the current measurement is completed.	The measurement result is stored in the CURL/H register.
Temperature sensor measurement completion	The TM bit of the TMEAS register is set to “1”, subsequently the temperature sensor measurement is completed.	The measurement result is stored in the TEMPnL/H register.
Overvoltage detection	The count of the VCELLnL/H register value exceeding the OVDETL/H register threshold on completion of each scan, reaches the detection delays in scan measurement specified in the CN0 to CN3 bits of the SETOV register.	The CF bit of the FET register is automatically reset to “0”.
Short circuit detection	The ISP-to-ISM level is larger than the threshold specified in the SC0 and SC1 bits of the SCWDT register, and the CDLY pin level reaches the predefined threshold.	The DF and CF bits of the FET register are automatically reset to “0”.
CRC error	The received CRC code does not match the calculation result.	The received SPI communication data is disabled.
Internal clock halt detection	Internally generated clock is not supplied for a specific time period.	The CF and DF bits of the FET register are automatically reset to “0”. Measurement functions do not operate normally.
WDT overflow detection	Writing/reading operation to/from the control register is not executed for longer than the overflow period defined in the WDT0 and WDT1 bits of the WDT register.	The ”L” level is asserted on the /INTO pin.
	Overflow is detected twice consecutively.	The DF and CF bits of the FET register are automatically reset to “0”.

■ Application Circuit Example 1 (7-Cell and MCU Power Supply = External 5V)



■Recommended Values for Externally Connected Components

Component	Recommended value
R_{VDD} (*1)	510Ω to 1.5kΩ
C_{VDD}	2.2μF to 10μF
R_{VDDR}	100Ω
C_{VDDR}	2.2μF to 10μF
R_{CEL}	150Ω to 10kΩ
C_{CEL}	0.1μF to 10μF
R_S	1mΩ

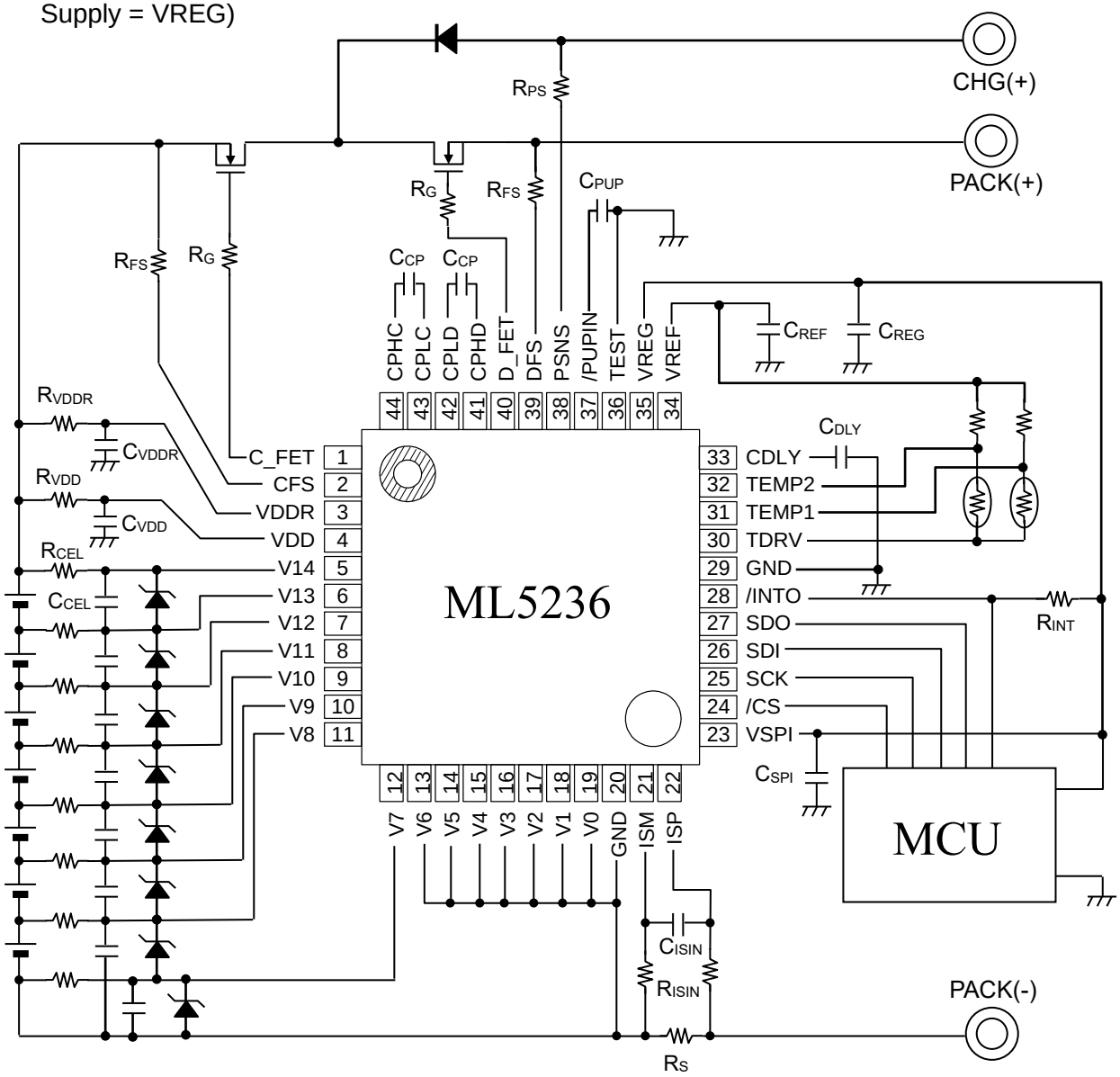
Component	Recommended value
R_{ISIN}	1kΩ
C_{ISIN}	0.1μF
C_{REG}, C_{REF}	4.7μF
R_{INT}	51kΩ
C_{SPI}	0.1μF
C_{DLY}	1nF to 10nF
C_{PUP}	0.1μF

Component	Recommended value
R_G	1kΩ
R_{FS}	1kΩ
C_{CP}	20nF (*2)

(*1) Recommend R_{VDD}=1.5kΩ for C_{VDD}=2.2 μF.
(*2) 10nF gate capacitance of the external Nch-FET is assumed.
(*3) In order to prevent the voltage of the Vn pin, which is connected to the lowest cell's negative pin, from dropping below GND level, the capacitor C_{CEL} should be connected between the lowest cell's positive pin and the GND.

Notice: Example of application circuit and the recommended values to parts list shall not guarantee performance under all conditions. Full and detailed tests are suggested on your actual application. e.

■ Application Circuit Example 2 (7-Cell, Isolated Charge/Discharge Path, and MCU Power Supply = VREG)



■Recommended Values for External Components

Component	Recommended value
R_{VDD} (*1)	510Ω to 1.5kΩ
C_{VDD}	2.2μF to 10μF
R_{VDDR}	100Ω
C_{VDDR}	2.2μF to 10μF
R_{CEL}	150Ω to 10kΩ
C_{CEL}	0.1μF to 10μF
R_S	1mΩ

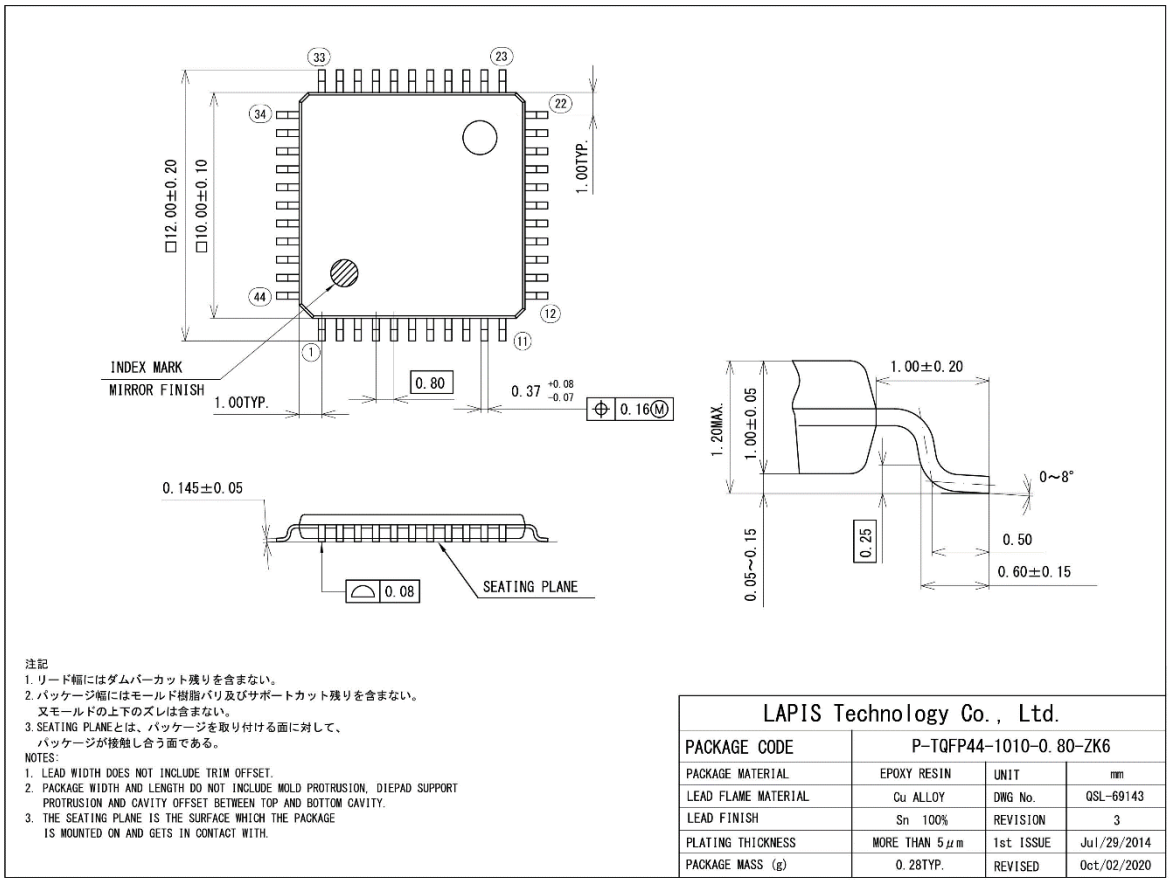
Component	Recommended value
R_{ISIN}	1kΩ
C_{ISIN}	0.1μF
C_{REG}, C_{REF}	4.7μF
R_{INT}	51kΩ
C_{SPI}	0.1μF
C_{DLY}	1nF to 10nF
C_{PUP}	0.1μF

Component	Recommended value
R_G	1kΩ
R_{FS}	1kΩ
C_{CP}	20nF (*2)

(*1) Recommend R_{VDD}=1.5kΩ for C_{VDD}=2.2 μF.
(*2) 10nF gate capacitance of the external Nch-FET is assumed.
(*3) In order to prevent the voltage of the Vn pin, which is connected to the lowest cell's negative pin, from dropping below GND level, the capacitor C_{CEL} should be connected between the lowest cell's positive pin and GND.

Notice: Example of application circuit and the recommended values to parts list shall not guarantee performance under all conditions. Full and detailed tests are recommended on your actual applications.

■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP44-1010-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69143
LEAD FINISH	Sn 100%	REVISION	3
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.28TYP.	REVISED	Oct/02/2020

Causion regarding surface mount type packages

Surface mount type packages are susceptible to applied heat in solder reflow or moisture absorption during storage. Please contact your local ROHM sales representative for the recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

■ Revision History

Document No.	Issue date	Page		Descriptions
		Previous	New	
FEDL5236-01	2014.09.02	—	—	First edition issued
FEDL5236-02	2015.06.26	—	36	Add it is recommended to measure the current amplification gain G_{IM} values to this page.
FEDL5236-03	2015.12.03	12,13	12,13	MCU interface: the SCK clock edge is corrected
		34	34	Power-on/Power-off Sequence: pin name is corrected.
FEDL5236-04	2016.03.25	46,47	46,47	Application Circuit example; capacitor connection of lowest cell is modified.
FEDL5236-05	2016.07.12	3	3	Pin Description corrected
		32	32	Table of Cell connection table and Handling of unused pin is corrected.
FEDL5236-06	2018.06.07	5	5	Absolute Maximum rating: Output voltage V_{out3}, short circuit output current I_{OS} is applied to CDLY pin.
FEDL5236-07	2019.11.21	10	10	Short current detection timing diagram: Error correction of C_FET, D_FET.
FEDL5236-08	2020.12.1	-	-	Changed Company name
		50	50	Changed “Notes”
FEDL5236-09	2022.05.09	12	12	MCU Interface: Added restrictions when applying external voltage to VSPI pin.
FEDL5236-10	Jan. 9, 2024	1	1	Add Application Part number, Delete notes
		49	49	Add Notes

Notes

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