Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5241

5 series Cell Li-ion Rechargeable Battery Protection IC

■ General Description

The ML5241 is a protection IC for the 3- to 5-cell Li-ion rechargeable battery pack. It detects individual cell overvoltage and battery cell open-wire, and alerts by alarm output signal. And the ML5241 has a SLEEP pin to reduce and minimize current consumption.

■ Features

- 3 to 5 cell high precision overvoltage detection function
  Overvoltage detection threshold and detection accuracy : 4.225V±25mV (0 °C to 60 °C)
  Overvoltage detection delay time : 2 sec(typ)

- Open-wire detection function
  Open-wire detection voltage : 0.6V(typ)
  Open-wire detection sink current : 100nA(typ)
  Open-wire detection delay time : 3.2sec(typ)

- Sleep function
  Set the SLEEP pin “H” and stop all functions for low power consumption.

- 3 types of alarm output
  Selected from CMOS / Nch open drain / Pch open drain

- Setting number of connected battery cells : defined with part-number
  5 cells = ML5241-001, 4 cells =ML5241-001A, 3 cells=ML5241-001B

- Low current consumption
  Operating : 1μA(typ), 2μA(max）(0°C to 60°C)
  Sleep mode : 0.1μA(typ), 0.4μA(max) (-20°C to 85°C)

- Power supply voltage : +5V to +25V

- Operating temperature : -20°C to +85°C

- Package : 10 pin WSON

■ Application

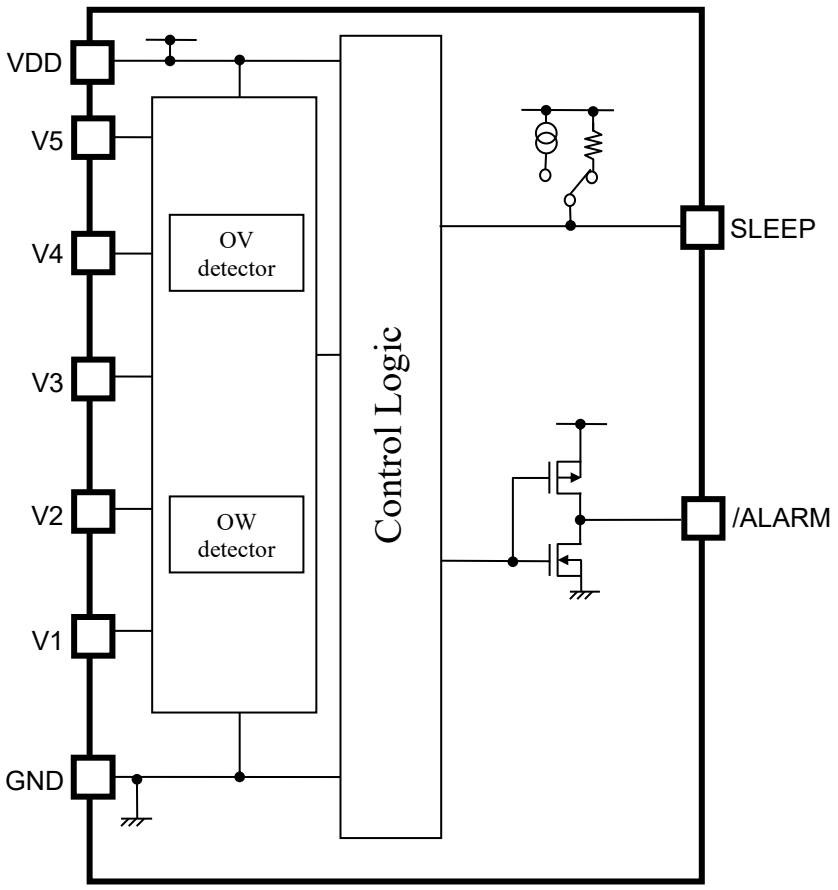
・Power tools and Garden tools
・Cordless Cleaner

■ Part number

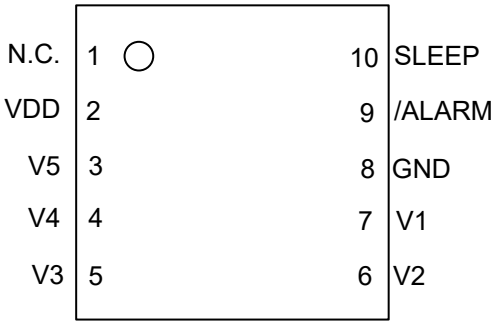
ML5241-001MD 5 cells, CMOS output

ROHM SEMICONDUCTOR

■ Block Diagram



■ Pin Configuration (top view)



■ Pin Description

Pin No.	Pin	I/O	Description
2	VDD	—	Power supply input pin.
3	V5	I	Battery cell 5 high voltage input pin
4	V4	I	Battery cell 5 low voltage input and Battery cell 4 high voltage input pin.
5	V3	I	Battery cell 4 low voltage input and Battery cell 3 high voltage input pin.
6	V2	I	Battery cell 3 low voltage input and Battery cell 2 high voltage input pin. Should be connected to GND for the 3 cell series connected battery pack application.
7	V1	I	Battery cell 2 low voltage input and Battery cell 1 high voltage input pin. Should be connected to GND for the 3 or 4 cell series connected battery pack application.
8	GND	—	Ground pin.
9	/ALARM	O	Alarm signal output pin. ・If CMOS output : Output level is ”L” level(GND level) if overvoltage/ open-wire is detected, else ”H” level (VDD power supply level). ・If Nch open drain output : Output level is ”L” level(GND level) if overvoltage/ open-wire is detected, else ”Hi-Z” level. ・If Pch open drain output： Output level is ”H”level (VDD power supply level) if overvoltage/open-wire is detected, else ”Hi-Z” level.
10	SLEEP	I	Sleep control input pin. For setting the sleep status, input Hi-Z level, else input GND level. In sleep status, pulled-up with 500kΩ(typ) resisitor. In operating status, pulled up with 0.1μA(typ) constant current.
1	N.C.	—	No connect. Leave them electrically unconnected.

■ Absolute Maximum Ratings

（GND= 0 V, Ta = 25 °C）

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Applied to VDD pin	−0.3 to +33	V
Input Voltage	V_{IN}	Applied to V5 to V1 and SLEEP pins	−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	Applied to /ALARM pin	−0.3 to V_{DD}+0.3	V
Short-circuit output current	I_{OS}	Applied to /ALARM pin	10	mA
Power dissipation	P_D	—	690	mW
Storage temperature	T_{STG}	—	−55 to +150	°C

■ Recommended Operating Conditions

（GND= 0 V）

Item	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	5 to 25	V
Operating temperature	T_{OP}	—	-20 to +85	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD}=5 to 25V, GND=0 V, Ta=-20 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
V5 to V1 pins Input leakage current	I_{VCL}	Each cell voltage = 3.6V SLEEP pin = “H”	-1	—	1	μA
/ALARM pin “H” output voltage	I_{OHA}	I_{OH} = -100μA	V_{DD}-0.2	—	V_{DD}	V
/ALARM pin “L” output voltage	V_{OLA}	I_{OL} = 100μA	0	—	0.2	V
/ALARM pin Output leakage current	I_{OLKA}	Output state is Hi-Z	-2	—	2	μA
SLEEP pin "H" input voltage	V_{IH2}	—	0.8 × V_{DD}	—	V_{DD}	
SLEEP pin "L" input voltage	V_{IL2}	—	0	—	0.2 × V_{DD}	
SLEEP pin "H" input current	I_{IH2}	V_{IH} = V_{DD}	—	—	2	μA
SLEEP pin "L" input current	I_{IL2}	V_{DD} = 18V, V_{IL} = GND	–300	–100	–20	nA
SLEEP pin Pull-up resistor	R_{SLP}	—	200	500	1000	kΩ

● Supply Current Characteristics

V_{DD}=5 to 25V, GND=0 V, Ta=-20 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation	I_{DD}	Each cell voltage=3.6V No output load Ta=0 to 60°C	—	1	2	μA
	I_{DDT}	Each cell voltage=3.6V No output load Ta=-20 to 85°C	—	1	3	μA
Current consumption in sleep mode	I_{DDS}	Each cell voltage=3.6V No output load Ta=-20 to 85°C	—	0.1	0.4	μA

(Note) VDD pin current consumption. V5 to V1 pin input current, /ALARM pin output current is not included.

● Code 001: Detection Threshold Chracteristics（Ta=0°C to 60°C）

V_{DD}=18V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.200	4.225	4.250	V
Overvoltage release threshold	V_{OVR}	—	3.975	4.025	4.075	V
Open-wire detection / release threshold	V_{OW}	—	0.5	0.6	0.7	V
Open-wire detection sink current	I_{OW}	—	50	150	300	nA
Quick test mode transition/release VDD-V5 pin voltage difference	V_{TST}	Ta=25°C	3	—	10	V

● Code 001: Detection delay time characteristtics（Ta=0°C to 60°C）

V_{DD}=18V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage/open-wire detection cycle	t_{OV}	—	300)	400	500	ms
Overvoltage detection delay time	t_{DOV}	Defined with detection cycle	5	—	6	cycle
Open-wire detection/release delay time	t_{DOW}	Defined with detection cycle	8	—	9	cycle
Quick test mode Overvoltage/open-wire detection cycle	t_{OVW}	Ta=25°C	75	100	125	ms
Quick test mode Overvoltage detection delay time, open-wire detection/release delay time	t_{DOVW}	Defined with detection cycle	—	—	1	time

■ Functional Description

● Selecting the number of battery cells

Number of battery cells is determined by part number.
5-cells=ML5241-001, 4-cells=ML5241-001A, 3-cells=ML5241-001B

● /ALARM output pin

/ALARM pin output status for overvoltage/open-wire detected state.

	/ALARM pin output status		
	CMOS Code 001	Nch open drain	Pch open drain
Overvoltage/open-wire detected state	"L" level	"L" level	"H" level
Undetected state	"H" level	"Hi-Z" level	"Hi-Z" level

● Handling VDD pin and V1 to V5 pins

Since the VDD pin is the power supply input, put a noise elimination RC filter in front of the VDD input for stabilization. The resistor value of this noise filter should be adjusted so that the voltage drop across the resistor is smaller than 0.3 V.

The V1 to V5 pins are the monitor pins for individual cell voltages. Put a noise elimination RC filter in front of each battery cell to prevent false detection.

● Unused pin Treatment

The followtin table shows how to handle unused pins

Unused pins	Recommended treatment
V1 , V2	Connected to GND pin
SLEEP	Connected to GND pin

● Power-on/Power-off sequence

Battery cells can be connected in any order, but it is recommend that the lowest voltage cell is connected first, and then connection continues from lower to higher voltage cells, and the highest voltage cell is connected last. There are no restrictions on the power supply voltage rise time at power-on, and power-off sequence or power supply voltage fall time at power-off.

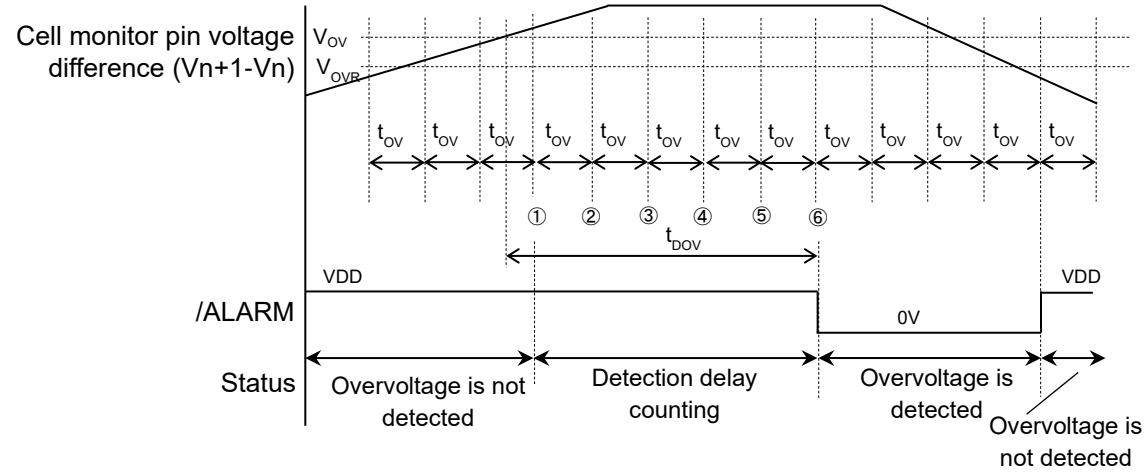
It may transition to the open-wire or overvoltage detection state if it takes long time to connect all cells.

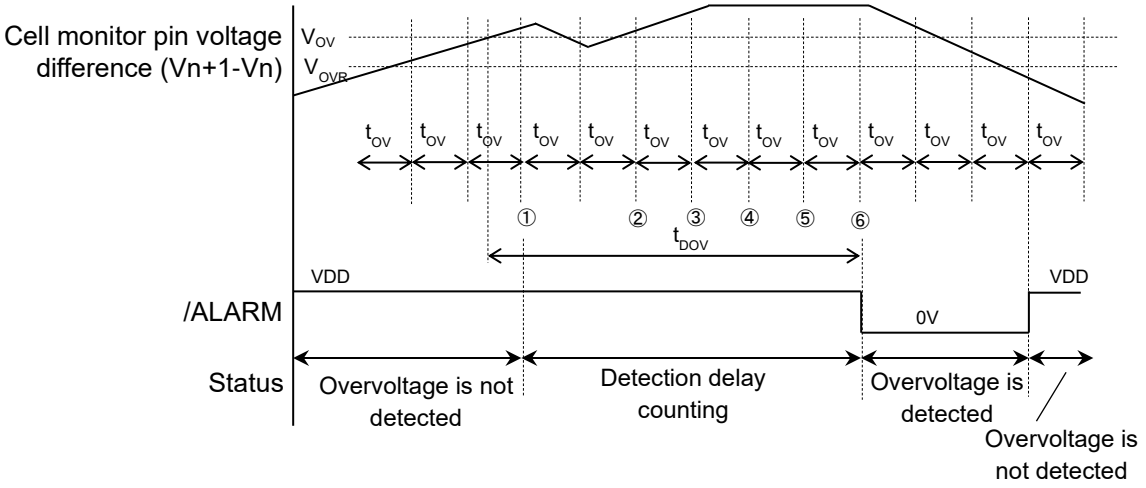
● Overvoltage detection function

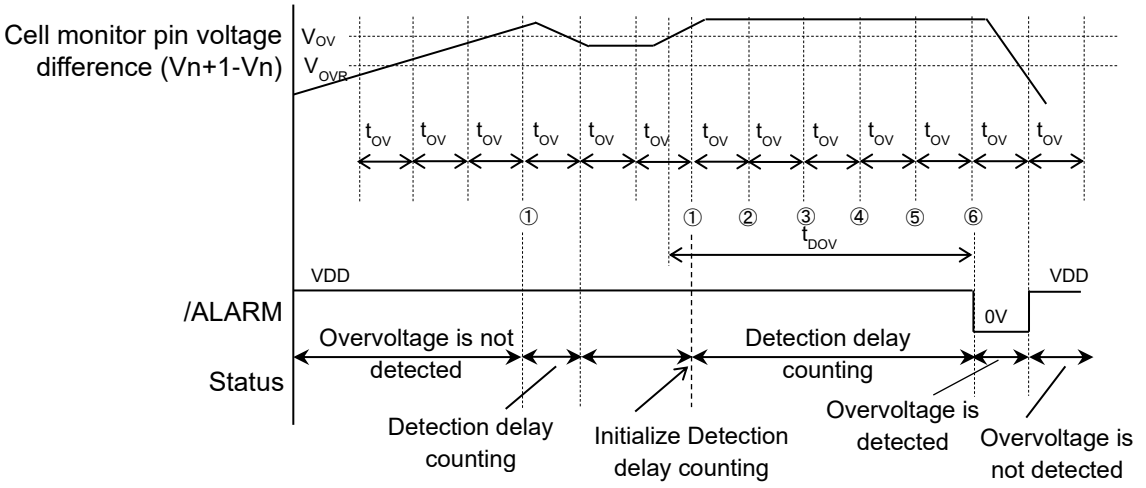
After power-on, overvoltage detection is started with cycle of 400ms(typ) (overvoltage detection cycle t_{OV}). When any one or more battery cell voltages reach or exceed the overvoltage detection threshold V_{OV} for series six times, it detects overvoltage state. And if /ALARM pin output type is CMOS output, /ALARM pin output changes from "H" level to "L" level.

If the state in which cell voltage of all cell is lower than overvoltage detection threshold V_{OV} is detected for series two times, detection delay time counting is initialized.

After the overvoltage detection, if the cell voltage of all cell is lower than overvoltage relase threshold V_{OVR} , and if /ALARM pin output type is CMOS output, /ALARM pin output changes from "L" level to "H" level.







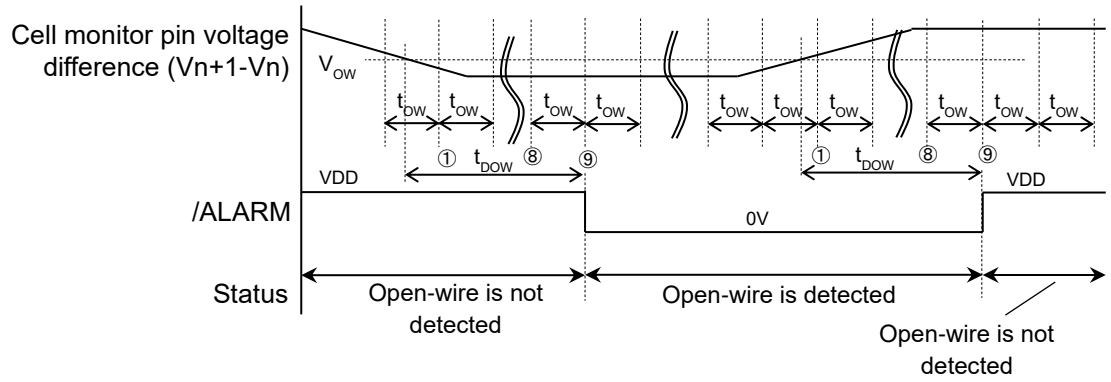
● Open-wire detection function

After power-on, open-wire detection is started with cycle of 400ms(typ) (open-wire detection cycle t_{OW}). When any one or more battery cell voltages reach or below the open-wire detection threshold V_{OW} for series nine times. It detects open-weire state. And if /ALARM output type is CMOS output, /ALARM pin output changes from “H” level to “L” level.

If the state in which voltage of all cell is higher than open-wire detection threshold V_{OW} is detected for once, detection delay time counting is initialized.

After the open-wire detection, if the state in which cell voltage of all cell is higher than open-wire detection threshold V_{OW} is detected for series nine times, and if /ALARM output type is CMOS output, /ALARM pin output changes from “L” level to “H” level.

If the state in which cell voltage of one or more cell is lower than open-wire detection threshold V_{OW} is detected for once, detection delay time counting is initialized.



● Sleep function

Set the SLEEP pin input “H” level and all function is stopped, and ML5241 is in the low power consumtion sleep mode.

In the sleep mode, the SLEEP pin is pulled up with 500kΩ(typ) resistor and the /ALARM pin is in the same state as overvoltage/open-wire detection shown below..

/ALARM pin outpout in sleep mode		
CMOS Code 001	Nch open drain	Pch open drain
“L” level	“L” level	“H” level

If the SLEEP pin is set ”L” level, the ML5241 powe-ups and its state changes from sleep mode to normal operation, and overvoltage and open-wire detection are started. In the normal operation state, 500kΩ(typ) pull-up resistor is disconnected and pulled up with 100nA(typ) current source.

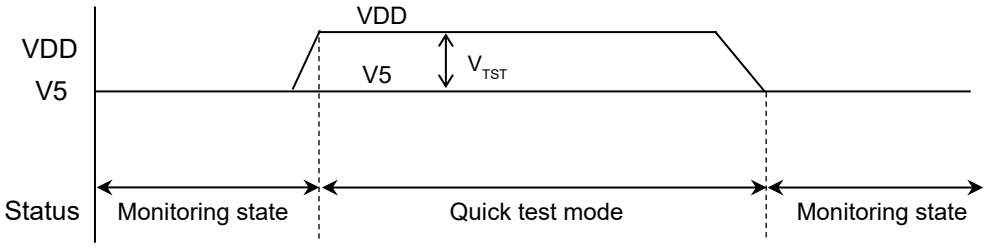
● Quick test mode

In the Quick test mode, overvoltage/open-wire detection cycle time is set 100ms(typ), overvoltage detectin delay time and openwire detection/release delay time are set equal or shorter than one detection cycle.

If the voltage of VDD pin is more than 10V higher than V5 pin, the state change into this quick test mode.

For recovering from quick test mode to normal mode, set the voltage of VDD pin lower than “the voltage of V5 + 3V”.

This test mode can decrease the test time after board mounting.



● Redefinition of overvoltage Detection/Release threshold Range and Step

The overvoltage detection/release thresholds can be redefined as shown in the following table. Since some combinations are unavailable, contact us for details

Detection voltage	Setting range	Step voltage
Overvoltage detection voltage	4.0V to 4.4V	25mV
Overvoltage release voltage	3.8V to 4.2V	25mV

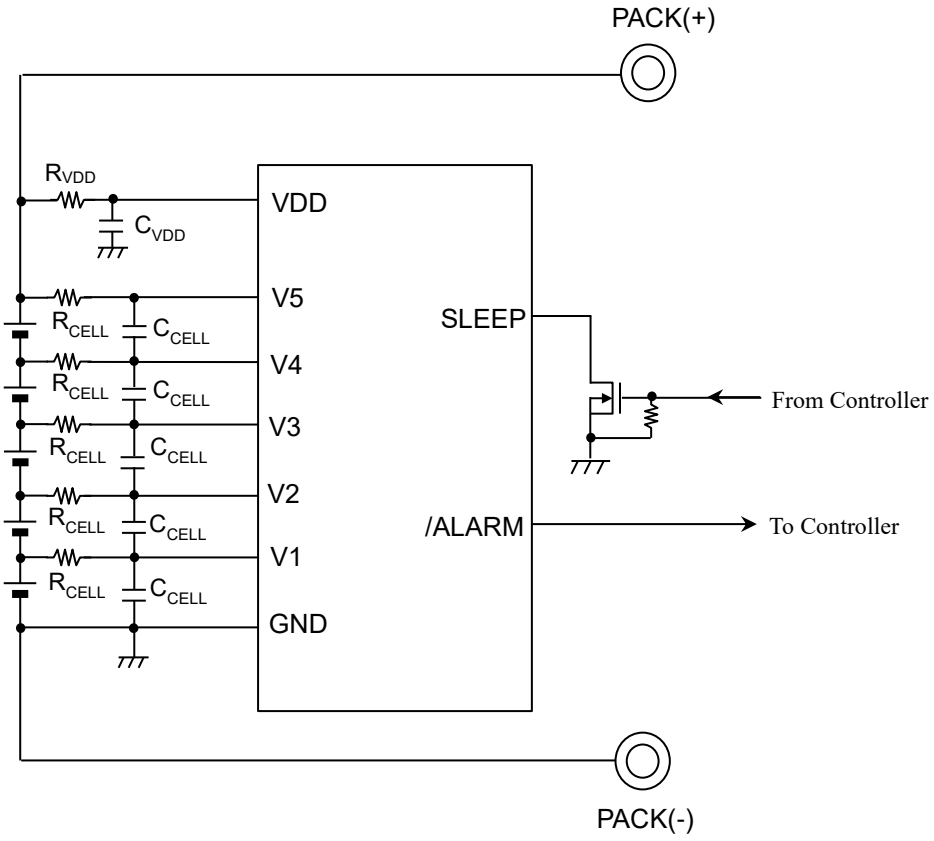
● Redefinition of overvoltage Detection Delay time and open-wire Detection/Relase Delay Time Range

The overvoltrage detection delay time and open-wire detection/release delay time can be redefined as shown in the following table.

Delay time	Settable time (detection cycle time)							Unit
Overvoltage detection delay time	1 to 2	3 to 4	5 to 6	7 to 8	9 to 10	11 to 12	13 to 4	cycle
Open-wire detection/release delay time	1 to 2	3 to 4	5 to 6	7 to 8	9 To 10	11 to 12	13 to 14	cycle

Delay time	Settable time (detection cycle=400ms)							Unit
Overvoltage detection delay time	0.4 to 0.8	1.2 to 1.6	2.0 to 2.4	2.8 to 3.2	3.6 to 4.0	4.4 to 4.8	5.2 to 5.6	sec
Open-wire detection/release delay time	0.4 to 0.8	1.2 to 1.6	2.0 to 2.4	2.8 to 3.2	3.6 to 4.0	4.4 to 4.8	5.2 to 5.6	sec

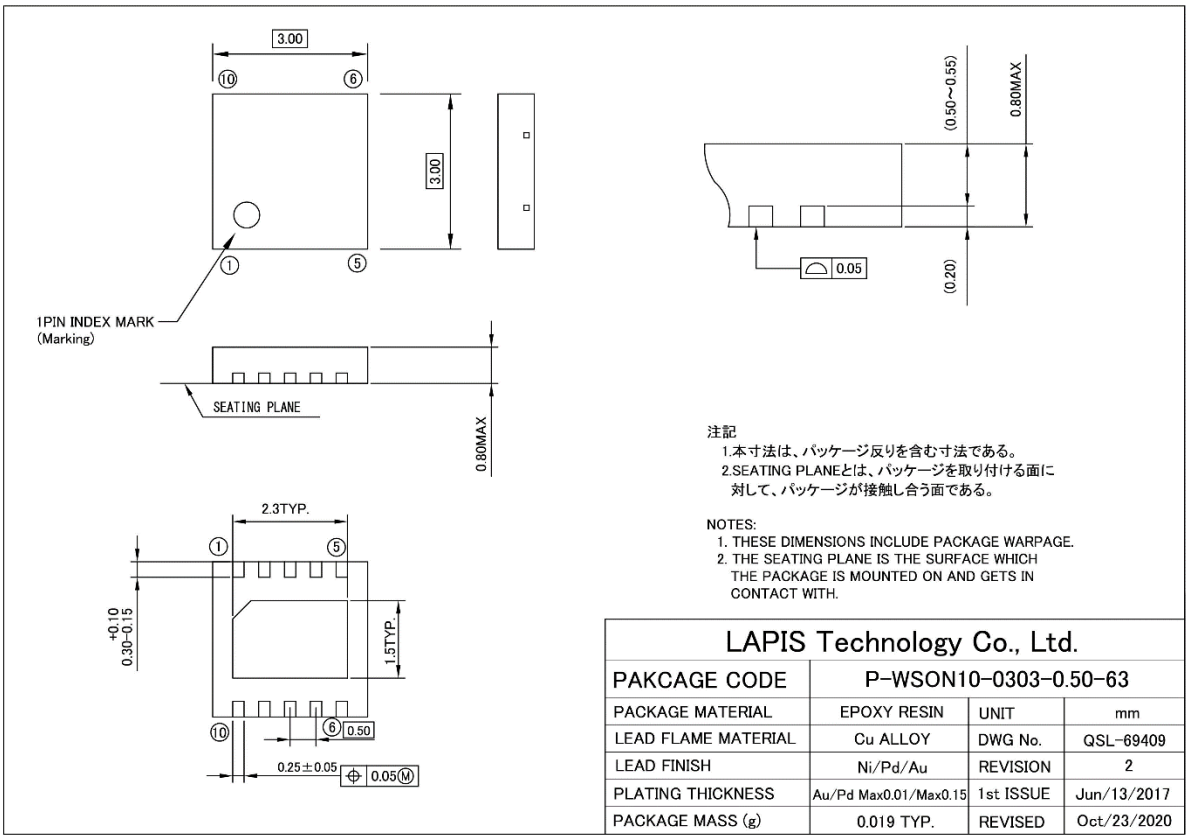
■ Application Circuit Example (5-cell system)



■ Recommended values for External Components

Component	Recommended Value
R_{VDD}	1kΩ
C_{VDD}	4.7μF
R_{CELL}	1kΩ
C_{CELL}	0.1μF

■ Package Dimensions



注記
1.本寸法は、パッケージ反りを含む寸法である。
2.SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。

NOTES:
1. THESE DIMENSIONS INCLUDE PACKAGE WARPAGE.
2. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PAKCAGE CODE	P-WSON10-0303-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69409
LEAD FINISH	Ni/Pd/Au	REVISION	2
PLATING THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Jun/13/2017
PACKAGE MASS (g)	0.019 TYP.	REVISED	Oct/23/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to heat applied in solder reflow and moisture absorbed during storage. Please contact your local ROHM sales representative for recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

■ Revision History

Document No.	Issue date	Page		Revision Description
		Before rvision	After revision	
FEDL5241-01	2019.07.23	—	—	Initial release.
FEDL5241-02	2020.12.01	—	—	Changed Company name
		14	14	Changed “Notes”
FEDL5241-03	Jan. 9, 2024	1	1	Add Application Part number
		14	14	Add Notes

Notes

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