Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5245

5 to 13 Series Cell Rechargeable Battery Protection IC

■ General Description

The ML5245 is a protection IC for 5- to13-cell Li-ion rechargeable battery pack. It detects individual cell overvoltage/undervoltage and pack overcurrent/over-temperature, and then automatically turns on or turns off the external charge/discharge NMOS-FETs accordingly.

Also, the ML5245 has a cell voltage monitor function so that the individual cell voltage can be monitored by an external microcontroller.

■ Features

- Number of connected cells : 10-cell / 13-cell
- Highly accurate overvoltage / undervoltege detection function
  - Overvoltage detection accuracy : ±15mV(25℃)
  - Undervoltage detection accuracy : ±50mV(25℃)
- Charge / discharge overcurrent detection function
  - Dischrage overcurrent detection accuracy : ±10mV(25℃)
  - Charge overcurrent detection accuracy : ±10mV(25℃)
- Short current detection function
  - Short current detection accuracy : ±15mV(25℃)
- Adjustable detection delay time for overvoltage / undervoltage / short current with external capacitor
- Temperature detection function : with external NTC(10kΩ, B=3435) and 4.7kΩ resistor.
  - Discharge inhibition temperature : 75℃ or higher
  - Charge inhibition temperature : 55℃ or higher, -5℃ or lower
- Cell voltage monitor function : Cell voltage multiplied by 0.5 is outputted from VMON pin
- FET overheat protection function : stop large charge/discharge current through FET body-diode and protect this IC from overheat.
- Number of connected cells, each detection voltage, each detectin delay time is selected with mask-option (Code number)
- Low power consumption
  - Normal state : 25μA(typ), 60μA（max）
  - Power down state : 0.1μA(typ),1μA(max)
- Supply voltage : +7V to +80V
- Operating temperature : -40℃ to +85℃
- Package : 30pin SSOP

■ Application

・Power tools and Garden tools
・Cordless Cleaner
・E-Bike and Electric assisted bicycle
・Uninterruptible Power Supplies (UPS)
・Energy Storage Systems (ESS)

■ Part number

ML5245-xxxMB (xxx: code number)
The detection voltage, etc., depends on the code number.
The parameters for the 001 code are listed in this data sheet.
Please refer to the code list for codes other than 001.

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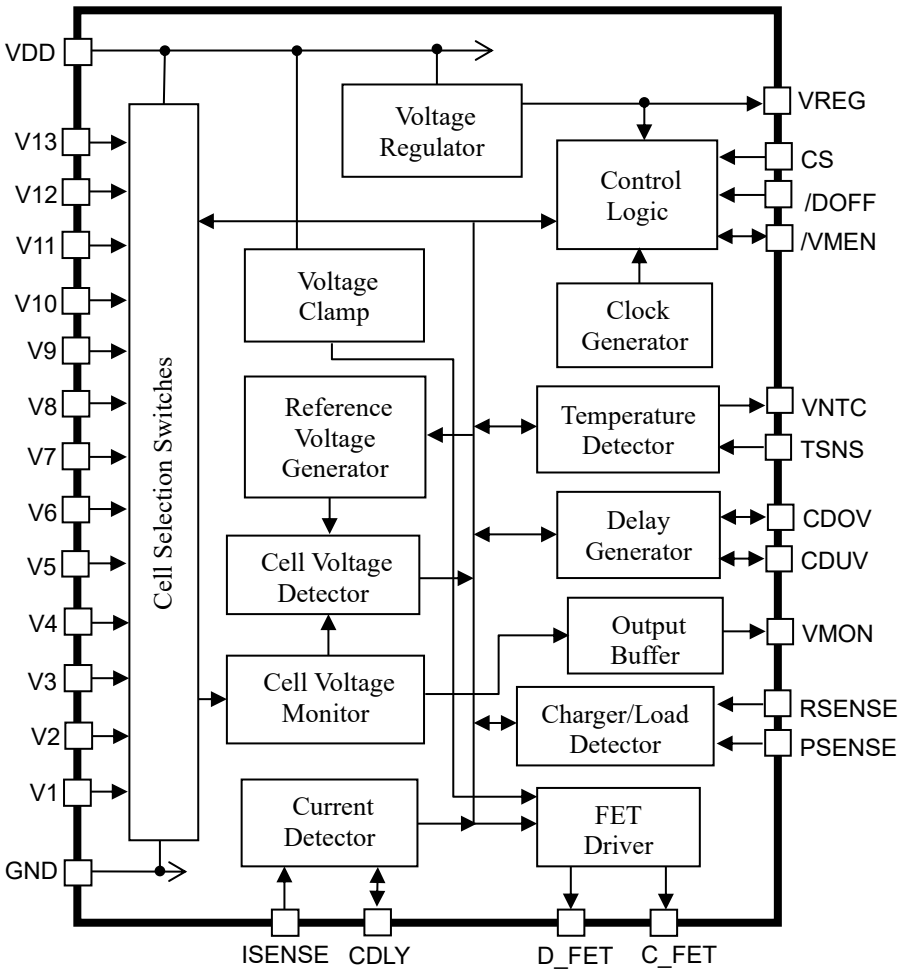
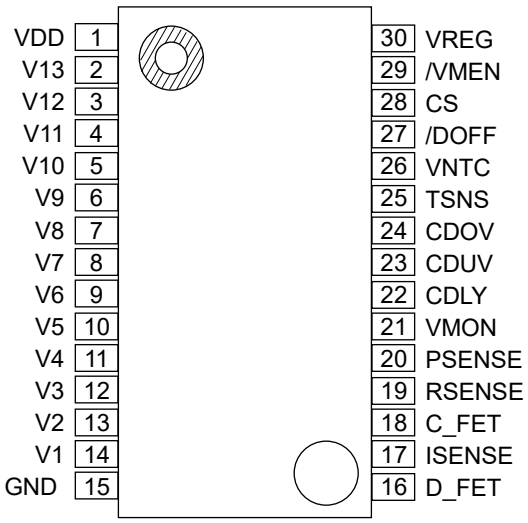
ROHM SEMICONDUCTOR

■ Block Diagram



■ Pin Configuration (top view)



■ Pin Description

Pin	Pin	I/O	Description
1	VDD	—	Power supply input pin. Connect and external CR filter for noise rejection
2	V13	I	Battery cell 13 high voltage input pin.
3	V12	I	Battery cell 13 low voltage input and battery cell 12 high voltage input pin
4	V11	I	Battery cell 12 low voltage input and battery cell 11 high voltage input pin
5	V10	I	Battery cell 11 low voltage input and battery cell 10 high voltage input pin
6	V9	I	Battery cell 10 low voltage input and battery cell 9 high voltage input pin
7	V8	I	Battery cell 9 low voltage input and battery cell 8 high voltage input pin
8	V7	I	Battery cell 8 low voltage input and battery cell 7 high voltage input pin
9	V6	I	Battery cell 7 low voltage input and battery cell 6 high voltage input pin
10	V5	I	Battery cell 6 low voltage input and battery cell 5 high voltage input pin
11	V4	I	Battery cell 5 low voltage input and battery cell 4 high voltage input pin
12	V3	I	Battery cell 4 low voltage input and battery cell 3 high voltage input pin
13	V2	I	Battery cell 3 low voltage input and battery cell 2 high voltage input pin
14	V1	I	Battery cell 2 low voltage input and battery cell 1 high voltage input pin
15	GND	—	Ground pin
16	D_FET	O	Discharge FET control signal output pin. Should be tied to the gate pin of the external NMOS FET.
17	ISENSE	I	Current sense resistor input pin. Connect a resistor of the resistance value corresponding to the detecting current between this pin and the GND pin. Should be tied to the GND if not used.
18	C_FET	O	Charge FET control signal output pin. Should be tied to the gate pin of the external NMOS FET.
19	RSENSE	IO	Load open detection input pin. Should be connected to the lower node where load is connected
20	PSENSE	IO	Charger connection / open detection input pin. Should be connected to the lower node where charger is connected. if charger and load is connected to the same node,RSENSE and PSENSE should be shorted.
21	VMON	O	Cell voltage monitor output pin. Cell voltage multiplied by 0.5 is outputted. When cell voltage is not outputted, voltage is 0V.
22	CDLY	IO	Short current detection delay time setting pin. Should be tied to the GND via capacitor.
23	CDUV	IO	Overdischarge detection delay time settgin pin. Shlould be tied to the GND via capacitor.
24	CDOV	IO	Overvoltage detection delay gtime setting pin. Should be tied to the GND via capacitor.
25	TSNS	I	Input pin for high / low temperature charge / discharge inhibition. Connect a thermistor between this pin and GND. Should be tied to the GND via 10kΩ resistor if not used.
26	VNTC	O	Thermistor power supply. Should be connected to TSNS through a 4.7 kΩ resistor.
27	/DOFF	I	OFF control command input pin for the discharge FET. The "L" level input forces "L" on the D_FET output, except when charge state is detected. Should be tied to the VREG pin if not used.
28	CS	I	Input for selecting number of connected cells. “L” level selects 13 cell and “H” level selects 10 cell.
29	/VMEN	IO	Cell voltage monitor output enable pin. This is Hi-z input and NMOS open-drain output, and for using cell volagte monitor function, connect external plull-up resistor. If the “L” pulse signal is inputted, this IC outputs the measured cell voltage into VMON pin during one cell monitoring cycle. If the measured cell voltage is outputted, an “L” level interrupt signal is outputted from this pin when the measured cell is changed. Should be tied to VREG pin if not used.
30	VREG	O	Built-in 4.3 V regulator output pin. Should be tied to GND through a 1 μF capacitor. Do not use this pin as power supply for an external circuit.

■ Absolute Maximum Ratings

GND= 0 V, Ta = +25 °C

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD pin	−0.3 to +86.5	V
Input voltage	V_{IN1}	Applied to V1 to V13, D_FET pins	−0.3 to V_{DD}+0.3	V
	V_{IN2}	Applied to CS, CDOV, CDUV, CDLY, ISENSE, TSNS pins	−0.3 to V_{REG}+0.3	V
	V_{IN3}	Applied to C_FET, RSENSE, PSENSE pins Voltage difference agains the VDD	−86.5 to +0.3	V
	V_{IN4}	Applied to /VMEN, /DOFF pins	−0.3 to +6.5	V
Output voltage	V_{OUT1}	Applied to VREG, /VMEN pins	−0.3 to +6.5	V
	V_{OUT2}	Applied to VMON, VNTC, CDOV, CDUV, CDLY pins	−0.3 to V_{REG}+0.3	V
	V_{OUT3}	Applied to D_FET pin	−0.3 to V_{DD}+0.3	V
	V_{OUT4}	Applied to C_FET pin	V_{DD}−86.5 to V_{DD}+0.3	V
Power dissipation	P_D	—	1.0	W
Short-circuit output current	I_{OS}	Applied to VREG, VMON, /VMEN, VNTC, CDOV, CDUV, CDLY, D_FET, C_FET pins	10	mA
Storage temperature	T_{STG}	—	−55 to+150	°C

■ Recommended Operating Conditions

GND= 0 V

Item	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	Applied to VDD pin	7 to 80	V
Operating temperature	T_{OP}	—	−40 to +85	°C

■ Electrical characteristics

● DC Characteristics

V_{DD}=7V to 80V, GND=0V, Ta=－40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (Note 1)	V_{IH}	—	0.8×V_{REG}	—	V_{REG}	V
Digital "L" input voltage (Note 1)	V_{IL}	—	0	—	0.2×V_{REG}	V
Digital "H" input current (Note 2)	I_{IH}	V_{IH} = V_{REG}	—	—	2	µA
Digital "L" input current (Note 2)	I_{IL}	V_{IL} = GND	–2	—	—	µA
Cell monitoring pin Input current (Note 3)	I_{INV1}	Norman mode Average current	—	0.1	3	µA
Cell monitoring pin Input leakage current (Note 3)	I_{ILVC}	Power down mode	—	—	2	µA
"L" output voltage (Note 4)	V_{OL}	I_{OL} = 1mA	—	—	0.2	V
Output leakage current (Note4)	I_{OLK}	V_{OH}=5.5V, V_{OL}=0V	–2	—	2	µA
"H" output voltage(Note5)	V_{OH1}	I_{OH}=－10µA V_{DD} =18V to 60V	10	14	18	V
"L" output voltage(Note 6)	V_{OL1}	I_{OL}=100µA	—	—	0.2	V
"L" output voltage(Note 7)	V_{OL2}	I_{OL}=1mA	—	—	0.2	V
"L" output voltage(Note 8)	V_{OL3}	I_{OL}=100µA	—	—	0.4	V
C_FET output leakage current	I_{LCF}	V_{CFET}=0 to V_{DD}	–2	—	2	µA
VREG pin output voltage	V_{REG}	With no output load VDD＝7V to 60V	3.8	4.3	4.8	V
VNTC output voltage	V_{NTC}	With 14.7kΩ resistor connected	2.2	2.4	2.6	V

Note 1: Applied to CS, /VMEN, /DOFF pins
Note 2: Applied to CS, /VMEN, /DOFF, TSNS, ISENSE pins
Note 3: Applied to V1 to V13 pins and defined in average current
Note 4: Applied to /VMEN pin
Note 5: Applied to C_FET, D_FET pins
Note 6: Applied to D_FET pin
Note 7: Applied to VMON pin
Note 8: Applied to CDOV, CDUV, CDLY pins

● Supply current characgteristics

V_{DD}= 7V to 60V, GND=0V, Ta=－40 to +85°C,

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation mode	I_{DD1}	With no output load, VMON enabled with 14.7kΩis connected to VNTC	—	25	60	µA
Current consumption in power down mode	I_{DDS}	—	—	0.1	1.0	µA

● Code 001 : detection voltage characteristics (Ta=25°C)

V_{DD}=52V, GND=0V, Ta=+25°C

Item	Symbol	Condition	Min.	Typ.	Max.	unit
Overvoltage detection threshold	V_{OV}	—	4.235	4.25	4.265	V
Overvoltage release threshold	V_{OVR}	—	4.05	4.10	4.15	V
Undervoltage detection threshold	V_{UV}	—	2.75	2.80	2.85	V
Undervoltage release threshold	V_{UVR}	—	2.95	3.00	3.05	V
Discharge overcurrent detection threshold	V_{OCU}	—	140	150	160	mV
Charge overcurrent detection threshold	V_{OCO}	—	-50	-40	-30	mV
Short circuit detection threshold	V_{SHRT}	—	285	300	315	mV
High temperature charge inhibition detection threshold	V_{CHD}	—	1.09	1.12	1.15	V
High temperature charge inhibition release threshold	V_{CHR}	—	1.17	1.22	1.27	V
High temperature discharge inhibition detection threshold	V_{DHD}	—	0.74	0.77	0.80	V
High temperature charge inhibition release threshold	V_{DHR}	—	0.82	0.85	0.88	V
Low temperature charge inhibition detection threshold	V_{CCD}	—	2.10	2.13	2.16	V
Low temperature charge inhibition release threshold	V_{CCR}	—	2.01	2.06	2.11	V

● Code 001 : detection voltage characteristics (Ta=0°C to 60°C)

V_{DD}=52V, GND=0V, Ta=0°C to +60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.225	4.25	4.275	V
Overvoltage release threshold	V_{OVR}	—	4.03	4.10	4.17	V
Undervoltage detection threshold	V_{UV}	—	2.7	2.8	2.9	V
Undervoltage release threshold	V_{UVR}	—	2.9	3.0	3.1	V
Discharge overcurrent detection threshold	V_{OCU}	—	135	150	165	mV
Charge overcurrent detection threshold	V_{OCO}	—	-55	-40	-25	mV
Short circuit detection threshold	V_{SHRT}	—	270	300	330	mV
High temperature charge inhibition detection threshold	V_{CHD}	—	1.07	1.12	1.17	V
High temperature charge inhibition release threshold	V_{CHR}	—	1.15	1.22	1.29	V
High temperature discharge inhibition detection threshold	V_{DHD}	—	0.72	0.77	0.82	V
High temperature charge inhibition release threshold	V_{DHR}	—	0.80	0.85	0.90	V
Low temperature charge inhibition detection threshold	V_{CCD}	—	2.08	2.13	2.18	V
Low temperature charge inhibition release threshold	V_{CCR}	—	1.99	2.06	2.13	V
Charge detection ISENSE pin threshold	V_{ISC}	—	-11	-6	-1	mV
Discharge detection ISENSE pin threshold	V_{ISD}	—	1	6	11	mV
VREG drop detection threshold	V_{UREG}	—	3.0	3.4	3.8	V
VREG drop release threshold	V_{RREG}	—	3.4	3.8	4.2	V

● Charger Detection / Removal and Load Removal Threshold Characteristics
(Ta=0°C to 60°C)

V_{DD}=52V, GND=0 V, Ta=0°C to +60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Charger detection PSENSE threshold	V_{PC1}	Wake-up from power-down mode	0.35 × V_{DD}	—	0.65 × V_{DD}	V
Charger removal PSENSE threshold	V_{PLU}	In charge overcurrent state	0	0.2	0.4	V
	V_{PLD}	Power-down mode	0.65 × V_{DD}	0.75 × V_{DD}	0.85 × V_{DD}	V
Load removal RSENSE threshold	V_{RL}	In discharge overcurrent state	1.0	1.2	1.4	V
PSENSE pin pull-up resistance	R_{PU}	In charge overcurrent state Power-down mode	200	500	1000	kΩ
RSENSE pin pull-down resistance	R_{PD}	In discharge overcurrent state Short-current state	1	3	7	MΩ
PSENSE pin Input leakage current	I_{LPS}	Without pull-up resistor	-2	—	2	µA
RSENSE pin Input leakage current	I_{LRS}	Without pull-down resistor	-2	—	2	µA

● Code 001 : Detection / Release Delay and Monitor Cycle Characteristics (Ta=0 to 60℃)

V_{DD}=52V, GND=0 V, Ta=0 to +60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage monitor cycle	t_{DET}	—	290	400	630	ms
Overvoltage detection delay (Note)	t_{OV}	C_{OV}=0.1µF	3.0	5.0	13.0	sec
Undervoltage detection delay (Note)	t_{UV}	C_{UV}=0.1µF	3.0	5.0	13.0	sec
Charge overcurrent detection delay	t_{OCO}	—	290	400	630	ms
Discharge overcurrent detection delay	t_{OCU}	—	290	400	630	ms
Short circuit detection delay	t_{SC}	C_{DLY}=10nF	0.6	1.0	1.4	ms
Temperature monitor cycle	t_{PT}	—	290	400	630	ms
Temperature measurement time	t_{TM}	—	2	3	5	ms
Temperature detection / release delay	t_{TDR}	Defined with temperature monitoring times	—	2	—	times
Charge state detection/release delay	t_{ISC}	—	50	100	150	ms
Discharge state detection / release delay	t_{ISD}	—	50	100	150	ms
Load removal detection delay	t_{ORL}	Discharge overcurrent state Short-current state	50	100	150	ms
Charger removal detection delay	t_{OCHG}	Charge overcurrent state	50	100	150	ms

(Note) The maximum time of ovcrcharge / overdischarge detection delay time is introduced by adding time lag due to cell voltage monitor cycle and overvoltage / undervoltage delay timer time (t_{OV}, t_{UV}).

● Cell voltage monitor output characteristics (Ta=25℃)

V_{DD}=52V, GND=0 V, Ta=25°C, with no load on VMON output

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VMON output voltage	V_{CELO4}	Cell voltage=4V	1.985	2.00	2.015	V
	V_{CELO1}	Cell voltage=3V	1.475	1.5	1.525	V

● Cell voltage monitor output characteristics (Ta=0 to 60℃)

V_{DD}=52V, GND=0 V, Ta=0 to +60°C, with no load on VMON output

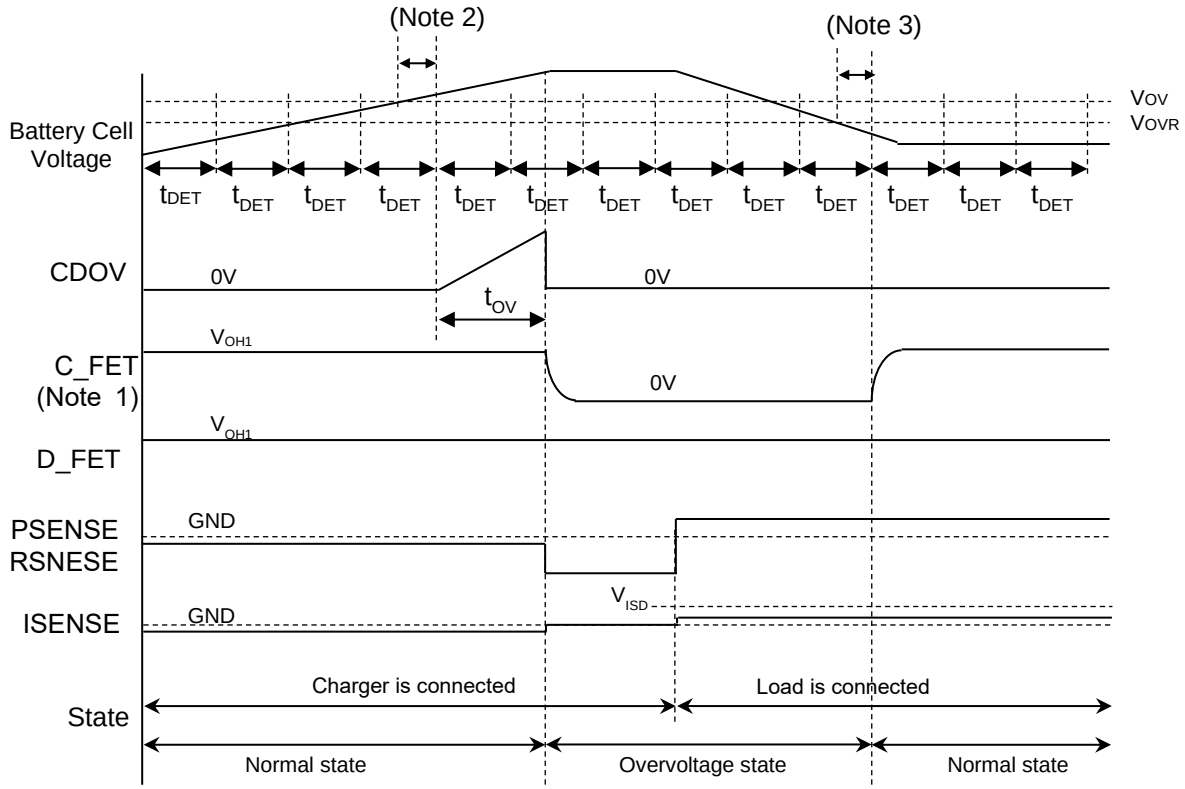
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage monitor range	V_{VMR}	—	0.1	—	4.5	V
VMON output voltage	V_{CELO4}	Cell voltage=4V	1.98	2.00	2.02	V
	V_{CELO1}	Cell voltage=3V	1.475	1.5	1.525	V
VMON output current capability	I_{VCO}	—	−100	—	+100	µA
/VMEN pin input “L” pulse width	t_{VEL}	Cell voltage output stared	1	—	—	µs
/VMEN pin output ”L” pulse width	T_{INT}	Switching the measured cell	1.0	1.8	2.6	ms
VMON output time	t_{VMO}	As per a cell monitoring	1.2	3	4.8	ms
VMON output settling time	t_{SVM}	No output load	—	—	1	ms

■ Timing Chart

This section shows the timing diagrams of application circuit example 1 (charge / discharge route is common)

● Overvoltage detection and recovery from overvoltage state with light load

Light load means that load is connected and ISENSE pin input voltage is lower than the Discharge detection ISENSE pin threshold (V_{ISD}).



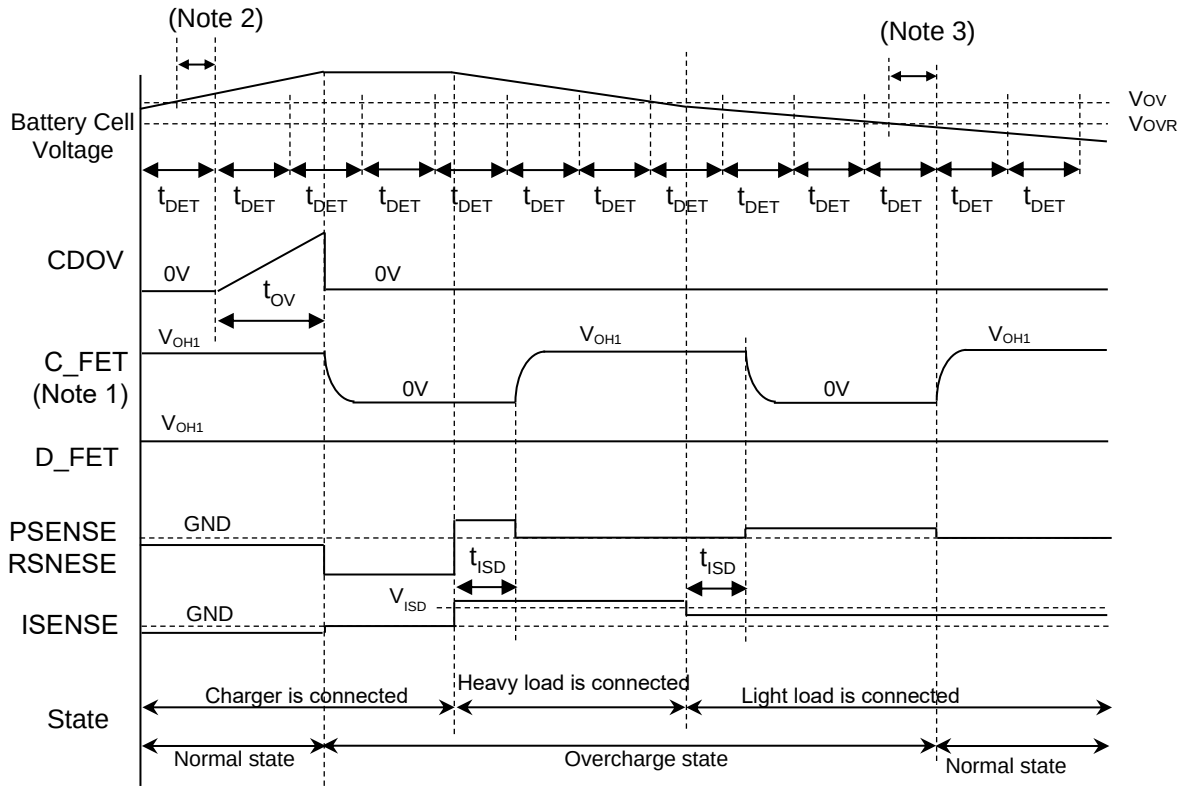
(Note 1) C_FET pin is pulled down with a resistor

(Note 2) Even if the voltage difference between Vn+1 and Vn reaches or rises above the overvoltage detection threshold V_{OV}, there may be a time lag before starting the overvoltage detection delay timer because cell voltages are monitored every 400 ms (typ.).

(Note 3) Even if the voltage difference between Vn+1 and Vn reaches or falls below the overvoltage release threshold V_{OVR}, there may be a time lag before recovering from the overvoltage state because cell voltages are monitored every 400 ms (typ.).

● Overvoltage detection and recovery from overvoltage state with Heavy load

Heavy load means that load is connected and ISENSE pin input voltage is higher than the Discharge detection ISENSE pin threshold (V_{ISD}).

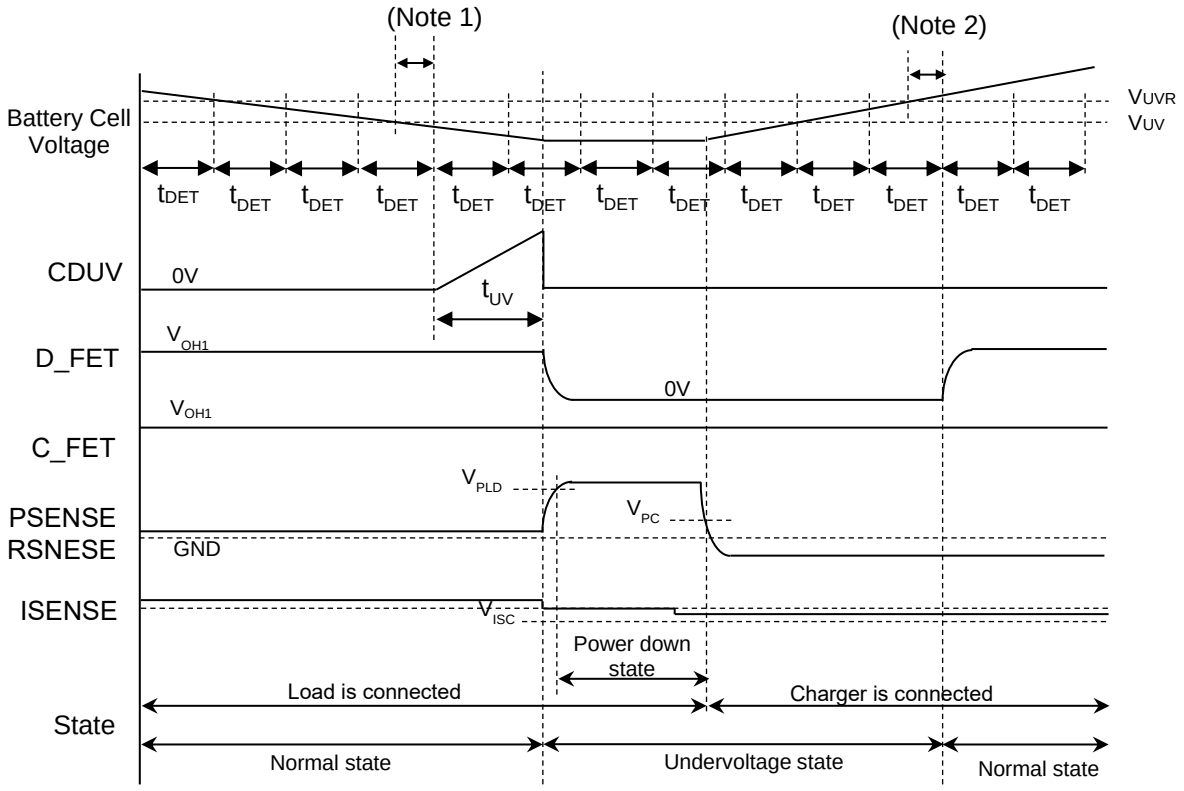


(Note 1) C_FET pin is pulled down with a resistor

(Note 2) Even if the voltage difference between Vn+1 and Vn reaches or rises above the overvoltage detection threshold V_{OV}, there may be a time lag before starting the overvoltage detection delay timer because cell voltages are monitored every 400 ms (typ.).

(Note 3) Even if the voltage difference between Vn+1 and Vn reaches or falls below the overvoltage release threshold V_{OVR}, there may be a time lag before recovering from the overvoltage state because cell voltages are monitored every 400 ms (typ.).

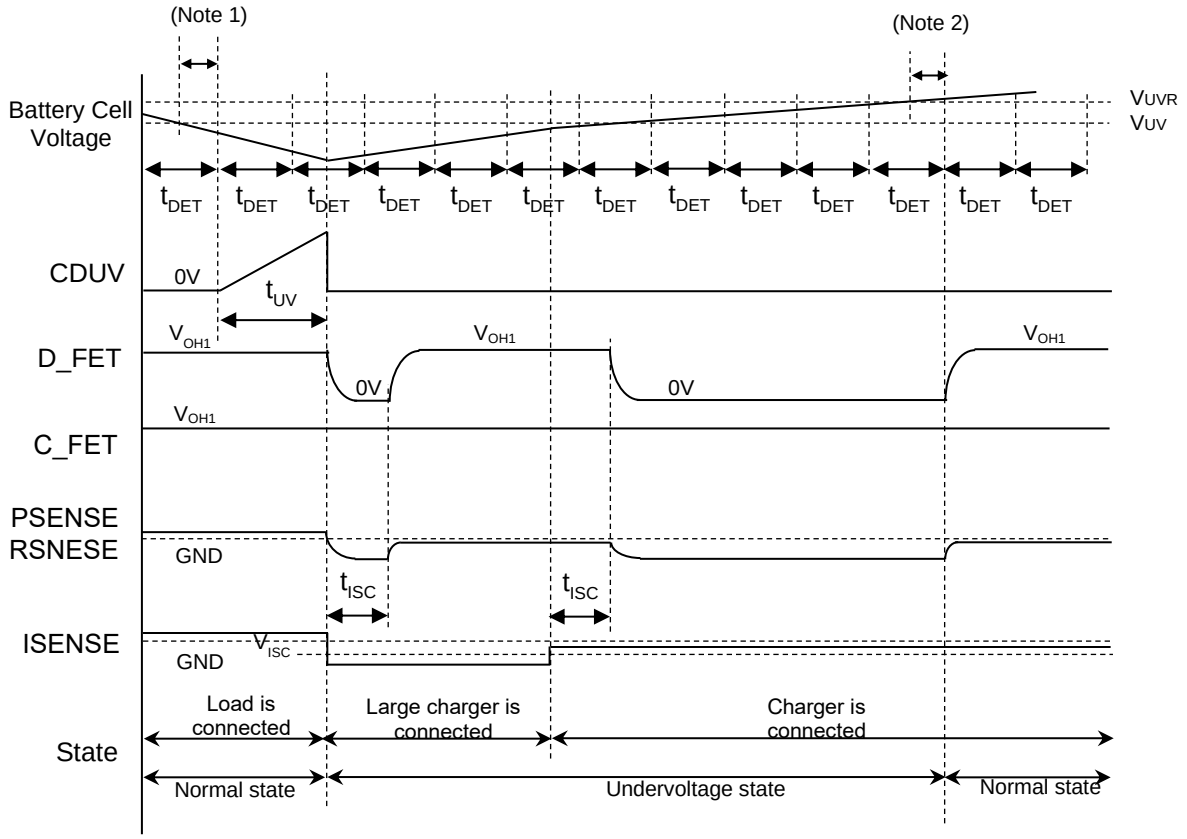
● Undervoltage Detection, Transition to Power-down Mode and Recovery



(Note 1) Even if the voltage difference between Vn+1 and Vn reaches or falls below the undervoltage detection threshold V_{UV}, there may be a time lag before starting the undervoltage detection delay timer because cell voltages are monitored every 400 ms (typ.).

(Note 2) Even if the voltage difference between Vn+1 and Vn reaches or rises above the undervoltage release threshold V_{UVR}, there may be a time lag before recovering from the undervoltage state because cell voltages are monitored every 400 ms (typ.).

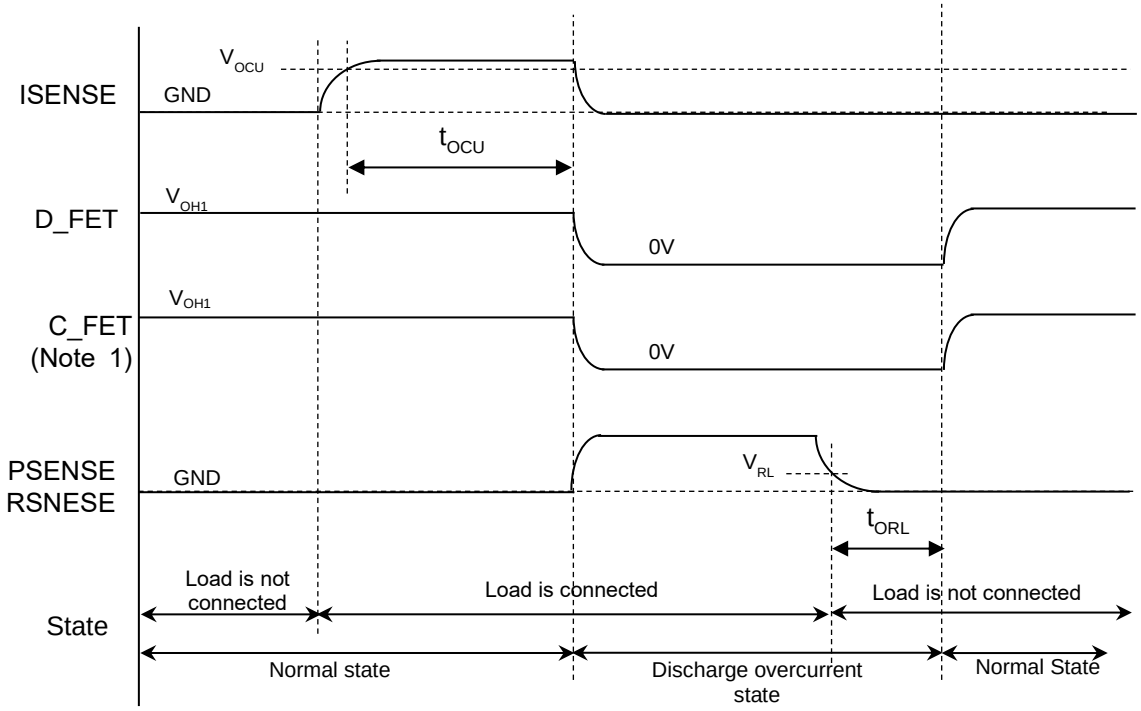
● Undervoltage Detection and Large charger connection



(Note 1) Even if the voltage difference between Vn+1 and Vn reaches or falls below the undervoltage detection threshold V_{UV}, there may be a time lag before starting the undervoltage detection delay timer because cell voltages are monitored every 400 ms (typ.).

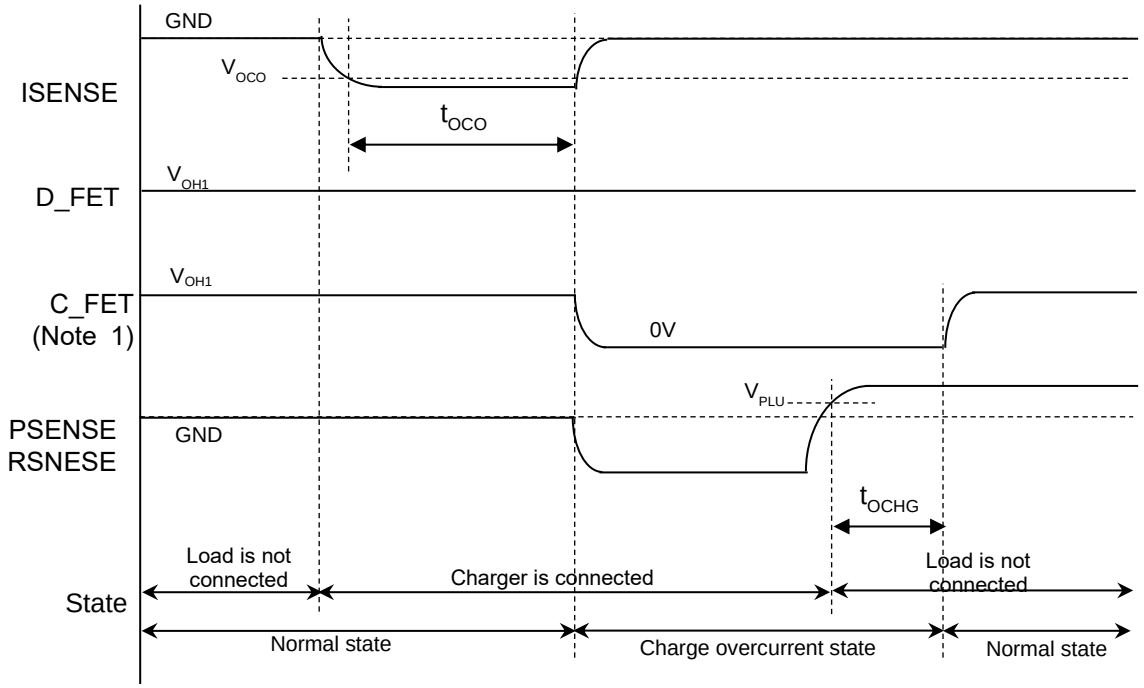
(Note 2) Even if the voltage difference between Vn+1 and Vn reaches or rises above the undervoltage release threshold V_{UVR}, there may be a time lag before recovering from the undervoltage state because cell voltages are monitored every 400 ms (typ.).

● Discharge overcurrent detection, recovery from discharge overcurrent state by load removal



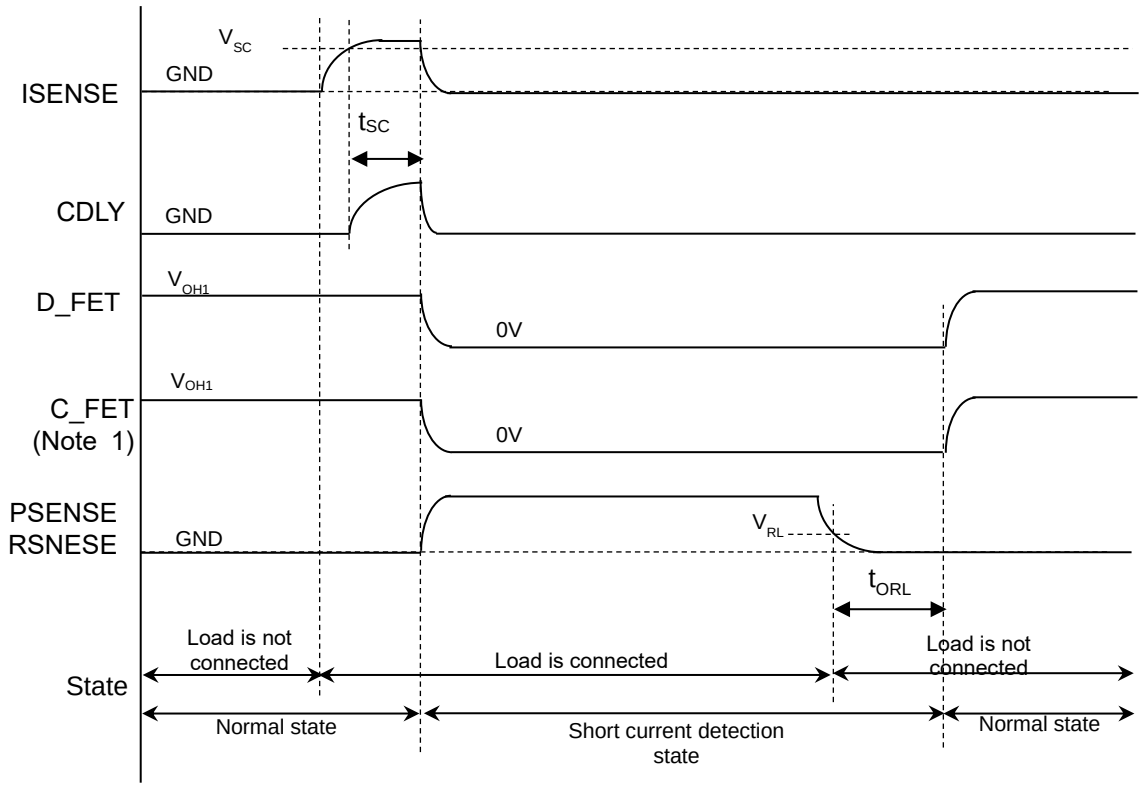
(Note 1) C_FET pin is pulled down with a resistor.

● Charge overcurrent detection and recovery from charge overcurrent state by charger removal



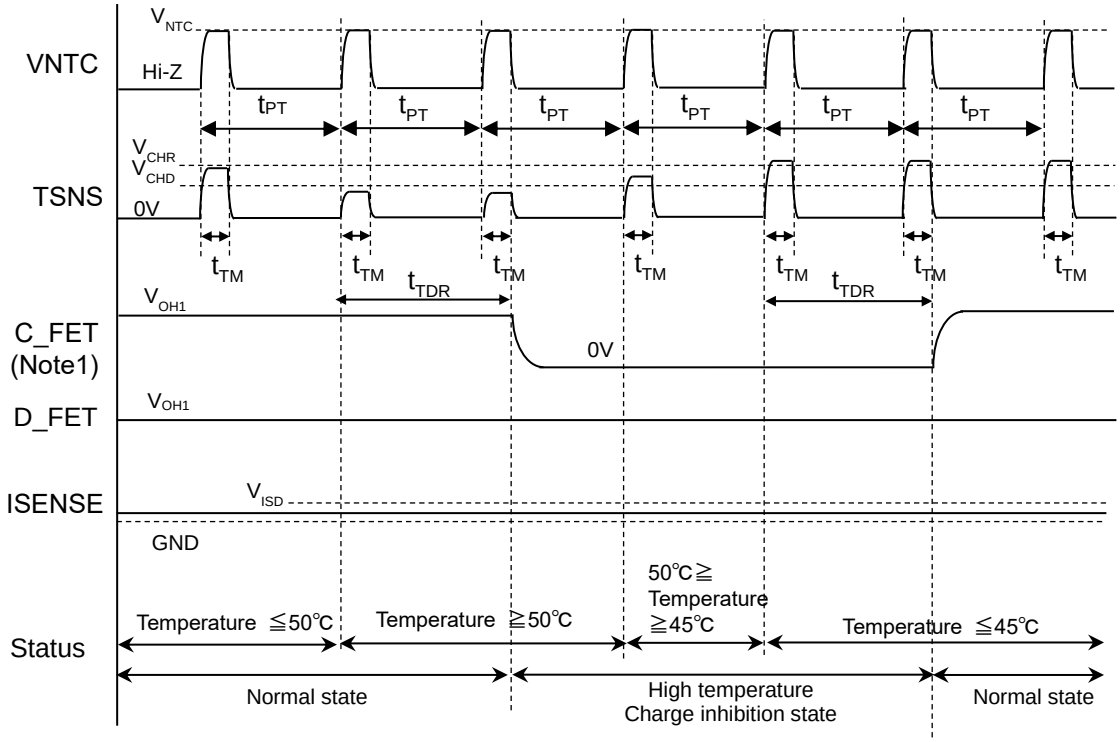
(Note 1) C_FET pin is pulled down with a resistor.

● Short Current Detection and recovery from Short Current State by Load Removal



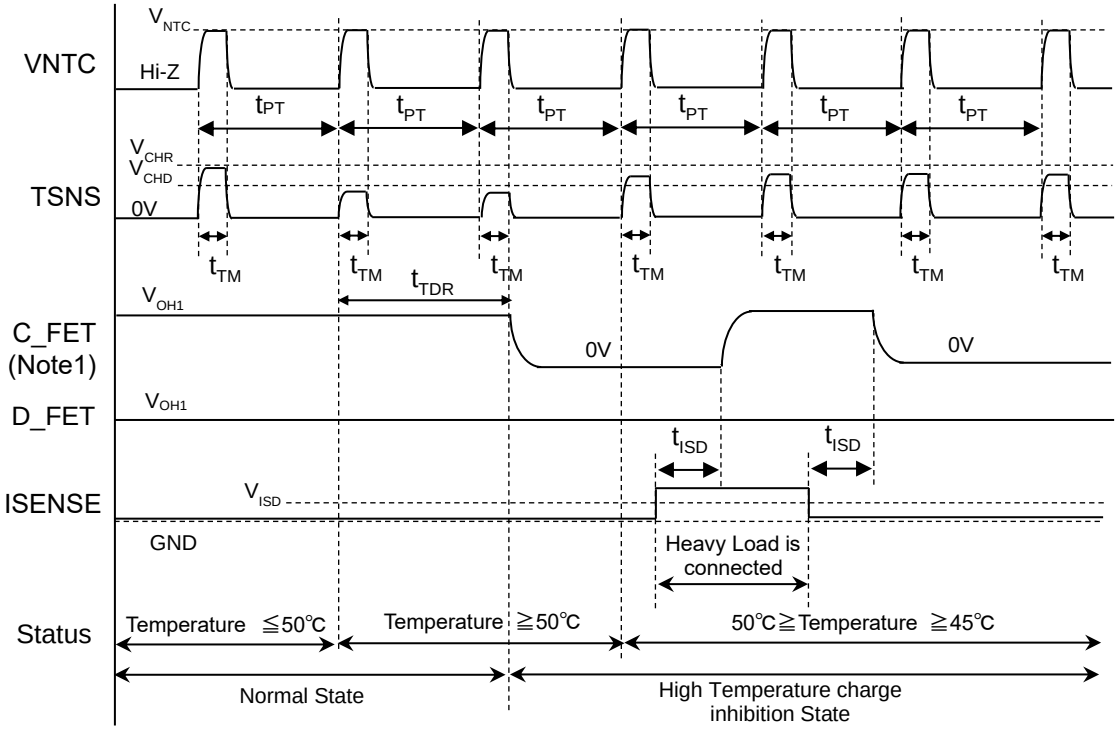
(Note 1) C_FET pin is pulled down with a resistor.

● High temperature charge inhibition detection and revcovery from high temperature charge inhibition state



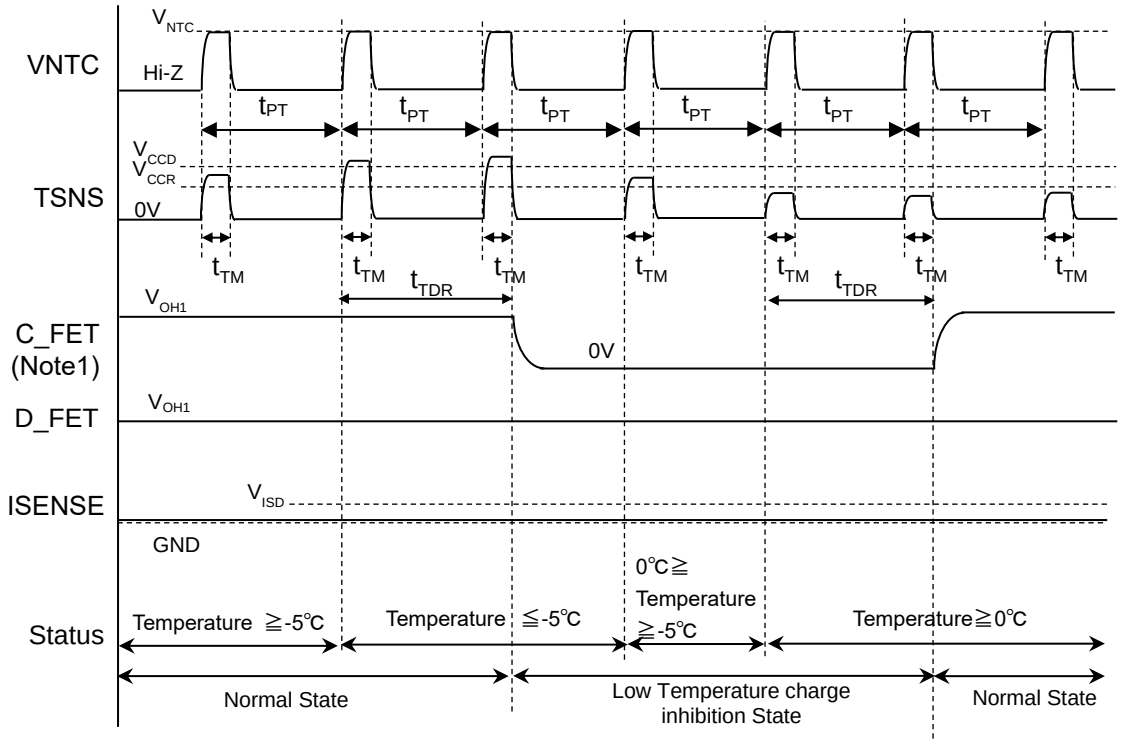
(Note 1) C_FET pin is pulled down with a resistor.

● High Temperature charge inihibition detection and heavy load connection



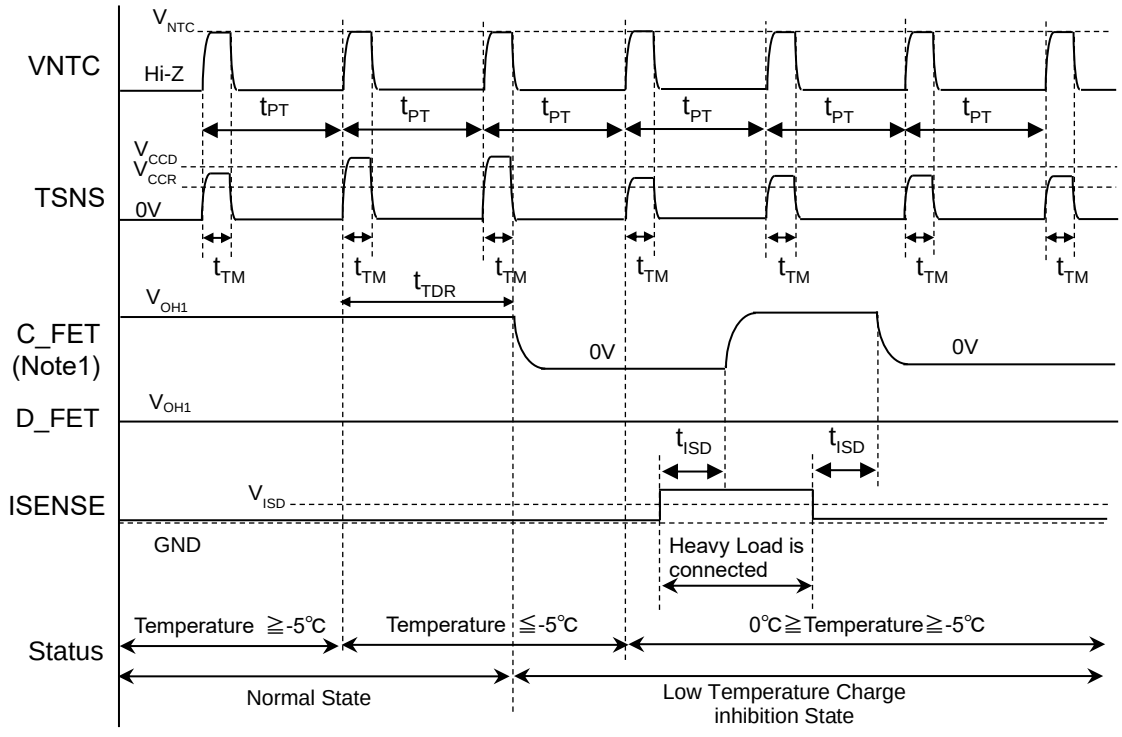
(Note 1) C_FET pin is pulled down with a resistor.

● Low temperatrure charge inhibition detection, recovery from Low temperature charge inhibition state



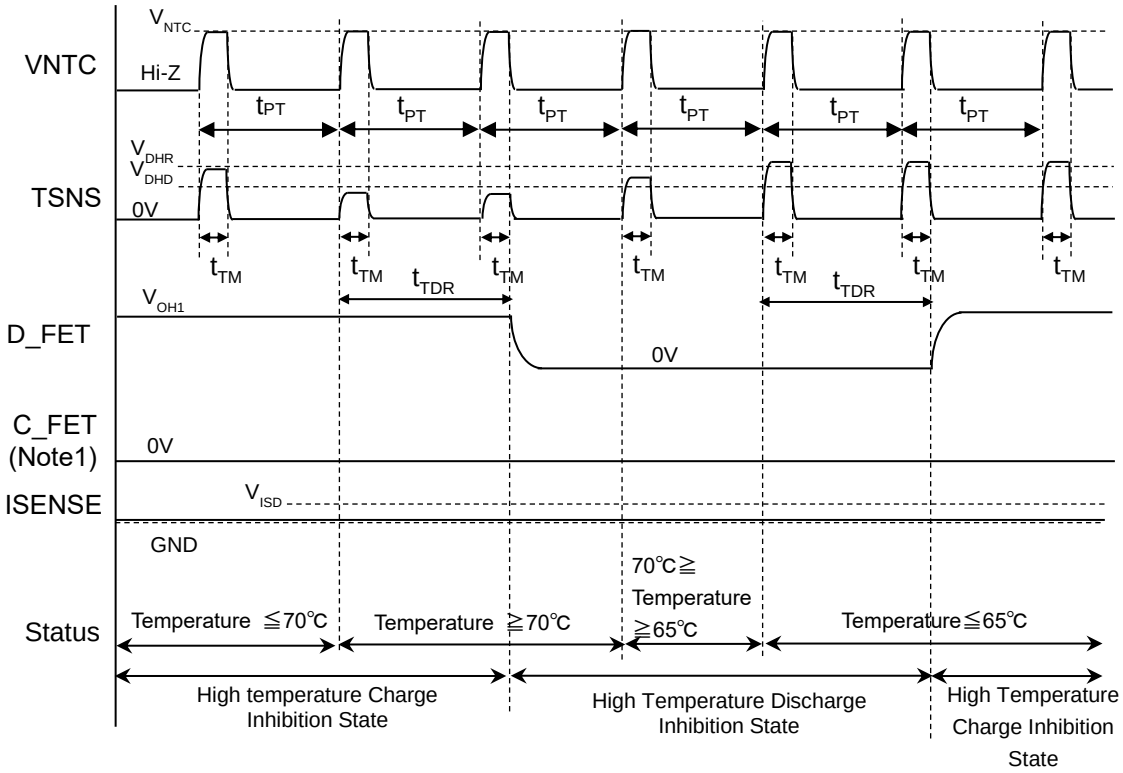
(Note 1) C_FET pin is pulled down with a resistor.

● Low temperature Charge inhibition detection and Heavy Load connection



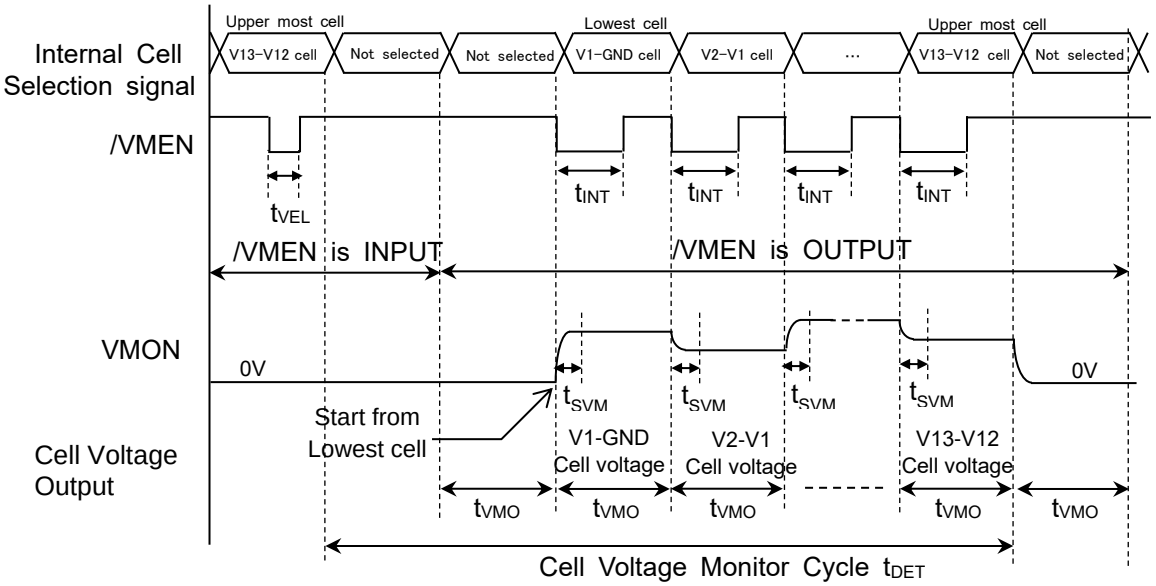
(Note 1) C_FET pin is pulled down with a resistor.

● High Temperature Discharge inhibition and recovery from High Temperature Discharge Inhibition State



(Note 1) C_FET pin is pulled down with a resistor.

● Cell Voltage Monitor Output (13 cell connected)



■ Function Description

● State of ML5245

The ML5245 has following ten states, which depend on individual cell voltages and the input level of the ISENSE and TSNS pins.

1. Initial state
2. Normal state
3. Overvoltage state
4. Undervoltage state(including power-down mode)
5. Discharge overcurrent state
6. Charge overcurrent state
7. Short circuit state
8. High Temperature Charge Inhibition state
9. Low Temperature Charge Inhibition state
10. High Temperature Discharge Inhibition state

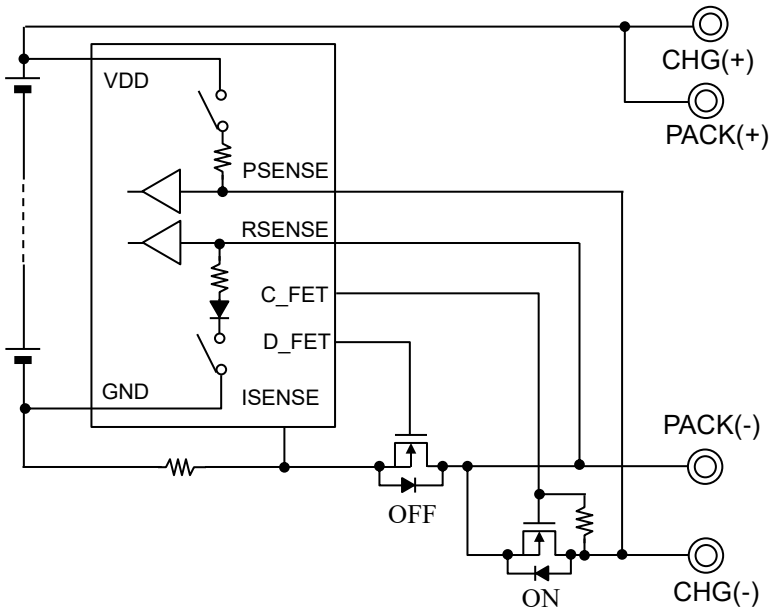
Each state is described below.

1. Initial State

The initial state refers to the period while the battery cells are being connected to the ML5233 and connection of all the battery cells specified by the CS pin is completed, before transitioning to the normal state.。

In the initial state, when the VREG pin voltage reaches or falls below the VREG drop detection threshold, the D_FET pin output is set to the "L" level and the C_FET pin output to the "H" level, where discharge is inhibited and charge is permitted.

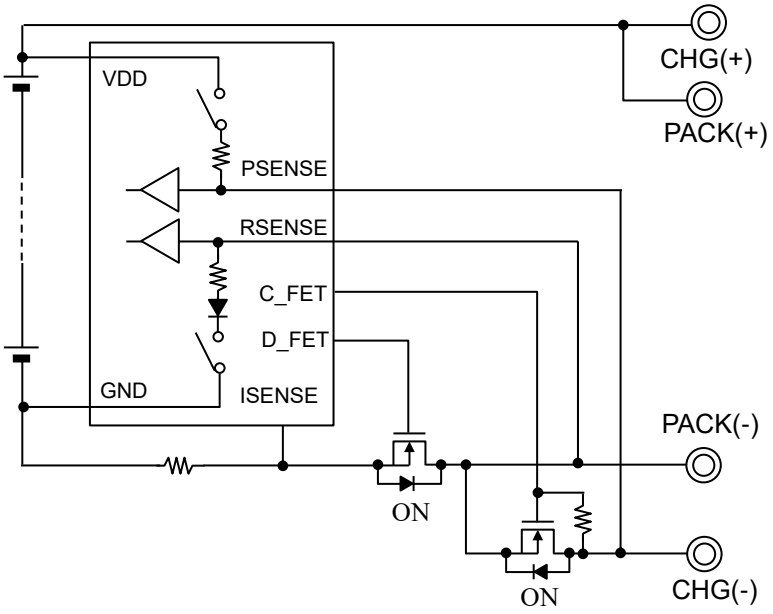
When the VREG pin level reaches or rises above the VREG drop release threshold V_{RREG}, individual cell voltage monitoring takes place. If all the battery cells specified by the CS pin reach or rise above the undervoltage release threshold V_{UVR}, the system transitions to the normal state. Overvoltage and overcurrent detection is also performed in parallel.



2. Normal Operation State

The normal state refers to the period where all the battery cell voltages do not reach or rise above the overvoltage/undervoltage detection threshold, the ISENSE pin voltage is below the overcurrent detection threshold, and the TSNS pin voltage is above the high temperature detection threshold. In the normal state, both the D_FET and C_FET pin outputs are set to the "H" level, where both charge and discharge is permitted.

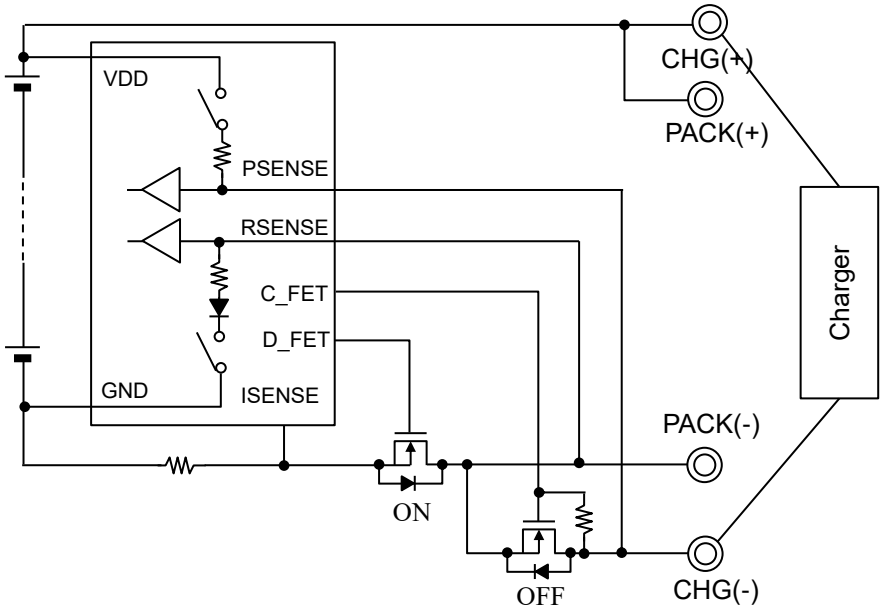
Individual cell voltages are monitored every 0.4 second for performing overvoltage/undervoltage detection, while the pack temperature is also monitored using an external thermistor every 0.4 second. The ISENSE pin voltage is always monitored to detect overcurrent in parallel.



3. Overvoltage State

When any one or more battery cell voltages reach or rise above the overvoltage detection threshold V_{OV} for longer than the overvoltage detection delay time t_{OV}, the system enters the overvoltage state. In the overvoltage state, the C_FET pin output is set to "Hi-Z" to inhibit charge, while the D_FET pin output maintains the value in the previous state.

Battery cell voltages decrease gradually by self-discharge or a connected load. When all of them reach or fall below the overvoltage detection release threshold V_{OVR}, the system recovers from the overvoltage state.



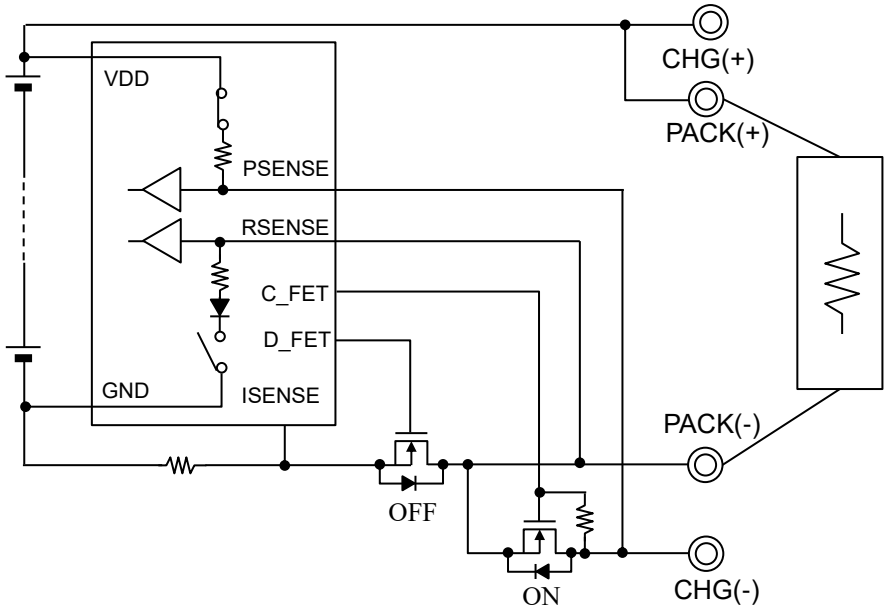
4. Undervoltage State

When any one or more battery cell voltages reach or fall below the undervoltage detection threshold V_{UV} for longer than the undervoltage detection delay time t_{UV}, the system enters the undervoltage state. In the undervoltage state, the D_FET pin output is set to the "L" level to inhibit discharge, while the C_FET pin output maintains the value in the previous state.

In the undervoltage state, a 500 kΩ pull-up resistor is connected between the PSENSE pin and VDD. When the PSENSE pin voltage increases and reaches the charger removal PSENSE threshold V_{PLD} after turning off the external discharge FET, the system enters power-down mode to reduce current consumption.
The PSENSE pin voltage decreases when a charger is present. If it reaches or falls below the charger detection voltage V_{PC}, the system wakes up all the circuits to resume monitoring individual battery cell voltages.

If the system was in the overvoltage, undervoltage, high temperature or any overcurrent state before entering power-down mode, these error flags are cleared during power-down. After wake-up, if these errors are detected again for longer than the specified detection delay time, the system reenters the corresponding error state.

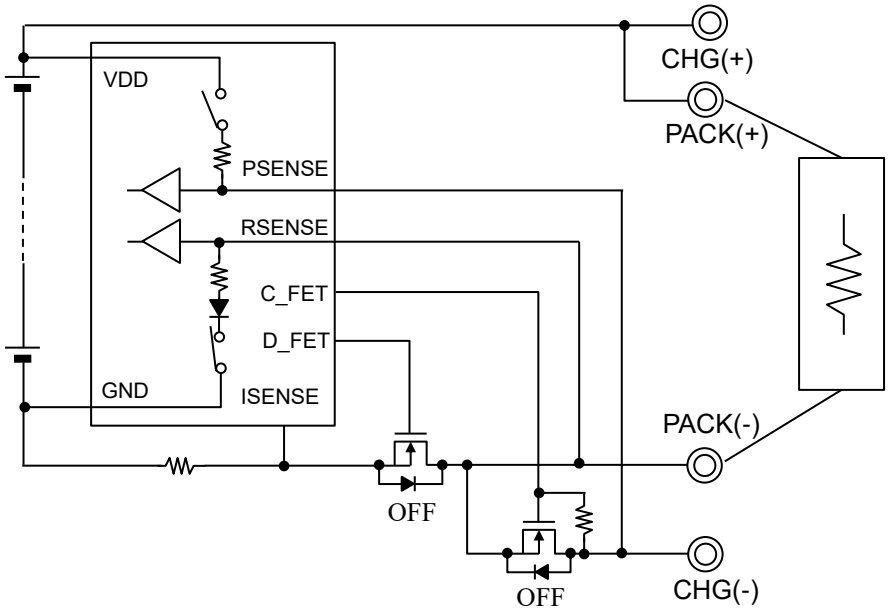
Battery cell voltages increase while charging, and if all cell voltages reach or rise above the undervoltage detection release threshold V_{UVR}, the system recovers from the undervoltage state



5. Discharge Overcurrent State

When the load is connected and ISENSE pin voltage reaches or rises above the discharge overcurrent detection threshold V_{OCU} for longer than the discharge overcurrent detection delay time t_{OCU}, the system enters the discharge overcurrent state, regardless of the individual battery cell voltages. In the discharge overcurrent state, the D_FET pin output is set to the "L" level to inhibit discharge, while the C_FET pin output is set to "Hi-Z" to monitor load removal.

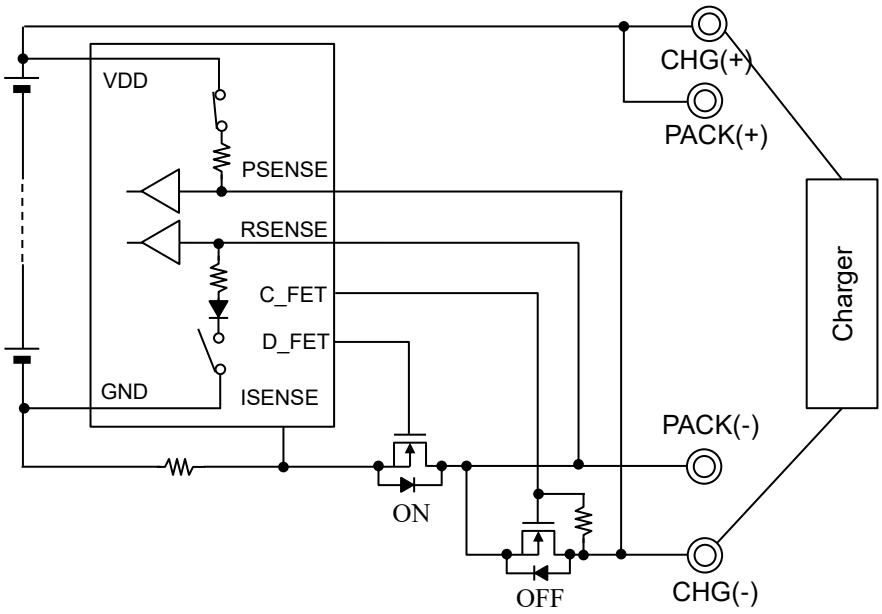
In the discharge overcurrent state, the RSENSE pin is pulled-down with a resistor and a backflow prevention diode. If the load is released, the RSENSE pin level approaches the GND level. The system recovers from the discharge overcurrent state when the RSENSE pin level reaches or falls below the load removal RSENSE threshold V_{RL} for longer than the load removal detection delay time t_{ORL} .



6. Charge Overcurrent State

When the charger is connected and ISENSE pin voltage reaches or falls below the charge overcurrent detection threshold V_{OCO} for longer than the charge overcurrent detection delay time t_{OCO}, the system enters the charge overcurrent state, regardless of the individual battery cell voltages. In the charge overcurrent state the C_FET pin output is set to "Hi-Z" to inhibit charge, while the D_FET pin output maintains the value in the previous state.

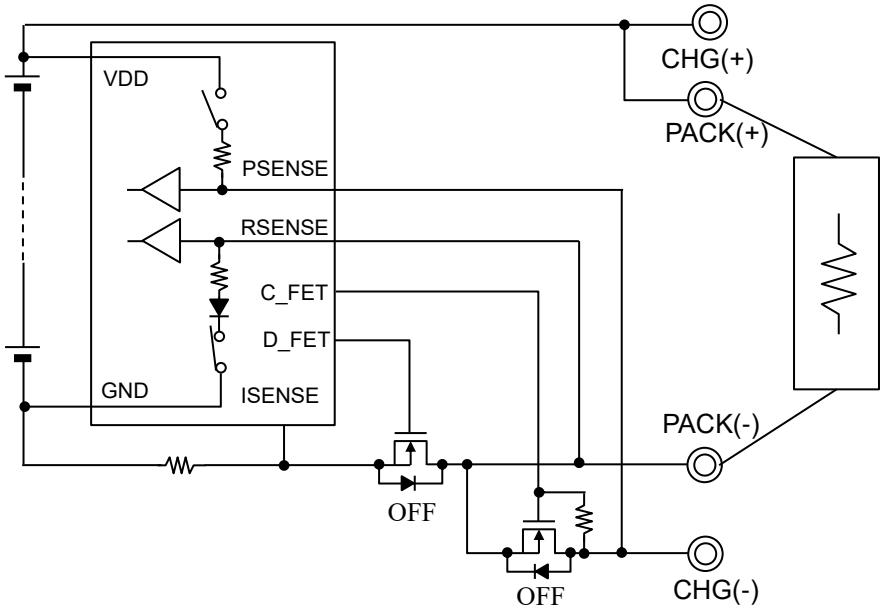
In the charge overcurrent state, a 500 kΩ pull-up resistor is connected between the PSENSE pin and VDD pin to detect charger removal. If the charger is removed, the PSENSE pin level increases. The system recovers from the charge overcurrent state when the PSENSE pin voltage reaches or rises above the charger removal detection threshold V_{PLU} for longer than the charger removal delay time t_{OCHG}.



7. Short Circuit State

When the pack is overloaded and the ISENSE pin voltage reaches or rises above the short circuit detection threshold V_{SHRT}, the capacitor connected to the CDLY pin is started to charge, regardless of the battery cell voltages. When the CDLY pin voltage is increased to a specific level, the system enters the short circuit state. In the short circuit state, the D_FET pin output is set to "L" level to inhibit discharge, while the C_FET pin output is set to "Hi-Z" to detect load removal.

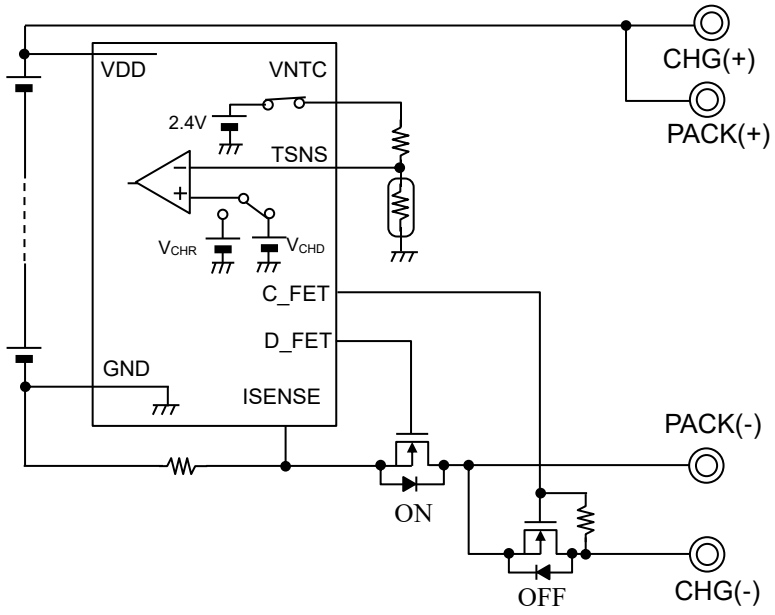
In the short circuit state, a pull-down resistor is connected between the RSENSE pin and the GND pin through a backflow prevention diode. If the load is removed, the RSENSE pin level approaches the GND level. The system recovers from the short circuit state when the RSENSE pin level reaches or falls below the load removal detection threshold V_{RL} for longer than the load removal detection delay time t_{ORL}.



8. High Temperature Charge Inhibition state

Pack temperature is monitored using an external thermistor every 0.4 seconds regardless of battery cell voltages and current measurement. When the TSNS pin voltage reaches or falls below the high temperature charge inhibition detection threshold V_{CHD} for longer than the temperature detection delay time t_{TDR}, the system enters the High Temperture Charge Inhibition state.

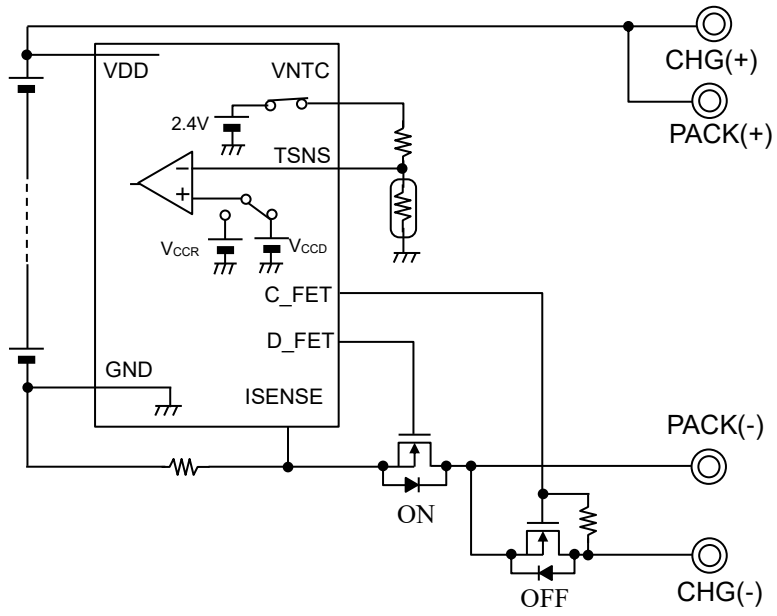
In the High Temperature Charge Inhibition state, the C_FET pin output is set to the "Hi-Z" state to inhibit charge.



9. Low Temperature Charge Inhibition state

Pack temperature is monitored using an external thermistor every 0.4 seconds regardless of battery cell voltages and current measurement. When the TSNS pin voltage reaches or rises above the Low Temperature Charge Inhibition detection threshold V_{CCD} for longer than the temperature detection delay time t_{TDR}, the system enters the Low Temperture Charge Inhibition state.

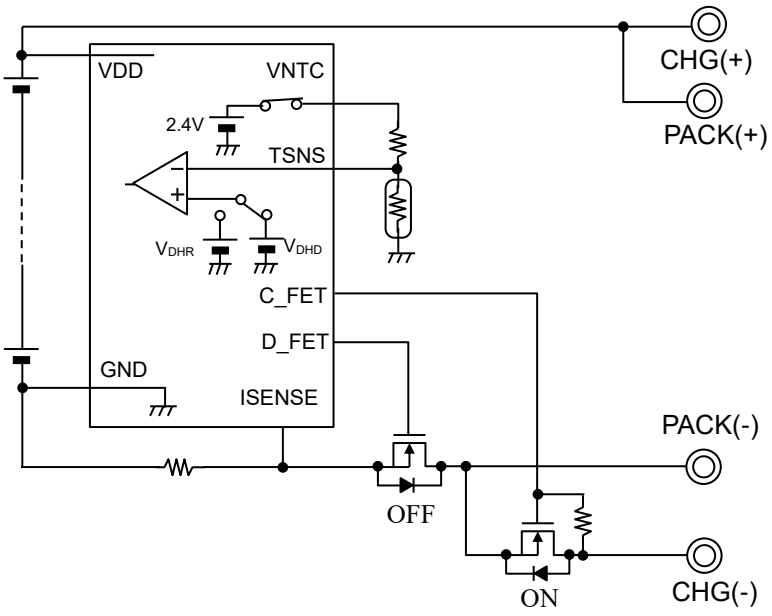
In the Low Temperature Charge Inhibition state, the C_FET pin output is set to the "Hi-Z" state to inhibit charge.



10. High Temperature Discharge Inhibition state

Pack temperature is monitored using an external thermistor every 0.4 seconds regardless of battery cell voltages and current measurement. When the TSNS pin voltage reaches or falls below the high temperature discharge inhibition detection threshold V_{DHD} for longer than the temperature detection delay time t_{TDR}, the system enters the High Temperture Discharge Inhibition state.

In the High Temperature Discharge Inhibition state, the D_FET pin output is set to the "L" state to inhibit charge.



● Cell voltage Monitoring function

ML5245 sequentially measures individual battery cell voltage from the lowermost cell to uppermost cell of the battery pack during cell monitor cycle (400ms (typ.)). By inputting the cell voltage output requirement signal (“L” pulse signal) from an external microcontroller, the measured cell voltage can be outputted into VMON pin. Since /VMEN pin is Hi-Z input in input state and open drain output in output state, connect external pull-up resistor.

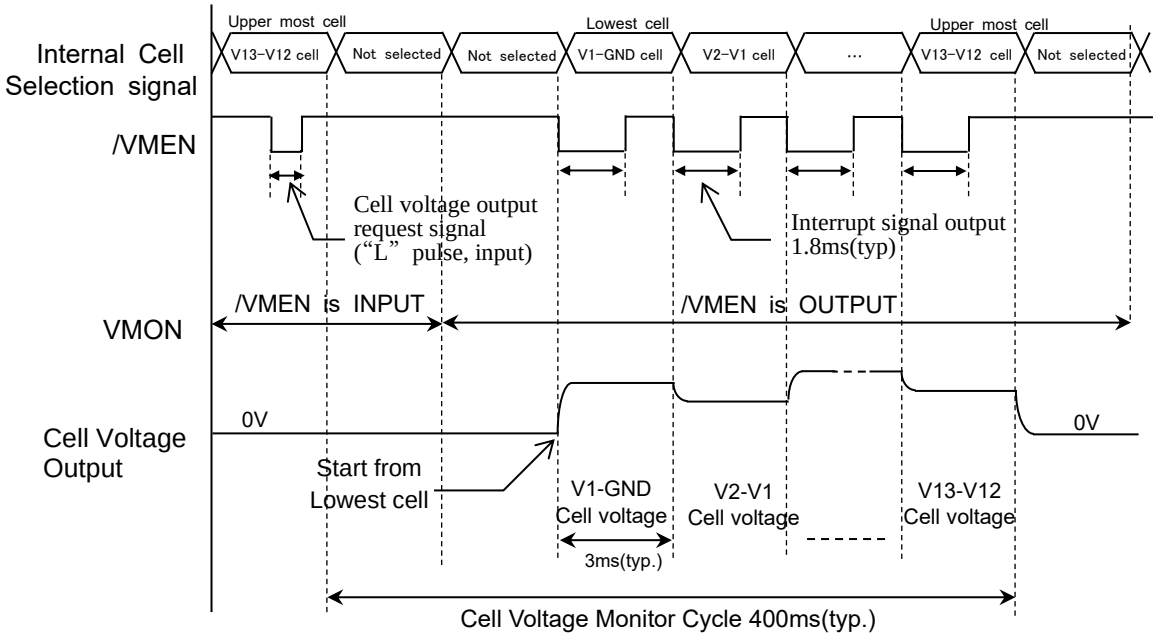
The timing chart of a cell voltage monitoring function is shown in the following figure. When the input level of /VMEN pin returns to “H” level after “L” level signal is once inputted to /VMEN pin, the measured cell voltages will be outputted into VMON pin during a cell voltage monitor cycle. In such period, /VMEN pin is in the output state and outputs an interrupt request signal whenever the measuring cell is switched.

It is noted that the measured cell voltages is not be outputted even if “L” level signal is continuously inputted to /VMEN pin since this cell voltage monitor function is enabled after the /VMEN pin is returned from “L” to “H”.

After wake-up and power-on, 60ms(typ) of internal circuit settling time is set up. In this period, inputting “L” pulse to /VEN pin is neglected.

While the cell voltage monitor function is enabled, ML5245 starts to measure the cell voltage from lowermost cell to uppermost and the measured cell voltage is amplified by 0.5 and outputted into VMON pin. During this period, /VMEN pin is in output state and an interrupt request signal, which has 1.8ms (typ.) pulse width, is outputted whenever the selected cell is changed. After the one cell voltage monitor cycle is completed, /VMEN pin returns to input state and remains the state until the cell voltage monitor will be started after the “L” pulse signal is inputted. While the cell voltage monitor function is disenabled, an output of VMON pin is 0V.

If the number of connected battery cells is less than 13 cells, VMON pin output is 0V during the measuring period of unconnected cells and if any cells are not selected during cell voltage monitoring cycle. When ML5245 is in power down state, this cell voltage monitoring function doesn’t run.



● Protection from FET overheating

If the charge/discharge connection is not separated, and one of charge/discharge FET is OFF, charge/discharge current flows through the body-diode of the FET which is turned-off. In such case, if the current is large, FET is much heated and might be broken.
ML5245 watchs charge/discharge state with ISENSE pin input voltage, and stops the currentflow of body-diode of FETs.

If the ISENSE pin input voltage is higher than discharge state detection voltage V_{ISD} for longer than discharge state detection delay time t_{ISD}, not depending on charge inhiniting state of overvoltage, set the C_FET pin "H" and stop the current flow through the body-diode of charge FET, and stop the overheating of FET. And in this status, if the voltage of ISENSE pin input is lower than Discharge state detection voltage V_{ISD} for longer than discharge release delay time t_{ISD}, the C_FET pin output changes to "Hi-Z" and the state returns to the charge inhibiting state such as overvoltage.

If the ISENSE pin input voltage is higher than charge state detection voltage V_{ISC} for longer than charge state detection delay time t_{ISC}, not depending on discharge inhiniting state of undervoltage, set the D_FET pin "H" and stop the current flow through the body-diode of discharge FET, and stop the overheating of FET. And in this status, if the voltage of ISENSE pin input is higher than Charge state detection voltage V_{ISC} for longer than Charge Release delay time t_{ISC}, the D_FET pin output changes to "L" and the state returns to the disharge inhibiting state such as undervoltage.

If the charge circuit and discharge circuit is separated as shown in the Application Circuit Example 2, and if the load is connected in charging state and discharge current flows, charge/discharge might be repeated after charge FET is turned off by overvoltage detection or other detection. In such case, charge FET's protection from overheating function should be disabled by creating new code of the ML5245.

● External control of Discharge FET

The D_FET pin output can be directly set "L" to stop discharging by the /DOFF pin input, regardless of the detected state on the ML5245.
But if the ISENSE pin input voltage is lower than charge state detection voltage V_{ISC} for longer than charge state detection delay time t_{ISC}, not depending on /DOFF input voltage, set the D_FET pin "H".
If the input level of /DOFF is VREG, the state of D_FET depends on the status of the ML5245.

● Output Pin Values in Each Detection State

The output pin values in each detection state are shown in the table below.

state	D_FET	C_FET	PSENSE	RSENSE	VREG
Initial state	GND	14V	Hi-Z	Hi-Z	4.3V
Normal state	14V	14V	Hi-Z	Hi-Z	4.3V
Overvoltage state	No change	Hi-Z	No change	No change	4.3V
Undervoltage state	GND	No change	Pull-up	No change	4.3V
Power Down sate	GND	Hi-Z	Pull-up	Hi-Z	0V
Discharge overcurrent state	GND	Hi-Z	No change	Pull-down	4.3V
Charge overcurrent state	No change	Hi-Z	Pull-up	No change	4.3V
Short current state	GND	Hi-Z	No change	Pull-down	4.3V
High temperture charge inhibition state	No change	Hi-Z	No change	No change	4.3V
Low temperature charge inhibition state	No change	Hi-Z	No change	No change	4.3V
High temperature discharge inhibition state	GND	No change	No change	No change	4.3V

(Note) "No change" means that the previous pin value is maintained in a new state.
In each state, it is expected that there is no charge/discharge current.

● Selecting the Number of Battery Cells

Cell count is selectable from predefined two values using the CS pin.

CS	Number of Battery cell	Unused Vn pins
GND	13cell	none
VREG	10cell	V1 to V3

If the number of cells is less than 13 cells, unconnected Vn pins should be tied to GND.

● Overvoltage / undervoltge detection delay time setting

Overvoltage detection delay time is calculated by adding two parameters; overvoltage detection delay time t_{OV} which depends on the capacitance C_{OV} connected to CDOV pin and GND, and time lag t_{DEL} from when the battery voltage raise above the overvoltage detectin voltage V_{OV} to when the cell voltage of overvoltage state is monitored, and described by the following equation.

Overvoltage detection delay time $(t_{OV}+t_{DEL})$ [sec] $= C_{OV}$ [µF] × 50 + t_{DEL}

If the battery cell voltage is higher than the overvoltage detection voltage, cell voltage is also monitored with 400ms(typ.) interval, time lag tDEL is brought before the overvoltage delay timer starts. This time lag is from 0 second to cell minotor cycle t_{DET}.

Undervoltage detection delay time is calculated by adding two parameters; undervoltage detection delay time t_{UV} which depends on the capacitance C_{UV} connected to CDUV pin and GND, and time lag t_{DEL} from when the battery voltage fall below the undervoltage detectin voltage V_{UV} to when the cell voltage of undervoltage state is monitored, and described by the following equation.

Undervoltage detection delay time $(t_{UV}+t_{DEL})$ [sec] $= C_{UV}$ [µF] × 50 + t_{DEL}

If the battery cell voltage is lower than the undervoltage detection voltage, cell voltage is also monitored with 400ms(typ.) interval, time lag tDEL is brought before the overvoltage delay timer starts. This time lag is from 0 second to cell minotor cycle t_{DET}.

If C_{OV}=0.1µF 、C_{UV}=0.1µF, overvoltage detection delay time and undervoltage detection delay time are 5.0+t_{DEL} second.

● Setting Short Circuit Detection Delay

The short circuit detection delay (t_{SC}) depends on the charge time of the capacitor (C_{DLY}) connected to the CDLY pin, which is described by the following equation.

Short circuit detection delay t_{SC} [ms] = C_{DLY} [nF] × 0.1

Recommended capacitance of C_{DLY} is 1nF. If the capacitance is small, 20 µs (typ.) should be added as a delay of the short current detection comparator. Note that the delay time of external CR filter on the ISENSE pin should be included.

● Power-on/Power-off Sequence

Battery cells can be connected in any order, but it is recommend that the GND and VDD pins are connected first, and then connection continues from lower to higher voltage cells. There are no restrictions on the power supply voltage rise time at power-on, and power-off sequence or power supply voltage fall time at power-off.

After power-on, the system usually transitions to the normal state. However, it may transition to the undervoltage state due to chattering at power-on or other reasons. If it has transitioned to the undervoltage state and moved to power-down mode, apply the charger connection detection threshold V_{PC} or lower level to the PSENSE pin to power it up again.

After power-on or power-up, there is 400ms(typ.) of stable time of internal cirucuit. During this interval, VMON pin doesn't output voltage value even if "L" signla is inputted in /VMEN pin.

● Handling VDD Pin and V0 to V13 Pins

Since the VDD pin is the power supply input, put a noise elimination RC filter in front of the VDD input for stabilization. If the drive current on the external charge/discharge control FETs is large, the resistor value of this noise filter should be adjusted so that the voltage drop across the resistor is smaller than 1 V.

The V0 to V13 pins are the monitor pins for individual cell voltages. Put a noise elimination RC filter in front of each battery cell to prevent false detection.

● Handling VREG Pin

The VREG pin is the power source of the built-in regulator which supplies power to the internal modules. Connect a 1 μF or larger capacitor between this pin and GND for stabilization. Do not use it as a power supply for external circuits since the supply current of the built-in regulator is limited.

● Unused pin Treatment

Following table shows how to haldle unused pins.

Unused pins	Recommended treatment
V1 to V8	Pull down
ISENSE	Pull down
CDLY、CDOV、CDUV	Open
/DOFF, /VMEN	Tied to the VREG pin
VNTC	Tied to the TSNS pin through 4.7kΩ resistor
TSNS	Pull down with a 10kΩ resistor

● Selectiong range of Number of battery cells

Number of Connected Battery Cells is selected from two preset numbers. Preset number is from 5 to 13.

CS pin level	Setting range (connected cells)								
GND	5	6	7	8	9	10	11	12	13
VREG	5	6	7	8	9	10	11	12	13

● Detection voltage, setting range and step width

Presetting range of each detection voltage is shown below.

Detection voltage	Symbol	Setting range	Setteing step witdth
Overvoltage detecttion	V_{OV}	3.65V to 4.35V	25mV
Overvoltage release	V_{OVR}	3.5V to 4.25V	25mV
Undervoltge detection	V_{UV}	1.5V to 3.0V	100mV
Undervoltge relase	V_{UVR}	2.3V to 3.5V	100mV
Charge overcurrent detection	V_{OCO}	-30mV to -100mV	10mV
Discharge overcurrent detection	V_{OCU}	50mV to 300mV	50mV
Short circuit detection	V_{SHRT}	100mV to 600mV	100mV
High Temperature discharge inhibition	V_{DHD}	0.6V to 1.2V	10mV
High Tempearture charge inhibition	V_{CHD}	0.7V to 1.3V	10mV
Low Temperature charge inhibition	V_{CCD}	2.0V to 2.2V	10mV

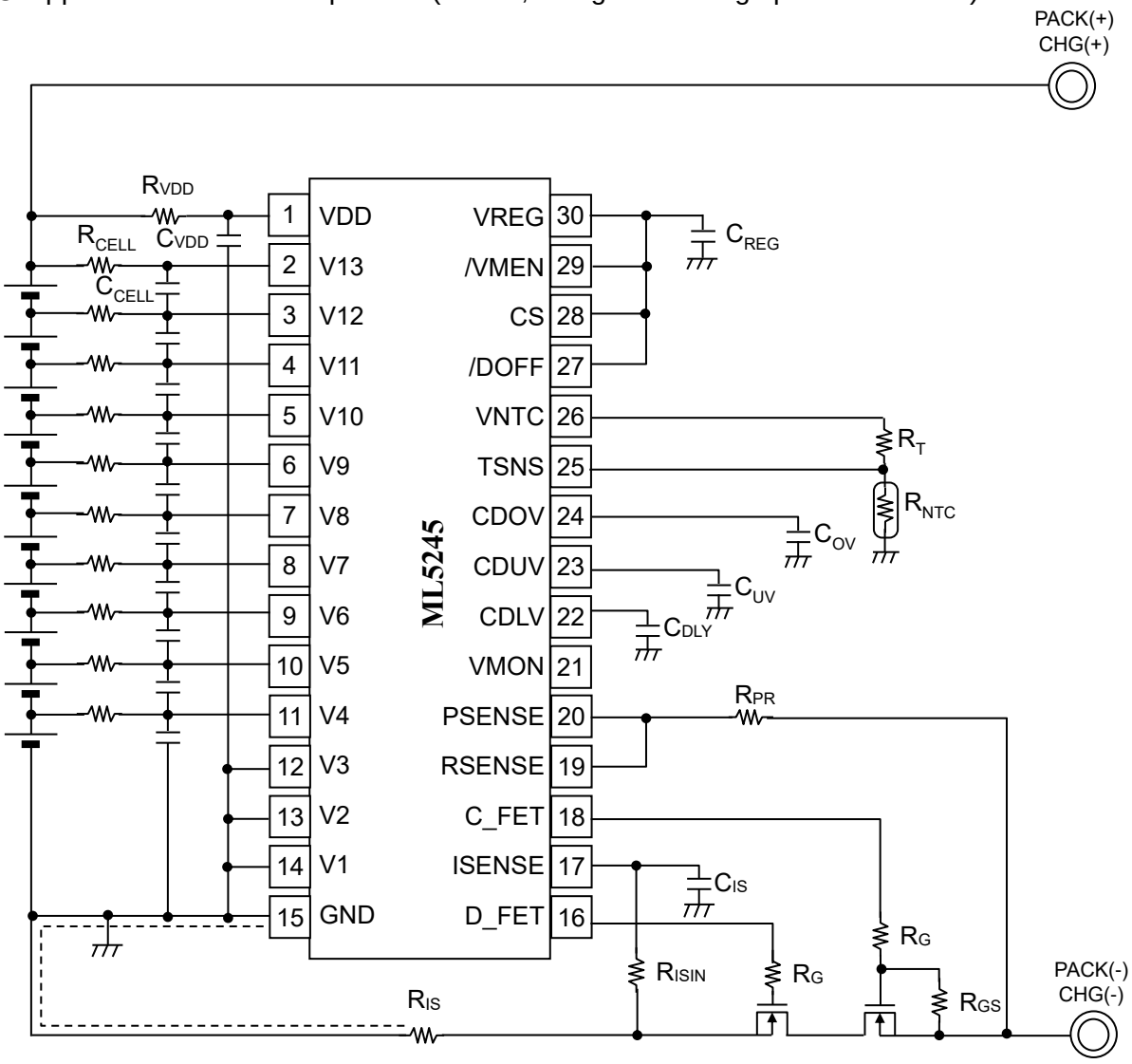
● Overcurrent detection delay time setting range

Presetting range of charge / discharge overcurrent detection delay time is shown beloe.

Detection delay time	Symbol	Setting value [ms]						
Discharge overcurrent detection delay time	t_{OCU}	25	50	100	200	300	400	500
		600	800	1000	1200	1600	2000	—
Charge overcurrent detection delay time	t_{OCO}	25	50	100	200	300	400	500
		600	800	1000	1200	1600	2000	—

■ Application Circuit Example

● Application Circuit Example 1 (10 cell, charge / discharge path is common)



The wire length indicated by a dotted line should be minimized, because the voltage drop due to wire resistance may affect the current detection accuracy.

■ Recommended Values for External Components

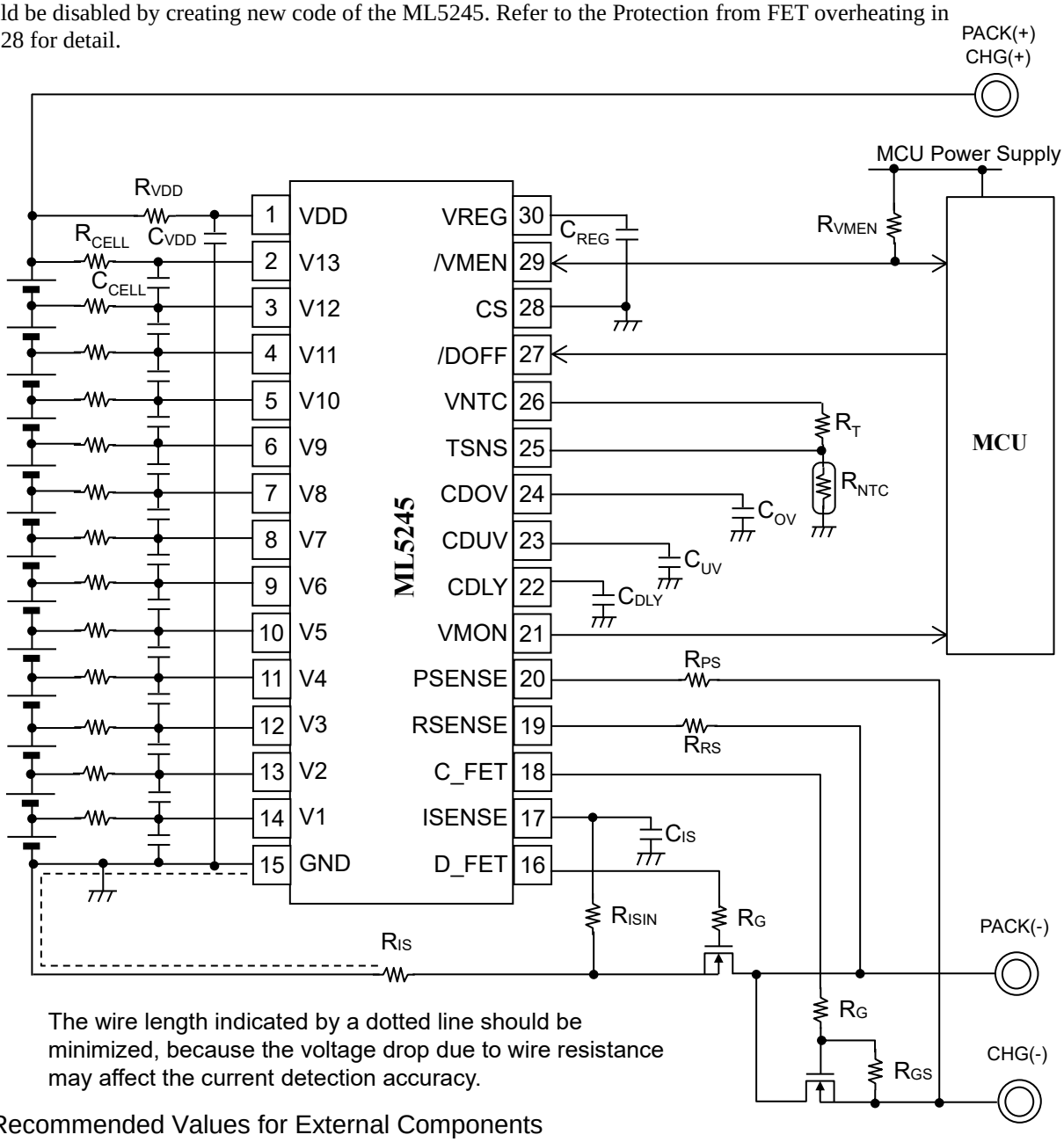
Component	Recommended value
R_{VDD}	510Ω
C_{VDD}	10μF or mode
R_{CEL}	1kΩ to 10kΩ
C_{CEL}	0.1μF or more
C_{REG}	1μF or more
C_{IS}	10nF
C_{DLY}	1nF to 10nF

Component	Recommended value
R_{IS}	3mΩ
R_{ISIN}	1kΩ
R_G,R_{PR}	10kΩ to 47kΩ
R_{GS}	1MΩ
R_T	4.7kΩ
R_{NTC}	10kΩ, B3435

(Note) This circuit example and the recommended values of external components are not always warranted. Evaluation on customer's application is required and select circuit and parts depend on customer's application.

● Application Circuit Example2 (13 cell, charge / discharge path is separated)

If battery discharging is enabled in the charging state, charge FET's protection function from overheating should be disabled by creating new code of the ML5245. Refer to the Protection from FET overheating in page28 for detail.



The wire length indicated by a dotted line should be minimized, because the voltage drop due to wire resistance may affect the current detection accuracy.

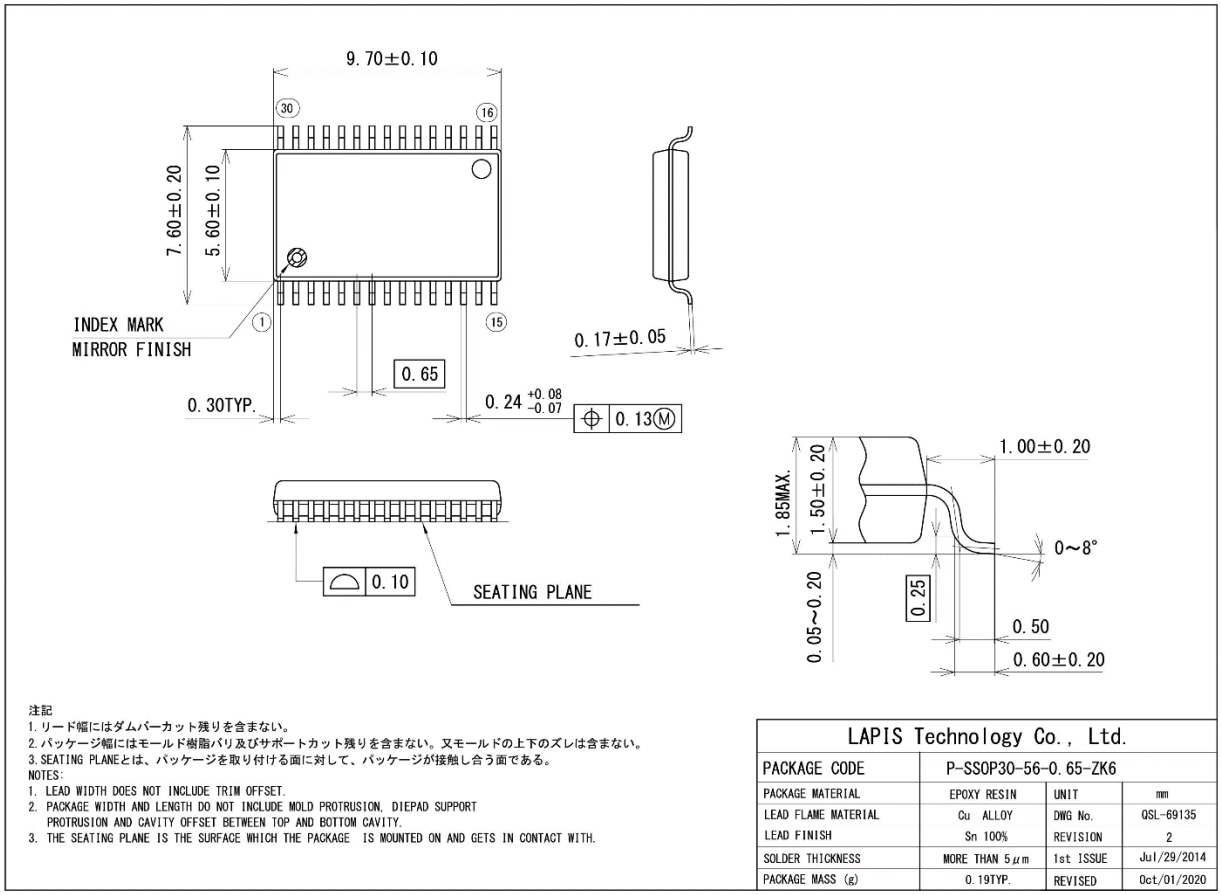
■ Recommended Values for External Components

Component	Recommended Value
R_{VDD}	510Ω
C_{VDD}	10μF or more
R_{CEL}	1kΩ to 10kΩ
C_{CEL}	0.1μF or more
C_{REG}	1μF or more
C_{IS}	10nF
C_{DLY}	1nF to 10nF

Component	Recommended Value
R_{IS}	3mΩ
R_{ISIN}	1kΩ
R_G,R_{PS}, R_{RS}	10kΩ to 47kΩ
R_{GS}	1MΩ
R_T	4.7kΩ
R_{NTC}	10kΩ, B3435
R_{VMEN}	100kΩ

(Note) This circuit example and the recommended values of external components are not always warranted. Evaluation on customer's application is required and select circuit and parts depend on customer's application.

■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-SSOP30-56-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69135
LEAD FINISH	Sn 100%	REVISION	2
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.19TYP.	REVISED	Oct/01/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to heat applied in solder reflow and moisture absorbed during storage. Please contact your local ROHM sales representative for recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

■ Revision History

Document No.	Issue date	Page		Revision description
		Before revision	After revision	
FEDL5245-01	2017.10.12	-	-	V1 issued.
FEDL5245-02	2017.12.1	9	9	In the Cell voltage monitor output characteristics, the VMON output voltage at 25°C is added.
FEDL5245-03	2019.08.22	28	28	PSENSE pin status in undervoltage is modified from “No change” to “Pull up”.
FEDL5245-04	2019.09.02	14	14	Timing chart: Charge overcurrent detection and recovery from charge overcurrent state by charger removal, mistype is corrected.
FEDL5245-05	2020.12.01	-	-	Changed Company name
		36	36	Changed “Notes”
FEDL5245-06	Jan. 9, 2024	1	1	Add Application Part number, Delete notes
		36	36	Add Notes

Notes

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