Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5248

7-Series Cell Li-ion Rechargeable Battery Protection analog-front-end IC

■ General Description

The ML5248 is a analog-front-end protection IC for the 7-cell Li-ion rechargeable battery pack. It has individial cell voltage monitoring and charge/discharge current monitoring function, and external MCU controls each cell overcharge/undervoltage protection and overcurrent protection.

And the ML5248 detects short current without external MCU and automatically turns on or turns off the external charege/discharge NMOS-FET.

■ Features

- 3 to 7 cell high precision cell voltage monitoring function : output cell voltage multiplied by 0.5 from VMON pin
- Built-in cell balancing switch on each cell : Switch ON resistance 6Ω(typ)
- charge/discharge current monitoring function :
  IMON pin outputs ISP-ISM voltage amplified by selected rate.
  Voltage amplifying rate selection: 10 / 50
- short-current protection function :
  Detection threshold voltage is selected from; ISP-ISM pin voltage =50mV/100mV/150mV/200mV(typ)
- external charge/discharge FET control : Built-in gate driver for highside NMOS-FET
- MCU interface : I2C compatible serial interface
- Built-in 3.3V regulator for and external MCU : 10mA (max) output current
- Built-in voltage reference for extrernal ADC (2.5V) : output currnet 100μA (max)
- PSNS/DFS pin voltage monitoring function
- Low current consumption
  Operating state : 32μA(typ), 65μA（max）
  Power-save state : 2μA(typ), 10μA(max)
  Power-down state : 0.1μA(typ), 1μA(max)
- supply voltage : +5V to +31.5V
- operating temperature : -40℃ to +85℃
- package : 30 pinSSOP (P-SSOP30-56-0.65-ZK6)

■ Application

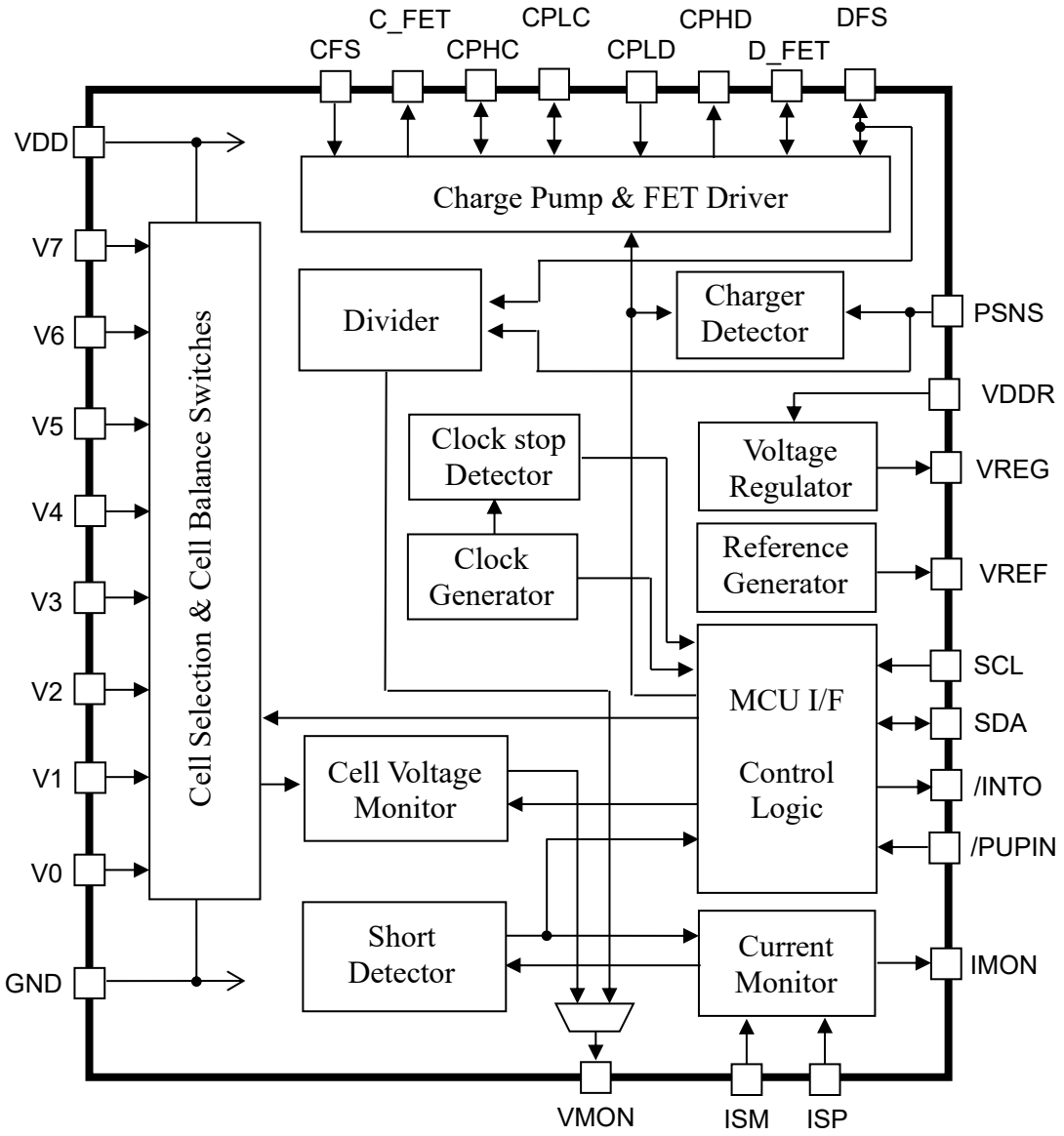
・Power tools and Garden tools
・Cordless Cleaner

■ Part number

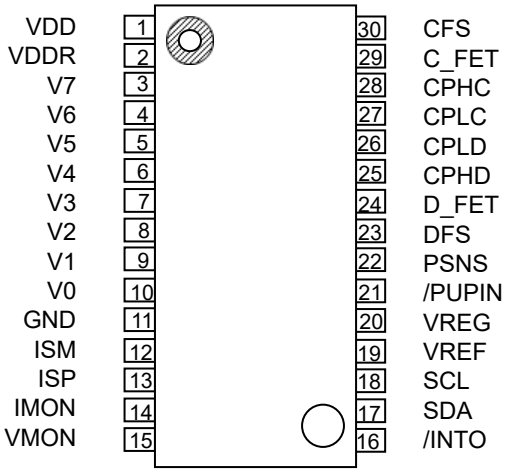
ML5248MB

ROHM SEMICONDUCTOR

■ Block Diagram



■ Pin Configuration (Top View)



■ Pin Description

Pin No.	Pin	I/O	Description
1	VDD	—	Power supply input pin. Connect an external CR filter for noise rejection.
2	VDDR	—	Power supply input pin only for internal regulator. Connect an external CR filter for noise rejection.
3	V7	I	Battery cell 7 positive terminal voltage input pin.
4	V6	I	Battery cell 7 negative terminal voltage input and battery cell 6positive terminal voltage input pin.
5	V5	I	Battery cell 6 negative terminal voltage input and battery cell 5 positive terminal voltage input pin.
6	V4	I	Battery cell 5 negative terminal voltage input and battery cell 4 positive terminal voltage input pin.
7	V3	I	Battery cell 4 negative terminal voltage input and battery cell 3 positive terminal voltage input pin. Should be connected to GND for the 3 cell series connected battery pack application.
8	V2	I	Battery cell 3 negative terminal voltage input and battery cell 2 positive terminal voltage input pin. Should be connected to GND for the 3 to 4cell series connected battery pack application.
9	V1	I	Battery cell 2 negative terminal voltage input and battery cell 1 positive terminal voltage input pin. Should be connected to GND for the 3 to 5 cell series connected battery pack application.
10	V0	I	Battery cell 1 negative terminal voltage input pin. Should be connected to GND for the 3 to 6 cell series connected battery pack application.
11	GND	—	Ground pin.
12	ISM	I	Current sense resistor negative terminal voltage input pin. Connected to the negative terminal of the most negative battery cell.
13	ISP	I	Current sense resistor positive termimal voltage input pin. The ISP pin level should be higher than the ISM pin level in discharge state.
14	IMON	O	Current monitor output pin. ISP-ISM voltage multiplied by 10/50 is outputted.
15	VMON	O	Cell voltage monitor output pin and PSNS and DFS pin voltage monitor pin. For cell voltage monitor, cell voltage multiplied by 0.5 is outputted. For PSNS and DFS pin voltage monitor, each voltage multiplied by 1/16 is outputted.
16	/INTO	O	Interrupt output pin for externla MCU. NMOS open drain output and output level is “L” if interrupt is asseerted.
17	SDA	IO	Serial interface data input/output pin. Should be pulled up externally.
18	SCL	I	Serial interface clock input pin. Should be pulled up externally.
19	VREF	O	2.5V reference level output . Shold be tied to GND through a 4.7µF capacitor.
20	VREG	O	Built-in 3.3V regulator output. Should be tied to GND through a 4.7µF capacitor. This pin can be used as power supply for an external MCU.
21	/PUPIN	I	Power-up trigger input pin. If input is “L” level, the state changes from power-down state to power-up state. A 1MΩ pull-up resistor is built-in between this pin and the VDD pin. should be connected capacitor larger than 0.1µF between this pin and the GND pin.
22	PSNS	I	Input pin for detecting the charger connection in power-down state. If the PSNS pin voltage is higher than VDD/2, this LSI power-up. The VMON pin can output the voltage of this pin multiplied by 1/16.

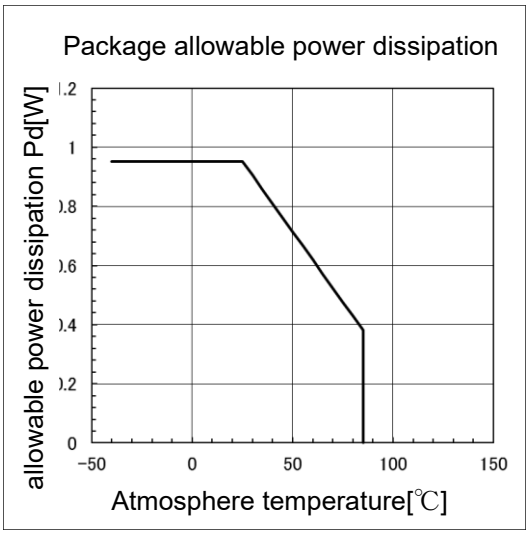
Pin No.	Pin	I/O	Description
23	DFS	I	D_FET pin charge pump reference voltage input pin. Should be tied to source pin of the extrernal charge/dischrarge Nch-FET. The VMON pin can output the voltage of this pin divided by 16.
24	D_FET	O	Discharge Nch-FET control signal output pin. should be tied to the gate pin of the external Nch-FET. If this output is “ON”, output level is DFS pin voltage of +11V(typ), and if this output is “OFF”, output level is DFS pin voltage.
25	CPHD	O	Charge pump capacitor for D_FET drive is connected. Connect a capacitor with approximately twice the gate capacitance of the discharge Nch-FET, between the CPHD and CPLD pins.
26	CPLD	O	
27	CPLC	O	Charge pump capacitor for C_FET drive is connected. Connect a capacitor with approximately twice the gate capacitance of the charge Nch-FET, between the CPHC and CPLC pins.
28	CPHC	O	
29	C_FET	O	Charge Nch-FET control signal output pin. Should be tied to the gate pin of the external Nch-FET. If this output is “ON”, output level is CFD pin voltage of +11V(typ), and if this output is “OFF”, output level is CFS pin voltage.
30	CFS	I	C_FET pin charge pump reference voltage input pin. should be tied to to source pin of the external charge/discharge Nch-FET.

■ Absolute Maximum Ratings

(GND= 0 V, Ta = 25 °C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD, VDDR pins	−0.3 to +50	V
Input voltage	V_{IN1}	Applied to V7 to V0 pins Vn+1 – Vn pin voltage difference (Note1), V0 – GND pin voltage difference	−0.3 to +6.5	V
	V_{IN2}	Applied to CFS,DFS,PSNS pins	−0.3 to 50	V
	V_{IN3}	Applied to /PUPIN pin	−0.3 to V_{DD}+0.3	V
	V_{IN4}	Applied to ISM, and ISP pins	−0.3 to V_{REG}+0.3	V
	V_{IN5}	Applied to SCL, SDA pins	−0.3 to +4.8	V
Output voltage	V_{OUT1}	Applied to D_FET pin V_{DFS}=DFS pin voltage	V_{DFS}−0.3 to +50.0	V
	V_{OUT2}	Applied to C_FET pin V_{CFS}=CFS pin voltage	V_{CFS}−0.3 to +50.0	V
	V_{OUT3}	Applied to SDA, /INTO and VREG pins	−0.3 to +4.8	V
	V_{OUT4}	Applied to VMON, IMON and VREF pins	−0.3 to V_{REG}+0.3	V
Short-circuit output current	I_{OS}	If VDD=36.5V, Applied to VREG, VREF, SDA, /INTO, VMON, IMON, C_FET and D_FET	20	mA
Cell balancing current	I_{CB}	Per one cell balancing switch	100	mA
Allowable Power dissipation	P_D	Ta=25℃	0.95	W
Junction emperature	Tj_{MAX}	—	125	°C
Package thermal resistance	θ ja	JEDEC 2 layer board	105	℃/W
Storage temperature	T_{STG}	—	−55 to +150	°C

Note : When battery connecting and disconnecting , Vn+1 – Vn pin voltage may exeed absolute maximum rating and it may damage input pins. It is suggested enough evaluation.



Package allowable power dissipation decreases as the atmosphere temperature (Ta) increase. If VREG pin output load current is large, make the power loss smaller than the value shown in this figure.

■ Recommended Operating Conditions

Item	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	Applied to VDD, VDDR pins	5～31.5	V
Operating temperature	Ta	If VREG output no-loaded	−40～85	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD}=5 to 31.5V, GND=0 V, Ta=−40 to 85°C, VREG output no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (Note 1)	V_{IH}	—	0.8 × V_{REG}	—	V_{REG}	V
Digital "L" input voltage (Note 1)	V_{IL}	—	0	—	0.2 × V_{REG}	V
/PUPIN pin ”H” input voltage	V_{IHP}	—	0.8 × V_{DD}	—	V_{DD}	V
/PUPIN pin ”L” input voltage	V_{ILP}	—	0	—	0.2 × V_{DD}	V
Digital "H" input current (Note 1)	I_{IH}	V_{IH} = V_{REG}	—	—	2	µA
Digital "L" input current (Note 1)	I_{IL}	V_{IL} = GND	–2	—	—	µA
/PUPIN pin ”H” input current	I_{IHP}	V_{IH} = V_{DD}	—	—	2	µA
/PUPIN pin ”L” input current	I_{ILP}	V_{DD}=31.5V, V_{IL} = GND	–70	−32	−11	µA
Digital "L" output voltage (Note 2)	V_{OL}	I_{OL}=1mA	0	—	0.2	V
Digital output leakage current (Note 2)	I_{OLK}	V_{OH}=3V V_{OL}=0V	–2	—	2	µA
Cell monitoring pin Input current (Note 3)	I_{INVC}	When measuring battery cell voltage, Cell balancing switches are off	−1.5	—	5	µA
Cell monitoring pin Input leakage current (Note 3)	I_{ILVC}	Except when measuring battery cell voltage, Cell balancing switches are off	−1.5	—	1.5	µA
FET “H” output voltage (Note 4)	V_{OHF}	I_{OH}=−1µA V_{DD}=V_S=16V to 31.5V V_S: CFS, DFS pin voltage	V_S+8	V_S+11	V_S+13.5	V
FET “L” output voltage (Note 4)	V_{OLF}	I_{OL}=1µA V_{DD}=V_S=16V to 31.5V V_S: CFS, DFS pin voltage	V_S	—	V_S+0.3	V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VREG output voltage	V_{REG}	If output is no loaded	3.0	3.3	3.6	V
	V_{REG1}	10V＜V_{DD}＜31.5V Output load current ＜ 10mA	3.0	3.3	3.6	V
	V_{REG2}	5V＜V_{DD}＜10V Output load current＜ 5mA	3.0	3.3	3.6	V
VREF output voltage	V_{REF1}	Ta＝0～60℃ Output load current＜ 100uA	2.485	2.50	2.515	V
	V_{REF2}	Ta＝－40～85℃ Output load current＜ 100uA	2.45	2.50	2.55	V
VREG low voltage Detection voltage	V_{RD}	—	2.2	2.45	2.7	V
VREG low voltage Release voltage	V_{RR}	—	2.4	2.75	3.0	V
Cell balancing switch ON resistance	R_{BL}	Internal balancing FET V_{DS}=0.3V V_{DD}=16V to 31.5V	2.5	6	12	Ω

Note 1: Applied to SCL, SDA pins
Note 2: Applied to SDA, /INTO pins
Note 3: Applied to V7 to V0 pins
Note 4: Applied to C_FET, D_FET pins

● Supply Current Characteristics

V_{DD}=5 to 31.5V, GND=0 V, Ta=－40 to 85°C, VREG, VREF output no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in operation	I_{DD1}	No output loaded VMEN bit=”1” IMEN bit=”1” ENSC bit=”1”	—	32	65	μA
Current consumption in Power save	I_{DD2}	No output loaded	—	2	10	μA
Current consumption in power down	I_{DDS}	No output loaded	—	0.1	1.0	μA

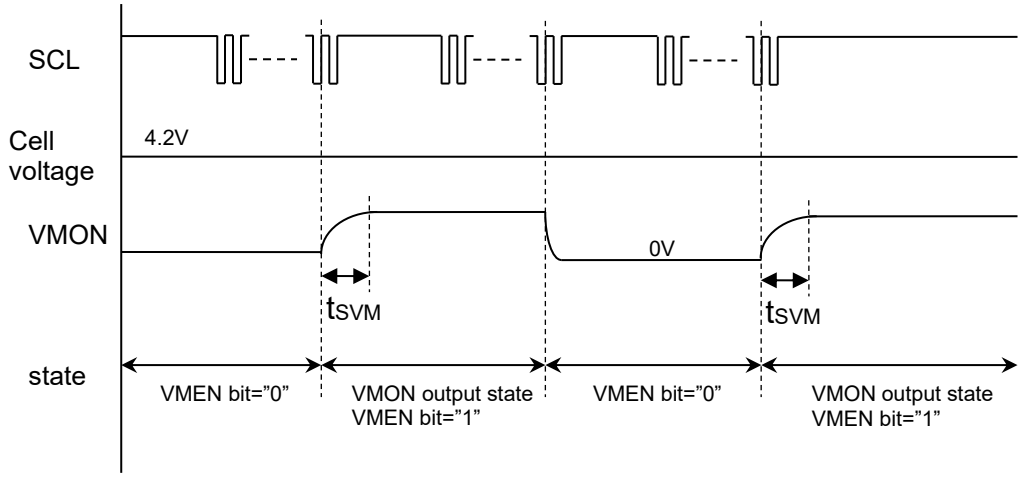
(Note) These current consumption are sum of two current, VDD pin and VDDR pin.

● Cell Voltage Monitor Output Characteristics (Ta=0～60℃)

V_{DD}=28V, GND=0V, Ta=0 to 60°C, VMON output no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage monitor range	V_{VMR}	—	0.1	—	4.5	V
VMON output voltage (when cell voltage monitoring)	V_{VMC4}	Cell voltage=4.2V No output loaded	2.05	2.10	2.15	V
	V_{VMC1}	Cell voltage =1V No output loaded	0.4	0.50	0.6	V
Cell voltage measurement accuracy (Note1)	V_{ECEL4}	Cell voltage =4.2V No output loaded	-20	—	+20	mV
	V_{ECEL1}	Cell voltage =1V No output loaded	-30	—	+30	mV
VMON output current	I_{OVM}	—	-100	—	+100	μA
VMON output settling time (when cell voltage monitoring)	t_{SVM}	No output loaded	—	—	1	ms

(Note 1) In case if corrected by calculation below with values stored in VGAIN register and OFFSET register.
Cell voltage＝VGAIN × [VMON output voltage] + OFFSET

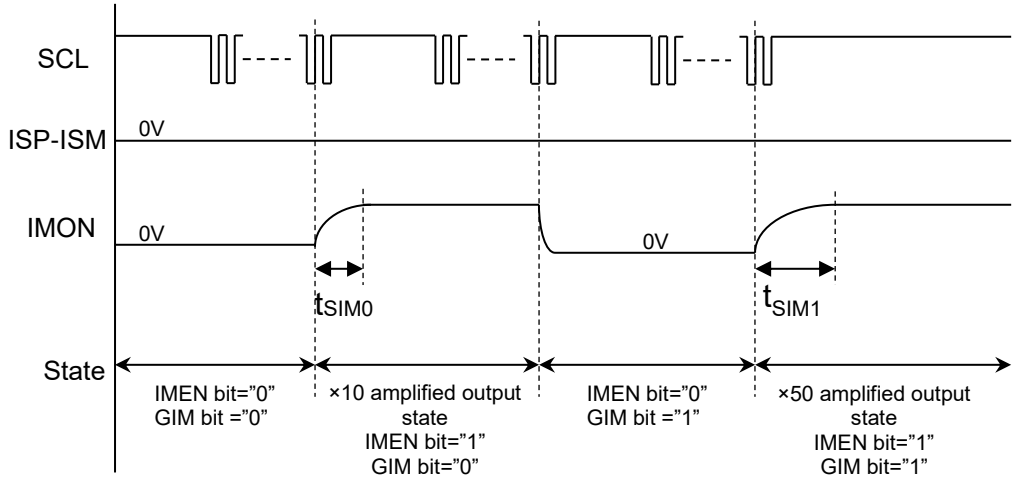


● Current monotor output characteristic (Ta=0 to 60℃)

V_{DD}=28V, GND=0V, Ta=0 to 60°C, shunt resistor=1mΩ, IMON output no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current monitor range (Note1)	I_{MR1}	GIM bit = “0”	-180	—	36	A
	I_{MR0}	GIM bit = “1”	-30	—	6	A
IMON output voltage	V_{IMON0}	ISP-ISM voltage difference =0V GIM bit=”0”	0.4	0.5	0.6	V
	V_{IMON1}	ISP-ISM voltage difference =0V GIM bit=”1”	0.2	0.5	0.8	V
IMON output voltage amplify rate (Note 2)	G_{IM0}	GIM bit=”0”	9.5	10	10.5	V/V
	G_{IM1}	GIM bit=”1”	47.5	50	52.5	V/V
IMON output current	I_{OIM}	—	-100	—	+100	μA
ISP、ISM pin input current (Note 2)	I_{IS}	ISP=SIM=0V GIM bit = “0” ZERO bit=”0”	0.05	0.46	1.2	μA
IMON output settling time	t_{SIM0}	GIM bit=”0”	—	—	1	ms
	t_{SIM1}	GIM bit=”1”	—	—	3	ms

(Note1) Current monitor range is positive in charging.
(Note2) When 1kΩ resistors are connected to ISP pin and ISM pin each.



● Detection Threshold Characteristics (Ta=25℃)

V_{DD}=31.5V, GND=0 V, Ta=25°C, VREG output no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Short circuit detection threshold	V_{SHRT0}	SC1,SC0 bit=(0,0)	30	50	70	mV
	V_{SHRT1}	SC1,SC0 bit=(0,1)	85	100	115	mV
	V_{SHRT2}	SC1,SC0 bit=(1,0)	135	150	165	mV
	V_{SHRT3}	SC1,SC0 bit=(1,1)	185	200	215	mV
Short circuit detection delay time (Note1)	t_{SHRT0}	TD1,TD0 bit=(0,0)	75	100	125	µs
	t_{SHRT1}	TD1,TD0 bit=(0,1)	150	200	250	µs
	t_{SHRT2}	TD1,TD0 bit=(1,0)	225	300	375	µs
	t_{SHRT3}	TD1,TD0 bit=(1,1)	300	400	500	µs

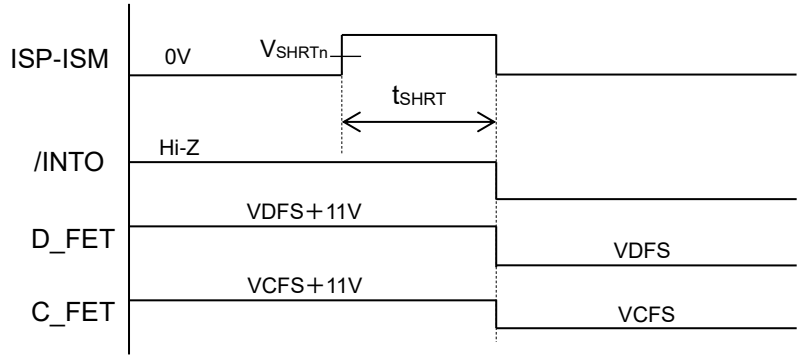
Note1) Short circuit detection delay time assumes that there is no capacitor between ISM-ISP.

● Detection Threshold Characteristics (Ta=0 to 60℃)

V_{DD}=31.5V, GND=0 V, Ta=0 to 60°C, VREG output no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Short circuit detection threshold	V_{SHRT0}	SC1,SC0 bit=(0,0)	30	50	70	mV
	V_{SHRT1}	SC1,SC0 bit=(0,1)	80	100	120	mV
	V_{SHRT2}	SC1,SC0 bit=(1,0)	130	150	170	mV
	V_{SHRT3}	SC1,SC0 bit=(1,1)	180	200	220	mV
Short circuit detection delay time (Note1)	t_{SHRT0}	TD1,TD0 bit=(0,0)	50	100	150	µs
	t_{SHRT1}	TD1,TD0 bit=(0,1)	100	200	300	µs
	t_{SHRT2}	TD1,TD0 bit=(1,0)	150	300	450	µs
	t_{SHRT3}	TD1,TD0 bit=(1,1)	200	400	600	µs

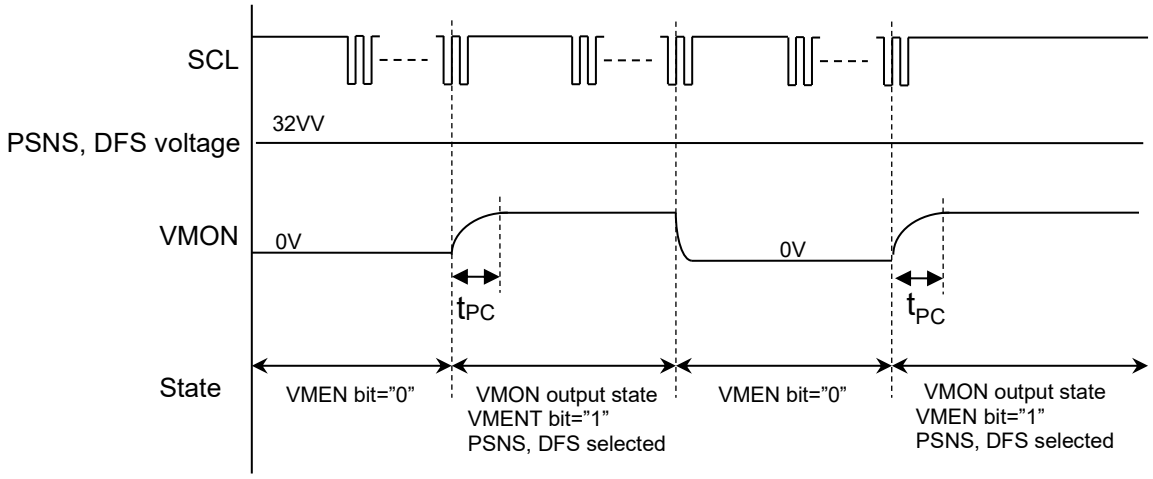
Note1) Short circuit detection delay time assumes that there is no capacitor between ISM-ISP.



● PSNS, DFS Pin Monitor Output Characteristic and Charger Detecting Voltage Characteristic (Ta=0 to 60℃)

V_{DD}=31.5V, GND=0 V, Ta=0 to 60°C, VREG output lo-loaded

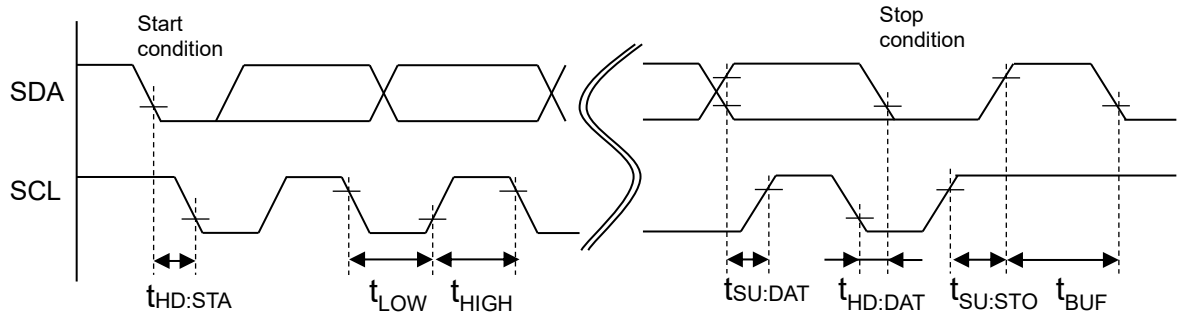
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VMON output voltage, PSNS, DFS pin monitoring	V_{PCO}	Input voltage = 32V	1.9	2.0	2.1	V
VMON output voltage settling time, PSNS, DFS pin monitoring	t_{PC}	Input voltage = 32V	—	—	(3	ms
Charger detection PSNS voltage	V_{PC}	Power-up from power down state	V_{DD}X0.2	V_{DD}X0.5	V_{DD}X0.8	V
PSNS pull-down resistor	R_{PD}	PSNS pin voltage is not monitored	200	500	1000	kΩ
DFS pull-up resistor	R_{PU}	DFS pin voltage is not measured	0.5	2	4	kΩ
PSNS pin voltage monitoring pull-down resistor	R_{DM1}	Pull-down resistor is removed (register PD=”0”)	8	20	50	MΩ
DFS pin voltage monitoring pull-down resistor	R_{DM2}	Pull-up resistor is removed (register PU=”0”)	8	20	50	MΩ
PSNS input current leakage	I_{LPS}	Pull-down resistor is removed. PSNS pin voltage is not monitored	-2	—	2	µA
DFS input current leakage	I_{LFS}	Pull-up resistor is removed. D_FET=OFF DFS pin voltage is not monitored	-2	—	2	µA



● AC Characteristic

V_{DD}=5 to 31.5V, GND=0 V, Ta=−40 to 85°C, VREG ouptput no-loaded

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	—	—	—	400	kHz
SCL hold time (start condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL “L” hold time	t_{LOW}	—	1.3	—	—	µs
SCL “H” hold time	dt_{HIGH}	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus free time	t_{BUF}	—	1.3	—	—	µs
/PUPIN “L” pulse width	t_{PUP}	—	1	—	—	ms

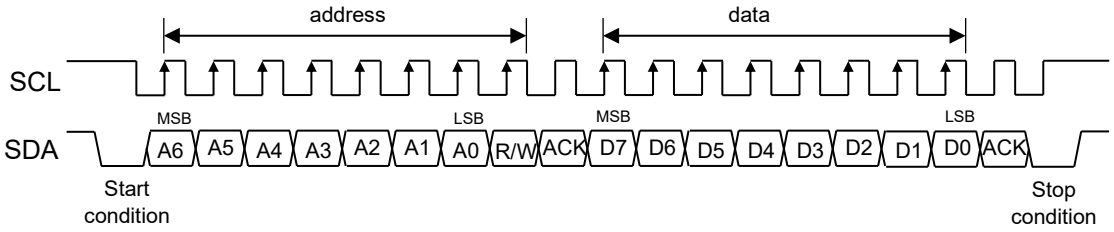


■ Functional Description

● I2C compatible serial Interface

The ML5248 is equipped with the I2C compatible serial interface. This interface is not fully compatible with I2C communication format, and it doesn't have slave address, the MCU communication is one-to –one.

Setting and control is executed by writing/reading control registers.



To write data set the RW bit "0", to read data set the RW bit "1"

● Control Register

The control register map is shown below.

address	Register name	R/W	Default	Description
00H	NOOP	R/W	00H	No function assigned
01H	VMON	R/W	00H	Cell voltage and PSNS/DFS pin voltage monitoring control
02H	IMON	R/W	00H	Current measurement control
03H	FET_INT	R/W	00H	FET control, interrupt control
04H	POWER	R/W	00H	Power-save/ power-down control
05H	CBAL	R/W	00H	Cell balancing contorl
06H	SETSC	R/W	00H	Short circuit detection control
07H	VGAIN	R	—	VMON output voltage gain correction
08H	OFFSET	R	—	VMON output voltage offset correction
09H	VREFOF	R	—	VREF output voltage offset correction
other	TEST	R/W	00H	test(don't use)

1. NOOP register（Adrs=00H）

	7	6	5	4	3	2	1	0
Bit	NO7	NO6	NO5	NO4	NO3	NO2	NO1	NO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

No function is assigned to the NOOP register. Read/write access to this register does not change the LSI status. The written data can be read as it is.

2. VMON register（Adrs=01H）

	7	6	5	4	3	2	1	0
Bit	—	—	—	VMEN	VM3	VM2	VM1	VM0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
dafault	0	0	0	0	0	0	0	0

VMON register select the voltage measuring battery cell number, select which pin voltage of PSNS or DFS to output from VMON pin.

VM0, VM1, VM2, VM3 select the battery cell voltage or PSNS pin or DFS pin voltage divided by 16, and VMEN bit enables VMON pin to output selected voltage.

VMEN	VM3	VM2	VM1	VM0	Selected battery cell
0	—	—	—	—	VMON pin=0V(default)
1	0	0	0	0	VMON pin=0V(default)
1	0	0	0	1	V1 cell (lowest)
1	0	0	1	0	V2 cell
1	0	0	1	1	V3 cell
1	0	1	0	0	V4 cell
1	0	1	0	1	V5 cell
1	0	1	1	0	V6 cell
1	0	1	1	1	V7 cell (uppsermost)
1	1	0	0	0	PSNS divided
1	1	0	0	1	DFS divided

3. IMON register（Adrs=02H）

	7	6	5	4	3	2	1	0
bit	—	—	—	IMEN	—	—	ZERO	GIM
R/W	R	R	R	R/W	R	R	R/W	R/W
default	0	0	0	0	0	0	0	0

IMON register controls current measurement and its conditions.
The GIM bit selects the volgtage gain of the current measurement amplifier.

GIM	Voltage gain G_{IM}
0	10 times (default)
1	50 times

The ZERO bit executres zero correntions of the current measurement amplifier.

ZERO	ISP input	ISM input
0	Pin input level	Pin input level
1	GND revel	GND level

The IMEN bit enables current measuring amplifiere result to output from IMON pin. If zero correnction and gain correction is held, IMEN bit is set “1”.

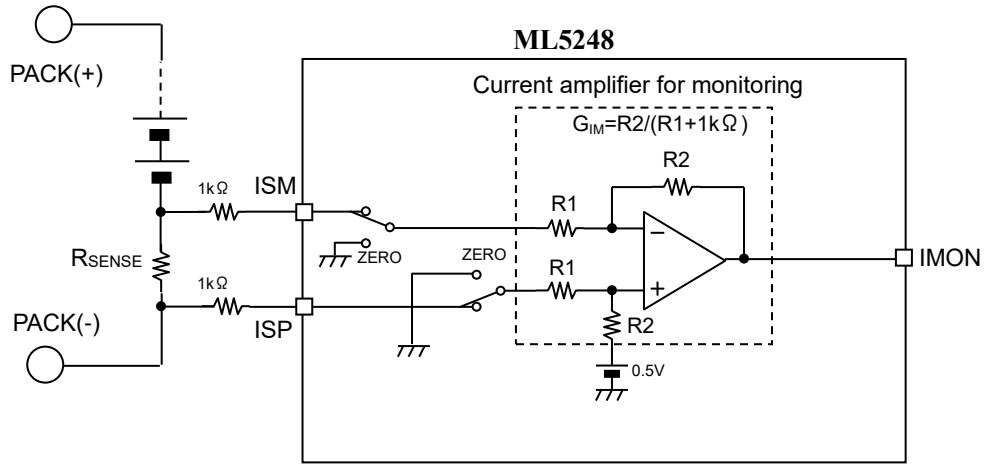
IMEN	IMON pin output
0	0V(default)
1	Current measuring amplifier output

Current measurement is executed with current sensing resistor R_{SENSE} connected between ISP and ISM pins, and measure input voltage difference of these pins.

Voltage difference between ISP and ISM pins is converted to voltage, its center is 0.5V(typ.), and output from IMON pin. IMON pin output voltage V_{IMON} is geven by the following equation with the current sensing resistor R_{SENSE} and its current I_{SENSE}.

$$V_{IMON} = (I_{SENSE} \times R_{SENSE}) \times G_{IM} + 0.5$$

The current measuring amplifier circuit is shown below.

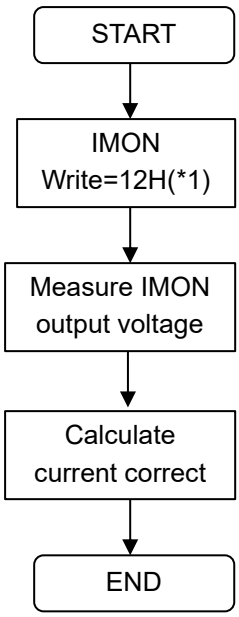


If the current is zero, V_{IMON} = 0.5V in the discharging state, V_{IMON} > 0.5V in the charging state, V_{IMON} < 0.5V.

When the ZERO bit is set "1", the input of ISM pin and ISP pin is switched to GND level in the LSI and set the input voltage difference of the current measuring amplifier is set to zero. By setting the IMON pin output voltage in this state as the reference voltage of zero current, internal 0.5V reference voltage and offset voltage of amplifier are corrected.

Short current detection characteristic does not depend on the IMON register setting.

The example flowchart of calibration for current measuring amplifier is shown below.
(Voltage gain is 10)



Write IMON register “12H” (*1) and set the zero current state.

Measure the IMON pin output voltage of zero current state with external ADC. Store its result in the variable VIM0.

Zero correction is held with the variable.
Zero correction value V_{IMZ}=VIM0

If Current sensing resistor value=R_{SENSE}、IMON voltage measured value=$V_{IMON,}$ measured current I_{SENSE} is given with the following expression.

$$I_{SENSE} = (V_{IMON} - V_{IMZ}) / G_{IM} / R_{SENSE}$$

(*1) In order to set voltage gain 50, 13H is written in the IMON register.

4. FET_INT register（Adrs=03H）

	7	6	5	4	3	2	1	0
bit	INTO	—	DEDCK	DETSC	PU	PD	CF	DF
R/W	R	R	R	R	R/W	R/W	R/W	R/W
default	0	0	0	0	0	0	0	0

FET_INT register controls C_FET、D_FET turn ON/OFF, PSNS pin pull-down resistor connection, DFS pin pull-up resistor connection, and indicates intrerrupt requests.

DF bit sets the D_FET pin output state. If the short current is detected, the DF bit is automatically cleared to “0”. But even if the state is recovered from short current detection to normal state, this bit is not set “1” automatically, external MCU should set this bit “1”.

DF	Discharge FET	D_FET pin output
0	OFF（default）	DFS pin voltageV_{DFS}
1	ON	V_{DFS}+11V(typ)

CF bit sets the C_FET pin output state. If the short current is detected, the CF bit is automatically delaerd to “0”. But even if the state is recovered ftrom short current detection to normal state, this bit is not set “1” automatically, external MCU should set this bit “1”.

CF	Charge FET	C_FET pin output
0	OFF(default)	CFS pin voltageV_{CFS}
1	ON	V_{CFS}+11V(typ)

PD bit sets the PSNS pin pull-down resistor connection.

PD	PSNS pin
0	Pull-down removed (default)
1	500kΩ pull-down

PU bit sets the DFS pin pull-up resistor connection

PU	DFS pin
0	Pull-up removed (default)
1	2MΩ pull-up

DETSC bit indicates the /INTO pin output state when short circuit is detected.

DETSC	Short current detection interrupt state
0	No interrupt（default）
1	Interrupt occured(short current is detected)

DEDCK bit indicates the /INTO pin output state when internal clock stop was detected. If the internal clock stop is detected, DF bit and CF bit are automatically cleared to “0”. But even if the internal clock stop is not detected, DF bit and CF bit are not set “1” automatically, external MCU should set these bits “1”.

DEDCK	Clock stop detection interrupt state
0	No interrupt（default）
1	Interrupt occured(clock stop is detected)

INTO bit indicates the /INTO pin output state

INTO	/INTO pin output state
0	No interrupt（default）
1	Interrupt occured

After the FET_INT resister is read, each bit of INTO、DETSC、DEDCK is cleared to default value, and /INTO pin is set Hi-Z state.

5. POWER register（Adrs=04H）

	7	6	5	4	3	2	1	0
bit	PUPIN	—	—	PDWN	—	—	—	PSV
R/W	R	R	R	R/W	R	R	R	R/W
default	0	0	0	0	0	0	0	0

Power register control the power-down and the power-save.

PSV bit set the state transition to power save

PDWN	Power-save
0	Normal state（default）
1	Power-save state

If the PSV bit is set “1”, the state is changed to the Power-save state. In the power-save state, VMON, IMON, FET_INT, CBAL, and SETSC registers are initialized. Changing these registers is disabled.

When the PSV bit is cleared to “0”, the status is recovered from power-save state to the normal state, and setting the VMON, IMON, FET_INT, CBAL, and SETSC registers is enabled. Wait for the VREF output to be stable, before measuring actions.

Before setting the PDWN bit “1” to be into the Power-down state, power-save state should be cleared and the state is changed to the normal state,.

The state of each functions are shown below.

Function	Operation in the power-save state
VREG pin output	Same as the normal state, output 3.3V(typ)
VREF pin output	Stopped, output is 0V(typ)
MCU serial interface	Same as the normal state, register read/write is enabled. But VMON, IMON, FET_INT, CBAL, and SETSC bits are initrialized and write is disabled.
Cell voltage monitoring	Stopped
Current monitoring	Stopped
Short current detection	Stopped
PSNS, DFS pin monitoring	Stopped
Charge/discharge FET control	Stopped
Internal clock stop detection	Stopped
Cell balancing switches	All switches are OFF

PDWN bit set the state transition to power down

PDWN	Power-down
0	Normal state（default）
1	Power-down state

If the PDWN bit is set “1”, 500kΩ pull-down resistor is automatically connected to PSENSE pin in the LSI and all the circuit is stopped.

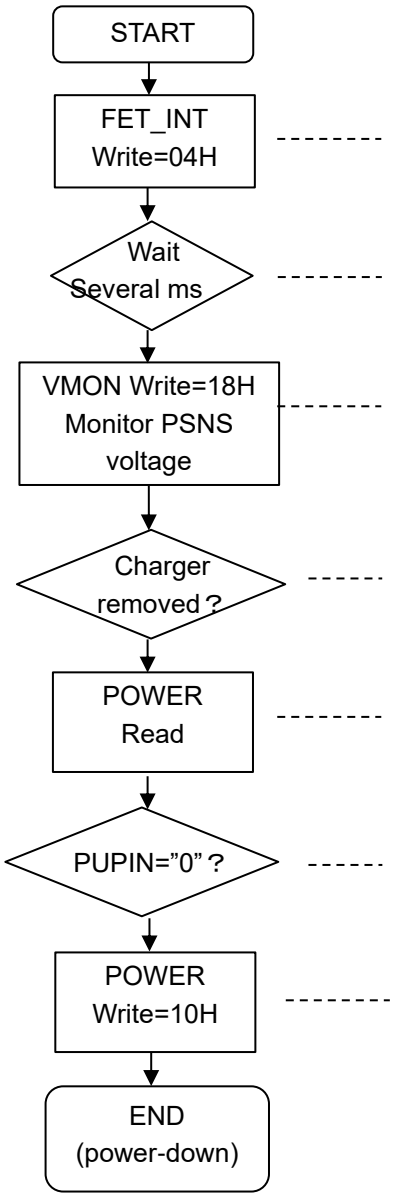
Before setting the PDWN bit “1”, C_FET and D_FET should be set OFF and charger disconnection should be confirmed with the PSENSE pin voltage. When the /PUPIN pin input is “L”, even if PDOWN bit is set to “1”, the state doesn’t get changed to power-down until the /PUPIN pin input rises to “H”. Before setting the PDWN bit “1”, it should be confirmed that /PUPIN pin is not “L” by reading the PUPIN bit which indicated /PUPIN pin state..

PUPIN	/PUPIN pin state
0	“H” level
1	“L” level

If charger connection is detected with PSENSE pin or if /PUPIN pin is asserted “L” input, the LSI is recovered from power-down state to normal state.

In the power down state, VREG output which is power supply for external micro-controller is set GND level. In recovering from power down state, every initial setting should be held after VREG has fully rised.

The example flow chart of powr-down is shown below.



Write FET register “04H” and set the C_FET and D_FET pins OFF. And in order to detect charger removal , connect 500kΩ(typ) pull-down resister to PSNS pin.

Wait for PSNS pin stable.

Write VMON register “18H” and monitor the VMON pin output voltage with external ADC to confirm that PSNS pin is not connected to charger.

Wait for PSNS pin voltage to be lower than V_{PC} to detect that charger is removed

Read the PUPIN bit of POWER register and confirm that the value is ”0” (/PUPIN pin is ”H”).

If the PUPIN bit =”1”, wait for PUPIN bit to be “0”, because setting PDWN bit =”1” is neglected if the PUPIN bit =”1”.

Write POWER register ”10H” to set the PDWN bit “1” and make the ML5248 power-down. In the power-down state, all the circuits are stopped and all the registers are initialized. The 500kΩ(typ) pull-down resistor is connected to the PSNS pin and wait for charger connection detection.

Output state of each pins in power-down state is shown below.

Pin name	State in power-down
VREG	0V
VREF	0V
/INTO	Hi-Z
C_FET	CFS pin lev
D_FET	DFS pin level

Recovering from power-down state is executed by charger connect detection by PSNS pin or “L” level linput to /PUPIN pin. If recovered from power-down state, wait for VREF and VREF become stable before each setttings.

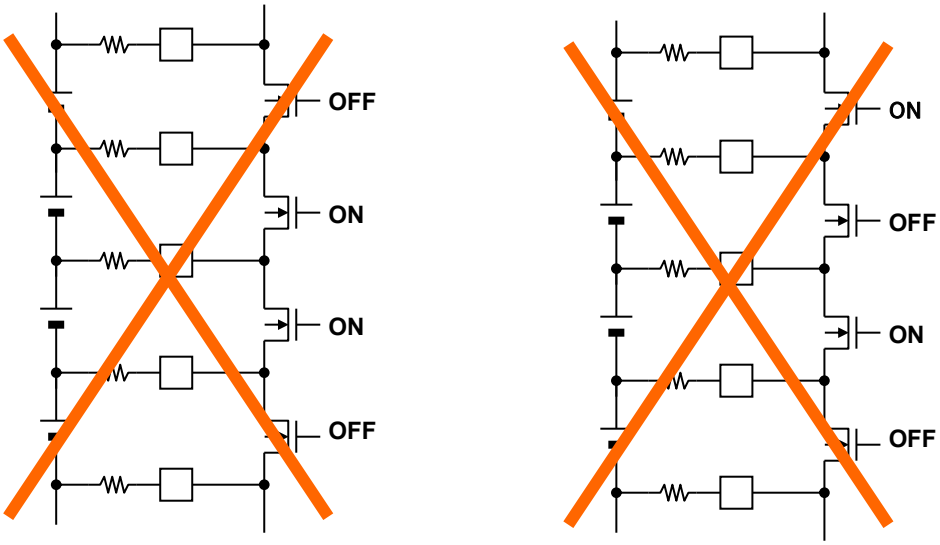
6. CBAL register（Adrs=05H）

	7	6	5	4	3	2	1	0
bit	—	SW7	SW6	SW5	SW4	SW3	SW2	SW1
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
default	0	0	0	0	0	0	0	0

CBAL register set the cell balancing switches ON/OFF.
SW7 to SW1 bit sets switches turning ON/OFF of each cell.

SW7	SW6	SW5	SW4	SW3	SW2	SW1	Switch ON/OFF
0	0	0	0	0	0	0	7cell OFF（default）
0	0	0	0	0	0	1	V1-V0 pin switch ON
0	0	0	0	0	1	0	V2-V1 pin switch ON
0	0	0	0	1	0	0	V3-V2 pin switch ON
0	0	0	1	0	0	0	V4-V3 pin switch ON
0	0	1	0	0	0	0	V5-V4 pin switch ON
0	1	0	0	0	0	0	V6-V5 pin switch ON
1	0	0	0	0	0	0	V7-V6 pin switch ON

More than one switch can be turned on in the same time, but following settings are inhibited because internal cell balancing switch might be broken.
(1) Side-by-side cell balancing switches are inhibited to be turned on in the same time.
(2) The cell balancing switches of both side of a cell balancing switch which is turned off is inhibited to be turned on in the same time.



As IC heats by cell balancing current and cell balancing switch resistor, restrict the number of switches of ON and time of ON, in order to keep the power consumption of cell balancing switch less than allowable power dissipation,

If cell voltage is outputted from VMON pin, the voltage of a cell whose cell balancing switch is turned on is measured as the voltage difference between two ports of cell balancing switch.

7. SETSC register（Adrs=06H）

	7	6	5	4	3	2	1	0
bit	ENSC	—	TD1	TD0	—	—	SC1	SC0
R/W	R/W	R	R/W	R/W	R	R	R/W	R/W
default	0	0	0	0	0	0	0	0

SETSC register sets the short current detecting voltage and short current detecting delay time.
Short current detecting voltage is selected with SC0 and SC1 bit depend on current sensing resistor value. While short current is detected, writing this register is inhibited.

SC1	SC0	Short current detecting voltage (ISP-ISM pin voltage)	Short current detecting current if current sending resistor value =1mΩ
0	0	50mV (default)	50A
0	1	100mV	100A
1	0	150mV	150A
1	1	200mV	200A

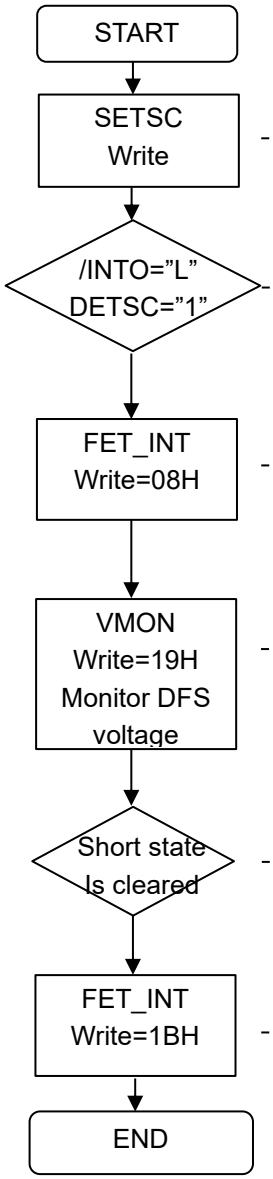
TD0, TD1 bits select the short current detecting delay ime. While short current is detected, writing this register is inhibited.

TD1	TD0	Short current detecting delay time
0	0	100μs (default)
0	1	200μs
1	0	300μs
1	1	400μs

ENSC bit sets the short current detection circuit run/stop.

ENSC	Short current detection circuit state
0	Stop (default)
1	Running

The example flow chart of setting short current detection and control flow after chort current detection is shown below.



Set the short current detecting voltage in the SC0 and SC1 bits of SETSC register, and set the ENSC bit "1" to start the short current detection circuit.

If the /INTO pin output is changed to "L" level, read the FET_INT register and check the interrupt requests. Now, only DETSC bit is assumed to be set "1".

Set the PU bit of FET_INT register "1" to connect the pull-up resistor to DFS pin. If the short current detection state is kept, DFS pin voltage stays GND level.,

Write VMON register 19H and monitor the VMON output voltage with external ADC, and check that short current state is kept with DFS pin voltage。

If the DFS pin voltage is still GND level, short current state is kept and wait until the voltage of DFS rise to VDD.
If the state is not in short current state, the voltage of DFS will be VDD level by its pull-up resistor

If recovery from short current state is recognized, set the DF and CF bit of the FET register "1"to enable charge and discharge.

8. VGAIN register（Adrs=07H）

	7	6	5	4	3	2	1	0
bit	—	VG6	VG5	VG4	VG3	VG2	VG1	VG0
R/W	R	R	R	R	R	R	R	R
default	—	—	—	—	—	—	—	—

VGAIN register stores the gain correction value of the VMON output voltage.
Cell voltage is calcurated from VMON output voltage by following corrention equation.

cell voltage = VAGIN × [VMON output voltage] + OFFSET

VGAIN: gain corrention value of the VGAIN register
OFFSET: offset corrention value of the OFFSET register

The VGAIN register value and gain corrention value are shown in thefollowing table.

Register value[Hex]	Gain correction value
00	2.000
01	2.001
02	2.002
03	2.003
04	2.004
05	2.005
06	2.006
07	2.007
…	…
0F	2.015
10	2.016
…	…
1F	2.031
20	2.032
…	…
2F	2.047
30	2.048
…	…
3F	2.063

Register value[Hex]	Gain correction value
40	1.936
41	1.937
42	1.938
43	1.939
44	1.940
45	1.941
46	1.942
47	1.943
…	…
4F	1.951
50	1.952
…	…
5F	1.967
60	1.968
…	…
6F	1.983
70	1.984
…	…
7F	1.999

9. OFFSET register（Adrs=08H）

	7	6	5	4	3	2	1	0
bit	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
R/W	R	R	R	R	R	R	R	R
default	—	—	—	—	—	—	—	—

OFFSET register stores the VMON output voltage offset correction value.
Cell voltage is calcurated from monitored VMON output voltage by following correction equation.

Cell voltage = VAGIN × [VMON output voltage] + OFFSET

VGAIN: gain correction value of the VGAIN register
OFFSET: off set correctin value of the OFFSET register

The OFFSET register value nd the offset correction value are shown in the following table.

Register value[Hex]	Offset correctin value [mV]
00	+0
01	+1
02	+2
03	+3
…	…
7F	+127
80	−128
81	−127
82	−126
83	−125
…	…
FD	−3
FE	−2
FF	−1

10. VREFOF register（Adrs=09H）

	7	6	5	4	3	2	1	0
bit	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0
R/W	R	R	R	R	R	R	R	R
default	—	—	—	—	—	—	—	—

VREFOF register stores the offset correction value of the VREF output voltage from 2.5V.
VREF voltage is calcurated by following correction equation.

VREF output voltage＝2,500 [mV] + VREFOF

VREFOF: offset value of the VREFOF register

If VREFG outpu voltage is used as the reference voltage of the external A/D converter and if VMON output voltage is measured with the external A/D converter, cell voltage is calcuragted by the following equation.

Cell voltage [mV] = VGAIN × ADC measuring code × LSB + OFFSET

VGAIN: VGAIN register gain correction value
OFFSET: OFFSET register offset corrention value
LSB: external N-bit ADC resolution = (2,500 [mV] + VREGFOF) / (2^N-1)

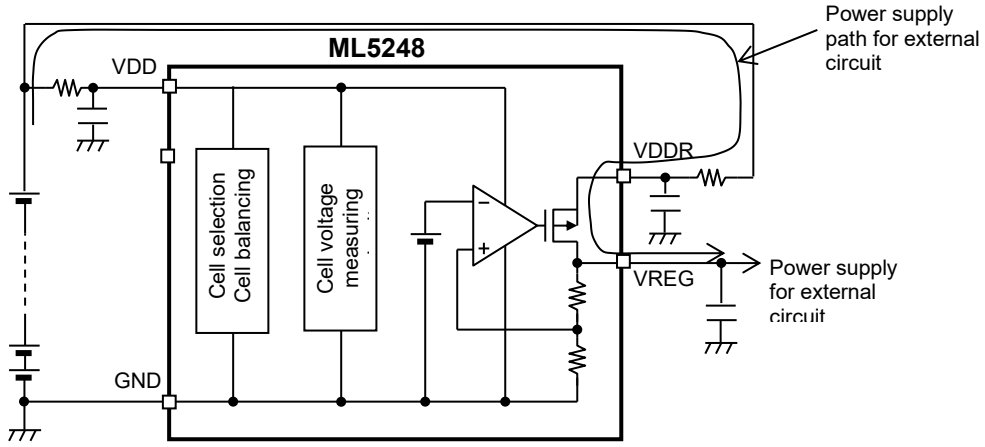
The VREFOF register value and the offset correction value is shown in the following table.

Register value[Hex]	Offset correction value [mV]
00	＋0
01	＋1
02	＋2
03	＋3
…	…
7F	＋127
80	－128
81	－127
82	－126
83	－125
…	…
FD	－3
FE	－2
FF	－1

● CONNECTING POWER SUPPLY (VDDR, VDD)

VDDR pin is the power supply pin only for the internal 3.3V regulator (VREG). If the output current of 3.3V regulator is large, it is recommended to make the voltage drop of RC filter register (for removing noise at the VDDR) smaller than 1V.

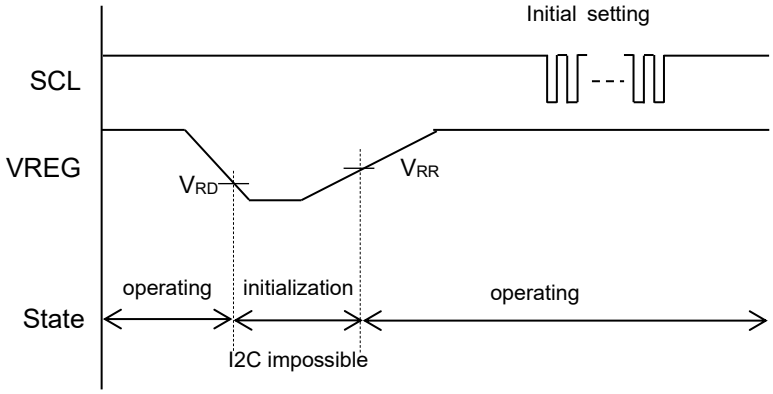
VDD pin is the power supply pin for all the ciurcuit other than internal 3.3V regulator.



● LOW VREG DETECTING FUNCTION

If a large output load is connected and the VREG pin voltage falls under the VREG low voltage detection voltage (V_{RD}), all registers are initialized.

If the VREG pin voltage rise over the VREG low voltage release voltage (V_{RR}), regster setting with I2C interface become effective. Wait for the VREG and VREF output voltage be stable, and start initial setting and monitoring.



● POWER-ON / POWER-OFF SEQUENCE

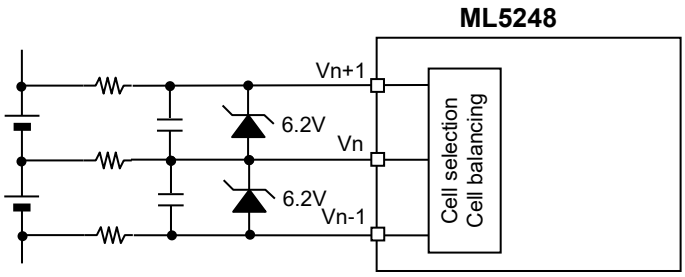
For POWER-ON, recommended battery connecting sequence is; connect the GND first, then connect the VDD, VDDR, and connect each cells from lower level.

If this sequence is not kept, absolute maximum rating is exceeded across the LSI and it may damage input pins of Vn+1 pin and Vn.

For POWER-OFF, recommended battery disconnecting sequence is; disconnect each cell from higher level first, then disconnect the VDD, VDDR, and lastly disconnect the GND.

And also in testing and evaluating with battery simulator, pay attention to the connecting and disconnecting sequence not to make an excessive voltage to absolute maximum rating of each Vn+1 pin and Vn pin.

As shown in the diagram bellow, it is recommend to use zener diode circuit for input pin protection, and good enough evaluation is requested.



Before battery connection to V_n pins of LSI, all of cell must be in a serial connection each other.

Connecting of individual battery cells to V_n pins of LSI without being a serial connection is forbidden because there is a possibility that absolute maximum rating is exceeded across the LSI and it may damage input pins of V_{n+1} and V_n.

There is no limitation on Power supply voltage rising time of power-on, power off order, and power supply voltage falling time of power-off.

Following the power-on, the ML5248 normally enter into normal state. ML5248 may rarely enter into the Power down state by the chattering or another reason during the connection of the battery cells. In this case, input the voltage lower than or equal to the Detecting charger connection PSENSE pin voltage (V_{PC}) to PSENSE pins, or input the “L” level to the /PUPIN pin, in order to power-up.

And, after the power-on or after the power-up, cell voltage measurement and current measurement should be done after the internal analog circuit is settled. To get the settling time of analog circuit, confirm the output settling time of VREF pin, VMON pin, and IMON pin in the application system.

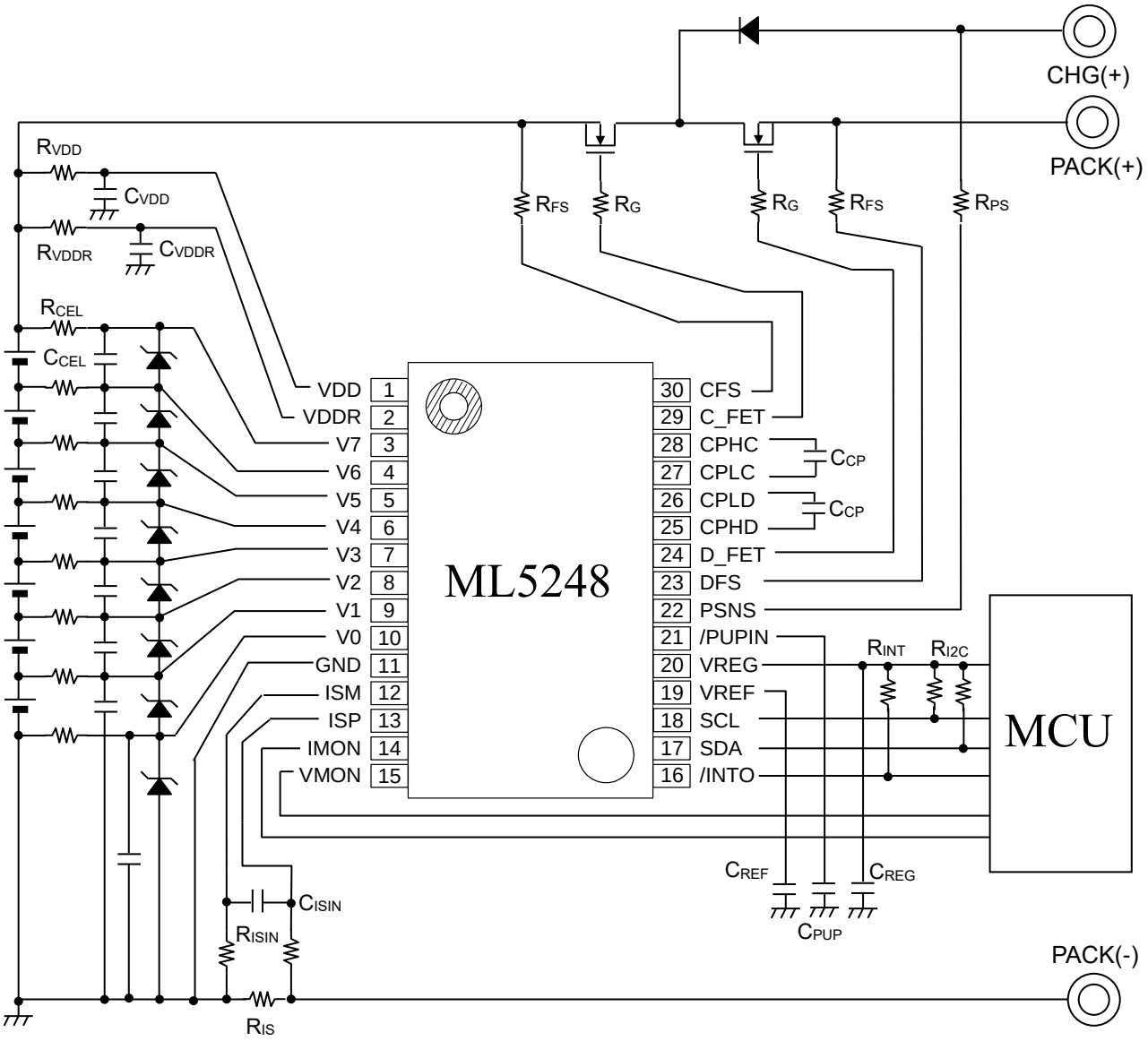
● CELL CONNECTING

If the number of connected cells is 3 to 6, connecting order in following table is recommended.

Number of Connected cells	V7	V6	V5	V4	V3	V2	V1	V0
6	Cell	Cell	Cell	Cell	Cell	Cell	Cell	GND
5	Cell	Cell	Cell	Cell	Cell	Cell	GND	GND
4	Cell	Cell	Cell	Cell	Cell	GND	GND	GND
3	Cell	Cell	Cell	Cell	GND	GND	GND	GND

■ EXAMPLE OF APPLICATION CIRCUIT

(7 cells, charge/discharge path isolated, MCU power supply =VREG)



■PARTS LIST

Symbol	Value
R_{VDD} (Note1)	510Ω
C_{VDD}	2.2μ~10μF
R_{VDDR}	100Ω
C_{VDDR}	2.2μ~10μF
R_{CEL}	150Ω~10kΩ
C_{CEL}	0.1μF or larger
R_{IS}	1mΩ

Symbol	Value
R_{ISIN}	1kΩ
C_{ISIN}, C_{RES}	0.1μF
C_{REG}, C_{REF}	4.7μF
C_{CP}	20nF (Note2)
C_{PUP}	1μF
R_G	1kΩ
R_{FS}	1kΩ

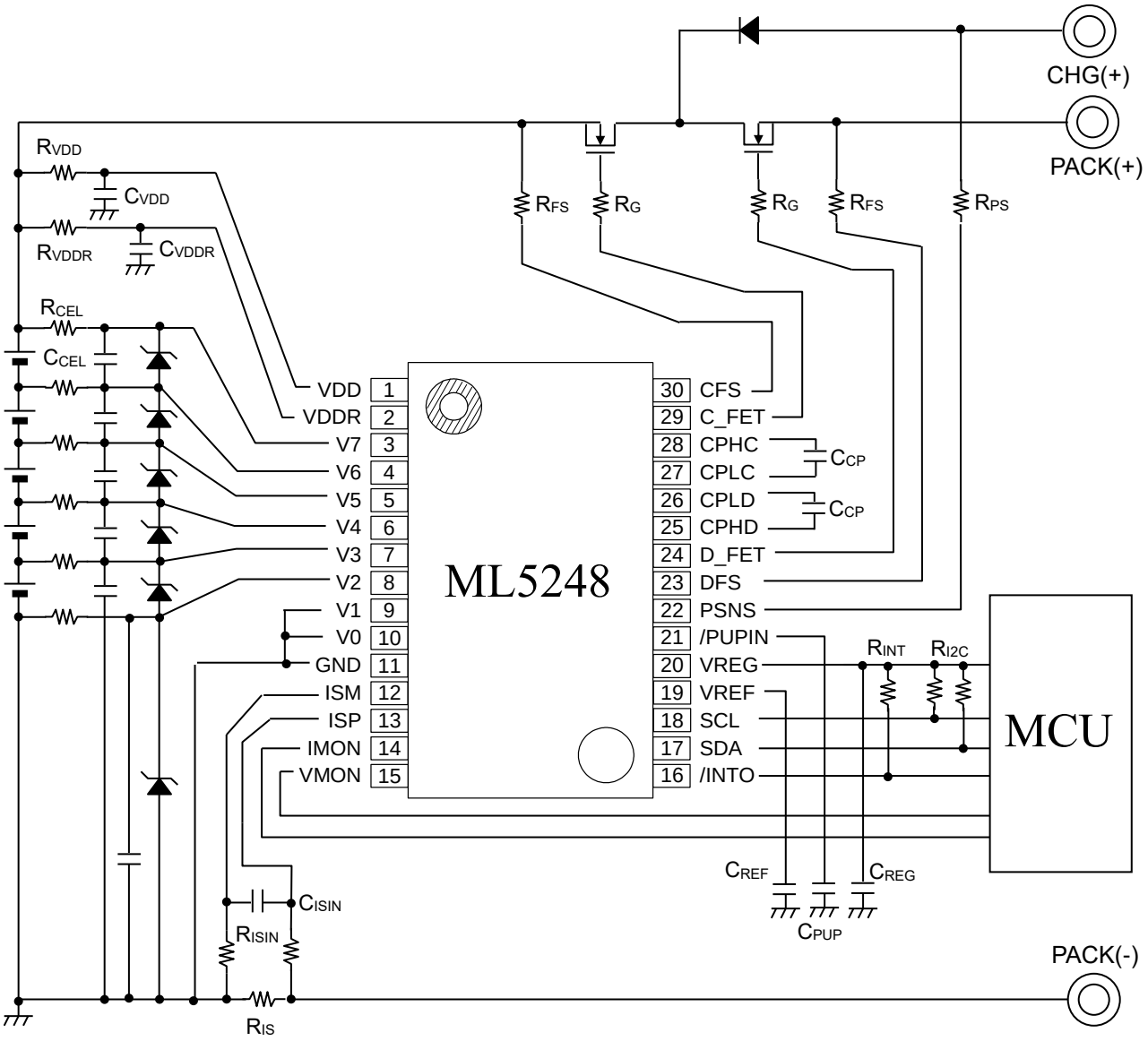
Symbol	Value
R_{PS}	1kΩ
R_{I2C}	47kΩ
R_{INT}	51kΩ

(Note 1) If C_{VDD}=2.2μF, R_{VDD}=1.5kΩ is recommended.
(Note 2) If external Nch-FET gate capacitance=10nF.

(Notice) Example of application circuit and the recommended values to parts list shall not guarantee performance under all conditions. Full and detailed tests are suggested on your actual application.

■ EXAMPLE OF APPLICATION CIRCUIT-2

(5 cells, charge/discharge path isolated, MCU power supply =VREG)



■ Parts List

Symbol	Value
R_{VDD} (Note1)	510Ω
C_{VDD}	2.2μ~10μF
R_{VDDR}	100Ω
C_{VDDR}	2.2μ~10μF
R_{CEL}	150Ω~10kΩ
C_{CEL}	0.1μF 以上
R_{IS}	1mΩ

Symbol	Value
R_{ISIN}	1kΩ
C_{ISIN}, C_{RES}	0.1μF
C_{REG}, C_{REF}	4.7μF
C_{CP}	20nF (Note2)
C_{PUP}	1μF
R_G	1kΩ
R_{FS}	1kΩ

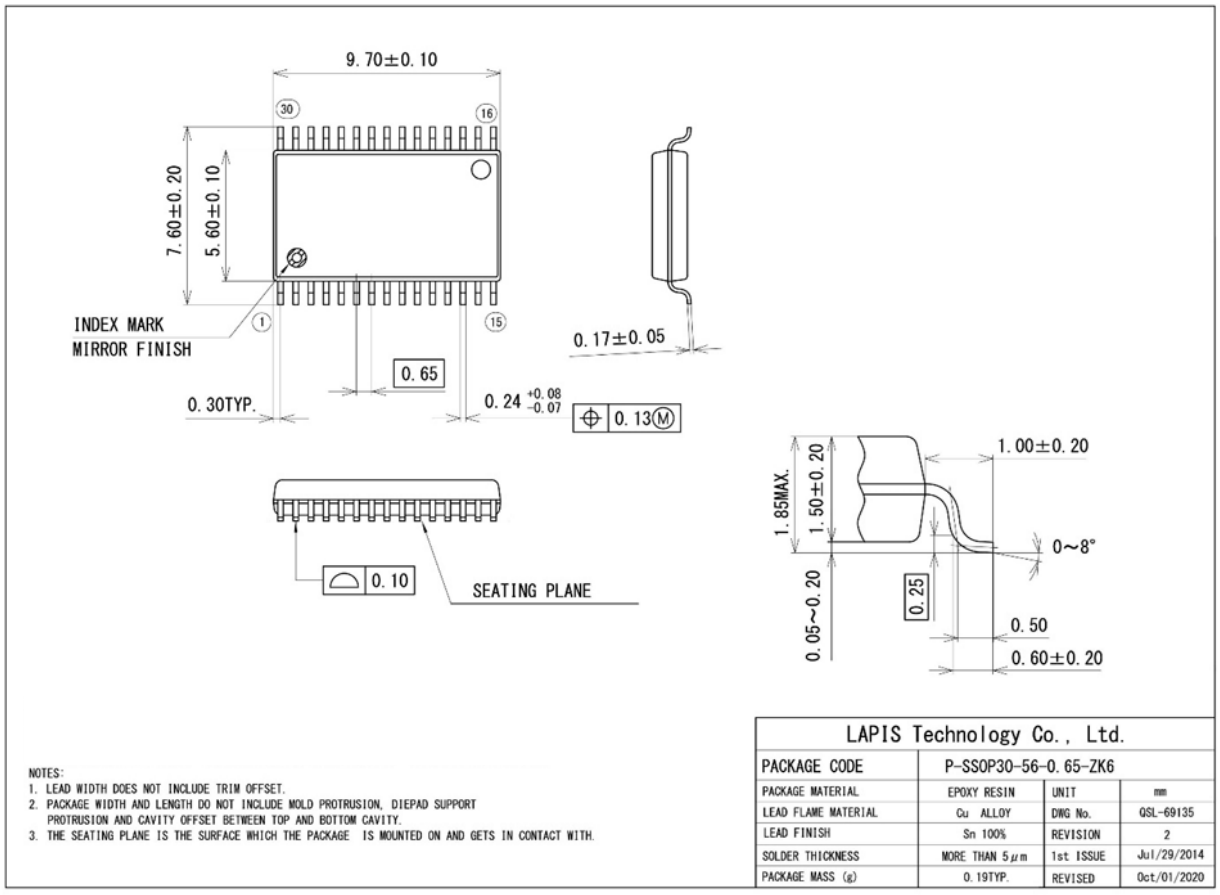
Symbol	Value
R_{PS}	1kΩ
R_{I2C}	47kΩ
R_{INT}	51kΩ

(Note 1) If C_{VDD}=2.2μF, R_{VDD}=1.5kΩ is recommended.

(Note 2) If external Nch-FET gate capacitance=10nF.

(Notice) Example of application circuit and the recommended values to parts list shall not guarantee performance under all conditions. Full and detailed tests are suggested on your actual application.

■ PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■ REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL5248-01	2018.5.21	—	—	First edition
FEDL5248-02	2020.11.30	—	—	Changed Company name
		18	18	FET_INT register, comment for the DEDCK bit is added.
		34	34	Changed “Notes”
FEDL5248-03	Jan. 9, 2024	1	1	Add Application Part number
		34	34	Add Notes

Notes

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LTSZ08023・01・002