

Analog Front-end IC for Protecting 4- to 10-series Lithium-ion Secondary Batteries

ML5262

General Description

The ML5262 is an analog front-end IC designed for protection systems in 4- to 10-series lithium-ion rechargeable battery packs. It provides automatic monitoring of individual cell voltages, charge/discharge current, and temperature, and incorporates a wide range of protection functions. By using an external control MCU, the LSI also enables state-of-charge (SoC) management and supports protection against overcharge, over-discharge, and overcurrent conditions for each cell.

Features

- High-accuracy cell voltage measurement using a 12-bit SAR ADC
- 16-bit $\Delta\Sigma$ ADC for charge/discharge current (ISP-ISM) with selectable gain $1\times/4\times$
- Auto cell balancing based on cell voltage difference (balance FET RON = 25 Ω typ.)
- Temperature sensor measurement function
- Primary protection: overcharge, overdischarge, charge/discharge overcurrent, short-circuit, high/low temperature
- Secondary protection: overcharge/overdischarge/overcurrent, high temperature, FET fault detection
- External fuse blow control (FUSE = 3.3 V typ. at secondary protection)
- Wake-up detection in sleep mode (interrupt to MCU when preset discharge current flows in sleep mode)
- SPI / I2C serial interface
- Built-in regulators for external MCU: 5 V (external NPN drive, 65 mA) 3.3 V (30 mA)

Product Name

- ML5262-001TBZ
MCU interface: SPI, Factory default for 10-cell apps
 - ML5262-101TBZ
MCU interface: I2C, Factory default for 10-cell apps
 - ML5262-102TBZ
MCU interface: I2C, Factory default for 4-cell apps
- Please refer to the code list for other setting values.

Applications

- Power tools / Gardening tools
- Cordless vacuum cleaners
- E-Bike / Electric-assist bicycles

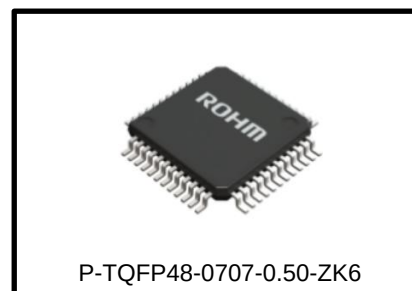
Key Specifications

- Input voltage range : +4.5V to +58V
- Current consumption : Normal 300 μ A (typ.)
Power-save 285 μ A (typ.)
Sleep 20 μ A (typ.)
Power down 1 μ A (typ.)
- Operating temperature : -40°C to +85°C
- Cell voltage measurement accuracy : ± 5 mV (typ.) @4V

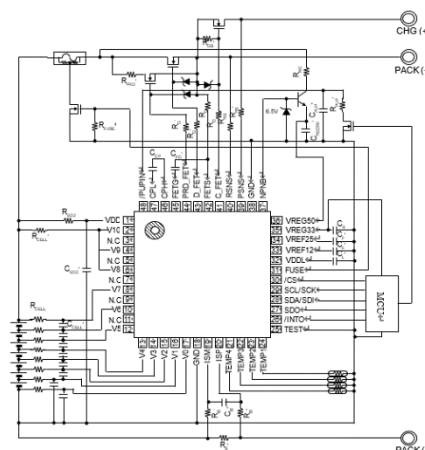
Package

W (typ.) x D (typ.) x H (max.)

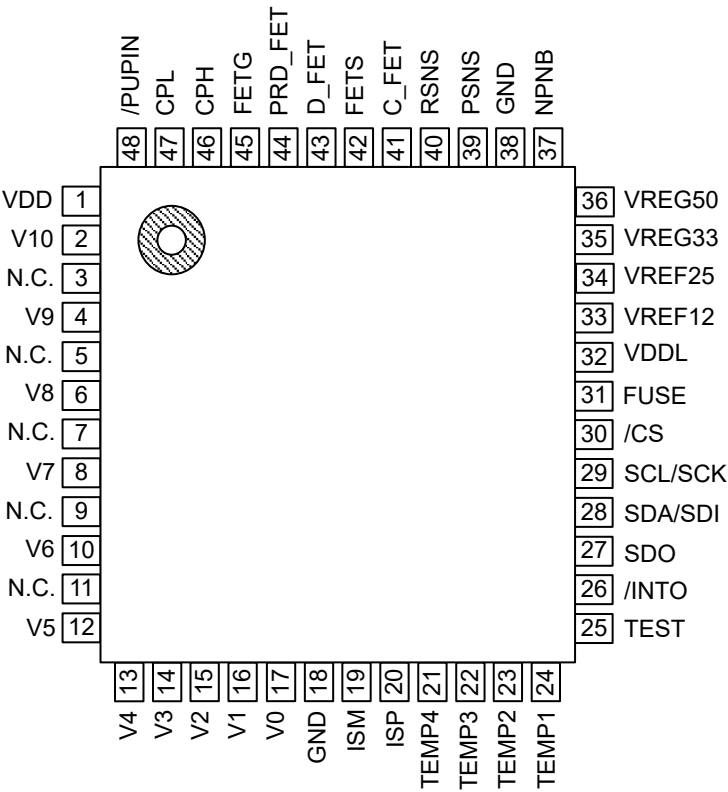
P-TQFP48-0707-0.50-ZK6 9.0 mm x 9.0 mm x 1.20 mm



Basic application circuit



• Pin Configuration



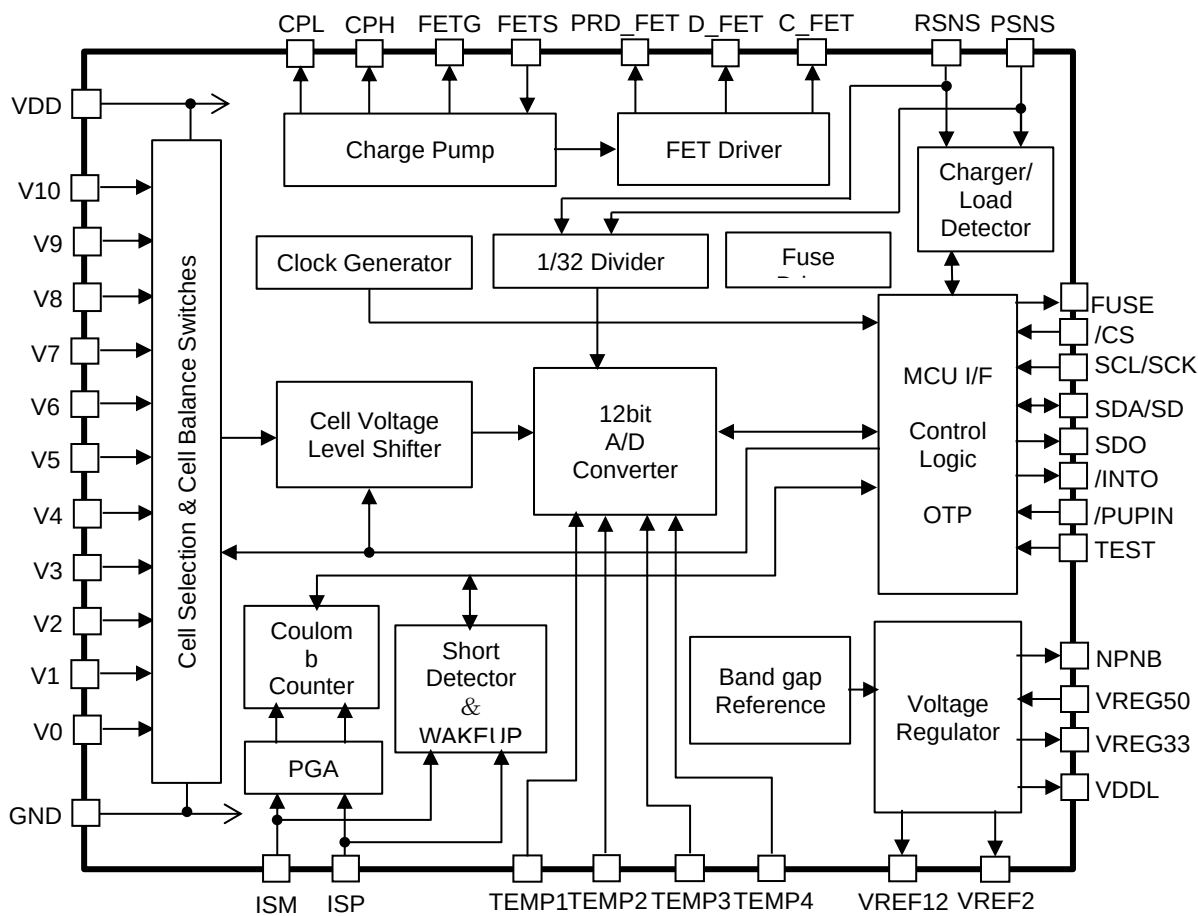
• Pin Description

Pin No.	Pin Name	I/O	Description
1	VDD	-	This is the power supply voltage input pin. Remove noise by configuring a CR filter using an external resistor and capacitor.
2	V10	I	Cell 10 positive input. If unused, connect to the highest cell via R _{CELL} .
3	N.C.	-	Unused pin. Leave it open.
4	V9	I	Cell 10 negative input and Cell 9 positive input. If unused, connect to the highest cell via R _{CELL} .
5	N.C.	-	Unused pin. Leave it open.
6	V8	I	Cell 9 negative input and Cell 8 positive input. If unused, connect to the highest cell via R _{CELL} .
7	N.C.	-	Unused pin. Leave it open.
8	V7	I	Cell 8 negative input and Cell 7 positive input. If unused, connect to the highest cell via R _{CELL} .
9	N.C.	-	Unused pin. Leave it open.
10	V6	I	Cell 7 negative input and Cell 6 positive input. If unused, connect to the highest cell via R _{CELL} .
11	N.C.	-	Unused pin. Leave it open.
12	V5	I	Cell 6 negative input and Cell 5 positive input. If unused, connect to the highest cell via R _{CELL} .
13	V4	I	Cell 5 negative input and Cell 4 positive input.
14	V3	I	Cell 4 negative input and Cell 3 positive input.
15	V2	I	Cell 3 negative input and Cell 2 positive input.
16	V1	I	Cell 2 negative input and Cell 1 positive input.
17	V0	I	Cell 1 negative input.
18	GND	-	Ground
19	ISM	I	This is a current sense resistor connection pin. Connect to the negative terminal of the lowest battery cell. If unused, connect to GND pin.
20	ISP	I	This is a current sense resistor connection pin. Connect so that the voltage is higher than the ISM pin during discharge (ISP>ISM). If unused, connect to GND pin.
21	TEMP4	I	This is a thermistor connection pin for temperature measurement. Connect an NTC thermistor between the TEMP4 pin and GND. A 10kΩ resistor is built in between the VREF25 and the TEMP4 pins. If unused, connect to VREF25 pin.
22	TEMP3	I	This is a thermistor connection pin for temperature measurement. Connect an NTC thermistor between the TEMP3 pin and GND. A 10kΩ resistor is built in between the VREF25 and the TEMP3 pins. If unused, connect to VREF25 pin.
23	TEMP2	I	This is a thermistor connection pin for temperature measurement. Connect an NTC thermistor between the TEMP2 pin and GND. A 10kΩ resistor is built in between the VREF25 and the TEMP2 pins. If unused, connect to VREF25 pin.
24	TEMP1	I	This is a thermistor connection pin for temperature measurement. Connect an NTC thermistor between the TEMP1 pin and GND. A 10kΩ resistor is built in between the VREF25 and the TEMP1 pins. If unused, connect to VREF25 pin.
25	TEST	I	This is an IC testing pin. Fix to GND.
26	/INTO	O	Interrupt signal output pin to an external MCU. NMOS open-drain output. When an interrupt occurs, this pin outputs an "L" level. If unused, leave it open.
27	SDO	O	This is the serial data output pin when the SPI interface is selected. When the /CS pin is at the "H" level, this pin becomes a high impedance. If unused, leave it open.
28	SDA/SDI	IO	When the SPI interface is selected, this is the serial data input pin, when the I2C interface is selected, this is the serial data input/output pin. When the I2C interface is selected, an external pull-up resistor must be connected. If unused, connect to VREG33 pin.

Pin No.	Pin Name	I/O	Description
29	SCL/SCK	I	This is the serial clock input pin. When the I2C interface is selected, an external pull-up resistor must be connected. If unused, connect to VREG33 pin.
30	/CS	I	This is the chip select input pin when the SPI interface is selected. The SPI interface is enabled when an "L" level is input on this pin. If unused, connect to VREG33 pin.
31	FUSE	O	Control signal output pin to the Nch-FET for cutting off the external fuse. Connect it to the gate terminal of the Nch-FET. When the LSI cuts off a fuse, it outputs 3.3V (typ.) from this pin. If unused, leave it open.
32	VDDL	O	Built-in 1.5V regulator output pin. Use as an external power source is prohibited. Connect a 1μF capacitor between this pin and GND.
33	VREF12	O	This is the 1.2V reference voltage output pin for the ΔΣ ADC. Connect a 3.3μF capacitor between this pin and GND.
34	VREF25	O	This is a 2.5V reference voltage output pin for the SAR ADC. Connect a 3.3μF capacitor between this pin and GND.
35	VREG33	O	Built-in 3.3V regulator output pin. Connect a 4.7μF capacitor between this pin and GND. This output can be used to power an external MCU and MCU interface.
36	VREG50	I	Current supply input pin for the VREG33 pin. Connect to the emitter terminal of an external NPN transistor. Connect a 10μF capacitor between this pin and GND. This power line can be used as a 5V regulator output.
37	NPNB	O	This is the base control output pin for the NPN transistor of the 5V regulator configured with an external NPN transistor. Connect it to the base terminal of the external NPN transistor.
38	GND	-	Ground.
39	PSNS	I	This is an input terminal for detecting the connection/release of a charger. 1/32-ratio voltage measurement available. If unused, connect to VDD pin.(Note 1)
40	RSNS	I	This is an input terminal for detecting the connection/release of a load. 1/32-ratio voltage measurement available. If unused, connect to VDD pin.
41	C_FET	O	This is the control signal output pin for the charging Nch-FET. Connect to the gate terminal of the charging Nch-FET. Outputs FETS + 11.4 V (typ.) when ON setting, and outputs FETS Voltage when OFF setting. If unused, leave it open.
42	FETS	I	This is an input terminal for the Charge-pump capacitor node. Connect it to the source terminal of the charging and discharging Nch-FET. Connect a 470nF capacitor between this pin and FETG pin. If unused, leave it open.
43	D_FET	O	This is the control signal output pin for the discharge Nch-FET. Connect to the gate terminal of the discharge Nch-FET. Outputs FETS + 11.4 V (typ.) when ON setting, and outputs FETS Voltage when OFF setting. If unused, leave it open.
44	PRD_FET	O	This is the control signal output pin for the pre-discharge Nch-FET. Connect to the gate terminal of the pre-discharging Nch-FET. Outputs FETS + 11.4 V (typ.) when ON setting, and outputs FETS Voltage when OFF setting. If unused, leave it open.
45	FETG	O	This is an input terminal for the Charge-pump capacitor node. Connect a 470nF capacitor between this pin and FETS pin. If unused, leave it open.
46	CPH	O	This is an input terminal for the Charge-pump capacitor node. Connect a 20nF capacitor between this pin and CPL pin. If unused, leave it open.
47	CPL	O	This is an input terminal for the Charge-pump capacitor node. Connect a 20nF capacitor between this pin and CPH pin. If unused, leave it open.
48	/PUPIN	I	This is the power-up trigger signal input pin. By inputting an "L" level to this pin, if the LSI is in a power-down state, it will transition to a power-up state. Also, if the LSI is in a sleep state, it will transition to a normal state. A 1MΩ pull-up resistor is built in between this pin and the VDD pin.

(Note 1) If fixed to VDD, the LSI cannot enter sleep or power-down state. When putting the LSI into the sleep or power-down state, control this pin by switching it to Open/VDD using an external circuit.

• Block Diagram Description

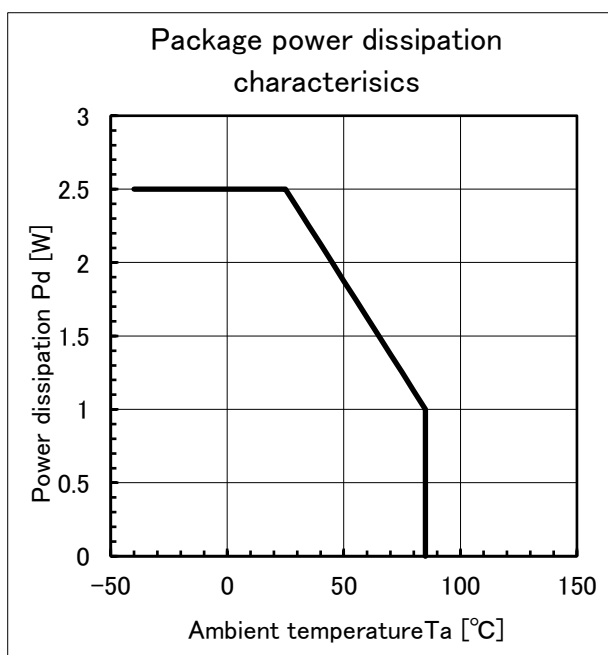


Absolute Maximum Ratings

GND=0V, Ta=25°C

Item	Symbol	Condition	Rating	Unit
Power supply voltage	V _{DD}	Applied to VDD pin	-0.3 to +60	V
Input voltage	V _{IN1}	Applied to V10~V0 pins The potential difference between Vn+1 and Vn pins *1	-0.3 to +36	V
	V _{IN2}	Applied to FETS, PSNS, RSNS pins	-0.3 to +60	V
	V _{IN3}	Applied to /PUPIN pin	-0.3 to V _{DD} +0.3	V
	V _{IN4}	Applied to ISM, ISP, TEMP1, TEMP2, TEMP3, TEMP4 pins	-0.3 to V _{REG} +0.3	V
	V _{IN5}	Applied to VREG50, V0, /CS, SCL/SCK, SDA/SDI, TEST pins	-0.3 to +6.5	V
Output voltage	V _{OUT1}	Applied to C_FET, D_FET, PRD_FET pins V _{FS} = voltage of FETS pin	V _{FS} -0.3 to +60	V
	V _{OUT2}	Applied to CPH, CPL, FETG pins	-0.3 to +60	V
	V _{OUT3}	Applied to VREG33 pin	- 0.3 to V _{REG50} +0.3	V
	V _{OUT4}	Applied to SDO, VREF25, VREF12, FUSE pins	- 0.3 to V _{REG} +0.3	V
	V _{OUT5}	Applied to VDDL pin	- 0.3 to +2.1	V
	V _{OUT6}	Applied to /INTO, SDA/SDI pins	-0.3 to +6.5	V
	V _{OUT7}	Applied to NPNB pin	-0.3 to V _{DD} +0.3	V
Output short-circuit current	I _{OS}	Applied to NPNB, VDDL, VREF25, VREF12, SDO, /INTO, C_FET, D_FET, PRD_FET, FUSE, SDA/SDI pins	10	mA
	I _{OSR}	Applied to VREG33 pin	100	mA
Cell balancing current	I _{CB}	Per cell balancing switch	95.5	mA
Power dissipation	P _D	Ta=25°C	2.5	W
Junction temperature	T _{JMAX}	-	125	°C
Package thermal resistance	θ _{ja}	When mounted on a JEDEC2-layer board	40	°C /W
Storage temperature	T _{STG}	-	-55 to +150	°C

*1: When connecting or disconnecting battery cells, the voltage between the Vn+1 and Vn pins may exceed the rated voltage and cause destruction, so please evaluate thoroughly before use.



As the ambient temperature (Ta) increases, the package power dissipation decreases. If the VREG33 pin output current is large, make sure that the power dissipation listed on the left is not exceeded.

▪ Recommended Operating Conditions

(GND=0V)

Item	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD1}	Applied to VDD pin FET Driver Disable Setting	4.5 to 58	V
	V_{DD2}	Applied to VDD pin FET Driver Enable Setting	4.5 to 45	V
Operating temperature	T_a	No output load	-40 to +85	°C

Electrical Characteristics

DC Characteristics

$V_{DD} = 4.5$ to $58V$, $GND = 0V$, $T_a = -40$ to $+85^{\circ}C$, No output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (*1)	V_{IH}	-	$0.8 \times V_{REG}$	—	V_{REG}	V
Digital "L" input voltage (*1)	V_{IL}	-	0	—	$0.2 \times V_{REG}$	V
/PUPIN pin "H" input voltage	V_{IHP}	-	2	—	V_{DD}	V
/PUPIN pin "L" input voltage	V_{ILP}	-	0	—	0.6	V
Digital "H" input current (*1)	I_{IH}	$V_{IH} = V_{REG}$	—	—	2	μA
Digital "L" input current (*1)	I_{IL}	$V_{IL} = GND$	-2	—	—	μA
/PUPIN pin "H" input current	I_{IHP}	$V_{IH} = V_{DD}$	-	-	2	μA
/PUPIN pin "L" input current	I_{ILP}	$V_{DD} = 58V$, $V_{IL} = GND$	-98	-58	-25	μA
Digital "H" output voltage (*2)	V_{OH}	$I_{OH} = -100\mu A$	$V_{REG} - 0.2$	-	V_{REG}	V
Digital "L" output voltage (*3)	V_{OL}	$I_{OL} = 1mA$	0	-	0.2	V
Digital output leakage current (*3)	I_{OLK}	$V_{OH} = V_{REG}$, $V_{OL} = 0V$	-2	-	2	μA
Cell monitor pin input current (*4)	I_{INVC}	When measuring battery cell voltage	-5	-	15	μA
Cell monitor pin input leakage current (*4)	I_{ILVC}	When not measuring battery cell voltage	-5	-	5	μA
FET "H" output voltage (*5)	V_{OHF1}	$I_{OH} = -1\mu A$ $V_{DD} = V_{FS} = 12.5V$ to $45V$ V_{FS} : voltage of FETS pin	$V_{FS} + 9$	$V_{FS} + 11$	$V_{FS} + 13$	V
	V_{OHF2}	$I_{OH} = -1\mu A$ $V_{DD} = V_S = 4.5V$ to $12.5V$	$V_S + 2.5$	—	$V_S + 12.5$	V
	V_{OHF3}	$I_{OH} = -1\mu A$ $V_{DD} = V_S = 4.5$ to $12.5V$ When the charger is connected	$V_S + 5$	—	$V_S + 12.5$	V
FET "L" output voltage (*6)	V_{OLF}	$V_{FS} = 0V$ to $45V$ V_{FS} : voltage of FETS pin	V_{FS}	-	$V_{FS} + 0.3$	V
FETS pin input current	I_{IHFS1}	Normal state $V_{FS} = 0V$ to $45V$ V_{FS} : voltage of FETS pin	-2	-	300	μA
	I_{IHFS2}	Sleep state $V_{FS} = 0V$ to $45V$	-2	-	30	μA
VREG50 output voltage	V_{REG50_1}	$V_{DD} = 8.0V$ to $58V$ load current $< 65mA$ (*7)	4.5	5.0	5.5	V
	V_{REG50_2}	$V_{DD} = 4.5V$ to $8.0V$ load current $< 5mA$	3.5	5.0	5.5	V
VREG33 output voltage	V_{REG_1}	$V_{DD} = 8V$ to $58V$ load current $< 30mA$ $T_a = 25^{\circ}C$	3.267	3.3	3.333	V
	V_{REG_2}	$V_{DD} = 8V$ to $58V$ load current $< 30mA$ $T_a = -40$ to $85^{\circ}C$	3.1	3.3	3.5	V
	V_{REG_L}	$V_{DD} = 4.5V$ to $8V$ load current $< 5mA$ $T_a = -40$ to $85^{\circ}C$	3.0	3.3	3.5	V
VDDL output voltage	V_{DDL}	$T_a = -40$ to $85^{\circ}C$ No output load	1.35	1.5	1.65	V
VREF25 output voltage	V_{REF25}	$T_a = -40 \sim 85^{\circ}C$ load current $< 500\mu A$	2.48	2.50	2.54	V
VREF12 output voltage	V_{REF12}	$T_a = -40 \sim 85^{\circ}C$ No output load	1.21	1.24	1.28	V
Cell balancing switch ON resistance	R_{BL}	Built-in balancing FET $V_{DS} = 0.1V$ Cell voltage = $3V$ or more	12	25	50	Ω
NPNB pin output current	I_{NPNB1}	(VREG50=4V) $V_{DD} = 8V$ to $58V$	0.5	2.9	5	mA
	I_{NPNB2}	(VREG50=4V) $V_{DD} = 4.5V$ to $8V$	0.18	-	5	mA

(* 1): Applied to /CS,SCL/SCK,SDA/SDI pins

(* 2): Applied to SDO,FUSE pins

(* 3): Applied to SDA/SDI, SDO,/INTO,FUSE pins

(* 4): Applied to V10 toV0 pins

(* 5): Applied to C_FET, D_FET, PRD_FET pins

(* 6): Applied to D_FET, PRD_FET pins

(* 7): This is peak current, not DC current. Be aware of the allowable loss of the external NPN transistor.

• Current Consumption

V_{DD}= 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, No output load

Item	Symbol	condition	Min.	Typ.	Max.	Unit
Normal state current consumption	I _{DD1}	Cell voltage measurement cycle = 200ms Number of connected cells = 10 cells When measuring with TEMP1 to TEMP4 pins	-	300	504	μA
Power-save state current consumption	I _{DD2}	Cell voltage measurement cycle = 1s Number of connected cells = 10 cells When measuring with TEMP1 to TEMP4 pins	-	285	450	μA
Sleep state current consumption	I _{DD3}	WKUP bit = "0"	-	20	50	μA
	I _{DD4}	WKUP bit = "1"		34	70	μA
Power-down state current consumption	I _{DD5}	-	-	1	2	μA

* The above current consumption is specified by the current flowing through VDD and VREG50 pins.

• Cell Voltage Measurement Characteristics

 $V_{DD} = 8$ to $58V$, $GND = 0V$, $T_a = -40$ to $+85^{\circ}C$, No output load, ENCC bit = "1"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage measurement range	V_{VMR}	(*1)	0.1	-	5	V
Cell voltage measurement resolution	V_{LSB}	-	-	5000/4095	-	mV
Cell voltage measurement error (*2)	V_{ER1}	Cell voltage = 4V $T_a = 25^{\circ}C$	- 5	-	5	mV
	V_{ER2}	Cell voltage = 1.6V to 4.3V $T_a = 0^{\circ}C$ to $60^{\circ}C$	-10	-	10	mV
	V_{ER3}	Cell voltage = 1.6V to 4.3V $T_a = -40^{\circ}C$ to $85^{\circ}C$	-20	-	20	mV
Cell voltage measurement error (*3)	V_{ER2}	Cell voltage = 1.6V to 4.3V $T_a = 0^{\circ}C$ to $60^{\circ}C$	-10	-	17.2	mV
Cell voltage measurement interval time	t_{MON0}	When TVC[1:0] bits = 0x0	32	40	48	ms
	t_{MON1}	When TVC[1:0] bits = 0x1	160	200	240	ms
	t_{MON2}	When TVC[1:0] bits = 0x2	240	300	360	ms
	t_{MON3}	When TVC[1:0] bits = 0x3	320	400	480	ms

(*1) This does not apply when the power supply voltage V_{DD} is lower than 8V.

(*2) The characteristics described herein are applicable at shipment.

(*3) The characteristics remain within the specified limits for up to 10 years at an average temperature of $60^{\circ}C$.

• Current Measurement Characteristics

V_{DD}= 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, Shunt resist = 0.5mΩ, No output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current measurement range (*1)	I _{MR1}	When IGAIN bit = "0"	-600	-	100	A
	I _{MR2}	When IGAIN bit = "1"	-150	-	25	A
Current measurement amplifier gain (*2)	G _{IM0}	When IGAIN bit = "0"	0.94	1	1.06	Gain
	G _{IM1}	When IGAIN bit = "1"	3.76	4	4.24	Gain
Current measurement resolution	I _{LSB1}	When IGAIN bit = "0"	-	18.92	-	mA
	I _{LSB2}	When IGAIN bit = "1"	-	4.73	-	mA
Current measurement error	I _{ER}	Ta = 0°C to 60°C When measuring -50A	-0.5	-	0.5	A
Measured value at zero current	I _{ZR}	ISP-ISM = 0V	-0.05	-	0.05	A
Current measurement time	t _{IM}	—	1.6	2	2.4	ms
Cell voltage synchronized current measurement Effective gain switching time	t _{ICVAL1}	Defined based on the time from the QVM output. When TVC[1:0] bits = 0x0	3.2	4	4.8	ms
	t _{ICVAL2}	Defined based on the time from the QVM output. When TVC[1:0] bits = 0x1	131	164	197	ms
	t _{ICVAL3}	Defined based on the time from the QVM output. When TVC[1:0] bits = 0x2	211	264	317	ms
	t _{ICVAL4}	Defined based on the time from the QVM output. When TVC[1:0] bits = 0x3	291	364	437	ms
Coulomb counter error	C _{CER}	Ta = 0°C to 60°C When measuring -50A	-5	-	5	%
Coulomb counter time	t _{CC0}	When CC[1:0] bits = 0x0	200	250	300	ms
	t _{CC1}	When CC[1:0] bits = 0x1	400	500	600	ms
	t _{CC2}	When CC[1:0] bits = 0x2	800	1000	1200	ms
	t _{CC3}	When CC[1:0] bits = 0x3	1600	2000	2400	ms
ISP, ISM pins input current	I _{IS}	Input voltage = -50mV to 0.3V	-2	-	2	μA

(*1) The charging current is positive, and the discharge current is negative.

(*2) This applies when 1 kΩ resistors are connected to the ISP and ISM pins, respectively.

• Temperature Sensor Measurement Characteristics

V_{DD}= 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, No output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TEMPn pin pull-up resistor	R _{TUP}	Between TEMPn and VREF25 pins Temperature measurement with TEMPn pin	7	10	13	kΩ
TEMPn pin pull-up resistor temperature coefficient	T _{CTUP}	-	-5.3	-3.6	-1.5	Ω/°C
TEMPn pin input voltage measurement error	V _{TER}	TEMPn pin input voltage = 0.3V to 2.3V	-15	-	15	mV
Temperature sensor measurement resolution	V _{TLSB}	-	-	2500/4095	-	mV
Temperature sensor measurement waiting time	t _{WTT}	-	0.75	0.94	1.13	ms
TEMPn pin input current	I _{TEMP}	When not measuring Input voltage = 0V to VREF25	-2	-	2	μA

• PSNS and RSNS and VDD Pins Voltage Measurement, Charger Detection Voltage Characteristics

V_{DD}= 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, No output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RSNS pin input voltage measurement error	V _{ERS50}	Input voltage = 58V	-2.5	-	2.5	V
	V _{ERS32}	Input voltage = 32V	-2.5	-	2.5	V
	V _{ERS1}	Input voltage = 1V	-0.5	-	0.5	V
PSNS pin input voltage measurement error	V _{EPS50}	Input voltage = 58V	-2.5	-	2.5	V
	V _{EPS32}	Input voltage = 32V	-2.5	-	2.5	V
	V _{EPS1}	Input voltage = 1V	-0.5	-	0.5	V
VDD voltage measurement error	V _{EVD50}	V _{DD} =58V	-2.5	-	2.5	V
	V _{EVD4p5}	V _{DD} =4.5V	-0.5	-	0.5	V
PSNS and RSNS and VDD pins input voltage measurement resolution	V _{SLSB}	-	-	19.53 6	-	mV
PSNS and RSNS and VDD pins voltage measurement waiting time	t _{WTVR}	-	0.75	0.94	1.13	ms
Charger connection detection PSNS pin voltage	V _{PC1}	When in the sleep state (WKUP = "0"). When in the power-down state.	1.6	3.0	4.4	V
Charger release detection voltage	V _{PLU}	When charging overcurrent is detected. Code difference (VDD_reg – PSNS_reg)	-	5 (97.7)	-	LSB (mV)
RSNS pin voltage when load release is detected	V _{RL}	When discharge overcurrent1,2 is detected. When a short-circuit current is detected.	-	102 (1.99)	-	LSB (V)
Wait time after load release detection	T _{RL}	When discharge overcurrent1,2 is detected. When a short-circuit current is detected.	40	50	60	ms
PSNS pull-down resistance	R _{PD}	When in the sleep state. When in the power-down state. When over-discharge is detected. When charging overcurrent is detected. When PSNSPD bit = "1".	200	500	1000	kΩ
RSNS pull-up resistance	R _{PU}	When discharge overcurrent1,2 is detected. When a short-circuit current is detected. When RSNSPU bit = "1".	0.5	2	4	MΩ
RSNS input leakage current	I _{LRS}	When in the normal state. When the RSNS pin voltage is not measured.	-2	-	2	μA
PSNS input leakage current	I _{LPS}	When in the normal state. When the PSNS pin voltage is not measured.	-2	-	2	μA

• Detection Voltage Characteristics

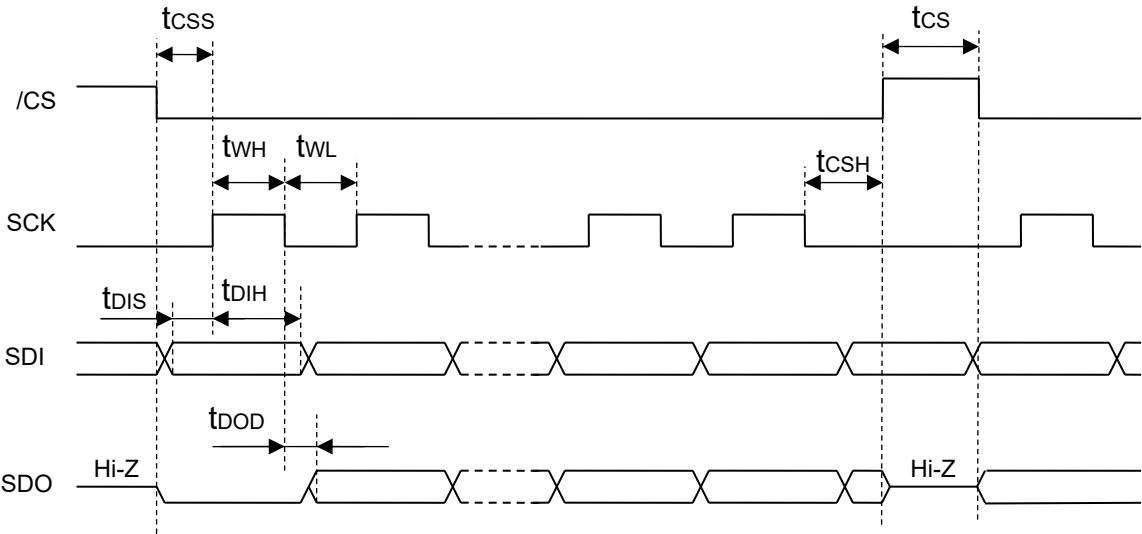
$V_{DD}= 4.5$ to $58V$, $GND= 0V$, $T_a= -40$ to $+85^{\circ}C$, Shunt resistor= $0.5m\Omega$, No output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage/undervoltage detection accuracy	V_{EV}	Cell voltage = $1V$ to $4.3V$ $T_a = 0^{\circ}C$ to $60^{\circ}C$	-10	-	10	mV
Overcurrent detection accuracy	A_{EI}	Shunt resistor = $0.5m\Omega$	-10	-	10	%
Temperature detection accuracy	V_{ET}	TEMPn pin input voltage = $0.3V$ to $2.3V$	-15	-	15	mV
Short-circuit current detection voltage	V_{S0}	SC[2:0] bits = $0x0$	20	25	30	mV
	V_{S1}	SC[2:0] bits = $0x1$	40	50	60	mV
	V_{S2}	SC[2:0] bits = $0x2$	60	75	90	mV
	V_{S3}	SC[2:0] bits = $0x3$	80	100	120	mV
	V_{S4}	SC[2:0] bits = $0x4$	100	125	150	mV
	V_{S5}	SC[2:0] bits = $0x5$	120	150	180	mV
	V_{S6}	SC[2:0] bits = $0x6$	140	175	210	mV
Short-circuit current detection delay time	t_{SHRT0}	TSC[1:0] bits = $0x0$	40	50	60	μs
	t_{SHRT1}	TSC[1:0] bits = $0x1$	80	100	120	μs
	t_{SHRT2}	TSC[1:0] bits = $0x2$	120	150	180	μs
	t_{SHRT3}	TSC[1:0] bits = $0x3$	160	200	240	μs
Wakeup detection voltage	V_{WK1}	When in the sleep state.	2	5	8	mV
Wakeup detection delay time	t_{WK}	-	1.6	2	2.4	ms
VREG50 drop detection voltage	V_{RD50}	-	2.6	2.9	3.2	V
VREG50 recovery detection voltage	V_{RR50}	-	2.9	3.2	3.5	V
VREG33 drop detection voltage	V_{RD33}	-	2.3	2.45	2.6	V
VREG33 recovery detection voltage	V_{RR33}	-	2.5	2.75	2.9	V
VDDL drop detection voltage	V_{RD15}	-	1.1	1.2	1.3	V
VDDL recovery detection voltage	V_{RR15}	-	1.2	1.3	1.4	V

• AC Characteristics
1. SPI Interface Characteristics

V_{DD}= 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, No output load

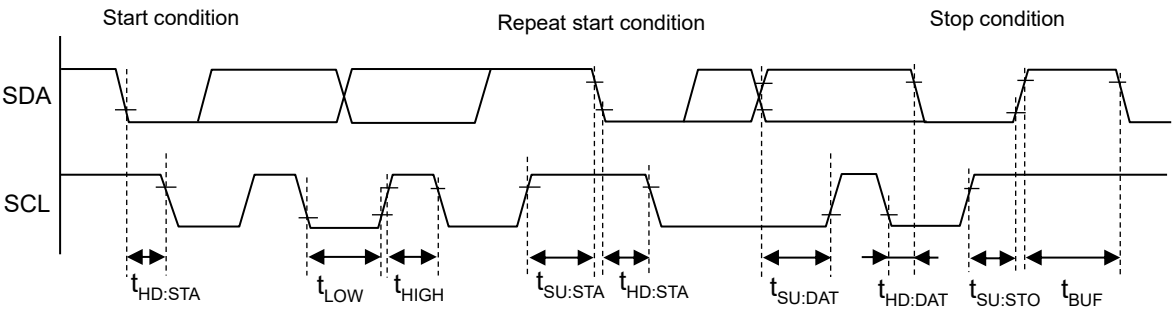
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
/CS-SCK setup time	t _{CSS}	-	100	-	-	ns
SCK-/CS hold time	t _{CSH}	-	100	-	-	ns
SCK "H" pulse width	t _{WH}	-	500	-	-	ns
SCK "L" pulse width	t _{WL}	-	500	-	-	ns
SCK-SDI setup time	t _{DIS}	-	50	-	-	ns
SCK-SDI hold time	t _{DIH}	-	50	-	-	ns
SCK-SDO output delay time	t _{DOD}	-	-	-	400	ns
/CS "H" pulse width	t _{CS}	-	500	-	-	ns



2. I2C Interface Characteristics

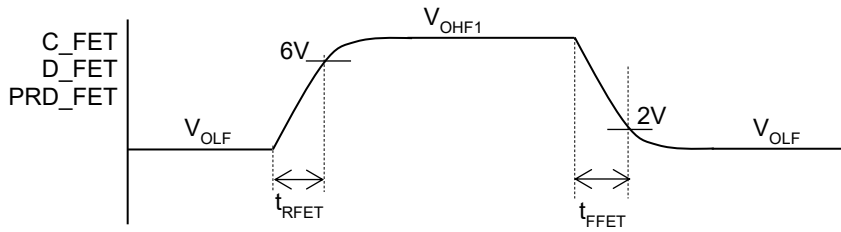
V_{DD}= 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, No output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	-	-	-	400	kHz
SCL hold time (start / repeated start condition)	t _{HD:STA}	-	0.6	-	-	μs
SCL “L” level time	t _{LOW}	-	1.3	-	-	μs
SCL “H” level time	t _{HIGH}	-	0.6	-	-	μs
SDA hold time	t _{HD:DAT}	-	0	-	-	μs
SDA setup time (repeated start condition)	t _{SU:DAT}	-	0.1	-	-	μs
SDA setup time (stop condition)	t _{SU:STO}	-	0.6	-	-	μs
Bus free time	t _{BUF}	-	1.3	-	-	μs



3. FET Driver Characteristics

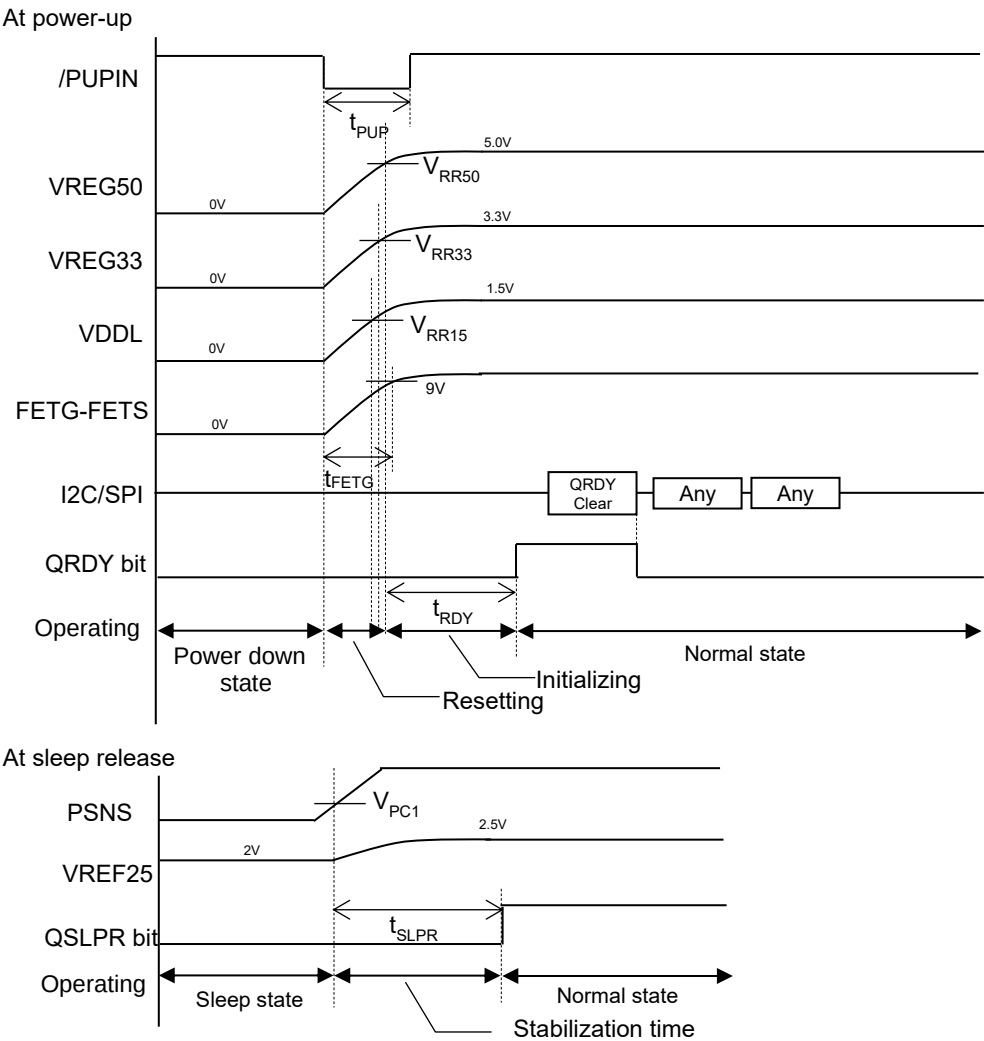
V _{DD} = 12.5 to 45V, GND= 0V, Ta= -40 to +85°C, No output load						
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
C_FET, D_FET, PRD_FET pins output rise time	t _{RFET}	Gate capacitance = 20nF Gate protection resistance = 100Ω	-	100	170	μs
C_FET, D_FET, PRD_FET pins output fall time	t _{FFET}	Gate capacitance = 20nF Gate protection resistance = 100Ω	-	50	85	μs



4. Power-up, Wake from Sleep Characteristics

V _{DD} = 4.5 to 58V, GND= 0V, Ta= -40 to +85°C, No output load						
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
/PUPIN “L” pulse width	t _{PUP}	-	1	-	-	ms
Waiting time for the initialization completion interrupt to occur(*1)	t _{RDY}	-	47	57	67	ms
FETG pin output time(*2)	t _{FETG}	C _{FG} =470nF, C _{CP} =20nF V _{DD} =12.5V~45V	-	25	50	ms
Sleep release stabilization time	t _{SLPR}	-	22	28	34	ms

(*1) t_{RDY} starts when all of the recovery-detection voltages of VREG50、VREG33、and VDDL are exceeded.
(*2) This output time is also required when returning from a state where DFET/PRDFET are OFF and RSNS is pulled up.



• Functional Description

MCU Interface

The ML5262 has SPI and I2C serial interfaces, and the SPI serial interface is enabled by the initial setting. It is also possible to set the I2C serial interface at the time of shipment.

Various settings are made by reading and writing data to each address in the control register. Data is written in units of 1 word (2 bytes). When writing data, set the R/W bit following the target address to "0"; when reading data, set the R/W bit to "1". The initial value of the target address is set to 0x64.

A CRC (Cycle Redundancy Code) generated by the polynomial X^8+X^2+X+1 is added to each word, and the initial value of the CRC calculation is 0x00. A data write operation to the specified register is performed only if the CRC calculation result and the received

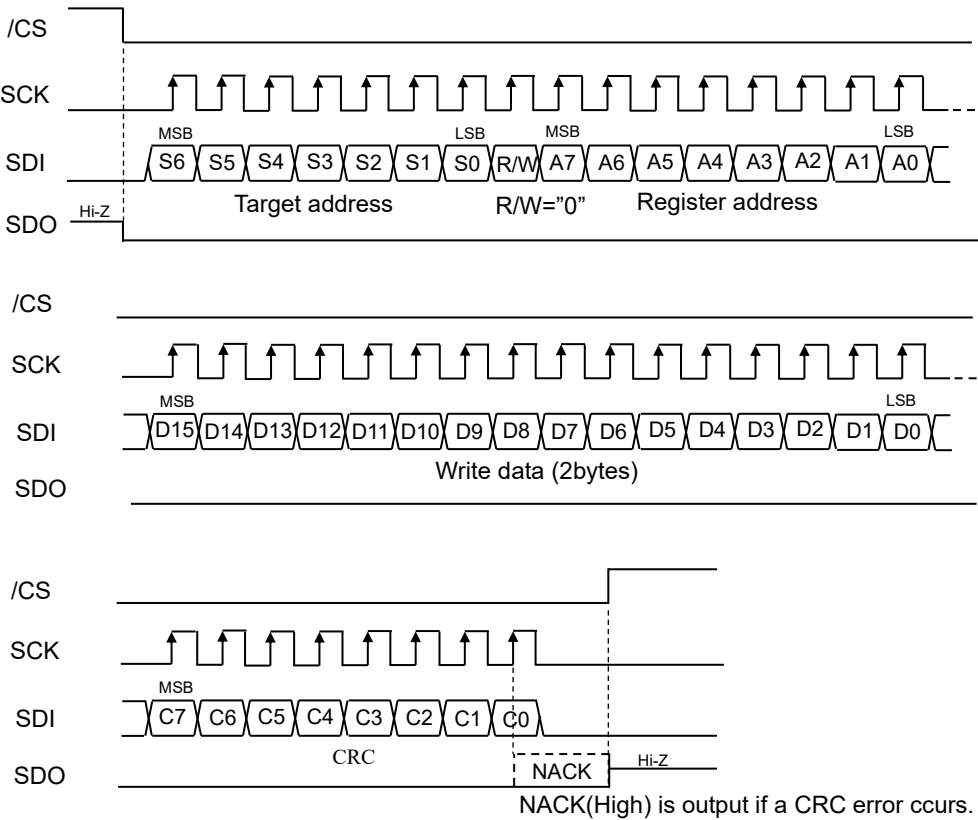
CRC code match. If they do not match, the data write operation is not performed and a NACK is returned.

It is also possible to set it so that the CRC is not added. For details, refer to the MCUIF register description.

1.SPI Serial Interface

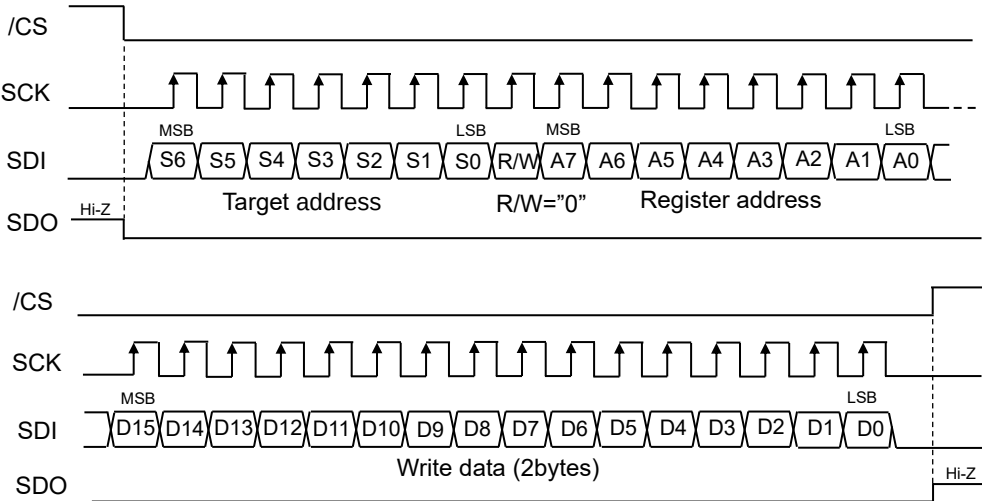
Setting the /CS pin to the "L" level enables the SPI interface and input data on the SDI pin is taken into the LSI with MSB first, synchronized with the rising edge of the input clock to the SCK pink. Reading data is output to the SDO pin with MSB first, synchronized with the falling edge of the input clock to the SCK pin. Setting the /CS pin to the "H" level disables the SPI interface and returns to the initial state.

1-1.Communication format when writing data (with CRC)



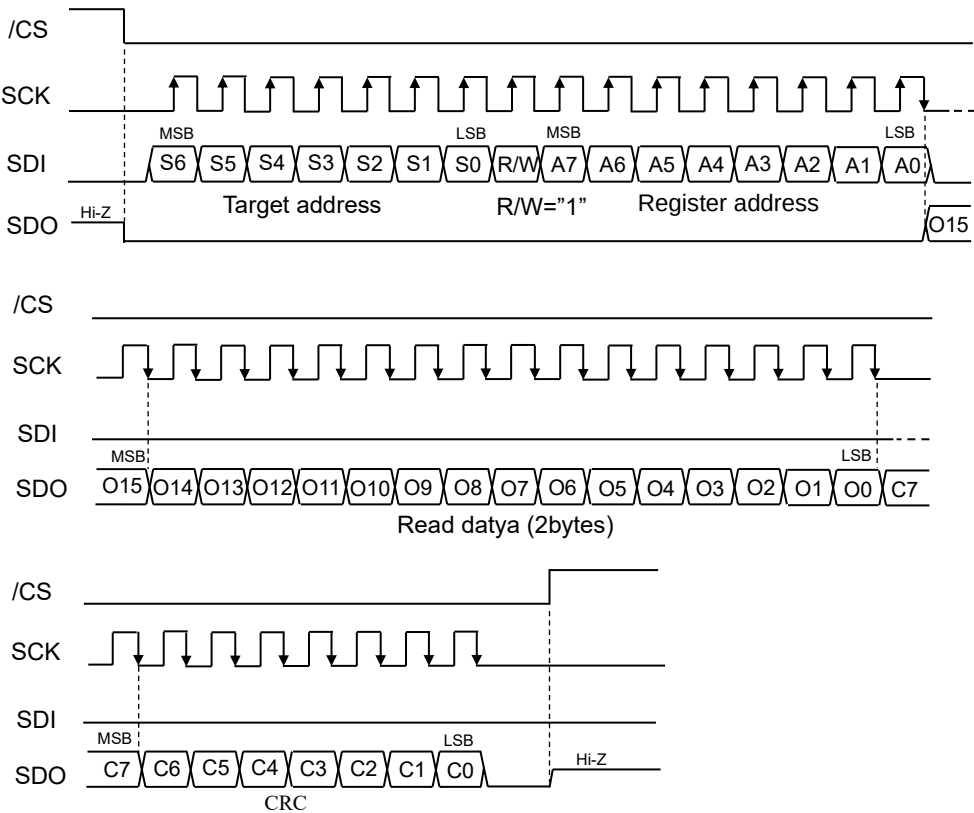
The address is automatically incremented, so continuous data can be written by repeatedly sending 1 word of writing data and the CRC.
The CRC added first is calculated from the target address + R/W bit, register address, and 1 word of write data. However, when writing continuous data, the CRC is calculated from only the 1 word of writing data.

1-2. Communication format when writing data (without CRC)



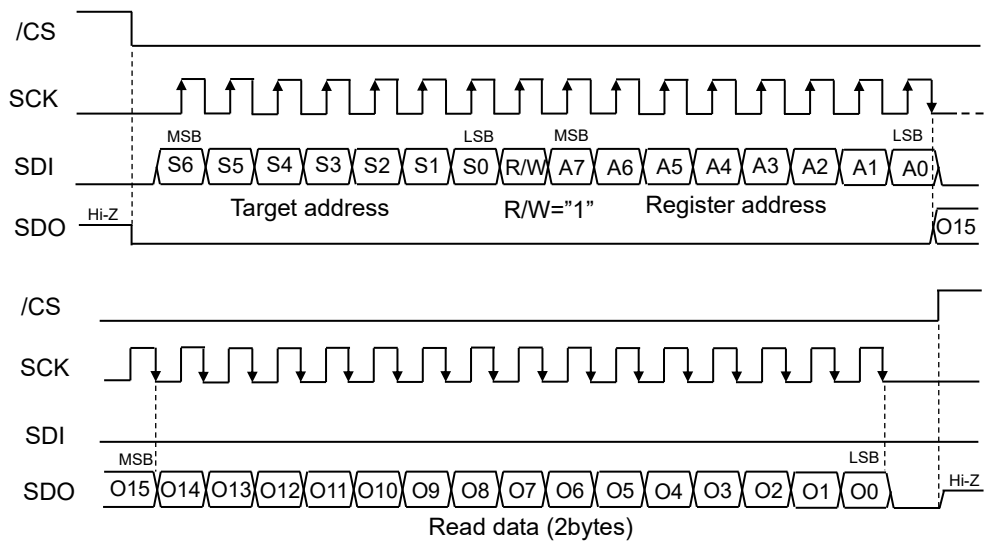
The address is automatically incremented, so continuous data can be written by repeatedly sending one word of writing data.

1-3. Communication format when reading data (with CRC)



The address is automatically incremented, so by continuing to input SCK, one word of read data and CRC will be repeatedly output. The CRC added first is calculated from the target address + R/W bit, register address, and 1 word of read data. However, when reading continuous data, the CRC is calculated from only the 1 word of read data.

1-4. Communication format when reading data (without CRC)

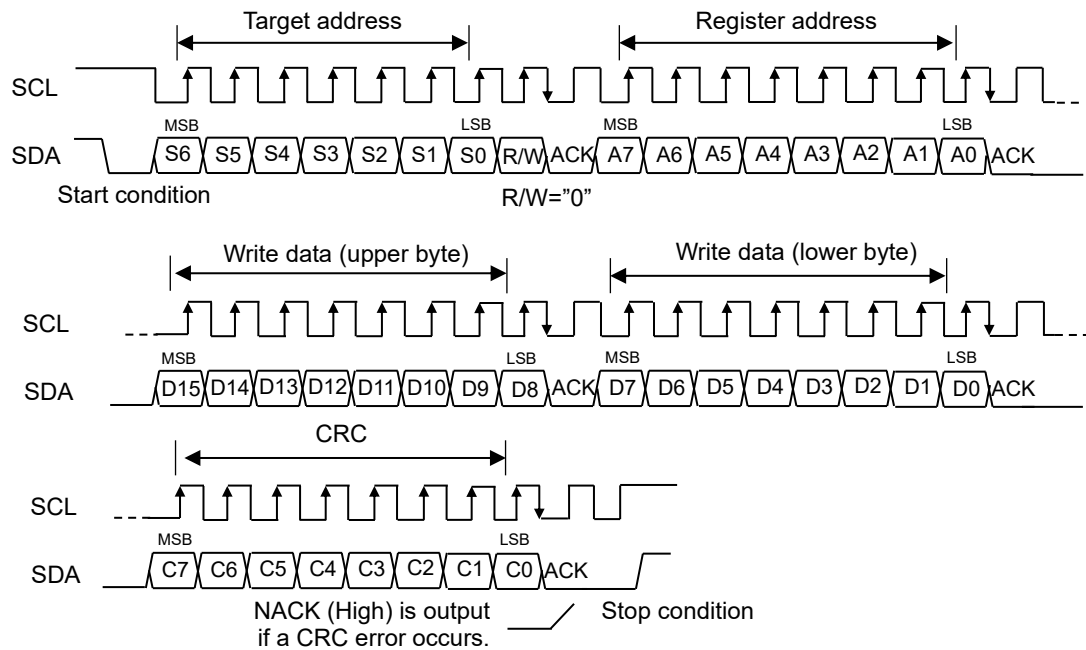


The address is automatically incremented, so by continuing to input SCK, one word of read data is repeatedly output.

2.I2C Serial Interface

Input data on the SDA pin is taken into the LSI with MSB first, synchronized with the rising edge of the input clock to the SCL pin. Output data is output to the SDA pin with MSB first, synchronized with the falling edge of the input clock to the SCL pin.

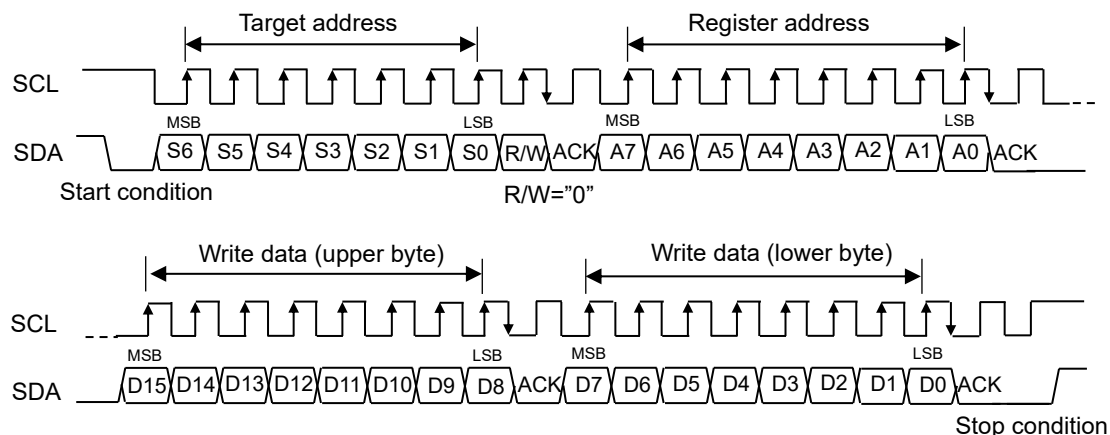
2-1. Communication format when writing data (with CRC)



The address is automatically incremented, so continuous data can be written by repeatedly sending 1 word of writing data and the CRC.

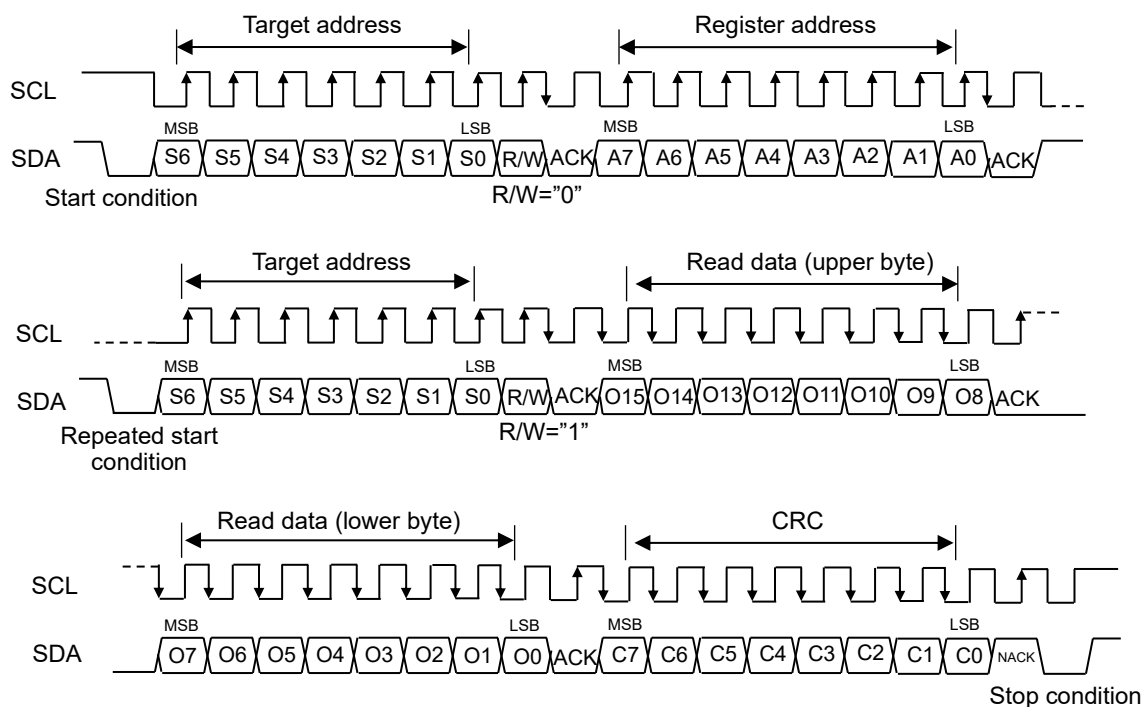
The CRC added first is calculated from the target address + R/W bit, register address, and 1 word of write data. However, when writing continuous data, the CRC is calculated from only the 1 word of writing data.

2-2. Communication format when writing data (without CRC)



The address is automatically incremented, so continuous data can be written by repeatedly sending one word of writing data.

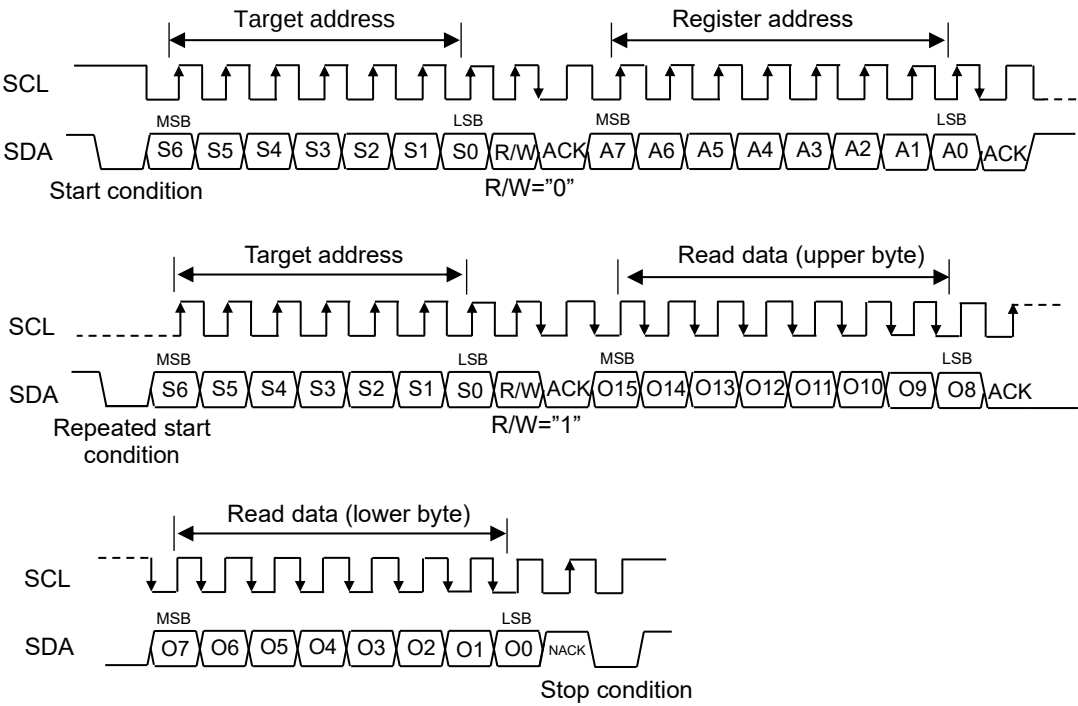
2-3. Communication format when reading data (with CRC)



The address is automatically incremented, so continuous reading data can be performed.

The CRC added initially is calculated from the target address + R/W bit after the start condition, the register address, the target address + R/W bit after the restarted start condition, and 1 word of read data, but the CRC when reading continuous data is calculated from only 1 word of read data.

2-4. Communication format when reading data (without CRC)



The address is automatically incremented, so continuous reading data can be performed.

Control Registers

The control register map is shown below.

Address	Register name	R/W	Initial Value	Register Overview
0x00	NOOP	R/W	0x0000	User register
0x01	MCUIF	R/W	0x6400	MCU interface option / Target address register
0x02	SEL	R/W	0x0000	Number of connected cells, TEMP pin for measurement, Current measurement gain, Coulomb counter operation setting register
0x03	PERIOD	R/W	0x0000	Measurement interval time setting register
0x04	INT_EN1	R/W	0x0001	Interrupt enable 1 register
0x05	INT_EN2	R/W	0x0000	Interrupt enable 2 register
0x06	INT_EN3	R/W	0x0000	Interrupt enable 3 register
0x07	INT_REQ1	R/W	0x0001	Interrupt request 1 register
0x08	INT_REQ2	R/W	0x0000	Interrupt request 2 register
0x09	INT_REQ3	R/W	0x0000	Interrupt request 3 register
0x0A	POWER	R/W	0x0A2A	Power control register
0x0B	FETCBAL	R/W	0x0081	FET/ Cell balancing setting register
0x0C	CBAL	R/W	0x0000	Cell balancing execution/monitor register 1
0x0D	-	R	-	Reserved register
0x0E	STATUS1	R	0x8041	Status register 1
0x0F	STATUS2	R	0x0000	Status register 2
0x10	LOCK	R/W	0x0000	Access permission register for protection function setting register
0x11	SETOV	R/W	0x0000	Overvoltage detection operation setting register
0x12	OVDET	R/W	0x0000	Overvoltage detection threshold setting register
0x13	OVRCV	R/W	0x0000	Overvoltage release threshold setting register
0x14	SETUV	R/W	0x0000	Undervoltage detection operation setting register
0x15	UVDET	R/W	0x0000	Undervoltage detection threshold setting register
0x16	UVRCV	R/W	0x0000	Undervoltage release threshold setting register
0x17	SETOCC	R/W	0x0000	Charging overcurrent detection operation setting register
0x18	SETOCD1	R/W	0x0000	Discharge overcurrent detection operation setting register 1
0x19	SETOCD2	R/W	0x0000	Discharge overcurrent detection operation setting register 2
0x1A	SCWDT	R/W	0x0000	Short-circuit current detection operation/WDT setting register
0x1B	CHG	R/W	0x0000	Charging condition detection operation setting register
0x1C	DSG	R/W	0x0000	Discharge condition detection operation setting register
0x1D	CCMASK	R/W	0x0000	Coulomb counter mask current control register
0x1E	PWRDLY	R/W	0x0000	Power status transition delay timer setting register
0x1F	SETOTUT	R/W	0x0000	Temperature detection operation setting register
0x20	OTD1	R/W	0x0000	TEMP1 discharge prohibition overtemperature detection threshold setting register
0x21	OTD2	R/W	0x0000	TEMP2 discharge prohibition overtemperature detection threshold setting register
0x22	OTD3	R/W	0x0000	TEMP3 discharge prohibition overtemperature detection threshold setting register
0x23	OTD4	R/W	0x0000	TEMP4 discharge prohibition overtemperature detection threshold setting register
0x24	OTDR1	R/W	0x0000	TEMP1 discharge prohibition overtemperature release threshold setting register
0x25	OTDR2	R/W	0x0000	TEMP2 discharge prohibition overtemperature release threshold setting register
0x26	OTDR3	R/W	0x0000	TEMP3 discharge prohibition overtemperature release threshold setting register
0x27	OTDR4	R/W	0x0000	TEMP4 discharge prohibition overtemperature release threshold setting register
0x28	UTD1	R/W	0x0000	TEMP1 discharge prohibition undertemperature detection threshold setting register
0x29	UTD2	R/W	0x0000	TEMP2 discharge prohibition undertemperature detection threshold setting register
0x2A	UTD3	R/W	0x0000	TEMP3 discharge prohibition undertemperature detection threshold setting register
0x2B	UTD4	R/W	0x0000	TEMP4 discharge prohibition undertemperature detection threshold setting register
0x2C	UTDR1	R/W	0x0000	TEMP1 discharge prohibition undertemperature release threshold setting register

Address	Register name	R/W	Initial Value	Register Overview
0x2D	UTDR2	R/W	0x0000	TEMP2 discharge prohibition undertemperature release threshold setting register
0x2E	UTDR3	R/W	0x0000	TEMP3 discharge prohibition undertemperature release threshold setting register
0x2F	UTDR4	R/W	0x0000	TEMP4 discharge prohibition undertemperature release threshold setting register
0x30	OTC1	R/W	0x0000	TEMP1 charging prohibition overtemperature detection threshold setting register
0x31	OTC2	R/W	0x0000	TEMP2 charging prohibition overtemperature detection threshold setting register
0x32	OTC3	R/W	0x0000	TEMP3 charging prohibition overtemperature detection threshold setting register
0x33	OTC4	R/W	0x0000	TEMP4 charging prohibition overtemperature detection threshold setting register
0x34	OTCR1	R/W	0x0000	TEMP1 charging prohibition overtemperature release threshold setting register
0x35	OTCR2	R/W	0x0000	TEMP2 charging prohibition overtemperature release threshold setting register
0x36	OTCR3	R/W	0x0000	TEMP3 charging prohibition overtemperature release threshold setting register
0x37	OTCR4	R/W	0x0000	TEMP4 charging prohibition overtemperature release threshold setting register
0x38	UTC1	R/W	0x0000	TEMP1 charging prohibition undertemperature detection threshold setting register
0x39	UTC2	R/W	0x0000	TEMP2 charging prohibition undertemperature detection threshold setting register
0x3A	UTC3	R/W	0x0000	TEMP3 charging prohibition undertemperature detection threshold setting register
0x3B	UTC4	R/W	0x0000	TEMP4 charging prohibition undertemperature detection threshold setting register
0x3C	UTCR1	R/W	0x0000	TEMP1 charging prohibition undertemperature release threshold setting register
0x3D	UTCR2	R/W	0x0000	TEMP2 charging prohibition undertemperature release threshold setting register
0x3E	UTCR3	R/W	0x0000	TEMP3 charging prohibition undertemperature release threshold setting register
0x3F	UTCR4	R/W	0x0000	TEMP4 charging prohibition undertemperature release threshold setting register
0x40	CBALEN	R/W	0x0000	Cell balancing permission voltage setting register
0x41	CBALST	R/W	0x0000	Cell balancing start potential difference setting register
0x42	CBALSP	R/W	0x0000	Cell balancing end potential difference setting register
0x43	PREDSG	R/W	0x0000	Pre-discharge setting register
0x44	SETSOV	R/W	0x0000	Secondary overvoltage detection operation setting register
0x45	SOVDET	R/W	0x0000	Secondary overvoltage detection threshold setting register
0x46	SETSUV	R/W	0x0000	Secondary undervoltage detection operation setting register
0x47	SUVDET	R/W	0x0000	Secondary undervoltage detection threshold setting register
0x48	S OCC	R/W	0x0000	Secondary charging overcurrent operation setting register
0x49	S O C D	R/W	0x0000	Secondary discharge overcurrent operation setting register
0x4A	SETSOT	R/W	0x0000	Secondary overtemperature detection operation setting register
0x4B	S O T	R/W	0x0000	Secondary overtemperature detection threshold setting register
0x4C	SCFET	R/W	0x0000	CFET failure detection operation setting register
0x4D	SDFET	R/W	0x0000	DFET failure detection operation setting register
0x4E	FUSE	R/W	0x0000	Fuse pin output operation setting register
0x4F	VCELL1	R	0x0***	Cell 1 measurement result register
0x50	VCELL2	R	0x0***	Cell 2 measurement result register
0x51	VCELL3	R	0x0***	Cell 3 measurement result register
0x52	VCELL4	R	0x0***	Cell 4 measurement result register
0x53	VCELL5	R	0x0***	Cell 5 measurement result register
0x54	VCELL6	R	0x0***	Cell 6 measurement result register
0x55	VCELL7	R	0x0***	Cell 7 measurement result register
0x56	VCELL8	R	0x0***	Cell 8 measurement result register
0x57	VCELL9	R	0x0***	Cell 9 measurement result register
0x58	VCELL10	R	0x0***	Cell 10 measurement result register
0x59	-	R	-	Reserved register
0x5A	G1_ICELL1	R	0x7FFF	Current measurement result register for cell 1 (Gainx1)

Address	Register name	R/W	Initial Value	Register Overview
0x5B	G1_ICELL2	R	0x7FFF	Current measurement result register for cell 2 (Gainx1)
0x5C	G1_ICELL3	R	0x7FFF	Current measurement result register for cell 3 (Gainx1)
0x5D	G1_ICELL4	R	0x7FFF	Current measurement result register for cell 4 (Gainx1)
0x5E	G1_ICELL5	R	0x7FFF	Current measurement result register for cell 5 (Gainx1)
0x5F	G1_ICELL6	R	0x7FFF	Current measurement result register for cell 6 (Gainx1)
0x60	G1_ICELL7	R	0x7FFF	Current measurement result register for cell 7 (Gainx1)
0x61	G1_ICELL8	R	0x7FFF	Current measurement result register for cell 8 (Gainx1)
0x62	G1_ICELL9	R	0x7FFF	Current measurement result register for cell 9 (Gainx1)
0x63	G1_ICELL10	R	0x7FFF	Current measurement result register for cell 10 (Gainx1)
0x64	G4_ICELL1	R	0x7FFF	Current measurement result register for cell 1 (Gainx4)
0x65	G4_ICELL2	R	0x7FFF	Current measurement result register for cell 2 (Gainx4)
0x66	G4_ICELL3	R	0x7FFF	Current measurement result register for cell 3 (Gainx4)
0x67	G4_ICELL4	R	0x7FFF	Current measurement result register for cell 4 (Gainx4)
0x68	G4_ICELL5	R	0x7FFF	Current measurement result register for cell 5 (Gainx4)
0x69	G4_ICELL6	R	0x7FFF	Current measurement result register for cell 6 (Gainx4)
0x6A	G4_ICELL7	R	0x7FFF	Current measurement result register for cell 7 (Gainx4)
0x6B	G4_ICELL8	R	0x7FFF	Current measurement result register for cell 8 (Gainx4)
0x6C	G4_ICELL9	R	0x7FFF	Current measurement result register for cell 9 (Gainx4)
0x6D	G4_ICELL10	R	0x7FFF	Current measurement result register for cell 10 (Gainx4)
0x6E	G1_CURR	R	0x7FFF	Current measurement result register (Gainx1)
0x6F	G4_CURR	R	0x7FFF	Current measurement result register (Gainx4)
0x70	CCL	R	0x****	Coulomb counter result register (lower 16 bits)
0x71	CCH	R	0x****	Coulomb counter result register (upper 16 bits)
0x72	INTEGCL	R/W	0x0000	Current integration result register (lower 16 bits)
0x73	INTEGCH	R/W	0x0000	Current integration result register (upper 16 bits)
0x74	TEMP1	R	0x0***	TEMP1 pin voltage measurement result register
0x75	TEMP2	R	0x0***	TEMP2 pin voltage measurement result register
0x76	TEMP3	R	0x0***	TEMP3 pin voltage measurement result register
0x77	TEMP4	R	0x0***	TEMP4 pin voltage measurement result register
0x78	PSNS	R	0x0***	PSNS pin voltage measurement result register
0x79	RSNS	R	0x0***	RSNS pin voltage measurement result register
0x7A	VDD	R	0x0***	VDD pin voltage measurement result register
0x7B	VGAIN	R/W	(*1)	Gain correction value setting register when measuring cell voltage
0x7C	VOFST	R/W	(*1)	Offset correction value setting register when measuring cell voltage
0x7D	CC_CAL	R/W	0x0000	Coulomb counter calibration setting register
0x7E	G1_CC_GAIN	R/W	(*1)	Gain correction value setting register when measuring current (Gainx1)
0x7F	G1_CC_OFST	R/W	(*1)	Offset correction value setting register when measuring current (Gainx1)
0x80	G4_CC_GAIN	R/W	(*1)	Gain correction value setting register when measuring current (Gainx4)
0x81	G4_CC_OFST	R/W	(*1)	Offset correction value setting register when measuring current (Gainx4)
0x82	RTEMP12	R/W	(*1)	Built-in 10kΩ correction resistor for TEMP1 and TEMP2 pins
0x83	RTEMP34	R/W	(*1)	Built-in 10kΩ correction resistor for TEMP3 and TEMP4 pins
0x84	OTPACPT	R/W	0x0000	OTP register access permission register
0x85	OTP	R/W	0x0000	OTP load control register
0x86~ 0xFF	<Reserve>	R	-	Reserved register

(*1) The initial value is the correction value obtained during the LSI manufacturing process.

For the OTP setting values, please refer to the attached document "ML5262_Code_list".

Please note that OTP programming operation is not guaranteed for mass-production units (OTP programming for mass-production devices is performed within the LSI manufacturing process).

1. NOOP register (Adrs = 0x00)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	NOP[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No function is assigned to the NOOP register, so read/write access to this register does not change the LSI state. Written data can be read as is.

2. MCUIF register (Adrs = 0x01)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	SADRS[6:0]								-	-	-	-	-	CRC	I2C
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W
Initial Value	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0

The MCUIF register is used to set the MCU serial interface, the presence/absence of CRC, and the target address.

- 1) The I2C bit selects the MCU interface.
Even if the I2C bit is changed, it does not take effect immediately and becomes valid only when it is loaded from the OTP memory.

I2C	MCU interface
0	SPI interface (initial value)
1	I2C interface

- 2) The CRC bit sets whether or not to include of CRC.
If the CRC bit is set to "1", the CRC will be added from the next communication.

CRC	with/without CRC
0	without CRC (initial Value)
1	with CRC

- 3) The SADRS[6:0] bits set the target address. The initial value is set to 0x64.
The serial interface is enabled when the received target address data matches SADRS[6:0].

3. SEL register (Adrs = 0x02)

	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	CSEL[2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	ENCC	IGAIN	-	-	TSEL[3:0]			
R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The SEL register is used to set the number of connected battery cells, the TEMP pin for measurement, the current measurement gain factor, and the coulomb counter operation.

- 1) The CSEL[2:0] bits set the number of connected battery cells.

CSEL[2:0]	Number of battery cells
0x0	10 cells (initial value)
0x1	9 cells
0x2	8 cells
0x3	7 cells
0x4	6 cells
0x5	5 cells
0x6	4 cells
Others	10 cells

- 2) The TSEL[3:0] bits set the TEMP pin for temperature measurement.

TSEL[0]	TEMP1 pin
0	Do not measure (initial value)
1	Measure

TSEL[1]	TEMP2 pin
0	Do not measure (initial value)
1	Measure

TSEL[2]	TEMP3 pin
0	Do not measure (initial value)
1	Measure

TSEL[3]	TEMP4 pin
0	Do not measure (initial value)
1	Measure

- 3) The IGAIN bit set the gain factor for current measurement.

IGAIN	Gain factor
0	1x (initial value)
1	4x

- 4) The ENCC bit set the coulomb counter operation.

ENCC	Coulomb counter operation
0	Stop (initial value)
1	Activate

4. PERIOD register (Adrs = 0x03)

	7	6	5	4	3	2	1	0
Bit name	-	-	CC[1:0]		TTP[1:0]		TVC[1:0]	
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	-	-	-	-	TTPP[1:0]		TVCP[1:0]	
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The PERIOD register is used to set the measurement cycle in the normal state and power-save state.
Bits 15 to 12 shall be fixed at 0.

- 1) The TVC[1:0] bits set the cell voltage measurement cycle in the normal state.

TVC[1:0]	Cell voltage measurement cycle in the normal state
0x0	40ms (initial value)
0x1	200ms
0x2	300ms
0x3	400ms

- 2) The TTP[1:0] bits set the temperature measurement cycle in the normal state.

TTP[1:0]	Temperature measurement cycle in the normal state
0x0	Measured after every cell voltage measurement cycle(initial value)
0x1	Measured once every two cell voltage measurements cycles
0x2	Measured once every four cell voltage measurements cycles
0x3	Measured once every eight cell voltage measurements cycles

- 3) The CC[1:0] bits set the coulomb counter interrupt generation period.

CC[1:0]	Coulomb counter interrupt generation cycle
0x0	250ms (initial value)
0x1	500ms
0x2	1000ms
0x3	2000ms

- 4) TVCP[1:0] bits set the cell voltage measurement cycle in the power-save state.

TVCP[1:0]	Cell voltage measurement cycle in the power-save state
0x0	1s (initial value)
0x1	2s
0x2	4s
0x3	8s

- 5) TTPP[1:0] bits set the temperature measurement cycle in the power-save state.

TTPP[1:0]	Temperature measurement cycle in the power-save state
0x0	Measured after every cell voltage measurement cycle(initial value)
0x1	Measured once every two cell voltage measurements cycles
0x2	Measured once every four cell voltage measurements cycles
0x3	Measured once every eight cell voltage measurements cycles

5. INT_EN1 register (Adrs = 0x04)

	7	6	5	4	3	2	1	0
Bit name	ESLPR	ESLP	EPSR	EPSD	EPRDSG	ECC	EVM	ERDY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
Bit name	EOCDR1	EOCD1	EOCCR	EOCC	EUVR	EUV	EOVR	EOV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The INT_EN1 register is used to set whether or not to enable the output of interrupt signals to the /INTO pin. Setting each bit to "1" enables the interrupt signal output of the INT_REQ1 register, and setting each bit to "0" disables it. The interrupt signals that each bit enables are as follows:

Bit name	Interrupt signal name
ERDY	Initialization completion interrupt
EVM	Various voltage measurement completion interrupt
ECC	Coulomb counter integration completion interrupt
EPRDSG	Pre-discharge completion interrupt
EPSD	Power-save state transition interrupt
EPSR	Returning from power-save mode to normal mode interrupt
ESLP	Sleep state transition interrupt
ESLPR	Returning from sleep mode to normal mode interrupt
EOV	Overvoltage detection interrupt
EOVR	Overvoltage release interrupt
EUV	Undervoltage detection interrupt
EUVR	Undervoltage release interrupt
EOCC	Charging overcurrent detection interrupt
EOCCR	Charging overcurrent release (charger release detection) interrupt
EOCD1	Discharge overcurrent 1 detection interrupt
EOCDR1	Discharge overcurrent 1 release (load release detection) interrupt

6. INT_EN2 register (Adrs = 0x05)

	7	6	5	4	3	2	1	0
Bit name	EOTDR	EOTD	EOTCR	EOTC	ESCR	ESC	EOCDR2	EOCD2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	EWKUP	ECCCAL	EOTP	EWDT	EUTDR	EUTD	EUTCR	EUTC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The INT_EN2 register is used to set whether or not to enable the output of interrupt signals to the /INTO pin. Setting each bit to "1" enables the interrupt signal output of the INT_REQ2 register, and setting each bit to "0" disables it. The interrupt signals that each bit enables are as follows:

Bit name	Interrupt signal name
EOCD2	Discharge overcurrent 2 detection interrupt
EOCDR2	Discharge overcurrent 2 release (load release detection) interrupt
ESC	Short-circuit current detection interrupt
ESCR	Short-circuit current detection release (load release detection) interrupt
EOTC	Charging prohibition overtemperature detection interrupt
EOTCR	Charging prohibition overtemperature detection release interrupt
EOTD	Discharge prohibition overtemperature detection interrupt
EOTDR	Discharge prohibition overtemperature detection release interrupt
EUTC	Charging prohibition undertemperature detection interrupt
EUTCR	Charging prohibition undertemperature detection release interrupt
EUTD	Discharge prohibition undertemperature detection interrupt
EUTDR	Discharge prohibition undertemperature detection release interrupt
EWDT	WDT detection interrupt
EOTP	OTP memory access completion interrupt
ECCCAL	Coulomb counter calibration completion interrupt
EWKUP	WKUP detection interrupt

7. INT_EN3 register (Adrs = 0x06)

	7	6	5	4	3	2	1	0
Bit name	EFUSE	ESDFET	ESCFET	ESOT	ESOCD	ESOCC	ESUV	ESOV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	-	-	-	-	-	EORG	EUVLO3	EUVLO5
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The INT_EN3 register is used to set whether or not to enable the output of interrupt signals to the /INTO pin. Setting each bit to "1" enables the interrupt signal output of the INT_REQ3 register, and setting each bit to "0" disables it.

The interrupt signals that each bit enables are as follows:

Bit name	Interrupt signal name
ESOV	Secondary overvoltage detection interrupt
ESUV	Secondary undervoltage detection interrupt
ESOCC	Secondary charging overcurrent detection interrupt
ESOCD	Secondary discharge overcurrent detection interrupt
ESOT	Secondary overtemperature detection interrupt
ESCFET	Charging control FET failure detection interrupt
ESDFET	Discharge control FET failure detection interrupt
EFUSE	Fuse cut completion interrupt
EUVLO5	VREG50 output voltage drop detection interrupt
EUVLO3	VREG33 output voltage drop detection interrupt
EORG	Current-measurment result over-range detection interrupt

8. INT_REQ1 register (Adrs = 0x07)

	7	6	5	4	3	2	1	0
Bit name	QSLPR	QSLP	QPSR	QPSD	QPRDSG	QCC	QVM	QRDY
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
Bit name	QOCDR1	QOCD1	QOCCR	QOCC	QUVR	QUV	QOVR	QOV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The INT_REQ1 register is an interrupt request flag register. Each interrupt request flag is set to "1" when an interrupt occurs, regardless of the setting of the INT_EN1 register. An "L" level is output to the /INTO pin only when an interrupt enabled in the INT_EN1 register occurs.

The interrupt is cleared by writing data "1". When clear only one interrupt, write "0" to the other bits. When all enabled interrupt request flags are cleared to "0", the /INTO pin output goes to the "Hi-Z" level.

Bit name	Interrupt signal name
QRDY	Initialization completion interrupt
QVM	Voltage measurement completion interrupt
QCC	Coulomb counter integration completion interrupt
QPRDSG	Pre-discharge completion interrupt
QPSD	Power-save state transition interrupt
QPSR	Returning from power-save mode to normal mode interrupt
QSLP	Sleep state transition interrupt
QSLPR	Returning from sleep mode to normal mode interrupt
QOV	Overvoltage detection interrupt
QOVR	Overvoltage release interrupt
QUV	Undervoltage detection interrupt
QUVR	Undervoltage release interrupt
QOCC	Charging overcurrent detection interrupt
QOCCR	Charging overcurrent release (charger release detection) interrupt
QOCD1	Discharge overcurrent 1 detection interrupt
QOCDR1	Discharge overcurrent 1 release (load release detection) interrupt

9. INT_REQ2 register (Adrs = 0x08)

	7	6	5	4	3	2	1	0
Bit name	QOTDR	QOTD	QOTCR	QOTC	QSCR	QSC	QOCDR2	QOCD2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	QWKUP	QCCCAL	QOTP	QWDT	QUTDR	QUTD	QUTCR	QUTC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The INT_REQ2 register is an interrupt request flag register. Each interrupt request flag is set to "1" when an interrupt occurs, regardless of the setting of the INT_EN2 register. An "L" level is output to the /INTO pin only when an interrupt enabled in the INT_EN2 register occurs.

The interrupt is cleared by writing data "1". When clear only one interrupt, write "0" to the other bits. When all enabled interrupt request flags are cleared to "0", the /INTO pin output goes to the "Hi-Z" level.

Bit name	Interrupt signal name
QOCD2	Discharge overcurrent 2 detection interrupt
QOCDR2	Discharge overcurrent 2 release (load release detection) interrupt
QSC	Short-circuit current detection interrupt
QSCR	Short-circuit current detection release (load release detection) interrupt
QOTC	Charging prohibition overtemperature detection interrupt
QOTCR	Charging prohibition overtemperature detection release interrupt
QOTD	Discharge prohibition overtemperature detection interrupt
QOTDR	Discharge prohibition overtemperature detection release interrupt
QUTC	Charging prohibition undertemperature detection interrupt
QUTCR	Charging prohibition undertemperature detection release interrupt
QUTD	Discharge prohibition undertemperature detection interrupt
QUTDR	Discharge prohibition undertemperature detection release interrupt
QWDT	WDT detection interrupt
QOTP	OTP memory access completion interrupt
QCCCAL	Coulomb counter calibration completion interrupt
QWKUP	WKUP detection interrupt

10. INT_REQ3 register (Adrs = 0x09)

	7	6	5	4	3	2	1	0
Bit name	QFUSE	QSDFET	QSCFET	QSOT	QSOCD	QSOCC	QSUV	QSOV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	-	-	-	-	-	QORG	QUVLO3	QUVLO5
R/W	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The INT_REQ3 register is an interrupt request flag register. Each interrupt request flag is set to "1" when an interrupt occurs, regardless of the setting of the INT_EN3 register. An "L" level is output to the /INTO pin only when an interrupt enabled in the INT_EN3 register occurs.

The interrupt is cleared by writing data "1". When clear only one interrupt, write "0" to the other bits. When all enabled interrupt request flags are cleared to "0", the /INTO pin output goes to the "Hi-Z" level.

Bit name	Interrupt signal name
QSOV	Secondary overvoltage detection interrupt
QSUV	Secondary undervoltage detection interrupt
QSOCC	Secondary charging overcurrent detection interrupt
QSOCD	Secondary discharge overcurrent detection interrupt
QSOT	Secondary overtemperature detection interrupt
QSCFET	Charging control FET failure detection interrupt
QSDFET	Discharge control FET failure detection interrupt
QFUSE	Fuse cut completion interrupt
QUVLO5	VREG50 output voltage drop detection interrupt
QUVLO3	VREG33 output voltage drop detection interrupt
QORG	Current-measurment result over-range detection interrupt

11. POWER register (Adrs = 0x0A)

	7	6	5	4	3	2	1	0
Bit name	PUPIN	PSNS	ENPD	PD	ENSLP	SLP	ENPSV	PSV
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	-	-	1	0	1	0	1	0

	15	14	13	12	11	10	9	8
Bit name	-	-	-	WKUP	ENRSNS	RSNSPU	ENPSNS	PSNSPD
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	1	0	1	0

The POWER register controls various power controls, the connection of the PSNS pin pull-down resistor, and the RSNS pin pull-up resistor.

- 1) The ENPSV and PSV bits are used to set the transition to the power-save state (the measurement cycle becomes slower, which reduces current consumption).

ENPSV	PSV	Transition to power-save state
0	-	Standalone control
1	0	Normal state (initial value)
1	1	Power-save state

When the ENPSV bit is "1", the PSV bit setting is valid.

- When "1" is written to the PSV bit, the LSI will enter the power-save state from the next measurement cycle.
- When "0" is written to the PSV bit, then return to the normal state at any time within 1 second.

When "0" is written to the ENPSV bit, the LSI will set the standalone control.

In the standalone control, if no charging/discharge current flows for the time specified in the PWRDLY register, the LSI automatically enters the power-save state and automatically returns to the normal state when the charging/discharge current flows. For details, refer to the CHG, DSG, and PWRDLY register.

- 2) The ENSLP and SLP bits are used to set the transition to the sleep state (all measurement functions are halted, which reduces current consumption. Only control-register access is allowed).

ENSLP	SLP	Transition to sleep state
0	-	Standalone control
1	0	Normal state (initial value)
1	1	Sleep state

When the ENSLP bit is "1", the SLP bit setting is valid.

- When "1" is written to the SLP bit, the LSI will enter the sleep-save state from the next measurement cycle.
- When "0" is written to the SLP bit, the LSI returns to the normal state after the 28ms stabilization time has elapsed.

When the LSI returns from the sleep state due to the WKUP detection function during the sleep state, the SLP bit is reset to "0".

There are two conditions required to transition to the sleep state: the PSNS pin state and the /PUPIN pin State.

- The LSI will not enter the sleep state until the PSNS pin voltage becomes equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}). Before setting the SLP bit to "1", verify using the "PSNS Pin State Check Method" that the PSNS pin is not at the "H" level.

[PSNS Pin State Check Method]

The PSNS pin condition can be read using the PSNS bit. Set the C_FET and D_FET pins to the OFF condition, connect a 500kΩ pull-up resistor to the PSNS pin, and then check that the PSNS pin condition.

PSNS	PSNS pin condition
0	"L" level
1	"H" level

- The LSI will not enter the sleep state until the /PUPIN pin goes to the "H" level. Before setting the SLP bit to "1", verify using the "/PUPIN Pin State Check Method" that the /PUPIN pin is not at the "L" level.

[/PUPIN Pin State Check Method]

The /PUPIN pin condition can be read using the /PUPIN bit. Check that the /PUPIN pin condition.

PUPIN	/PUPIN pin condition
0	"H" level
1	"L" level

Writing "0" is written to the ENSLP bit, the LSI is set to standalone control mode.

In the standalone control, after the power-save state has continued for the time set in the PWRDLY register, the subsequent operation is determined by the WKUP bit status as shown below.

WKUP	C_FET pin condition	D_FET pin condition
0	OFF	OFF
1	OFF	Previous state retention

[WKUP bit = "0"]

The C_FET and D_FET pins are automatically set to the OFF state, a 500 kΩ pull-down resistor is applied to the PSNS pin, and the LSI enters the sleep state. Upon entry into sleep, if a charger is connected and the PSNS pin and the PSNS pin voltage becomes equal to or higher than the charger-connection detection voltage V_{PC1} , or if an "L" level is input to the /PUPIN pin, the LSI returns to the normal state after a stabilization period of 28 ms.

[WKUP bit = "1"]

Only the C_FET pin is automatically turned OFF, and the LSI transitions to the sleep state. After entering the sleep state, if a charger is connected, return the LSI to the normal state by applying an "L" level to the /PUPIN pin.

3) The ENPD and PD bits are used to configure the transition to the power-down state (in which most circuit operation are halted, the LSI enters a low-current consumption state. And access to the control registers becomes unavailable).

ENPD	PD	Transition to the power-down state
0	*	Standalone control
1	0	Normal state or power-save state or sleep state (initial value)
1	1	Power-down state

When the ENPD bit is "1", the PD bit setting is valid.

- When "1" is written to the PD bit, the LSI will transition to the power-down state.

There are two conditions required to transition to the power-down state: the PSNS pin state and the /PUPIN pin state.

- The LSI will not enter the power-down state until the PSNS pin voltage becomes equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}). Before setting the PD bit to "1", verify using the "PSNS Pin State Check Method" that the PSNS pin is not at the "H" level.
- The LSI will not enter the power-down state until the /PUPIN pin goes to the "H" level. Before setting the PD bit to "1", verify using the "/PUPIN Pin State Check Method" that the /PUPIN pin is not at the "L" level.

When "0" is written to the ENPD bit, the LSI will set the standalone control.

In standalone control, after transitioning to the over-discharge detection state, the LSI enters the power-down state once the time specified in the PWRDLY register has elapsed.

However, if the PSNS pin input is at the "H" level or the /PUPIN pin input is at the "L" level, the LSI will not transition to the power-down state.

4) The ENPSNS and PSNSPD bits control the connection of a pull-down resistor to the PSNS pin.

ENPSNS	PSNSPD	PSNS pin condition
0	*	Pull-down resistor not connected
1	0	Pull-down resistor not connected (initial value)
1	1	500kΩ pull-down resistor connected

When the ENPSNS bit is "1", the PSNSPD bit setting is valid.

- When "1" is written to the PSNSPD bit, connects a pull-down resistor.
- When "0" is written to the PSNSPD bit, the pull-down resistor is disconnected.

- 5) The ENRSNS and RSNSPU bits control the connection of a pull-up resistor to the RSNS pin.

ENRSNS	RSNSPU	RSNS pin condition
0	*	Pull-up resistor not connected
1	0	Pull-up resistor not connected (initial value)
1	1	2MΩ pull-up resistor connected

When the ENRSNS bit is "1", the RSNSPU bit setting is valid.

- When "1" is written to the RSNSPU bit, connects a pull-up resistor.
- When "0" is written to the RSNSPU bit, the pull-up resistor is disconnected.

- 6) The WKUP bit control whether the WKUP detection circuit for discharge current is enabled or disabled.

When this function is enabled, the discharge control FET will not turn off when the LSI transitions to the sleep state under standalone control.

WKUP	WKUP detection operation
0	Stop (initial value)
1	Activate

12.FETCBAL register (Adrs = 0x0B)

	7	6	5	4	3	2	1	0
Bit name	ENCB	PSVCB	ENPRDF	PRDF	ENDF	DF	ENCF	CF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
Bit name	-	-	-	-	-	-	ENFUS	FUS
R/W	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The FETCBAL register controls the output of the C_FET, PRD_FET, D_FET, and FUSE pins, as well as cell balancing. When using the FET function, the operating voltage range is 4.5 to 45V.

- 1) The ENCF and CF bits control the C_FET pin output.

ENCF	CF	Charging control FET status	C_FET pin output voltage
0	*	Standalone control (initial value)	
1	0	OFF	FETS pin voltage : V_S
1	1	ON	V_S+13V

When the ENCF bit is "1", the CF bit setting is valid.

- 2) The ENDF and DF bits control the D_FET pin output.

ENDF	DF	Discharge control FET status	D_FET pin output voltage
0	*	Standalone control (initial value)	
1	0	OFF	FETS pin voltage : V_S
1	1	ON	V_S+13V

When the ENDF bit is "1", the DF bit setting is valid.

- 3) The ENPRDF and PRDF bits control the PRD_FET pin output.

ENPRDF	PRDF	Pre-discharge control FET status	PRD_FET pin output voltage
0	*	Standalone control (initial value)	
1	0	OFF	FETS pin voltage : V_S
1	1	ON	V_S+13V

When the ENPRDF bit is "1", the PRDF bit setting is valid.

- 4) The PSVCB bit sets the cell balancing operation in the power-save state.

The ENCB bit sets the cell balancing operation using the CBAL register, which is described later.

ENCB	PSVCB	Cell balancing operation in the power-save state
0	0	Prohibited
0	1	Permitted
1	*	CBAL register settings are valid (initial value)

When the ENCB bit is "0", the PSVCB bit setting is valid.

When the ENCB bit is "1", the CBAL register setting is valid.

When changing the ENCB bit from "1" to "0", set the CBAL register to 0b00000000 after the QVM bit in the INT_REQ1 register is set to "1", and then set the ENCB bit to "0".

There are no restrictions on changing the ENCB bit from "0" to "1".

- 5) The ENFUS and FUS bits control the FUSE pin output.

ENFUS	FUS	FUSE pin output
0	*	FUSE register setting is valid (initial value)
1	0	0V
1	1	VREG33

When the ENFUS bit is "1", the FUS bit setting is valid, and the FUSE register setting is invalid.

Also, the fuse cut completion interrupt QFUSE will not be generated.

The FUSE bit in the STATUS2 register is not set even if both the ENFUS bit and FUS bit are "1".

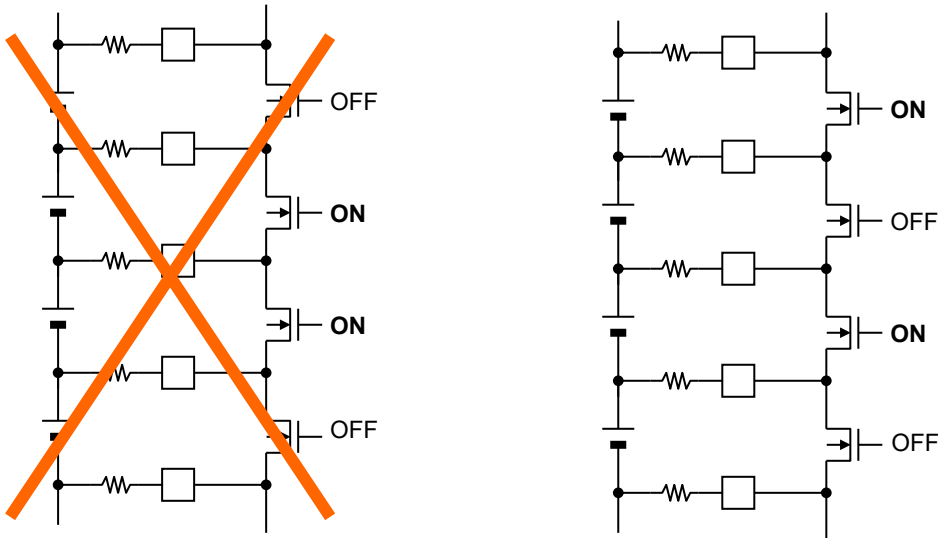
13.CBAL register (Adrs = 0x0C)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	CBAL[9:0]									
R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CBAL register is used to set the cell balancing switch on/off. The CBAL[9:0] bits control each cell on/off. The cell balancing execution period is the time other than the cell voltage measurement period, and the specified cell balancing switch is turned ON after completing the cell voltage measurement. If the setting is changed while executing cell balancing, it takes effect immediately. Also, when reading the CBAL register, any bit in the cell-balancing switch-ON permitted state will read as "1", regardless of the cell-balancing execution period.

CBAL[9:0]	Switch ON/OFF
0b0000000000	OFF (initial value)
0b0000000001	V1-V0 switch turned ON
0b0000000010	V2-V1 switch turned ON
0b0000000100	V3-V2 switch turned ON
0b0000001000	V4-V3 switch turned ON
0b0000010000	V5-V4 switch turned ON
0b0000100000	V6-V5 switch turned ON
0b0001000000	V7-V6 switch turned ON
0b0010000000	V8-V7 switch turned ON
0b0100000000	V9-V8 switch turned ON
0b1000000000	V10-V9 switch turned ON

It is possible to turn on multiple switches at the same time, but turning on adjacent cell balance switches is prohibited because this may cause damage to the built-in cell balance switch FETs. However, it is possible to turn on the cell balance switches for only the odd cells or only the even cells.



When switching the cell balance switch ON/OFF, be sure to set all cell balancing switches to OFF for 1 ms or more before turning them ON. Also, heat is generated by the cell balancing current and the ON resistance of the cell balancing switches, so set restrictions on the number of switches that are turned on and the ON time so that the power loss in the cell balancing switches does not exceed the allowable power dissipation.

14.STATUS1 register (Adrs = 0x0E)

	7	6	5	4	3	2	1	0
Bit name	OCC	UV	OV	SLP	PSV	PRDF	DF	CF
R/W	R	R	R	R	R	R	R	R
Initial Value	0	1	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
Bit name	INTO	PSNS	PUPIN	DSG	CHG	SC	OCD2	OCD1
R/W	R	R	R	R	R	R	R	R
Initial Value	1	-	-	0	0	0	0	0

The STATUS1 register indicates various conditions.

- 1) The CF bit indicates the C_FET pin status.

CF	C_FET pin output status
0	OFF
1	ON (initial value)

- 2) The DF bit indicates the D_FET pin status.

DF	D_FET pin output status
0	OFF (initial value)
1	ON

- 3) The PRDF bit indicates the PRD_FET pin status.

PRDF	PRD_FET pin output status
0	OFF (initial value)
1	ON

- 4) The PSV bit indicates whether the LSI is in the power-save state.

PSV	LSI state
0	Normal state (initial value)
1	Power-save state

- 5) The SLP bit indicates whether the LSI is in the sleep state.

SLP	LSI state
0	Normal state (initial value)
1	Sleep state

- 6) The OV bit indicates the overvoltage detection status.

OV	Overvoltage detection status
0	Undetected (initial value)
1	Detected

- 7) The UV bit indicates the undervoltage detection status.

UV	Undervoltage detection status
0	Undetected
1	Detected (initial value)

- 8) The OCC bit indicates the charging overcurrent detection status.

OCC	Charging overcurrent detection status
0	Undetected (initial value)
1	Detected

- 9) The OCD1 bit indicates the discharge overcurrent 1 detection status.

OCD1	Discharge overcurrent 1 detection status
0	Undetected (initial value)
1	Detected

- 10) The OCD2 bit indicates the discharge overcurrent 2 detection status.

OCD2	Discharge overcurrent 2 detection status
0	Undetected (initial value)
1	Detected

- 11) The SC bit indicates the short-circuit current detection status.

SC	Short-circuit current detection status
0	Undetected (initial value)
1	Detected

- 12) The CHG bit indicates the charging condition detection status.

CHG	Charging condition detection status
0	Undetected (initial value)
1	Detected

- 13) The DSG bit indicates the discharge condition detection status.

DSG	Discharge condition detection status
0	Undetected (initial value)
1	Detected

- 14) The PUPIN bit indicates the /PUPIN pin status.

PUPIN	/PUPIN pin output status
0	"H" level
1	"L" level

- 15) The PSNS bit indicates the PSNS pin status.

PSNS	PSNS pin output status
0	"L" level
1	"H" level

- 16) The INTO bit indicates the /INTO pin status.

INTO	/INTO pin output status
0	OFF
1	ON (initial value)

15.STATUS2 register (Adrs = 0x0F)

	7	6	5	4	3	2	1	0
Bit name	SOCD	SOCC	SUV	SOV	UTD	UTC	OTD	OTC
R/W	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	-	-	UVLO3	UVLO5	FUSE	SDFET	SCFET	SOT
R/W	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0

The STATUS2 register indicates various conditions.

- 1) The OTC bit indicates the charging prohibition overtemperature detection status.

OTC	Charging prohibition overtemperature detection status
0	Undetected (initial value)
1	Detected

- 2) The OTD bit indicates the discharge prohibition overtemperature detection status.

OTD	Discharge prohibition overtemperature detection status
0	Undetected (initial value)
1	Detected

- 3) The UTC bit indicates the charging prohibition undertemperature detection status.

UTC	Charging prohibition undertemperature detection status
0	Undetected (initial value)
1	Detected

- 4) The UTD bit indicates the discharge prohibition undertemperature detection status.

UTD	Discharge prohibition undertemperature detection status
0	Undetected (initial value)
1	Detected

- 5) The SOV bit indicates the secondary overvoltage detection status.

SOV	Secondary overvoltage detection status
0	Undetected (initial value)
1	Detected

- 6) The SUV bit indicates the secondary undervoltage detection status.

SUV	Secondary undervoltage detection status
0	Undetected (initial value)
1	Detected

- 7) The SOCC bit indicates the secondary charging overcurrent detection status.

SOCC	Secondary charging overcurrent detection status
0	Undetected (initial value)
1	Detected

- 8) The SOCD bit indicates the secondary discharge overcurrent detection status.

SOCD	Secondary discharge overcurrent detection status
0	Undetected (initial value)
1	Detected

- 9) The SOT bit indicates the secondary overtemperature detection status.

SOT	Secondary overtemperature detection status
0	UnDetected (initial value)
1	Detected

- 10) The SCFET bit indicates the charging control FET failure detection status.

SCFET	Charging control FET failure detection status
0	Undetected (initial value)
1	Detected

- 11) The SDFET bit indicates the discharge control FET failure detection status.

SDFET	Discharge control FET failure detection status
0	Undetected (initial value)
1	Detected

- 12) The FUSE bit indicates the fuse status.

FUSE	Fuse status
0	Not cut-off (initial value)
1	Cut-off

- 13) The UVLO5 bit indicates the VREG50 output voltage drop detection status.

UVLO5	VREG50 output voltage drop detection status
0	Undetected (initial value)
1	Detected

- 14) The UVLO3 bit indicates the VREG33 output voltage drop detection status.

UVLO3	VREG33 output voltage drop detection status
0	Undetected (initial value)
1	Detected

16.LOCK register (Adrs = 0x10)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	LOCK[7:0]							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The LOCK register is used to allow writing to the registers that set various protection functions.

Before writing to the registers listed below, set the LOCK[7:0] bits to 0x69. To prohibit writing to a register, set data other than 0x69.

Address	Register name	R/W	Initial Value	Register Overview
0x11	SETOV	R/W	0x0000	Overvoltage detection operation setting register
0x12	OVDET	R/W	0x0000	Overvoltage detection threshold setting register
0x13	OVRCV	R/W	0x0000	Overvoltage release threshold setting register
0x14	SETUV	R/W	0x0000	Undervoltage detection operation setting register
0x15	UVDET	R/W	0x0000	Undervoltage detection threshold setting register
0x16	UVRCV	R/W	0x0000	Undervoltage release threshold setting register
0x17	SETOCC	R/W	0x0000	Charging overcurrent detection operation setting register
0x18	SETOCD1	R/W	0x0000	Discharge overcurrent detection operation setting register 1
0x19	SETOCD2	R/W	0x0000	Discharge overcurrent detection operation setting register 2
0x1A	SCWDT	R/W	0x0000	Short-circuit current detection operation/WDT setting register
0x1B	CHG	R/W	0x0000	Charging condition detection operation setting register
0x1C	DSG	R/W	0x0000	Discharge condition detection operation setting register
0x1D	CCMASK	R/W	0x0000	Coulomb counter mask current control register
0x1E	PWRDLY	R/W	0x0000	Power status transition delay timer setting register
0x1F	SETOTUT	R/W	0x0000	Temperature detection operation setting register
0x20	OTD1	R/W	0x0000	TEMP1 discharge prohibition overtemperature detection threshold setting register
0x21	OTD2	R/W	0x0000	TEMP2 discharge prohibition overtemperature detection threshold setting register
0x22	OTD3	R/W	0x0000	TEMP3 discharge prohibition overtemperature detection threshold setting register
0x23	OTD4	R/W	0x0000	TEMP4 discharge prohibition overtemperature detection threshold setting register
0x24	OTDR1	R/W	0x0000	TEMP1 discharge prohibition overtemperature release threshold setting register
0x25	OTDR2	R/W	0x0000	TEMP2 discharge prohibition overtemperature release threshold setting register
0x26	OTDR3	R/W	0x0000	TEMP3 discharge prohibition overtemperature release threshold setting register
0x27	OTDR4	R/W	0x0000	TEMP4 discharge prohibition overtemperature release threshold setting register
0x28	UTD1	R/W	0x0000	TEMP1 discharge prohibition undertemperature detection threshold setting register
0x29	UTD2	R/W	0x0000	TEMP2 discharge prohibition undertemperature detection threshold setting register
0x2A	UTD3	R/W	0x0000	TEMP3 discharge prohibition undertemperature detection threshold setting register
0x2B	UTD4	R/W	0x0000	TEMP4 discharge prohibition undertemperature detection threshold setting register
0x2C	UTDR1	R/W	0x0000	TEMP1 discharge prohibition undertemperature release threshold setting register
0x2D	UTDR2	R/W	0x0000	TEMP2 discharge prohibition undertemperature release threshold setting register
0x2E	UTDR3	R/W	0x0000	TEMP3 discharge prohibition undertemperature release threshold setting register
0x2F	UTDR4	R/W	0x0000	TEMP4 discharge prohibition undertemperature release threshold setting register
0x30	OTC1	R/W	0x0000	TEMP1 charging prohibition overtemperature detection threshold setting register
0x31	OTC2	R/W	0x0000	TEMP2 charging prohibition overtemperature detection threshold setting register
0x32	OTC3	R/W	0x0000	TEMP3 charging prohibition overtemperature detection threshold setting register

Address	Register name	R/W	Initial Value	Register Overview
0x33	OTC4	R/W	0x0000	TEMP4 charging prohibition overtemperature detection threshold setting register
0x34	OTCR1	R/W	0x0000	TEMP1 charging prohibition overtemperature release threshold setting register
0x35	OTCR2	R/W	0x0000	TEMP2 charging prohibition overtemperature release threshold setting register
0x36	OTCR3	R/W	0x0000	TEMP3 charging prohibition overtemperature release threshold setting register
0x37	OTCR4	R/W	0x0000	TEMP4 charging prohibition overtemperature release threshold setting register
0x38	UTC1	R/W	0x0000	TEMP1 charging prohibition undertemperature detection threshold setting register
0x39	UTC2	R/W	0x0000	TEMP2 charging prohibition undertemperature detection threshold setting register
0x3A	UTC3	R/W	0x0000	TEMP3 charging prohibition undertemperature detection threshold setting register
0x3B	UTC4	R/W	0x0000	TEMP4 charging prohibition undertemperature detection threshold setting register
0x3C	UTCR1	R/W	0x0000	TEMP1 charging prohibition undertemperature release threshold setting register
0x3D	UTCR2	R/W	0x0000	TEMP2 charging prohibition undertemperature release threshold setting register
0x3E	UTCR3	R/W	0x0000	TEMP3 charging prohibition undertemperature release threshold setting register
0x3F	UTCR4	R/W	0x0000	TEMP4 charging prohibition undertemperature release threshold setting register
0x40	CBALEN	R/W	0x0000	Cell balancing permission voltage setting register
0x41	CBALST	R/W	0x0000	Cell balancing start potential difference setting register
0x42	CBALSP	R/W	0x0000	Cell balancing end potential difference setting register
0x43	PRED SG	R/W	0x0000	Pre-discharge setting register
0x44	SETSOV	R/W	0x0000	Secondary overvoltage detection operation setting register
0x45	SOVDET	R/W	0x0000	Secondary overvoltage detection threshold setting register
0x46	SETSUV	R/W	0x0000	Secondary undervoltage detection operation setting register
0x47	SUVDET	R/W	0x0000	Secondary undervoltage detection threshold setting register
0x48	SOCC	R/W	0x0000	Secondary charging overcurrent operation setting register
0x49	S OCD	R/W	0x0000	Secondary discharge overcurrent operation setting register
0x4A	SETSOT	R/W	0x0000	Secondary overtemperature detection operation setting register
0x4B	SOT	R/W	0x0000	Secondary overtemperature detection threshold setting register
0x4C	SCFET	R/W	0x0000	C_FET failure detection operation setting register
0x4D	SDFET	R/W	0x0000	D_FET failure detection operation setting register
0x4E	FUSE	R/W	0x0000	Fuse cut-off operation setting register

17.SETOV register (Adrs = 0x11) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	ENOV	OVDLY[6:0]						
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETOV register is used to enable the overvoltage detection and set the detection delay time.

- 1) The OVDLY[6:0] bits set the number of cell voltage measurements as the overvoltage detection delay time. The detection delay time is calculated as "cell voltage measurement period x the number of cell voltage measurements".

OVDLY[6:0]	Number of cell voltage measurements
0x00	0 (initial value)
0x01	1
0x02	2
...	...
0x7D	125
0x7E	126
0x7F	127

- 2) The ENOV bit sets whether the overvoltage detection operation is activated or stopped.

ENOV	Overvoltage detection operation
0	Stop (initial value)
1	Activate

18.OVDET register (Adrs = 0x12) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OV[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OVDET register is used to set the overvoltage detection threshold.

The OV[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV.

When changing the settings, perform the operation when the ENOV bit is "0".

19.OVRCV register (Adrs = 0x13) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OVR[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OVRCV register is used to set the overvoltage release threshold.

The OVR[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV.

When changing the settings, perform the operation when the ENO bit is "0".

20.SETUV register (Adrs = 0x14) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	ENUV	UVDLY[6:0]						
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETUV register is used to enable the undervoltage detection operation and set the detection delay time.

- 1) The UVDLY[6:0] bits set the number of cell voltage measurements as the undervoltage detection delay time. The detection delay time is calculated as "cell voltage measurement period x the number of cell voltage measurements".

UVDLY[6:0]	Number of cell voltage measurements
0x00	0 (initial value)
0x01	1
0x02	2
...	...
0x7D	125
0x7E	126
0x7F	127

- 2) The ENUV bit sets whether the undervoltage detection operation is activated or stopped.

ENUV	Undervoltage detection operation
0	Stop (initial value)
1	Activate

21.UVDET register (Adrs = 0x15) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UV[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UVDET register is used to set the undervoltage detection operation or stop, the detection threshold, and the detection delay time.

The UV[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV.

When changing the settings, perform the operation when the ENUV bit is "0".

22.UVRCV register (Adrs = 0x16) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UVR[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UVRCV register is used to set the undervoltage release threshold.

The UVR[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV.

When changing the settings, perform the operation when the ENOV bit is "0".

23.SETOCC register (Adrs = 0x17) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENOCC	-	-	-	OCCDLY[3:0]				-	-	OCC[5:0]					
R/W	RW	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETOCC register is used to enable the charging overcurrent detection operation and set the charging overcurrent detection threshold and detection delay time.

- 1) The OCC[5:0] bits set the charging overcurrent detection threshold.
 [When the shunt resistor = 0.5mΩ]
 A unit value of 2.422A (128 x the current-measurement resolution of 18.9212mA) is used for the setting.
 Setting range : 0A to about 152A
 [When the shunt resistor =1.0mΩ]
 A unit value of 1.211A (128 x the current-measurement resolution of 9.4606mA) is used for the setting.
 Setting range : 0A to about 76A
 When changing the settings, perform the operation when the ENOCC bit is "0".

- 2) The OCCDLY[3:0] bits set the charging overcurrent detection delay time in 25ms steps.

OCCDLY[3:0]	Charging overcurrent detection delay time
0x0	25ms (initial value)
0x1	50ms
0x2	75ms
...	...
0xD	350ms
0xE	375ms
0xF	400ms

- 3) The ENOCC bit sets whether the charging overcurrent detection operation is activated or stopped.

ENOCC	Charging overcurrent detection operation
0	Stop (initial value)
1	Activate

24. SETOCD1、SETOCD2 register (Adrs = 0x18, 19) Note: Unlocking the LOCK register is required before writing.
SETOCD1 (Adrs=18H)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	EN OCD1	-	-	-	OCDDLY1[3:0]				-	-	OCD1[5:0]					
R/W	RW	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SETOCD2 (Adrs=19H)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	EN OCD2	-	-	-	OCDDLY2[3:0]				-	-	OCD2[5:0]					
R/W	RW	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETOCD1 and SETOCD2 registers are used to enable two types of discharge overcurrent detection operation and set the discharge overcurrent detection threshold and the detection delay time.

- The OCD1[5:0] and OCD2[5:0] bits set the discharge overcurrent detection threshold.
[When the shunt resistor = 0.5mΩ]
A unit value of 9.688A (512 x the current-measurement resolution of 18.9212mA) is used for the setting.
Setting range : 0A to about 610A
[When the shunt resistor = 1.0mΩ]
A unit value of 4.844A (512 x the current-measurement resolution of 9.4606mA) is used for the setting.
Setting range : 0A to about 305A
When changing the settings, perform the operation when the ENOCD1 and ENOCD2 bits are "0".

- The OCDDLY1[3:0] and OCDDLY2[3:0] bits set the discharge overcurrent detection delay time in 25ms steps.

OCDDLY1[3:0]	Discharge overcurrent 1 detection delay time	OCDDLY2[3:0]	Discharge overcurrent 2 detection delay time
0x0	25ms (initial value)	0x0	25ms (initial value)
0x1	50ms	0x1	50ms
0x2	75ms	0x2	75ms
...	...	...	...
0xD	350ms	0xD	350ms
0xE	375ms	0xE	375ms
0xF	400ms	0xF	400ms

- The ENOCD1 and ENOCD2 bits set whether the discharge overcurrent detection operation is activated or stopped.

ENOCD1	Discharge overcurrent 1 detection operation	ENOCD2	Discharge overcurrent 2 detection operation
0	Stop (initial value)	0	Stop (initial value)
1	Activate	1	Activate

25. SCWDT register (Adrs = 0x1A) Note: Unlocking the LOCK register is required before writing.

	7	6	5	4	3	2	1	0
Bit name	ENSC	-	TSC[1:0]		-	SC[2:0]		
R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	-	-	-	-	ENWDT	-	WDT[1:0]	
R/W	R	R	R	R	R/W	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The SCWDT register is used to enable the short current detection circuit operation and set the threshold voltage, and also to enable the watchdog timer operation and set the overflow time.

- 1) The SC[2:0] bits select the short-circuit current detection threshold voltage according to the shunt resistance. When changing the settings, perform the operation when the ENSC bit is "0".

SC[2:0]	Short-circuit current detection voltage (Voltage between ISP-ISM pins)	When shunt resistance is 0.5mΩ Short-circuit detection current value
0x0	25mV(initial value)	50A
0x1	50mV	100A
0x2	75mV	150A
0x3	100mV	200A
0x4	125mV	250A
0x5	150mV	300A
0x6	175mV	350A
0x7	200mV	400A

- 2) The TSC[1:0] bits select the short-circuit current detection delay time.

TSC[1:0]	Short-circuit current detection delay time
0x0	50μs (initial value)
0x1	100μs
0x2	150μs
0x3	200μs

- 3) The ENSC bit sets whether the short-circuit detection operation is activated or stopped.

ENSC	Short-circuit detection operation
0	Stop (initial value)
1	Activate

- 4) The WDT[1:0] bits select the watchdog timer's overflow time. When changing the settings, perform the operation when the ENWDT bit is "0".

WDT[1:0]	Overflow time
0x0	2 s (initial value)
0x1	4 s
0x2	8 s
0x3	16 s

- 5) The ENWDT bit sets whether the watchdog timer operation is activated or stopped.

ENWDT	Watchdog timer operation
0	Stop (initial value)
1	Activate

In standalone mode, the watchdog timer may generate false detections, so set ENWDT bit to "0" to stop.

26. CHG register (Adrs = 0x1B) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENCHG	-	-	-	-	CHGDLY[2:0]			CHG[7:0]							
R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CHG register is used to set the current threshold for charging condition detection and the charging condition release delay time.

- 1) The CHG[7:0] bits set the current threshold for charging condition detection.
 [When the shunt resistor = 0.5mΩ]
 A unit value of 18.9212mA is used for the setting.
 Setting range : 0A to about 4.8A
 [When the shunt resistor = 1.0mΩ]
 A unit value of 9.4606mA is used for the setting.
 Setting range : 0A to about 2.4A
 When changing the settings, perform the operation when the ENCHG bit is "0".
- 2) The CHGDLY[2:0] bits set the charging condition release delay time in the 25ms steps.
 During the charge-state detection delay time, if the charge-state detection current threshold is exceeded, the LSI immediately enters the charging state.

CHGDLY[2:0]	Charging condition release delay time
0x0	25ms (initial value)
0x1	50ms
0x2	75ms
0x3	100ms
0x4	125ms
0x5	150ms
0x6	175ms
0x7	200ms

- 3) The ENCHG bit sets whether the charging condition detection operation is activated or stopped.

ENCHG	Charging condition detection operation
0	Stop (initial value)
1	Activate

If the charging condition is detected when an undervoltage condition or a discharge prohibition over/undertemperature condition is detected, the D_FET pin output automatically changes to the "H" level, and the discharge is permitted. At this time, the pre-discharge function does not work.
 Also, in the power-save state, if the ENPSV bit in the POWER register is "0", the LSI automatically returns to the normal state if the charging condition is detected.

27.DSG register (Adrs = 0x1C) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENDSG	-	-	-	-	DSGDLY[2:0]			DSG[7:0]							
R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DSG register is used to set the current threshold for discharge condition detection and the discharge condition release delay time.

- The DSG[7:0] bits set the current threshold for discharge condition detection.
 [When the shunt resistor = 0.5mΩ]
 A unit value of 18.9212mA is used for the setting.
 Setting range : 0A to about 4.8A
 [When the shunt resistor = 1.0mΩ]
 A unit value of 9.4606mA is used for the setting.
 Setting range : 0A to about 2.4A
 When changing the settings, perform the operation when the ENDSG bit is "0".
- The DSGDLY[2:0] bits set the discharge condition release delay time in the 25ms steps.
 During the discharge-state detection delay time, if the discharge-state detection current threshold is exceeded, the LSI immediately enters the discharging state.

DSGDLY[2:0]	Discharge condition release delay time
0x0	25ms (initial value)
0x1	50ms
0x2	75ms
0x3	100ms
0x4	125ms
0x5	150ms
0x6	175ms
0x7	200ms

- The ENDSG bit sets whether the discharge condition detection operation is activated or stopped.

ENDSG	Discharge condition detection operation
0	Stop (initial value)
1	Activate

If the discharge condition is detected while detecting an overvoltage condition or a charging prohibition over/undertemperature condition, the C_FET pin output automatically changes to the "H" level, and the charging is permitted.

Also, in the power-save state, if the ENPSV bit in the POWER register is "0", the LSI automatically returns to the normal state if the discharge condition is detected.

28.CCMASK register (Adrs = 0x1D) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	DSGMASK[6:0]							-	CHGMASK[6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CCMASK register masks the minute current region to prevent the no-load current measurement offset error from being added to the coulomb counter.

- The CHGMASK[6:0] bits set the mask current for the charging current.
- The DSGMASK[6:0] bits set the mask current for the discharge current.
 When the shunt resistor = 0.5mΩ
 [When the current gain is x1]
 A unit value of 18.9212mA is used for the setting.
 Setting range : 0A to about 2.4A
 [When the current gain is x4]
 A unit value of 4.7304mA is used for the setting.
 Setting range : 0A to about 0.6A

29. PWRDLY register (Adrs = 0x1E) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	PDDL[3:0]				SLPDLY[3:0]				PSVDLY[3:0]			
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PWRDLY register is used to set the delay time for transition to the power-save state, sleep state, and power-down state.

- 1) The PSVDLY[3:0] bits set the power-save transition delay time in the 1s step.

PSVDLY[3:0]	Power-save state transition delay time	PSVDLY[3:0]	Power-save state transition delay time
0x0	0s (initial value)	0x8	8s
0x1	1s	0x9	9s
0x2	2s	0xA	10s
0x3	3s	0xB	11s
0x4	4s	0xC	12s
0x5	5s	0xD	13s
0x6	6s	0xE	14s
0x7	7s	0xF	15s

- 2) The SLPDLY[3:0] and PDDL[3:0] bits set the delay time for transition to the sleep state and power down state in 16s step.

SLPDLY[3:0] PDDL[3:0]	Sleep/Power-down state transition delay time	SLPDLY[3:0] PDDL[3:0]	Sleep/Power-down state transition delay time
0x0	16s (initial value)	0x8	144s
0x1	32s	0x9	160s
0x2	48s	0xA	176s
0x3	64s	0xB	192s
0x4	80s	0xC	208s
0x5	96s	0xD	224s
0x6	112s	0xE	240s
0x7	128s	0xF	256s

When the ENPSV bit, or ENSLP bit, ENPD bit in the POWER register is set to "1", the transition delay time settings are invalid.

30.SETOTUT register (Adrs = 0x1F) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	RPUP[3:0]				ENOTUT	OTUTDLY[6:0]						
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETOTUT register is used to enable the temperature detection operation, set the detection delay time and the TEMP pin pull-up resistor.

- 1) The OTUTDLY[6:0] bits set the number of temperature measurements as the detection delay time.

OTUTDLY[6:0]	Number of temperature measurements for detection delay
0x00	0 (initial value)
0x01	1
0x02	2
0x03	3
...	...
0x7D	125
0x7E	126
0x7F	127

- 2) The ENOTUT bit sets whether the temperature detection operation is activated or stopped.

ENOTUT	Temperature detection operation
0	Stop (initial value)
1	Activate

- 3) The RPUP[3:0] bits configure whether or not a pull-up resistor is connected to the TEMPn pin.

RPUP[3:0]	TEMP pin pull-up resistor
0x0	Not connected all TEMP pins (initial value)
0x1	TEMP1 pin measurement
0x2	TEMP2 pin measurement
0x4	TEMP3 pin measurement
0x8	TEMP4 pin measurement

31.OTD1 register (Adrs = 0x20) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTD1[11:0]											
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTD1 register is used to set the discharge prohibition overtemperature detection threshold for the TEMP1 pin. The OTD1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

32.OTD2 register (Adrs = 0x21) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTD2[11:0]											
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTD2 register is used to set the discharge prohibition overtemperature detection threshold for the TEMP2 pin. The OTD2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

33.OTD3 register (Adrs = 0x22) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTD3[11:0]											
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTD3 register is used to set the discharge prohibition overtemperature detection threshold for the TEMP3 pin. The OTD3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

34.OTD4 register (Adrs = 0x23) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTD4[11:0]											
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTD4 register is used to set the discharge prohibition overtemperature detection threshold for the TEMP4 pin. The OTD4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

35.OTDR1 register (Adrs = 0x24) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTDR1[11:0]											
R/W	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTDR1 register is used to set the discharge prohibition overtemperature release threshold for the TEMP1 pin. The OTDR1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

36.OTDR2 register (Adrs = 0x25) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTDR2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTDR2 register is used to set the discharge prohibition overtemperature release threshold for the TEMP2 pin. The OTDR2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

37.OTDR3 register (Adrs = 0x26) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTDR3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTDR3 register is used to set the discharge prohibition overtemperature release threshold for the TEMP3 pin. The OTDR3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

38.OTDR4 register (Adrs = 0x27) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTDR4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTDR4 register is used to set the discharge prohibition overtemperature release threshold for the TEMP4 pin. The OTDR4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

39.UTD1 register (Adrs = 0x28) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTD1[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTD1 register is used to set the discharge prohibition undertemperature detection threshold for the TEMP1 pin. The UTD1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

40.UTD2 register (Adrs = 0x29) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTD2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTD2 register is used to set the discharge prohibition undertemperature detection threshold for the TEMP2 pin. The UTD2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

41.UTD3 register (Adrs = 0x2A) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTD3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTD3 register is used to set the discharge prohibition undertemperature detection threshold for the TEMP3 pin. The UTD3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

42.UTD4 register (Adrs = 0x2B) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTD4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTD4 register is used to set the discharge prohibition undertemperature detection threshold for the TEMP4 pin. The UTD4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

43.UTDR1 register (Adrs = 0x2C) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTDR1[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTDR1 register is used to set the discharge prohibition undertemperature release threshold for the TEMP1 pin. The UTDR1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

44.UTDR2 register (Adrs = 0x2D) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTDR2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTDR2 register is used to set the discharge prohibition undertemperature release threshold for the TEMP2 pin. The UTDR2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

45.UTDR3 register (Adrs = 0x2E) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTDR3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTDR3 register is used to set the discharge prohibition undertemperature release threshold for the TEMP3 pin. The UTDR3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

46.UTDR4 register (Adrs = 0x2F) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTDR4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTDR4 register is used to set the discharge prohibition undertemperature release threshold for the TEMP4 pin. The UTDR4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

47.OTC1 register (Adrs = 0x30) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTC1[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTC1 register is used to set the charging prohibition overtemperature detection threshold for the TEMP1 pin. The OTC1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

48.OTC2 register (Adrs = 0x31) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTC2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTC2 register is used to set the charging prohibition overtemperature detection threshold for the TEMP2 pin. The OTC2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

49.OTC3 register (Adrs = 0x32) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTC3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTC3 register is used to set the charging prohibition overtemperature detection threshold for the TEMP3 pin. The OTC3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

50.OTC4 register (Adrs = 0x33) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTC4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTC4 register is used to set the charging prohibition overtemperature detection threshold for the TEMP4 pin. The OTC4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

51.OTCR1 register (Adrs = 0x34) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTCR1[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTCR1 register is used to set the charging prohibition overtemperature release threshold for the TEMP1 pin. The OTCR1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

52.OTCR2 register (Adrs = 0x35) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTCR2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTCR2 register is used to set the charging prohibition overtemperature release threshold for the TEMP2 pin. The OTCR2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

53.OTCR3 register (Adrs = 0x36) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTCR3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTCR3 register is used to set the charging prohibition overtemperature release threshold for the TEMP3 pin. The OTCR3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

54.OTCR4 register (Adrs = 0x37) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	OTCR4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTCR4 register is used to set the charging prohibition overtemperature release threshold for the TEMP4 pin. The OTCR4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

55.UTC1 register (Adrs = 0x38) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTC1[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTC1 register is used to set the charging prohibition undertemperature detection threshold for the TEMP1 pin. The UTC1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

56. UTC2 register (Adrs = 0x39) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTC2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTC2 register is used to set the charging prohibition undertemperature detection threshold for the TEMP2 pin. The UTC2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

57. UTC3 register (Adrs = 0x3A) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTC3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTC3 register is used to set the charging prohibition undertemperature detection threshold for the TEMP3 pin. The UTC3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

58. UTC4 register (Adrs = 0x3B) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTC4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTC4 register is used to set the charging prohibition undertemperature detection threshold for the TEMP4 pin. The UTC4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

59. UTCR1 register (Adrs = 0x3C) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTCR1[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTCR1 register is used to set the charging prohibition undertemperature release threshold for the TEMP1 pin. The UTCR1[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

60. UTCR2 register (Adrs = 0x3D) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTCR2[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTCR2 register is used to set the charging prohibition undertemperature release threshold for the TEMP2 pin. The UTCR2[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

61. UTCR3 register (Adrs = 0x3E) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTCR3[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTCR3 register is used to set the charging prohibition undertemperature release threshold for the TEMP3 pin. The UTCR3[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

62. UTCR4 register (Adrs = 0x3F) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	UTCR4[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The UTCR4 register is used to set the charging prohibition undertemperature release threshold for the TEMP4 pin. The UTCR4[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin. When changing the settings, perform the operation when the ENOTUT bit is "0".

63. CBALEN register (Adrs = 0x40) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	CBALEN[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CBALEN register is used to set the cell balancing permission voltage. The CBALEN[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV. Cell balancing is not performed for cells below the cell balancing permission voltage, even if the difference with the minimum cell voltage is large.

64. CBALST register (Adrs = 0x41) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	CBALST[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CBALST register is used to set the cell balancing start potential difference. The CBALST[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV. Cell balancing is performed on cells that are equal to or higher than the cell balancing permission voltage and whose potential difference from the minimum cell voltage is equal to or higher than the cell balancing start potential difference. Note that even if the minimum cell voltage is equal to or less than the cell balancing permission voltage, the cell balancing operation is determined based on the potential difference from the minimum cell voltage.

65. CBALSP register (Adrs = 0x42) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	CBALSP[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CBALSP register is used to set the cell balancing end potential difference. The CBALSP[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV. The cell balancing operation ends when the potential difference between the cell voltage being balanced and the minimum cell voltage is equal to or lower than the cell balancing end potential difference. Note that the cell balancing operation also ends if the cell voltage falls below the cell balancing permission voltage.

66.PREDSG register (Adrs = 0x43) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENTPRD	TPRDSG[6:0]							ENVPRD	VPRDSG[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PREDSG register is used to set the pre-discharge function.

The pre-discharge function prevents inrush current when the discharge control FET is changed from OFF to ON by passing a small discharge current until the battery pack output rises above a specified voltage or until a specified time has elapsed. When the ENPRDF bit in the FETCBAL register is "1", this register setting is invalid.

- 1) The VPRDSG[6:0] bits set the pre-discharge completion voltage in the 64LSB step (1LSB = 2500/4095mV). If the difference between the VDD terminal voltage measurement value and the RSNS terminal voltage measurement value falls below the pre-discharge completion voltage, the pre-discharge ends.

VPRDSG[6:0]	Pre-discharge completion voltage
0x00	320LSB,195mV (initial value)
0x01~0x04	320LSB,195mV
0x05	384LSB,234mV
0x06	448LSB,274mV
...	...
0x7D	8064LSB,4.92V
0x7E	8128LSB,4.96V
0x7F	8192LSB,5.00V

- 2) The ENVPRD bit sets whether the pre-discharge completion voltage setting is enabled or disabled. When the ENVPRD bit is set to "1", if the difference between the VDD terminal voltage measurement result and the RSNS terminal voltage measurement result falls below the pre-discharge completion voltage, the pre-discharge ends, the PRD_FET terminal output changes from 13V to 0V, and a pre-discharge interrupt (QPRDSG) is generated.

ENVPRD	Pre-discharge completion voltage setting
0	Disabled (initial value)
1	Enable

- 3) The TPRDSG[6:0] bits set the pre-discharge time in the range of 25 to 3200 ms in the 25ms steps. When the pre-discharge time has elapsed, the pre-discharge ends, the PRD_FET terminal output changes from Vs+11V(Typ.) to 0V, and a pre-discharge interrupt (QPRDSG) is generated.

TPRDSG[6:0]	Pre-discharge time
0x00	25ms (initial value)
0x01	50ms
0x02	75ms
0x03	100ms
...	...
0x7D	3150ms
0x7E	3175ms
0x7F	3200ms

- 4) The ENTPRD bit sets whether the pre-discharge time setting is enabled or disabled.

ENTPRD	Pre-discharge time setting
0	Disabled (initial value)
1	Enable

67.SETSOV register (Adrs = 0x44) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	ENSOV	SOVDLY[6:0]						
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETSOV register is used to set the secondary overvoltage detection operation.

- 1) The SOVDLY[6:0] bits set the number of cell voltage measurements as the secondary overvoltage detection delay time. The detection delay time is calculated as "cell voltage measurement period x the number of cell voltage measurements".

SOVDLY[6:0]	Number of cell voltage measurements
0x00	0 (initial value)
0x01	4
0x02	8
0x03	12
...	...
0x7D	500
0x7E	504
0x7F	508

- 2) The ENSOV bit sets whether the secondary overvoltage detection operation is activated or stopped.

ENSOV	Secondary overvoltage detection operation
0	Stop (initial value)
1	Activate

68.SOVDET register (Adrs = 0x45) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	SOV[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SOVDET register is used to set the secondary overvoltage detection threshold.

The SOV[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV.

When changing the settings, perform the operation when the ENSOV bit is "0".

The SOV[11:0] bits must be set to a value higher than the overvoltage detection threshold set by the OV[11:0] bits in the OVDET register.

69.SETSUV register (Adrs = 0x46) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	ENSUV	SUVDLY[6:0]						
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETSUV register is used to set the secondary undervoltage detection operation and detection delay time.

- 1) The SUVDLY[6:0] bits set the number of cell voltage measurements as the secondary undervoltage detection delay time. The detection delay time is calculated as "cell voltage measurement period x the number of cell voltage measurements".

SUVDLY[6:0]	Number of cell voltage measurements
0x00	0 (initial value)
0x01	4
0x02	8
...	...
0x7D	500
0x7E	504
0x7F	508

- 2) The ENSUV bit sets whether the secondary undervoltage detection operation is activated or stopped.

ENSUV	Secondary undervoltage detection operation
0	Stop(initial value)
1	Activate

70.SUVDET register (Adrs = 0x47) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	SUV[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SUVDET register is used to set the secondary undervoltage detection threshold.

The SUV[11:0] bits are defined with a cell voltage measurement resolution of 5000/4095mV.

When changing the settings, perform the operation when the ENSUV bit is "0".

The SUV[11:0] bits must be set to a value lower than the undervoltage detection threshold set by the UV[11:0] bits in the UVDET register.

71. SOCC register (Adrs = 0x48) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENSOCC	-	-	-	SOCCDLY[3:0]				-	-	SOCC[5:0]					
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SOCC register is used to set the secondary charging overcurrent detection operation, and the secondary detection threshold, detection delay time.

- 1) The SOCC[5:0] bits set the secondary charging overcurrent detection threshold.
 [When the shunt resistor = 0.5mΩ]
 A unit value of 2.422A (128 x the current-measurement resolution of 18.9212mA) is used for the setting.
 Setting range : 0A to about 152A
 [When the shunt resistor = 1.0mΩ]
 A unit value of 1.211A (128 x the current-measurement resolution of 9.4606mA) is used for the setting.
 Setting range : 0A to about 76A
 When changing the settings, perform the operation when the ENSOCC bit is "0".

- 2) The SOCCDLY[3:0] bits set the secondary charging overcurrent detection delay time in the 1s step.

SOCCDLY[3:0]	Secondary charging overcurrent detection delay time
0x0	0s (initial value)
0x1	0s to 1s
0x2	1s to 2s
...	...
0xD	12s to 13s
0xE	13s to 14s
0xF	14s to 15s

- 3) The ENSOCC bit sets whether the secondary charging overcurrent detection operation is activated or stopped.

ENSOCC	Secondary charging overcurrent detection operation
0	Stop (initial value)
1	Activate

72.SOCD register (Adrs = 0x49) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENSOCD	-	-	-	SOCDDL[3:0]				-	-	SOCD[5:0]					
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SOCD register is used to set the secondary discharge overcurrent detection enable, and detection threshold, detection delay time.

- The SOCD[5:0] bits set the secondary discharge overcurrent detection threshold.
 [When the shunt resistor = 0.5mΩ]
 A unit value of 9.688A (512 x the current-measurement resolution of 18.9212mA) is used for the setting.
 Setting range : 0A to about 610A
 [When the shunt resistor = 1.0mΩ]
 A unit value of 4.844A (512 x the current-measurement resolution of 9.4606mA) is used for the setting.
 Setting range : 0A to about 305A
 When changing the settings, perform the operation when the ENSOCD bit is "0".

- The SOCDDL[3:0] bits set the secondary discharge overcurrent detection delay time in the 1s step.

SOCDDL[3:0]	Secondary discharge overcurrent detection delay time
0x0	0s (initial value)
0x1	0s to 1s
0x2	1s to 2s
...	...
0xD	12s to 13s
0xE	13s to 14s
0xF	14s to 15s

- The ENSOCD bit sets whether the secondary discharge overcurrent detection operation is activated or stopped.

ENSOCD	Secondary discharge overcurrent detection operation
0	Stop (initial value)
1	Activate

73.SETSOT register (Adrs = 0x4A) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	ENSOT[3:0]				-	SOTDLY[6:0]						
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SETSOT register is used to set the secondary overtemperature detection using the TEMP pin and its delay time.

- The SOTDLY[6:0] bits set the detection delay time by the number of temperature measurements.

SOTDLY[6:0]	Number of temperature measurements for detection delay
0x00	0 (initial value)
0x01	4
0x02	8
...	...
0x7D	500
0x7E	504
0x7F	508

- The ENSOT[3:0] bits set the TEMP pin to which the secondary overtemperature detection operation is applied.

ENSOT[0]	TEMP1 pin
0	Not applied (initial value)
1	Applied

ENSOT[1]	TEMP2 pin
0	Not applied (initial value)
1	Applied

ENSOT[2]	TEMP3 pin
0	Not applied (initial value)
1	Applied

ENSOT[3]	TEMP4 pin
0	Not applied (initial value)
1	Applied

74.SOT register (Adrs = 0x4B) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	SOT[11:0]											
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SOT register is used to set the secondary overtemperature detection threshold.

The SOT[11:0] bits are defined with a voltage measurement resolution of 2500/4095mV at the TEMP pin.

When changing the settings, perform the operation when the ENSOT bit is "0".

75.SCFET register (Adrs = 0x4C) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENSCF	-	-	-	SCFDLY[3:0]					-	-	-	-	SCFET[3:0]		
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SCFET register is used to set the charging control FET failure detection operation, detection threshold, and detection delay time.

When C_FET is in the OFF state, an abnormality is detected if a current equal to or higher than the threshold flows for a longer time than the detection delay time.

- 1) The SCFET[3:0] bits set the charging current detection threshold.
 [When the shunt resistor = 0.5mΩ]
 A unit value of 0.302A (16 x the current-measurement resolution of 18.9212mA) is used for the setting.
 Setting range : 0A to about 4.5A
 [When the shunt resistor = 1.0mΩ]
 A unit value of 0.151A (16 x the current-measurement resolution of 9.4606mA) is used for the setting.
 Setting range : 0A to about 2.2A
 When changing the settings, perform the operation when the ENSCF bit is "0".

- 2) The SCFDLY[3:0] bits set the detection delay time in the 1s step.

SCFDLY[3:0]	Detection delay time
0x0	0s (initial value)
0x1	0s to 1s
0x2	1s to 2s
...	...
0xD	12s to 13s
0xE	13s to 14s
0xF	14s to 15s

- 3) The ENSCF bit sets whether the charging control FET failure detection operation is activated or stopped.

ENSCF	Charging control FET failure detection operation
0	Stop (initial value)
1	Activate

76.SDFET register (Adrs = 0x4D) Note: Unlocking the LOCK register is required before writing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ENSDF	-	-	-	SDFDLY[3:0]				-	-	-	-	SDFET[3:0]			
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SDFET register is used to set the discharge control FET failure detection operation, failure detection threshold, and detection delay time.

When D_FET is in the OFF state, an abnormality is detected if a current equal to or higher than the threshold flows for a longer time than the detection delay time.

- 1) The SDFET[3:0] bits set the discharge current detection threshold.

[When the shunt resistor = 0.5mΩ]

A unit value of 1.21A (64 x the current-measurement resolution of 18.9212mA) is used for the setting.

Setting range : 0A to about 18.1A

[When the shunt resistor = 1.0mΩ]

A unit value of 0.605A (64 x the current-measurement resolution of 9.4606mA) is used for the setting.

Setting range : 0A to about 9.0A

When changing the settings, perform the operation when the ENSDF bit is "0".

- 2) The SDFDLY[3:0] bits set the detection delay time in the 1s step.

SDFDLY[3:0]	Detection delay time
0x0	0s (initial value)
0x1	0s to 1s
0x2	1s to 2s
...	...
0xD	12s to 13s
0xE	13s to 14s
0xF	14s to 15s

- 3) The ENSDF bit sets whether the discharge control FET failure detection operation is activated or stopped.

ENSDF	Discharge control FET failure detection operation
0	Stop (initial value)
1	Activate

77.FUSE register (Adrs = 0x4E) Note: Unlocking the LOCK register is required before writing.

	7	6	5	4	3	2	1	0
Bit name	ENFUSE	FSDFET	FSCFET	FSOT	FSOCD	FSOCC	FSUV	FSOV
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
Bit name	TBLOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

The FUSE register is used to set the external fuse cut-off operation, secondary abnormality detection selection, and fuse cut time.

- 1) The ENFUSE bit sets whether the external fuse cut-off operation is activated or stopped.

ENFUSE	External fuse cut-off operation
0	Stop (initial value)
1	Activate

By setting the following each bits to "1", an "H" level is output to the FUSE pin when a secondary abnormality is detected, and the external fuse is cut off. If set to "0", the external fuse will not be cut off even if the corresponding secondary abnormality is detected.

Bits	Secondary abnormality detection that cut-off fuse
FSOV	Secondary overvoltage detection
FSUV	Secondary undervoltage detection
FSOCC	Secondary charging overcurrent detection
FSOCD	Secondary discharge overcurrent detection
FSOT	Secondary overtemperature detection
FSCFET	Charging control FET failure detection
FSDFET	Discharge control FET failure detection

- 2) The TBLOW[7:0] bits set the fuse cut-off time.

TBLOW[7:0]	Fuse cut-off time
0x00	Infinity (initial value)
0x01	0s to 1s
0x02	1s to 2s
0x03	2s to 3s
...	...
0xFE	253s to 254s
0xFF	254s to 255s

After the fuse cut-off time has elapsed, a fuse cut completion interrupt (QFUSE) of the INT_REQ3 register will be generated, and the LSI enters into the sleep state from the next voltage measurement cycle. However, the LSI will not enter the sleep state until the PSNS pin voltage becomes equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}) and the /PUPIN pin becomes an "H" level.

When the TBLOW[7:0] bits are 0x00, the LSI continues to output an "H" level to the FUSE pin, an interrupt is generated immediately, and the LSI enters the sleep state from the next voltage measurement cycle. Even after entering the sleep state, the LSI continuously outputs an "H" level to the FUSE pin.

Also, the FUSE bit in the STATUS2 register is set to "1" and retains set until the ENFUSE bit is set to "0".

78.VCELLn register (Adrs = 0x4F~0x58)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	VCELLn[11:0]											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*

The VCELLn registers (n = 1 to 10) store the measurement results of each cell voltage.
The cell voltage measurement resolution is 5000/4095mV.

79. G1_ICELLn register (Adrs = 0x5A~0x63)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G1_ICELLn[15:0]															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The G1_ICELLn registers (n = 1 to 10) store the current measurement results when measuring each cell voltage at current gain is 1x.

The G1_ICELLn [15] bit is the sign bit. It is "0" for charging current and "1" for discharging current. The value is represented in 2's complement binary format.

[When the shunt resistor = 0.5mΩ]

The current measurement resolution is 18.9212mA.

[When the shunt resistor = 1.0mΩ]

The current measurement resolution is 9.4606mA.

If the current gain is not set to 1x in the IGAIN bit of the SEL register, this register stores 0x7FFF.

80. G4_ICELLn register (Adrs = 0x64~0x6D)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G4_ICELLn[15:0]															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The G4_ICELLn registers (n = 1 to 10) store the current measurement results when measuring each cell voltage at current gain is 4x.

The G4_ICELLn [15] bit is the sign bit. It is "0" for charging current and "1" for discharging current. The value is represented in 2's complement binary format.

[When the shunt resistor = 0.5mΩ]

The current measurement resolution is 4.7304mA.

[When the shunt resistor = 1.0mΩ]

The current measurement resolution is 2.3652mA.

If the current gain is not set to 4x in the IGAIN bit of the SEL register, this register stores 0x7FFF.

81. G1_CURR register (Adrs = 0x6E)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name		G1_CURR[15:0]															
R/W		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The G1_CURR register store the current measurement result at current gain is 1x. It is updated every 2ms.

The G1_CURR[15] bit is the sign bit. It is "0" for charging current and "1" for discharging current. The value is represented in 2's complement binary format.

[When the shunt resistor = 0.5mΩ]

The current measurement resolution is 18.9212mA.

[When the shunt resistor = 1.0mΩ]

The current measurement resolution is 9.4606mA.

If the current gain is not set to 1x in the IGAIN bit of the SEL register, this register stores 0x7FFF.

82.G4_CURR register (Adrs = 0x6F)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G4_CURR[15:0]															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The G4_CURR register store the current measurement result at current gain is 4x. It is updated every 2ms. The G4_CURR[15] bit is the sign bit. It is "0" for charging current and "1" for discharging current. The value is represented in 2's complement binary format.

[When the shunt resistor = 0.5mΩ]

The current measurement resolution is 4.7304mA.

[When the shunt resistor = 1.0mΩ]

The current measurement resolution is 2.3652mA.

If the current gain is not set to 4x in the IGAIN bit of the SEL register, this register stores 0x7FFF.

83.CCL register (Adrs = 0x70)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	CCL[15:0]															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

The CCL register stores the lower 16 bits of the coulomb counter. It is updated every cycle set by the CC[1:0] bits in the PERIOD register.

The current integration unit is expressed by the following formula.

"Current measurement resolution" * 0.002(CURR measurement period) / 3600[Ah]

When the shunt resistance is 0.5mΩ, the current measurement integration unit is 10.5118nAh.

84.CCH register (Adrs = 0x71)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	CCH[15:0]															
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

The CCH register stores the upper 16 bits of the coulomb counter. It is updated every cycle set by the CC[1:0] bits in the PERIOD register.

The CCH[15] bit is the sign bit. It is "0" for charging current and "1" for discharging current. The value is represented in 2's complement binary format.

The CCH register value is updated when the CCL register, which holds the lower data, is read, so read the two registers consecutively in the order of the CCL and CCH.

85.INTEGCL vregister (Adrs = 0x72)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	INTEGCL[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The INTEGCL register stores the lower 16 bits of the coulomb counter. The G1_CURR register value or G4_CURR register value is integrated every 2 ms against the value set in the INTEGCL register.

The current integration unit is expressed by the following formula.

"Current measurement resolution" * 0.002(CURR measurement period) / 3600 * 4[Ah]

When the shunt resistance is 0.5mΩ, the current measurement integration unit is 42.048nAh.

86. INTEGCH register (Adrs = 0x73)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	INTEGCH[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The INTEGCH register stores the upper 16 bits of the coulomb counter. It is updated every 2ms.
 The INTEGCH[15] bit is not a sign bit. The remaining battery capacity is displayed in straight binary format.
 [Notes on Register Read and Write Operations]

The INTEGCH register value is updated when the INTEGCL register, which holds the lower data, is read, so read and write the two registers consecutively in the order of the INTEGCL and INTEGCH.

87. TEMPn register (Adrs = 0x74~0x77)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	TEMPn[11:0]											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*

The TEMPn register (n = 1 to 4) stores the voltage measurement result of the TEMPn pin (n = 1 to 4).
 The voltage measurement resolution of the TEMPn pin is 2500/4095mV.

88. PSNS register (Adrs = 0x78)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	PSNS[11:0]											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*

The PSNS register stores the measurement result of the PSNS pin voltage scaled down to 1/32.
 The voltage measurement resolution of the PSNS pin is 32*2500/4095mV.

89. RSNS register (Adrs = 0x79)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	RSNS[11:0]											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*

The RSNS register stores the measurement result of the RSNS pin voltage scaled down to 1/32.
 The voltage measurement resolution of the RSNS pin is 32*2500/4095mV.

90. VDD register (Adrs = 0x7A)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	VDD[11:0]											
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*

The VDD register stores the measurement result of the VDD pin voltage scaled down to 1/32.
 The voltage measurement resolution of the VDD pin is 32*2500/4095mV.

91.VGAIN register (Adrs = 0x7B)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	-	VGAIN[6:0]						
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The VGAIN register is used to set the gain correction value of the cell voltage measurement result.

The relationship between the VGAIN[6:0] bits and the gain correction value is shown below.

Gain correction value = $1 + 2^{(-11)} * \text{VGAIN}$ (2's complement binary)

The initial value stores a correction value obtained during the LSI manufacturing process.

VGAIN[6:0]	Gain correction value
0x00	1.0000
0x01	1.0005
0x02	1.0010
0x03	1.0015
...	...
0x3C	1.0293
0x3D	1.0298
0x3E	1.0303
0x3F	1.0308

VGAIN[6:0]	Gain correction value
0x40	0.9688
0x41	0.9692
0x42	0.9697
0x43	0.9702
...	...
0x7C	0.9981
0x7D	0.9985
0x7E	0.9990
0x7F	0.9995

92.VOFST register (Adrs = 0x7C)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	VOFST[7:0]							
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The VOFST register is used to set the offset correction value of the cell voltage measurement result.

The relationship between the VOFST[7:0] bits and the offset correction value when the cell voltage measurement resolution LSB = 5000/409mV is shown in the table below.

The initial value stores a correction value obtained during the LSI manufacturing process.

VOFST[7:0]	Offset correction value
0x00	0
0x01	+1LSB
0x02	+2LSB
0x03	+3LSB
...	...
0x7D	+125LSB
0x7E	+126LSB
0x7F	+127LSB

VOFST[7:0]	Offset correction value
0x80	-128LSB
0x81	-127LSB
0x82	-126LSB
0x83	-125LSB
...	...
0xFD	-3LSB
0xFE	-2LSB
0xFF	-1LSB

The VGAIN and VOFST registers store correction values obtained during the LSI manufacturing process. When performing recalibration, it is recommended to first rewrite the VGAIN and VOFST registers to 0x00, then measure the cell voltage at an arbitrary cell voltage, calculate the correction values, store them in an MCU or equivalent the LSI, and finally set those values to the VGAIN and VOFST registers.

93.CC_CAL register (Adrs = 0x7D)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	CAL_FS[8:0]										-	-	ZS_CAL	-	-	FS_CAL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The CC_CAL register is used to set the calibration of the coulomb counter.

- 1) The FS_CAL bit initiates full-scale calibration.
Input the potential difference across the shunt resistor when the maximum discharge current flows through it between the ISP-ISM pins from outside. After the calibration is completed, the QCCCAL bit in the INT_REQ2 register is set.

FS_CAL	Full-scale calibration
0	Completed (initial value)
1	Execute

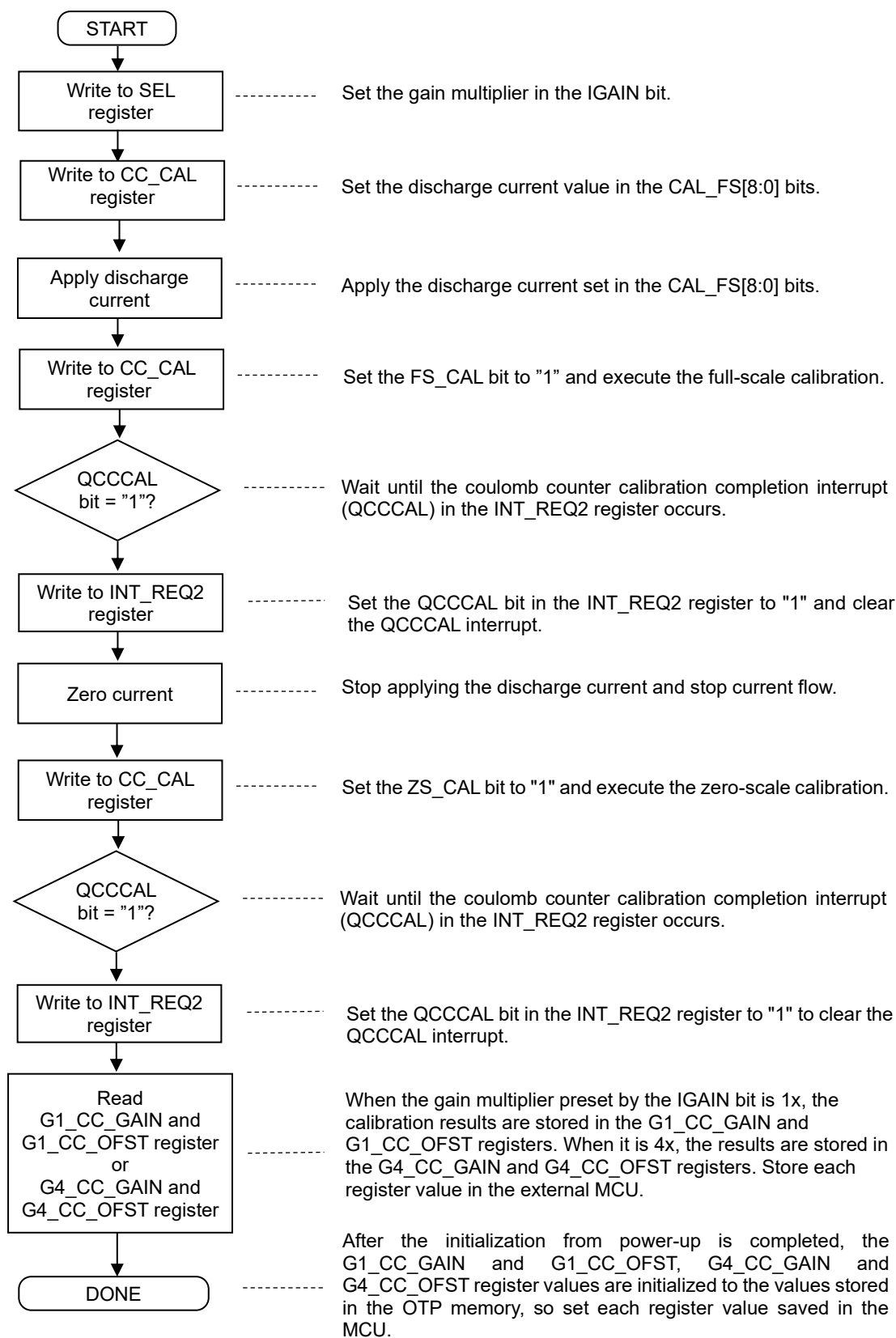
- 2) The ZS_CAL bit initiates zero-scale calibration.
After the calibration is completed, the QCCCAL bit in the INT_REQ2 register is set.

ZS_CAL	Zero-scale calibration
0	Completed (initial value)
1	Execute

- 3) The CAL_FS[8:0] bits set the input full scale when full-scale calibration is executed.
When the current gain is set to 1x,
[When the shunt resistor = 0.5mΩ]
Set CAL_FS[8:0] to a value in the range of 0x003 to 0x136 (-6A to -620A).
[When the shunt resistor = 1.0mΩ]
Set CAL_FS[8:0] to a value in the range of 0x003 to 0x136 (-3A to -310A).
When the current gain is set to 4x,
[When the shunt resistor = 0.5mΩ]
Set CAL_FS[8:0] to a value in the range of 0x003 to 0x136 (-1.5A to -155A)
[When the shunt resistor = 1.0mΩ]
Set CAL_FS[8:0] to a value in the range of 0x003 to 0x136 (-0.75A to -77.5A)

※if the set full-scale current is insufficient, the calibration accuracy may decrease.

The flow chart for executing the coulomb counter calibration is shown below. Calculate the calibration values following the flowchart corresponding to each current-gain multiplier.



94.G1_CC_GAIN register (Adrs = 0x7E)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G1_CC_GAIN[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The G1_CC_GAIN register is used to set the gain correction value for the current measurement result when the gain is 1x. The initial value is the correction value determined during the LSI manufacturing process.

The relationship between the G1_CC_GAIN[15:0] bits and the gain correction value is as follows:

$$\text{Gain correction value} = 1 + 2^{(-13)} * 3 * \text{G1_CC_GAIN (2's complement binary)}$$

G1_CC_GAIN[15:0]	Gain correction value
0x0000	1.0000
0x0001	1.0004
0x0002	1.0007
0x0003	1.0011
...	...
0x7FFC	12.9985
0x7FFD	12.9989
0x7FFE	12.9993
0x7FFF	12.9996

G1_CC_GAIN[15:0]	Gain correction value
0x8000-0xF555	Setting prohibited
0xF556	0.0002
0xF557	0.0006
0xF558	0.0010
...	...
0xFFFFC	0.9985
0xFFFFD	0.9989
0xFFFFE	0.9993
0xFFFFF	0.9996

95.G1_CC_OFST register (Adrs = 0x7F)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G1_CC_OFST[15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The G1_CC_OFST register is used to set the offset correction value for the current measurement result when the gain is 1x. The initial value is the correction value determined during the LSI manufacturing process.

The relationship between the G1_CC_OFST[15:0] bits and the offset correction value at the current measurement resolution LSB = 18.9212mA when the shunt resistor is 0.5 mΩ.

G1_CC_OFST[15:0]	Offset correction value
0x0000	0
0x0001	+1LSB
0x0002	+2LSB
0x0003	+3LSB
...	...
0x7FFC	+32765LSB
0x7FFD	+32766LSB
0x7FFE	+32767LSB

G1_CC_OFST[15:0]	Offset correction value
0x8000	-32768LSB
0x8001	-32767LSB
0x8002	-32766LSB
0x8003	-32765LSB
...	...
0xFFFFD	-3LSB
0xFFFFE	-2LSB
0xFFFFF	-1LSB

96. G4_CC_GAIN register (Adrs = 0x80)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G4_CC_GAIN [15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The G4_CC_GAIN register is used to set the gain correction value for the current measurement result when the gain is 4x. The initial value is the correction value determined during the LSI manufacturing process.

The relationship between the G4_CCGAIN[15:0] bits and the gain correction value is as follows:

Gain correction value = $1 + 2^{(-13)} * 3 * \text{G4_CC_GAIN}$ (2's complement binary)

G4_CC_GAIN [15:0]	Gain correction value
0x0000	1.0000
0x0001	1.0004
0x0002	1.0007
0x0003	1.0011
...	...
0x7FFC	12.9985
0x7FFD	12.9989
0x7FFE	12.9993
0x7FFF	12.9996

G4_CC_GAIN [15:0]	Gain correction value
0x8000-0xF555	Setting prohibited
0xF556	0.0002
0xF557	0.0006
0xF558	0.0010
...	...
0xFFFC	0.9985
0xFFFD	0.9989
0xFFFE	0.9993
0xFFFF	0.9996

97. G4_CC_OFST register (Adrs = 0x81)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	G4_CC_OFST [15:0]															
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The G4_CC_OFST register is used to set the offset correction value for the current measurement result when the gain is 4x. The initial value is the correction value determined during the LSI manufacturing process.

The relationship between the G4_CC_OFST[15:0] bits and the offset correction value at the current measurement resolution LSB = 4.7304mA when the shunt resistor is 0.5 mΩ.

G4_CC_OFST [15:0]	Offset correction value
0x0000	0
0x0001	+1LSB
0x0002	+2LSB
0x0003	+3LSB
...	...
0x7FFC	+32765LSB
0x7FFD	+32766LSB
0x7FFE	+32767LSB

G4_CC_OFST [15:0]	Offset correction value
0x8000	-32768LSB
0x8001	-32767LSB
0x8002	-32766LSB
0x8003	-32765LSB
...	...
0xFFFD	-3LSB
0xFFFE	-2LSB
0xFFFF	-1LSB

98.RTEMP12 register (Adrs = 0x82)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RTEMP2[7:0]								RTEMP1[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The RTEMP12 register sets the correction value for the 10kΩ pull-up resistors on the TEMP1 and TEMP2 pins.

The initial value is the correction value determined during the LSI manufacturing process.

The relationship between the RTEMP1[7:0] bits and correction values is shown in the table below. The LSB is set to 20Ω. RTEMP2[7:0] has the same format.

The RTEMP12 register value can be rewritten, but it does not affect the temperature detection operation.

RTEMP1[7:0]	Correction value
0x00	0
0x01	+1LSB (+20Ω)
0x02	+2LSB (+40Ω)
0x03	+3LSB (+60Ω)
...	...
0x7D	+125LSB (+2500Ω)
0x7E	+126LSB (+2520Ω)
0x7F	+127LSB (+2540Ω)

RTEMP1[7:0]	Correction value
0x80	-128LSB (-2560Ω)
0x81	-127LSB (-2540Ω)
0x82	-126LSB (-2520Ω)
0x83	-125LSB (-2500Ω)
...	...
0xFD	-3LSB (-60Ω)
0xFE	-2LSB (-40Ω)
0xFF	-1LSB (-20Ω)

99.RTEMP34 register (Adrs = 0x83)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RTEMP4[7:0]								RTEMP3[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The RTEMP34 register sets the correction value for the 10kΩ pull-up resistors on the TEMP3 and TEMP4 pins.

The initial value is the correction value determined during the LSI manufacturing process.

The relationship between the RTEMP3[7:0] bits and correction values is shown in the table below. The LSB is set to 20Ω. RTEMP4[7:0] has the same format.

The RTEMP34 register value can be rewritten, but it does not affect the temperature detection operation.

RTEMP3[7:0]	Correction value
0x00	0
0x01	+1LSB (+20Ω)
0x02	+2LSB (+40Ω)
0x03	+3LSB (+60Ω)
...	...
0x7D	+125LSB (+2500Ω)
0x7E	+126LSB (+2520Ω)
0x7F	+127LSB (+2540Ω)

RTEMP3[7:0]	Correction value
0x80	-128LSB (-2560Ω)
0x81	-127LSB (-2540Ω)
0x82	-126LSB (-2520Ω)
0x83	-125LSB (-2500Ω)
...	...
0xFD	-3LSB (-60Ω)
0xFE	-2LSB (-40Ω)
0xFF	-1LSB (-20Ω)

100.OTPACPT register (Adrs = 0x84)

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name		-	-	-	-	-	-	-	-	OTPACPT[7:0]							
R/W		R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTPACPT register is used to set the access permission for the OTP register.

Setting the OTPACPT[7:0] bits to 0xC3 permits access to the OTP register. The access permission for the OTP register will remain enabled unless the setting is changed from 0xC3.

Note that when the OTPACPT[7:0] bits are set to 0xC3, the INTEGCL and INTEGCH register values will not be updated.

101.OTP register (Adrs = 0x85)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	-	-	-	-	-	-	-	-	-	LDWA	LDER	LOAD	-	-	-	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The OTP register is used to set the load operation of the OTP memory.
Before accessing the OTP register, set the OTPACPT register to 0xC3.

When the LOAD bit is set to "1"

[Operation]

- The contents of the OTP memory are loaded into each register.
- When the load operation is completed, the LOAD bit is reset to "0", and the QOTP bit in the INT_REQ2 register is set to "1".

[When an error is detected during the load operation]

- The LDER bit is set to "1", an "H" level is output to the FUSE pin regardless of the FUSE register and POWER register settings, and the LSI enters the sleep state.
- At this time, the FUSE bit in the STATUS2 register is set to "1".
- Even after entering the sleep state, the LSI outputs an "H" level continuously to the FUSE pin.

[Note]

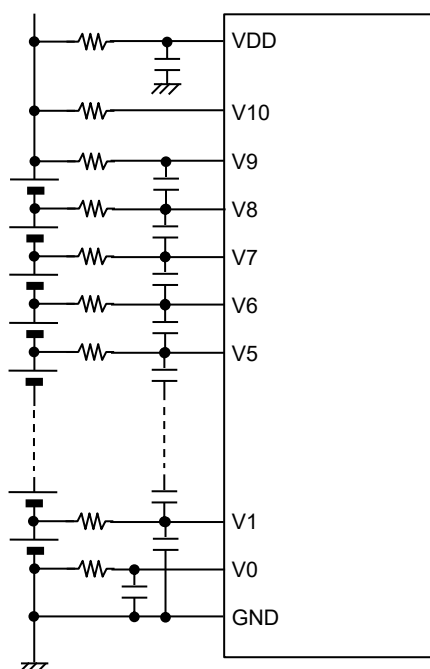
- If a load error is detected, the LSI cannot return to the normal state from the sleep state.
- If a load operation is performed after a power-supply comparator abnormality is detected, the LDWA bit is set to "1".

That all register access is prohibited during the load operation of the OTP memory. Therefore, before accessing each register, set the EOTP bit in the INT_EN2 register to "1" and detect the occurrence of a QOTP interrupt on the /INTO pin output.

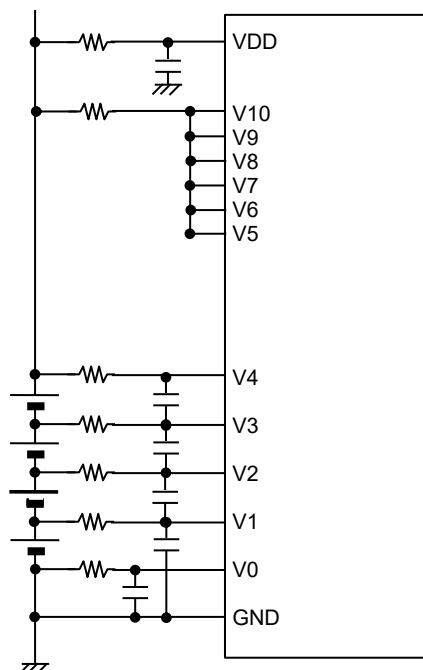
- Cell Connection Method

When the number of connected cells is 9 or less, connect the Vn pin from the lower cell, and connect the unused Vn pin to the top cell via a resistor.

When connecting 9 cells



When connecting 4 cells



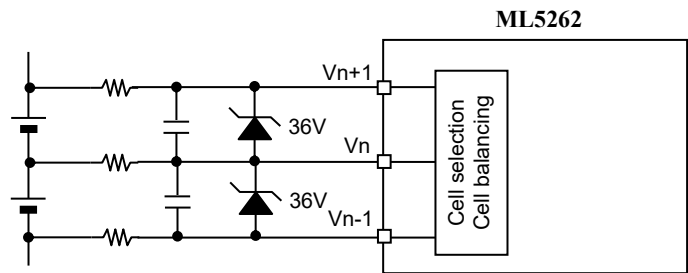
• Power-on/off Sequence

At power-up, it is recommended to connect the battery cells in order from the lower cells after connecting the GND and VDD terminals. If this connection order is not followed, the voltage between the cell connection terminals Vn+1 and Vn may exceed the absolute maximum rating, which can result in the LSI destruction.

At power-off, remove the cell connections starting from the highest cell, and disconnect the VDD and GND terminals last, in that order.

Also, when evaluating or inspecting using a battery simulator or similar, pay careful attention to the procedures for connecting and disconnecting the power supply so that the voltage between the cell connection terminals Vn+1 and Vn does not exceed the absolute maximum rating.

For terminal protection, it is recommended to add external TVS diodes as illustrated below. Ensure adequate evaluation is performed when using the LSI with the added TVS diodes.



Connect the battery cells to each cell-connection terminal Vn after the battery cells have been connected in series in advance.

Connecting battery cells one by one when they are not already connected in series is prohibited, as the voltage between the Vn+1 and Vn terminals may exceed the absolute maximum rating and cause the LSI destruction.

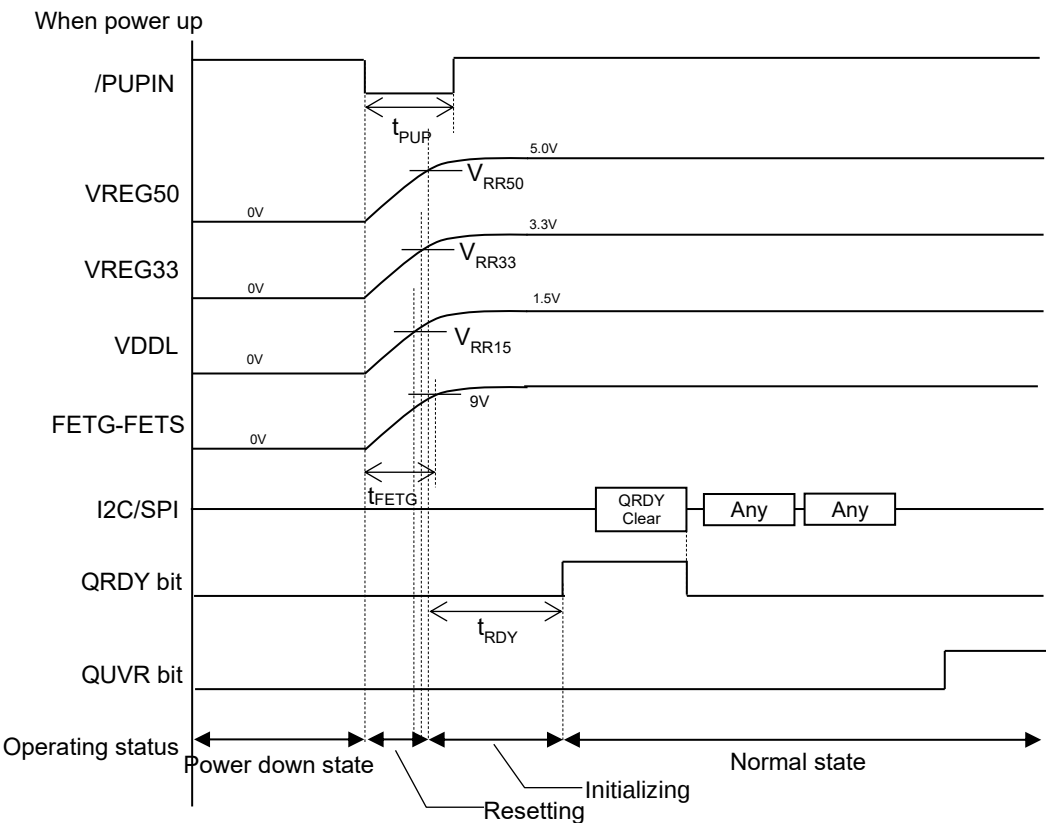
At power-up, ensure that the power-supply voltage rises to 4.5V or higher within 5ms.

Note that the initial state after power-up starts from the over-discharge detection state. Therefore, until the LSI transitions to the over-discharge release state, apply a voltage equal to or higher than the PSNS charger-connection detection threshold V_{PC1} to the PSNS terminal, or input an "L" level to the /PUPIN terminal.

For details, refer to the Power-Up and Sleep-Release Characteristics section.

After power-on and after a power-up operation, an initialization sequence is executed. Therefore, perform all initial settings only after the QRDY bit in the INT_REQ1 register is set. Accessing any register before the QRDY bit is set is prohibited.

The operation timing chart during power-up after power-on is shown below.

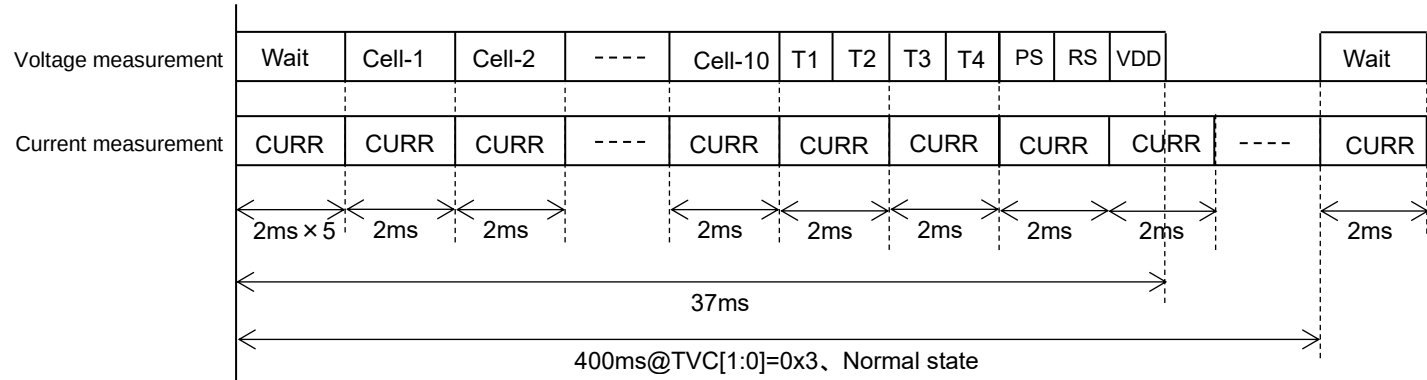


• Measurement Sequence

The ML5262 repeatedly measures cell voltage, temperature, and PSNS, RSNS, VDD pin voltage and current in a specified sequence.

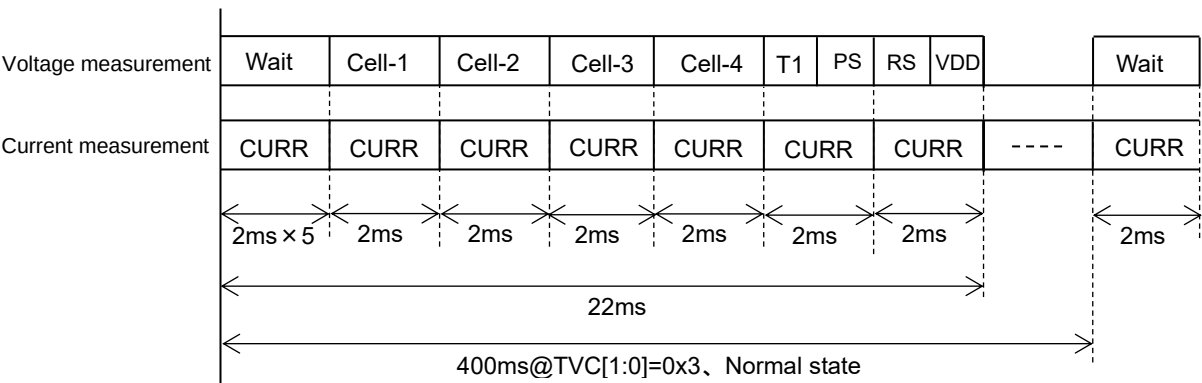
The sequences of various voltage and current measurements are shown below.

[Number of connected cells = 10cells, with all TEMP pins measurements]



The current measurement results when measuring each cell voltage, are stored in the G1_ICELLn or G4_ICELLn registers and the G1_CURR or G4_CURR registers. The resistance value of the battery cell can be obtained from the simultaneous measurement results of each cell's voltage and current.

[Number of connected cells = 4cells, with onlyl measuring TEMP1 pin]

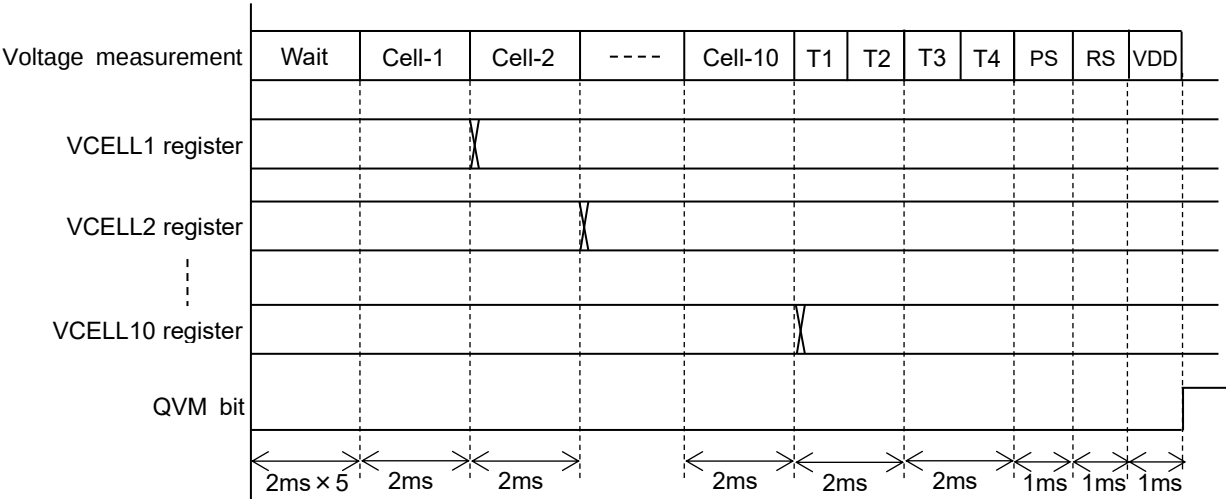


The unmeasured voltage measurement sequence will be deleted according to the number of connected battery cells and the measurement TEMP pin set in the SEL register, but the cell voltage measurement cycle set in the PERIOD register will not change.

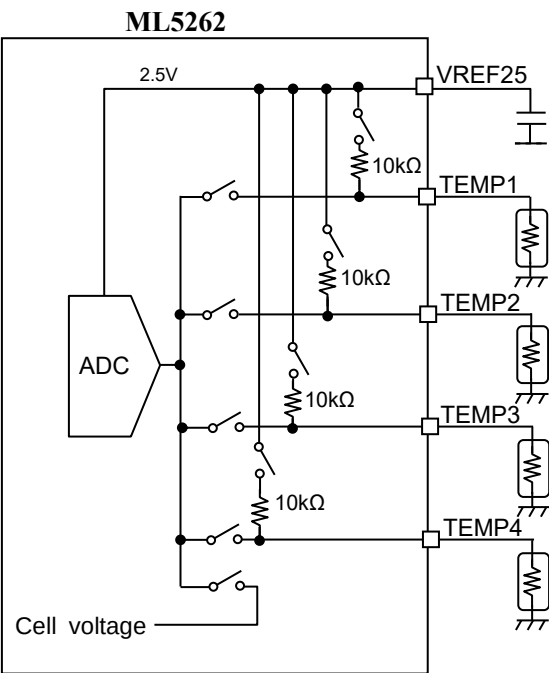
Cell Voltage Measurement Function

The cell voltages are measured starting from the lowest cell up to the number of connected cells specified by the CELL[3:0] bits in the SEL register. The measurement time for each cell voltage is 2ms (typ.), and the result is stored in the VCELLn registers. The cell voltage measurement results should be read after the voltage measurement completion interrupt (QVM) bit set. Each VCELLn register is updated with the new measurement result for every cell voltage measurement cycle set by the TVC[1:0] bit in the PERIOD register.

The following is a timing chart showing cell voltage (number of connected battery cells = 10 cells) and temperature measurements at all TEMPn pins.



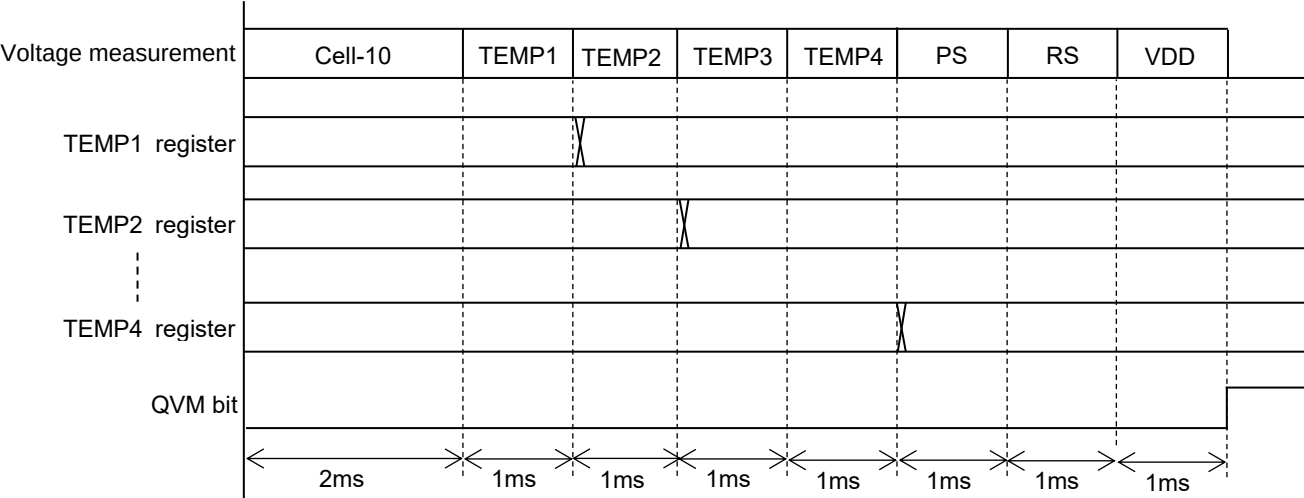
- Temperature Sensor Measurement
- Connect a thermistor to each TEMPn pin as shown below. A pull-up resistor of 10 kΩ (typ.) is built in between each TEMP pin and the VREF25 pin, and the pull-up resistor is automatically connected when measuring the voltage at each TEMP pin according to the setting of the RPUP[3:0] bits in the SETOTUT register. The pull-up resistor correction value is stored in the RTEMP12 and RTEMP34 registers, so use them when calculating the temperature.



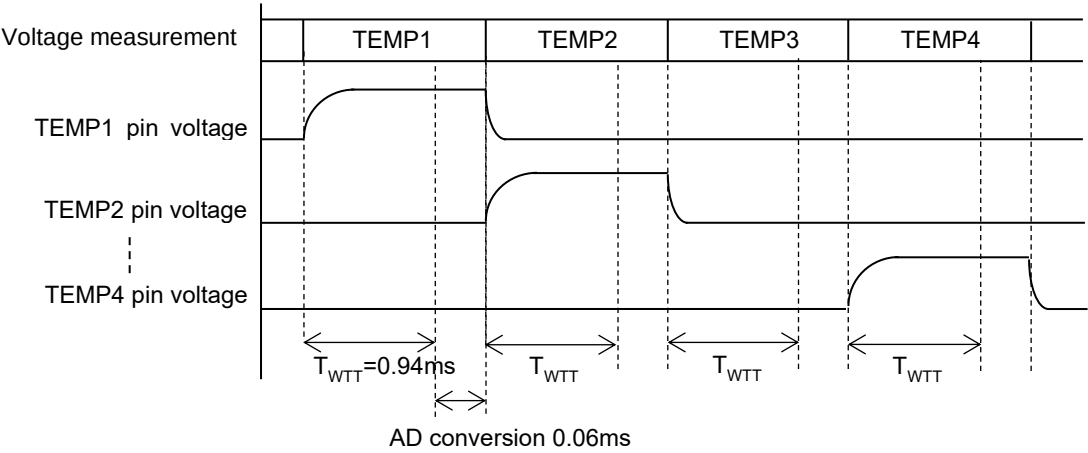
The TEMP pin voltage is measured in order, starting from TEMP1, for the TEMP pin specified by the TSEL[3:0] bits in the SEL register.

The measurement time for each TEMP pin voltage is 1ms (typ.), and the measurement result is stored in the TEMPn register. The TEMP pin voltage measurement result should be read after the voltage measurement completion interrupt (QVM) bit has been set. Each TEMPn register is updated with a new measurement result for every cell voltage measurement cycle set by the TVC[1:0] bits in the PERIOD register.

The following is a timing chart showing temperature measurements at all TEMP pins when the number of connected battery cells is 10.

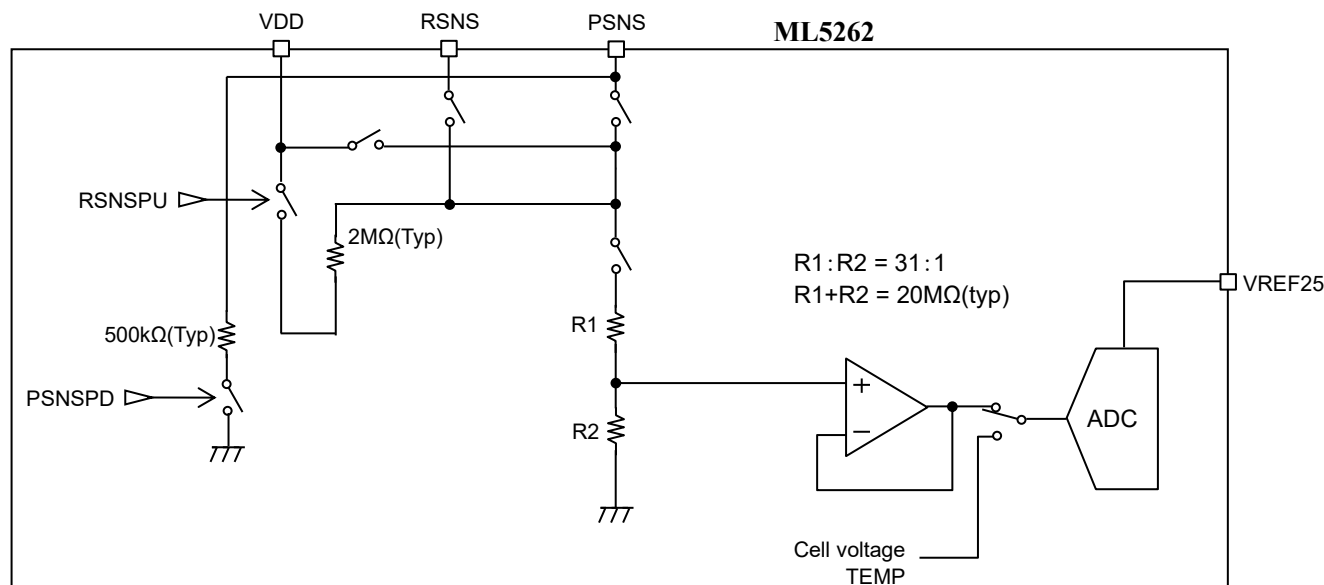


Voltage measurement for each TEMP pin begins after a stabilization time of 0.94ms (typ.) has elapsed since the built-in pull-up resistor was connected. If connect a capacitor to each TEMPn pin, select a capacitance value that will allow the TEMP pin voltage to stabilize within this time.



• PSNS / RSNS / VDD Pin Voltage Measurement

The voltage measured is the input voltage at the PSNS, RSNS, and VDD pins divided by 1/32.
The measurement circuit inside the LSI is shown below.



The measurement time for each of the voltages at the PSNS, RSNS, and VDD pins is 1ms (typ.), and each measurement result is stored in the PSNS, RSNS, and VDD registers. Read the measurement results of PSNS, RSNS, and VDD pin voltages after the voltage measurement completion interrupt (QVM) bit has been set.

The PSNS, RSNS, and VDD registers are updated with a new measurement result for every cell voltage measurement cycle set by the TVC[1:0] bits in the PERIOD register.

The voltage measurements at the PSNS, RSNS, and VDD pins start after the internal 1/32-divider resistors are connected and a setting time of 0.94 ms (typ.) has elapsed, similar to the TEMP pin.

The pull-down resistor of the PSNS pin and the pull-up resistor of the RSNS pin are automatically connected depending on the abnormal-detection status. However, when controlling the connection from the MCU, control it using the ENRSNS, PSNSPD, and ENPSNS, RSNSPU bits in the POWER register.

By measuring the voltage at the RSNS and PSNS pins, the load connection status of the battery pack output can be determined.

[When in a discharge over-current or short-circuit detection state]

A 2 MΩ pull-up resistor is connected to the RSNS pin (to detect load disconnection at the battery-pack output). When the RSNS pin voltage becomes the voltage V_{RL} , which is close to the VDD voltage, the LSI recognizes a load-disconnect condition.

[When in a charge over-current or over-discharge detection state]

A 500 kΩ pull-down resistor is connected to the PSNS pin (to detect charger disconnection at the battery-pack output).

When the PSNS pin voltage becomes the voltage V_{PLU} , which is lower than the VDD pin voltage, the LSI recognizes a charger-disconnect condition.

The charger-disconnect detection during charge over-current is performed by comparing the voltage difference V_{PLU} between the VDD-pin voltage-measurement result (VDD register value) and the PSNS-pin voltage-measurement result (PSNS register value).

Similarly, pre-discharge-completion detection is performed by comparing the voltage difference between the VDD-pin voltage-measurement result (VDD register value) and the RSNS-pin voltage-measurement result (RSNS register value). In addition, the voltages at the PSNS, RSNS, and VDD pins are not measured in the power-save state.

- Current Measurement

The voltage between the ISP pin and ISM pin is measured every 2 ms using a 16-bit $\Delta\Sigma$ ADC, and the result is stored in the G1_CURR register or C4_CURR register.

[Current-gain of 1x]

When shunt resistor is 0.5m Ω , the current measurement resolution is 18.9212mA.

When shunt resistor is 1.0m Ω , the current measurement resolution is 9.4606mA.

[Current-gain of 4x]

When shunt resistor is 0.5m Ω , the current measurement resolution is 4.7304mA.

When shunt resistor is 1.0m Ω , the current measurement resolution is 2.3652mA.

In addition, the current measurement results are stored in the G1_ICELLn or G4_ICELLn registers synchronized with the cell voltage measurement cycle of each cell, making it possible to calculate the resistance value of each cell.

• Current-gain Adjustment Function

The current gain for the voltage between the ISP and ISM pins can be changed to 1× or 4× by using the IGAIN bit in the SEL register. The recommended operations for switching between 1× and 4× are shown below.

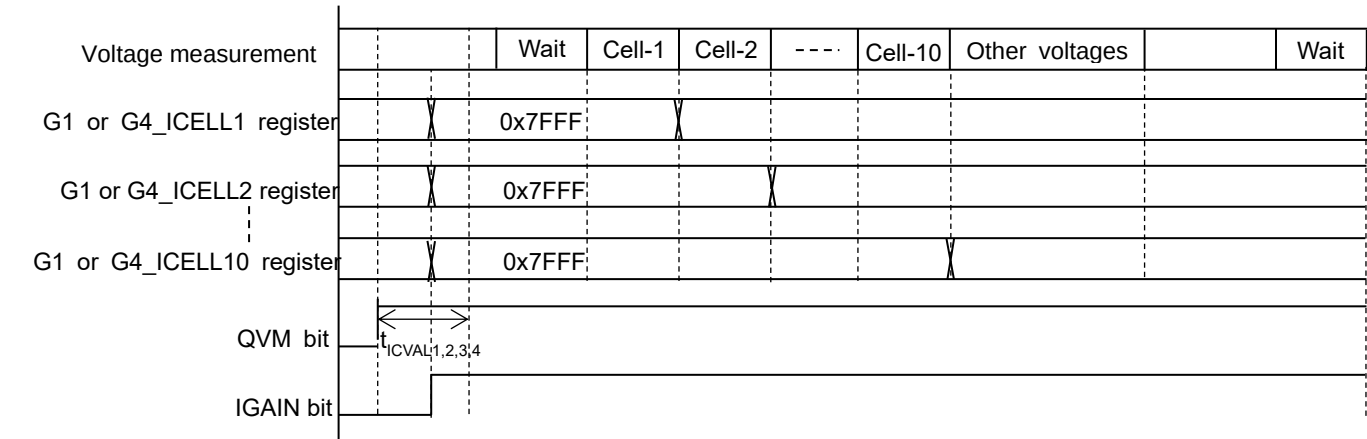
- [When switching from 1× to 4×]
After reading the G1_CURR register and confirming that no current abnormality is present, perform the gain switching.
- [When switching from 4× to 1×]
After detecting the QORG interrupt output, perform the gain switching.

During the $\Delta\Sigma$ -ADC settling time after the gain switching, the various current-measurement result registers store the invalid value 0x7FFF. After the settling time has elapsed, the measurement results are stored in the G1_CURR and G4_CURR registers and the G1_ICELLn and G4_ICELLn registers according to the current-gain setting. If the gain is switched during a voltage-measurement sequence, the G1_ICELLn and G4_ICELLn registers will store the invalid value 0x7FFF for that measurement sequence, and valid measurement results will be stored starting from the next measurement sequence. If you need valid results starting from that next measurement sequence, the timing of the gain switching triggered by the QVM interrupt output depends on the setting of the TVC[1:0] bits in the PERIOD register.

TVC[1:0] bit	The timing of the gain switching triggered by the QVM interrupt output
0x0	Within t _{ICVAL1}
0x1	Within t _{ICVAL2}
0x2	Within t _{ICVAL3}
0x3	Within t _{ICVAL4}

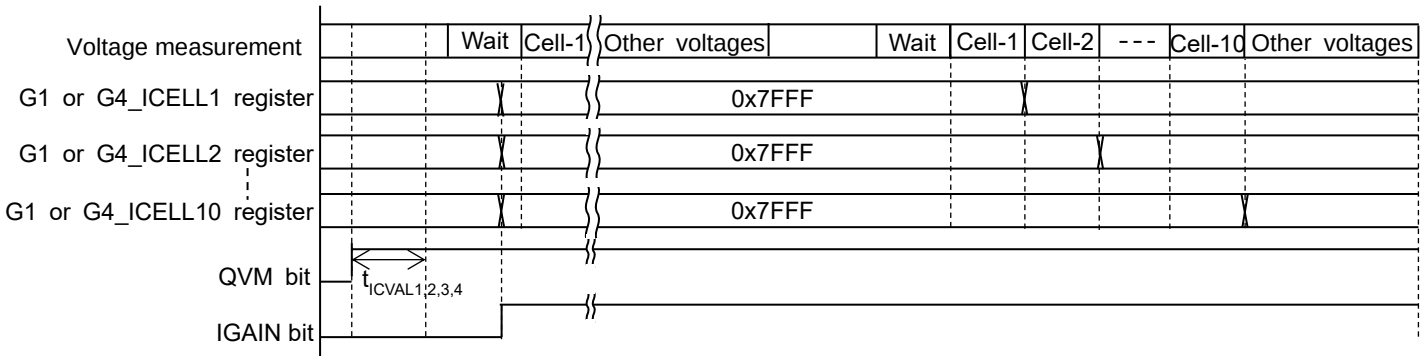
The differences in the sequences when switching the current gain at t_{ICVAL1}, t_{ICVAL2}, t_{ICVAL3}, and t_{ICVAL4}, compared with switching at other timings, are shown below.

[Switching the IGAIN bit within the t_{ICVAL1,2,3,4}]



When the IGAIN bit is switched within the t_{ICVAL1,2,3,4} interval after the rising edge of the QVM bit, the measurement results are stored in the G1_ICELLn or G4_ICELLn registers starting from that measurement sequence.

[Switching the IGAIN bit outside the t_{ICVAL1,2,3,4}]



When the IGAIN bit is switched outside the t_{ICVAL1,2,3,4} time windows after the rising edge of the QVM bit, the measurement results are stored in the G1_ICELLn or G4_ICELLn registers starting from the next measurement sequence.

• Coulomb Counter

The LSI has a coulomb counter that integrates the current measurement results.
The results of integration over the cycle specified by the CC[1:0] bits of the PERIOD register are stored in the CCL and CCH registers, and the results of continuous integration are stored in the INTEGCL and INTEGCH registers.
The CCL and CCH registers are updated at the specified cycle, so read the register values each time the coulomb counter integration completion interrupt (QCC) in the INT_REQ1 register occurs and have the MCU accumulate the values. The remaining battery capacity can be calculated considering the battery cell's self-discharge amount.
By simply setting the battery capacity value when the battery is fully charged, the remaining battery capacity can be determined using the INTEGCL and INTEGCH registers, eliminating the need for integration by the MCU.

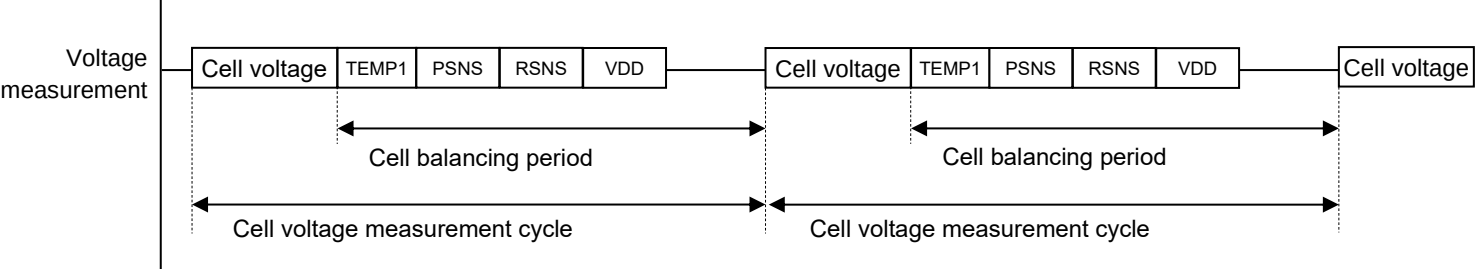
The setting unit of the CCL register is as follows:
 $\text{Current measurement resolution} \times 0.002 (\text{CURR measurement period}) / 3600 [\text{Ah}]$
*When the shunt resistance is 0.5mΩ, it is 10.5118nAh.

The setting unit of the INTEGCL register is as follows:
 $\text{Current measurement resolution} \times 0.002 (\text{CURR measurement cycle}) / 3600 \times 4 [\text{Ah}]$
*When the shunt resistance is 0.5mΩ, it is 42.048nAh.

• Cell Balancing Function

If the difference between the cell voltage measurement result and the lowest cell voltage is equal to or higher than the cell balancing start potential difference set in the CBALST[11:0] bits in the CBALST register and the cell voltage is equal to or higher than the cell balancing permission voltage set in the CBALEN[11:0] bits in the CBALEN register, cell balancing is performed outside the cell voltage measurement period.
If the highest cell voltage is an even cell, cell balancing will be performed on the even cells that satisfy the cell balancing conditions. Similarly, if the highest cell voltage is an odd cell, cell balancing will be performed on the odd cells that satisfy the cell balancing conditions.
Cell balancing ends when the potential difference between the cells being balanced falls below the cell balancing end potential difference set by the CBALSP[11:0] bits in the CBALSP register, or when the cell voltage being balanced falls below the cell balancing permission voltage.

The cell balancing execution period is shown below. The cell balancing execution time varies depending on the cell voltage measurement cycle.



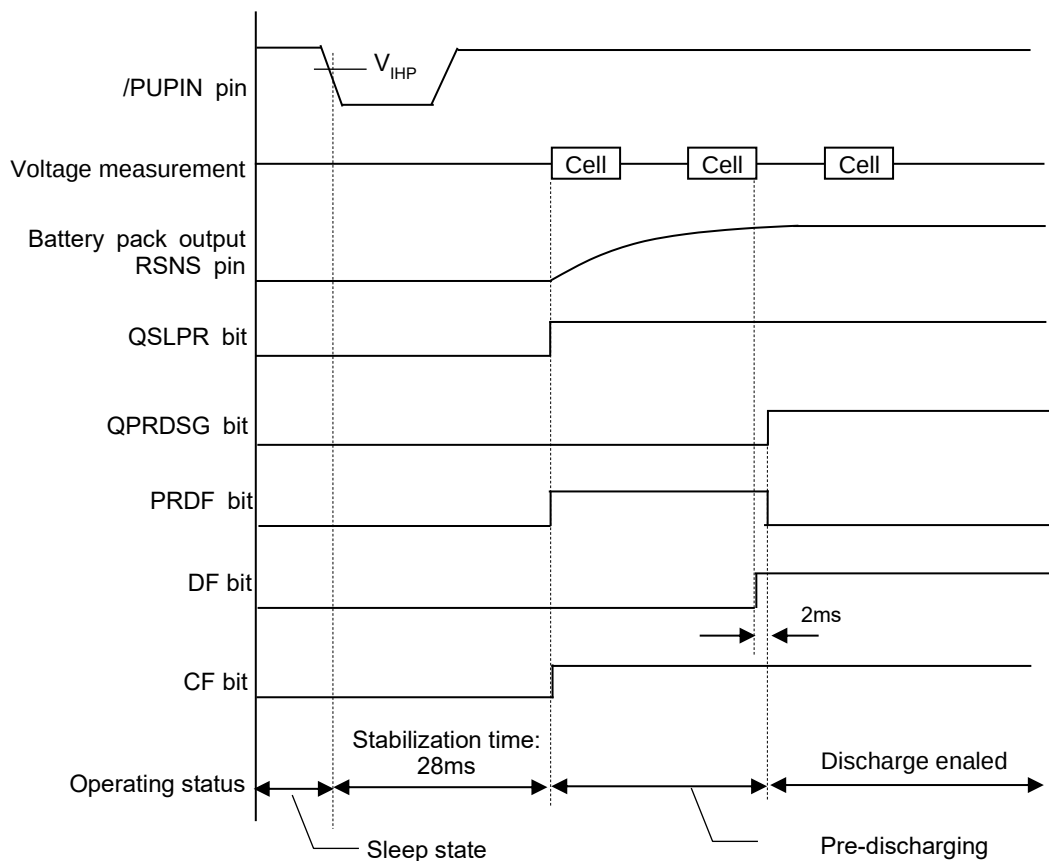
Please select the external resistance value R_{CELL} and capacitance value C_{CELL} for each V_n pin so that the V_n pin input voltage stabilizes within the 2ms (typ.) waiting time from the end of the cell balancing execution period to the start of cell voltage measurement.

• Pre-Discharge Function

The pre-discharge function prevents inrush current when the discharge control FET is changed from off to on by passing a small discharge current until the battery pack output falls below a specified voltage or until a specified time has elapsed. This function can be used at operating voltages up to 45 V.

The VPRDSG[6:0] bits in the PREDSG register set the pre-discharge completion voltage, and the TPRDSG[6:0] bits set the pre-discharge time. For details, refer to the PREDSG register.

Below is a timing chart for returning from the sleep state to the normal state by inputting the /PUPIN pin. This shows the case where the battery pack output drops below the specified voltage.



[Operation Description]

- Input an "L" level to the /PUPIN pin.
- After a settling time of 28 ms, the CF bit and PRDF bit in the FETCBA register are set to "1", and pre-discharge starts.
- The QSLPR bit, the interrupt indicating the return from the sleep state to the normal state in the INT_REQ1 register, is set to "1".
- The battery-pack output voltage (RSNS pin voltage) rises.
- When the difference between the VDD-pin voltage-measurement result and the RSNS-pin voltage-measurement result becomes less than or equal to the voltage set by the VPRDSG[6:0] bits in the PREDSG register, the DF bit in the FETCBAL register is set to "1".
- After 2 ms, the PRDF bit is reset to "0", and the QPRDSG bit, the pre-discharge-completion interrupt, is set to "1".

- Power-save Function

The LSI has a power-save function that slows down the measurement cycle to reduce current consumption. The TVCP[1:0] bits in the PERIOD register set the cell voltage measurement cycle, and the TTPP[1:0] bits set the TEMPn pin measurement cycle.

In standalone control, the LSI automatically enters the power-save state when a specified time has elapsed without any charging or discharge current flowing. When a charging/discharge current starts flowing, the LSI will automatically return to the normal state.

For details, refer to the CHG, DSG, and PWRDLY registers.

It also automatically returns to the normal state if the LSI detects an abnormality in the cell voltage, temperature, or current and starts measuring the detection delay time. The power-save state will be maintained if an abnormality is detected in the watchdog timer or the built-in regulator's voltage drop detection.

To control the transition to the power-save state with the MCU, set the ENPSV bit in the POWER register to "1". When the PSV bit is "1", the LSI unconditionally enters the power-save state from the next measurement cycle and continues until the PSV bit becomes "0". However, if the sleep function is under a standalone control, i.e. the ENSLP bit in the POWER register is "0", the LSI automatically enters the sleep state after the time specified by SLPDLY[3:0] bits in the PWRDLY register has elapsed.

Note that in the power-save state, the PSNS, RSNS, and VDD pins voltage are not measured.

• Sleep Function

The LSI has a sleep function that reduces current consumption even further than the power-save function. In the sleep state, all measurement operations are stopped and become the low current consumption condition and only access to the control register is enabled.

In standalone control, when the power-save state has elapsed for the time specified by the PWRDLY register, the C_FET pin automatically turn off and the LSI enters the sleep state. The operation of the D_FET pin depends on the WKUP bit. When WKUP = '0', the pin is in the OFF state, and when WKUP = '1', it turns ON to perform discharge-current detection. The operation of the PSNS pin also depends on the WKUP bit. When WKUP = '0', a 500 kΩ pull-down resistor is connected and the LSI enters the sleep state. When WKUP = '1', the 500 kΩ pull-down resistor is not connected, and the LSI enters the sleep state. At this time, the sleep state transition interrupt (QSLP) bit in the INT_REQ1 register and the SLP bit of the STATUS1 register are set to "1".

To control the transition to the sleep state with the MCU, set the ENSLP bit in the POWER register to "1". When the SLP bit is "1", the LSI enters the sleep state from the next measurement cycle, all measurement operations stop, the low current consumption condition, and only access to the control register is enabled. However, when the PSNS pin input is at "H" level, even if the SLP bit is set to "1" the LSI will not enter the sleep state until the PSNS pin voltage is equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}).

The PSNS pin condition can be read using the PSNS bit. Before setting the SLP bit to "1", set the C_FET and D_FET pins to the OFF condition, connect a 500kΩ pull-down resistor to the PSNS pin, and then check that the PSNS pin condition is not at the "H" level.

Similarly, even if the SLP bit is set to "1" when the /PUPIN pin input is at the "L" level, the LSI will not enter the sleep state until the /PUPIN pin goes to the "H" level. The /PUPIN pin condition can be read using the PUPIN bit, so before setting the SLP bit to "1", ensure that the /PUPIN pin condition is not at the "L" level.

The following table shows the output condition of each pin after the LSI enters the sleep state.

Pin name	Pin condition during the sleep state
NPNB, VREG50, VREG33, VDDL, /INTO, SDO, FUSE	Same as the normal operation condition
VREF12	1V
VREF25	2V
D_FET, PRD_FET, C_FET	FETS pin voltage
PSNS	When WKUP="0" : 500kΩ pull-down When WKUP="1" : Hi-Z
RSNS	Hi-Z

To return from the sleep state, use one of the following methods.

- (1) When the WKUP bit is "0" and a voltage equal to or higher than the charger connection detection voltage (V_{PC1}) is detected at the PSNS pin.
- (2) Input an "L" level to the /PUPIN pin.
- (3) Set the ENSLP bit in the POWER register to "1" and the SLP bit to "0".
- (4) When the WKUP bit is "1" and discharge current is detected.

* When the WKUP bit is "1", recovery from the sleep state by charger connection detection must be performed using method (2) or (3).

When any of the above conditions are met, the LSI will return to the normal state after a stabilization time of 28ms has elapsed.

Note that if the ENSLP and SLP bits are "1", the LSI will enter the sleep state again if the PSNS pin or /PUPIN pin meets the sleep transition conditions before the stabilization time of 28 ms has elapsed.

• Power-down Function

The LSI has a power-down function that stops most circuit operations and minimizes current consumption.

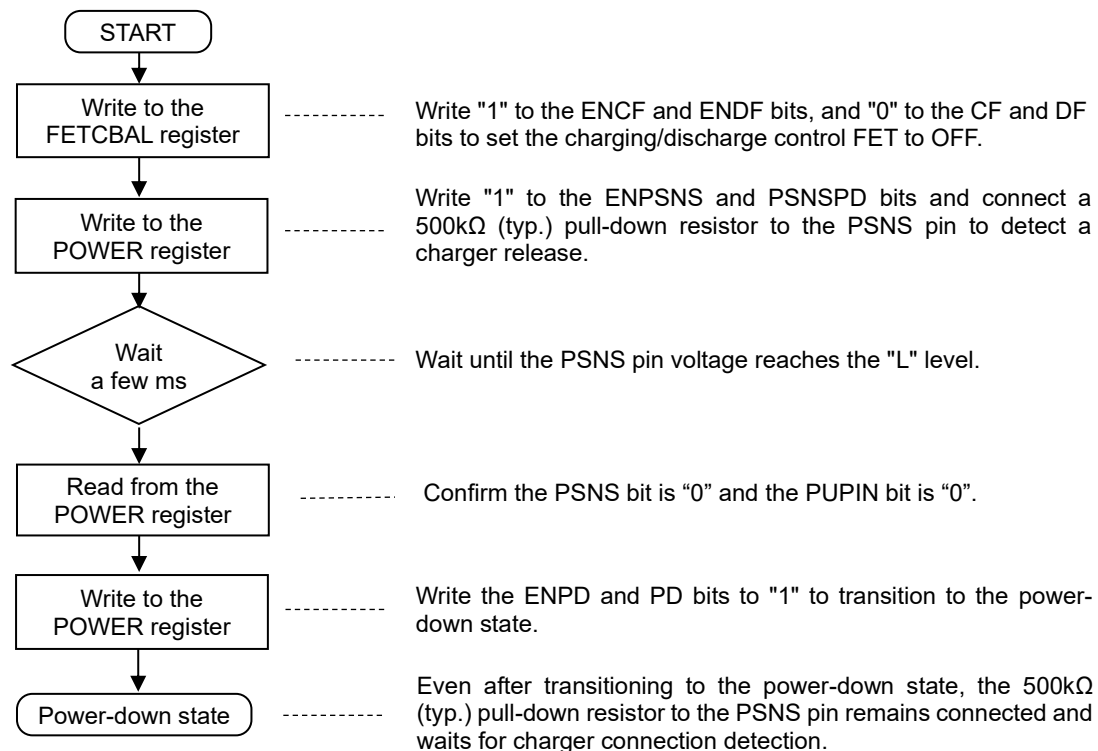
In standalone control, if the time specified by the PDDL[3:0] bits in the PWRDLY register has elapsed after entering the undervoltage condition and the PSNS pin voltage is equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}), the LSI enters the power-down state.

To control the transition to the power-down state with the MCU, set the ENPD bit in the POWER register to "1". After that, setting the PD bit to "1" will stop most circuit operations. However, when the PSNS pin input is at "H" level, even if the PD bit is set to "1" the LSI will not enter the power-down state until the PSNS pin voltage is equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}).

The PSNS pin condition can be read using the PSNS bit in the POWER register. Before setting the PD bit to "1", set the C_FET and D_FET pins to the OFF condition, connect a 500kΩ pull-down resistor to the PSNS pin, and then check that the PSNS pin condition is not at the "H" level.

Similarly, even if the PD bit is set to "1" when the /PUPIN pin input is at the "L" level, the LSI will not enter the power-down state until the /PUPIN pin goes to the "H" level. The /PUPIN pin condition can be read using the PUPIN bit in the POWER register, so before setting the PD bit to "1", ensure that the /PUPIN pin condition is not at the "L" level.

Below is an example of the control flow for transitioning to the power-down state.



The following table shows the output condition of each pin after the LSI enters the power-down state.

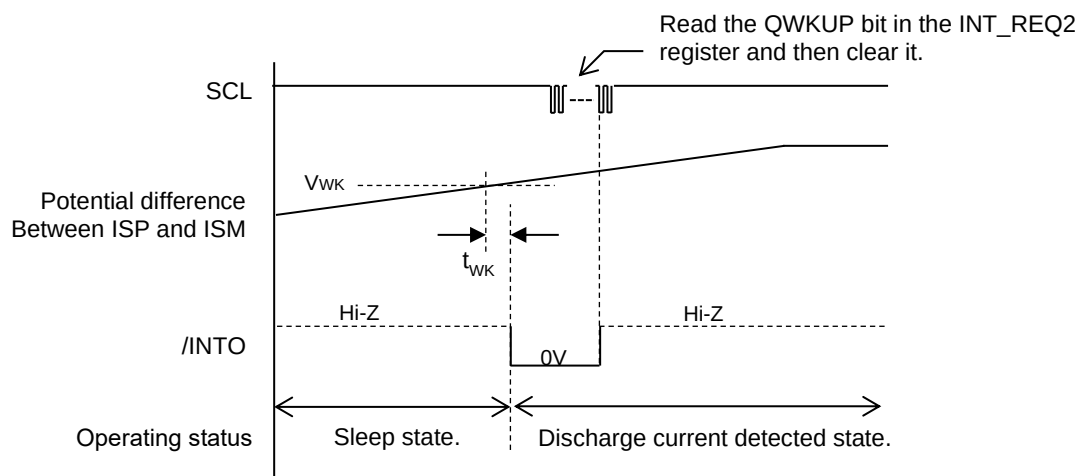
Pin name	Pin condition during the power-down state
NPNB, VREG50, VREG33, VDDL, VREF25, VREF12	0V
/INTO, SDO	Hi-Z
D_FET, PRD_FET, C_FET	FETS pin voltage
FUSE	0V
PSNS	500kΩ pull-down
RSNS	Hi-Z

The LSI will return from the power-down state when a charger connection is detected at the PSNS pin, or when an "L" level is input to the /PUPIN pin. When returning from the power-down state, each control register is initialized with the data stored in the OTP memory. Therefore, perform the various initial settings after the QRDY bit in the INT_REQ1 register has been set.

• Wakeup Detection Function

When the LSI is in the sleep state, it detects that discharge current is flowing by monitoring the potential difference between the ISP and ISM pins, and then wakes up to the normal state. The operating/stop setting of the wake-up detection circuit is controlled by the WKUP bit in the POWER register.

When using this function, make sure that discharge current can flow while the LSI is in the sleep state.



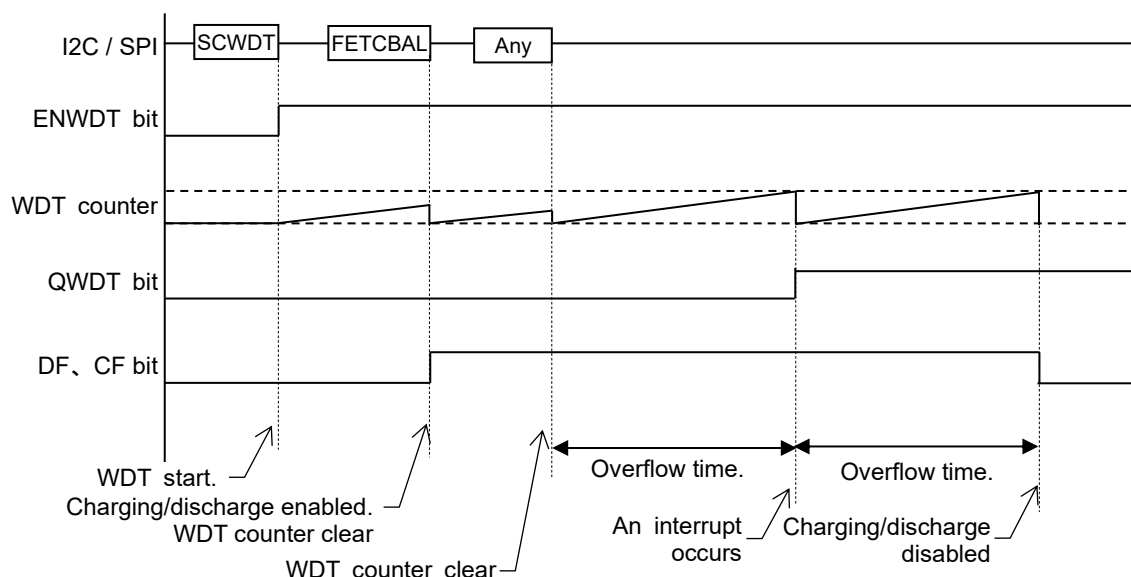
After setting the wake-up detection circuit to the operating state, if the voltage between the ISP and ISM pins becomes equal to or higher than the wake-up detection voltage V_{WK} and this condition continues for a period longer than the wake-up detection delay time t_{WK} , an 'L' level is output to the /INTO pin to notify the MCU. When the INT_REQ2 register is read, the QWKUP bit is set to '1', allowing the MCU to recognize that discharge current has started to flow.

Note that during the sleep state, the short-circuit current detection function is disabled.

• Watchdog Timer Function

The LSI has a watchdog timer function that detects an abnormality if no data write/read operation to the control register is performed for a certain period. The watchdog timer is configured using the SCWDT register. For details, refer to the SCWDT register.

An example of a watchdog timer operation is shown below.



If a data write/read operation to the control register is not performed for the overflow time or longer, the QWDT bit in the INT_REQ2 register is set to "1". The watchdog timer counter is not cleared by a data write/read operation that includes a CRC error.

In addition, if the ENCF, ENDF, and ENPRDF bits in the FETCBAL register are set to "1", when two consecutive overflows are detected, the DF, CF, and PRDF bits are automatically reset to "0" and charging and discharging are prohibited.

Also, if the ENCB bit in the FETCBAL register is set to "1", the CBAL[9:0] bits in the CBAL register are all automatically reset to "0" and the cell balance operation is stopped.

Even if the LSI returns to the normal state, these bits do not automatically return to their original setting, so they must be set again by the external MCU.

If the ENCF, ENDF, and ENPRDF bits in the FETCBAL register are set to "0", even if two consecutive overflows are detected, the DF, CF, and PRDF bits will not be reset and will retain the current setting.

• Standalone Primary Protection Function

The LSI has a standalone protection function that prohibits charging and discharging by comparing the measurement results of cell voltage, temperature, and current as shown below with various abnormality detection thresholds.

1. Overvoltage detection function
2. Undervoltage detection function
3. Charging overcurrent detection function
4. Discharge overcurrent detection function
5. Short-circuit current detection function
6. Discharge prohibition overtemperature detection function
7. Discharge prohibition undertemperature detection function
8. Charging prohibition overtemperature detection function
9. Charging prohibition undertemperature detection function
10. FET overheating protection function

The following describes the various standalone primary protection functions.

1. Overvoltage Detection Function

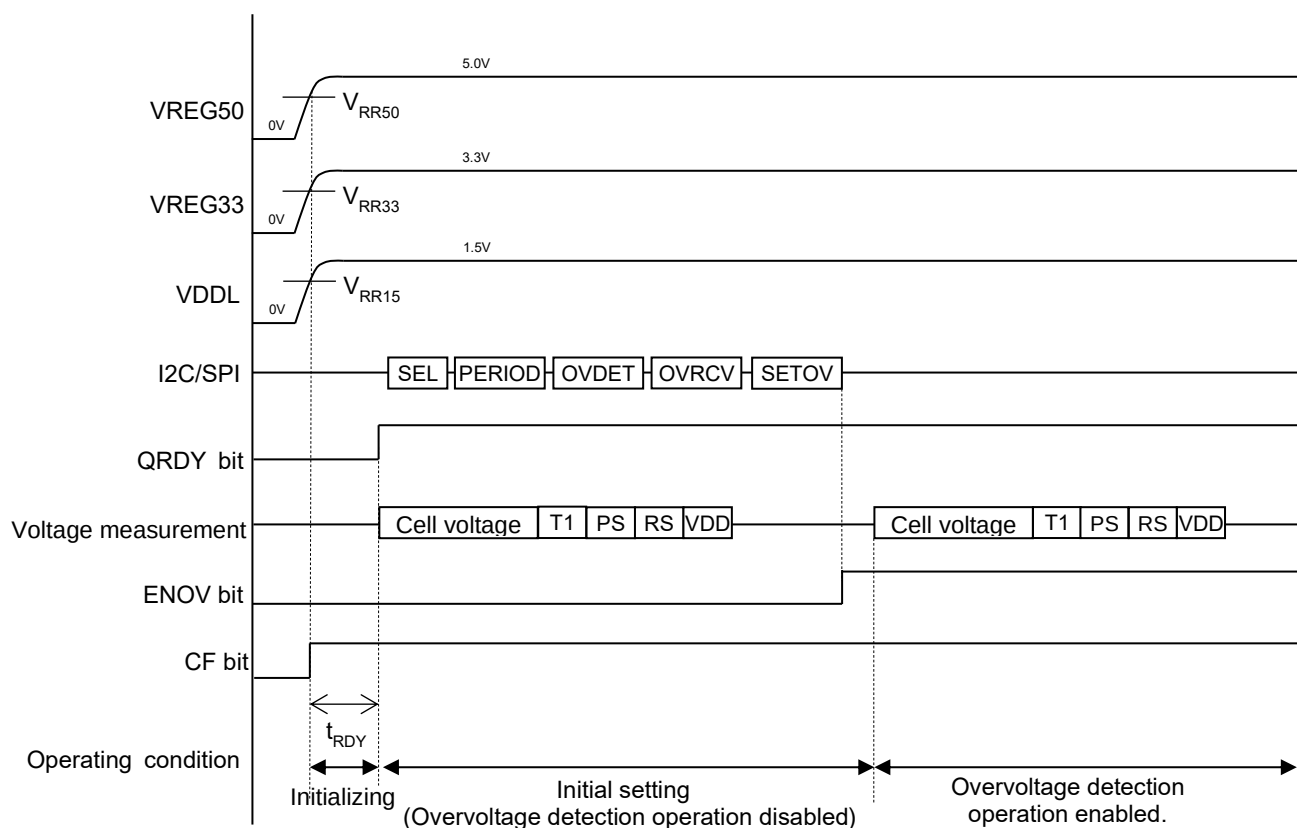
When the value of the cell voltage measurement result register (VCELLn register) exceeds the value of the over charge detection threshold register (OVDET register), and this condition continues for the number of cell voltage measurement cycles specified by the OV[6:0] bits in the SETOV register, the LSI enters the over charge state. In this state, the CF bit in the FETCBAL register is reset to "0", and charging is prohibited.

After configuring the OVDET register and OVDLY bit, set the ENOV bit in the SETOV register to "1" to enable the overvoltage detection function.

When changing the setting, be sure to set the ENOV bit to "0" before changing the settings.

When powering on or power-up state, the LSI starts in the undervoltage and charging permission condition. Therefore, input a voltage equal to or higher than the charger connection detection PSNS pin voltage (V_{PC1}) to the PSNS pin, or input an "L" level to the /PUPIN pin to maintain the power-up condition.

Below is a timing chart for the initializing operation.



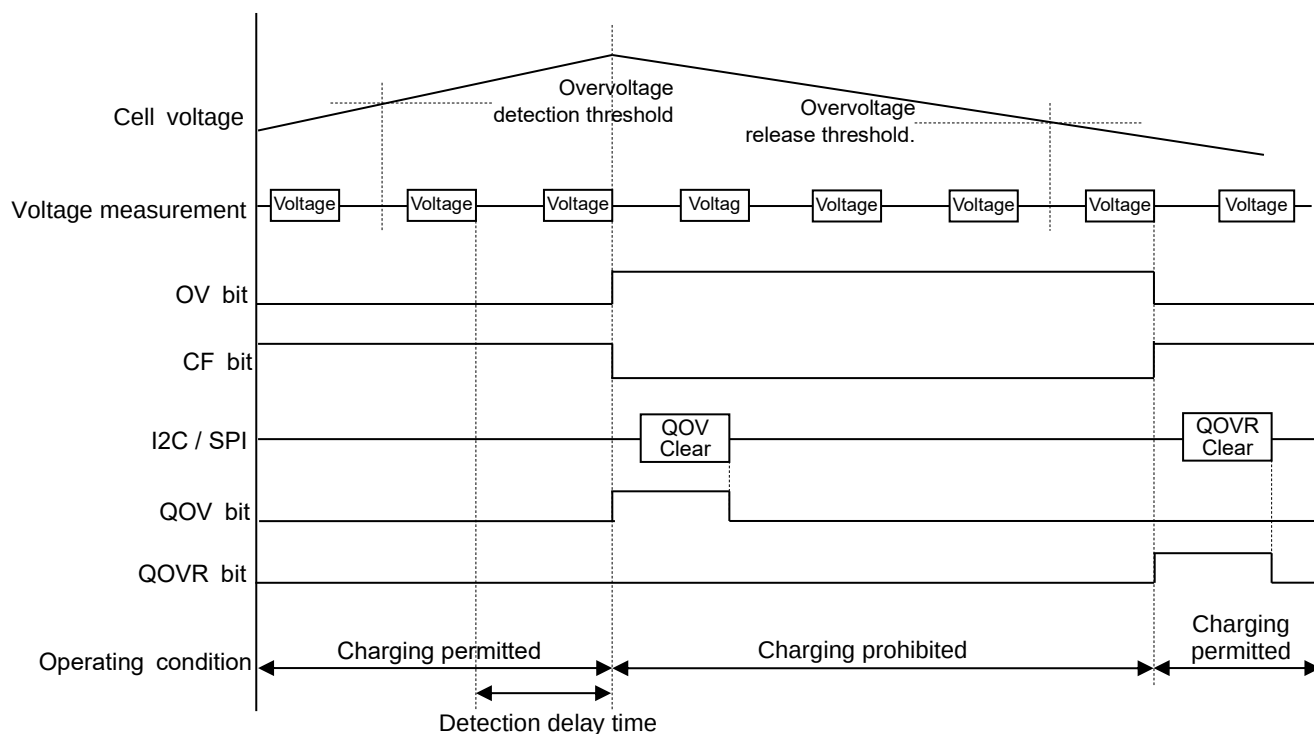
After the QRDY bit has been set, set the number of connected cells, cell voltage measurement cycle, overvoltage detection/release threshold, and overvoltage detection delay time.

Access to each register is prohibited before the QRDY bit has been set.

After setting the ENOV bit to "1", the overvoltage detection operation is enabled from the first voltage measurement sequence, and the cell voltage measurement result is compared with the overvoltage detection/release threshold when the voltage measurement is completed.

Below is a timing chart for the overvoltage detection/release operation.

The detection delay time is when the number of cell voltage measurements count is set to 1, and no other abnormalities are detected.



When one or more battery cells become equal to or higher than the overvoltage detection threshold and this condition continues for the overvoltage detection delay time, the LSI enters the overvoltage state. In this state, the OV bit in the STATUS1 register is set to "1", the CF bit in the FETCBAL register is reset to "0", and charging is prohibited. At the same time, the QOV bit in the INT_REQ1 register is also set to "1", notifying the MCU that an overvoltage condition has been detected.

In addition, if the number of cell voltage measurements as the overvoltage detection delay time is three or more, and one or more battery cells are equal to or higher than the overvoltage detection threshold and the overvoltage detection delay time is waiting to elapse, the detection delay time will be reset if the measurement results of all battery cells fall below the overvoltage detection threshold two consecutive times.

After entering the overvoltage condition, if all battery cells become equal to or lower than the overvoltage release threshold, the overvoltage condition will be released and the OV bit in the STATUS1 register will be reset to "0". In addition, the CF bit in the FETCBAL register is set to "1" and charging is permitted. At the same time, the QOVR bit of the INT_REQ1 register is also set to "1", notifying the MCU that the overvoltage has been released.

2. Undervoltage Detection Function

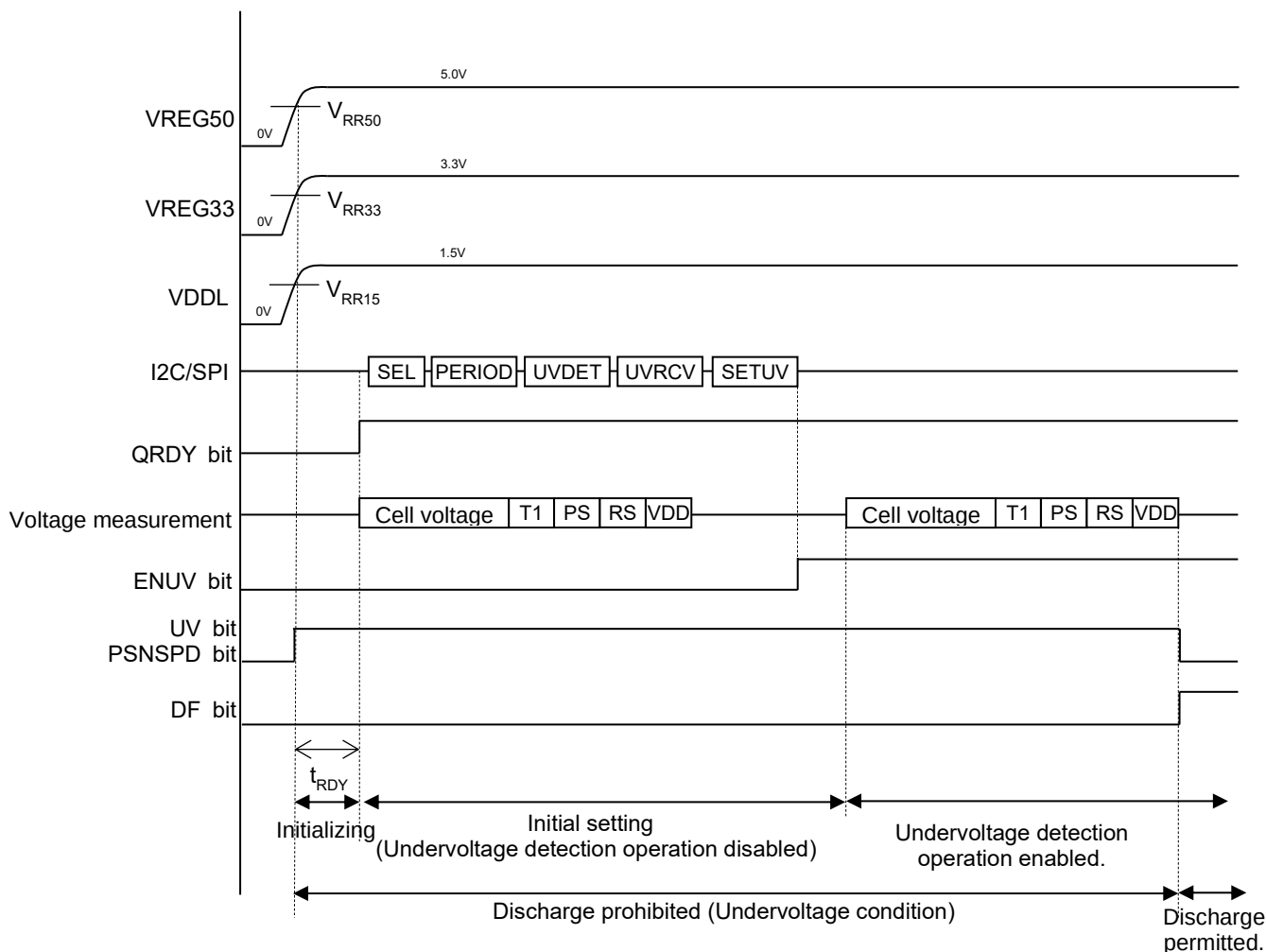
When the value of the cell voltage measurement result register (VCELLn register) becomes equal to or lower than the value of the under voltage detection threshold register (UVDET register), and this condition continues for the number of cell voltage measurement cycles specified by the UVDLY[6:0] bits in the SETUV register, the LSI enters the under voltage state. In this state, the DF bit in the FETCBAL register is reset to "0", and discharging is prohibited.

After configuring the UVDET register and UVDLY bit, set the ENUV bit in the SETUV register to "1" to enable the undervoltage detection function.

When changing the setting, be sure to reset the ENUV bit to "0" before changing the settings.

When powering on or power-up state, the LSI starts in the undervoltage and charging permission condition. Therefore, input a voltage equal to or higher than the charger connection detection PSNS pin voltage (V_{PC1}) to the PSNS pin, or input an "L" level to the /PUPIN pin to maintain the power-up condition.

Below is a timing chart for the initializing operation.



After the QRDY bit has been set, set the number of connected cells, cell voltage measurement cycle, undervoltage detection/release threshold, and undervoltage detection delay time.

Access to each register is prohibited before the QRDY bit has been set.

After setting the ENUV bit to "1", the undervoltage detection operation is enabled from the first voltage measurement sequence, and the cell voltage measurement result is compared with the undervoltage detection/release threshold when the voltage measurement is completed.

If all cell voltages are equal to or higher than the undervoltage release threshold,

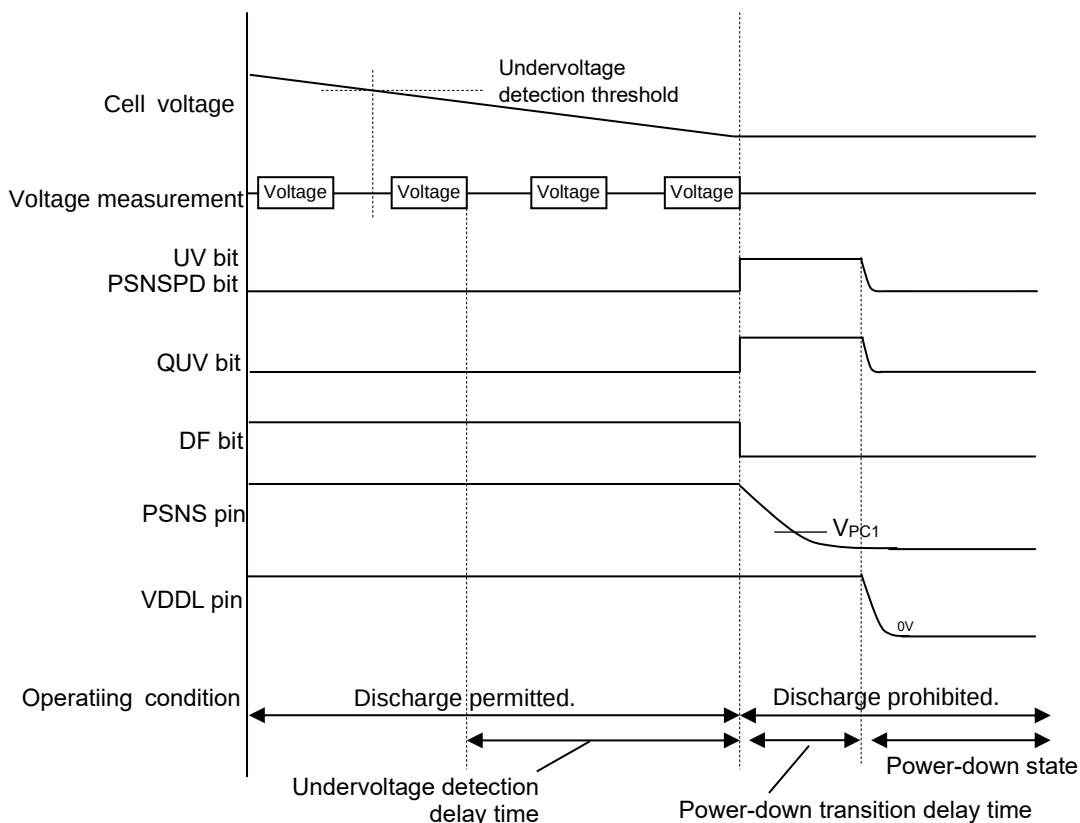
[When the pre-discharge function is disabled]

- The DF bit in the FETCBAL register is set to "1", discharging is permitted, and the undervoltage condition is released.
- The QUVR bit of the INT_REQ1 register becomes "1" to notify the MCU that the discharge is permitted.

[When the pre-discharge function is enabled]

- The PRDF bit is set to "1".
- After pre-discharge is completed, the DF bit is set to "1" and the PRDF bit is reset to "0", discharging is permitted, and the undervoltage condition is released.
- the QUVR bit of the INT_REQ1 register becomes "1" to notify the MCU that the discharge is permitted.

Next is a timing chart for undervoltage detection and transition to the power-down state. The detection delay time is when the number of cell voltage measurement counts is set to 2, and no other abnormalities are detected.

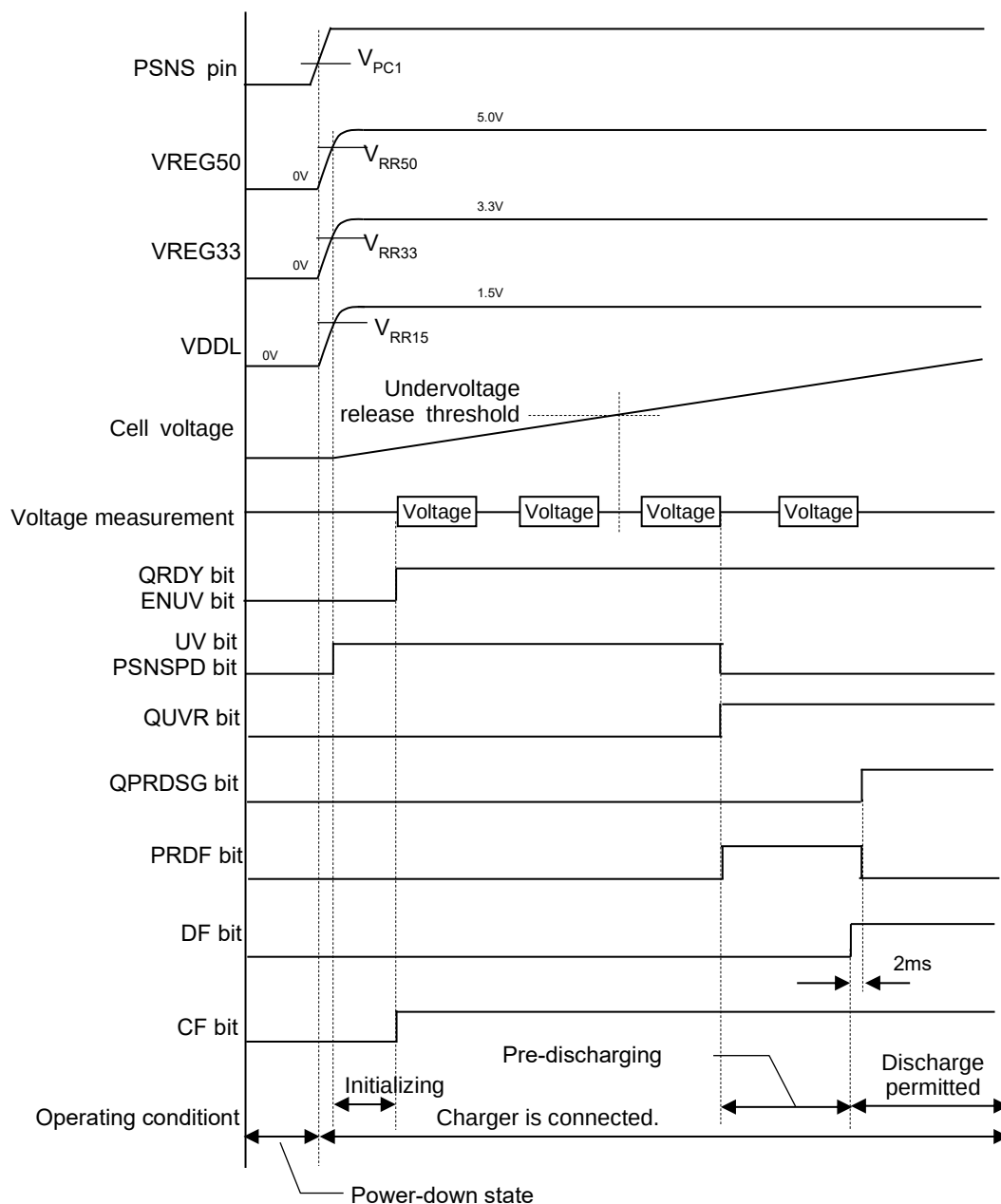


When one or more battery cells become equal to or lower than the undervoltage detection threshold and this condition continues for the undervoltage detection delay time, the LSI enters the undervoltage state. In this state, the UV bit in the STATUS1 register is set to "1", the DF bit in the FETCBAL register is reset to "0", and discharge is prohibited. At the same time, the QUV bit in the INT_REQ1 register is also set to "1", notifying the MCU that undervoltage condition has been detected.

In addition, if the number of cell voltage measurements as the undervoltage detection delay time is three or more, and one or more battery cells are equal to or lower than the undervoltage detection threshold and the undervoltage detection delay time is waiting to elapse, the detection delay time will be reset if the measurement results of all battery cells exceed the undervoltage detection threshold two consecutive times.

When an undervoltage is detected, a 500k Ω (typ.) pull-down resistor is automatically connected to the PSNS pin, and after the delay time set by the PDDL[3:0] bits in the PWRDLY register has elapsed, if the PSNS pin voltage is equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}), the LSI enters the power-down state.

Next is a timing chart of the power-up and undervoltage release operation due to charger connection when the pre-discharge function and FET overheat protection function are disabled. Also, no other abnormalities are detected.



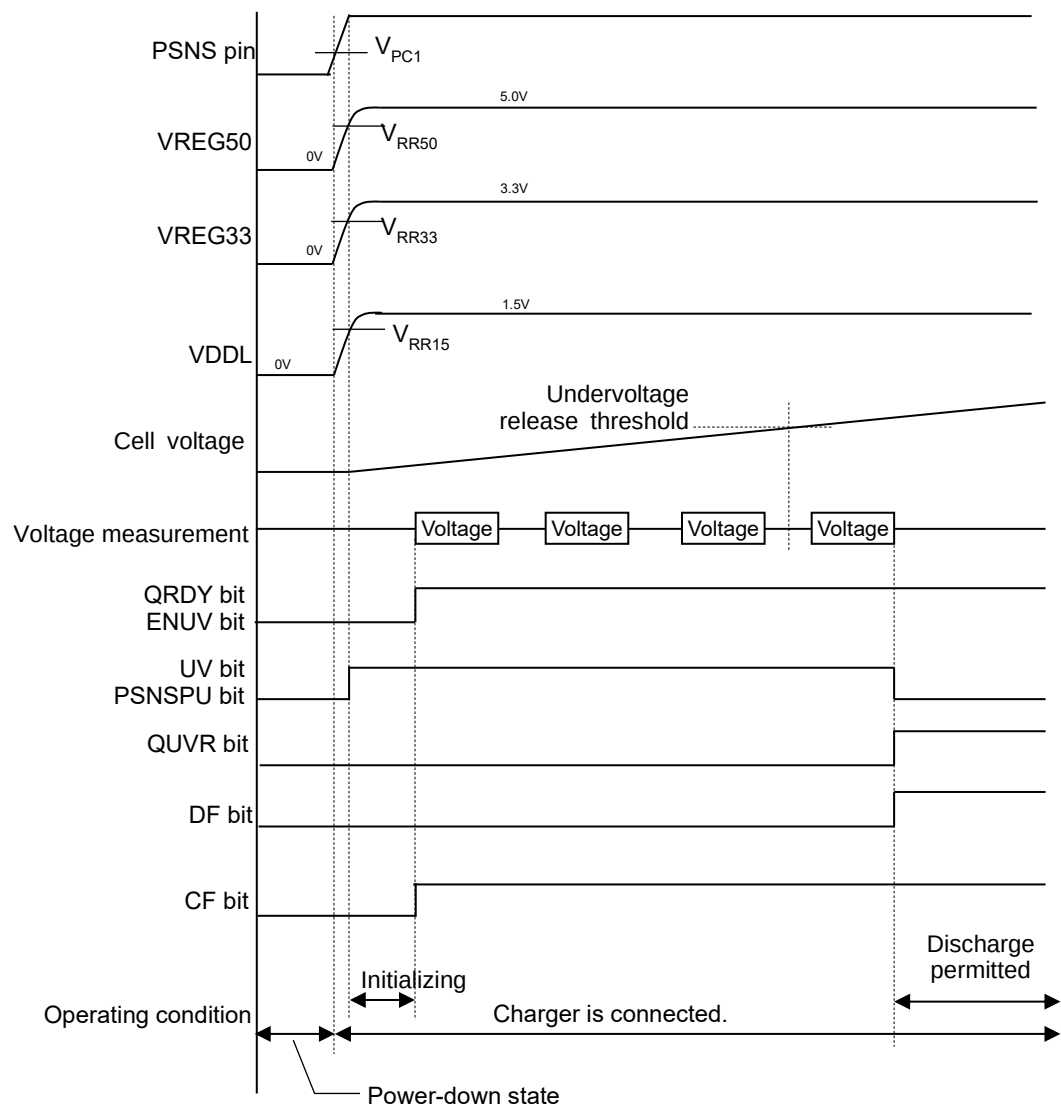
When a charger is connected, the PSNS pin voltage rises, and when it becomes equal to or higher than the charger connection detection PSNS pin voltage (V_{PC1}), the LSI powers up and starts initialization and the initial value stored in the OTP memory is set to each register.

After initialization, voltage measurement starts, and when voltage measurement is completed, the cell voltage measurement result is compared with the undervoltage detection/release threshold. If all cell voltages are equal to or higher than the undervoltage release threshold, the PRDF bit is set to "1". In addition, when the pre-discharge completion condition set in the PREDSG register is satisfied, the DF bit is set to "1", discharge is permitted, and the undervoltage condition is released.

At this time, the QUVR bit in the INT_REQ1 register is set to "1", notifying the MCU that discharge is permitted. After 2ms, the PRDF bit is reset to "0", and the QPRDSG bit is set to "1", notifying the MCU that the pre-discharge is complete.

If the charger is disconnected before the undervoltage detection condition is released, the PSNS pin voltage will drop due to the internal 500kΩ pull-down resistor, and when it falls below the charger connection detection PSNS pin voltage (V_{PC1}), the LSI will enter the power-down state again.

Next is a timing chart of the power-up and undervoltage release operation due to charger connection when the pre-discharge function and FET overheat protection function are disabled. Also, no other abnormalities are detected.



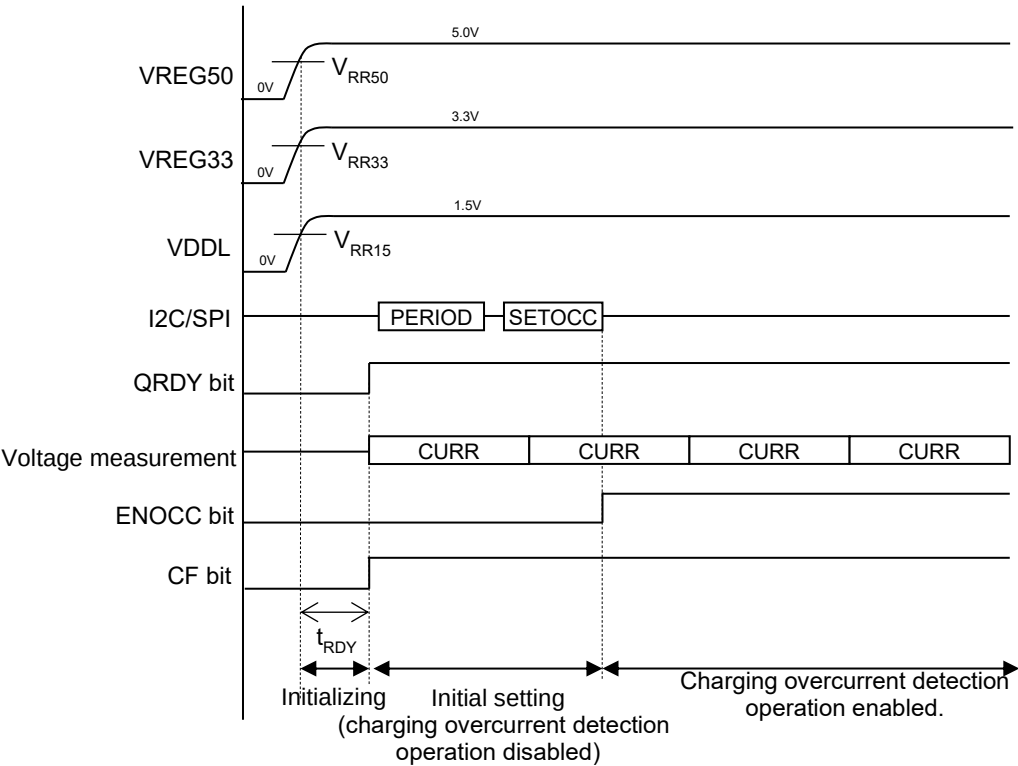
When a charger is connected, the PSNS pin voltage rises, and when it becomes equal to or higher than the charger connection detection PSNS pin voltage (V_{PC1}), the LSI powers up and starts initialization and the initial value stored in the OTP memory is set to each register.

After initialization, voltage measurement starts, and when voltage measurement is completed, the cell voltage measurement result is compared with the undervoltage detection/release threshold. If all cell voltages are equal to or higher than the undervoltage release threshold, the DF bit is set to "1", discharge is permitted, and the undervoltage condition is released.

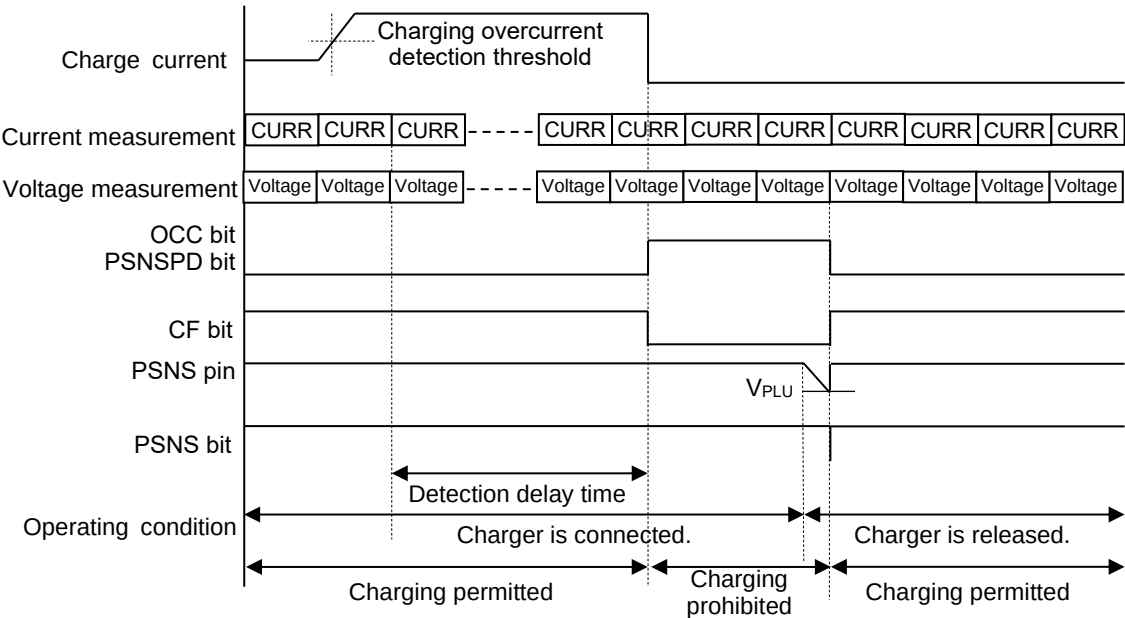
At this time, the QUVR bit in the INT_REQ1 register is set to "1", notifying the MCU that discharge is permitted.

3. Charging Overcurrent Detection Function

When the value of the current measurement result register (G1_CURR or G4_CURR register) becomes equal to or higher than the OCC[3:0] bit value of the charging overcurrent detection operation setting register (SETOCC register), and this condition continues for the time specified by the OCCDLY[3:0] bits in the SETOCC register, the LSI enters the charging overcurrent state. In this state, the CF bit in the FETCBAL register is reset to "0", and charging is prohibited. Below is a timing chart for the initializing operation.



Next is a timing chart for the charging overcurrent detection/release operation.

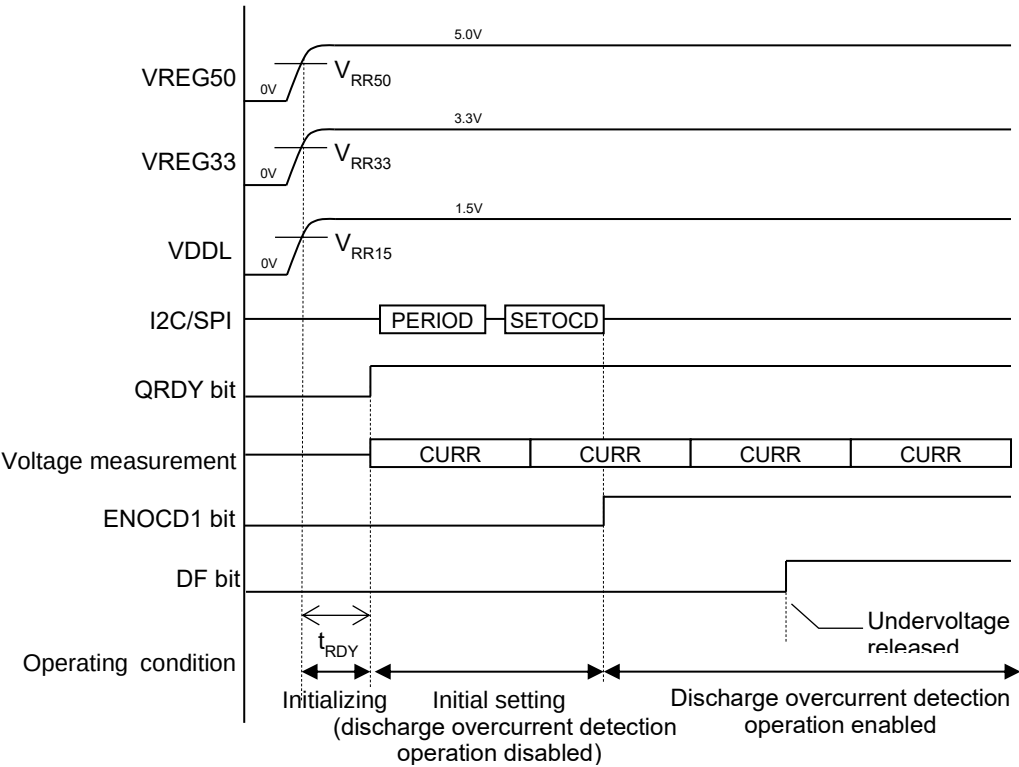


When a charging overcurrent is detected, a 500kΩ (typ.) pull-down resistor is automatically connected to the PSNS pin to detect charger release. When the charger is released, the PSNS pin voltage drops, and when it falls below the charger release detection PSNS pin voltage (V_{PLU}), the charging overcurrent condition is released, and charging is permitted. If the current measurement result register value falls below the charging overcurrent detection threshold two consecutive times, the detection delay time is reset. In addition, after entering the charging overcurrent state, the PSNS bits in the POWER register and STATUS1 register switch their threshold to the charger-disconnection detection voltage V_{PLU} . When the LSI returns from the charging overcurrent state, the threshold switches back to the charger-connection detection voltage V_{PC1} at the PSNS pin.

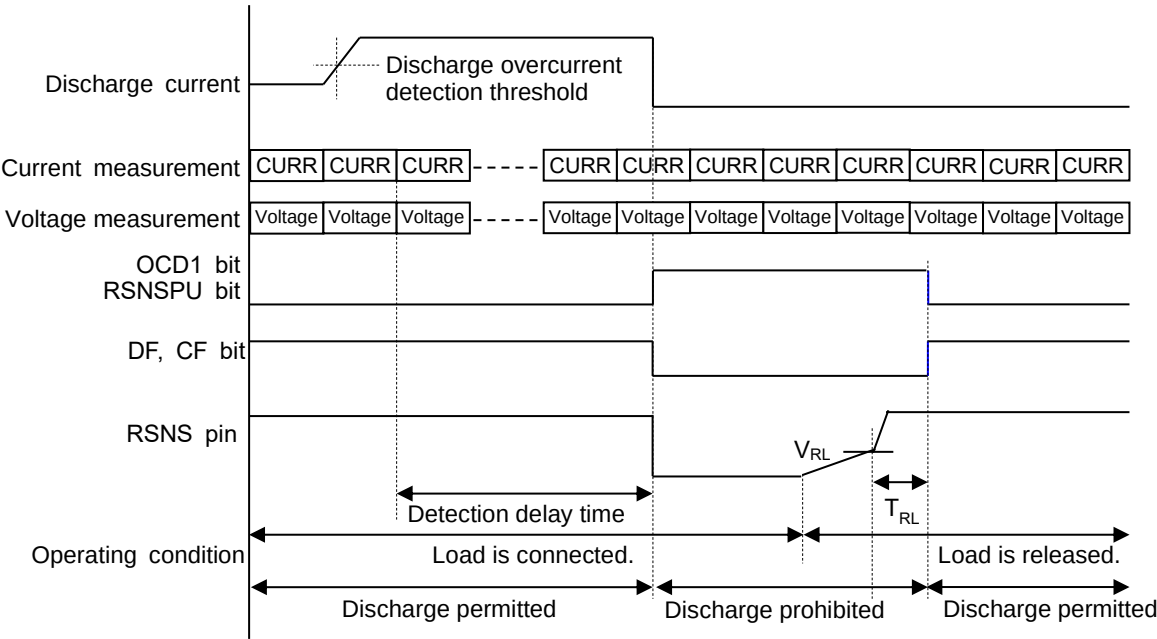
4. Discharge Overcurrent Detection Function

When the value of the current measurement result register becomes equal to or higher than the $OCD1[3:0]$ bit value of the discharge overcurrent detection operation setting register (SET1 register), and this condition continues for the time specified by the $OCDDL1[3:0]$ bits in the SETOCD1 register, the LSI enters the discharge overcurrent state. In this state, the DF bit and the CF bit in the FETCBAL register are reset to “0”, and charging and discharging are prohibited. The SETOCD2 register has the same function.

Below is a timing chart for the initializing operation. It assumes that the pre-discharge function is disabled.



Next is a timing chart for the discharge overcurrent detection/release operation. It also assumes that the pre-discharge function is disabled.



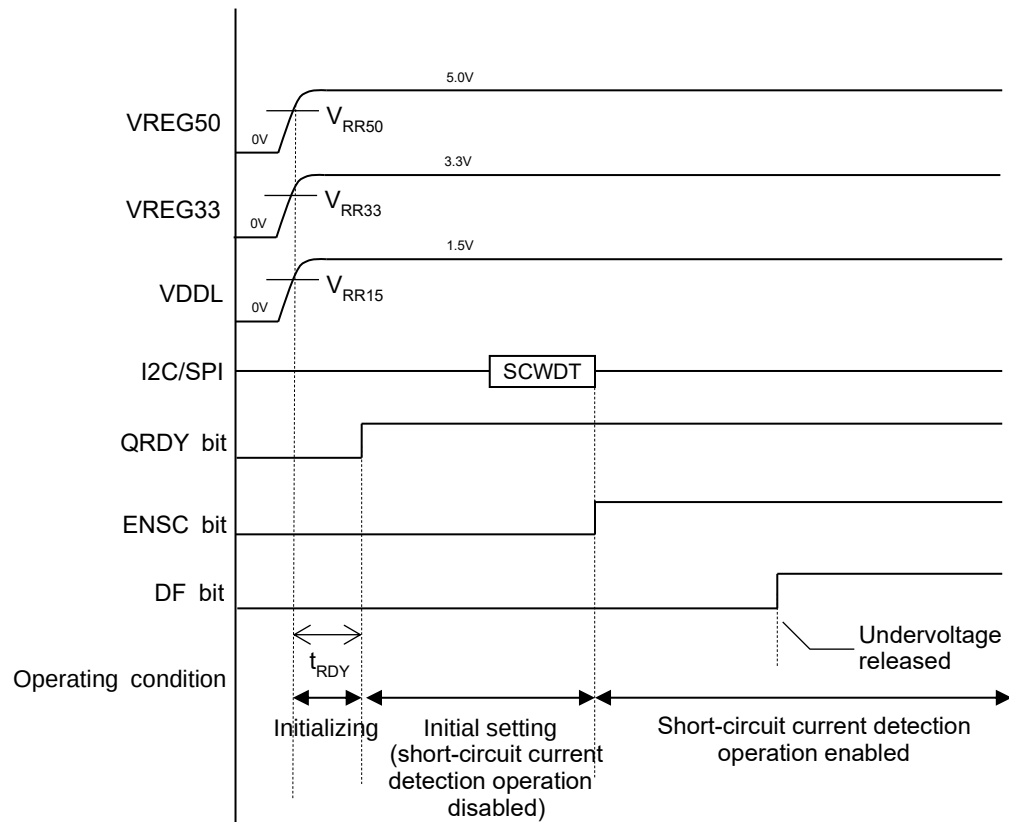
When the LSI enters the discharge overcurrent state, a 2M Ω (typ.) pull-down resistor is automatically connected to the RSNS pin to detect load release. When the load is released, the RSNS pin voltage rises, and when the voltage at the RSNS pin exceeds the load-release detection threshold V_{RL} , and this condition continues for the load-release detection delay time T_{RL} , the discharge overcurrent state is cleared and the LSI returns to the discharge-enabled state.

If the discharge current value of current measurement result register falls below the discharge overcurrent detection threshold two consecutive times, the detection delay time is reset.

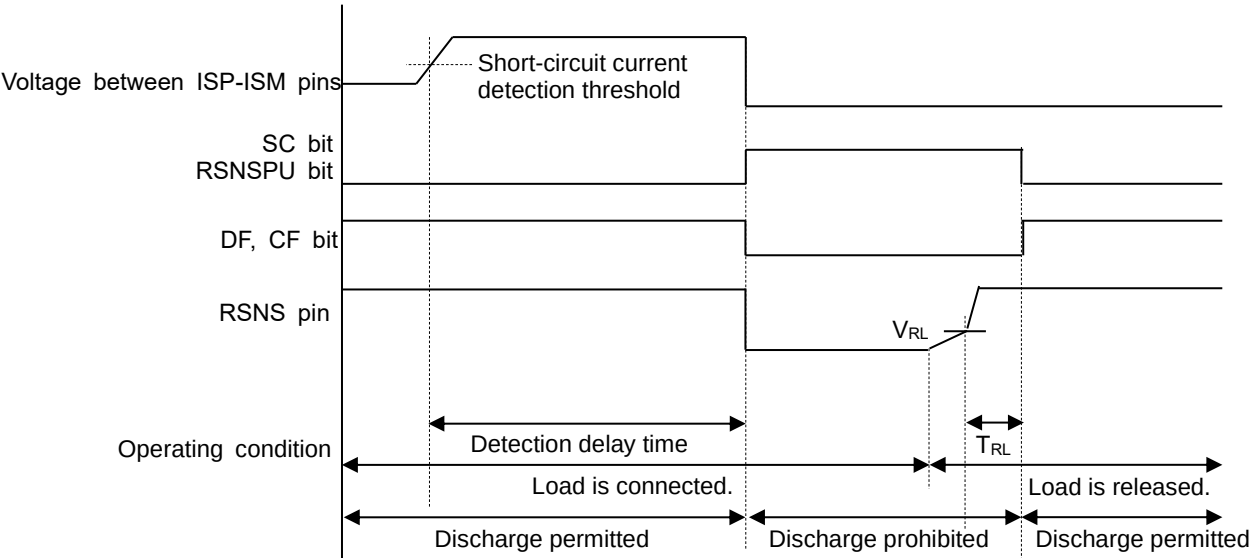
5. Short-circuit Current Detection Function

Short-circuit current detection uses a comparator to compare the voltage between the ISP-ISM pins with the short-circuit current detection threshold voltage specified by the SC[2:0] bits in the SCWDT register. When the voltage between the ISP-ISM pins remains equal to or higher than the short-circuit current detection threshold for the time specified by the TSC[1:0] bits in the SCWDT register, the LSI enters the short-circuit current detection state, and the DF and CF bits in the FETCBAL register are reset to “0”, prohibiting both charging and discharging.

Below is a timing chart for the initializing operation. It assumes that the pre-discharge function is disabled.



Next is a timing chart for the short-circuit current detection/release operation. It also assumes that the pre-discharge function is disabled.

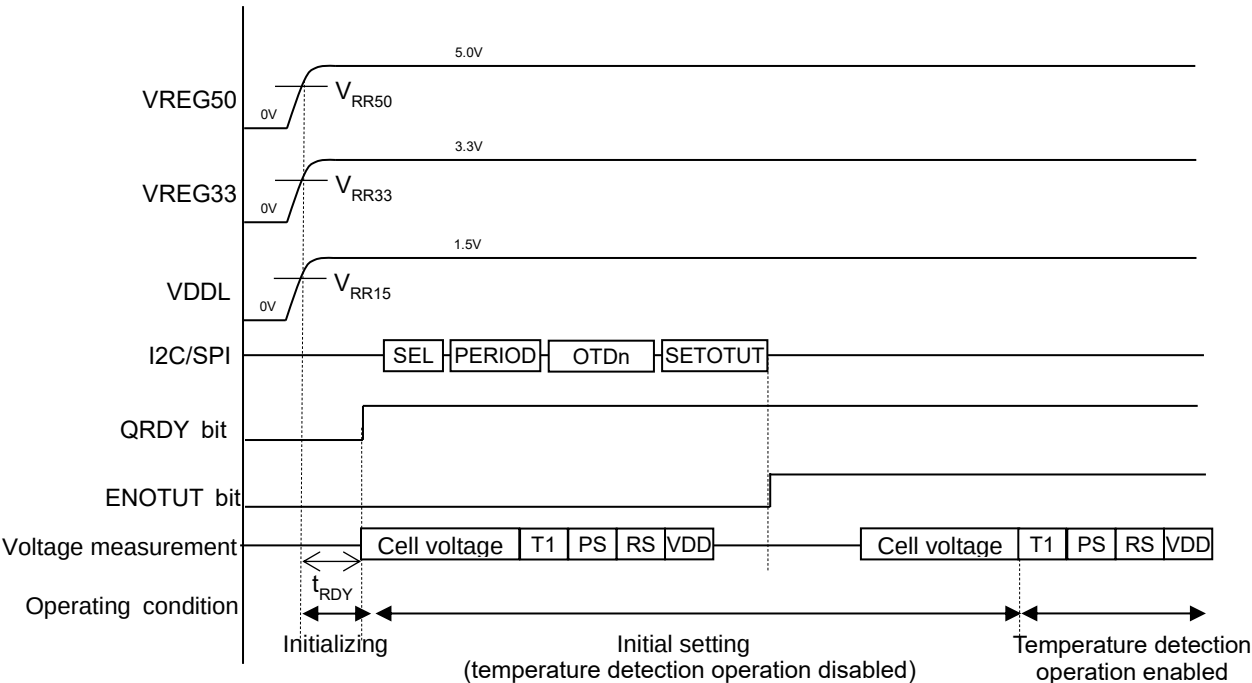


When a short-circuit current is detected, a 2M Ω (typ.) pull-up resistor is automatically connected to the RSNS pin to detect load release. When the load is released, the RSNS pin voltage rises, and when the voltage at the RSNS pin exceeds the load-release detection threshold V_{RL} and this condition continues for the load-release detection delay time T_{RL} , the short-circuit current detection state is cleared, and the LSI returns to the discharge-enabled state. If the voltage between the ISP-ISM pins falls below the short-circuit current detection threshold, the detection delay time is reset.

6. Discharge Prohibition Overtemperature Detection Function

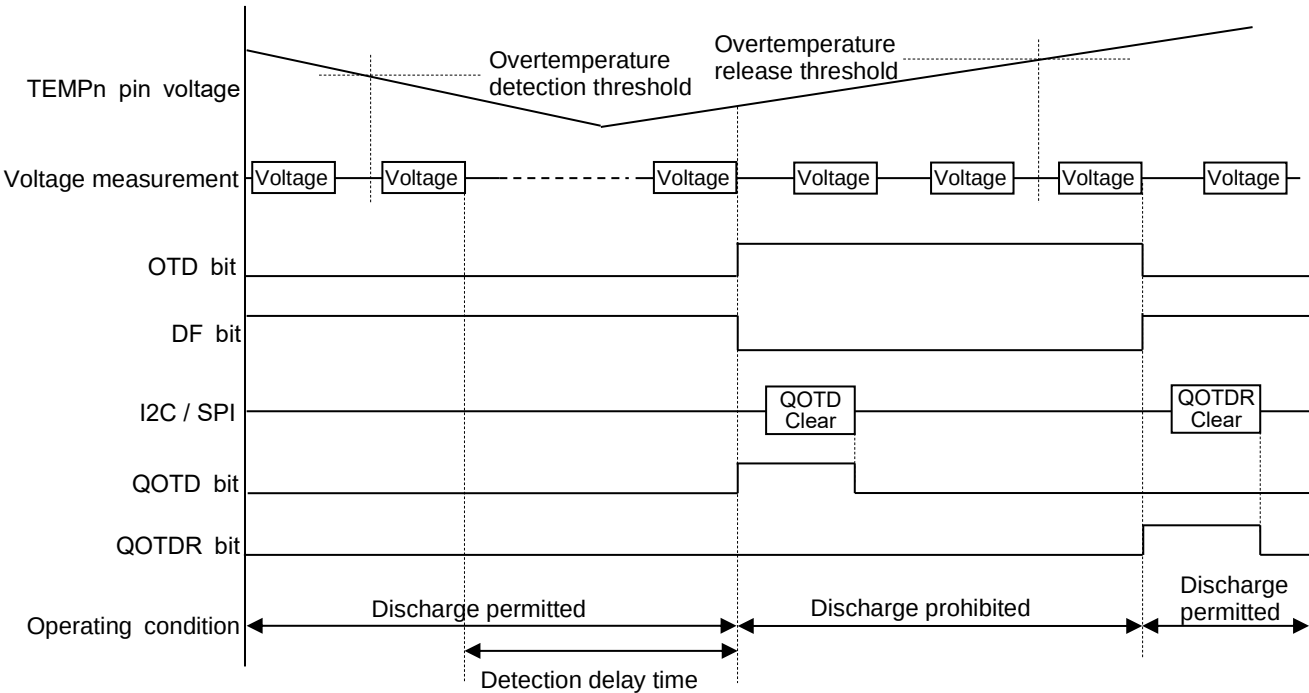
When the value of the temperature measurement result register (TEMPn register) becomes equal to or lower than the OTDn[11:0] bits value of the discharge prohibition high temperature detection threshold register (OTDn register), and this condition continues for the number of temperature monitoring cycles specified by the OTUTDLY1[6:0] bits in the temperature detection operation setting register (SETOTUT register) , the LSI enters the discharge overtemperature detection state. In this state, the DF bit in the FETCBAL register is reset to “0”, and discharge is prohibited.

Below is a timing chart for the initializing operation.



After setting the ENOTUT bit to "1", the temperature detection operation is enabled from the first voltage measurement sequence. When the voltage measurement is completed, the temperature measurement result is compared with the discharge prohibition overtemperature detection threshold.

Next is a timing chart for the discharge prohibition overtemperature detection/release operation. It assumes that no other abnormalities are detected, and the pre-discharge function is disabled.



When the TEMPn pin voltage becomes equal to or lower than the discharge prohibition overtemperature detection threshold and the detection time has elapsed, the discharge prohibition overtemperature is detected and the OTD bit in the STATUS2 register is set to "1" and the DF bit in the FETCBAL register is reset to "0" prohibiting discharge. At the same time, the QOTD bit in the INT_REQ2 register is set to "1", notifying the MCU that a discharge prohibition overtemperature has been detected.

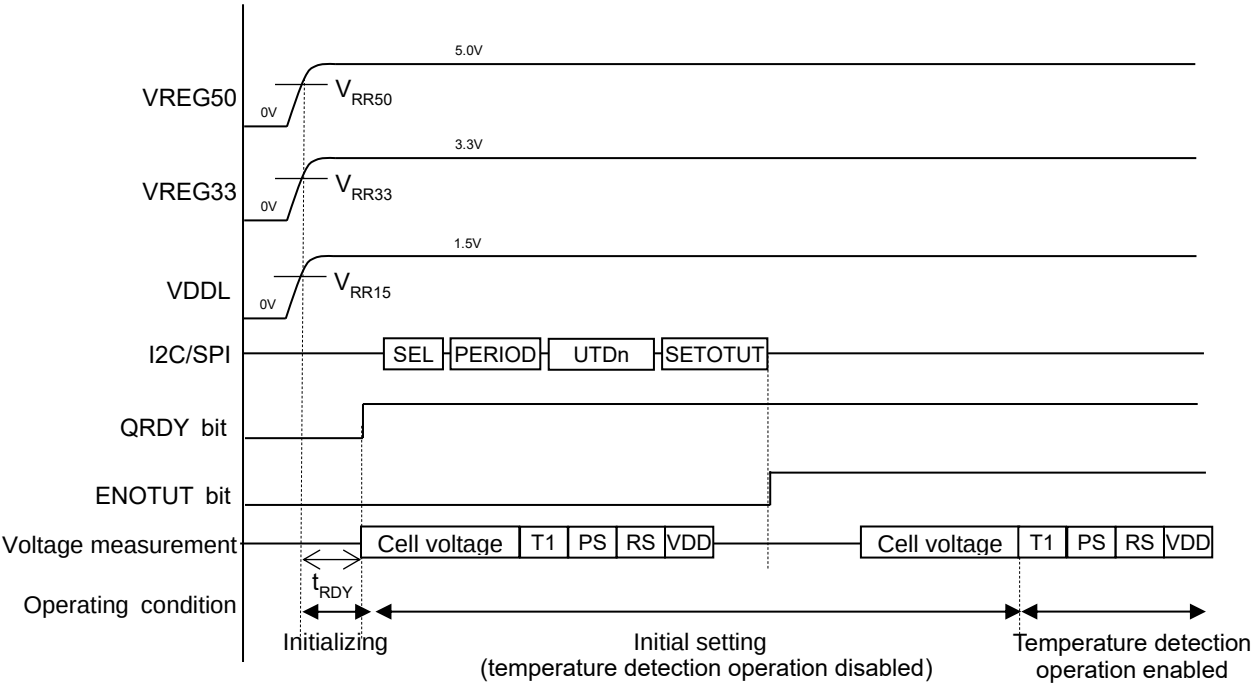
Note that if all of the TEMPn pin voltage measurement results exceed the detection threshold two consecutive times, the detection delay time is reset.

After detecting a discharge prohibition overtemperature, when all of the TEMPn pin measurement results become equal to or higher than the OTDRn[11:0] bits in the discharge prohibition high temperature release threshold register (OTDRn register), the discharge prohibition overtemperature detection condition is released and the OTD bit in the STATUS2 register is reset to "0". In addition, the DF bit in the FETCBAL register is set to "1" permitting discharge. At the same time, the QOTDR bit in the INT_REQ2 register is set to "1", notifying the MCU that a discharge prohibition overtemperature detection condition has been released.

7. Discharge Prohibition Undertemperature Detection Function

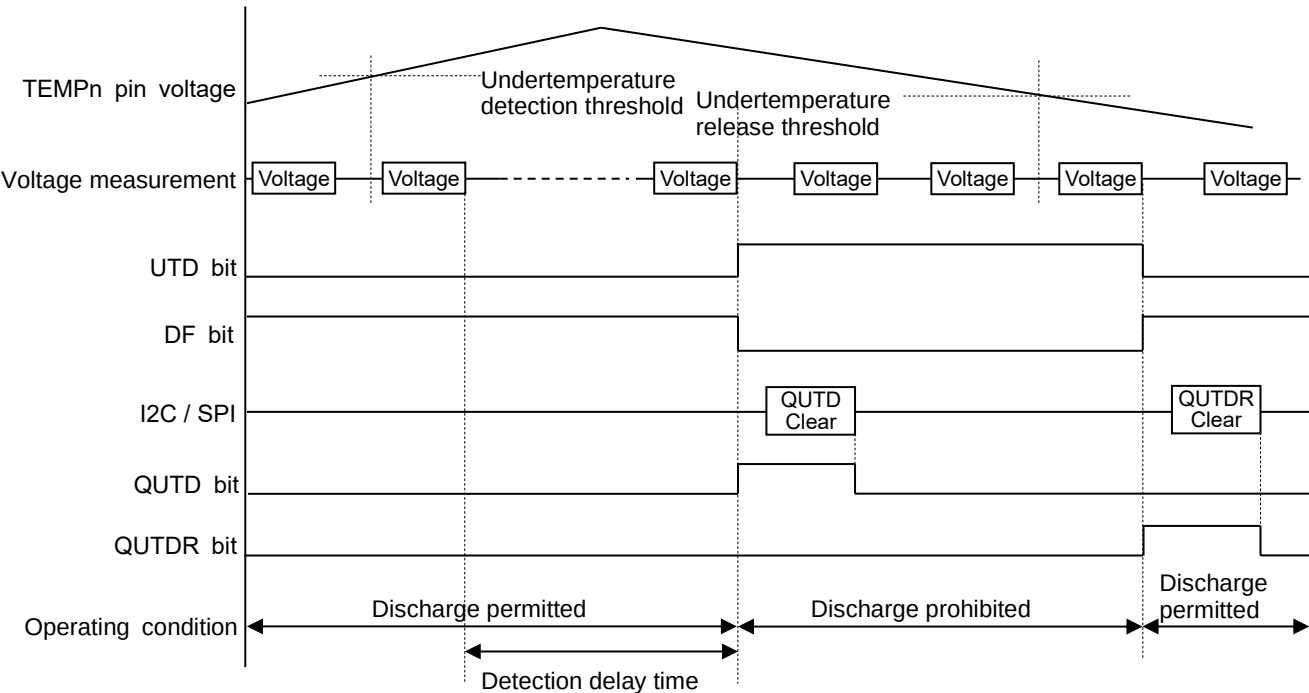
When the value of the temperature measurement result register (TEMPn register) becomes equal to or higher than the UTDn[11:0] bits value of the discharge prohibition undertemperature detection threshold register (UTDn register), and this condition continues for the number of temperature monitoring cycles specified by the OTUTDLY1[6:0] bits in the temperature detection operation setting register (SETOTUT register) , the LSI enters the discharge prohibition undertemperature detection state. In this state, the DF bit in the FETCBAL register is reset to “0”, and discharge is prohibited.

Below is a timing chart for the initializing operation.



After setting the ENOTUT bit to "1", the temperature detection operation is enabled from the first voltage measurement sequence. When the voltage measurement is completed, the temperature measurement result is compared with the discharge prohibition undertemperature detection threshold.

Next is a timing chart for the discharge prohibition undertemperature detection/release operation. It assumes that no other abnormalities are detected and the pre-discharge function is disabled.



When the TEMPn pin voltage becomes equal to or higher than the discharge prohibition undertemperature detection threshold and the detection time has elapsed, the discharge prohibition undertemperature is detected and the UTD bit in the STATUS2 register is set to "1". Also, the DF bit in the FETCBAL register is reset to "0" prohibiting discharge. At the same time, the QUTD bit in the INT_REQ2 register is set to "1", notifying the MCU that a discharge prohibition undertemperature has been detected.

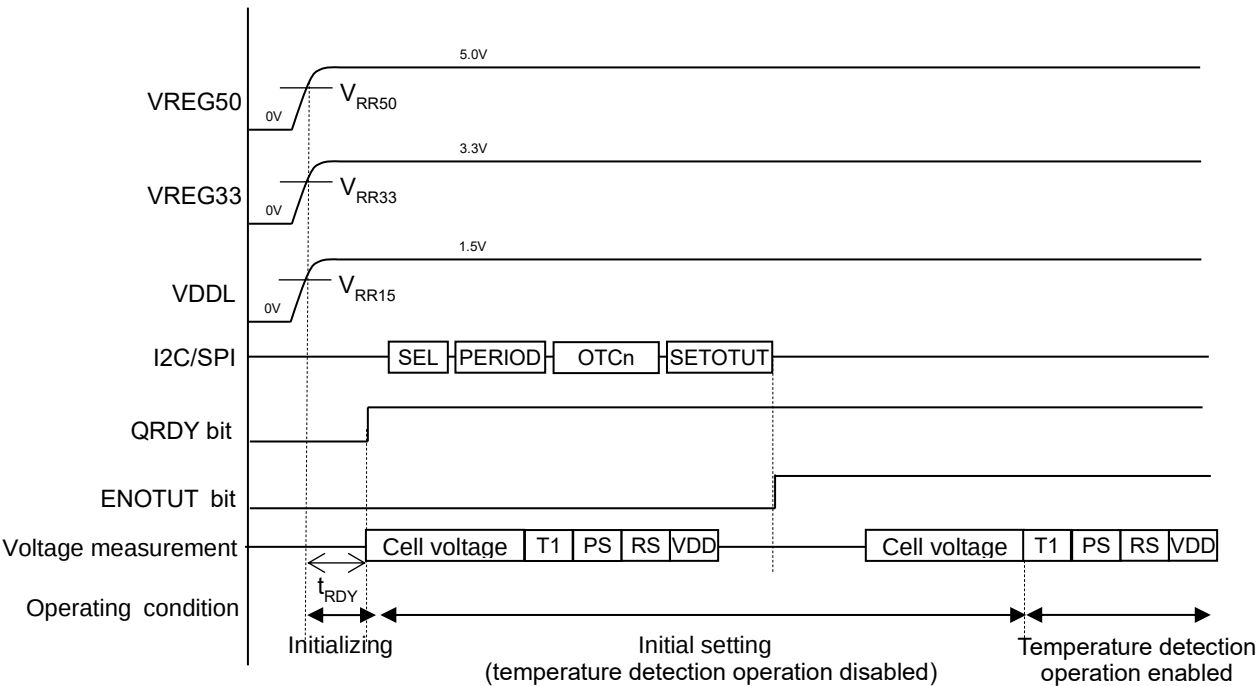
Note that if all of the TEMPn pin voltage measurement results fall below the detection threshold two consecutive times, the detection delay time is reset.

After detecting a discharge prohibition undertemperature, when all of the TEMPn pin measurement results become equal to or lower than the UTDRn[11:0] bits in the discharge prohibition undertemperature release threshold register (UTDRn register), the discharge prohibition undertemperature detection condition is released and the UTD bit in the STATUS2 register is reset to "0". In addition, the DF bit is set to "1" permitting discharge. At the same time, the QUTDR bit in the INT_REQ2 register is set to "1", notifying the MCU that a discharge prohibition undertemperature detection condition has been released.

8. Charging Prohibition Overtemperature Detection Function

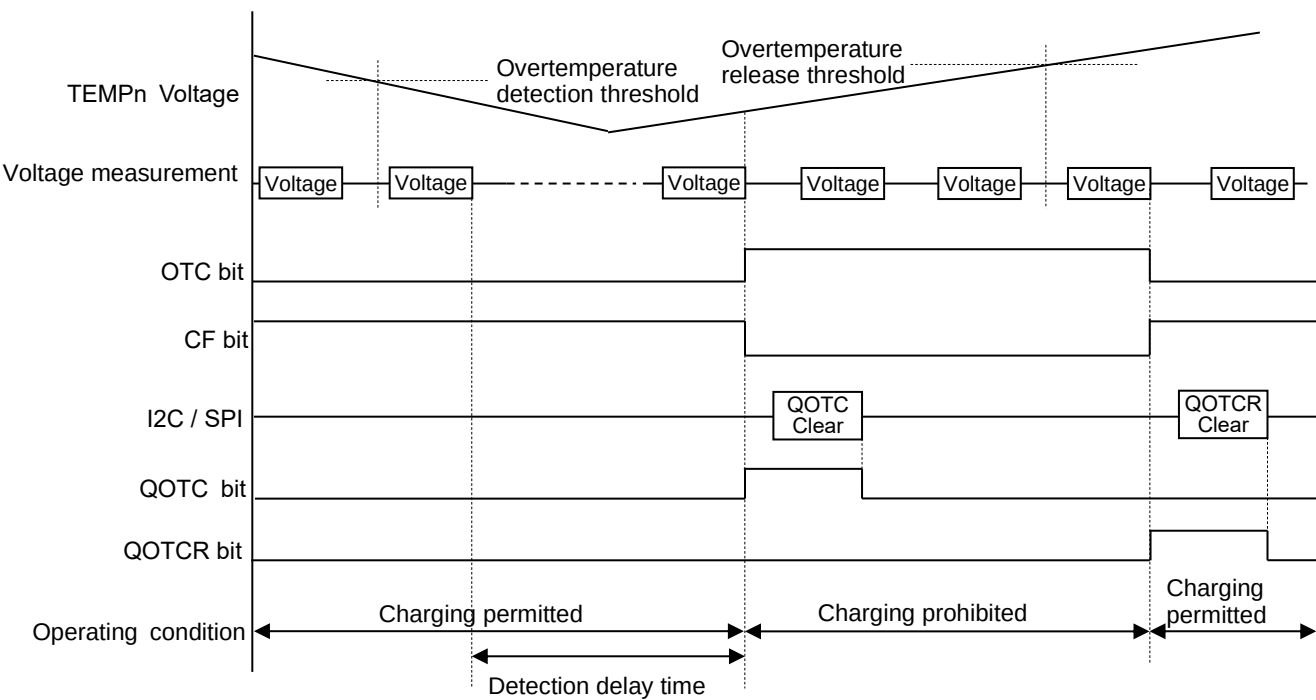
When the value of the temperature measurement result register (TEMPn register) becomes equal to or lower than the OTCn[11:0] bits value of the charging prohibition overtemperature detection threshold register (OTCn register), and this condition continues for the number of temperature monitoring cycles specified by the OTUTDLY[6:0] bits in the temperature detection operation setting register (SETOTUT register), the LSI enters the charging prohibition overtemperature detection state. In this state, the CF bit in the FETCBAL register is reset to “0”, and charging is prohibited.

Below is a timing chart for the initializing operation.



After setting the ENOTUT bit to "1", the temperature detection operation is enabled from the first voltage measurement sequence. When the voltage measurement is completed, the temperature measurement result is compared with the charging prohibition overtemperature detection threshold.

Next is a timing chart for the charging prohibition overtemperature detection/release operation. It assumes that no other abnormalities are detected.



When the TEMPn pin voltage becomes equal to or lower than the charging prohibition overtemperature detection threshold and the detection time has elapsed, the charging prohibition overtemperature is detected and the OTC bit in the STATUS2 register is set to "1". Also, the CF bit in the FETCBAL register is reset to "0" prohibiting charging. At the same time, the QOTC bit in the INT_REQ1 register is set to "1", notifying the MCU that a charging prohibition overtemperature has been detected.

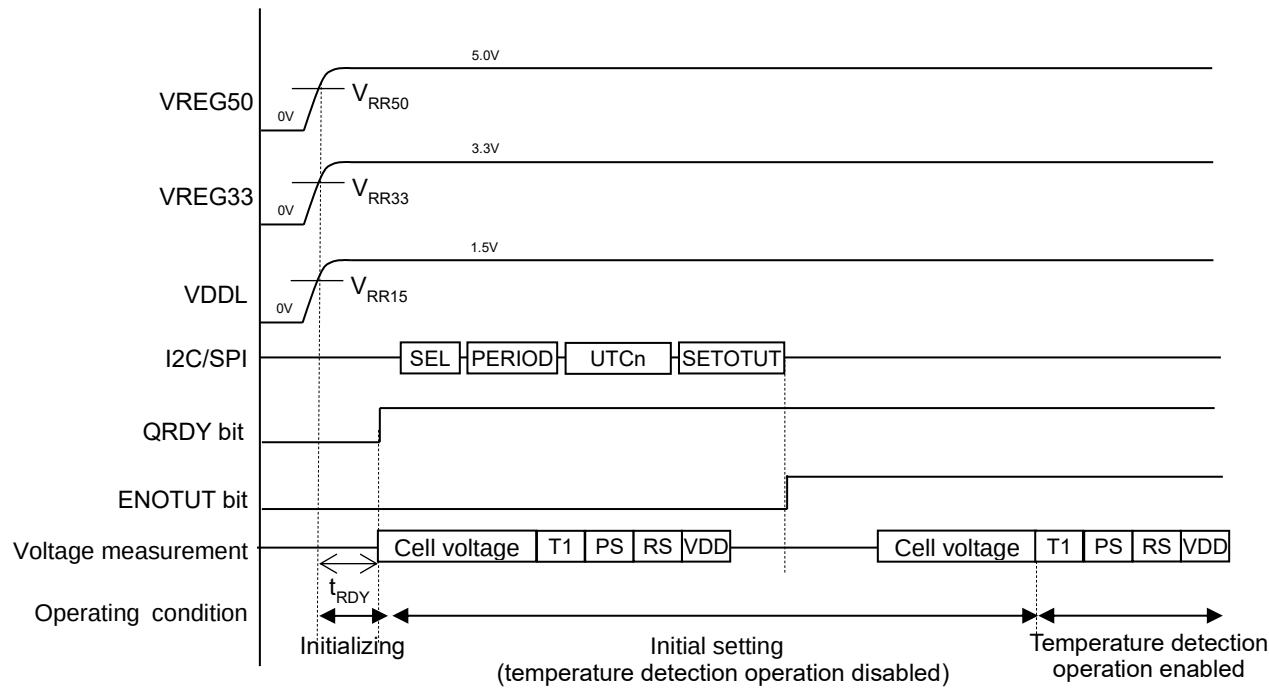
Note that if all of the TEMPn pin voltage measurement results fall below the detection threshold two consecutive times, the detection delay time is reset.

After detecting a charging prohibition overtemperature, when all of the TEMPn pin measurement results become equal to or higher than the OTCRn[11:0] bits in the charging prohibition overtemperature release threshold register (OTCRn register), the charging prohibition overtemperature detection condition is released and the OTC bit in the STATUS2 register is reset to "0". In addition, the CF bit in the FETCBAL register is set to "1" permitting charging. At the same time, the QOTCR bit in the INT_REQ2 register is set to "1", notifying the MCU that a charging prohibition overtemperature detection condition has been released.

9. Charging Prohibition Undertemperature Detection Function

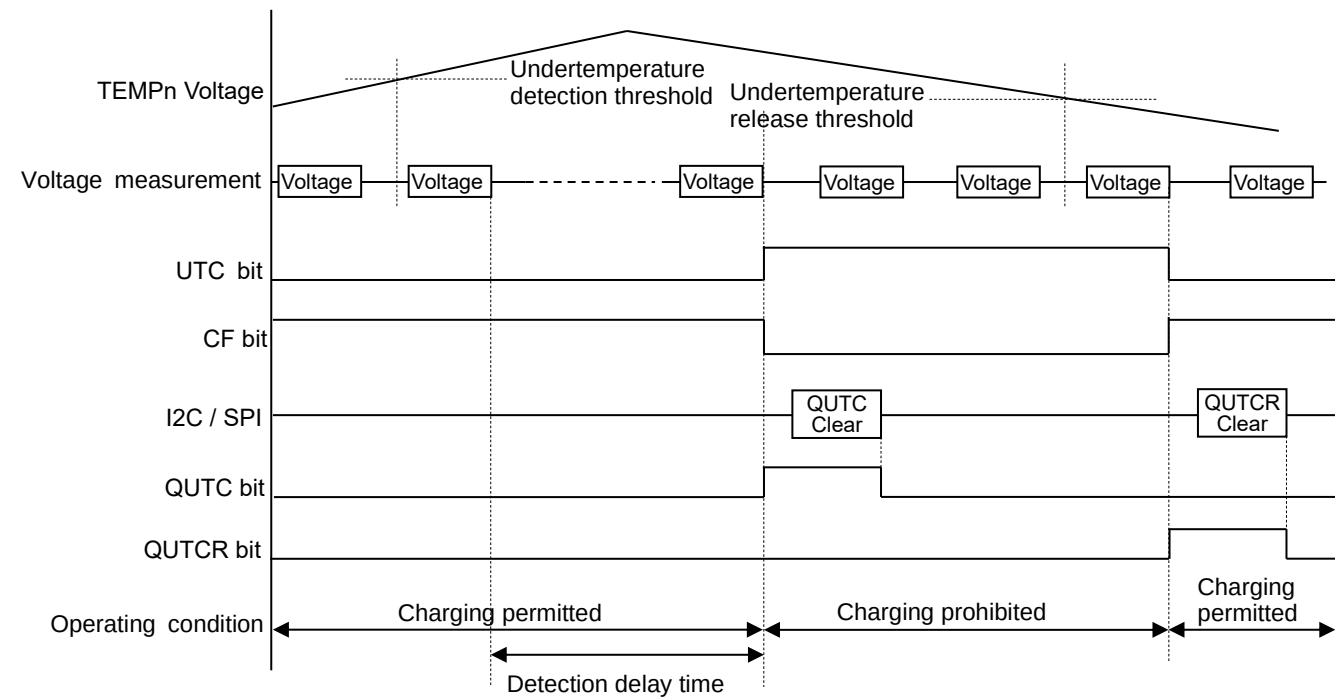
When the value of the temperature measurement result register (TEMPn register) becomes equal to or higher than the UTCn[11:0] bits value of the charging prohibition undertemperature detection threshold register (UTCn register), and this condition continues for the number of temperature monitoring cycles specified by the OTUTDLY[6:0] bits in the temperature detection operation setting register (SETOTUT register), the LSI enters the charging prohibition undertemperature detection state. In this state, the CF bit in the FETCBAL register is reset to “0”, and charging is prohibited.

Below is a timing chart for the initializing operation.



After setting the ENOTUT bit to "1", the temperature detection operation is enabled from the first voltage measurement sequence. When the voltage measurement is completed, the temperature measurement result is compared with the charging prohibition undertemperature detection threshold.

Next is a timing chart for the charging prohibition undertemperature detection/release operation. It assumes that no other abnormalities are detected.



When the TEMPn pin voltage becomes equal to or lower than the charging prohibition undertemperature detection threshold and the detection time has elapsed, the charging prohibition undertemperature is detected and the UTC bit in the STATUS2 register is set to "1". Also, the CF bit in the FETCBAL register is reset to "0" prohibiting charging. At the same time, the QUTC bit in the INT_REQ1 register is set to "1", notifying the MCU that a charging prohibition undertemperature has been detected.

Note that if all of the TEMPn pin voltage measurement results fall below the detection threshold two consecutive times, the detection delay time is reset.

After detecting a charging prohibition undertemperature, when all of the TEMPn pin measurement results become equal to or lower than the UTCRn[11:0] bits in the charging prohibition undertemperature release threshold register (UTCRn register), the charging prohibition undertemperature detection condition is released and the UTC bit in the STATUS2 register is reset to "0". In addition, the CF bit in the FETCBAL register is set to "1" permitting charging. At the same time, the QUTCR bit in the INT_REQ2 register is set to "1", notifying the MCU that a charging prohibition undertemperature detection condition has been released.

10. FET Overheating Protection Function

When one of the charge/discharge control FETs is OFF, the charging or discharge current flows through the body diode of the turned-off FET. If the current is large at this time, the FET will heat up and may be destroyed. Even in the case of overvoltage, undervoltage, overtemperature, or undertemperature detection, if a charging or discharging condition is detected, the charge/discharge control FET is turned on to prevent charging or discharging current from flowing through the FET's body diode.

[a charging condition is detected]

The charging condition detection operation is set by the charging condition detection operation setting register (CHG register). If a charging condition is detected during the undervoltage detection condition, the DF bit in the FETCBAL register is set to "1" and the discharge control FET is turned on. At this time, the undervoltage condition is maintained.

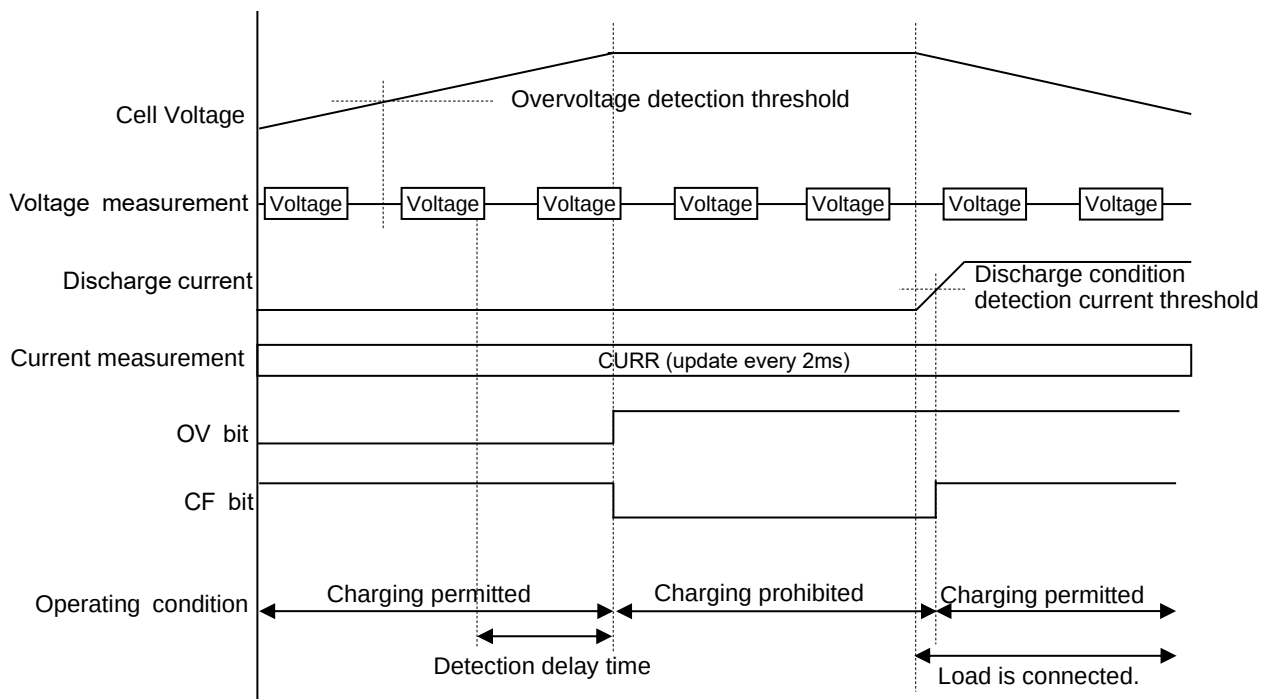
Similarly, if the charging condition is detected during the discharge prohibition overtemperature/undertemperature detection condition, the discharge control FET is turned on and each detection condition is maintained. At this time, the pre-discharge function is disabled.

[a discharge condition is detected]

The discharge condition detection operation is set by the discharge condition detection operation setting register (DSG register). If a discharge condition is detected during the overvoltage detection condition, the CF bit in the FETCBAL register is set to "1" and the charging control FET is turned on. At this time, the overvoltage condition is maintained.

Similarly, if the discharging condition is detected during the charging prohibition overtemperature/undertemperature detection condition, the charging control FET is turned on and each detection condition is maintained.

Below is a timing chart for the discharge condition detected after overvoltage detection.



The same applies when a discharging condition is detected during the charging overcurrent detection condition, and when a charging condition is detected during the discharge overcurrent detection condition, or the short-circuit current detection condition.

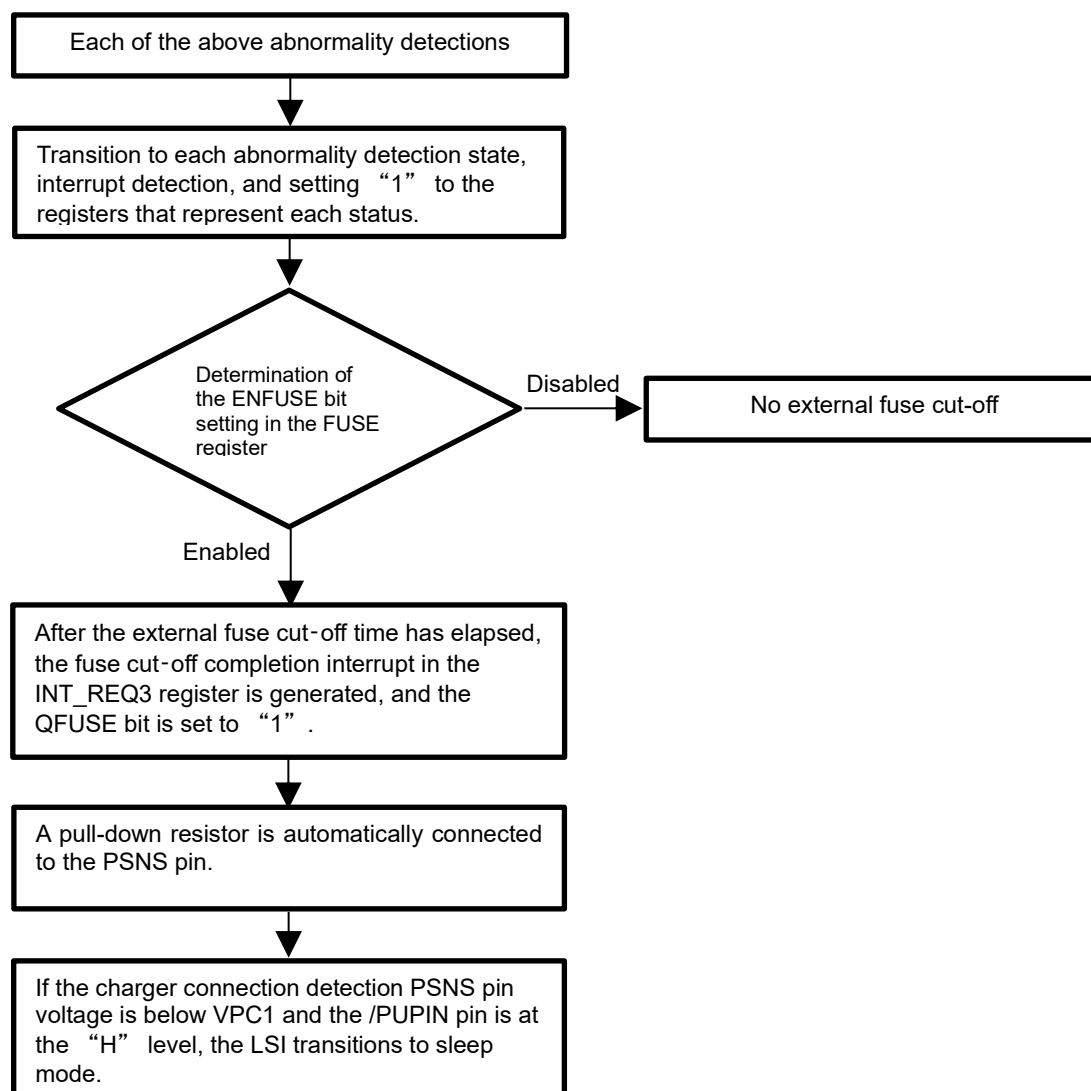
The FET overheating protection is also applied during secondary protection detection conditions.

• Standalone Secondary Protection Function

In addition to the primary protection function, the LSI has secondary protection functions, as shown below. When an abnormality is detected in the secondary protection, an external fuse can be cut off.

1. Secondary overvoltage detection function
2. Secondary undervoltage detection function
3. Secondary charging overcurrent detection function
4. Secondary discharge overcurrent detection function
5. Secondary overtemperature detection function
6. Charging control FET failure detection function
7. Discharge control FET failure detection function
8. External fuse cut-off function

The flowchart below illustrates the internal operation of the ML5262 from secondary protection abnormality detection to the transition to sleep mode after the external fuse is cut-off.



The various standalone secondary protection features are described below.

1. Secondary Overvoltage Detection Function

When the value of the cell voltage measurement result register (VCELLn register) remains equal to or higher than the secondary overcharge detection threshold register (SOVDET register) for the number of cell voltage measurements specified by the SOVDLY[6:0] bits in the SETSOV register, the LSI detects a secondary overvoltage and charging is prohibited.

After configuring the SOVDET register and SOVDLY bit, set the ENSOV bit in the SETSOV register to "1" to enable the secondary overvoltage detection function. When changing the setting, be sure to reset the ENSOV bit to "0" before changing the settings.

The secondary overvoltage detection operation is the same as the primary overvoltage detection operation.

If a secondary overvoltage condition is detected, the SOV bit in the STATUS2 register is set to "1", and the CF bit in the FETCBAL register is unconditionally reset to "0" even when the ENCF bit is "1", prohibiting charging. At the same time, the QSOV bit in the INT_REQ3 register is set to "1", notifying the MCU that a secondary overvoltage has been detected.

The secondary overvoltage condition can be cleared by resetting the ENSOV bit in the SETSOV register to "0".

2. Secondary Undervoltage Detection Function

When the value of the cell voltage measurement result register (VCELLn register) becomes equal to or lower than the secondary overdischarge detection threshold register (SUVDET register) for the number of cell voltage measurements specified by the SUVDLY[6:0] bits in the SETSUV register, the LSI detects a secondary undervoltage and discharging is prohibited.

After configuring the SUVDET register and SUVDLY bit, set the ENSUV bit in the SETSUV register to "1" to enable the secondary undervoltage detection function. When changing the setting, be sure to reset the ENSUV bit to "0" before changing the settings.

The secondary undervoltage detection operation is the same as the primary undervoltage detection operation.

If a secondary undervoltage condition is detected, the SUV bit in the STATUS2 register is set to "1", and the DF bit in the FETCBAL register is unconditionally reset to "0" even when the ENDF bit is "1", prohibiting discharge. At the same time, the QSUV bit in the INT_REQ3 register is set to "1", notifying the MCU that a secondary undervoltage has been detected.

Note that even if a secondary undervoltage condition is detected, the LSI does not transit to the power-down state, and the pull-down resistor is not connected to the PSNS pin.

The secondary undervoltage condition can be cleared by resetting the ENSUV bit in the SETSUV register to "0".

3. Secondary Charging Overcurrent Detection Function

When the value of the current measurement result register becomes equal to or higher than the SOCC[3:0] bit value in the secondary charging overcurrent detection operation setting register (SOCC register) for the time specified by the SOCCDLY[3:0] bit in the SOCC register, the LSI detects a charging overcurrent and the CF bit in the FETCBAL register reset to "0" and charging is prohibited.

The secondary charging overcurrent detection operation is the same as the primary charging overcurrent detection operation.

If a secondary charging overcurrent condition is detected, the SOCC bit in the STATUS2 register is set to "1", and the CF bit in the FETCBAL register is unconditionally reset to "0" even when the ENCF bit is "1", and prohibiting charging. At the same time, the QSOCC bit in the INT_REQ3 register is set to "1", notifying the MCU that a secondary charging overcurrent has been detected.

Note that once a secondary charging overcurrent condition is detected, this condition will be maintained even if the charger is released. The pull-down resistor will not be connected to the PSNS pin.

The secondary charging overcurrent condition can be cleared by resetting the ENSOCC bit in the SOCC register to "0".

4. Secondary Discharge Overcurrent Detection Function

When the value of the current measurement result register becomes equal to or higher than the SOCD[3:0] bit value in the secondary discharging overcurrent detection operation setting register (SOCD register) for the time specified by the SOCDDLY[3:0] bit in the SOCD register, the LSI detects a charging overcurrent and the DF bit in the FETCBAL register reset to "0" and discharging is prohibited.

The secondary discharge overcurrent detection operation is the same as the primary discharge overcurrent detection operation.

If a secondary discharge overcurrent condition is detected, the SOCD bit in the STATUS2 register is set to "1", and the DF bit in the FETCBAL register is unconditionally reset to "0" even when the ENDF bit is "1", and prohibiting discharging. At the same time, the QSOCD bit in the INT_REQ3 register is also set to "1", notifying the MCU that a secondary discharge overcurrent has been detected.

Note that once a secondary discharge overcurrent condition is detected, this condition will be maintained even if the load is released. The pull-up resistor will not be connected to the RSNS pin.

The secondary discharge overcurrent state can be cleared by setting the ENSOCD bit in the SOCD register to "0".

5. Secondary Overtemperature Detection Function

When the value of the temperature measurement result register (TEMPn register) becomes equal to or lower than the SOT[11:0] bit value in the secondary overtemperature detection threshold register (SOT register) for the number of temperature monitoring specified by the SOTDLY[6:0] bits in the secondary overtemperature detection operation setting register (SETSOT register), the LSI detects a secondary overtemperature condition and the CF bit and DF bit in the FETCBAL register reset to "0" and charging and discharging are prohibited.

The secondary overtemperature detection operation is the same as the primary discharge prohibition overtemperature detection operation.

If a secondary overtemperature condition is detected, the SOT bit in the STATUS2 register is set to "1", and the CF bit and DF bit in the FETCBAL register are unconditionally reset to "0" even when the ENCF bit is "1" or the ENDF bit is "1", and prohibiting charging and discharging. At the same time, the QSOT bit in the INT_REQ3 register is also set to "1", notifying the MCU that a secondary overtemperature has been detected.

The secondary overtemperature detection condition can be cleared by setting all of the ENSOT[3:0] bits in the SETSOT register to "0".

6. Charging Control FET Failure Detection Function

When C_FET is off, if a charging current equal to or higher than the SCFET[[3:0] bit value in the SCFET register flows for equal to or longer than the detection delay time specified by the SCFDLY[3:0] bits, the LSI detects a charging control FET failure.

If a charging control FET failure is detected, the QSCFET bit in the INT_REQ3 register and the SCFET bit in the STATUS2 register are set to "1", notifying the MCU that a charging control FET failure has been detected.

The charging control FET failure detection condition can be cleared by setting the ENSCF bit in the SCFET register to "0".

7. Discharge Control FET Failure Detection Function

When PRD_FET and D_FET are off, if a discharge current equal to or higher than the SDFET[3:0] bit value in the SDFET register flows for equal to or longer than the detection delay time specified by the SDFDLY[3:0] bits, the LSI detects a discharge control FET failure.

If a discharge control FET failure is detected, the QSDFET bit in the INT_REQ3 register and the SDFET bit in the STATUS2 register are set to "1", notifying the MCU that a discharge control FET failure has been detected.

The discharge control FET failure detection condition can be cleared by setting the ENSDF bit in the SDFET register to "0".

8. External Fuse Cut-Off Function

This function outputs a signal from the FUSE pin to cut off the external fuse if an abnormality is detected in any of the secondary protection functions.

The secondary abnormality detection condition for cutting off the external fuse and the fuse cut time are selected in the FUSE register.

If the external fuse cut time has elapsed, the QFUSE bit in the INT_REQ3 register and the FUSE bit in the STATUS2 register are set to "1", notifying the MCU that the fuse has been cut off.

In addition, the 500kΩ (typ.) pull-down resistor is automatically connected to the PSNS pin, and if the PSNS pin voltage is equal to or lower than the charger connection detection PSNS pin voltage (V_{PC1}) and the /PUPIN pin is at an "H" level, the LSI will enter the sleep state.

The fuse cut completion detection condition is cleared by resetting the ENFUSE bit in the FUSE register to "0".

For details on waking the LSI from the sleep state, refer to the sleep function description.

• Interrupt Notification Function

An interrupt signal is output from the /INTO pin to notify an external MCU of the completion of various measurements and the occurrence of errors.

The INT_EN1, INT_EN2, and INT_EN3 registers are used to enable various interrupts, and interrupts that have occurred can be confirmed and cleared by reading/writing the INT_REQ1, INT_REQ2, and INT_REQ3 registers.

The table below shows the interrupt sources, conditions for occurrence, and the condition after occurrence. However, this applies to the case of standalone control.

Interrupt source	Interrupt occurrence conditions	Condition after interrupt occurs
Initialization completion QRDY	After power-up, when data loading from the OTP memory to each register is complete.	The contents of the OTP memory are set in each register.
Each voltage measurement completion QVM	When the measurement of cell voltage, current during cell voltage measurement, TEMPn pin, PSNS pin, RSNS pin, and VDD pin voltage is completed.	The measurement results are stored in the VCELLn, G1_ICELLn or G4_ICELLn, TEMPn, PSNS, RSNS, and VDD registers.
Coulomb counter integration completion QCC	When the integration of the current measurement result register value for the period set by the CC[2:0] bits in the PERIOD register is completed.	The accumulated result is stored in the CCL/CCH registers.
Pre-discharge completion QPDSG	When the time set by the TPRDSG[6:0] bits in the PREDSG register has elapsed, or when the voltage difference between the VDD and RSNS pins becomes equal to or lower than the voltage set by the VPRDSG[6:0] bits.	The PRDF bit in the FETCBAL register is reset to "0", and the pre-discharge operation is completed.
Power-save state transition QPSD	When the charging or discharging currents remain below the thresholds set in the CHG and DSG registers for a duration equal to or longer than the time set in the PWRDLY register.	The cell-voltage and temperature measurement intervals change to the power-save period specified in the PERIOD register. Measurements of the PSNS pin voltage, RSNS pin voltage, and VDD pin voltage are not performed.
Return from power-save state QPSR	After any of the following conditions are detected: (1) The charging or discharging currents exceeds the thresholds set in the CHG and DSG registers (2) The abnormal detection delay time measurement has started. Although the results of abnormality detection are reflected in the STATUS register after a delay time has elapsed, the interrupt is generated immediately after the abnormality is detected.	The cell-voltage and temperature measurement intervals change to the normal-mode period specified in the PERIOD register.
Sleep state transition QSLP	When the power-save state continues for a duration equal to or longer than the time set in the PWRDLY register.	All measurement operations are stopped, the LSI enters a low-power consumption state, and only access to the control registers remains enabled.
Return from sleep state QSLPR	After any of the following conditions are detected and a stabilization time of 28 ms has elapsed: (1) The voltage at the PSNS pin becomes equal to or higher than the charger-connection detection PSNS pin voltage (V_{PC1}) while the discharge-control FET is OFF. (2) /PUPIN pin is at the "L" level. (3) When the WKUP bit is "1" and a discharge current is detected	The cell-voltage and temperature measurement intervals change to the normal-mode period specified in the PERIOD register.
Overvoltage detection QOV	When the value of any one of the VCELLn registers remains higher than the OVDET register value for the duration of the detection delay time.	The CF bit in the FETCBAL register is reset to "0", and charging is prohibited.

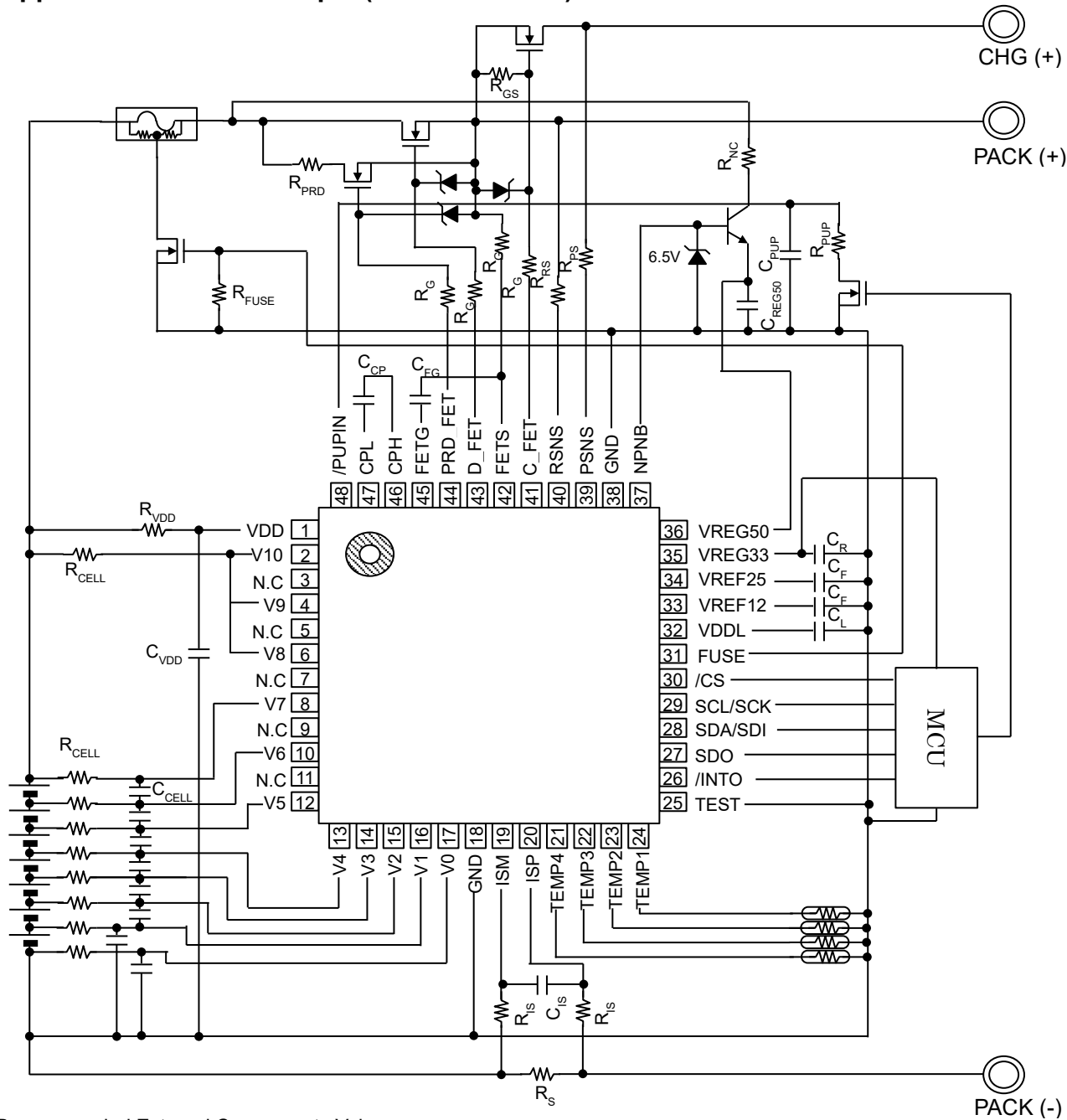
Interrupt source	Interrupt occurrence conditions	Condition after interrupt occurs
Overvoltage release QOVR	When all VCELLn register values become equal to or lower than the value set in the OVRC register.	The CF bit in the FETCBAL register is set to "1", and charging is enabled.
Undervoltage detection QUV	When the value of any one of the VCELLn registers remains equal to or lower than the UVDET register value for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited. When a 500 kΩ pull-down resistor is connected to the PSNS pin and the PSNS pin voltage becomes equal to or lower than the charger - connection detection PSNS pin voltage (V_{PC1}), and the time specified in the PWRDLY register has elapsed, the LSI transitions to the power-down state.
Undervoltage release QUVR	When all VCELLn register values become higher than the value set in the UVRCV register.	When the pre-discharge function is enabled, the PRDF bit in the FETCBAL register is set to "1", and once the pre-discharge completion conditions specified in the PRED SG register are satisfied, the DF bit in the FETCBAL register is set to "1", enabling discharging. When the pre-discharge function is disabled, the DF bit in the FETCBAL register is set to "1", and discharging is enabled.
Charging overcurrent detection QOCC	When the current measurement result register value remains equal to or higher than the value set in the SETOCC register for the duration of the detection delay time.	The CF bit in the FETCBAL register is reset to "0", and charging is prohibited. A 500 kΩ pull-down resistor is connected to the PSNS pin.
Charging overcurrent release QOCCR	When the difference between the VDD pin voltage and the PSNS pin voltage becomes equal to or lower than the charger-disconnection detection voltage (V_{PLU}).	The CF bit in the FETCBAL register is set to "1", and charging is enabled.
Discharge overcurrent 1 detection QOCD1	When the current measurement result register value remains equal to or higher than the value set in the SETOCD1 register for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited. A 2 MΩ pull-up resistor is connected to the RSNS pin.
Discharge overcurrent 1 release QOCDR1	When the RSNS pin voltage becomes equal to or higher than the load-disconnection RSNS pin voltage (V_{RL}).	When the pre-discharge function is enabled, the PRDF bit in the FETCBAL register is set to "1", and once the pre-discharge completion conditions specified in the PRED SG register are satisfied, the DF bit in the FETCBAL register is set to "1", enabling discharging. When the pre-discharge function is disabled, the DF bit in the FETCBAL register is set to "1", and discharging is enabled.
Discharge overcurrent 2 detection QOCD2	When the current measurement result register value remains equal to or higher than the value set in the SETOCD2 register for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited. A 2 MΩ pull-up resistor is connected to the RSNS pin.
Discharge overcurrent 2 release QOCDR2	When the RSNS pin voltage becomes equal to or higher than the load-disconnection detection RSNS pin voltage (V_{RL}).	When the pre-discharge function is enabled, the PRDF bit in the FETCBAL register is set to "1", and once the pre-discharge completion conditions specified in the PRED SG register are satisfied, the DF bit in the FETCBAL register is set to "1", enabling discharging. When the pre-discharge function is disabled, the DF bit in the FETCBAL register is set to "1", and discharging is enabled.

Interrupt source	Interrupt occurrence conditions	Condition after interrupt occurs
Short-circuit current detection QSC	When the voltage between the ISP and ISM pins remains equal to or higher than the value set in the SCWDT register for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited. A 2 MΩ pull-up resistor is connected to the RSNS pin.
Short-circuit current detection release QSCR	When the PSNS pin voltage becomes equal to or higher than the charger-connection detection PSNS pin voltage (V_{PC1}).	When the pre-discharge function is enabled, the PRDF bit in the FETCBAL register is set to "1", and once the pre-discharge completion conditions specified in the PREDSG register are satisfied, the DF bit in the FETCBAL register is set to "1", enabling discharging. When the pre-discharge function is disabled, the DF bit in the FETCBAL register is set to "1", and discharging is enabled.
Charging prohibition overtemperature detection QOTC	When the TEMPn register value remains equal to or lower than the value set in the OTCn register for the duration of the detection delay time.	The CF bit in the FETCBAL register is reset to "0", and charging is prohibited.
Charging prohibition overtemperature detection release QOTCR	When the TEMPn register value becomes equal to or higher than the value set in the OTCRn register.	The CF bit in the FETCBAL register is set to "1", and charging is enabled.
Discharge prohibition overtemperature detection QOTD	When the TEMPn register value remains equal to or lower than the value set in the OTDn register for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited.
Discharge prohibition overtemperature detection release QOTDR	When the TEMPn register value becomes equal to or higher than the value set in the OTDRn register.	When the pre-discharge function is enabled, the PRDF bit in the FETCBAL register is set to "1", and once the pre-discharge completion conditions specified in the PREDSG register are satisfied, the DF bit in the FETCBAL register is set to "1", enabling discharging. When the pre-discharge function is disabled, the DF bit in the FETCBAL register is set to "1", and discharging is enabled.
Charging prohibition undertemperature detection QUTC	When the TEMPn register value remains equal to or higher than the value set in the UTCn register for the duration of the detection delay time.	The CF bit in the FETCBAL register is reset to "0", and charging is prohibited.
Charging prohibition undertemperature detection release QUTCRC	When the TEMPn register value becomes equal to or lower than the value set in the UTCRn register.	The CF bit in the FETCBAL register is set to "1", and charging is enabled.
Discharge prohibition undertemperature detection QUTD	When the TEMPn register value remains equal to or higher than the value set in the UTDn register for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited.
Discharge prohibition undertemperature detection release QUTDR	When the TEMPn register value becomes equal to or lower than the value set in the UTDn register.	When the pre-discharge function is enabled, the PRDF bit in the FETCBAL register is set to "1", and once the pre-discharge completion conditions specified in the PREDSG register are satisfied, the DF bit in the FETCBAL register is set to "1", enabling discharging. When the pre-discharge function is disabled, the DF bit in the FETCBAL register is set to "1", and discharging is enabled.

Interrupt source	Interrupt occurrence conditions	Condition after interrupt occurs
WDT detection QWDT	When no data write or read operation to the control registers is performed for a duration equal to or longer than the overflow time.	In standalone-control mode, no state changes occur. When the ENDF and ENCF bits are set to "1", if an overflow is detected twice consecutively, the DF and CF bits are reset to "0", and charging and discharging are prohibited. When the ENCB bit is set to "1", all CBAL[9:0] bits in the CBAL register are reset to "0", and the cell-balancing operation is stopped.
OTP memory access completion QOTP	When the data-loading operation of the OTP memory is completed.	The contents of the OTP memory are loaded into each register.
CC calibration completion QCCCAL	When the CC calibration operation is completed.	The calibration results are stored in the G1_CC_GAIN and G1_CC_OFST registers, or in the G4_CC_GAIN and G4_CC_OFST registers.
WKUP detection QWKUP	When the voltage between the ISP and ISM pins becomes equal to or higher than the wake-up detection voltage (V_{WK}) and this condition continues for a duration equal to or longer than the wake-up detection delay time (t_{WK}).	The LSI transitions from the sleep state to the normal state.
Secondary overvoltage detection QSOV	When the value of any one of the VCELLn registers remains higher than the SOVDET register value for the duration of the detection delay time.	The CF bit in the FETCBAL register is reset to "0", and charging is prohibited. If the secondary overcharge-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.
Secondary undervoltage detection QSUV	When the value of any one of the VCELLn registers remains equal to or lower than the SUVDET register value for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited. If the secondary overdischarge-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.
Secondary charging overcurrent detection QSOCC	When the current measurement result register value remains equal to or higher than the value set in the SOCC register for the duration of the detection delay time.	The CF bit in the FETCBAL register is reset to "0", and charging is prohibited. If the secondary overcharge-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.
Secondary discharge overcurrent detection QSOCD	When the current measurement result register value remains equal to or higher than the value set in the SOCD register for the duration of the detection delay time.	The DF bit in the FETCBAL register is reset to "0", and discharging is prohibited. If the secondary overdischarge-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.
Secondary overtemperature detection QSOT	When the TEMPn register value remains equal to or lower than the value set in the SOT register for the duration of the detection delay time.	The CF and DF bits in the FETCBAL register are reset to "0", and both charging and discharging are prohibited. If the secondary overtemperature-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.
Charging control FET failure detection QSCFET	When the C_FET is set to OFF and the current measurement result register value remains equal to or higher than the SCFET register value for the duration of the detection delay time.	If the charging-control FET failure-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.
Discharge control FET failure detection QSDFET	When both the PRD_FET and D_FET are set to OFF and the current measurement result register value remains equal to or higher than the SDFET register value for the duration of the detection delay time.	If the discharging-control FET failure-detection state is selected in the FUSE register, an "H" level is output to the FUSE pin.

Interrupt source	Interrupt occurrence conditions	Condition after interrupt occurs
Fuse cut completion QFUSE	When the time set in the FUSE register has elapsed.	The LSI transitions to the sleep state, and a sleep-transition QSLP interrupt is generated.
VREG50 output voltage drop detection QUVLO5	When the VREG50 output voltage drops to a level equal to or lower than the VREG50 drop-detection voltage (VRD50).	No change.
VREG33 output voltage drop detection QUVLO3	When the VREG33 output voltage drops to a level equal to or lower than the VREG33 drop-detection voltage (VRD33).	No change.
Current measurement result Over-Range detection QORG	When the current measurement result is less than 0x8000 or greater than 0x7FFE.	No change.

Application Circuit Example (7 cells connect)



Recommended External Components Values

Component	Recommended value
R _{VDD} (*1)	510Ω~1.5kΩ
C _{VDD}	2.2μF~10μF
R _{CELL}	10Ω~1kΩ
C _{CELL} (*3)	0.1μF~1μF
R _S	0.5mΩ
R _{IS}	1kΩ
C _{IS}	10nF

Component	Recommended value
C _{REG50}	10μF
C _R	4.7μF
C _L	1μF
C _F	3.3μF
C _{FG}	0.47μF (*2)
C _{CP}	20nF (*2)
R _G	100Ω

Component	Recommended value
R _{PRD}	4.7kΩ
R _{PS} , R _{RS}	1kΩ
R _{NC}	10Ω
R _{FUSE}	10kΩ
C _{PUP}	0.1μF
R _{PUP}	100Ω
R _{GS}	1MΩ

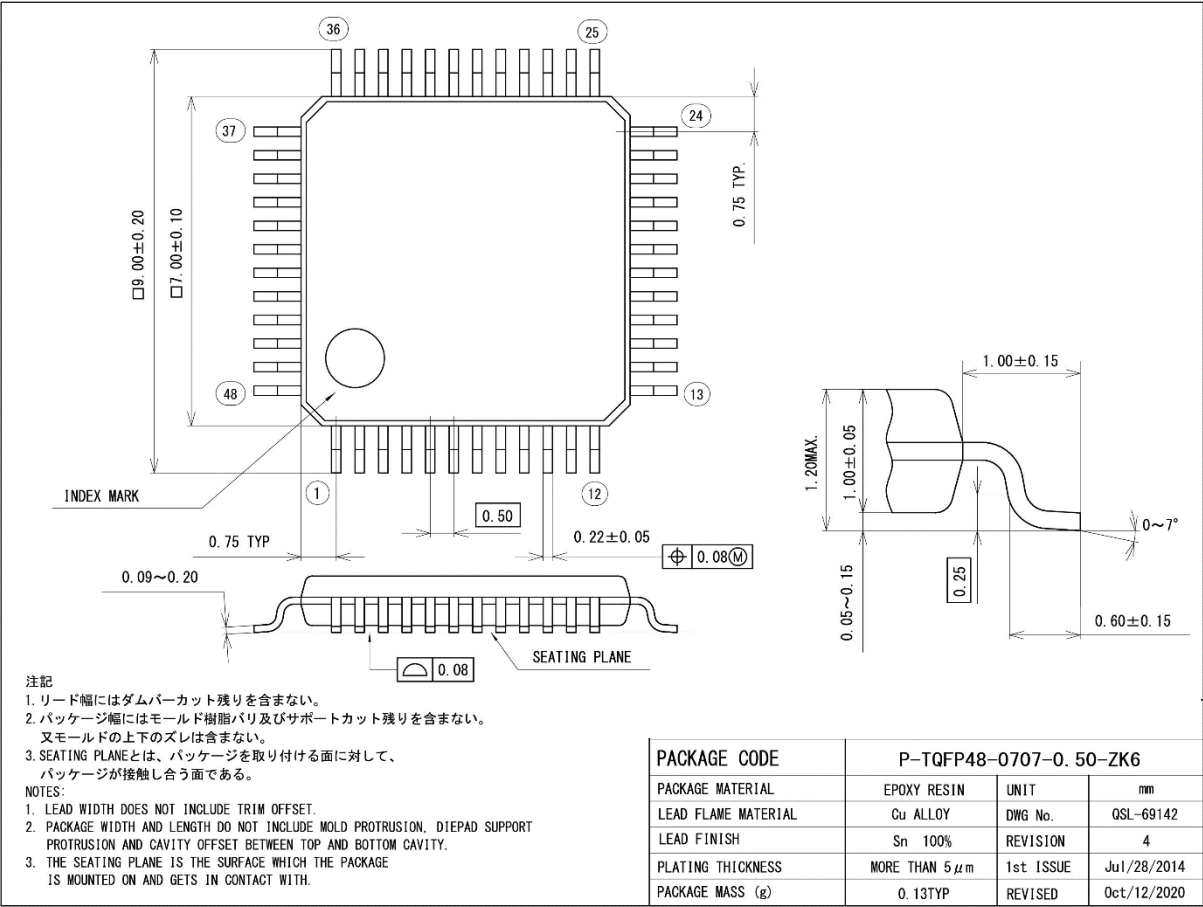
(*1) When R_{VDD} is 1.5kΩ, C_{VDD} is recommended to be 2.2μF. When R_{VDD} is 510Ω, C_{VDD} is recommended to be 4.7μF.

(*2) Adjust it according to the load of the external N-channel FET.

(*3) To prevent the V0 pin connected to the lowest battery cell from falling below the GND level due to a sudden change in cell voltage, the C_{CELL} capacitor of the V1 pin connected to the lowest battery cell should be connected to GND.

* The circuit examples and recommended values for external components do not guarantee operation under all operating conditions, so select the optimum circuit configuration and component values after thorough evaluation in the actual application.

• Package Dimensions



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, when considering reflow mounting, contact a ROHM sales office for the product name, package name, number of pins, package code, and desired mounting conditions (reflow method, temperature, and number of times).

Revision History

Revision	Change	
	Page	Details
2026.05.15 Rev001	-	Initial version
2026.07.30 Rev002	P.1	Add Product name
	P.10	Correction: Cell Voltage Measurement Characteristics condition
	P.34	Typo Correction: ENSLP, SLP bits
	P.42	Typo Correction: UVLO3 bit
	P.47	Typo Correction: OCC bit
	P.64	Typo Correction: SOCC bit
	P.66	Typo Correction: SCFET bit
	P.67	Typo Correction: SDFET bit
	P.77	Typo Correction: RTEMP34
	P.85	Typo Correction: PSNS/ RSNS/ VDD pin voltage measurement
	P.117	Typo Correction: QPSR
	P.118	Typo Correction: QSLP
	P.118	Typo Correction: QOCD2
	P.122	Correction: Application circuit example
	P.125	Notice replacement

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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