Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ML9480

Static, 1/2 Duty, 1/3 Duty, 1/4 Duty 40 Outputs LCD Driver

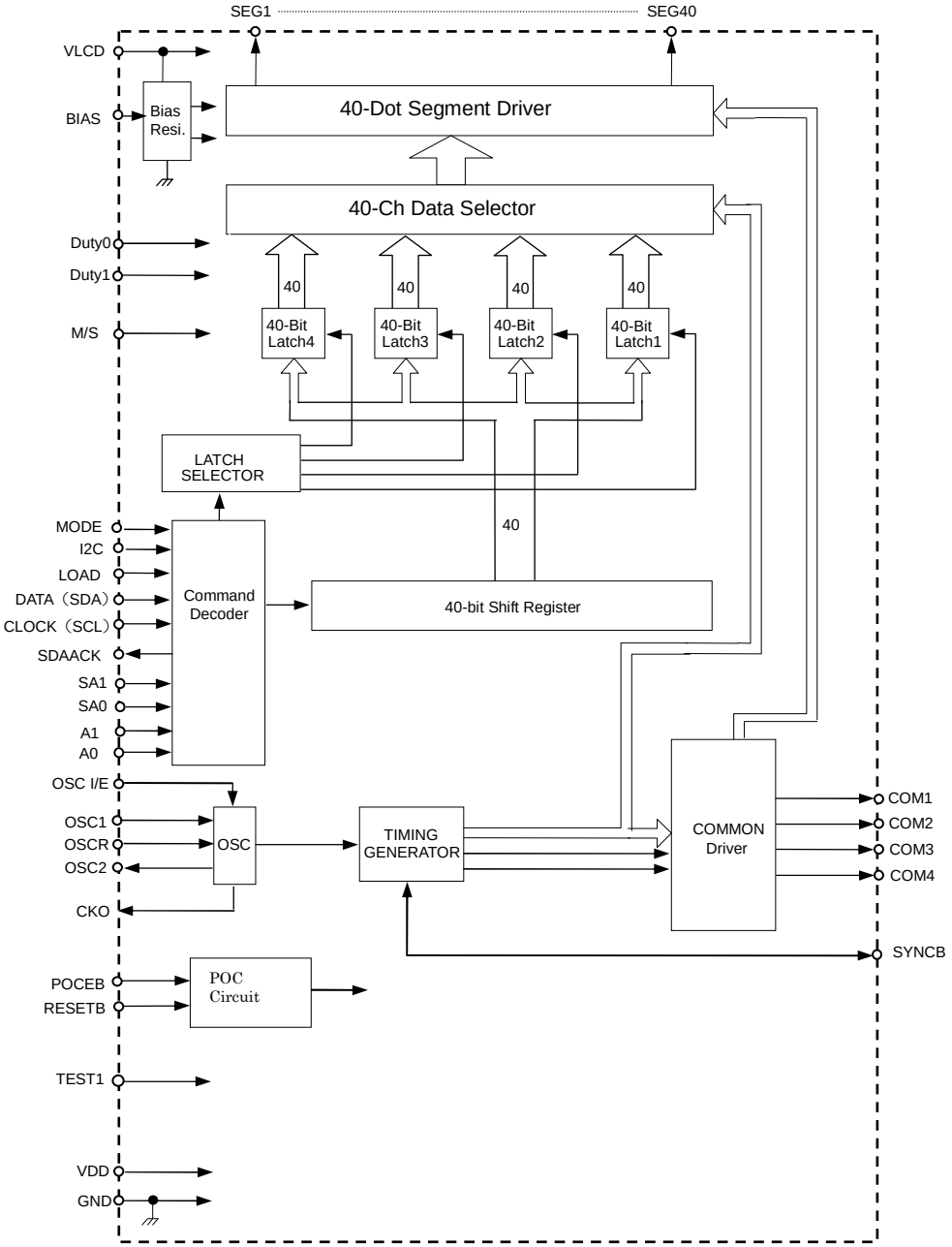
GENERAL DESCRIPTION

The ML9480 is an LCD driver LSI, consists of a 40-bit shift register, a 160-bit data latch, 40 sets of LCD drivers, and a common signal generation circuit.
It can directly drive an LCD up to 40 segments for static display, 80 segments for 1/2-duty display, 120 segments for 1/3-duty display, and 160 segments for 1/4-duty display.
The three-wire serial interface and I^2C interface are selectable.

FEATURES

- Logic power supply voltage : 2.7 to 5.5 V
- LCD drive power supply voltage : 4.5 to 5.5 V
- Maximum number of segments
  Static display : 40 segments
  1/2-duty display : 80 segments
  1/3-duty display : 120 segments
  1/4-duty display : 160 segments
- Interface with microcomputer :
  Serial interface : DATA, CLOCK, LOAD
  CLOCK transfer speed up to 1 MHz
  I^2C interface : SDA, SCL, SDAACK
  SCL transfer speed up to 400 kHz
- Built-in CR oscillator circuit using the internal resistor or External resistor
- Cascade connectable (up to sixteen chips)
- Built-in common signal generation circuit
- Built-in common output intermediate-value voltage generation circuit
- Built-in POC (Power On Clear) circuit
- Gold bump chip (ML9480DVWA)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	Ta = 25°C	-0.3 to 6.0	V
LCD drive power supply voltage	V_{LCD}	Ta = 25°C	-0.3 to 6.0	V
Input voltage	V_I	Ta = 25°C	– 0.3 to V_{DD} + 0.3	V
Output short-circuit current	Is	Ta = 25°C	-2.0 to +2.0	mA
Chip temperature	Tc	—	125	°C
Storage temperature	T_{STG}	—	-55 to +150	°C

Note: Do not use the ML9480 by short-circuiting one output pin to another output pin as well as to other pin (input pin, input/output pin, or power supply pin).

RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}*	—	2.7 to 5.5	V
LCD drive power supply voltage	V_{LCD}*	—	4.5 to 5.5	V
OSC IN clock frequency	f_{CP1}	—	up to 10	kHz
Data clock frequency	f_{CP2}	—	up to 1.0	MHz
SCL clock frequency	f_{SCL}	—	up to 400	kHz
Operating temperature	T_a	—	-40 to +105	°C

Note(*): Use at $V_{DD} \leq V_{LCD}$.

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$f_{FRM} = f_{OSC} /24$

Recommended setting range for external component (oscillator circuit)

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta= –40 to +105°C)

Item	Symbol	Condition	Min	TYP	Max	Unit
Oscillation resistor	R_f	—	423	470	517	kΩ
Frame frequency	f_{FRM}	(F1,F0)=(0,1)	47	75	114	Hz

The relation between oscillation resistor and frame frequency is as the equation below.

$f_{FRM} = f_{OSC} /(16 \times 24)$

fosc = 1 / (Device coefficient x External resistor R_f)

Device coefficient = $73.8 \times 10^{-12} \pm 25\%$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta= -40 to +105°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" input voltage		V_{IH}	—	$0.8V_{DD}$	—	V_{DD}	V	(*1)
"L" input voltage		V_{IL}	—	GND	—	$0.2V_{DD}$	V	(*1)
Input leakage current 1		I_{L1}	$V_I = V_{DD}$ or 0 V	-1.0	—	1.0	μA	(*1)
Input leakage current 2		I_{L2}	$V_I = V_{DD}$ or 0V POCEB="H"	-1.0	—	1.0	μA	RESETB
Pull-up current		I_{pu}	V_{DD} = 5.0V,V_I = 0 V POCEB = "L"	30	—	140	μA	RESETB
"H" output voltage		V_{OH}	I_O = -600uA	$0.9V_{DD}$	—	—	V	CKO, SYNCB
"L" output voltage 1		V_{OL1}	I_O = 600uA	—	—	$0.1V_{DD}$	V	CKO, SYNCB
"L" output voltage 2		V_{OL2}	VDD=5V, V_{OL} = 0.4V	3	—	—	mA	SDAACK
Driver ON resistor	Segment	V_{OHS}	V_{LCD} = 5V	—	5	15	kΩ	SEG1 to SEG40
	Common	V_{OHC}	V_{LCD} = 5V	—	5	12	kΩ	COM 1 to COM4

(*1) : DATA(SDA), CLOCK(SCL), LOAD, M/S, SYNCB, Duty1, Duty0, BIAS, SA1,SA0, A1, A0, OSC1, OSC I/E, I2C, POCEB, MODE

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta= -40 to +105°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Static supply current	I_{DDS}	V_{DD}=V_{LCD}=5.5 V Input pin fixed to "H" or "L" Oscillation stopped, output no-load POCEB="L"		—	8	15	μA	VDD
	I_{LCDS}			—	9	15	μA	VLCD
Dynamic supply current 1	I_{DD1}	V_{DD}=V_{LCD}= 5.5 V (*2)(*3) Clock OSC1 external input f_{CP1}=1.8kHz	(*6)	—	10	18	μA	VDD
	I_{LCD1}		(*7)	—	9	13	μA	VLCD
Dynamic supply current 2	I_{DD2}	V_{DD}=V_{LCD}= 5.5 V (*2)(*3) Internal oscillation	(*6)	—	59	90	μA	VDD
	I_{LCD2}		(*7)	—	9	15	μA	VLCD
Dynamic supply current 3	I_{DD3}	V_{DD}=V_{LCD}= 5.5 V (*2)(*4)(*6) Internal oscillation At three-wire serial IF data input		—	100	200	μA	VDD
	I_{LCD3}			—	9	15	μA	VLCD
Dynamic supply current 4	I_{DD4}	V_{DD}=V_{LCD}= 5.5 V (*2)(*5)(*6) Internal oscillation At I^2C IF data input		—	188	310	μA	VDD
	I_{LCD4}			—	9	15	μA	VLCD

(*2) : M/S = "H", 1/4-duty, 1/3-bias, (F1,F0,FSEL) = (1,1,0) 95 Hz, POCEB = "L", output pin no-load.
(*3) : Three-wire serial or I^2C interface. Input pin fixed to "H" or "L".
(*4) : Serial interface, data input frequency = 1 MHz.
(*5) : I^2C interface, data input frequency = 400 kHz.
(*6) : Alternately inputs "0" and "1" for LCD display data (checkered display).
(*7) : Inputs all "1s" for LCD display data (all illuminated).

Switching Characteristics

- OSC timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
OSC IN clock frequency (external input)	f_{CP1}	Clock input from OSC1. OSC2 and OSCR open. OSC I/E = "L"	—	1.8	10	kHz	OSC1
Clock pulse width (External input)	t_{WCP1}		40	—	—	μs	OSC1
Clock rise and fall time (external input)	t_{OSC}		—	—	(*1)	μs	OSC1
External Rf clock frequency (Internal oscillation)	f_{OSC1}	Between OSC1 and OSC2 R_f = 470kΩ (F1,F0)=(0,1) OSCR open. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSC2
Internal clock frequency (Internal oscillation)	f_{OSC2}	OSC1 open. (F1,F0)=(0,1) OSC2 and OSCR short-circuited. OSC I/E = "H"	18	28.8	44	kHz	OSC1, OSCR, OSC2

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{FRM} = f_{OSC} /24$$

(*1) t_{OSC} is a reference value.
The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value. Make the rise as steep as possible. Reference value: max=2μs.

- Serial interface timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Data clock frequency	f_{CP2}		—	—	1	MHz	CLOCK
Data clock pulse width	t_{WCP2}		100	—	—	ns	CLOCK
Data setup time	t_{SU}		50	—	—	ns	DATA
Data hold time	t_{HD}		50	—	—	ns	CLOCK
CLOCK-LOAD timing	t_{CL}		100	—	—	ns	CLOCK
LOAD-CLOCK timing	t_{LC}		100	—	—	ns	LOAD
LOAD pulse width	t_{WLD}		100	—	—	ns	LOAD
Signal rise and fall time	tsr,tsf		—	—	(*2)	ns	CLOCK,DATA, LOAD

(*2) tsr and tsf shall be reference values.
The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value. Make the rise as steep as possible. Reference value: max=10ns.

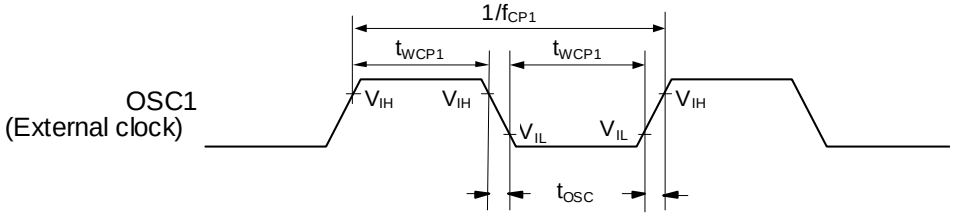
- I^2C interface timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

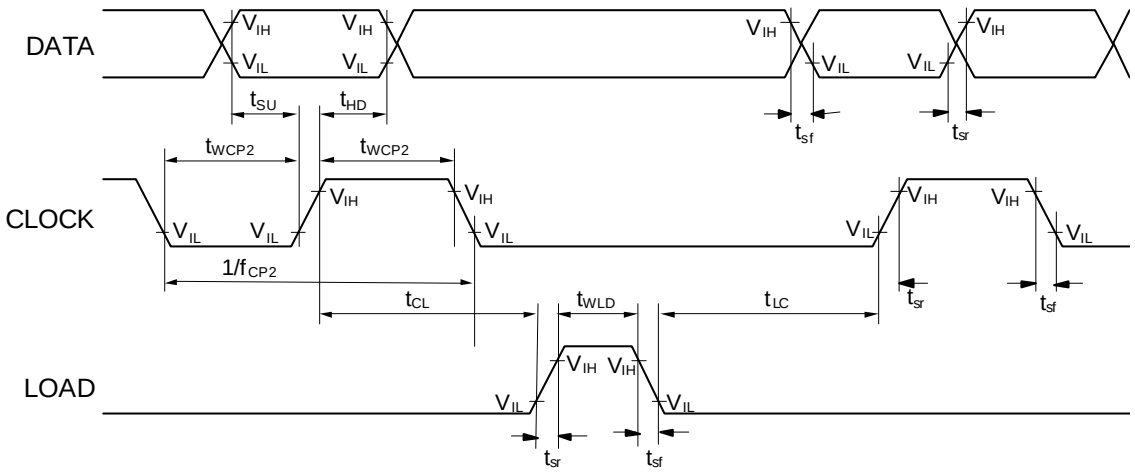
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
SCL clock frequency	f_{SCL}		—	—	400	kHz	SCL
Hold time (repeat) "STATRT" condition	$t_{HD,STA}$		0.6	—	—	μs	SCL,SDA
SCL "L" pulse width	t_{LOW}		1.3	—	—	μs	SCL
SCL "H" pulse width	t_{HIGH}		0.6	—	—	μs	SCL
Setup time for repeat "START" condition	$t_{SU,STA}$		0.6	—	—	μs	SCL,SDA
Data hold time	$t_{HD,DAT}$		0	—	—	ns	SCL,SDA
Data setup time	$t_{SU,DAT}$		100	—	—	ns	SCL,SDA
Setup time for "STOP" condition	$t_{SU,STO}$		0.6	—	—	μs	SCL,SDA
Bus free time between "STOP" condition and "START" condition	t_{BUF}		1.3	—	—	μs	SCL
Data valid acknowledge time	$t_{VD,ACK}$		—	—	1.2	μs	SCL,SDAAACK
Signal rise and fall time	tir,tif		—	—	(*3)	μs	SCL,SDA
Data bus load capacitance	Cb		—	—	400	pF	SDA,SDAACK
Noise pulse width tolerance	t_{wf}		—	—	50	ns	SCL,SDA

(*3) tir and tif shall be reference values.
The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value. Make the rise as steep as possible. Reference value: max=0.1μs.

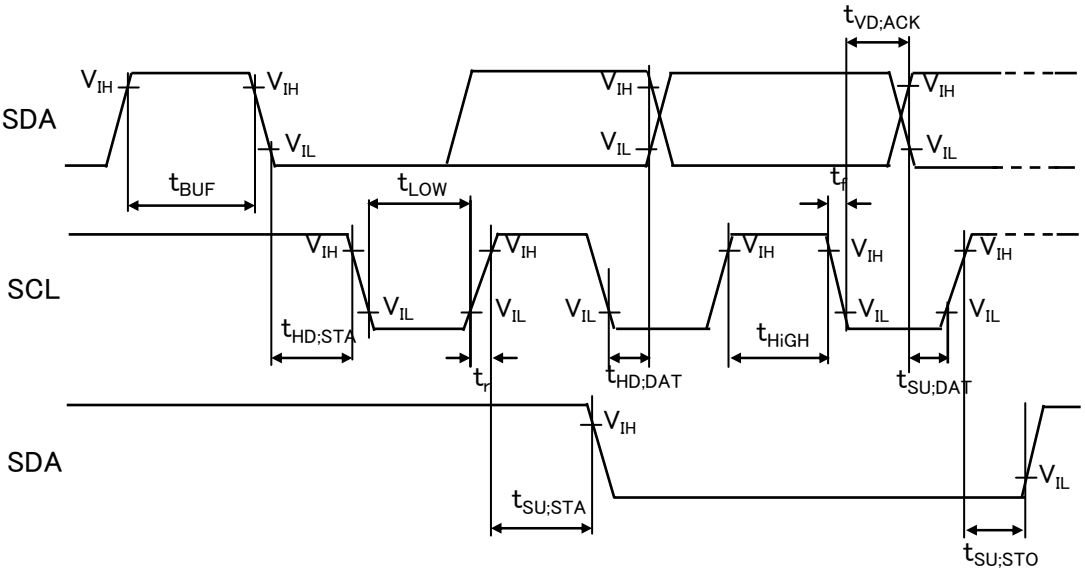
Timing chart (OSC1)



Timing chart (Serial interface)



Timing chart (I^2C interface)



REFERENCE DATA

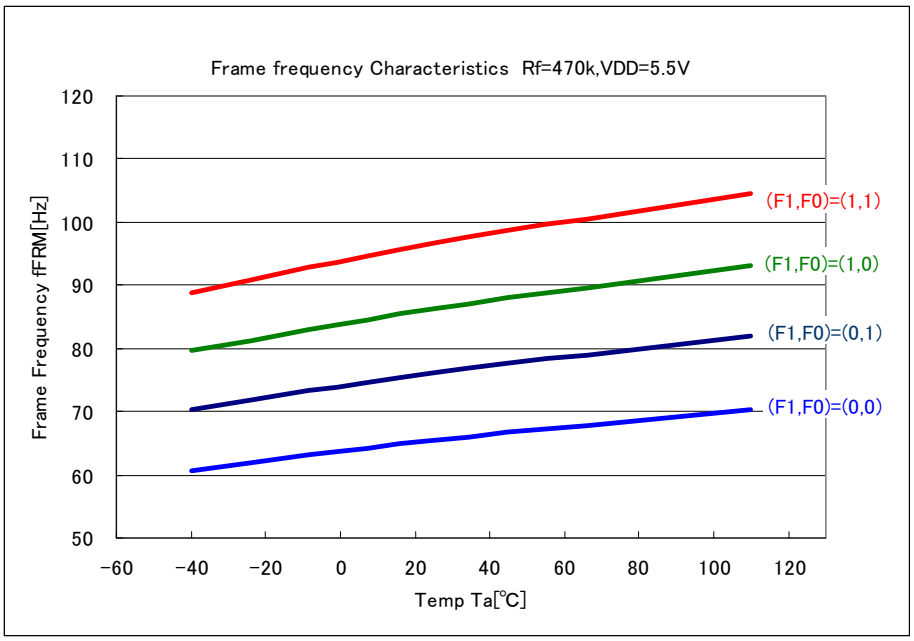
Frame frequency Characteristics

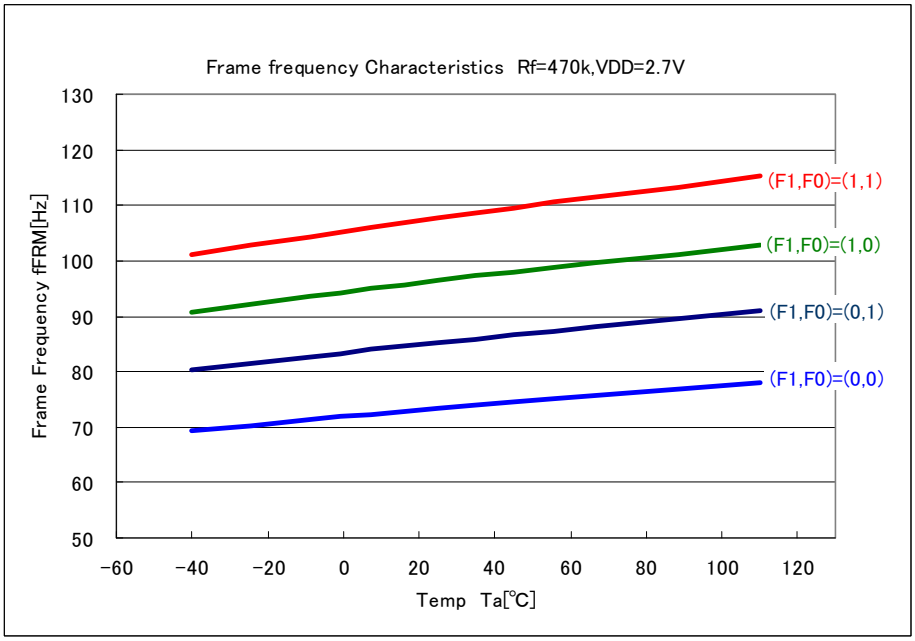
VDD=5.5V/2.7V Rf=470Ω

Frame frequency $f_{FRM} = f_{OSC} /(16 \times 24)$

fosc = 1 / (Device coefficient x External resistor R_f)

Device coefficient = $73.8 \times 10^{-12} \pm 25\%$

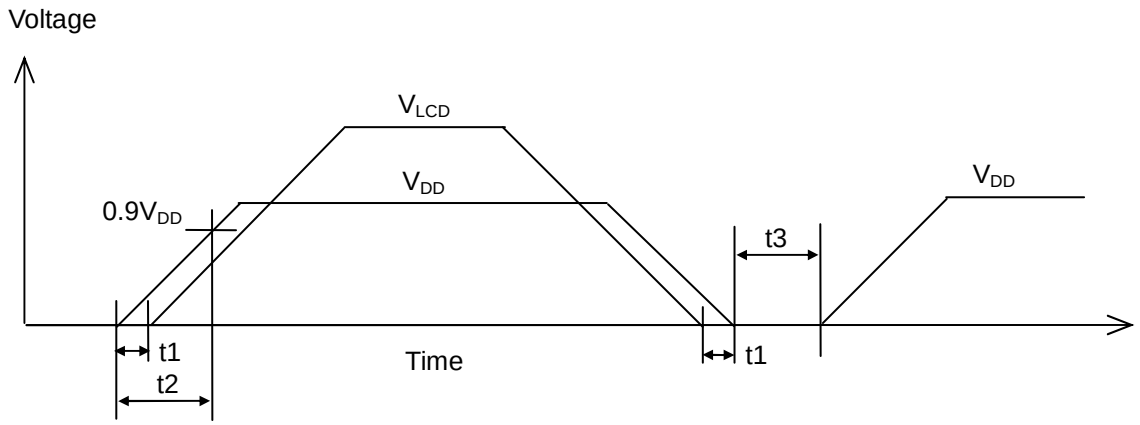




POWER ON/OFF TIMING

To turn on the power supply, raise the logic power supply first, then LCD drive power supply in order to prevent the IC from malfunctioning.
To fall the power supply, fall the LCD drive power supply first, then the logic power supply.
For a VDD pin ranging from 0 V to VDDmin, set VDD ≥ VLCD and t1 ≥ 0 [ns].

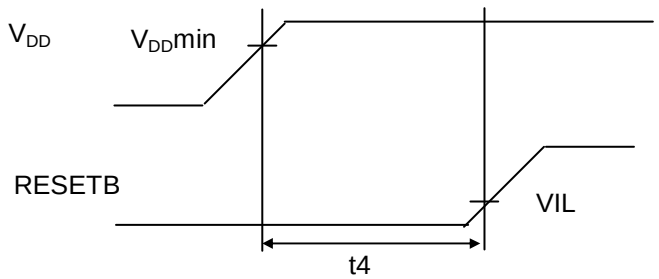
To enable the Internal POC circuit, the VDD power supply rise time t2 range needs to be 100 [µs] ≤ t2 ≤ 500 [ms].
For the VDD power supply to turn OFF then turn ON again, it is necessary to secure the POC discharge time t3 ≥ 100 [ms].



INITIALIZATION SIGNAL TIMING

When RESETB signal is externally input

The RESETB pin input is valid both for POCEB = "L" and "H". Usable in combination with the POC.
Keep the RESETB pin at "L" level until the VDD reaches VDDmin. (t4 ≥ 200[ns])



When Internal POC circuit is used

When using the Internal POC circuit in the initialization, set the POCEB pin to "L".
At this time, the power ON/OFF timing conditions are t1 to t3 above mentioned.

When RESETB pin POC circuit is used

If the power ON/OFF timing conditions t1 to t3 cannot be kept, the RESETB pin needs to have a capacitance to configure the POC circuit. For this case, connect a capacitance value according to the power supply rise time.
For the power supply rise time t2 and external capacitance value, use the following formula as a guide:

$$C_{RST}\ [F] > t2\ [sec] / (30 \times 10^3)$$

PIN DESCRIPTIONS

Pad number	Symbol	I/O	Description
32	M/S	I	This is the input to switch between the master and slave modes. It has a schmitt circuit. When this pin is "H", the mode is master. When this pin is "L", the mode is slave.
3,4	Duty0 Duty1 *1	I	Display duty switch pins. These have schmitt circuits. Duty0="L", Duty1="L" : Static (COM1=COM2=COM3=COM4) Duty0="H", Duty1="L" : 1/2Duty (COM1=COM3, COM2=COM4) Duty0="L", Duty1="H" : 1/3Duty (COM2=COM4) Duty0="H", Duty1="H" : 1/4Duty
35	BIAS	I	This pin sets the LCD bias. It has a schmitt circuit. BIAS="L": 1/3bias BIAS="H": 1/2bias When the static mode selection, fix this pin at “H” or “L” level.
7,8	SA1 SA0	I	Slave address input pins. These have schmitt circuits.
5,6	A1 A0	I	Sub address input pins. These have schmitt circuits.
34	OSC I/E	I	This input selects whether to use the external clock input mode or to use the Internal oscillation mode or external oscillation mode. It has a schmitt circuit. When this pin is "H", the mode is the Internal or external Rf oscillation mode. When this pin is "L", the mode is the external clock input mode. Use the slave chip as it is connected to GND.
24 to 26	OSC1, OSCR, OSC2 *2	I I O	These pins are for the oscillator circuit to generate common signals. The OSC1 and OSCR pins are input pins and have a schmitt circuit. OSC2 is an output pin. It becomes an output when the OSC I/E pin = "H" and a high impedance when the OSC I/E pin = "L". 【In the master mode (M/S pin ="H") 】 Three types are selectable: Internal oscillation mode, external oscillation mode, and external clock input mode. •Internal oscillation mode: Set the OSC I/E pin to "H", short the OSCR and OSC2 pins, and open the OSC1 pin. •External Rf oscillation mode: Set the OSC I/E pin to "H", connect an oscillation resistor Rf between the OSC1 and OSC2 pins, and open the OSCR pin. •External clock input mode: Set the OSC I/E pin to "L", open the OSCR and OSC2 pins, and input the external clock to the OSC1 pin. 【 In the slave mode (M/S pin ="L") 】 Open the OSCR and OSC2 pins and connect the OSC1 pin to the ML9480's CKO pin that has been set to the master mode.
27	CKO	O	Clock output pin. In the master mode (M/S pin = "H", FSEL=”0”), the 1/16 division signal of the oscillation frequency is output. In the master mode (M/S pin = "H", FSEL=”1”), the 1/8 division signal of the oscillation frequency is output. In the slave mode (M/S pin = "L"), the output is fixed to "L". For a cascade connection, connect this pin to the OSC1 pin of the chip that has been set to the slave mode.

28	SYNCB	I/O	Input/output pin for common synchronization. It has a schmitt circuit. It becomes the synchronization signal output pin in the master mode (M/S pin = "H"). It becomes the synchronization signal input pin in the slave mode (M/S pin = "L"). For cascade connection, connect all of the involved ML9480s' SYNC pins by the common line.
30	I2C	I	Interface switching pin. It has a schmitt circuit. When this pin is "H", the interface is I^2C. When this pin is "L", the interface is three-wire serial.
11	DATA (SDA)	I	Display data input pin. It has a schmitt circuit. I2C="L": Serial interface; DATA Input the display data in the order of SEG40, SEG39, ... , SEG2, and SEG1. The display data turns on at "H" and turns off at "L". I2C="H": I^2C interface; SDA Input the display data in units of 8 bits. The display data turns on at "H" and turns off at "L". This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
12	CLOCK (SCL)	I	Shift clock input pin for display data. It has a schmitt circuit. I2C="L": Serial interface; CLOCK The display data input to the DATA pin is serially input to the shift register at the CLOCK signal rise. I2C="H": I^2C interface; SCL The display data input to the SDA pin is serially input to the shift register at the SCL signal rise. This pin has a built-in noise filter through which noises in widths up to 50 ns are removed. This noise filter is valid only when I2C = "H".
13	LOAD	I	Input pin for the load signal of display data. It has a schmitt circuit. I2C="L": Serial interface; LOAD The display data in the shift register is transmitted as is to the segment driver for the "H" duration. When this pin is brought into "L", the shift register is disconnected from the segment driver. The display data in the shift register immediately before it become "L" is held in the data latch and transmitted to the segment driver. I2C="H": I^2C interface Use this pin as it is connected to GND.
10	SDAACK	O	I2C="L": Serial interface Use this pin as it is opened. I2C="H": I^2C interface The I^2C bus acknowledge output signal. Normally, use it as it is connected with the SDA pin. Connect an external pull-up resistor whenever necessary, as it is an open drain pin. The pull-up connection destination supply voltage shall be the V_{DD} supply voltage or less.
33	POCEB	I	Internal POC circuit enable pin. It has a schmitt circuit. When this pin is "H", the POC circuit becomes OFF and the constant current (8µA) is cut. The RESETB pin pull-up resistor is cut as well. When this pin is "L", the POC circuit becomes ON. The RESETB pin is connected to a pull-up resistor.
23	RESETB *3	I	Reset signal input pin for initializing inside the IC. It has a schmitt circuit. The "L" level enables the reset. This pin has an Internal pull-up resistor. Open when POCEB = "H". Pull-up when POCEB = "L". The power-on reset operation is available by connecting an external capacitor.

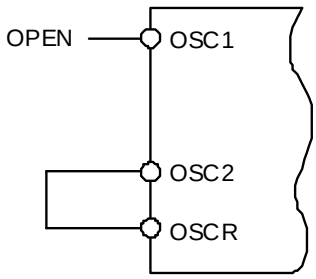
31	MODE	I	I2C interface command table switching pin. It has a schmitt circuit. This pin is valid only when I2C = "H". When this pin is "L", the command table is table A. When this pin is "H", the command table is table B. When the three-wire serial interface mode selection, fix this pin at “H” or “L” level.
36	TEST1	I	Pin for testing the IC. It has a Internal pull-down resistor. Use it as it is connected to GND.
45 to 64, 69 to 88	SEG1 ~SEG40	O	Outputs for LCD display. Connected to the segment pins on the LCD panel. In the display off mode, all the outputs are fixed to GND.
40 to 43, 65 to 68, 90 to 93	COM1 ~COM4	O	Outputs for LCD display. Connected to the common pins on the LCD panel. The output pins are located at three positions: center and both ends of the chip. Each is connected inside the chip. Use the COM pins in accordance with the panel to be used. In the display off mode, all the outputs are fixed to GND. When the slave is set (M/S=”L”), COM1 to COM4 outputs are GND level fixed.
14 to 16	VDD	-	Power supply pin for logic circuit.
20 to 22	VLCD	-	Power supply pin for LCD driver.
17 to 19	GND	-	Ground pin.
9,29	VDDO	-	VDD output pin. Use this pin when fixing the mode setting input pin to "H" on the COG.
2,37	GNDO	-	Ground output pin. Use this pin when fixing the mode setting input pin to "L" on the COG.
1,38, 39,44, 89,94	DUMMY	-	Floating pin. At this time, avoid this pin from shorting with pins other than DUMMY in the wiring on the COG.

*1: For details of the COM /SEG waveform when a duty is selected, refer to "Common waveform" on page 24 and "Common Segment waveform" on page 25 to 29.

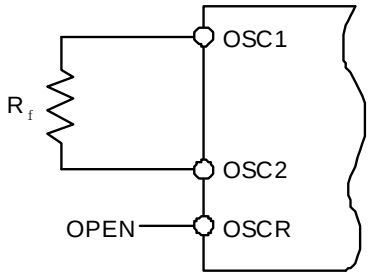
*2: Oscillator circuit configuration

• When M/S = "H", OSC I/E = "H"

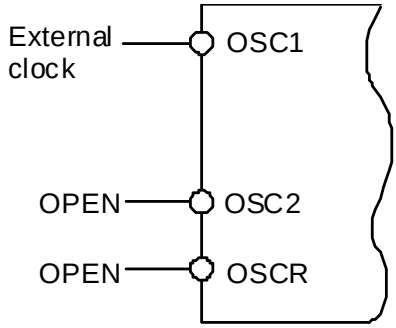
[Internal Rf oscillation mode]



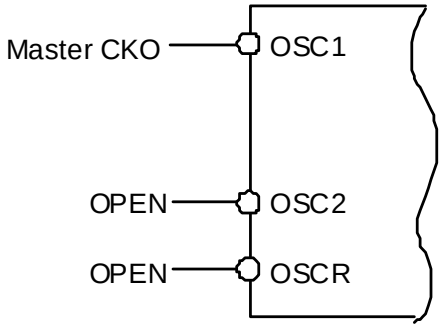
[External Rf oscillation mode]



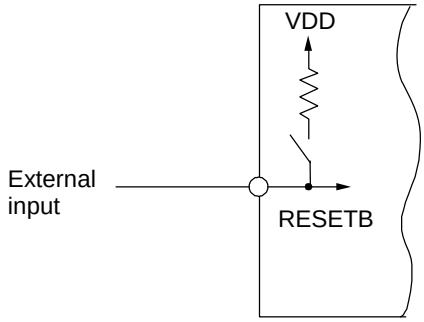
• External clock input mode when M/S = "H" and OSC I/E = "L"



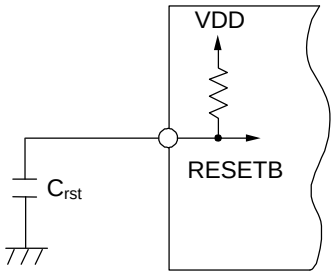
• M/S = "L", slave mode, external clock input mode



*3: Reset circuit configuration
• External input to RESTB when POCEB = "H"



• POC circuit configuration when POCEB = "L"

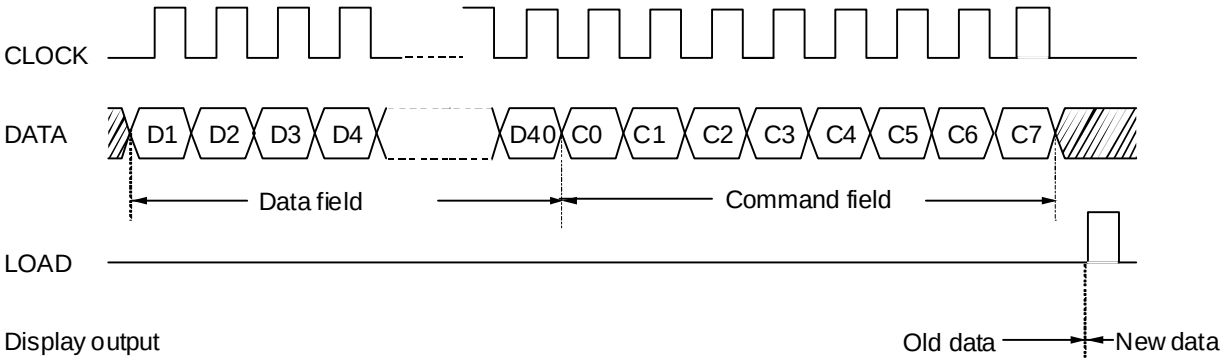


DESCRIPTION

Operation description (Serial interface)

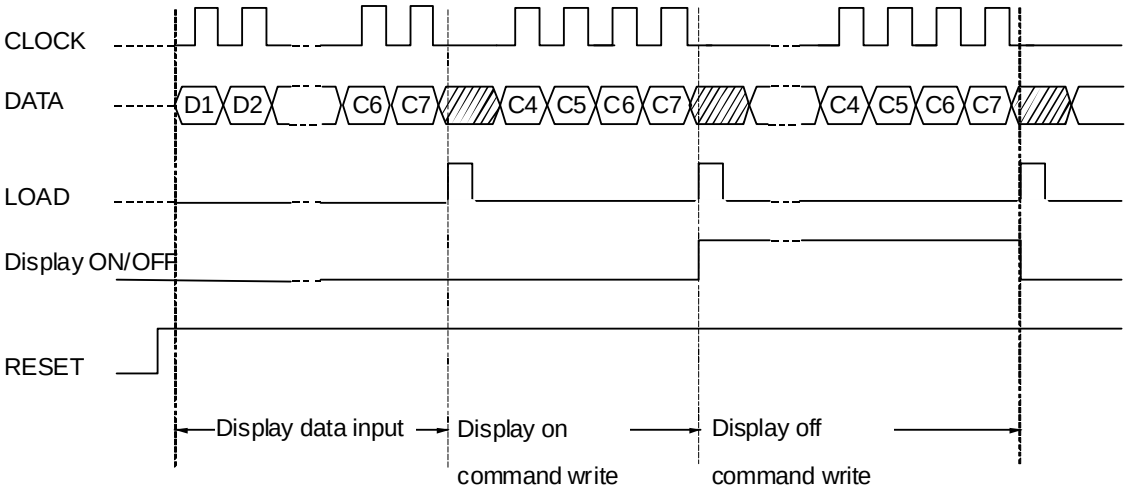
• Display data input

As described in the Data configuration section, the display data consists of the data field that corresponds to each segment on/off and the command field that indicates the display data input.
When inputting the display data, the "F3" command is set in the command field. When the "F1" or "F2" command is set in the command field, the display data in the data field becomes invalid.
The data input to the DATA pin is loaded to the shift register at the CLOCK pulse rise, transferred to the display data latch during the LOAD pulse at the "H" level, then output via the segment driver.



• Display on, Display off

The display becomes off at power-on reset. To display, write the display on command.
The display off is the command that makes all segments off. Writing the display off command、turns off the lights regardless of the display data.
The display on is the command to release the display off. Writing the display on command returns the display to the original state.



List of Commands

The ML9480 have two type command table. Command table can be selected by I2C and MODE input pins.

I2C Pin	MODE Pin	I/F	COMMAND
L	*	Serial	Command table A
H	L	I2C	Command table A
H	H	I2C	Command table B

List of Command table A Serial interface and I2C interface (When MODE pin is "L")

Command name	C7	C6	C5	C4	C3	C2	C1	C0	Operation
F0	0	0	x	x	x	x	x	x	Disabled
F1	0	1	F1 (*2)	F0 (*2)	FSEL (*2)	x	x	x	Frame frequency setting (valid for Internal CR oscillation) When FSEL =”0” (F1,F0)=(0, 0): 65Hz (F1,F0)=(0, 1): 75Hz (F1,F0)=(1, 0): 85Hz (F1,F0)=(1, 1): 95Hz When FSEL = ”1” (F1,F0)=(0, 0): 130Hz (F1,F0)=(0, 1): 150Hz (F1,F0)=(1, 0): 170Hz (F1,F0)=(1, 1): 190Hz
F2	1	0	1	D (*2)	x	x	x	x	Display on/off "0" : Off（COM=SEG=GND） "1" : On
F3(*1)	1	1	SA1	SA0	A1	A0	Co1	Co0	Data write address setting (Co1,Co0)=(0, 0): Corresponding to common 1 (Co1,Co0)=(0, 1): Corresponding to common 2 (Co1,Co0)=(1, 0): Corresponding to common 3 (Co1,Co0)=(1, 1): Corresponding to common 4 SA1, SA0, A1, A0: Chip address

x: Don't care
(*1): For the I^2C interface, SA1 and SA0 are set at a slave address.
These bits become "Don't care".
(*2): The register is set to the following value by the RESETB = "L" input or by the power-on POC.
F1="0", F0="0", FSEL="0", D="0"

List of Command table B I^2C interface(When MODE pin is "H")

Command name	Operation code								Initialize
	C7	C6	C5	C4	C3	C2	C1	C0	
Mode Set	C	1	0	x	D	B	M1	M0	D=B=M1=M2=”0”
Display RAM Address	C	0	P5	P4	P3	P2	P1	P0	
Chip Address	C	1	1	0	0	A2	A1	A0	
Frame Frequency Select	C	1	1	0	1	F1	F0	FSEL	F1=FSEL=”0” F0=”1”
Bank Select	C	1	1	1	1	0	I	O	I=O=”0”
Blink select	C	1	1	1	0	AB	BF1	BF0	AB=BF1=BF0=”0”

x: Don't care
C: Continue bit 0:last control byte in the transfer 1:control byte continue

MODE SET

	C7	C6	C5	C4	C3	C2	C1	C0
MODE SET	C	1	0	x	D	B	M1	M0

D: Display ON/OFF
“0”: OFF (COM=SEG=GND)
“1”: ON

B: LCD Bias Setting
“0”: 1/3 Bias
“1”: 1/2 Bias
This command becomes effective at I2C pin =”H” and MODE pin=”H”.

M[1:0]: Duty setting
M[1:0]=(0, 1) : Static
M[1:0]=(1, 0) : 1/2Duty
M[1:0]=(1, 1) : 1/3Duty
M[1:0]=(0, 0) : 1/4Duty
This command becomes effective at I2C pin =”H” and MODE pin=”H”.

Display RAM Address

	C7	C6	C5	C4	C3	C2	C1	C0
Display RAM address	C	0	P5	P4	P3	P2	P1	P0

P[5:0]=00_0000 to 10_0111
The increment of the display RAM address is carried out automatically.
Static +8, 1/2duty +4, 1/3duty +3, 1/4duty +2

Chip Address

	C7	C6	C5	C4	C3	C2	C1	C0
Display RAM address	C	1	1	0	0	A2	A1	A0

A[2:0] = 111 to 000
The terminal corresponding to A2 is SA1 pin.
The terminal corresponding to A1 is A1 pin.
The terminal corresponding to A0 is A0 pin.

Frame frequency select

	C7	C6	C5	C4	C3	C2	C1	C0
Frame Frequency	C	1	1	0	1	F1	F0	FSEL

Frame frequency setting.
This command becomes effective at I2C pin =”H”, MODE pin=”H”, BIAS pin =”L” and internal CR oscillation.
When BIAS pin =”H” and internal CR oscillation, frame frequency is set to 75Hz (initialize).

When FSEL =”0”
(F1,F0)=(0, 0): 65Hz
(F1,F0)=(0, 1): 75Hz
(F1,F0)=(1, 0): 85Hz
(F1,F0)=(1, 1): 95Hz

When FSEL = ”1”
(F1,F0)=(0, 0): 130Hz
(F1,F0)=(0, 1): 150Hz
(F1,F0)=(1, 0): 170Hz
(F1,F0)=(1, 1): 190Hz

Bank Select

	C7	C6	C5	C4	C3	C2	C1	C0
Bank Select	C	1	1	1	1	0	I	O

I: Input bank selection

I	Static	1/2Duty
0	COM1	COM1 & COM2
1	COM3	COM3 & COM4

This command has no effect in 1/3Duty and 1/4Duty mode.

O: Output bank selection

O	Static	1/2Duty
0	COM1	COM1 & COM2
1	COM3	COM3 & COM4

This command has no effect in 1/3Duty and 1/4Duty mode.

Blink Select

	C7	C6	C5	C4	C3	C2	C1	C0
Blink Select	C	1	1	1	0	AB	BF1	BF0

AB: Blink mode selection
“0”: Normal Blinking
“1”: Alternate RAM blinking does not apply in 1/3Duty and 1/4Duty.

BF[1:0]: Blink frequency selection

BF1	BF0	Blink Frequency			
0	0	Blink OFF			
		65Hz/130Hz	75Hz/150Hz	85Hz/170Hz	95Hz/190Hz
0	1	2.03Hz	2.34Hz	2.66Hz	2.97Hz
1	0	1.01Hz	1.17Hz	1.33Hz	1.48Hz
1	1	0.51Hz	0.59Hz	0.66Hz	0.74Hz

Display data RAM

This is the RAM storing the data of display and has an organization of 40 x 4.
Display RAM data RAM address map

Display RAM data “1” ... Dot is displayed
Display RAM data “0” ... Dot is not displayed

Display data RAM address map

	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5		SEG 37	SEG 38	SEG 39	SEG 40
COM1						・・・				
COM2						・・・				
COM3						・・・				
COM4						・・・				

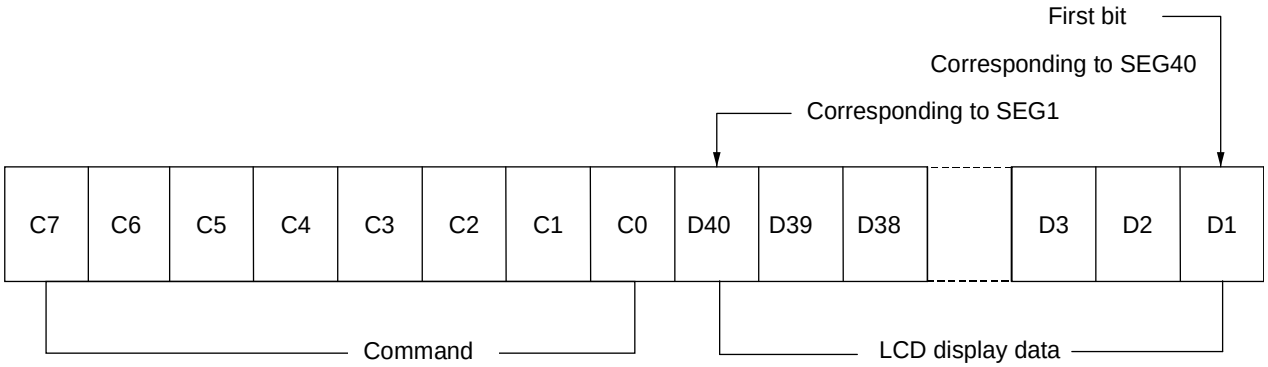
Static drive ... COM1
1/2duty drive ... COM1, COM2
1/3duty drive ... COM1, COM2, COM3
1/4duty drive ... COM1, COM2, COM3, COM4

Cascade connection

When command table B is chosen (I2C pin =”H”, MODE pin =”H”), ML9480 cannot used cascade connection.

Data configuration

• Data configuration (Serial interface)

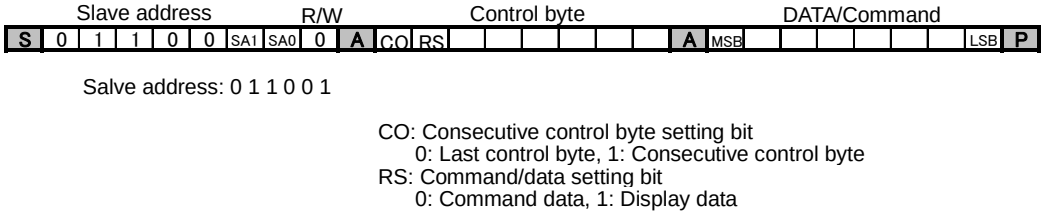


Note 1 : The commands F1 and F2 settings become valid when the least four bits of C4 to C7 are input.
(The bits from D1 to D40 and from C0 to C3 are not necessary.)

Note 2 : If the dummy bit is needed for the reason of number of transfer bits, put it on the first bit side.

Note 3 : The command execution follows the contents of the C7 to C0 registers immediately before the LOAD becomes "H".

• Data configuration (I^2C interface, When MODE pin is "L")



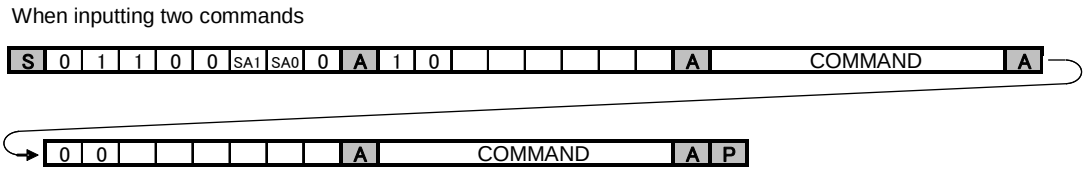
For the I^2C interface, each IC is assigned with a 7-bit slave address. The first one byte in the transfer consists of this 7-bit slave address and the R/W bit that indicates the data transfer direction. Always input "0" to the eighth R/W bit because the ML9480 is a write-only LSI.
The eight bits next to the slave address is a control byte. The first one bit is CO: consecutive command setting bit and the next one bit is RS: command/data setting bit (the remaining six bits are the Don't care bits).

When CO = "0": Means the last control byte.
When CO = "1": Means the control bytes are successively input.
When RS = "0": Means the data to be input next is the command data.
When RS = "1": Means the data to be input next is the display data.

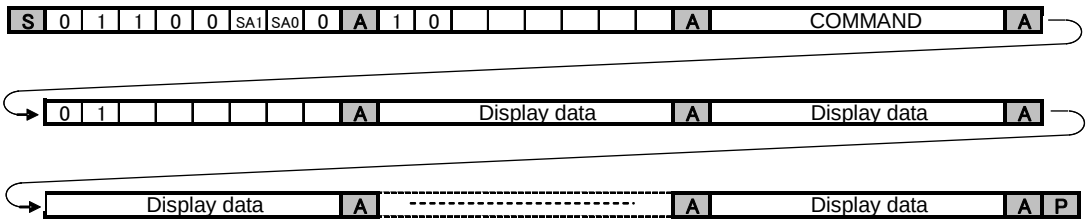
The display data can be successively input.

Example of Data Setting

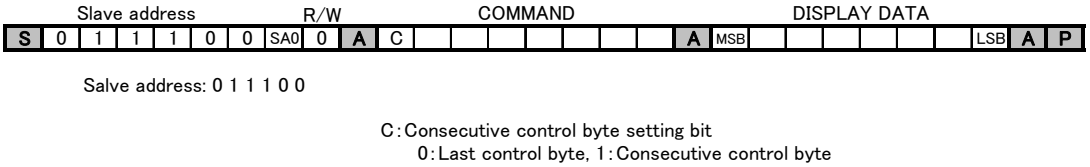
- When inputting two commands



- When inputting the command and display data



• Data configuration (I^2C interface, When MODE pin is "H")



For the I^2C interface, each IC is assigned with a 7-bit slave address. The first one byte in the transfer consists of this 7-bit slave address and the R/W bit that indicates the data transfer direction. Always input "0" to the eighth R/W bit because the ML9480 is a write-only LSI.
The eight bits next to the slave address is a control byte. The first one bit is CO: consecutive command setting bit.

When CO = "0": Means the last control byte.
When CO = "1": Means the control bytes are successively input.

Data write method

• Serial interface

The data is written to the address set by the data write setting command (F3).
For the Serial interface, the data is written in units of 40 bits.
Written from D40 to SEG1, D39 to SEG2, ... , D2 to SEG39, and D1 to SEG40.

	MSB					Segment Output								LSB
	1	2	3	4		32	33	34	35	36	37	38	39	40
COM1	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2	D1
COM2	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2	D1
COM3	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2	D1
COM4	D40	D39	D38	D37		D9	D8	D7	D6	D5	D4	D3	D2	D1

• I^2C interface (When MODE pin is "L")

The data is written to the address set by the slave address.
For the I^2C interface (When MODE pin is "L"), the data is written to the specified address starting with the LSB side in units of 8 bits.
(The data is written in the order from SEG33-40, SEG25-SEG32, SEG17-SEG24, SEG9-SEG16, and SEG1-SEG8.)

	LSB					Segment Output								MSB
	1	2	3	4		32	33	34	35	36	37	38	39	40
COM1	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7	D8
COM2	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7	D8
COM3	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7	D8
COM4	D1	D2	D3	D4		D8	D1	D2	D3	D4	D5	D6	D7	D8

• I^2C interface (When MODE pin is "H")

The data is written to the address set by the display RAM address.

For the I^2C interface (When MODE pin is "H"), the data is written to the specified address starting with the LSB side in units of 8 bits.

■ Static

	LSB					Segment Output							MSB
	1	2	3	4	5	6	7	8	9	37	38	39	40
COM1	D8	D7	D6	D5	D4	D3	D2	D1	D8	D4	D3	D2	D1
COM2	x	x	x	x	x	x	x	x	x	x	x	x	x
COM3	x	x	x	x	x	x	x	x	x	x	x	x	x
COM4	x	x	x	x	x	x	x	x	x	x	x	x	x

■ 1/2Duty

	LSB					Segment Output							MSB
	1	2	3	4	5	6	7	8	9	37	38	39	40
COM1	D8	D6	D4	D2	D8	D6	D4	D2	D8	D8	D6	D4	D2
COM2	D7	D5	D3	D1	D7	D5	D3	D1	D7	D7	D5	D3	D1
COM3	x	x	x	x		x	x	x	x	x	x	x	x
COM4	x	x	x	x		x	x	x	x	x	x	x	x

■ 1/3Duty

	LSB					Segment Output							MSB
	1	2	3	4	5	6	7	8	9	37	38	39	40
COM1	D8	D5	D2	D8	D5	D2	D8	D5	D2	D2	D8	D5	D2
COM2	D7	D4	D1	D7	D4	D1	D7	D4	D1	D1	D7	D4	D1
COM3	D6	D3	x	D6	D3	x	D6	D3	x	x	D6	D3	x
COM4	x	x	x	x	x	x	x	x	x	x	x	x	x

■ 1/4Duty

	LSB					Segment Output							MSB
	1	2	3	4	5	6	7	8	9	37	38	39	40
COM1	D8	D4	D8	D4	D8	D4	D8	D4	D8	D8	D4	D8	D4
COM2	D7	D3	D7	D3	D7	D3	D7	D3	D7	D7	D3	D7	D3
COM3	D6	D2	D6	D2	D6	D2	D6	D2	D6	D6	D2	D6	D2
COM4	D5	D1	D5	D1	D5	D1	D5	D1	D5	D5	D1	D5	D1

• RAM writing in 1/3 duty drive mode (When I2C pin is "H" and MODE pin is "H")

■ 1/3Duty (Standard RAM filling)

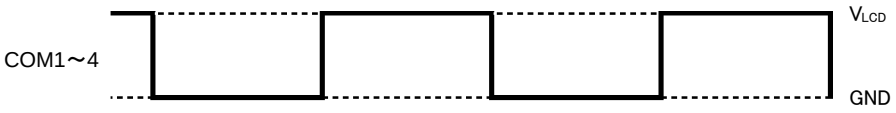
	LSB					Segment Output				MSB
	1	2	3	4	5	6	7	8	9	・・・
COM1	a8	a5	a2	b8	b5	b2	c8	c5	c2	・・・
COM2	a7	a4	a1	b7	b4	b1	c7	c4	c1	・・・
COM3	a6	a3	x	b6	b3	x	c6	c3	x	・・・
COM4	x	x	x	x	x	x	x	x	x	・・・

■ 1/3Duty (Entire RAM filling by rewriting)

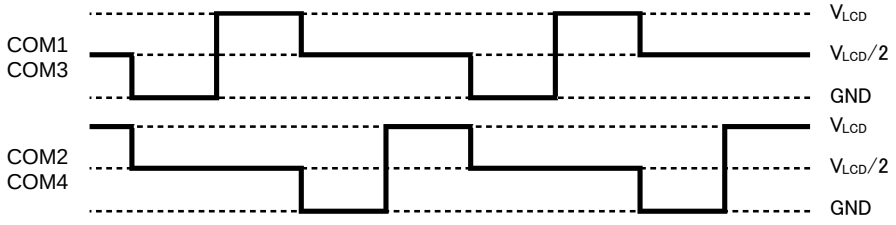
	LSB					Segment Output				MSB
	1	2	3	4	5	6	7	8	9	
COM1	a8	a5	a2/b8	b5	b2/c8	c5	c2/d8	d5	d2/e8	
COM2	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	
COM3	a6	a3	b6	b3	c6	c3	d6	d3	e6	
COM4	x	x	x	x	x	x	x	x	x	

- Common waveforms

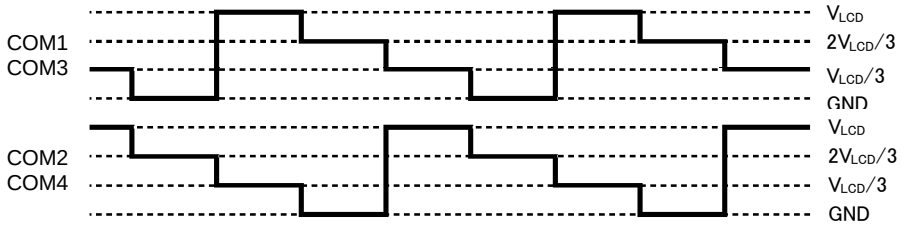
(1) At static



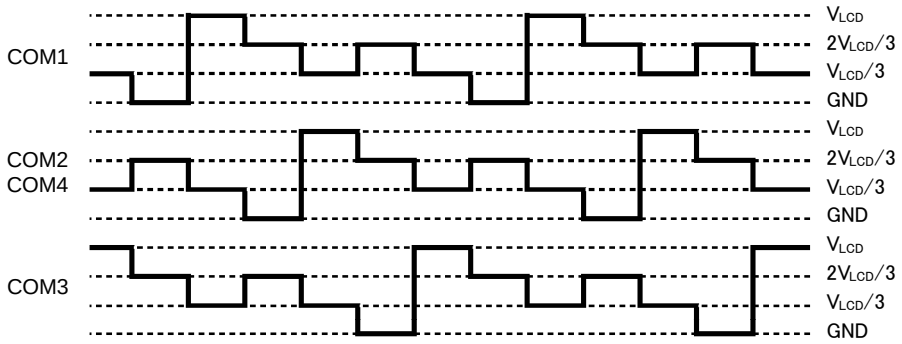
(2) At 1/2-duty
At 1/2-bias



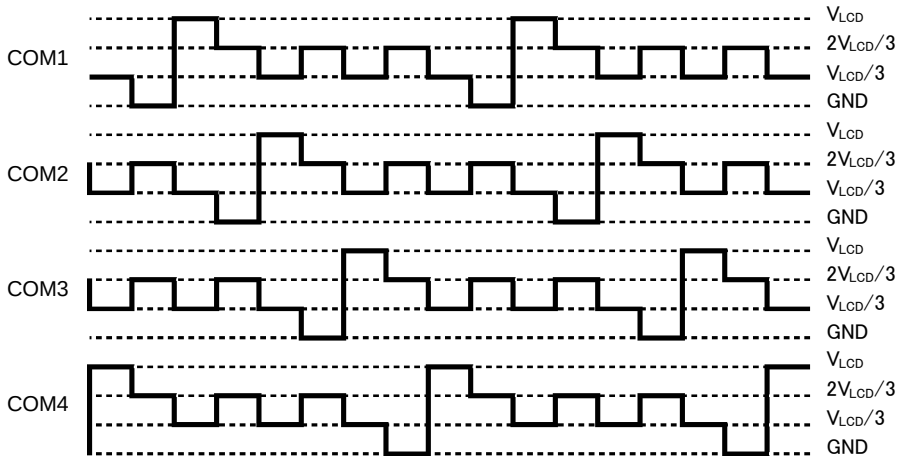
At 1/3-bias



(3) At 1/3-duty

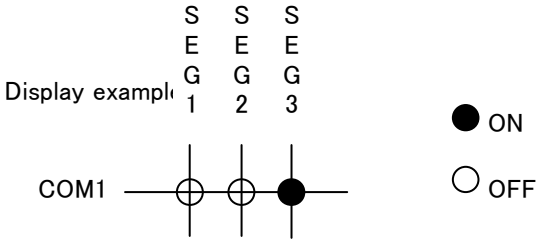


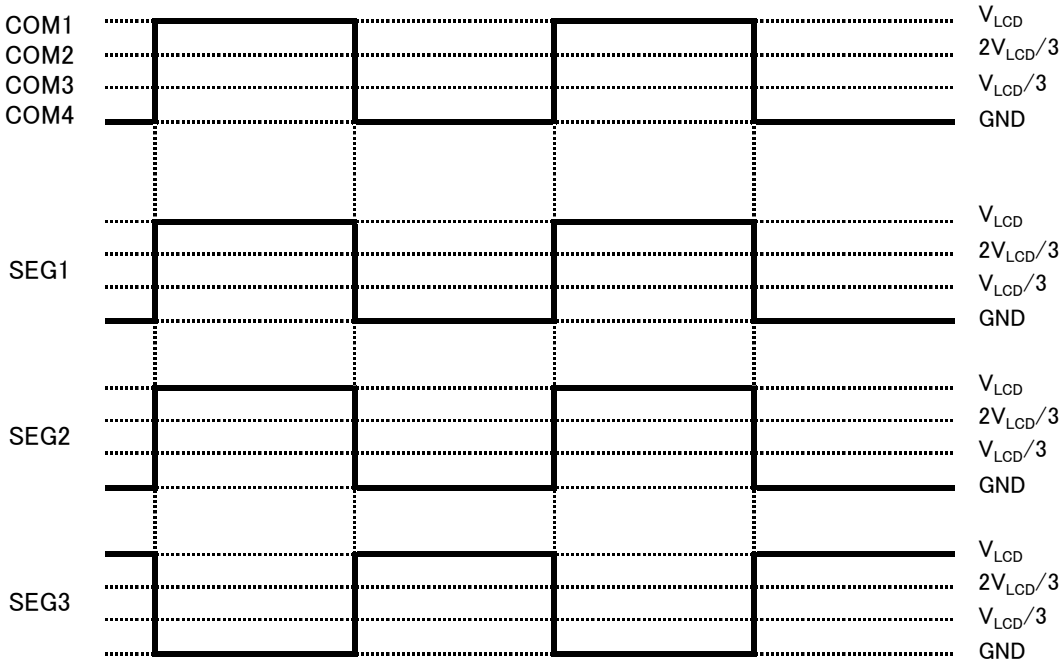
(4) At 1/4-duty



- Common and segment output waveforms

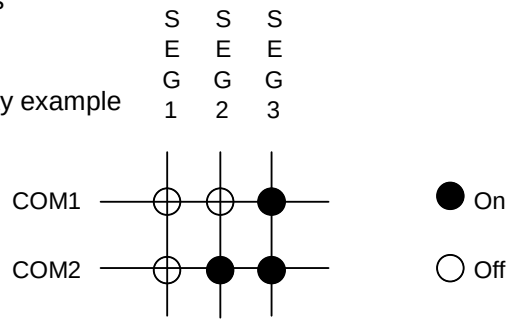
・At Static

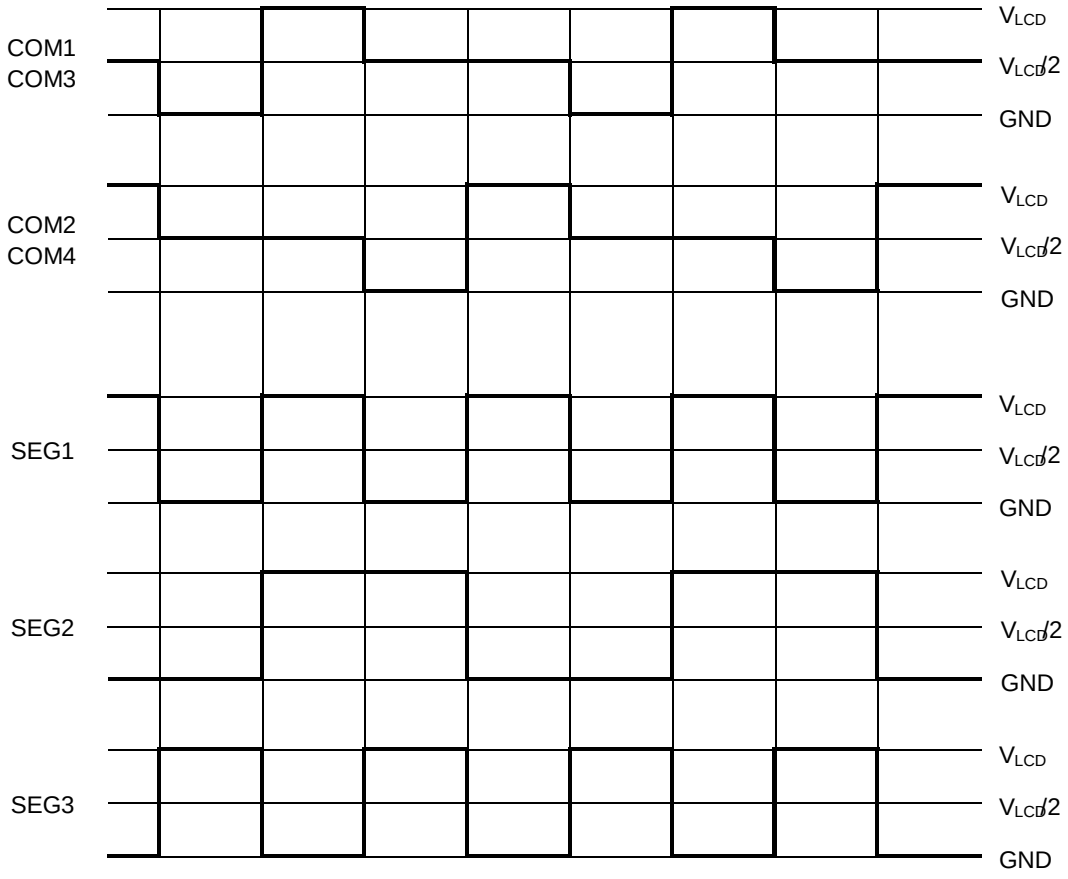




- Common and segment output waveforms
  - ・At 1/2 Duty、1/2bias

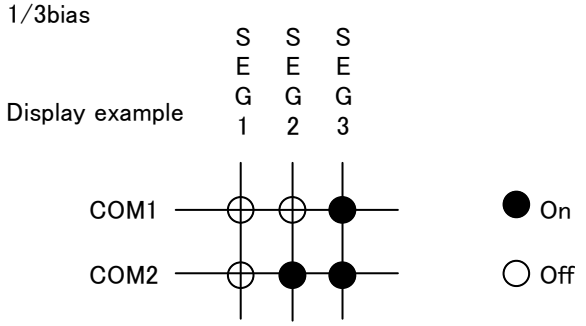
Display example

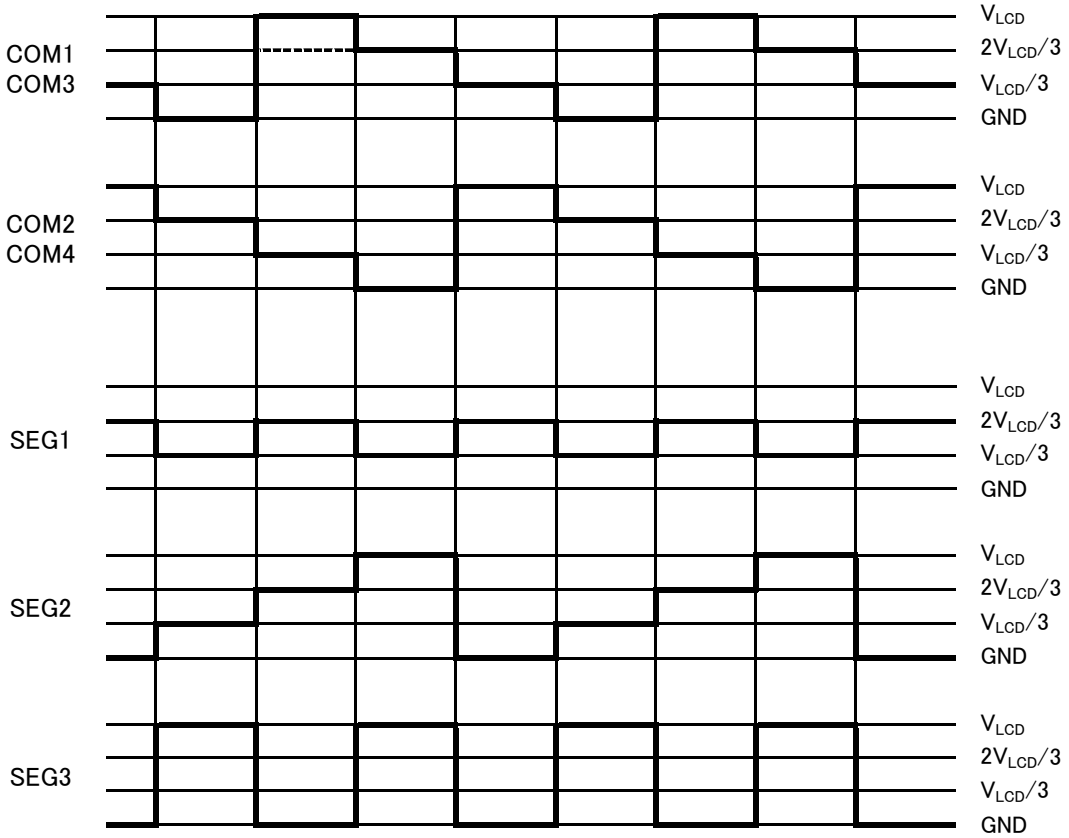




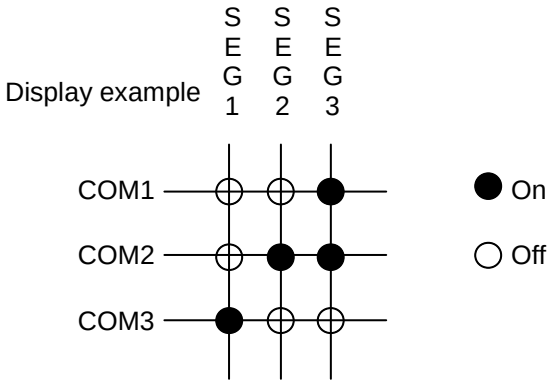
- Common and segment output waveforms

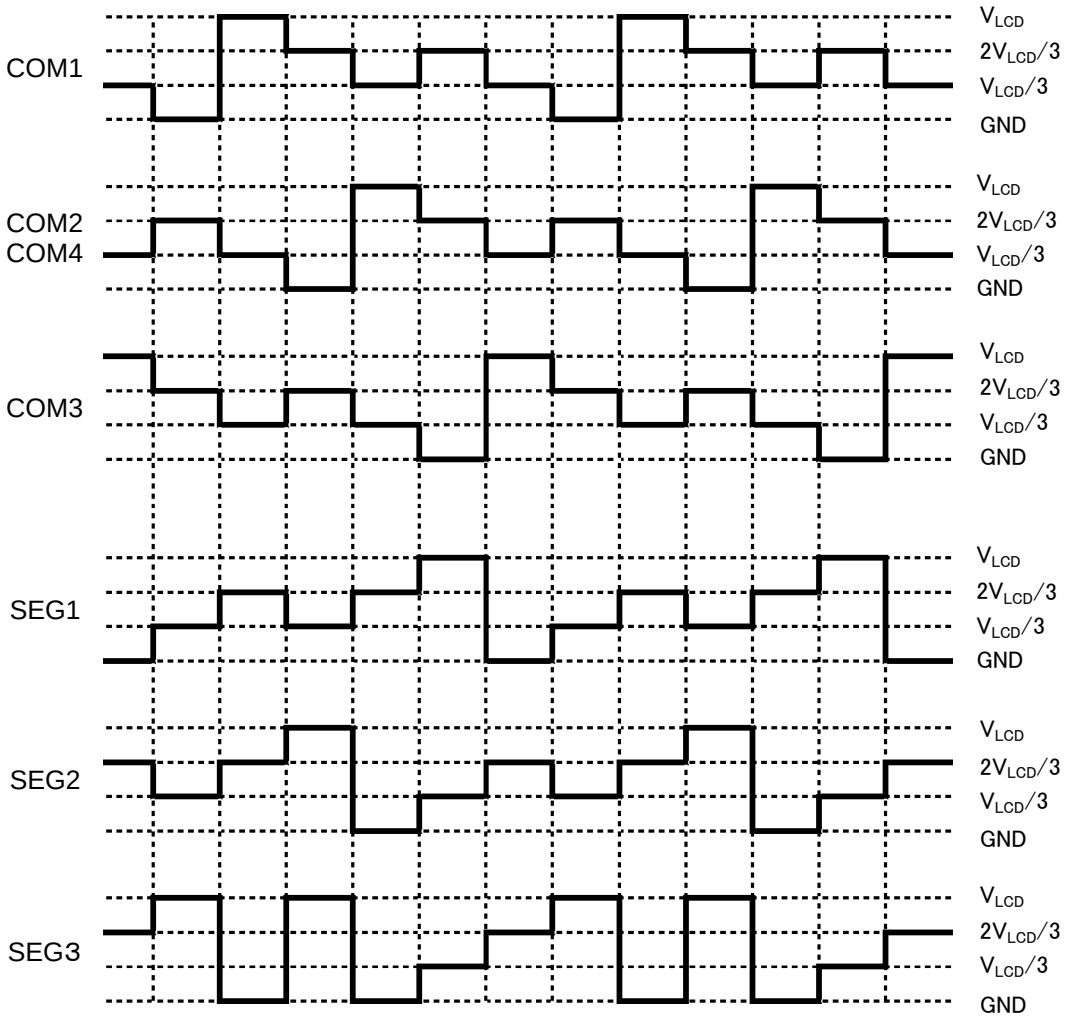
・At 1/2 Duty、1/3bias



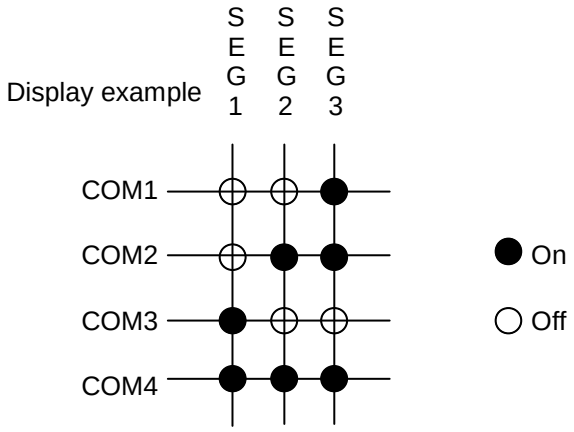


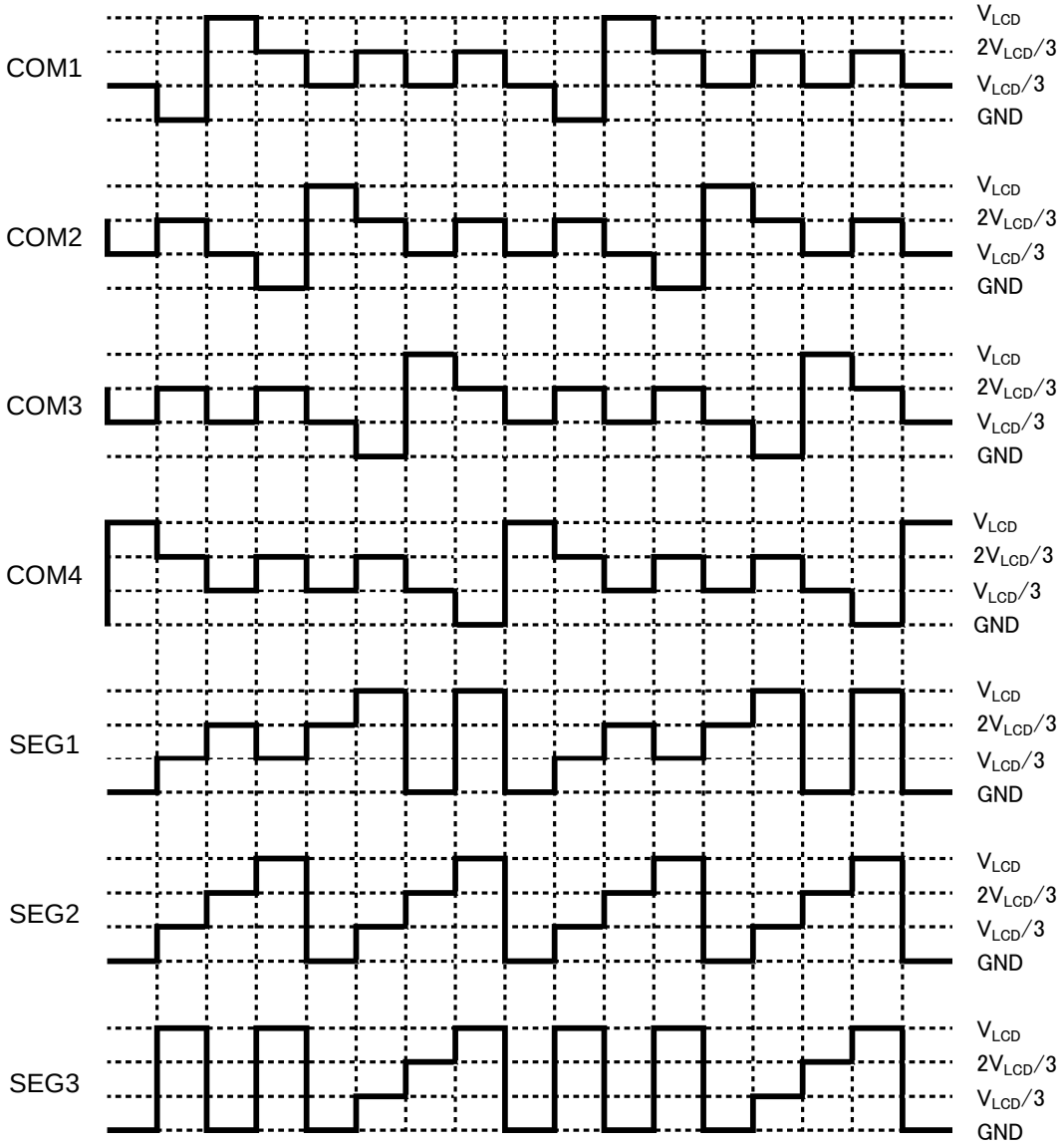
- Common and segment output waveforms
  · At 1/3-duty



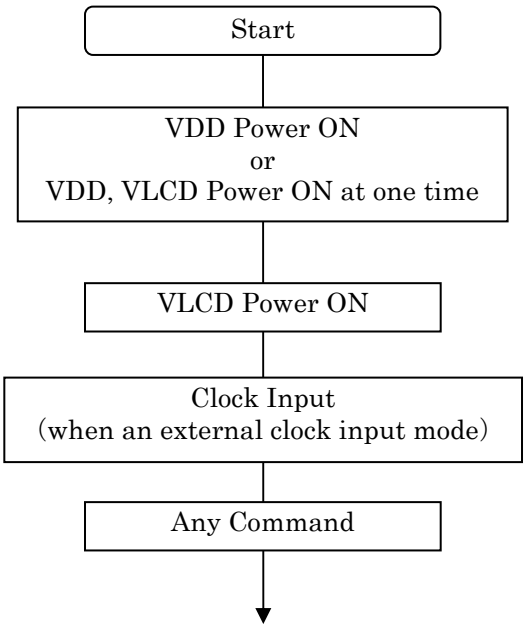


- Common and segment output waveforms
  · At 1/4-duty

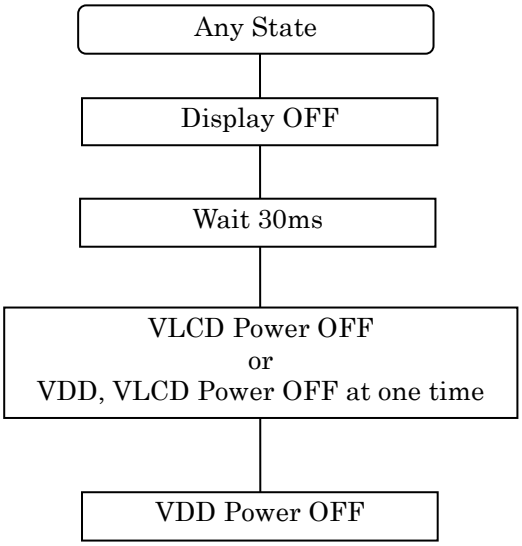




POWER ON SEQUENCE



POWER OFF SEQUENCE

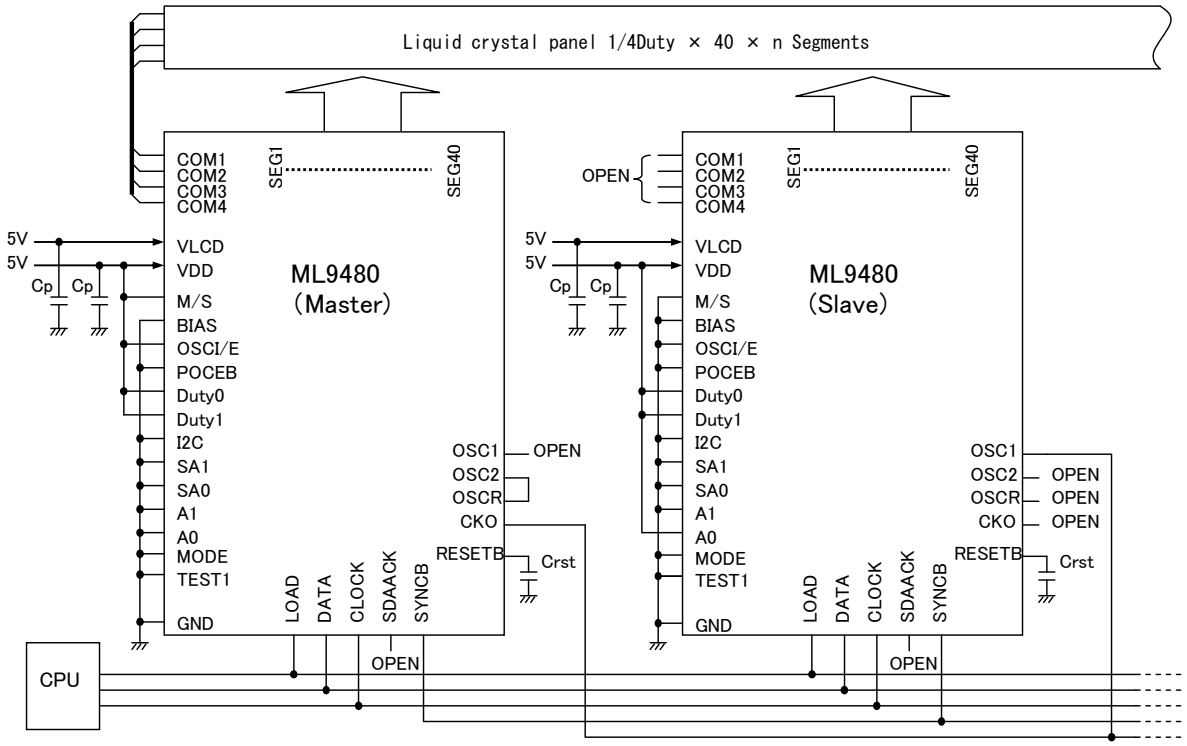


EXAMPLE OF APPLICATION CIRCUIT

Cascade configuration 1

Serial interface
Internal CR oscillator circuit used
1/4Duty
RESETB pin + external capacitance connection to configure POC circuit
The common outputs of the slave chip output GND-level. So Com1 to Com4 set to open.

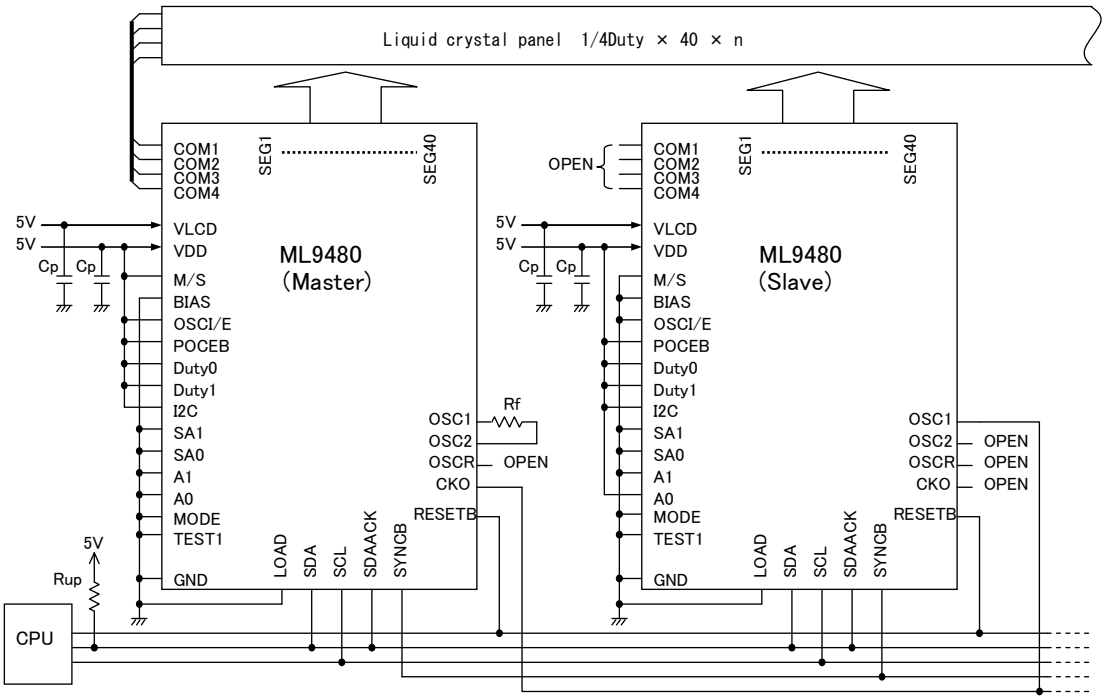
[External component]
Cp = 0.1 [µF] (bypass capacitor between power supplies)
Crst = 4.7 [µF] (capacitance for external POC circuit)



Cascade configuration 2

II^{2}C interface
External Rf-based CR oscillator circuit used
1/4Duty
External RESETB signal input
The common outputs of the slave chip output GND-level. So Com1 to Com4 set to open.

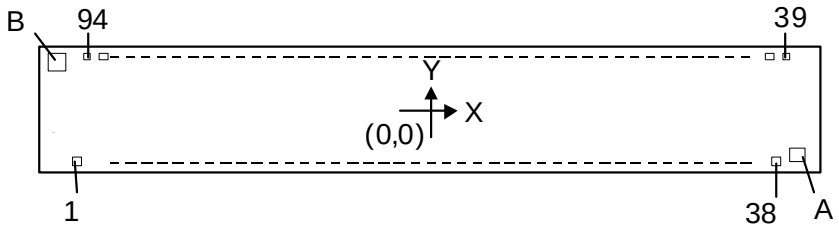
[External component]
Cp = 0.1 [μF] (bypass capacitor between power supplies),
Rf = 470 [kΩ] (external R, resistor for CR oscillator circuit),
Rup = Resistor for SDA data bus pull-up



PAD CONFIGURATION

Pad layout (pattern face)

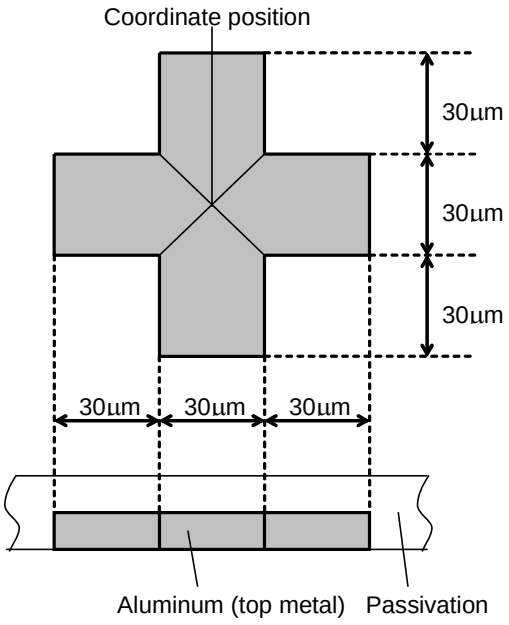
Chip size	: 3.30 mm × 0.90mm
Chip thickness	: 400 μm ± 20 μm
Minimum bump pitch	: 50 μm
Bump height	: 15 μm ±3 μm



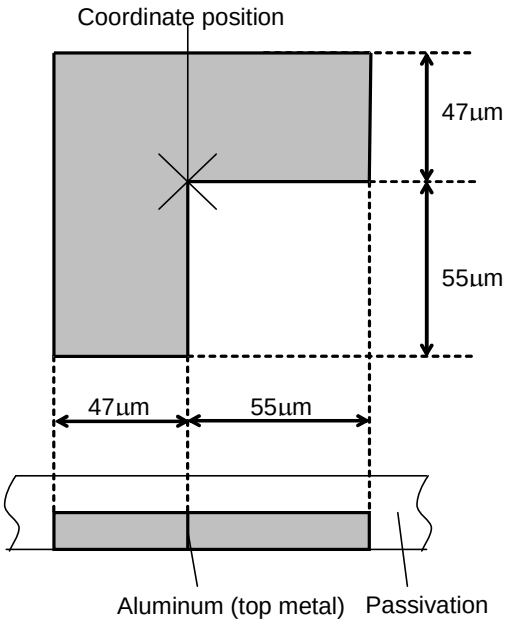
Bump and alignment mark dimensions (pattern face)

PAD No.1~38	: 32 μm x 80 μm
PAD No.39~94	: 30 μm x 84 μm
Alignment marks A and B	: See below

[Mark A]



[Mark B]



Alignment Mark	X-coordinate (μm)	Y-coordinate (μm)
Mark A	1506	-190
Mark B	-1539	309

Pad center coordinates

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
1	DUMMY	-1430	-308	41	COM2	1325	309
2	GNDO	-1350	-308	42	COM3	1275	309
3	Duty1	-1270	-308	43	COM4	1225	309
4	Duty0	-1190	-308	44	DUMMY	1175	309
5	A0	-1110	-308	45	SEG1	1125	309
6	A1	-1030	-308	46	SEG2	1075	309
7	SA0	-950	-308	47	SEG3	1025	309
8	SA1	-870	-308	48	SEG4	975	309
9	VDDO	-790	-308	49	SEG5	925	309
10	SDAACK	-710	-308	50	SEG6	875	309
11	DATA(SDA)	-630	-308	51	SEG7	825	309
12	CLOCK(SCL)	-550	-308	52	SEG8	775	309
13	LOAD	-470	-308	53	SEG9	725	309
14	VDD	-390	-308	54	SEG10	675	309
15	VDD	-310	-308	55	SEG11	625	309
16	VDD	-230	-308	56	SEG12	575	309
17	GND	-150	-308	57	SEG13	525	309
18	GND	-70	-308	58	SEG14	475	309
19	GND	10	-308	59	SEG15	425	309
20	VLCD	90	-308	60	SEG16	375	309
21	VLCD	170	-308	61	SEG17	325	309
22	VLCD	250	-308	62	SEG18	275	309
23	RESETB	330	-308	63	SEG19	225	309
24	OSC1	410	-308	64	SEG20	175	309
25	OSC2	490	-308	65	COM1	125	309
26	OSCR	570	-308	66	COM2	75	309
27	CKO	650	-308	67	COM3	25	309
28	SYNCB	730	-308	68	COM4	-25	309
29	VDDO	810	-308	69	SEG21	-75	309
30	I2C	890	-308	70	SEG22	-125	309
31	MODE	970	-308	71	SEG23	-175	309
32	M/S	1050	-308	72	SEG24	-225	309
33	POCEB	1130	-308	73	SEG25	-275	309
34	OSCI/E	1210	-308	74	SEG26	-325	309
35	BIAS	1290	-308	75	SEG27	-375	309
36	TEST1	1370	-308	76	SEG28	-425	309
37	GNDO	1450	-308	77	SEG29	-475	309
38	DUMMY	1530	-308	78	SEG30	-525	309
39	DUMMY	1425	309	79	SEG31	-575	309
40	COM1	1375	309	80	SEG32	-625	309

Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)	Pad number	Pad name	X-coordinate (μm)	Y-coordinate (μm)
81	SEG33	-675	309				
82	SEG34	-725	309				
83	SEG35	-775	309				
84	SEG36	-825	309				
85	SEG37	-875	309				
86	SEG38	-925	309				
87	SEG39	-975	309				
88	SEG40	-1025	309				
89	DUMMY	-1075	309				
90	COM4	-1125	309				
91	COM3	-1175	309				
92	COM2	-1225	309				
93	COM1	-1275	309				
94	DUMMY	-1325	309				

REVISION HISTORY

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL9480-01	Oct .1,2012	–	–	Final edition 1 issued

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