

Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. ("LAPIS Technology") and LAPIS Technology succeeded LAPIS Semiconductor's LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ML9484

Static, 1/2 Duty, 1/3 Duty, 1/4 Duty 50 Outputs LCD Driver

GENERAL DESCRIPTION

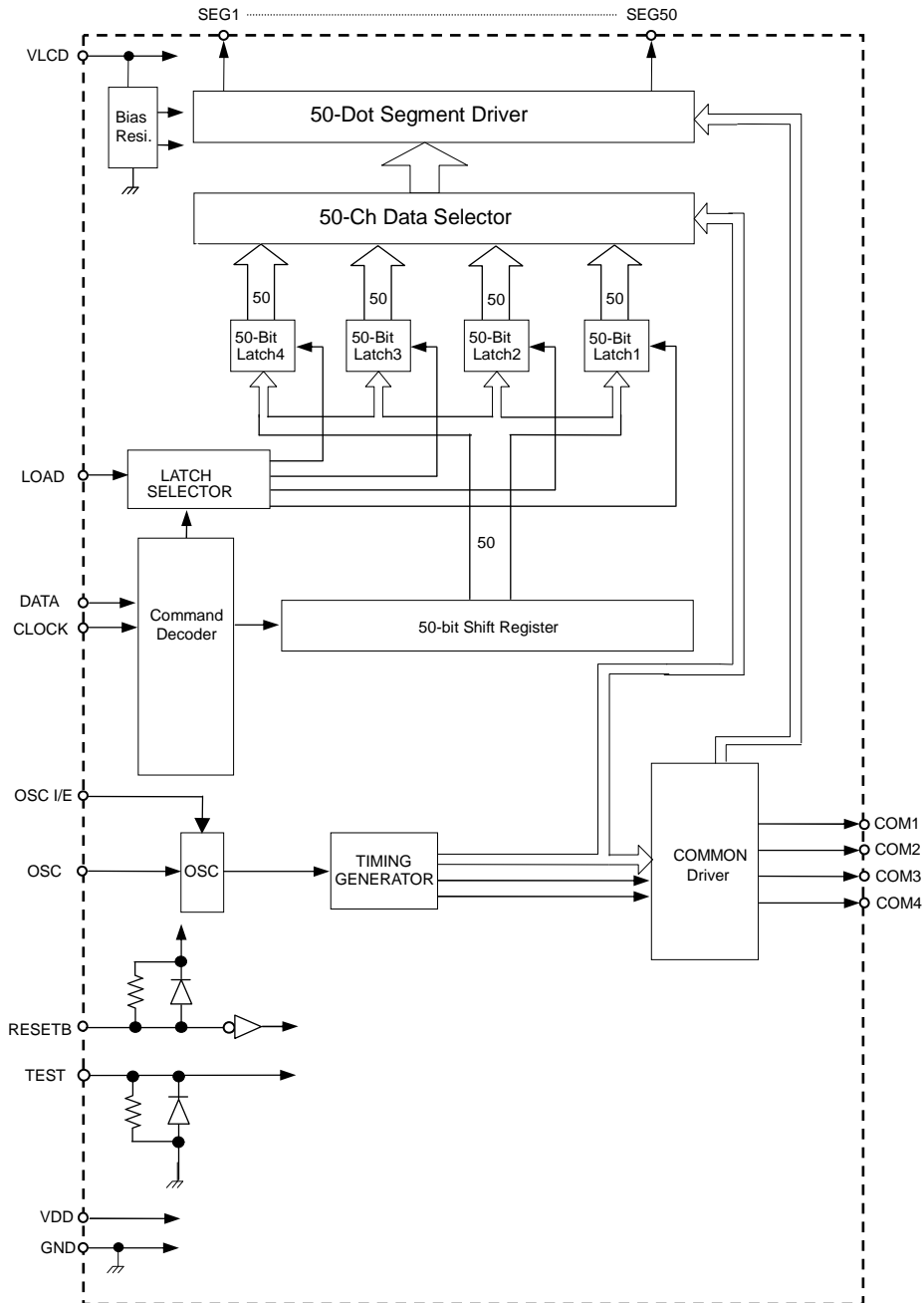
The ML9484 is an LCD driver LSI, consists of a 50-bit shift register, a 200-bit data latch, 50 sets of LCD drivers, and a common signal generation circuit.

It can directly drive an LCD up to 50 segments for static display, 100 segments for 1/2-duty display, 150 segments for 1/3-duty display, and 200 segments for 1/4-duty display.

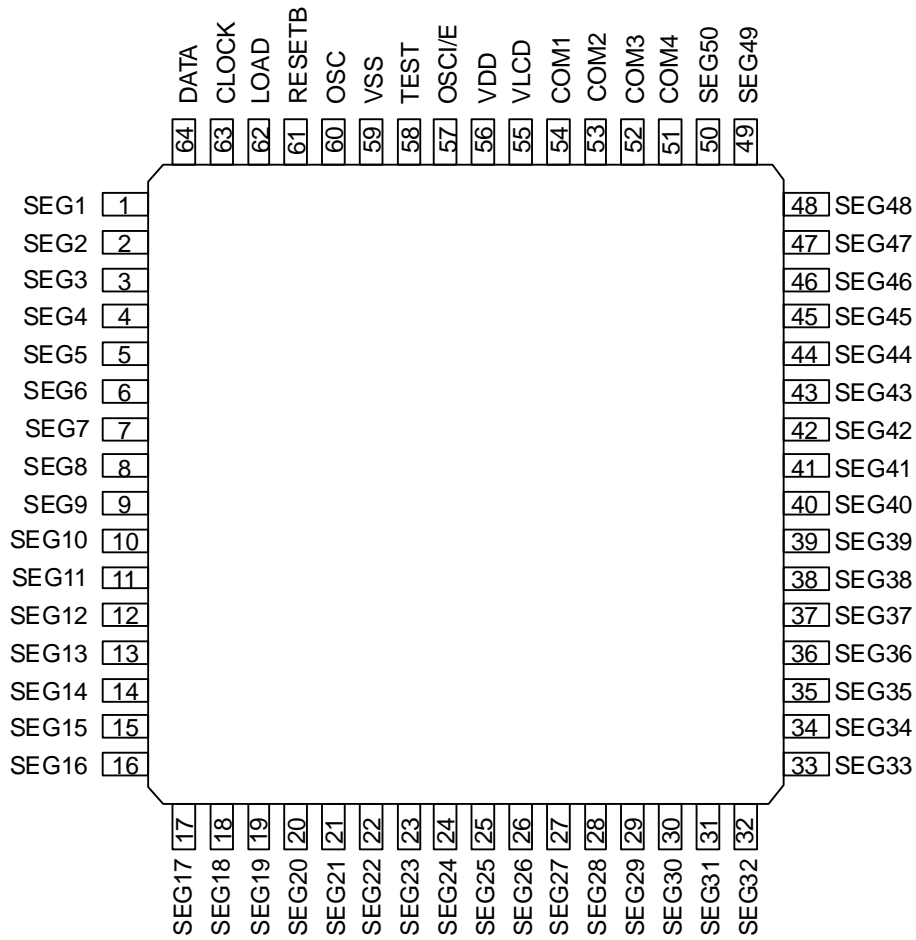
FEATURES

- Logic power supply voltage : 2.7 to 5.5 V
- LCD drive power supply voltage : 4.5 to 5.5 V
- Maximum number of segments
 - Static display : 50 segments
 - 1/2-duty display : 100 segments
 - 1/3-duty display : 150 segments
 - 1/4-duty display : 200 segments
- Serially interfaces with the CPU using the three signal lines of DATA, CLOCK, and LOAD
- Selectable internal CR oscillator circuit or external clock input
- Built-in bias circuit
- Built-in common output intermediate-value voltage generation circuit
- Command-selectable A-waveform or B-waveform
- Package : 64-pin plastic TQFP

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic TQFP

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Rating	Unit
Logic power supply voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to 6.0	V
LCD drive power supply voltage	V_{LCD}	$T_a = 25^\circ\text{C}$	-0.3 to 6.0	V
Input voltage	V_I	$T_a = 25^\circ\text{C}$	- 0.3 to $V_{DD} + 0.3$	V
Output short-circuit current	I_S	$T_a = 25^\circ\text{C}$	-2.0 to +2.0	mA
Power dissipation	P_D	$T_a \leq 105^\circ\text{C}$	145	mW
Storage temperature	T_{STG}	—	-55 to +150	$^\circ\text{C}$

Note: Do not use the ML9484 by short-circuiting one output pin to another output pin as well as to other pin (input pin, input/output pin, or power supply pin).

RECOMMENDED OPERATION CONDITIONS

Item	Symbol	Condition	Range	Unit
Logic power supply voltage	V_{DD}^*	—	2.7 to 5.5	V
LCD drive power supply voltage	V_{LCD}^*	—	4.5 to 5.5	V
OSC IN clock frequency	f_{CP1}	—	0.5 to 10	kHz
Data clock frequency	f_{CP2}	—	0.01 to 1.0	MHz
Operating temperature	T_a	—	-40 to +105	$^\circ\text{C}$

Note(*): Use at $V_{DD} \leq V_{LCD}$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD} = 2.7$ to 5.5 V, $V_{LCD} = 4.5$ to 5.5 V, $T_a = -40$ to $+105^\circ\text{C}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin	
"H" input voltage	V_{IH}	—	$0.8V_{DD}$	—	V_{DD}	V	(*1)	
"L" input voltage	V_{IL}	—	GND	—	$0.2V_{DD}$	V	(*1)	
Input leakage current 1	I_{L1}	$V_I = V_{DD}$ or 0 V	-1	—	1	μA	(*2)	
Input leakage current 2	I_{L2}	$V_I = V_{DD}$	-1	—	1	μA	RESETB	
Pull-up current	I_{pu}	$V_{DD} = 5.0\text{V}, V_I = 0$ V	30	—	140	μA	RESETB	
Driver ON resistor	Segment	V_{OHS}	$V_{LCD} = 5\text{V}$	—	5	15	k Ω	SEG1 to SEG50
	Common	V_{OHC}	$V_{LCD} = 5\text{V}$	—	5	12	k Ω	COM 1 to COM4
Static supply current	I_{DDs}	$V_{DD}=V_{LCD}=5.5$ V Input pin fixed to "H" or "L"	—	1	7	μA	VDD	
	I_{LCDs}	Oscillation stopped, output no-load	—	9	15	μA	VLCD	
Dynamic supply current 1	I_{DD1}	$V_{DD}=V_{LCD}= 5.5$ V (*3) Clock OSC external input	—	2	10	μA	VDD	
	I_{LCD1}	$f_{CP1}=1.8\text{kHz}$	—	9	15	μA	VLCD	
Dynamic supply current 2	I_{DD2}	$V_{DD}=V_{LCD}= 5.5$ V (*4) Internal oscillation=95Hz	—	53	82	μA	VDD	
	I_{LCD2}		—	9	15	μA	VLCD	

(*1): DATA, CLOCK, LOAD, RESETB, OSC, OSC I/E

(*2): DATA, CLOCK, LOAD, OSC, OSC I/E

(*3): 1/4-duty, 1/3-bias, OSC I/E="L", Output pin no-load.

(*4): 1/4-duty, 1/3-bias, OSC I/E="H", (F2, F, F0) = (0, 1, 1) 95 Hz, Output pin no-load.

Switching Characteristics

- OSC timing

(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
OSC IN clock frequency (External input)	f _{CP1}	Clock input from OSC. OSC I/E = "L"	0.5	1.8	10	kHz	OSC
Clock pulse width (External input)	t _{WCP1}		40	—	—	μs	OSC
Clock rise and fall time (External input)	t _{OSC}		—	—	(*1)	μs	OSC
Internal clock frequency (Internal oscillation)	f _{OSC1}	OSC open. (F2, F1, F0)=(0, 0, 1) OSC I/E = "H"	18	28.8	44	kHz	OSC

The relation between OSC IN clock frequency and frame frequency is as the equation below.

$$f_{FRM} = f_{CP1} / 24$$

(*1) t_{OSC} is a reference value.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: max=2μs.

- Serial interface timing

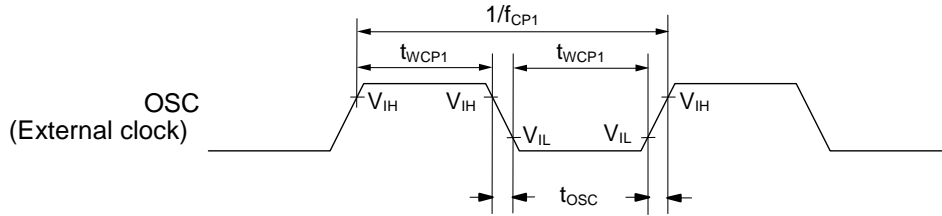
(V_{DD} = 2.7 to 5.5 V, V_{LCD} = 4.5 to 5.5 V, Ta = -40 to +105°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Data clock frequency	f _{CP2}		0.01	—	1	MHz	CLOCK
Data clock pulse width	t _{WCP2}		100	—	—	ns	CLOCK
Data setup time	t _{SU}		50	—	—	ns	DATA
Data hold time	t _{HD}		50	—	—	ns	CLOCK
CLOCK-LOAD timing	t _{CL}		100	—	—	ns	CLOCK
LOAD-CLOCK timing	t _{LC}		100	—	—	ns	LOAD
LOAD pulse width	t _{WLD}		100	—	—	ns	LOAD
Signal rise and fall time	tsr,tsf		—	—	(*2)	ns	CLOCK,DATA, LOAD

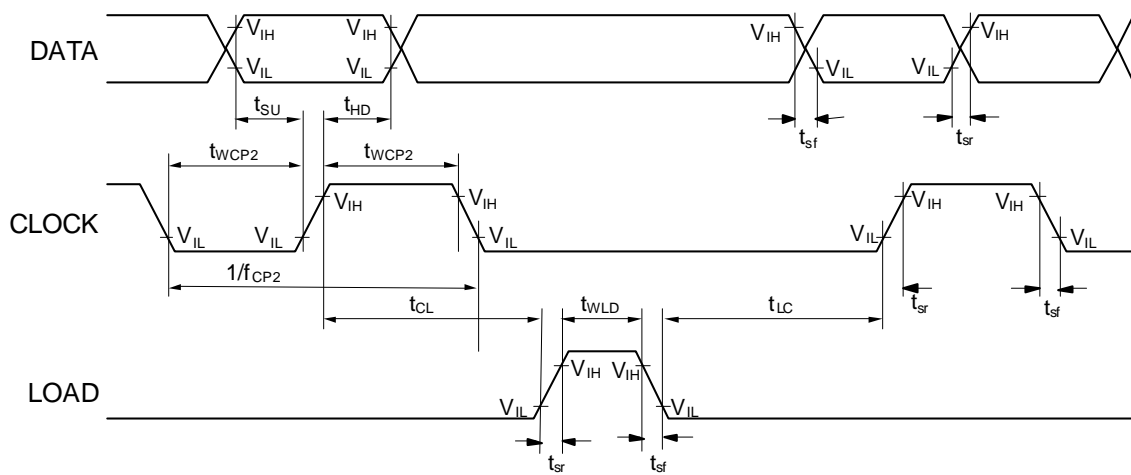
(*2) tsr and tsf shall be reference values.

The longer the clock rise and fall time, the more susceptible to extraneous noises around the threshold value.
Make the rise as steep as possible. Reference value: max=10ns.

Timing chart (OSC)



Timing chart (Serial interface)

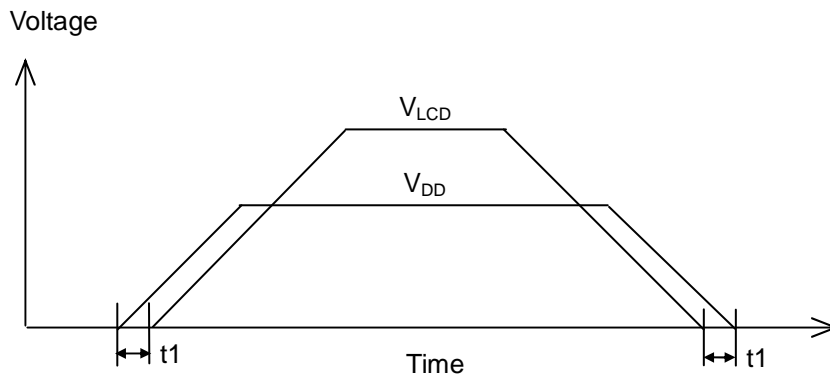


POWER ON/OFF TIMING

To turn on the power supply, raise the logic power supply first, then LCD drive power supply in order to prevent the IC from malfunctioning.

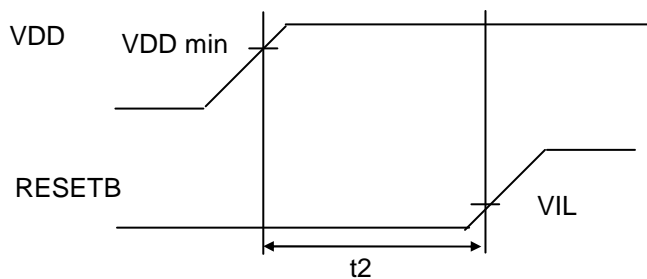
To fall the power supply, fall the LCD drive power supply first, then the logic power supply.

For a VDD pin ranging from 0 V to VDDmin, set $V_{DD} \geq V_{LCD}$ and $t_1 \geq 0$ [ns].



INITIALIZATION SIGNAL TIMING

Keep the RESETB pin at "L" level until the VDD reaches VDD min. ($t_2 \geq 200$ [ns])



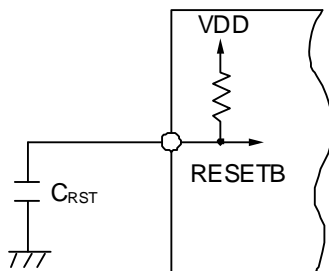
The value of the current of the pull-up resistor is specified for RESETB pin.

The customer needs to select an external capacitor that meets the timing requirements shown above.

PIN DESCRIPTIONS

Pad number	Symbol	I/O	Description
1 to 50	SEG1 to SEG50	O	Outputs for LCD display. Connected to the segment pins on the LCD panel. In the display off mode, all the outputs are fixed to GND.
51 to 54	COM1 to COM4	O	Outputs for LCD display. Connected to the common pins on the LCD panel. In the display off mode, all the outputs are fixed to GND.
55	VLCD	-	Power supply pin for LCD driver.
56	VDD	-	Power supply pin for logic circuit.
57	OSC I/E	I	This input selects whether to use the external clock input mode or to use the Internal oscillation mode. It has a schmitt circuit. When this pin is "H", the mode is the Internal Rf oscillation mode. When this pin is "L", the mode is the external clock input mode.
58	TEST	I	IC test pin. Has a pull-down resistor built-in. Use it as it is connected to GND.
59	GND	-	Ground pin.
60	OSC	I	Pin for oscillation. Has a Schmitt circuit built-in. Internal Rf oscillation mode: Set the OSCI/E pin to "H", open the OSC pin. External clock input mode: Set the OSCI/E pin to "L", input the external clock to the OSC pin.
61	RESETB	I	Reset signal input pin for initializing inside the IC. It has a schmitt circuit. The "L" level enables the reset. This pin has an Internal pull-up resistor. The power-on reset operation is available by connecting an external capacitor. *1
62	LOAD	I	Input pin for the load signal of display data. It has a schmitt circuit. The display data in the shift register is transmitted as is to the segment driver for the "H" duration. When this pin is brought into "L", the shift register is disconnected from the segment driver. The display data in the shift register immediately before it become "L" is held in the data latch and transmitted to the segment driver.
63	CLOCK	I	Shift clock input pin for display data. It has a schmitt circuit. The display data input to the DATA pin is serially input to the shift register at the CLOCK signal rise.
64	DATA	I	Display data input pin. It has a schmitt circuit. Input the display data in the order of SEG50, SEG49, ... , SEG2, and SEG1. The display data turns on at "H" and turns off at "L".

*1: Reset circuit configuration

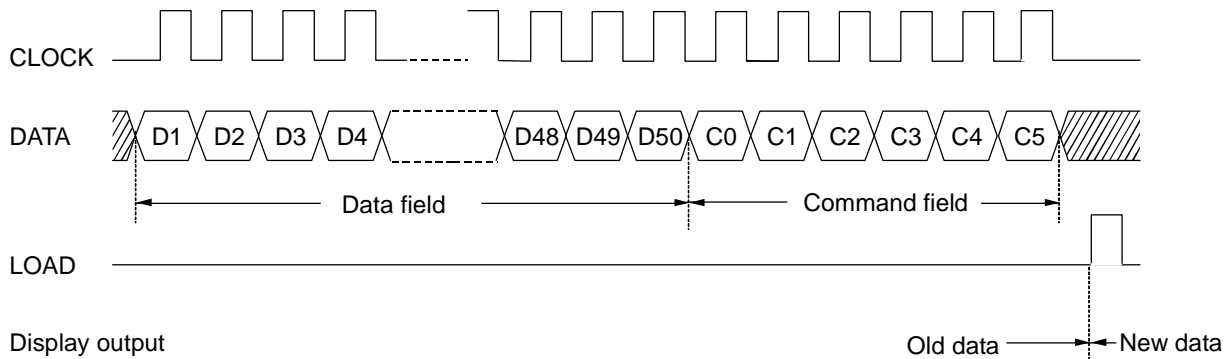


DESCRIPTION

Operation description

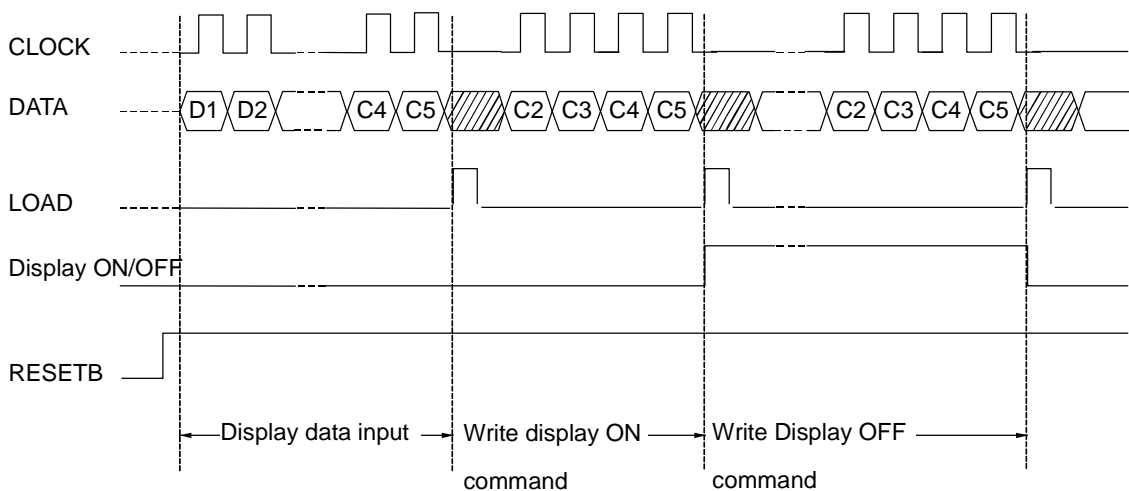
• Display data input

As described in the Data configuration section, the display data consists of the data field that corresponds to each segment on/off and the command field that indicates the display data input. When inputting the display data, the "F1" command is set in the command field. When the "F2" to "F5" command is set in the command field, the display data in the data field becomes invalid. The data input to the DATA pin is loaded to the shift register at the CLOCK pulse rise, transferred to the display data latch during the LOAD pulse at the "H" level, then output via the segment driver.



• Display on, Display off

The display becomes off at power-on reset. To display, write the display on command. The display off is the command that makes all segments off. Writing the display off command turns off the lights regardless of the display data. The display on is the command to release the display off. Writing the display on command returns the display to the original state.



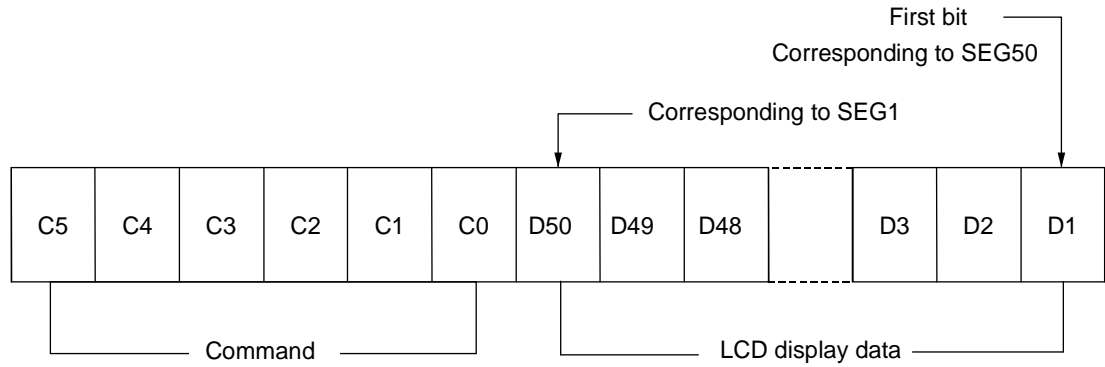
List of Commands

Command name	C5	C4	C3	C2	C1	C0	Operation
F0	0	0	0	x	x	x	Disabled
F1	0	0	1	Co1	Co0	x	Data write address setting (Co1,Co0)=(0, 0): Corresponding to common 1 (Co1,Co0)=(0, 1): Corresponding to common 2 (Co1,Co0)=(1, 0): Corresponding to common 3 (Co1,Co0)=(1, 1): Corresponding to common 4
F2	0	1	0	F2 (0)	F1 (0)	F0 (0)	Frame frequency setting (F2, F1, F0)=(0, 0, 0): 65Hz (F2, F1, F0)=(0, 0, 1): 75Hz (F2, F1, F0)=(0, 1, 0): 85Hz (F2, F1, F0)=(0, 1, 1): 95Hz (F2, F1, F0)=(1, 0, 0): 130Hz (F2, F1, F0)=(1, 0, 1): 150Hz (F2, F1, F0)=(1, 1, 0): 170Hz (F2, F1, F0)=(1, 1, 1): 190Hz (valid for Internal CR oscillation)
F3	0	1	1	BIAS (0)	WSEL (0)	x	LCD Bias setting BIAS="0" : 1/3-bias BIAS="1" : 1/2-bias LCD Driving Waveform setting WSEL="0" : A-Waveform WSEL="1" : B-Waveform
F4	1	0	0	D1 (0)	D0 (0)	x	Display Duty setting (D1, D0)=(0, 0): Static (COM1=COM2=COM3=COM4) (D1, D0)=(0, 1): 1/2-duty (COM1=COM3, COM2=COM4) (D1, D0)=(1, 0): 1/3-duty (COM2=COM4) (D1, D0)=(1, 1): 1/4-duty
F5	1	0	1	DSP (0)	x	x	Display on/off setting DSP="0" : Off (COM=SEG=GND) DSP="1" : On
F6	1	1	0	x	x	x	Disabled
F7	1	1	1	x	x	x	Disabled

x: Don't care
(): Reset Value

Data configuration

[Input data]



Note 1 : The commands F4 settings become valid when the least four bits of C2 to C5 are input.

(The bits from D1 to D50 and from C0 to C1 are not necessary.)

The commands F3 and F4 settings become valid when the least five bits of C1 to C5 are input.

(The bits from D1 to D50 and from C0 are not necessary.)

The commands F2 settings become valid when the least six bits of C0 to C5 are input.

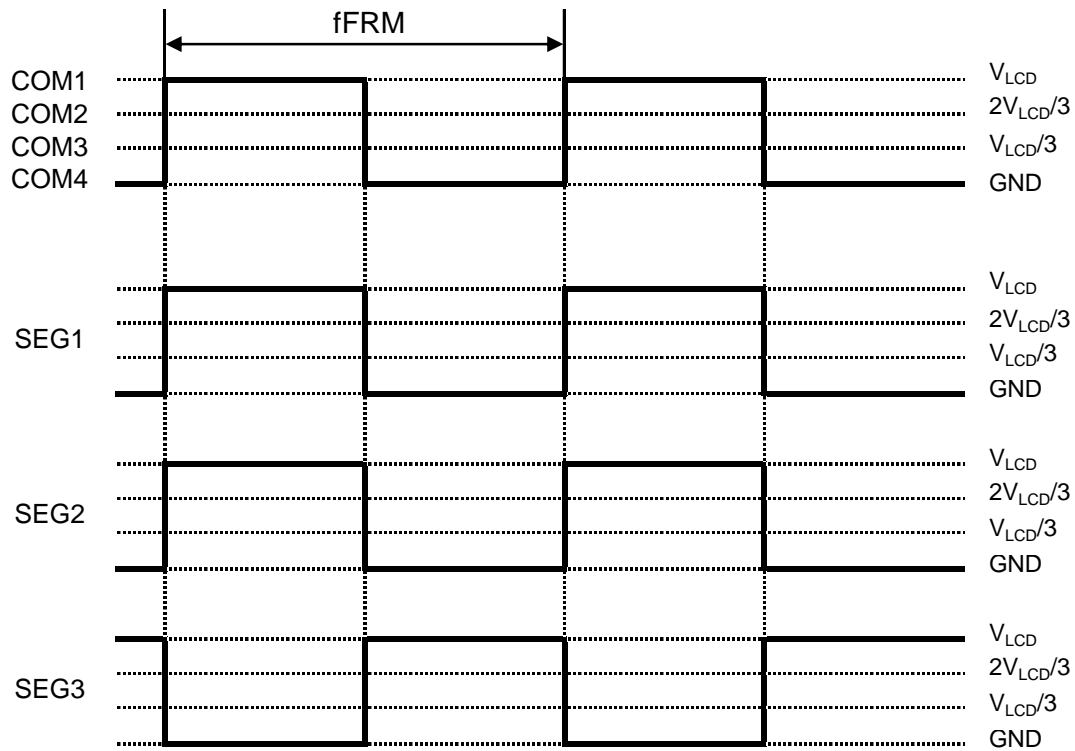
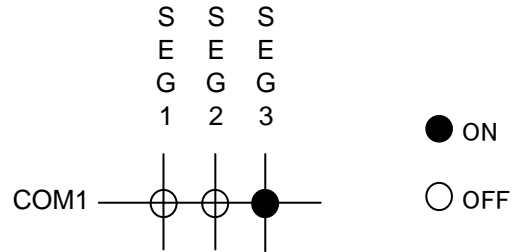
(The bits from D1 to D50 are not necessary.)

Note 2 : If the dummy bit is needed for the reason of number of transfer bits, put it on the first bit side.

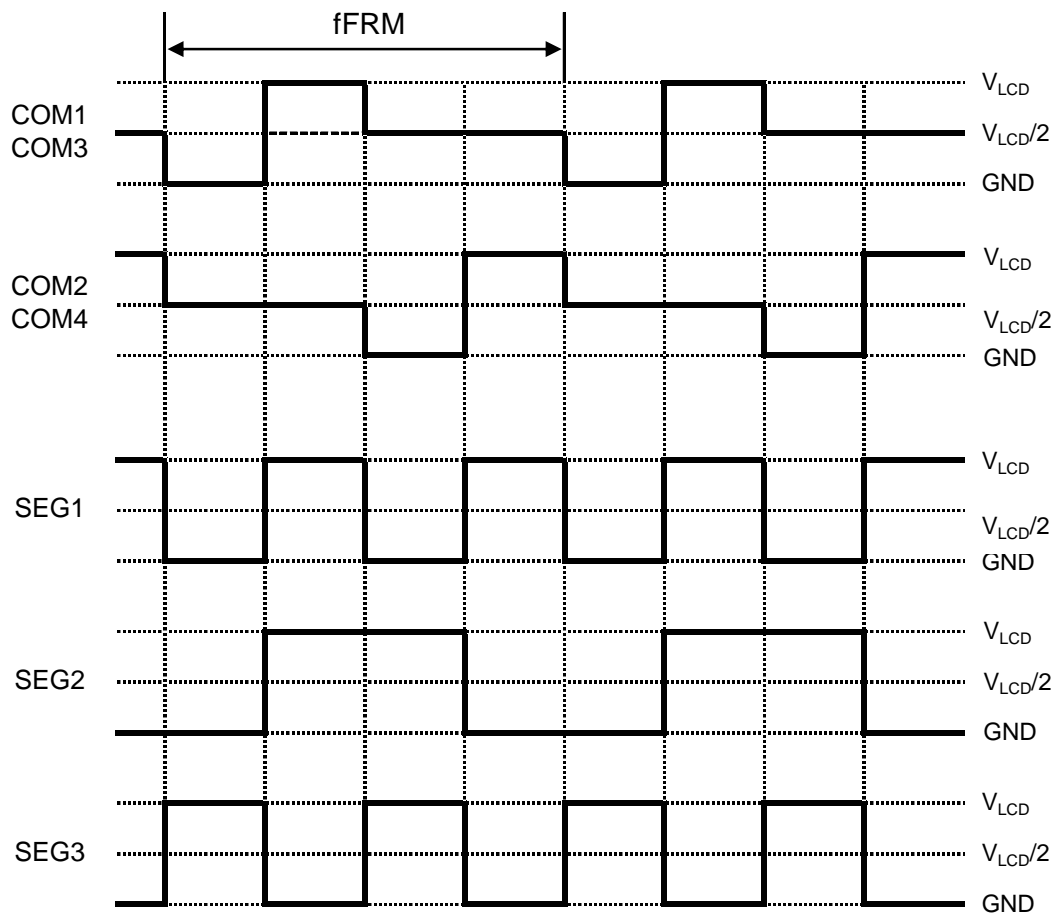
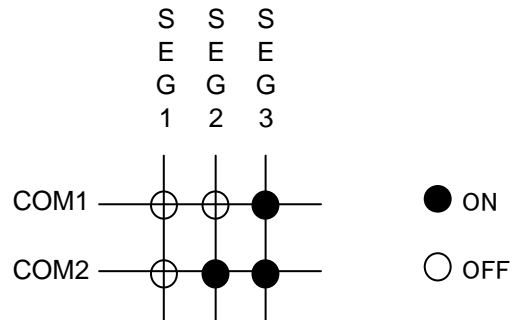
Note 3 : The command execution follows the contents of the C5 to C0 registers immediately before the LOAD becomes "H".

LCD Driving Waveform

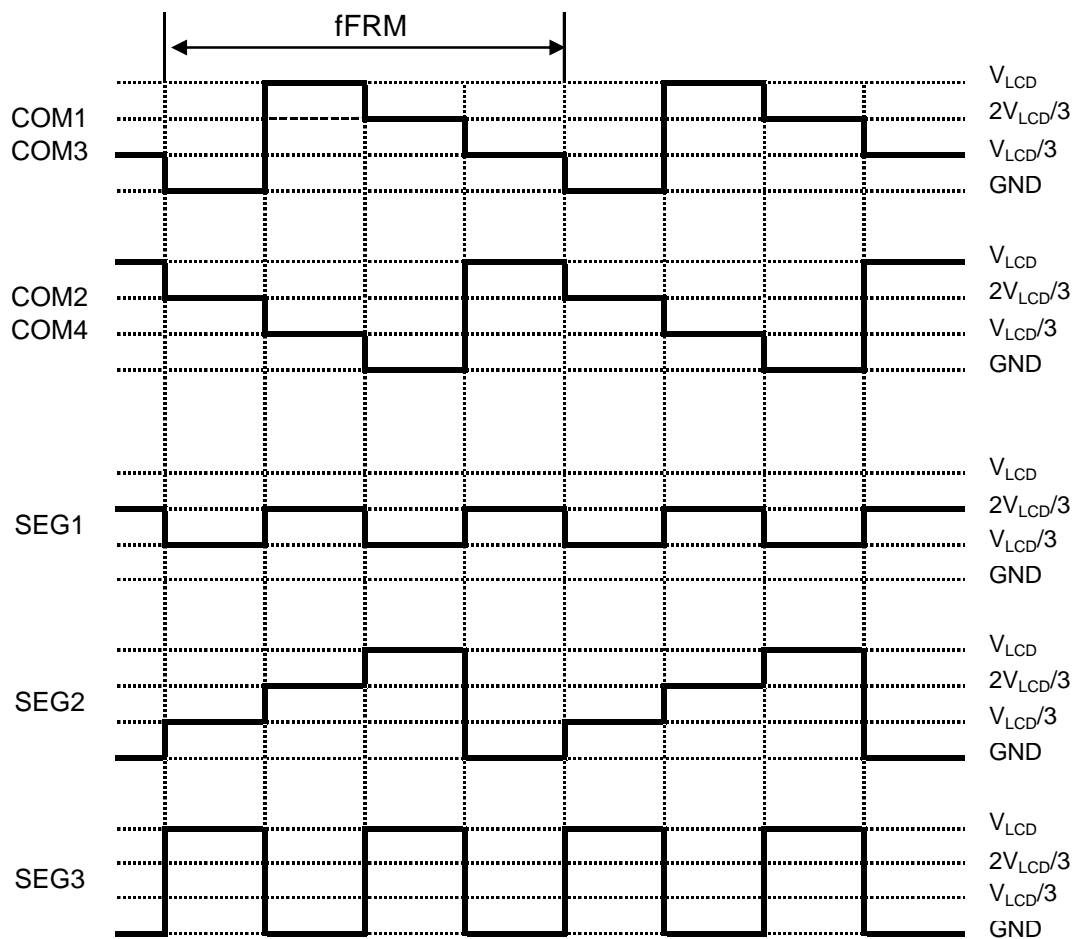
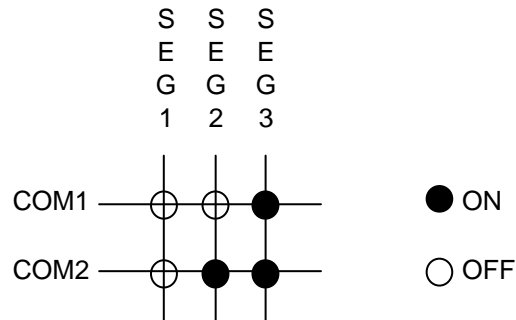
- Static mode (same as A-waveform and B-waveform)



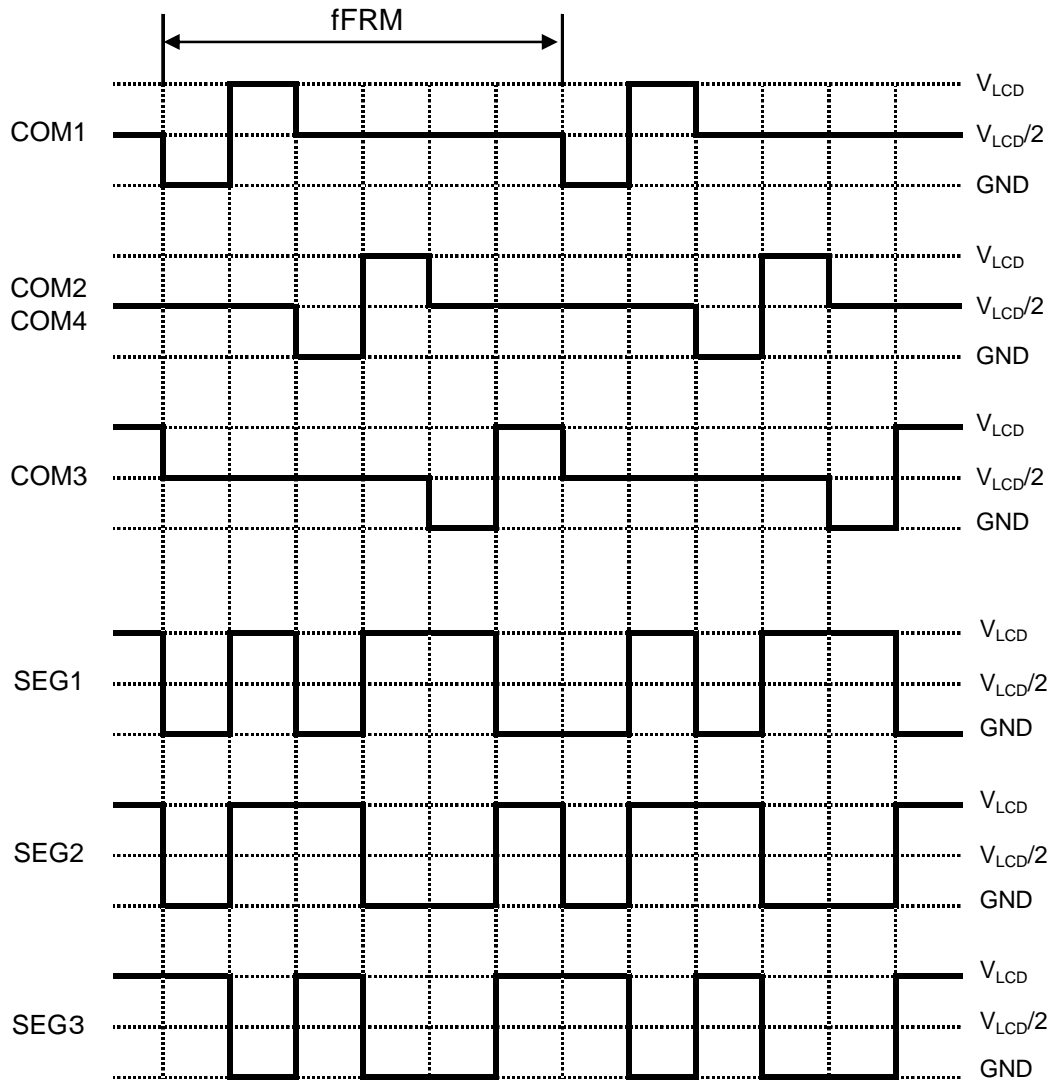
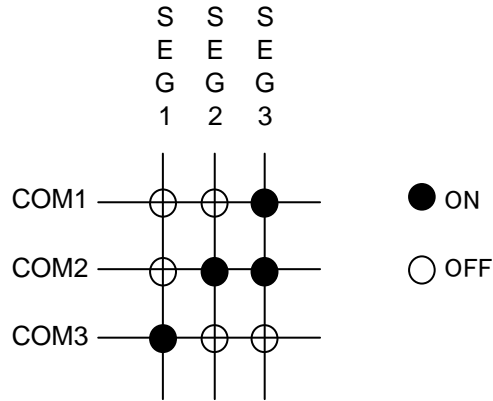
- 1/2-duty, 1/2-bias mode (A-waveform)



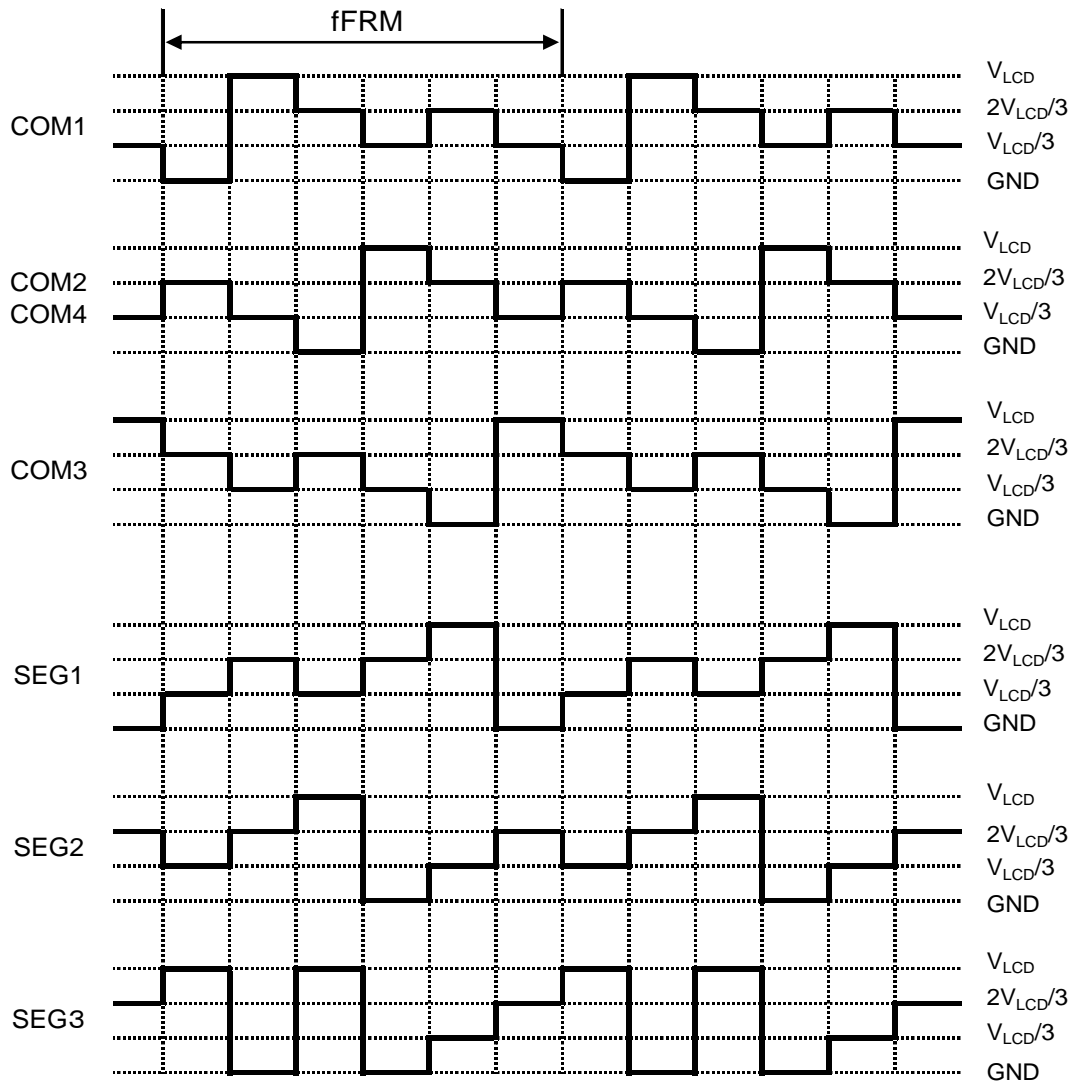
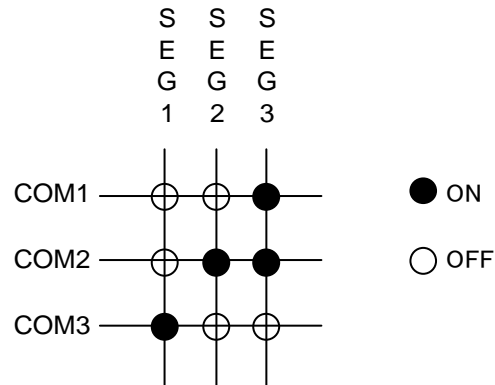
- 1/2-duty, 1/3-bias mode (A-waveform)



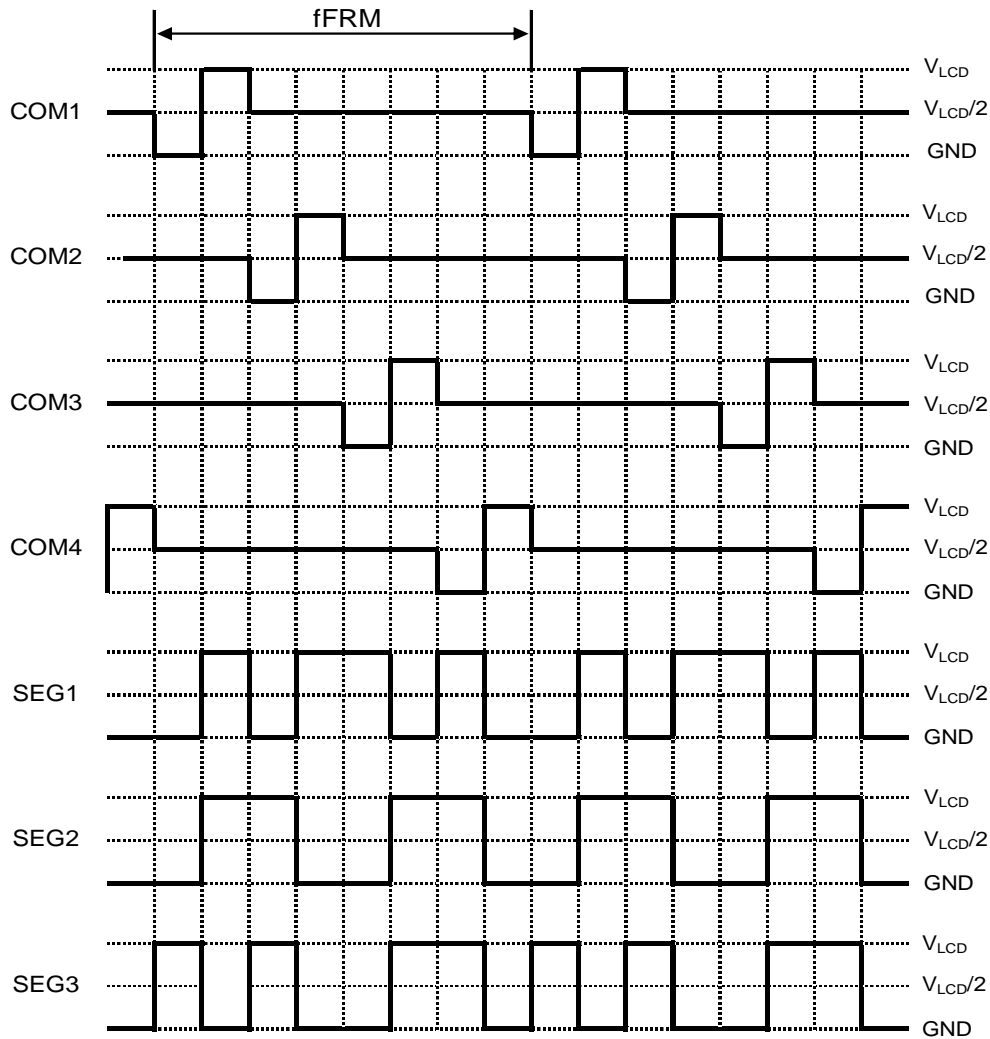
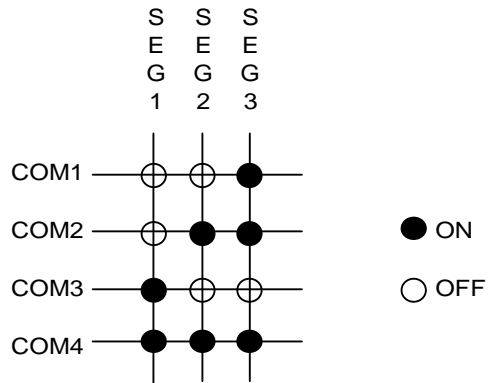
- 1/3-duty, 1/2-bias mode (A-waveform)



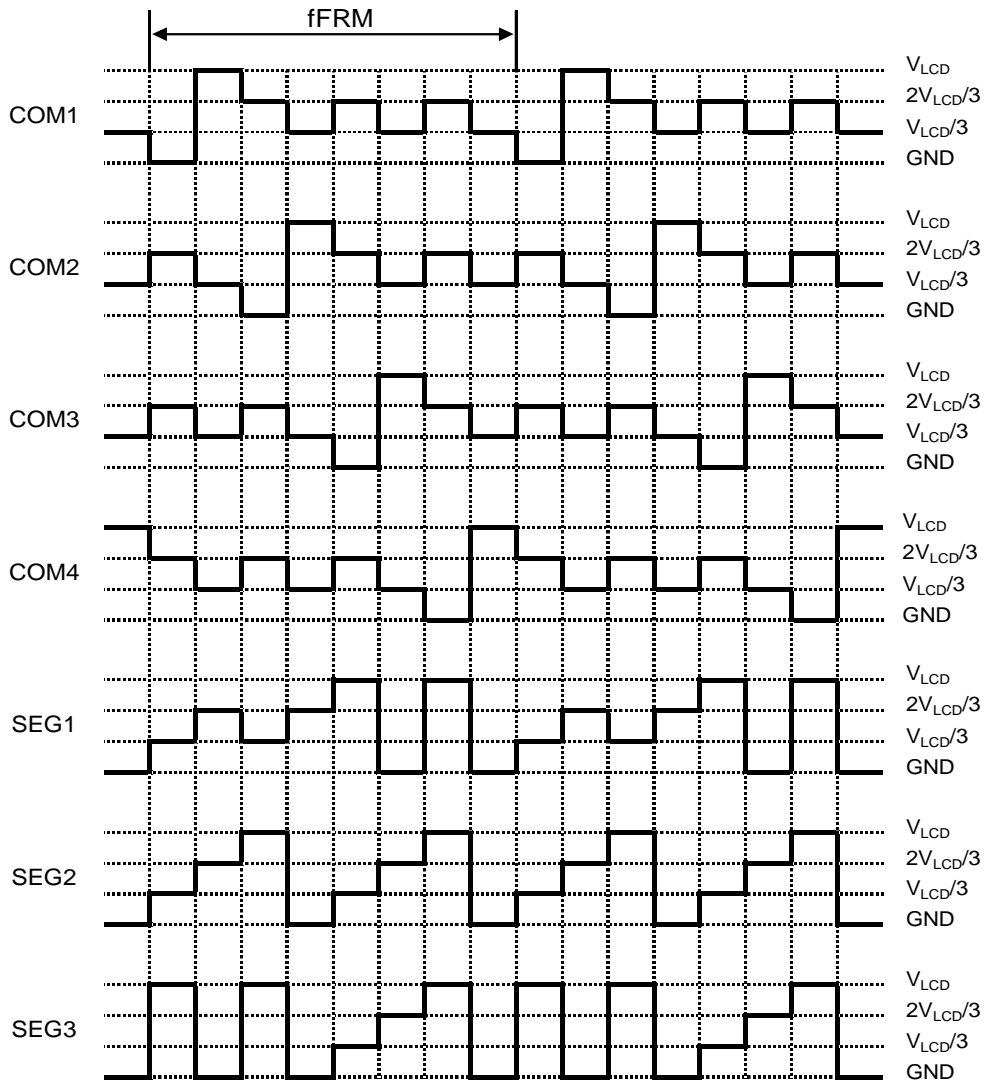
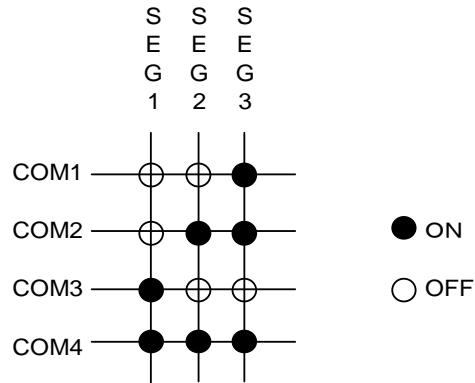
- 1/3-duty, 1/3-bias mode (A-waveform)



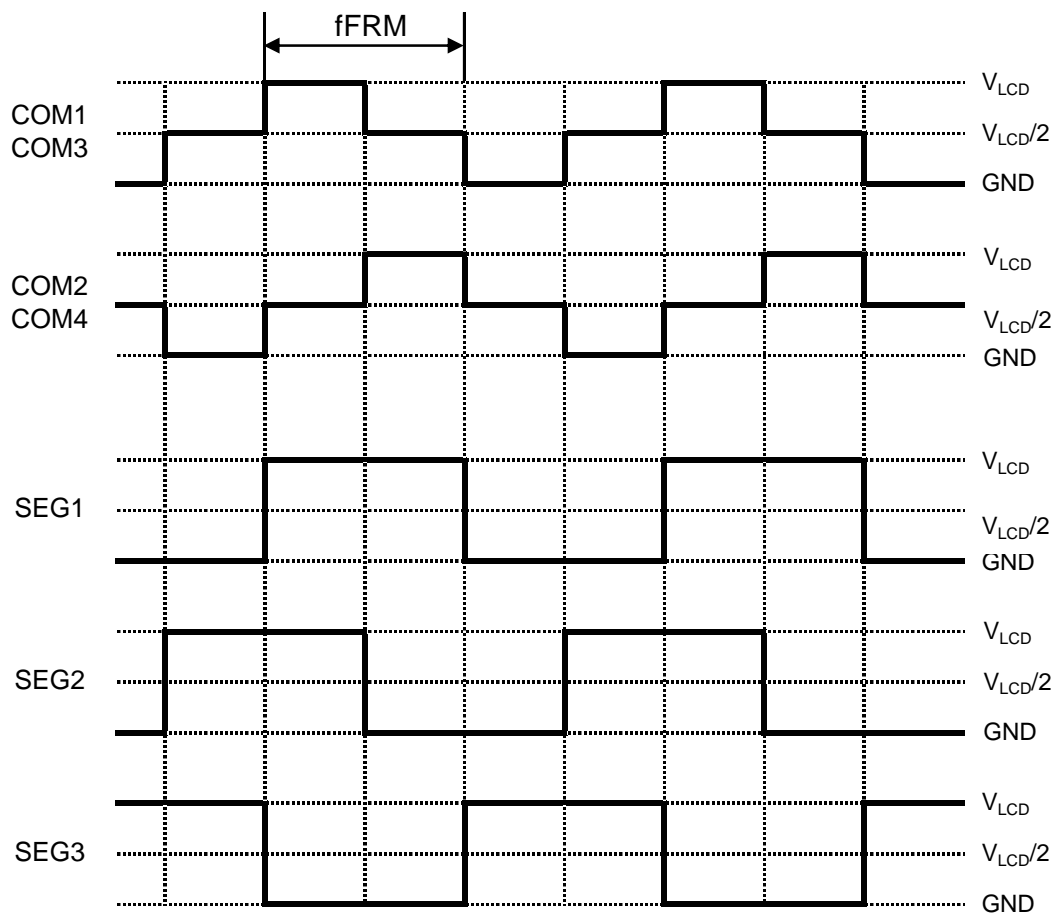
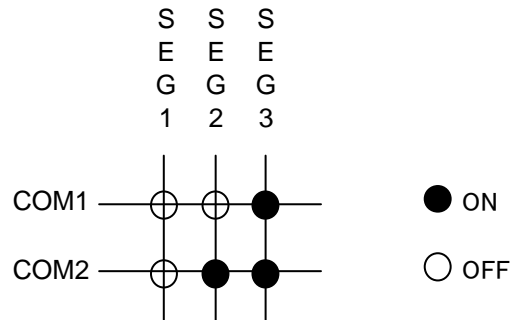
- 1/4-duty, 1/2-bias mode (A-waveform)



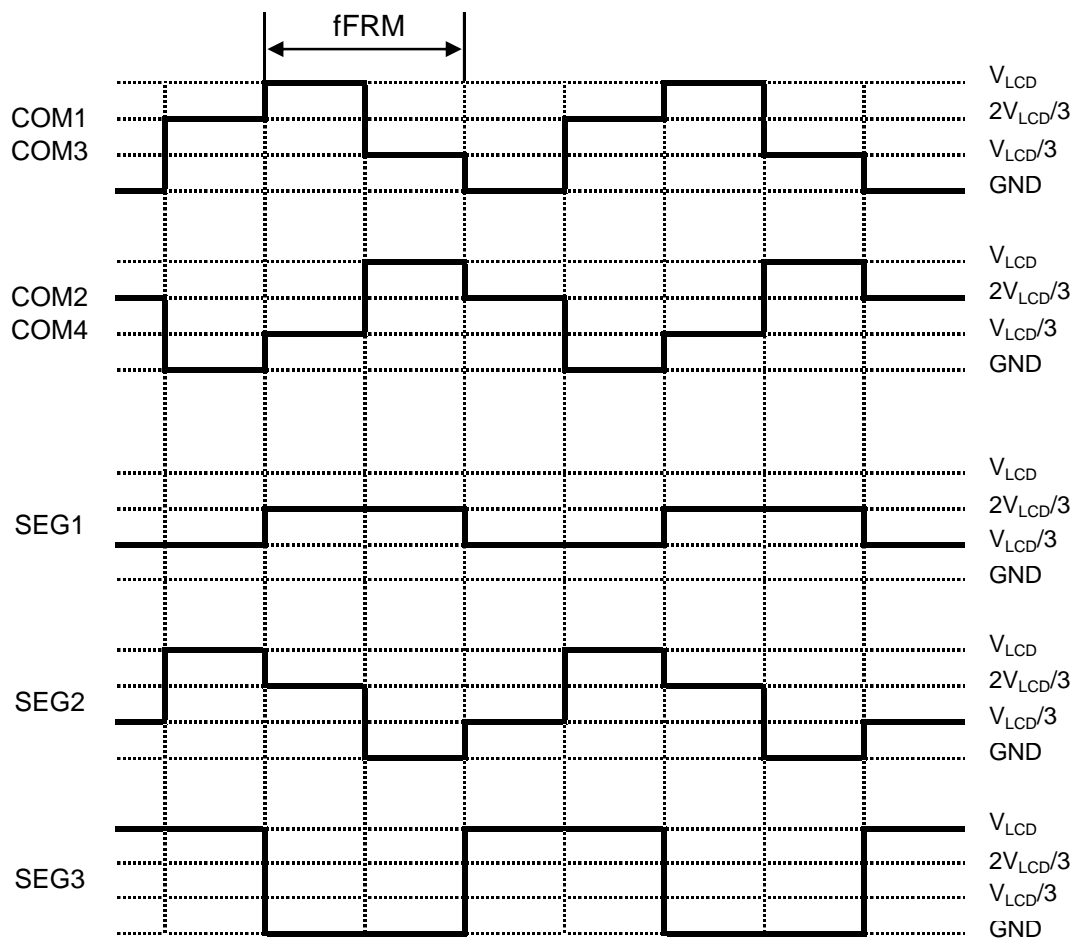
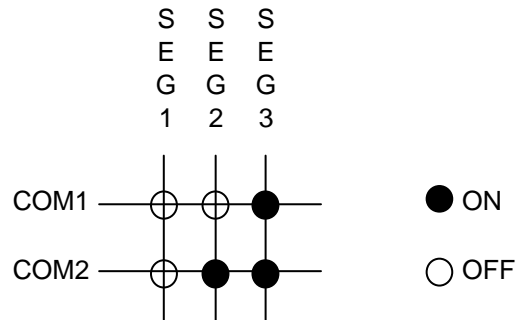
- 1/4-duty, 1/3-bias mode (A-waveform)



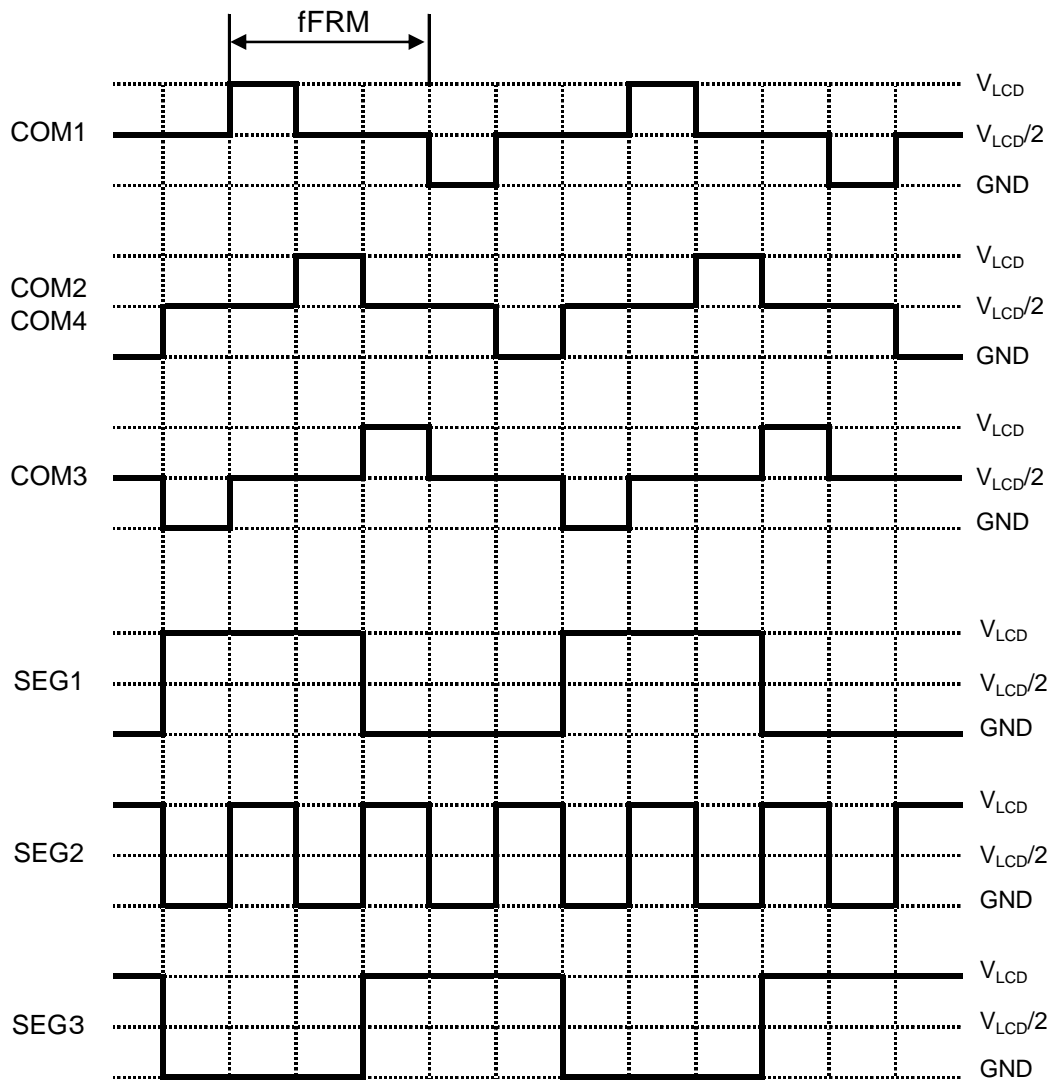
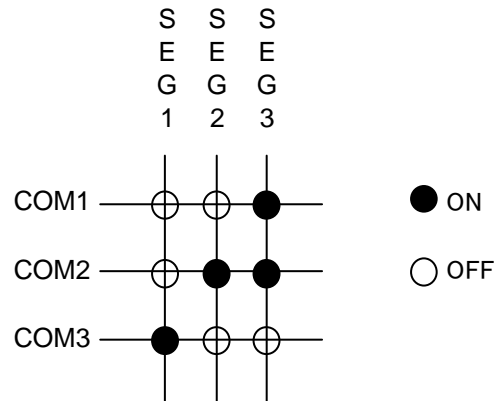
- 1/2-duty, 1/2-bias mode (B-waveform)



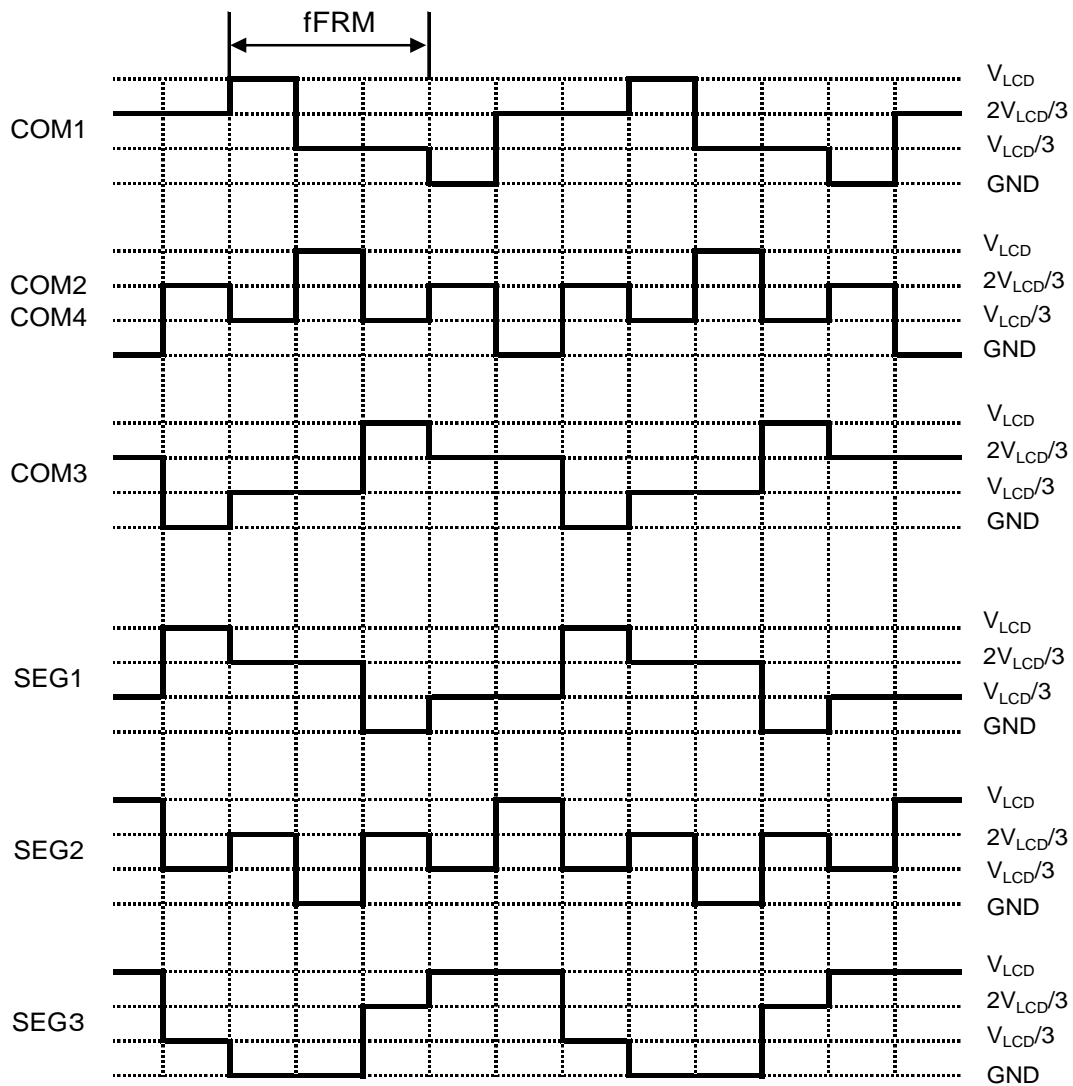
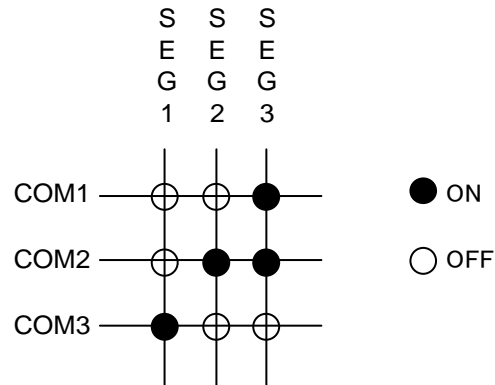
- 1/2-duty, 1/3-bias mode (B-waveform)



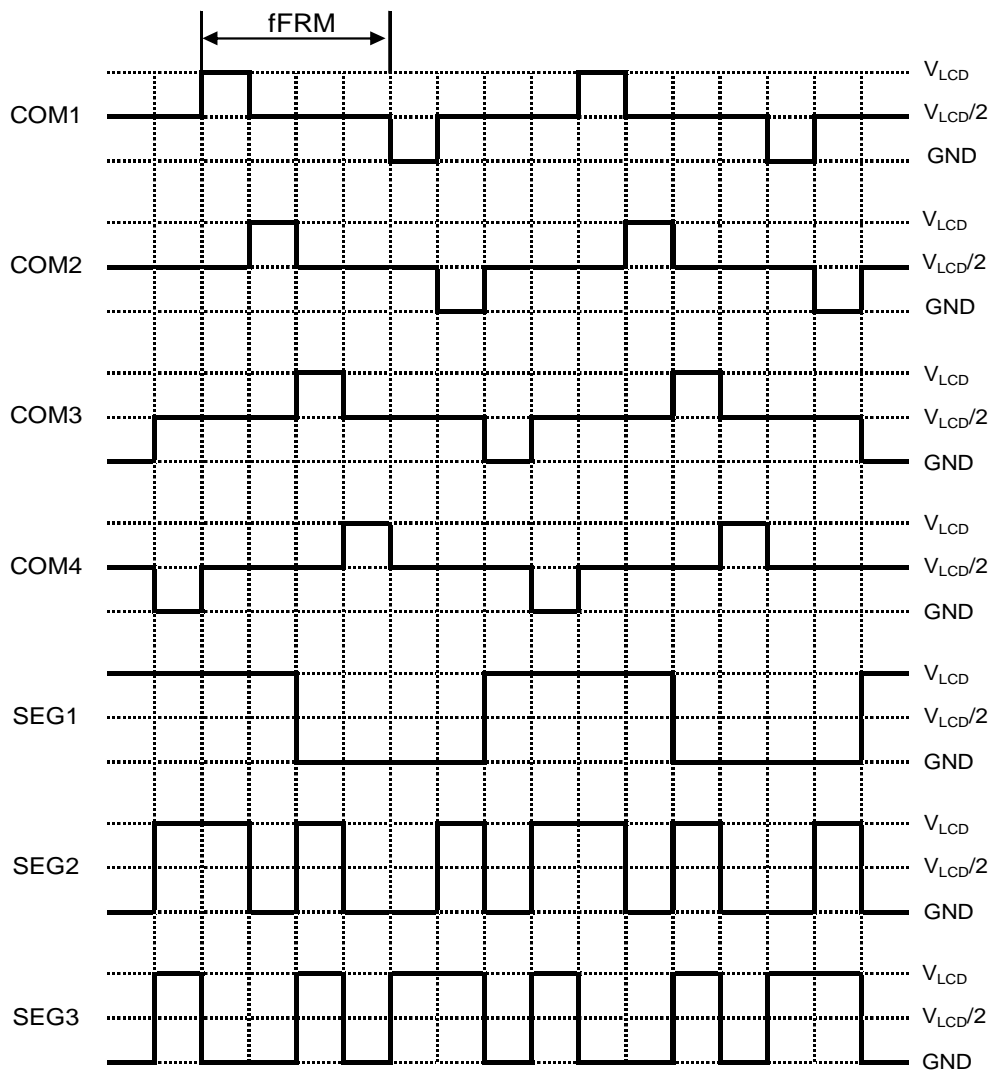
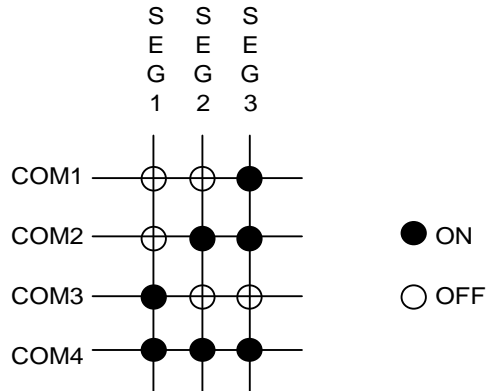
- 1/3-duty, 1/2-bias mode (B-waveform)



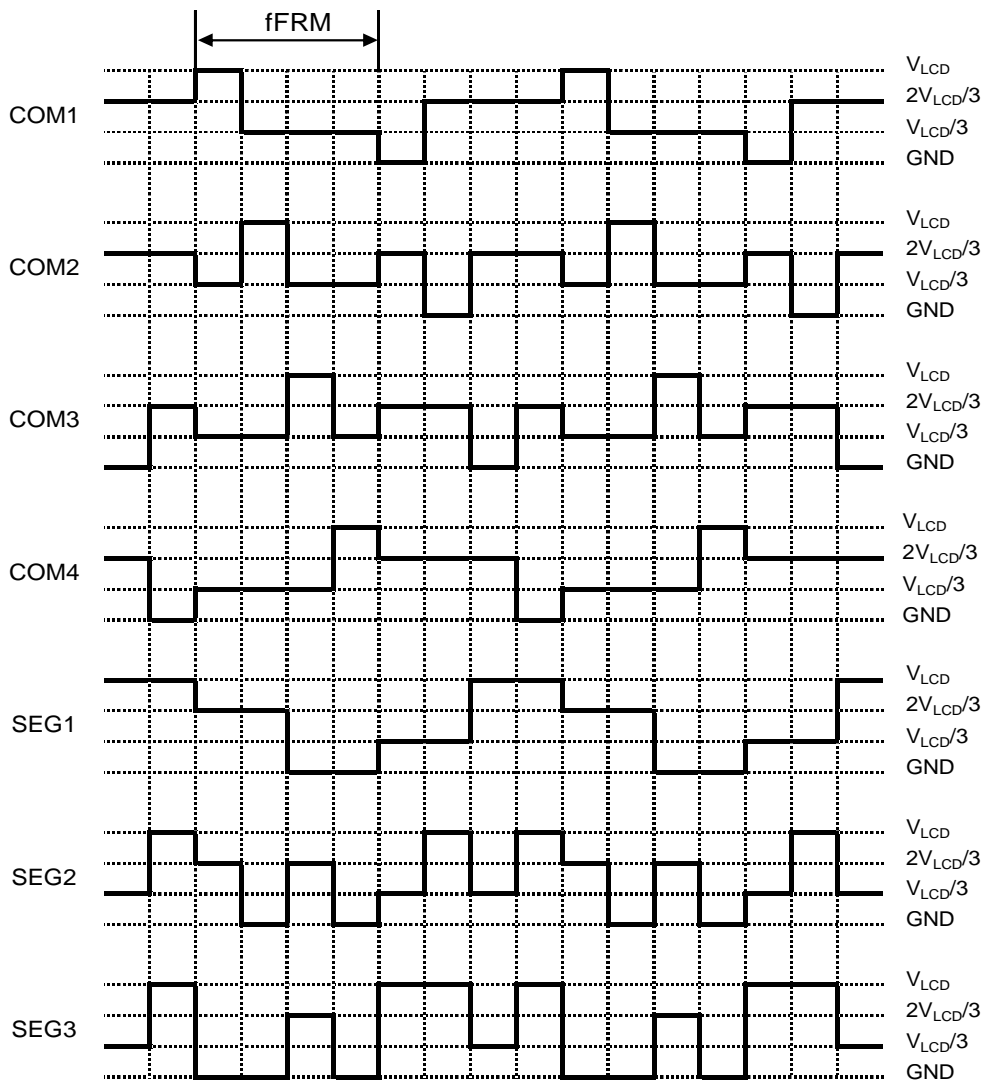
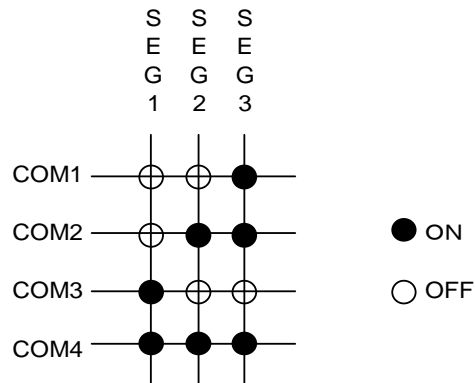
- 1/3-duty, 1/3-bias mode (B-waveform)



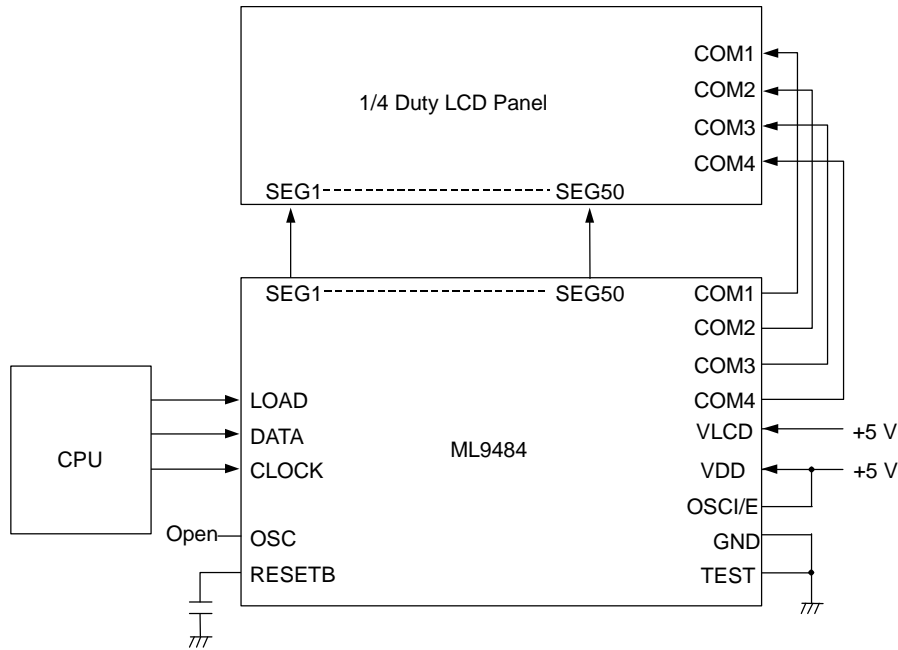
- 1/4-duty, 1/2-bias mode (B-waveform)



- 1/4-duty, 1/3-bias mode (B-waveform)



EXAMPLE OF APPLICATION CIRCUIT

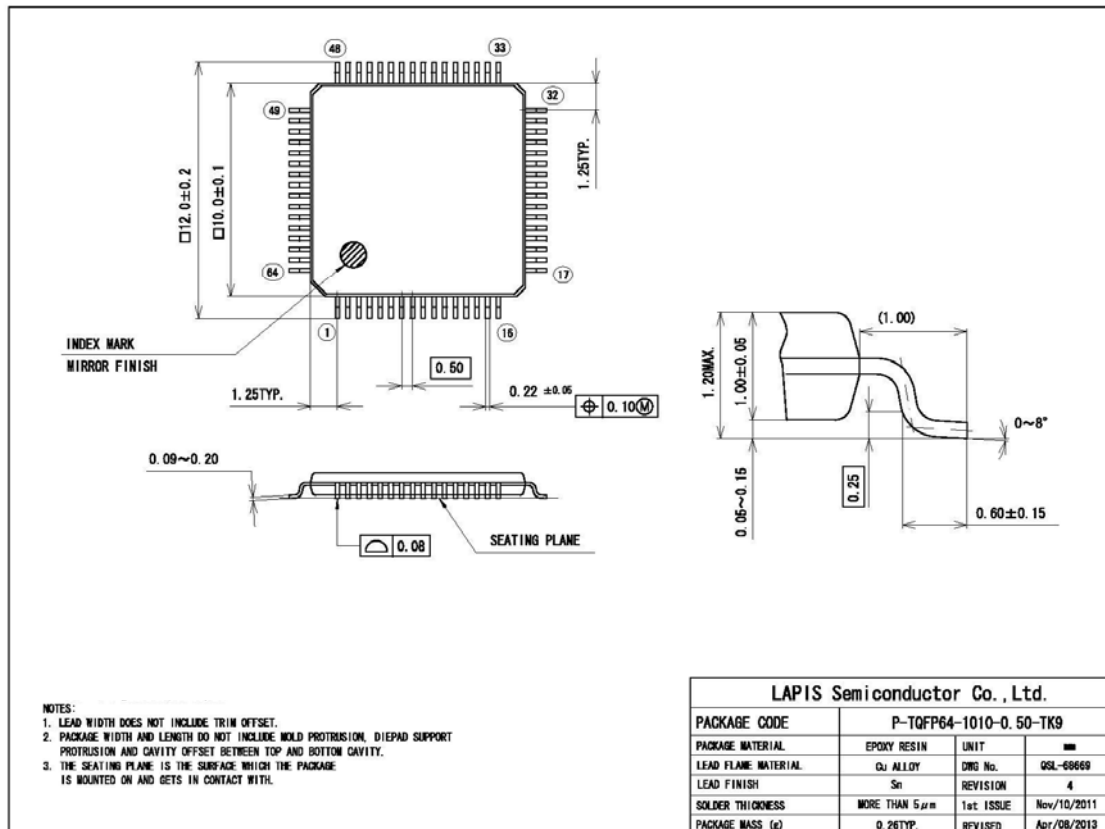


REFRESH

Although the ML9484 holds operation state by commands, excessive external noise might change the internal state.

On a chip-mounting and system level, it is necessary to take countermeasures against preventing noise from occurring. It is recommended to use the refresh sequence periodically to control sudden noise.

PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL9484-01	Dec .25, 2013	–	–	Final edition 1 issued

NOTES

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing. If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

Copyright 2013 LAPIS Semiconductor Co., Ltd.