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Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.

October 1, 2020

ML610Q426/ ML610426

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

This LSI is a high performance CMOS 8-bit microcontroller equipped with an 8-bit CPU nX-U8/100 and integrated with peripheral functions such as the synchronous serial port, UART, melody driver, RC oscillation type A/D converter, and LCD driver.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. Additionally, it adopts the low-/high-speed dual clock system, standby mode, and process that prohibits leak current at high temperatures, and is most suitable for battery-driven applications.

Flash version can rewrite programs on-board, which can contribute to reduction in product development TAT. The flash memory incorporated into this Flash version implements the mask ROM-equivalent low-voltage operation and low-power consumption, enabling volume production by the Flash version.

FEATURES

- CPU
 - 8-bit RISC CPU (CPU name: nX-U8/100)
 - Instruction system: 16-bit instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-Chip debug function
 - Minimum instruction execution time
 - 30.5 μ s (@32.768 kHz system clock)
 - 1.0 μ s (@1 MHz system clock)
- Internal memory
 - ML610Q426 :
 - Internal 40KByte Flash ROM (20K \times 16 bits) (including unusable 1KByte TEST area)
 - Internal 2KByte Data RAM (2048 \times 8 bits)
 - Internal 124-byte RAM for display
 - ML610426 :
 - Internal 40KByte MASK ROM (20K \times 16 bits) (including unusable 1KByte TEST area)
 - Internal 2KByte Data RAM (2048 \times 8 bits)
 - Internal 124-byte RAM for display
- Interrupt controller
 - ML610426, ML610Q426 :
 - 1 non-maskable interrupt sources (Internal source: 1)
 - 24 maskable interrupt sources (Internal sources: 19, External sources: 5) : ML610426/ML610Q426
 - 27 maskable interrupt sources (Internal sources: 19, External sources: 8) :-ML610Q426C
- Time base counter
 - Low-speed time base counter \times 1 channel
 - Frequency compensation (Compensation range: Approx. -488 ppm to $+488$ ppm.
 - Compensation accuracy: Approx. 0.48ppm)
 - High-speed time base counter \times 1 channel

- Watchdog timer
 - Non-maskable interrupt and reset
 - Free running
 - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)
- Timers
 - 8 bits × 4 channels (Timer0-3: 16-bit × 2 configuration available by using Timer0-1 or TimerI-J)
 - Clock frequency measurement mode (in one channel of 16-bit configuration using TimerI-J)
 - Continuous timer mode/One shot timer mode
 - Timer count start/stop by software and external trigger
- 1 kHz timer
 - 10 Hz/1 Hz interrupt function
- PWM
 - Resolution 16 bits × 1 channel
 - Continuous PWM mode/One shot PWM mode
 - PWM start/stop by software and external trigger
- Synchronous serial port
 - Master/slave selectable × 2 channel
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable
- UART
 - Half-Duplex Communication
 - TXD/RXD × 1 channel
 - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - Built-in baud rate generator
- I²C bus interface
 - Master function only
 - Standard mode (50 kbps@1MHz, 100kbps@1MHz)
- Melody driver
 - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
 - Tone length: 63 types
 - Tempo: 15 types
 - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)
- RC oscillation type A/D converter
 - 16-bit counter
 - Time division × 1.5 channels
- General-purpose ports
 - ML610Q426, ML610426 :
 - Input-only port: 5 channels
 - Input/output port: 7 channels (including secondary functions)
 - ML610Q426C :
 - Input-only port: 7 channels
 - Input/output port: 13 channels (including secondary functions)

- LCD driver
 - Number of segments^(*) and duty
 - ML610Q426/426: Up to 800 dots (select among 50seg x 16com, 51seg x 15com, 52seg x 14com, 53seg x 13com, 54seg x 12com, 55seg x 11com, 56seg x 10com, 57seg x 9com, 58seg x 8com, 59seg x 7com, 60seg x 6com, 61seg x 5com, and 62seg x 4com), 1/1 to 1/16 duty
 - ML610Q426C: Up to 672 dots (select among 42seg x 16com, 43seg x 15com, 44seg x 14com, 45seg x 13com, 46seg x 12com, 47seg x 11com, 48seg x 10com, 49seg x 9com, 50seg x 8com, 51seg x 7com, 52seg x 6com, 53seg x 5com, and 54seg x 4com), 1/1 to 1/16 duty
 - 1/2, 1/3, 1/4 bias (built-in bias generation circuit)
 - 1/1 bias (LED mode)
 - Frame frequency selectable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
 - Bias voltage multiplying clock selectable (8 types)
 - Contrast adjustment (1/1 bias, 1/2 bias, 1/3 bias: 16 steps, 1/4 bias: 10 steps)
 - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
- ^(*) 8 segment pins are changed to general purpose port by mask option.
- EL driver
 - pumping clock signal and discharge pulse signal output for the back light of LCD panel and minimum external components
- Reset
 - Reset by the RESET_N pin
 - Reset by power-on detection
 - Reset by the watchdog timer (WDT) 2nd overflow
- Power supply voltage detect function
 - Judgment voltages: One of 16 levels
 - Judgment accuracy: $\pm 2\%$ (Typ.)
 - Input channels: Operating voltage(V_{DD}) or 1 external input
- Clock
 - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
Crystal oscillation (32.768 kHz)
 - High-speed clock:
Built-in RC oscillation (1MHz)
- Power management
 - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
 - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
 - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
- Guaranteed operating range
 - Operating temperature: -20°C to 70°C
 - Operating voltage: $V_{DD} = 1.1\text{V}$ to 3.6V

• Product name – Supported Function

The line-up of the ML610Q426 and the ML610426 is below.

- Chip (Die) -	ROM type	Operating temperature	LCD driver Number of segment	Product availability
ML610Q426-xxxWA	Flash ROM	-20°C to +70°C	Up to 800 dots	Yes
ML610Q426P-xxxWA	Flash ROM	-40°C to +85°C	Up to 800 dots	-
ML610Q426C-xxxWA	Flash ROM	-20°C to +70°C	Up to 672 dots	Yes
ML610Q426PC-xxxWA	Flash ROM	-40°C to +85°C	Up to 672 dots	-
ML610426-xxxWA	Mask ROM	-20°C to +70°C	Up to 800 dots	Yes
ML610426P-xxxWA	Mask ROM	-40°C to +85°C	Up to 800 dots	-
ML610426C-xxxWA	Mask ROM	-20°C to +70°C	Up to 672 dots	-
ML610426PC-xxxWA	Mask ROM	-40°C to +85°C	Up to 672 dots	-

-100-pin plastic TQFP -	ROM type	Operating temperature	LCD driver Number of segment	Product availability
ML610Q426-xxxTB	Flash ROM	-20°C to +70°C	Up to 800 dots	-
ML610Q426P-xxxTB	Flash ROM	-40°C to +85°C	Up to 800 dots	-
ML610Q426C-xxxTB	Flash ROM	-20°C to +70°C	Up to 672 dots	-
ML610Q426PC-xxxTB	Flash ROM	-40°C to +85°C	Up to 672 dots	-
ML610426-xxxTB	Mask ROM	-20°C to +70°C	Up to 800 dots	-
ML610426P-xxxTB	Mask ROM	-40°C to +85°C	Up to 800 dots	-
ML610426C-xxxTB	Mask ROM	-20°C to +70°C	Up to 672 dots	-
ML610426PC-xxxTB	Mask ROM	-40°C to +85°C	Up to 672 dots	-

xxx: ROM code number (xxx of the blank product is NNN)

Q: Flash ROM version

P: Wide range temperature version (P version)

C: larger I/O and less LCD segment pin version by mask option (C version)

WA: Chip (Die),

TB: TQFP

BLOCK DIAGRAM**ML610Q426/ML610426 Block Diagram**

Figure 1 shows the block diagram of the ML610Q426.

"*" indicates the secondary function of each port.

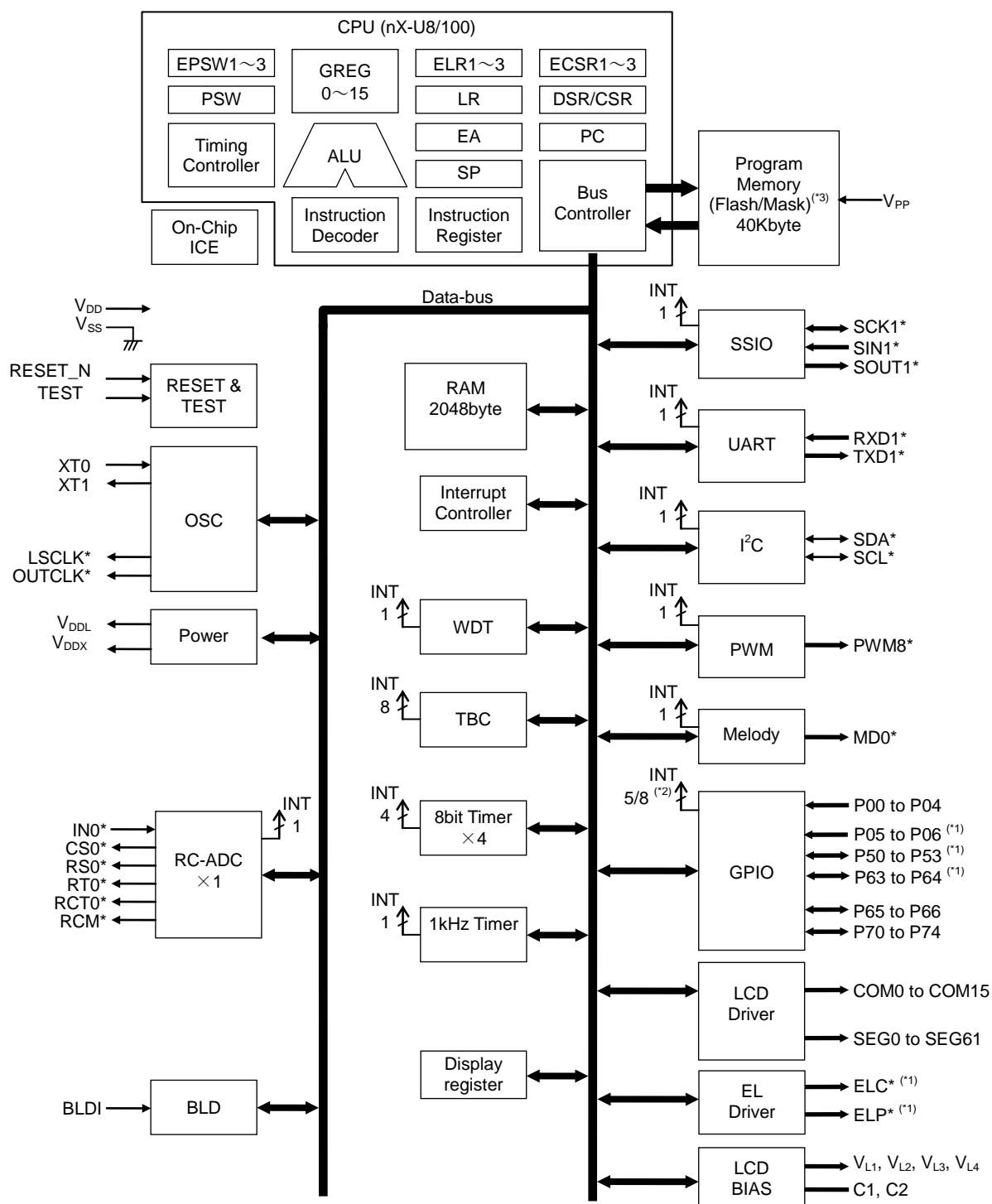


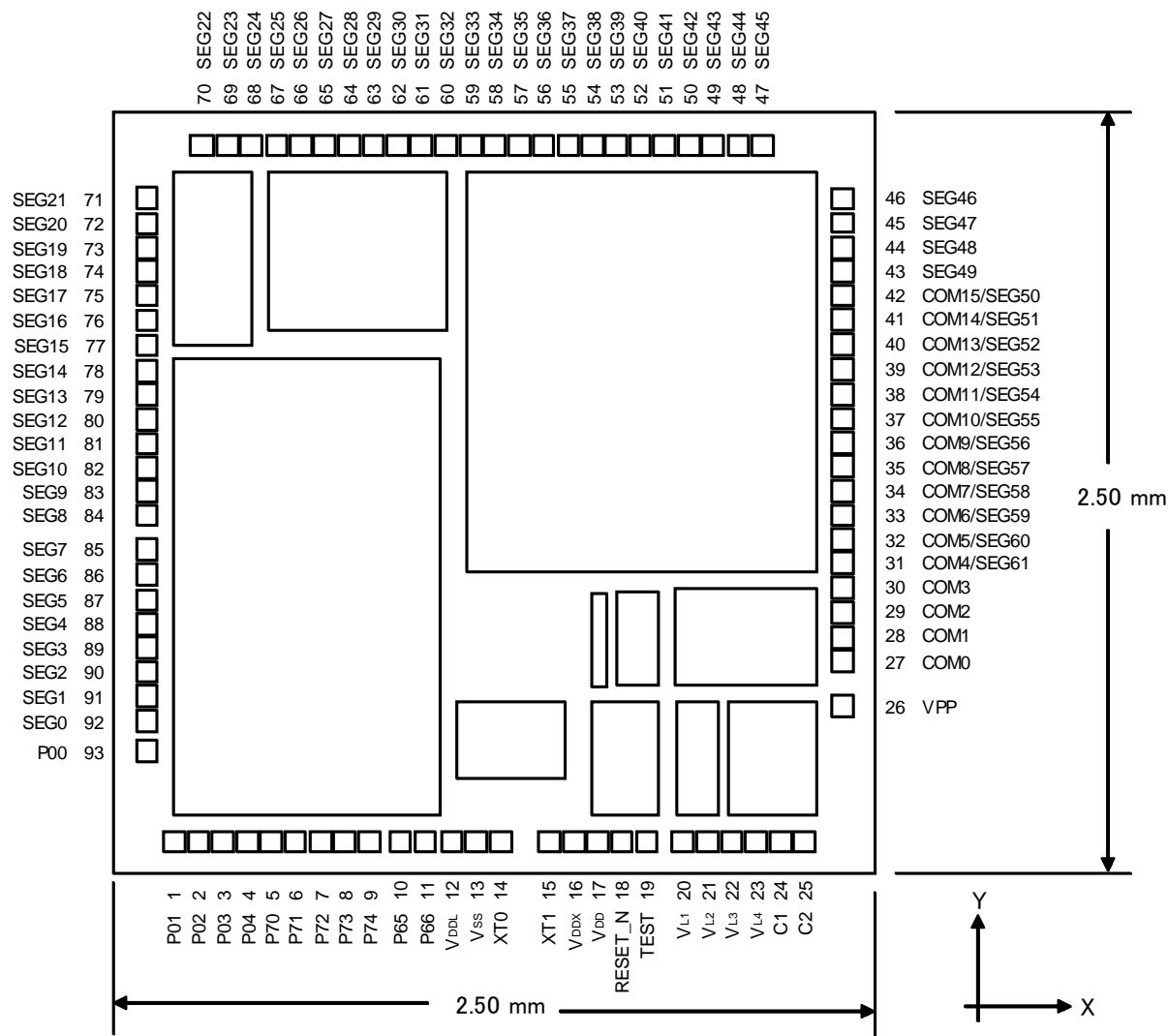
Figure 1 ML610Q426 Block Diagram

(*) SEG0-7 are changed to these pins by mask option (only ML610Q426)

(*) SEG0-7 to I/O change by mask option increases from 5 interrupts to 8 interrupts (only ML610Q426)

(*) Flash ROM version : ML610Q426, Mask ROM version : ML610426.

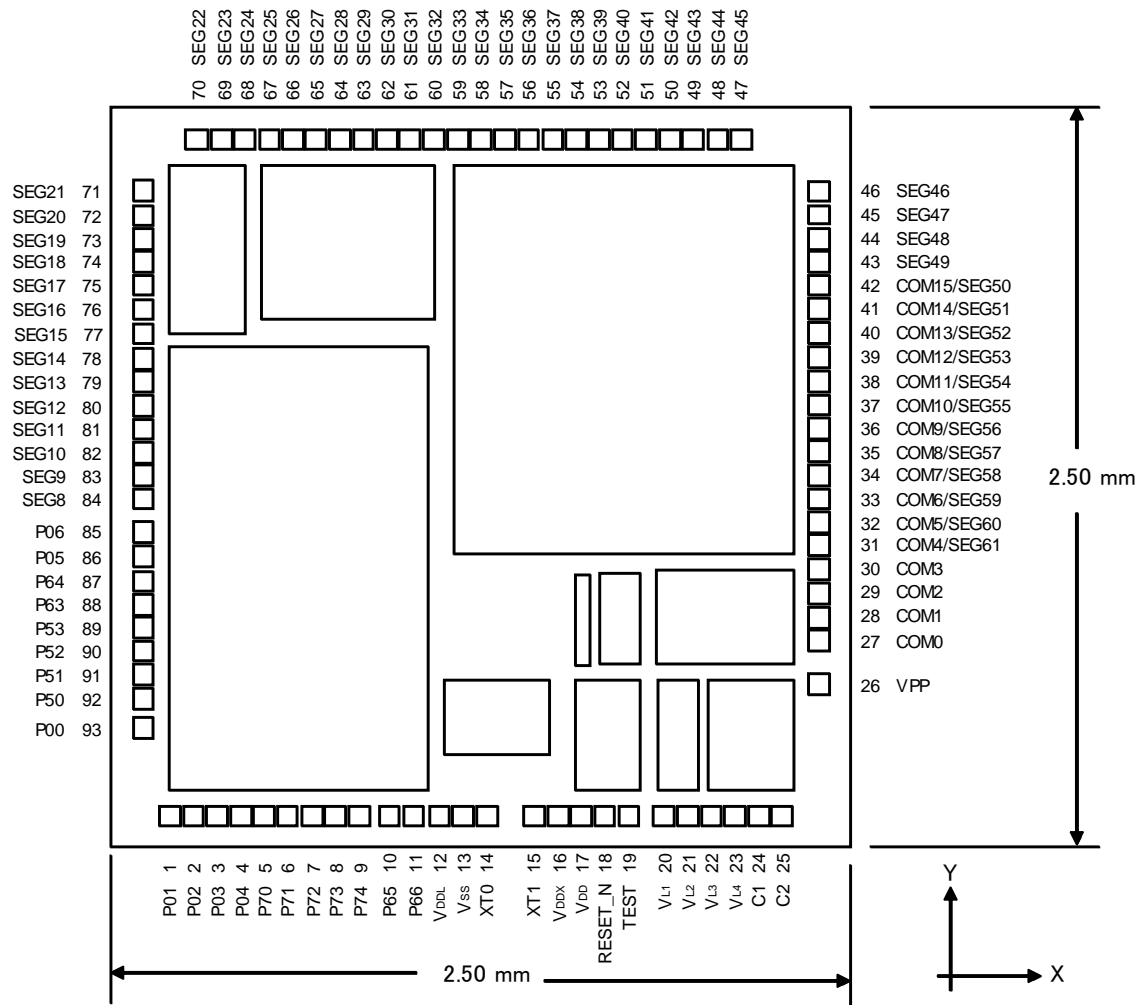
ML610Q426 Chip Dimension



Chip size: 2.50mm x 2.50mm
PAD count: 93 pins
Minimum PAD pitch: 80 μ m
PAD aperture: 70 μ m x 70 μ m
Chip thickness: 350 μ m
Voltage of the rear side of chip: V_{SS} level

Figure 2 ML610Q426 Chip Dimension

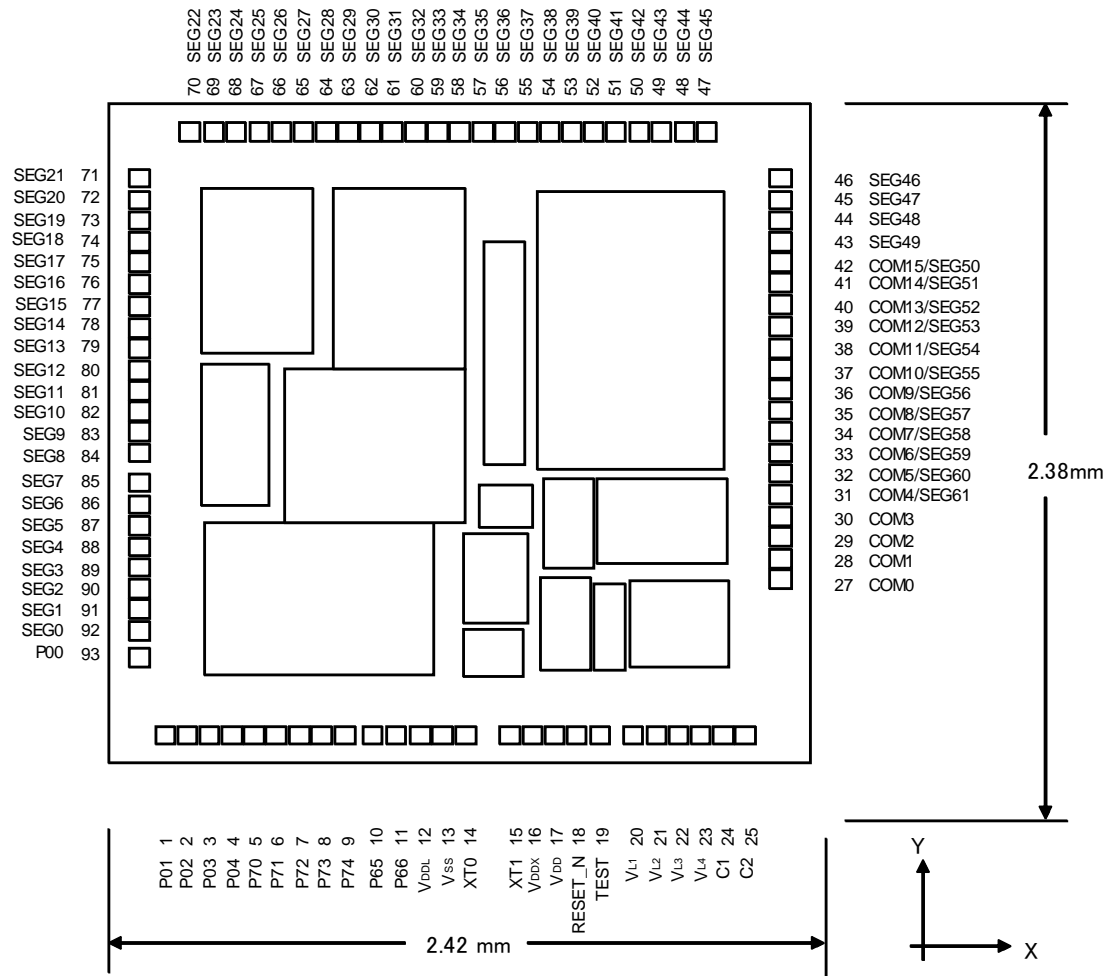
ML610Q426C Chip Dimension



Chip size:	2.50 mm × 2.50 mm
PAD count:	93 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V _{SS} level

Figure 3 ML610Q426C Chip Dimension

ML610426 Chip Dimension



Chip size:	2.42mm × 2.38mm
PAD count:	92 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V _{SS} level

Figure 4 ML610426 Chip Dimension

ML610Q426/ML610Q426C Pad Coordinates

Table 1 Pad Coordinates of ML610Q426/ML610Q426C

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	P01	-1055	-1144	51	SEG41	560	1144
2	P02	-975	-1144	52	SEG40	480	1144
3	P03	-895	-1144	53	SEG39	400	1144
4	P04	-815	-1144	54	SEG38	320	1144
5	P70	-735	-1144	55	SEG37	240	1144
6	P71	-655	-1144	56	SEG36	160	1144
7	P72	-575	-1144	57	SEG35	80	1144
8	P73	-495	-1144	58	SEG34	0	1144
9	P74	-415	-1144	59	SEG33	-80	1144
10	P65	-310	-1144	60	SEG32	-160	1144
11	P66	-230	-1144	61	SEG31	-240	1144
12	VDDL	-140	-1144	62	SEG30	-320	1144
13	VSS	-60	-1144	63	SEG29	-400	1144
14	XT0	20	-1144	64	SEG28	-480	1144
15	XT1	180	-1144	65	SEG27	-560	1144
16	VDDX	260	-1144	66	SEG26	-640	1144
17	VDD	340	-1144	67	SEG25	-720	1144
18	RESET_N	420	-1144	68	SEG24	-800	1144
19	TEST	500	-1144	69	SEG23	-880	1144
20	VL1	620	-1144	70	SEG22	-960	1144
21	VL2	700	-1144	71	SEG21	-1144	970
22	VL3	780	-1144	72	SEG20	-1144	890
23	VL4	860	-1144	73	SEG19	-1144	810
24	C1	940	-1144	74	SEG18	-1144	730
25	C2	1020	-1144	75	SEG17	-1144	650
26	VPP	1144	-700	76	SEG16	-1144	570
27	COM0	1144	-550	77	SEG15	-1144	490
28	COM1	1144	-470	78	SEG14	-1144	410
29	COM2	1144	-390	79	SEG13	-1144	330
30	COM3	1144	-310	80	SEG12	-1144	250
31	COM4/SEG61	1144	-230	81	SEG11	-1144	170
32	COM5/SEG60	1144	-150	82	SEG10	-1144	90
33	COM6/SEG59	1144	-70	83	SEG9	-1144	10
34	COM7/SEG58	1144	10	84	SEG8	-1144	-70
35	COM8/SEG57	1144	90	85	SEG7 ⁽¹⁾	-1144	-187
36	COM9/SEG56	1144	170		P06 ⁽²⁾		
37	COM10/SEG55	1144	250	86	SEG6 ⁽¹⁾	-1144	-267
38	COM11/SEG54	1144	330		P05 ⁽²⁾		
39	COM12/SEG53	1144	410	87	SEG5 ⁽¹⁾	-1144	-347
40	COM13/SEG52	1144	490		P64 ⁽²⁾		
41	COM14/SEG51	1144	570	88	SEG4 ⁽¹⁾	-1144	-427
42	COM15/SEG50	1144	650		P63 ⁽²⁾		
43	SEG49	1144	730	89	SEG3 ⁽¹⁾	-1144	-507
44	SEG48	1144	810		P53 ⁽²⁾		
45	SEG47	1144	890	90	SEG2 ⁽¹⁾	-1144	-587
46	SEG46	1144	970		P52 ⁽²⁾		
47	SEG45	880	1144	91	SEG1 ⁽¹⁾	-1144	-667
48	SEG44	800	1144		P51 ⁽²⁾		
49	SEG43	720	1144	92	SEG0 ⁽¹⁾	-1144	-747
50	SEG42	640	1144		P50 ⁽²⁾		
				93	p00	-1144	-847

(*1) Pad for ML610Q426 (*2) Pad for ML610Q426C

ML610426 Pad Coordinates

Table 2 Pad Coordinates of ML610426

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (μm)	Y (μm)	PAD No.	Pad Name	X (μm)	Y (μm)
1	P01	-1055	-1084	51	SEG41	618	1084
2	P02	-975	-1084	52	SEG40	538	1084
3	P03	-895	-1084	53	SEG39	458	1084
4	P04	-815	-1084	54	SEG38	378	1084
5	P70	-735	-1084	55	SEG37	298	1084
6	P71	-655	-1084	56	SEG36	218	1084
7	P72	-575	-1084	57	SEG35	138	1084
8	P73	-495	-1084	58	SEG34	58	1084
9	P74	-415	-1084	59	SEG33	-22	1084
10	P65	-310	-1084	60	SEG32	-102	1084
11	P66	-230	-1084	61	SEG31	-182	1084
12	VDDL	-140	-1084	62	SEG30	-262	1084
13	VSS	-60	-1084	63	SEG29	-342	1084
14	XT0	20	-1084	64	SEG28	-422	1084
15	XT1	180	-1084	65	SEG27	-502	1084
16	VDDX	260	-1084	66	SEG26	-582	1084
17	VDD	340	-1084	67	SEG25	-662	1084
18	RESET_N	420	-1084	68	SEG24	-742	1084
19	TEST	500	-1084	69	SEG23	-822	1084
20	VL1	620	-1084	70	SEG22	-902	1084
21	VL2	700	-1084	71	SEG21	-1104	980
22	VL3	780	-1084	72	SEG20	-1104	900
23	VL4	860	-1084	73	SEG19	-1104	820
24	C1	940	-1084	74	SEG18	-1104	740
25	C2	1020	-1084	75	SEG17	-1104	660
26	(No pin)	-	-	76	SEG16	-1104	580
27	COM0	1104	-630	77	SEG15	-1104	500
28	COM1	1104	-550	78	SEG14	-1104	420
29	COM2	1104	-470	79	SEG13	-1104	340
30	COM3	1104	-390	80	SEG12	-1104	260
31	COM4/SEG61	1104	-310	81	SEG11	-1104	180
32	COM5/SEG60	1104	-230	82	SEG10	-1104	100
33	COM6/SEG59	1104	-150	83	SEG9	-1104	20
34	COM7/SEG58	1104	-70	84	SEG8	-1104	-60
35	COM8/SEG57	1104	10	85	SEG7	-1104	-177
36	COM9/SEG56	1104	90				
37	COM10/SEG55	1104	170	86	SEG6	-1104	-257
38	COM11/SEG54	1104	250		P05		
39	COM12/SEG53	1104	330	87	SEG5	-1104	-337
40	COM13/SEG52	1104	410				
41	COM14/SEG51	1104	490	88	SEG4	-1104	-417
42	COM15/SEG50	1104	570				
43	SEG49	1104	650	89	SEG3	-1104	-497
44	SEG48	1104	730				
45	SEG47	1104	810	90	SEG2	-1104	-577
46	SEG46	1104	890				
47	SEG45	938	1084	91	SEG1	-1104	-657
48	SEG44	858	1084				
49	SEG43	778	1084	92	SEG0	-1104	-737
50	SEG42	698	1084				
				93	p00	-1104	837

Note:

No pin for PAD No. 26

PIN LIST

ML610Q426/426 Pin List

PAD No.	Primary function			Secondary, Tertiary, or Quaternary function			
	Pin name	I/O	Function	Secondary/ Tertiary/ Quaternary	Pin name	I/O	Function
13	V _{SS}	—	Negative power supply pin	—	—	—	—
17	V _{DD}	—	Positive power supply pin	—	—	—	—
12	V _{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—
16	V _{DDX} ⁽¹⁾	—	Power supply pin for low-speed oscillator (internally generated)	—	—	—	—
26	V _{PP} ⁽²⁾	—	Power supply pin for Flash ROM	—	—	—	—
20	V _{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
21	V _{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
22	V _{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
23	V _{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—
24	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—
25	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—
19	TEST	I/O	Test pin	—	—	—	—
18	RESET_N	I	Reset input pin	—	—	—	—
14	XT0	I	Low-speed clock oscillation pin	—	—	—	—
15	XT1	O	Low-speed clock oscillation pin	—	—	—	—
93	P00/EXI0/ TPRUN0	I	Input port, External interrupt, Timer and PWM common external trigger input	—	—	—	—
1	P01/EXI1/ TPRUN1	I	Input port, External interrupt, Timer and PWM common external trigger input	—	—	—	—
2	P02/EXI2/ TPRUN2	I	Input port, External interrupt, Timer and PWM common external trigger input	—	—	—	—
3	P03/EXI3/ RXD1/ TPRUN3	I	Input port, External interrupt, UART1 data input, Timer and PWM common external trigger input	—	—	—	—
4	P04/EXI4/ T0IP8CK	I	Input port, External interrupt, Timer 0/Timer 1/PWM8 external clock input	—	—	—	—
10	P65	I/O	Input/output port	Secondary	LSCLK	O	Low-speed clock output
				Tertiary	RCM	O	RC type ADC oscillation monitor
				Quaternary	SDA	O	I ² C data input/output
11	P66	I/O	Input/output port, P8RUN, BLDI	Secondary	OUTCLK	O	High-speed clock output
				Tertiary	MD0	O	Melody 0 output
				Quaternary	SCL	O	I ² C clock input/output
5	P70	I/O	Input/output port, TIJRUN	Secondary	IN0	I	RC type ADC0 oscillation input pin
				Tertiary	SIN1	I	SSIO1 data input
				Quaternary	ELP	I/O	Pumping clock output
6	P71	I/O	Input/output port, T0IP8CK	Secondary	CS0	O	RC type ADC0 reference capacitor connection pin
				Tertiary	SCK1	I/O	SSIO1 synchronous clock input/output
				Quaternary	ELC	I/O	Discharge pulse signal output
7	P72	I/O	Input/output port, T1JCK	Secondary	RCT0	O	RC type ADC0 reference resistor connection pin
				Tertiary	SOUT1		SSIO1 data output
				Quaternary	RXD1		UART1 data input
8	P73	I/O	Input/output port	Secondary	RS0	O	RC type ADC0 measurement resistor sensor connection pin
				Tertiary	MD0	O	Melody 0 output
				Quaternary	TXD1	O	UART1 data output
9	P74	I/O	Input/output port	Secondary	RT0	O	RC type ADC0 resistor/capacitor sensor connection pin
				Tertiary	PWM8	O	PWM8 output

^{(*)1} Pin for ML610426 and ML610Q426 ^{(*)2} Pin for ML610Q426

PAD No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary/ Tertiary/ Quaternary	Pin name	I/O	Function
92	SEG0	O	LCD segment pin	—	—	—	—
	P50/EX18	I/O	Input/output port, External interrupt	Secondary Tertiary	MD0 SIN1	O I	Melody 0 output SSIO1 data input
91	SEG1	O	LCD segment pin	—	—	—	—
	P51/EX18	I/O	Input/output port, External interrupt	Secondary Tertiary	— SCK1	— I/O	— SSIO1 synchronous clock input/output
90	SEG2	O	LCD segment pin	—	—	—	—
	P52/EX18	I/O	Input/output port, External interrupt	Secondary Tertiary	RXD1 SOUT1	I O	UART1 data input SSIO1 data output
89	SEG3	O	LCD segment pin	—	—	—	—
	P53/EX18	I/O	Input/output port, External interrupt	Secondary	TXD1	O	UART1 data output
88	SEG4	O	LCD segment pin	—	—	—	—
	P63	I/O	Input/output port	Secondary Tertiary	— ELP	— O	— Pumping clock output
				Quaternary	PWM8	O	PWM8 output
87	SEG5	O	LCD segment pin	—	—	—	—
	P64	I/O	Input/output port	Secondary Tertiary	— ELC	— O	— Discharge pulse signal output
86	SEG6	O	LCD segment pin	—	—	—	—
	P05/EX15/ T1JCK	I	Input port, External interrupt, Timer 1/Timer B external clock input	—	—	—	—
85	SEG7	O	LCD segment pin	—	—	—	—
	P06/EX16	I	Input port, External interrupt	—	—	—	—
84	SEG8	O	LCD segment pin	—	—	—	—
83	SEG9	O	LCD segment pin	—	—	—	—
82	SEG10	O	LCD segment pin	—	—	—	—
81	SEG11	O	LCD segment pin	—	—	—	—
80	SEG12	O	LCD segment pin	—	—	—	—
79	SEG13	O	LCD segment pin	—	—	—	—
78	SEG14	O	LCD segment pin	—	—	—	—
77	SEG15	O	LCD segment pin	—	—	—	—
76	SEG16	O	LCD segment pin	—	—	—	—
75	SEG17	O	LCD segment pin	—	—	—	—
74	SEG18	O	LCD segment pin	—	—	—	—
73	SEG19	O	LCD segment pin	—	—	—	—
72	SEG20	O	LCD segment pin	—	—	—	—
71	SEG21	O	LCD segment pin	—	—	—	—
70	SEG22	O	LCD segment pin	—	—	—	—
69	SEG23	O	LCD segment pin	—	—	—	—
68	SEG24	O	LCD segment pin	—	—	—	—
67	SEG25	O	LCD segment pin	—	—	—	—
66	SEG26	O	LCD segment pin	—	—	—	—
65	SEG27	O	LCD segment pin	—	—	—	—
64	SEG28	O	LCD segment pin	—	—	—	—
63	SEG29	O	LCD segment pin	—	—	—	—
62	SEG30	O	LCD segment pin	—	—	—	—
61	SEG31	O	LCD segment pin	—	—	—	—
60	SEG32	O	LCD segment pin	—	—	—	—
59	SEG33	O	LCD segment pin	—	—	—	—
58	SEG34	O	LCD segment pin	—	—	—	—
57	SEG35	O	LCD segment pin	—	—	—	—

ML610Q426/426 Pin List

PAD No.	Primary function			Secondary function or Tertiary function			
	Pin name	I/O	Function	Secondary/ Tertiary/ Quaternary	Pin name	I/O	Function
56	SEG36	O	LCD segment pin	—	—	—	—
55	SEG37	O	LCD segment pin	—	—	—	—
54	SEG38	O	LCD segment pin	—	—	—	—
53	SEG39	O	LCD segment pin	—	—	—	—
52	SEG40	O	LCD segment pin	—	—	—	—
51	SEG41	O	LCD segment pin	—	—	—	—
50	SEG42	O	LCD segment pin	—	—	—	—
49	SEG43	O	LCD segment pin	—	—	—	—
48	SEG44	O	LCD segment pin	—	—	—	—
47	SEG45	O	LCD segment pin	—	—	—	—
46	SEG46	O	LCD segment pin	—	—	—	—
45	SEG47	O	LCD segment pin	—	—	—	—
44	SEG48	O	LCD segment pin	—	—	—	—
43	SEG49	O	LCD segment pin	—	—	—	—
42	COM15/ SEG50	O	LCD common/segment pin	—	—	—	—
41	COM14/ SEG51	O	LCD common/segment pin	—	—	—	—
40	COM13/ SEG52	O	LCD common/segment pin	—	—	—	—
39	COM12/ SEG53	O	LCD common/segment pin	—	—	—	—
38	COM11/ SEG54	O	LCD common/segment pin	—	—	—	—
37	COM10/ SEG55	O	LCD common/segment pin	—	—	—	—
36	COM9/ SEG56	O	LCD common/segment pin	—	—	—	—
35	COM8/ SEG57	O	LCD common/segment pin	—	—	—	—
34	COM7/ SEG58	O	LCD common/segment pin	—	—	—	—
33	COM6/ SEG59	O	LCD common/segment pin	—	—	—	—
32	COM5/ SEG60	O	LCD common/segment pin	—	—	—	—
31	COM4/ SEG61	O	LCD common/segment pin	—	—	—	—
30	COM3	O	LCD common pin	—	—	—	—
29	COM2	O	LCD common pin	—	—	—	—
28	COM1	O	LCD common pin	—	—	—	—
27	COM0	O	LCD common pin	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors C _{DL} and C _{GL} are connected across this pin and V _{SS} as required.	—	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P65 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P66 pin.	Secondary	—
General-purpose input port				
P00-P04	I	General-purpose input port.	Primary	Positive
P05-P06	I	General-purpose input port. These pins are available in case SEG0-SEG7 pins are changed by mask option.	Primary	Positive
General-purpose input/output port				
P50-P53	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. These pins are available in case SEG0-SEG7 pins are changed by mask option.	Primary	Positive
P63-P64	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. These pins are available in case SEG0-SEG7 pins are changed by mask option.	Primary	Positive
P65-P66	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P70-P74	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
UART				
TXD1	O	UART data output pin. This pin is used as the quaternary function of the P73 pin or tertiary function of P53 pin.	Tertiary/ Quaternary	Positive
RXD1	I	UART data input pin. This pin is used as the quaternary function of the P72 pin or tertiary function of P52 pin or the primary function of the P03 pin.	Primary/ Tertiary/ Quaternary	Positive
I²C bus interface				
SDA	I/O	I ² C data input/output pin. This pin is used as the quaternary function of the P65 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Quaternary	Positive
SCL	O	I ² C clock output pin. This pin is used as the quaternary function of the P66 pin. This pin has an NMOS open drain output. When using this pin as a function of the I ² C, externally connect a pull-up resistor.	Quaternary	Positive
Synchronous serial (SSIO)				
SCK1	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P71 pin or P51 pin.	Tertiary	—
SIN1	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P70 pin or P50 pin.	Tertiary	Positive
SOUT1	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P72 pin or P52 pin.	Tertiary	Positive
PWM				
PWM8	O	PWM8 output pin. This pin is used as the tertiary function of the P74 or the quaternary function P63 pin.	Secondary/ Tertiary	Positive
TOIP8CK	I	PWM8 external clock input pin. This pin is used as the primary function of the P04 pin or P71 pin.	Primary	—
P8RUN	I	PWM8 external trigger input pin. This pin is used as the primary function of the P66 pin and the primary function of the P66 pin.	Primary	Positive/ negative
TPRUN0, TPRUN1, TPRUN2, TPRUN3	I	PWM8 common external trigger input pin. This pin is used as the primary function of the P00, P01, P02 and P03 pin.	Primary	Positive/ negative
External interrupt				
EXI0-4	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P04 pins.	Primary	Positive/ negative
EXI5-6	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P05-P06 pins. These pins are available in case SEG0-SEG7 pins are changed by mask option.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P53 pins. These pins are available in case SEG0-SEG7 pins are changed by mask option.	Primary	Positive/ negative
Timer				
TOIP8CK	I	External clock input pin used for Timer 0 and Timer I. This pin is used as the primary function of the P04 pin or P71 pin	Primary	—
T1JCK	I	External clock input pin used for Timer 1 and Timer B. This pin is used as the primary function of the P72 pin or P05 pin.	Primary	—
TIJRUN	I	TimerI/TimerJ external trigger input. This pin is used as the primary function of the P70 pin.	Primary	Positive/ negative
TPRUN0, TPRUN1, TPRUN2, TPRUN3	I	TimerI/TimerJ common external trigger input. These pins are used as the primary functions of the P00, P01, P02 and P03 pins.	Primary	Positive/ negative

Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the tertiary function of the P66 pin or tertiary function of P73 pin or secondary function of the P50 pin.	Secondary/ Tertiary	Positive/ negative
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P70 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P71 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P72 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P73 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P74 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the tertiary function of the P65 pin.	Tertiary	—
BLD				
BLDI	I	Battery level detection input. This pin is used as the primary function of the P66 pin.	Primary	—

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
LCD drive signal				
COM0-7	O	Common output pins.	—	—
COM8-15	O	Common output pins.	—	—
SEG0-7	O	Segment output pins. These pins are available in case P05-P06, P50-P53, and P63-P64 pins are changed by mask option.	—	—
SEG8-39	O	Segment output pins.	—	—
SEG40-53	O	Segment output pins.	—	—
SEG54-61	O	Segment output pins.	—	—
EL driver signal				
ELP	O	Pumping clock output pin. This pin is used as the quaternary function of the P70 pin or tertiary function of the P63 pin.	Tertiary	—
ELC	O	Discharge pulse signal output pin. This pin is used as the quaternary function of the P71 pin or tertiary function of the P64 pin.	Tertiary	Positive
LCD driver power supply				
V _{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V _{SS} and V _{L1} , V _{L2} , V _{L3} , and V _{L4} respectively.	—	—
V _{L2}	—		—	—
V _{L3}	—		—	—
V _{L4}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C ₁₂ is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V _{SS}	—	Negative power supply pin.	—	—
V _{DD}	—	Positive power supply pin.	—	—
V _{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C _L (see measuring circuit 1) are connected between this pin and V _{SS} .	—	—
V _{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor C _X (see measuring circuit 1) is connected between this pin and V _{SS} .	—	—
V _{PP}	—	Power supply pin for programming Flash ROM.A pull up resistor is internally connected.	—	—

TERMINATION OF UNUSED PINS

Table 5 shows methods of terminating the unused pins.

Table 5 Termination of Unused Pins

Pin	Recommended pin termination
V _{PP}	Open
V _{L1} , V _{L2} , V _{L3} , V _{L4}	Open
C1, C2	Open
RESET_N	Open
TEST	Open
P00 to P06	V _{DD} or V _{SS}
P50 to P53	Open
P63 to P66	Open
P70 to P74	Open
COM0 to COM15	Open
SEG0 to SEG61	Open

Note:

It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = 25°C	-0.3 to +4.6	V
Power supply voltage 2	V _{PP}	Ta = 25°C	-0.3 to +9.5	V
Power supply voltage 3	V _{DDL}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 4	V _{DDX}	Ta = 25°C	-0.3 to +3.6	V
Power supply voltage 5	V _{L1}	Ta = 25°C	-0.3 to +1.75	V
Power supply voltage 6	V _{L2}	Ta = 25°C	-0.3 to +3.5	V
Power supply voltage 7	V _{L3}	Ta = 25°C	-0.3 to +5.25	V
Power supply voltage 8	V _{L4}	Ta = 25°C	-0.3 to +7.0	V
Input voltage	V _{IN}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output voltage	V _{OUT}	Ta = 25°C	-0.3 to V _{DD} +0.3	V
Output current 1	I _{OUT1}	Port5-7, Ta = 25°C	-12 to +11	mA
Power dissipation	PD	Ta = 25°C	1.0	mW
Storage temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	ML610426, ML610Q426	-20 to +70	°C
Operating voltage	V _{DD}	—	1.1 to 3.6	V
Operating frequency (CPU)	f _{OP}	VDD = 1.1 to 3.6V	30k to 157k	Hz
		VDD = 1.3 to 3.6V	30k to 1.25M	
Capacitor externally connected to V _{DD} pin	C _V	—	1.0±30%	μF
Capacitor externally connected to V _{DDL} pin	C _L	—	1.0±30%	μF
Capacitor externally connected to V _{DDLX} pin	C _X	ML610426/Q426	0.1±30%	μF
Capacitors externally connected to V _{L1, 2, 3, 4} pins	C _{a, b, c, d}	—	1.0±30%	μF
Capacitors externally connected across C1 and C2 pins	C ₁₂	—	1.0±30%	μF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f _{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R _L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor	C _{DL} /C _{GL}	C _L =6pF of crystal oscillation	—	12	—	pF
		C _L =9pF of crystal oscillation	—	18	—	

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Operating temperature	T _{OP}	Flash ROM, At write/erase	0 to +40	°C
Operating voltage	V _{DD}	At write/erase ^(*)	2.75 to 3.6	V
	V _{DDL}		2.5 to 2.75	
	V _{PP}		7.7 to 8.3	
Rewrite counts	CEP	—	80	cycles
Data retention	YDR	—	10	years

(*) : In addition the power supply to VDD pin and VPP pin, within the range 2.5V to 2.75V has to be supplied to VDDL pin when programming and erasing Flash ROM

DC CHARACTERISTICS (1/5)

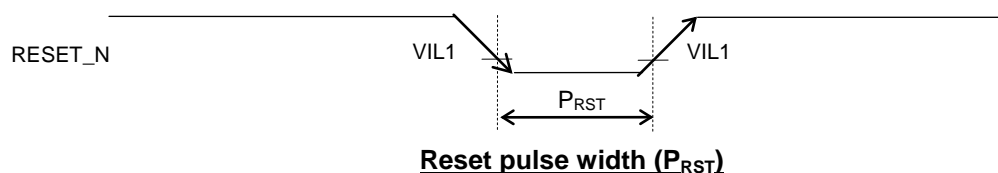
(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

(V _{DD} = 1.1 to 3.6V, V _{SS} = 0V, T _A = 25 to 175 °C, unless otherwise specified)								
Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
1MHz RC oscillation frequency	f _{RC}	V _{DD} = 1.3 to 3.6V	T _A = 25°C	Typ. -10%	1.0	Typ. +10%	MHz	1
			*1	Typ. -25%	1.0	Typ. +25%	MHz	
Low-speed crystal oscillation start time*2	T _{XTL}	—		—	0.6	2	s	
1MHz RC oscillation start time	T _{RC}	—		—	—	10	μs	
Reset pulse width	P _{RST}	—		200	—	—	μs	
Reset noise elimination pulse width	P _{NRST}	—		—	—	0.3		
Power-on reset generated power rise time	T _{POR}	—		—	—	10	ms	

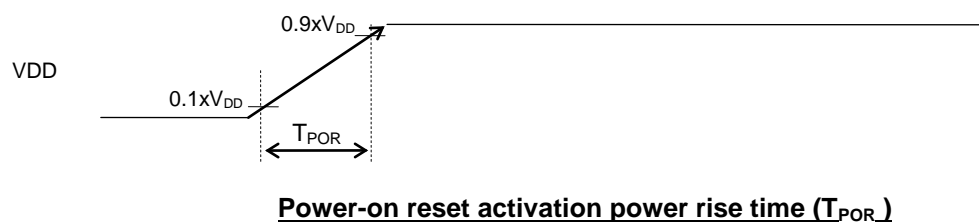
*1: Recommended operating temperature (Ta = -20 to +70°C)

*2 : Use 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).

[Reset pulse width]



[Power-on reset activation power rise time]



DC CHARACTERISTICS (2/5)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit	
				Min.	Min.	Min.			
V _{L1} voltage	V _{L1}	V _{DD} = 3.0V, T _j = 25°C	CN4-0 = 00H	0.89	0.94	0.99	V	1	
			CN4-0 = 02H	0.93	0.98	1.03			
			CN4-0 = 04H	0.97	1.02	1.07			
			CN4-0 = 06H	1.01	1.06	1.11			
			CN4-0 = 08H	1.05	1.10	1.15			
			CN4-0 = 0AH	1.09	1.14	1.19			
			CN4-0 = 0CH	1.13	1.18	1.23			
			CN4-0 = 0EH	1.17	1.22	1.27			
			CN4-0 = 10H	1.21	1.26	1.31			
			CN4-0 = 12H	1.25	1.30	1.35			
			CN4-0 = 14H* ¹	1.29	1.34	1.39			
			CN4-0 = 16H* ¹	1.33	1.38	1.43			
			CN4-0 = 18H* ¹	1.37	1.42	1.47			
			CN4-0 = 1AH* ¹	1.41	1.46	1.51			
			CN4-0 = 1CH* ¹	1.45	1.50	1.55			
CN4-0 = 1EH* ¹	1.49	1.54	1.59						
V _{L1} temperature deviation	ΔV _{L1}	V _{DD} = 3.0V		—	-1.5	—	mV/°C	1	
V _{L1} voltage dependency	ΔV _{L1}	V _{DD} = 1.3 to 3.6V		—	5	20	mV/V		
V _{L2} voltage	V _{L2}	V _{DD} = 3.0V, T _j = 25°C, 1MΩ load (V _{L4} –V _{SS})	1/2bias	V _{L1}	V _{L1}	V _{L1}	V		
V _{L3} voltage	V _{L3}		1/3bias, 1/1bias	Typ.	V _{L1} ×2	Typ.			
			1/4bias	-10%		+4%			
			1/2bias	V _{L1}	V _{L1}	V _{L1}			
V _{L4} voltage	V _{L4}		1/3bias, 1/1bias	TYP.	V _{L1} ×2	TYP.			
			1/4bias	-10%	V _{L1} ×3	+4%			
			1/2bias	Typ.	V _{L1} ×2	Typ.			
LCD bias voltage generation time	T _{BIAS}		—	1/3bias, 1/1bias	-10%	V _{L1} ×3		+4%	ms
				1/4bias		V _{L1} ×4			
		—		—	—	600			

*1: When using 1/4 bias, the VL1 voltage is set to typ. 1.30 V (same voltage as in CN4-0 = 12H).

DC CHARACTERISTICS (3/5)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
BLD threshold voltage	V _{BLD}	V _{DD} , V _{BLDI} = 1.1 to 3.6V	LD3-0 = 0H	Typ. -6%	1.16	Typ. +6%	V	
			LD3-0 = 1H		1.18			
			LD3-0 = 2H		1.20			
			LD3-0 = 3H		1.22			
			LD3-0 = 4H		1.24			
			LD3-0 = 5H		1.26			
			LD3-0 = 6H		1.28			
			LD3-0 = 7H		1.30			
			LD3-0 = 8H		2.35			
			LD3-0 = 9H		2.40			
			LD3-0 = 0AH		2.45			
			LD3-0 = 0BH		2.50			
			LD3-0 = 0CH		2.55			
			LD3-0 = 0DH		2.60			
			LD3-0 = 0EH		2.65			
			LD3-0 = 0FH		2.70			
BLD input voltage from I/O ports	V _{BLDI}	—		1.1	—	V _{DD}	V	
BLD threshold voltage temperature deviation	ΔV _{BLD}	—		—	0	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C		0.25	0.65	μA	1
			Ta = -20 to 70°C		—	6		
Supply current 2	IDD2	CPU: In HALT state LTBC: Operating ^{*3*4} High-speed oscillation: Stopped LCD/BIAS circuits: Stopped	Ta = 25°C	—	0.5	1.4	μA	
Supply current 3	IDD3	CPU: In 32.768kHz operating state. ^{*1*3} High-speed oscillation: Stopped. LCD/BIAS circuits: Operating. ^{*2}	Ta = 25°C	—	5	7.5	μA	
Supply current 4	IDD4	CPU: In 1MHz CR operating state. LCD/BIAS circuits: Operating. ^{*2*3}	Ta = 25°C	—	140	170	μA	

*1 : CPU operating rate is 100% (No HALT state).

*2 : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz,
Bias voltage multiplying clock: 1/128 LSCLK (256Hz)*3 : Use 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).

*4 : Significant bits of BLKCON0 to BLKCON4 registers are all "1"

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Output voltage 1 (P50–P53) (P63-P66) (P70-P74)	VOH1	IOH1 = −0.5mA, V _{DD} = 1.8 to 3.6V		V _{DD} −0.5	—	—		
		IOH1 = -0.1mA, V _{DD} = 1.3 to 3.6V		V _{DD} −0.3	—	—		
		P65-P66, P70-P74	IOH1 = -0.03mA, V _{DD} = 1.1 to 3.6V	V _{DD} −0.3	—	—		
		P50-P53, P63-P64	IOH1 = -0.015mA, V _{DD} = 1.1 to 3.6V					
	VOL1	IOL1 = +0.5mA, V _{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V _{DD} = 1.3 to 3.6V		—	—	0.5		
		IOL1 = +0.03mA, V _{DD} = 1.1 to 3.6V		—	—	0.3		
Output voltage 1 (P65–P66)	VOL2	IOL2 = +3mA, V _{DD} = 2.0 to 3.6V (when I2C mode is selected)		—	—	0.4		
Output voltage 3 (COM0–COM15) (SEG0–SEG61)	VOH3	1/4, 1/3, 1/1 bias	IOH3 = −0.03mA, VL1=1.2V	V _{L4} −0.2	—	—	V	2
	VOMH3		IOMH3 = +0.03mA, VL1=1.2V	—	—	V _{L3} +0.2		
	VOMH3S		IOMH3S = −0.03mA, VL1=1.2V	V _{L3} −0.2	—	—		
	VOM3		IOM3 = +0.03mA, VL1=1.2V	—	—	V _{L2} +0.2		
	VOM3S		IOM3S = −0.03mA, VL1=1.2V	V _{L2} −0.2	—	—		
	VOML3		IOML3 = +0.03mA, VL1=1.2V	—	—	V _{L1} +0.2		
	VOML3S		IOML3S = −0.03mA, VL1=1.2V	V _{L1} −0.2	—	—		
	VOL3		IOL3 = +0.03mA, VL1=1.2V	—	—	0.2		
	VOH3	1/2bias	IOH3 = −1μA, CN4-0=1AH,1CH,1EH	V _{L4} −0.2	—	—		
	VOMH3		IOMH3 = +1μA, CN4-0=1AH,1CH,1EH	—	—	V _{L123} +0.2		
	VOML3S		IOML3S = −1μA, CN4-0=1AH,1CH,1EH	V _{L123} −0.2	—	—		
	VOL3		IOL3 = +1μA, CN4-0=1AH,1CH,1EH	—	—	0.2		
	Output leakage (P50–P53) (P63-P66) (P70-P74)	IOOH	VOH = V _{DD} (in high-impedance state)		—	—		
IOOL		VOL = V _{SS} (in high-impedance state)		−1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V _{DD}		—	—	1	μA	4
	IIL1	VIL1 = V _{SS}	V _{DD} = 1.8 to 3.6V	−600	−300	−20		
			V _{DD} = 1.3 to 3.6V	−600	−300	-10		
V _{DD} = 1.1 to 3.6V			−600	−300	-2			
Input current 1 (TEST)	IIH1	VIH1 = V _{DD}	V _{DD} = 1.8 to 3.6V	20	300	600		
			V _{DD} = 1.3 to 3.6V	10	300	600		
			V _{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V _{SS}		-1	—	—		
Input current 2 (P00-P06) (P50–P53) (P63-P66) (P70-P74)	IIH2	VIH2 = V _{DD} (when pulled-down)	V _{DD} = 1.8 to 3.6V	2	30	200		
			V _{DD} = 1.3 to 3.6V	0.2	30	200		
			V _{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V _{SS} (when pulled-up)	V _{DD} = 1.8 to 3.6V	−200	−30	−2		
			V _{DD} = 1.3 to 3.6V	−200	−30	-0.2		
			V _{DD} = 1.1 to 3.6V	−200	−30	-0.01		
	IIH2Z	VIH2 = V _{DD} (in high-impedance state)		—	—	1		
IIL2Z	VIL2 = V _{SS} (in high-impedance state)		−1	—	—			

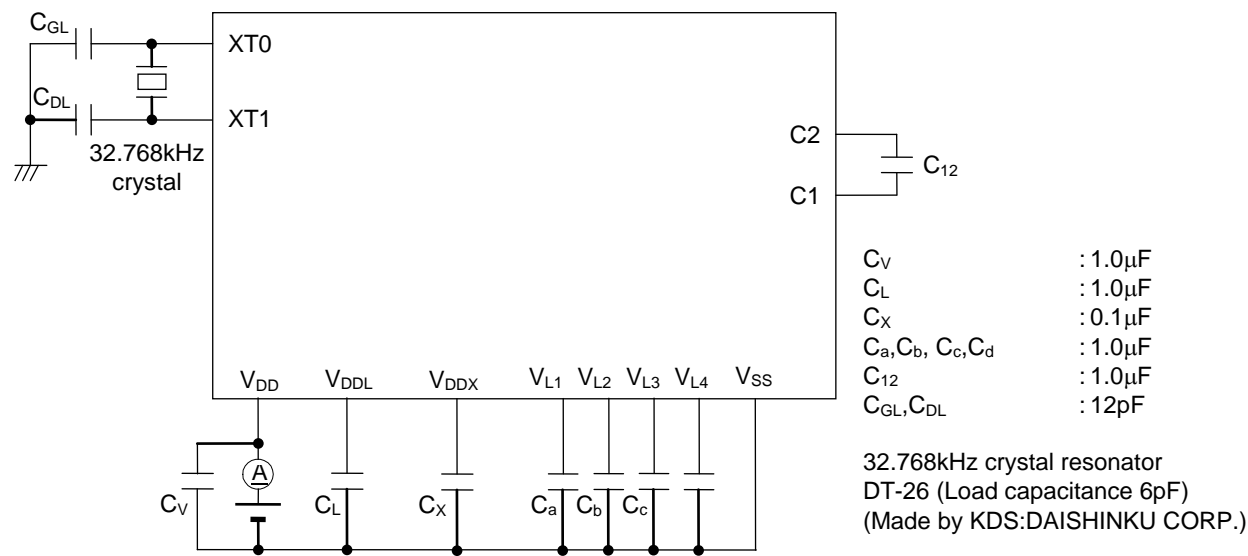
DC CHARACTERISTICS (5/5)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

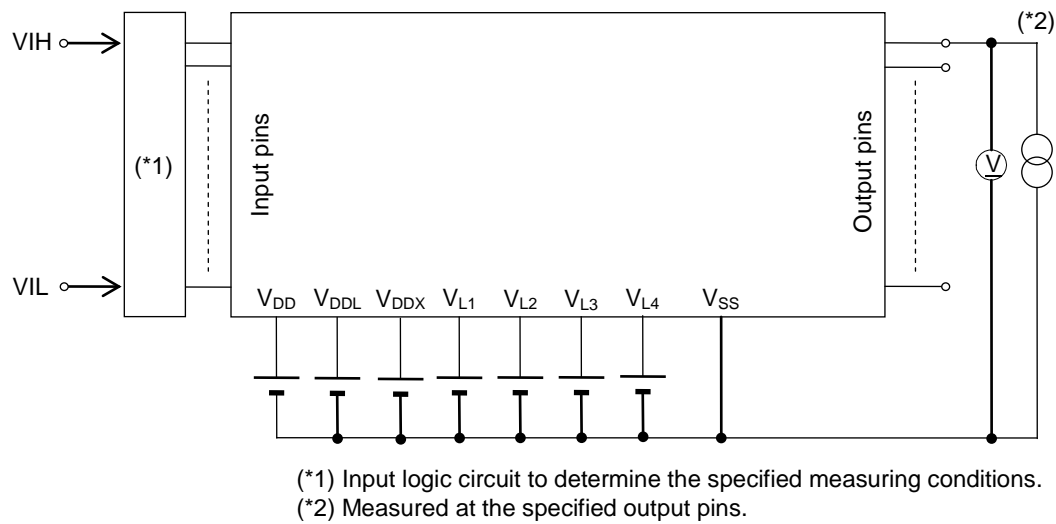
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (P00-P06) (P50-P53) (P63-P66) (P70-P74)	VIH1	V _{DD} = 1.3 to 3.6V	0.7 ×V _{DD}	—	V _{DD}	V	5
		V _{DD} = 1.1 to 3.6V	0.7 ×V _{DD}	—	V _{DD}		
	VIL1	V _{DD} = 1.3 to 3.6V	0	—	0.3 ×V _{DD}		
		V _{DD} = 1.1 to 3.6V	0	—	0.2 ×V _{DD}		
Input pin capacitance (P00-P06) (P50-P53) (P63-P66) (P70-P74)	CIN	f = 10kHz V _{rms} = 50mV Ta = 25°C	—	—	5	pF	—

MEASURING CIRCUITS

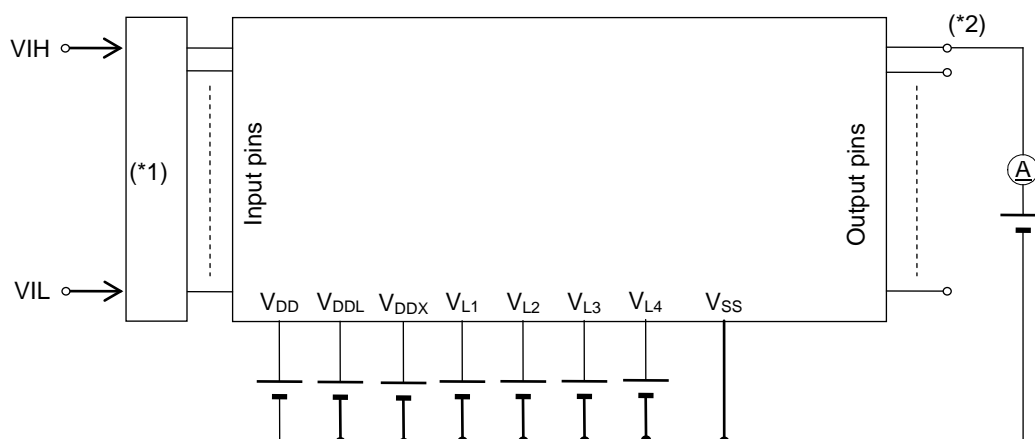
MEASURING CIRCUIT 1



MEASURING CIRCUIT 2



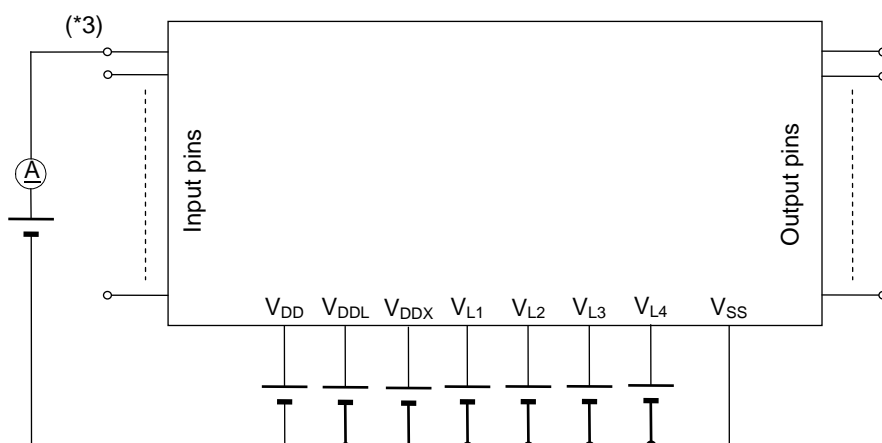
MEASURING CIRCUIT 3



*1: Input logic circuit to determine the specified measuring conditions.

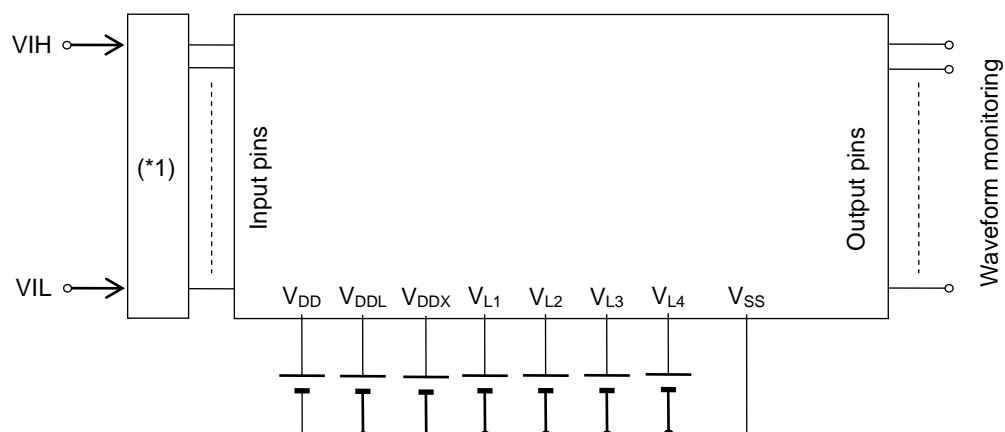
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

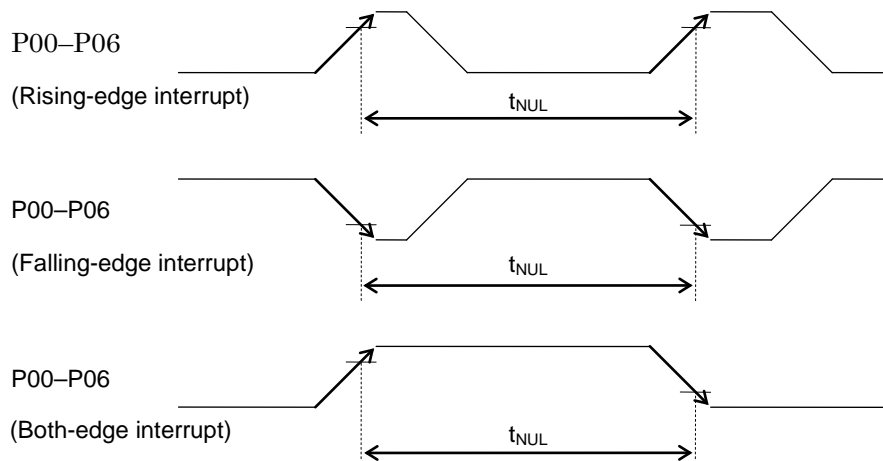
MEASURING CIRCUIT 5



*1: Input logic circuit to determine the specified measuring conditions.

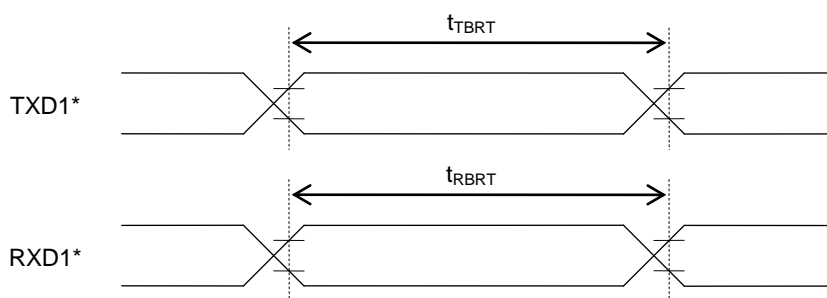
AC CHARACTERISTICS (External Interrupt)(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T _{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

**AC CHARACTERISTICS (UART)**(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t _{TBRT}	—	—	BRT ^{*1}	—	s
Receive baud rate	t _{RBRT}	—	BRT ^{*1} -3%	BRT ^{*1}	BRT ^{*1} +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA1BRTL,H) and the UART mode register 0 (UA1MOD0).



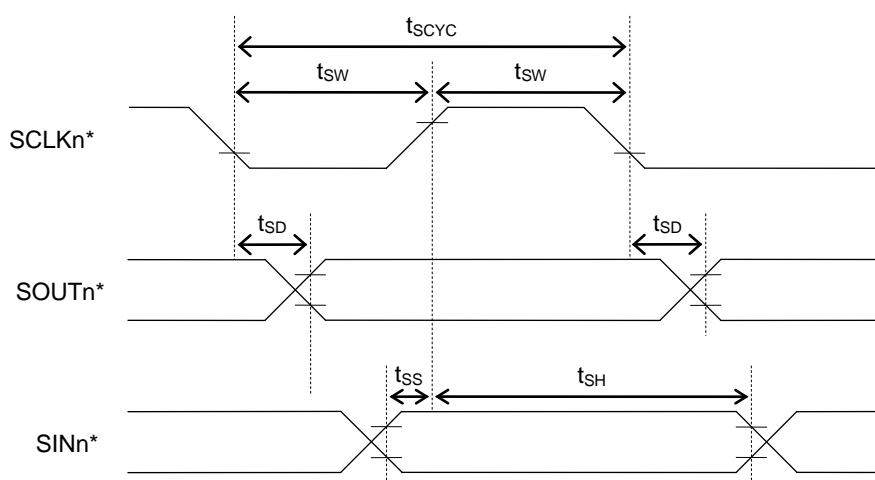
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)(V_{DD} = 1.3 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLKn input cycle (slave mode)	t _{SCYC}	—	10	—	—	μs
SCLKn output cycle (master mode)	t _{SCYC}	—	—	SCLKn* ¹	—	s
SCLKn input pulse width (slave mode)	t _{SW}	—	4	—	—	μs
SCLKn output pulse width (master mode)	t _{SW}	—	SCLKn* ¹ ×0.4	SCLKn* ¹ ×0.5	SCLKn* ¹ ×0.6	s
SOUTn output delay time (slave mode)	t _{SD}	output load 10pF	P72/SOUT1	—	500	ns
			P52/SOUT1	—	850	
SOUTn output delay time (master mode)	t _{SD}	output load 10pF	P72/SOUT1	—	500	ns
			P52/SOUT1	—	650	
SINn input setup time (slave mode)	t _{SS}	—	80	—	—	ns
SINn input setup time (master mode)	t _{SS}	P70/SIN1	500	—	—	ns
		P50/SIN1	850	—	—	
SINn input hold time	t _{SH}	—	300	—	—	ns

n = 1

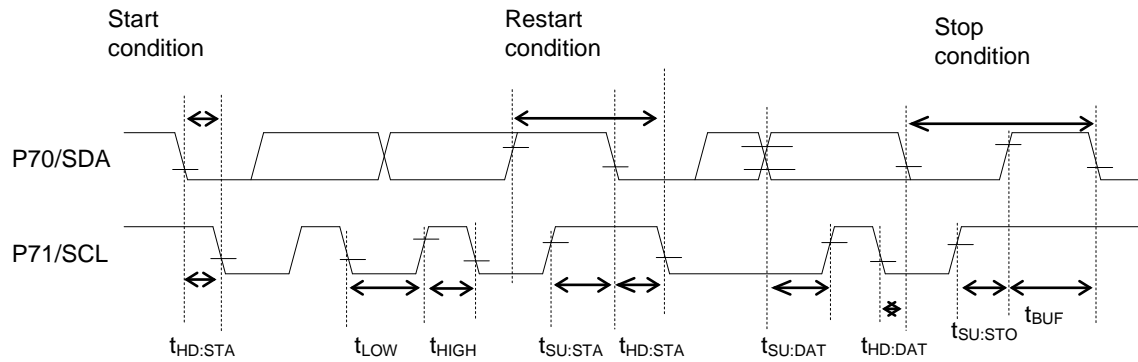
*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIOOnMOD1)



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I2C Bus Interface: Standard Mode)(V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f _{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	4.0	—	—	μs
SCL "L" level time	t _{LOW}	—	4.7	—	—	μs
SCL "H" level time	t _{HIGH}	—	4.0	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	4.7	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	3.45	μs
SDA setup time	t _{SU:DAT}	—	0.25	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	4.0	—	—	μs
Bus-free time	t _{BUF}	—	4.7	—	—	μs



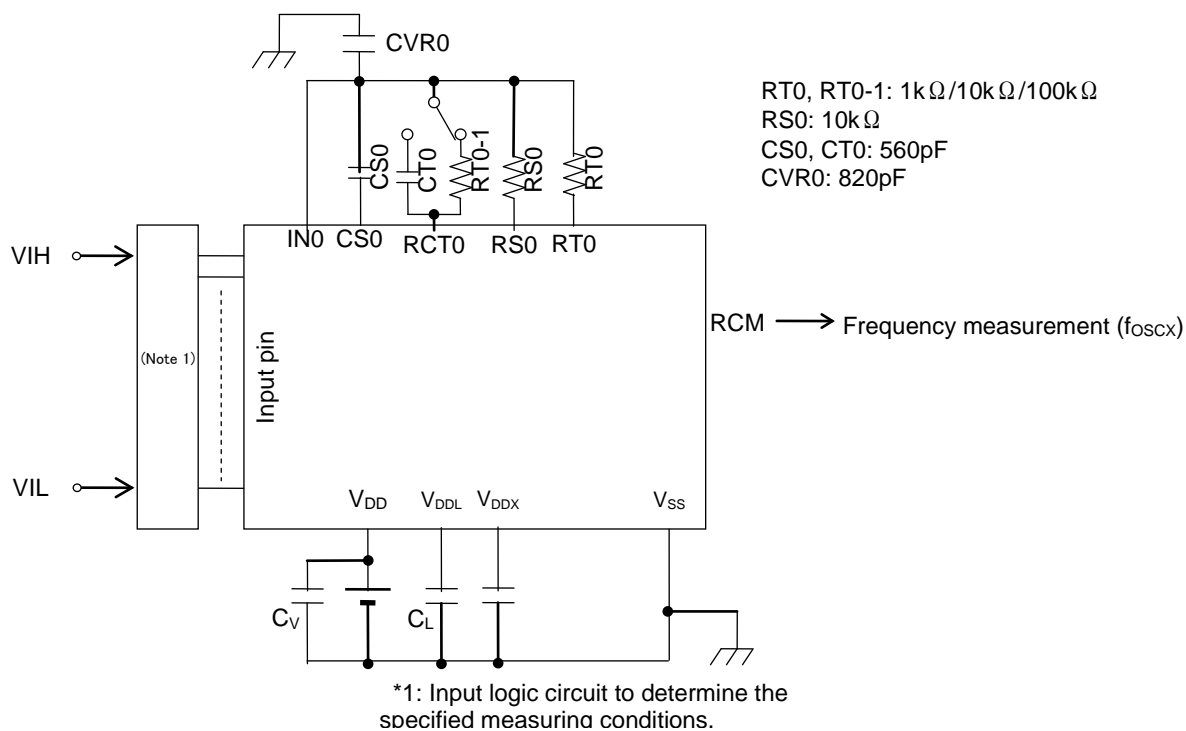
AC Characteristics (RC Oscillation A/D Converter)Condition for $V_{DD}=1.8$ to $3.6V$ $(V_{DD}=1.8$ to $3.6V$, $V_{SS}=0V$, $T_a=-20$ to $+70^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0, RT0, RT0-1	CS0, CT0 $\geq 740pF$	1	—	—	k Ω
Oscillation frequency $V_{DD} = 3.0V$	f_{OSC1}	Resistor for oscillation=1k Ω	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10k Ω	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100k Ω	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 3.0V$	Kf1	RT0, RT0-1=1k Ω	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1=10k Ω	0.981	1	1.019	—
	Kf3	RT0, RT0-1=100k Ω	0.099	0.101	0.104	—

^{*1}: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}, \quad \frac{f_{OSCx}(RT0-1-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}$$

(x = 1, 2, 3)



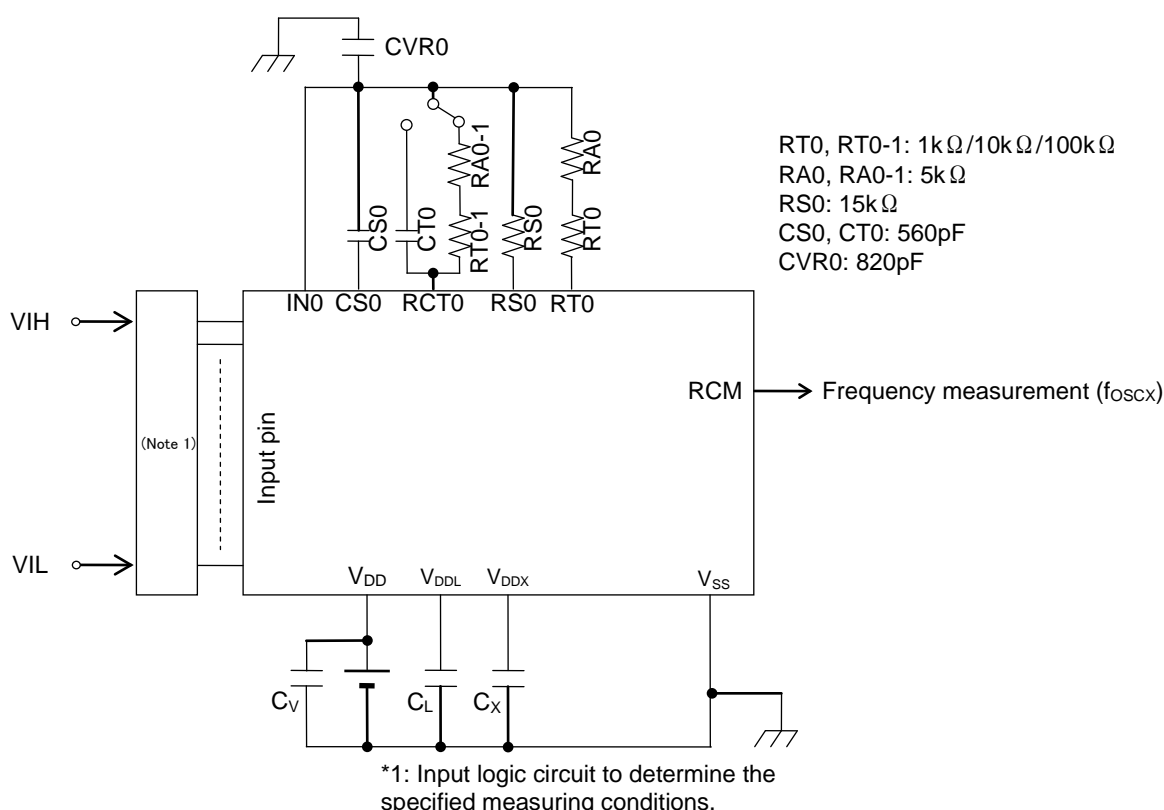
Condition for $V_{DD}=1.1$ to $3.6V$ $(V_{DD} = 1.1$ to $3.6V$, $V_{SS} = 0V$, $T_a = -20$ to $+70^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0, RT0,RT0-1	CS0, CT0 $\geq 740pF$	1	—	—	k Ω
Oscillation frequency $V_{DD} = 1.5V$	f_{OSC1}	Resistor for oscillation=6k Ω	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15k Ω	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105k Ω	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 1.5V$	Kf1	RT0, RT0-1=1k Ω	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1=10k Ω	0.973	1	1.028	—
	Kf3	RT0, RT0-1=100k Ω	0.142	0.147	0.152	—
Oscillation frequency $V_{DD} = 3.0V$	f_{OSC1}	Resistor for oscillation=6k Ω	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15k Ω	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105k Ω	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio ^{*1} $V_{DD} = 3.0V$	Kf1	RT0, RT0-1=1k Ω	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1=10k Ω	0.982	1	1.018	—
	Kf3	RT0, RT0-1=100k Ω	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})}, \quad \frac{f_{OSCx}(RT0-1-CS0 \text{ oscillation})}{f_{OSCx}(RS0-CS0 \text{ oscillation})},$$

(x = 1, 2, 3)



Note:

·Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0 pin), including CVR0. Especially, do not have long wiring between IN0 and RS0. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

·When RT0 (Thermistor and etc.) requires long wiring due to the restricted placement, please have $V_{SS}(GND)$ trace next to the signal.

·Please make wiring to components (capacitor, resistor, and so on) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q426-01	Mar.17, 2015	–	–	Final edition 1

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