Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL62Q2700-04
Issue Date: Mar 26, 2024

ML62Q2700 Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q2700 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory (Flash memory), data memory (RAM), data Flash (Erase unit:128byte, Write unit:1byte) and rich peripheral functions such as the multiplier/divider, CRC generator, Clock generator, Timer, General Purpose Ports, UART, Synchronous serial port, I^2C bus interface unit(Master, Slave), Voltage Level Supervisor (VLS), Successive approximation type 12bit A/D converter, Audio playback function, LCD driver, Safety function (IEC60730/60335 Class B) and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP (In-System Programming) function supports the Flash programming in production line.

- Applications

Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

Note:
This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems. Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product list

The ML62Q2700 Group has products as show in the Table1 with multiple package and memory size combinations.

Table 1 Product List

Program memory	Data memory (RAM)	Data Flash	48pin TQFP48 WQFN48	52pin TQFP52	64pin QFP64 TQFP64	80pin QFP80	100pin QFP100 TQFP100
256Kbyte	16Kbyte	4Kbyte	-	-	ML62Q2727	ML62Q2737	ML62Q2747
192Kbyte			-	-	ML62Q2726	ML62Q2736	ML62Q2746
160Kbyte			-	-	ML62Q2725	ML62Q2735	ML62Q2745
96Kbyte	8Kbyte		ML62Q2703	ML62Q2713	ML62Q2723	-	-
64Kbyte			ML62Q2702	ML62Q2712	ML62Q2722	-	-

Please see the last 2 pages “Notes for product usage” and “Notes” in this document on use with this product.

FEATURES

- CPU
  - 16-bit RISC CPU : nX-U16/100 (A35 core)
  - Instruction system : 16-bit length instructions
  - Instruction set : Transfer, arithmetic operations, comparison, logic operations, ultiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function (connect to the Lapis Technology on-chip debug emulator)
  - Minimum instruction execution time : 1 count of system clock
    Approximately 30.5µs/62.5ns/41.6ns (at 32.768kHz/16MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Signed or Unsigned is selectable

Parameter	Expression	Operation time [cycle]
Multiplication	16bit × 16bit	4
Division	32bit ÷ 16bit	8
	32bit ÷ 32bit	16
Multiply-accumulate (non-saturating, non-saturating)	16bit × 16bit + 32bit	4

- Operating voltage and temperature
  - Operating voltage : V_{DD} = 1.8 to 5.5V
  - Operating temperature : -40°C to +105°C

- Flash memory

Parameter	Program memory area	Data Flash memory area
Erase/Write count	100 cycles	10,000 cycles
Write unit	32bit (4byte)	8bit (1byte)
Erase unit	16Kbyte/1Kbyte	all area/128byte
Erase/Write temperature	0°C to +40°C	-40°C to +85°C

  - Background Operation (CPU can work while erasing and rewriting to the Data Flash memory area.)
  - The built-in on-chip debug function and ISP (In-System Programming) function enable Flash programming

    This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
    Super Flash® is a registered trademark of Silicon Storage Technology, Inc.

- Data RAM area
  - Rewrite unit: 8bit/16bit (1byte/2byte)
  - Parity check function is available (interrupt or reset is generatable at Parity error)

- Clock generation circuit
  - Low-speed clock (LSCLK)
    Internal low-speed RC oscillation (RC32K) : Approx. 32.768kHz
    External low-speed clock input (EXT32K) : Approx. 32.768kHz
    External low-speed crystal oscillation (XT32K) : Approx. 32.768kHz,
    Selectable 4 mode (Tough, Normal, Low power mode, and Ultra low power mode)
  - High-speed clock (HSCLK)
    PLL oscillation: selectable 3 oscillation frequency (24MHz, 16MHz, and 1MHz) by code option
  - Built-in dedicated clock generator (RC1K: Approx. 1.024kHz) for Watch Dog Timer (WDT)
  - High-speed time base clock (HTBCLK)
    Generates a clock with a period of 2 to 8 times that of HSCLK as a peripheral clock.

- Reset
  - System resets by reset input pin, Power-On Reset, voltage level supervisor (VLS), WDT overflow, WDT invalid clear, RAM parity error, and PC error (unused ROM area access (instruction access))
  - Software reset by BRK instruction (reset CPU only)
  - Reset the peripherals individually/collectively by software

- Power management
  - Optimal power management with various standby modes
    - STOP/STOP-D mode (All clocks are stopped), HALT-D mode (clocks for System and part of the peripheral block are stopped), HALT/HALT-H mode (clocks for System are stopped)
    - HALT-D mode is suitable for long term standby, HALT-H mode is suitable for short term Intermittent operation standby
  - Indivisual clock input control to the peripheral blocks by software
  - High-speed clock frequency (HSCLK) is configurable (1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of PLL clock, Max. 7steps)
  - Clock gear: High-speed system clock frequency is changeable dynamically (1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of HSCLK, Max. 6steps)

- Interrupt controller
  - Non-maskable interrupt source : 1 (Internal sources: Watchdog timer)
  - Maskable interrupt sources : Max. 50 (included the external interrupt 9 sources)
  - Four step interrupt levels
  - External interrupt ports (EXI) : 8 (selectable from Max.32 pins) with sampling filter and edge (rise, fall, both) selection.
  - Expanded external interrupt ports : Max. 4 with sampling filter and edge (rise, fall, both) selection.

- General-purpose ports (GPIO)
  - I/O port : Max. 92 (Including pins for shared functions)
  - Input port : 3 (Including one pin for shared on-chip debug and two pins for shared low speed crystal oscillation)
  - Carrier frequency output function (for IR communication)

- Watchdog timer (WDT) : 1 channel
  - Overflow period : 8selectable (7.8, 15.6, 31.3, 62.5, 125, 500, 2000, 8000ms)
  - Selectable window function (enable or disable):
    configurable clear enable period (50% or 75% of overflow period) with invalid clear
    When disable, Interrupts the first overflow and resets the second overflow
    When enable, reset occurs for the first overflow
  - Selectable WDT operation : select Enable or Disable by code option
  - Selectable operation during HALT/HALT-H mode and HALT-D mode (Continue counting/Stop counting)
  - WDT counter operation monitoring function (Readable WDT counter)

- Low-speed Time base counter (LTBC) : 2 channels
  - Generate 8 frequencies (128, 64, 32, 16, 8, 4, 2, 1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
  - 4 interrupts are generatable from 8 different frequencies internal pulse signals
  - One of internal pulse signals selected to interrupt is outputable from general purpose port (TBCO)

- Functional timer : Max. 8 channels
  - Various modes (continuous, one shot, capture, PWM with the same period and different duties, and complementary PWM output with the dead time)
  - Event trigger (external pin, 16bit timer, functional timer, LTBC, RC1K)
  - Selectable counter clock from various sources (divided by 1 to 8 of LSCLK, HSCLK, HTBCLK, and external clock)

- 16-bit General timers : Max. 8 channels
  - Timer output (toggled by overflow)
  - Selectable counter clock from various sources (divided by 1 to 8 of LSCLK, HSCLK, HTBCLK, LTBC, RC1K, and external clock)
  - Timer X is shared with waiting for the stability of low-speed crystal oscillation

- Synchronous Serial Port : Max. 7 channels (with FIFO: 1 channel, without FIFO: Max. 6 channels)
  - FIFO: 4steps for each transmitting and receiving
  - Selectable from Master and Slave
  - Selectable from LSB first or MSB first
  - Selectable 8-bit length or 16-bit length

- UART (Full-duplex communication mode): Max. 6 channels
  - Selectable from 5 to 8bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits, Positive logic or Negative logic, LSB first or MSB first
  - Sampling filter for receiving data and start bit
  - Built-in baud rate generator
    - 1bps to 4,800bps (Clock frequency is 32.768kHz)
    - 300bps to 2Mbps (Clock frequency is 16MHz)
    - 600bps to 3Mbps (Clock frequency is 24MHz)

- I^2C bus : 3 channels
  - Select from Master mode or Slave mode: 1 channel. Master mode only: 2 channels
  - Standard mode (100kbps), fast mode (400kbps) and 1Mbps mode (1Mbps)
  - 7bit address format
  - Master mode : Handshake (Clock synchronization), 10bit slave address format is supported
  - Slave mode : Clock stretch function

- Successive approximation type 12bit A/D converter (SA-ADC) : input Max. 16 channels
  - Conversion time: Min. 1.375μs / ch (When the V_{DD} is higher than 2.7V and the conversion clock is 16MHz)
  - Reference voltages are selectable from VDD pin input voltage or External reference voltage (VREF pin)
  - dedicated result register for each channel
  - Continuous conversion, Trigger start, Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage Level Supervisor (VLS) : 1 channel
  - Threshold voltage: selectable from 15 level (from 1.85V to 4.00V)
  - Functional Voltage level detection reset (VLS reset) or Functional Voltage level detection interrupt (VLS0 interrupt) is generatable
  - Equipped with single mode / with sampling filter / low consumption operation

- Audio playback function: 1channel
  - Audio synthesis method: 4bit ADPCM2, 8bit-non-linear PCM, 8bit Straight PCM, 16bit Straight PCM
  - Sampling frequency: 7.81kHz, 15.63kHz, 31.25kHz, 10.42kHz, 20.83kHz, 6.25kHz, 12.50kHz, 25.00kHz.

- LCD driver
  - Max. 480 dots (60seg x 8 com) *1
    ML62Q2702/ML62Q2703:
    24seg × 8com (com Max.), 29seg × 3com (seg Max.)
    ML62Q2712/ML62Q2713:
    27seg × 8com (com Max.), 32seg × 3com (seg Max.)
    ML62Q2722/ML62Q2723/ML62Q2725/ML62Q2726/ML62Q2727:
    35seg × 8com (com Max.), 40seg × 3com (seg Max.)
    ML62Q2735/ML62Q2736/ML62Q2737:
    45seg × 8com (com Max.), 50seg × 3com (seg Max.)
    ML62Q2745/ML62Q2746/ML62Q2747:
    60seg × 8com (com Max.), 65seg × 3com (seg Max.)
    *1 : Five pins are shared for common or segment, selectable by setting a SFR
  - 1/3 bias (built-in bias generation circuit)
  - Frame frequency selection (Approx. 32Hz, 38Hz, 64Hz, 75Hz, 128Hz, and 150Hz)
  - Four bias generation modes (Internal voltage boost, External capacitive voltage divide, Internal capacitive voltage divide, and External supply voltages)
  - Contrast adjustment (16 steps) is available in the Internal voltage boost mode.

- CRC (Cyclic Redundancy Check) generator
  - Generation equation: $X^{16}+X^{12}+X^{5}+1$
  - Selectable from LSB first or MSB first
  - Built-in Automatic program memory CRC calculation mode in HALT mode

- Safety Function
  - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
  - RAM/SFR guard
  - Automatic program memory CRC calculation
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - Clock mutual monitoring, WDT counter monitoring
  - SA-ADC test
  - Communication loop back test (UART, Synchronous serial port, I^2C bus (master))
  - GPIO test

- Packaging and shipping form

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Product name	
			Tray	Tape & Reel
48 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.50	ML62Q2702-xxxTBZWAY ML62Q2703-xxxTBZWAY	ML62Q2702-xxxTBZWBY ML62Q2703-xxxTBZWBY
48 pin plastic WQFN	7.0 × 7.0 (-)	0.50	ML62Q2702-xxxGDZW5AY ML62Q2703-xxxGDZW5AY	ML62Q2702-xxxGDZW5BY ML62Q2703-xxxGDZW5BY
52 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.65	ML62Q2712-xxxTBZWAY ML62Q2713-xxxTBZWAY	ML62Q2712-xxxTBZWBY ML62Q2713-xxxTBZWBY
64 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.50	ML62Q2722-xxxTBZWAY ML62Q2723-xxxTBZWAY ML62Q2725-xxxTBZWAY ML62Q2726-xxxTBZWAY ML62Q2727-xxxTBZWAY	ML62Q2722-xxxTBZWBY ML62Q2723-xxxTBZWBY ML62Q2725-xxxTBZWBY ML62Q2726-xxxTBZWBY ML62Q2727-xxxTBZWBY
64 pin plastic QFP	14.0 × 14.0 (16.0 × 16.0)	0.80	ML62Q2722-xxxGAZWAY ML62Q2723-xxxGAZWAY ML62Q2725-xxxGAZWAY ML62Q2726-xxxGAZWAY ML62Q2727-xxxGAZWAY	-
80 pin plastic QFP	14.0 × 14.0 (16.0 × 16.0)	0.65	ML62Q2735-xxxGAZWAY ML62Q2736-xxxGAZWAY ML62Q2737-xxxGAZWAY	-
100 pin plastic TQFP	14.0 × 14.0 (16.0 × 16.0)	0.50	ML62Q2745-xxxTBZWAY ML62Q2746-xxxTBZWAY ML62Q2747-xxxTBZWAY	-
100 pin plastic QFP	14.0 × 20.0 (19.0 × 25.0)	0.65	ML62Q2745-xxxGAZWAY ML62Q2746-xxxGAZWAY ML62Q2747-xxxGAZWAY	-

xxx: ROM code number, (NNN: ROM code is blank)

How To Read The Part Number

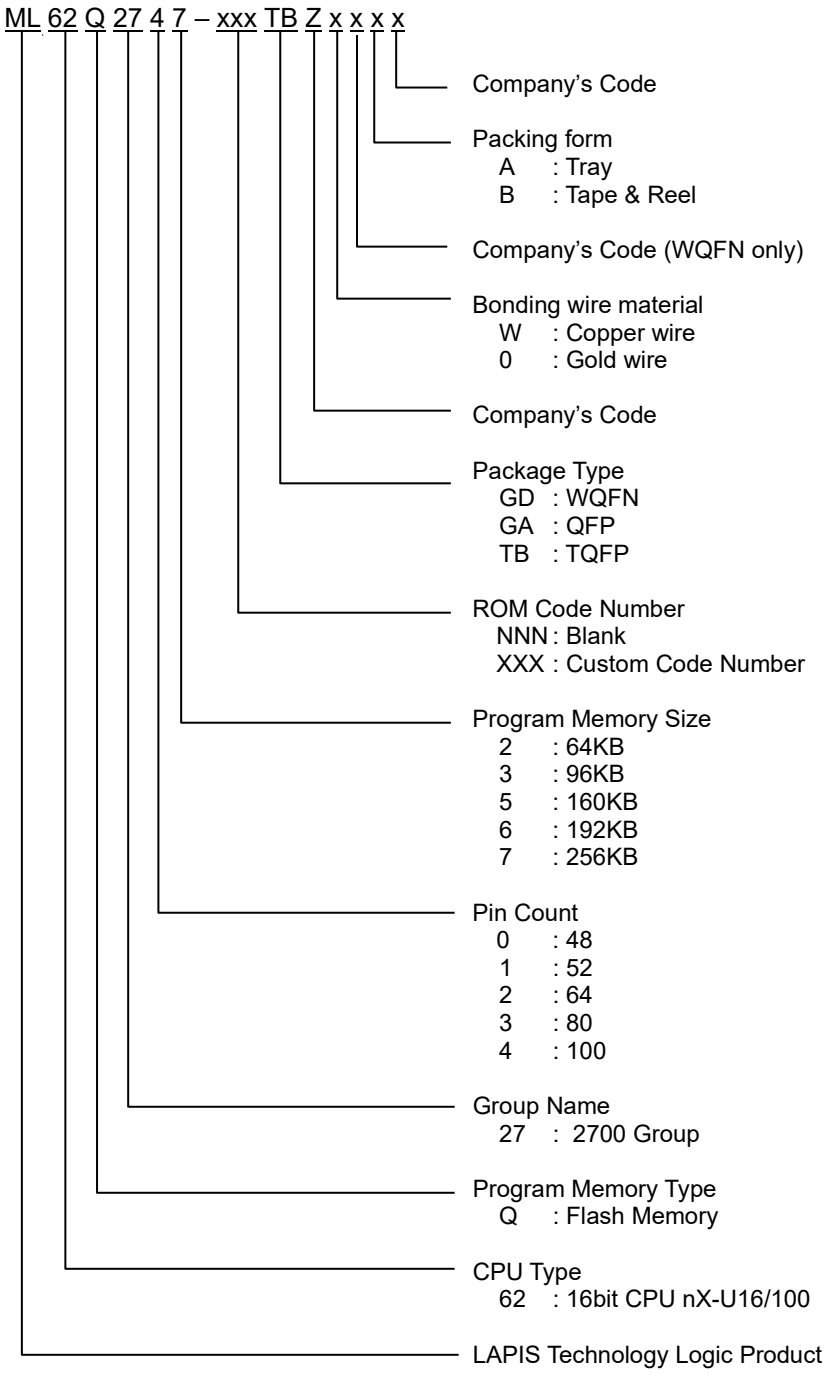


Figure 1 Part Number

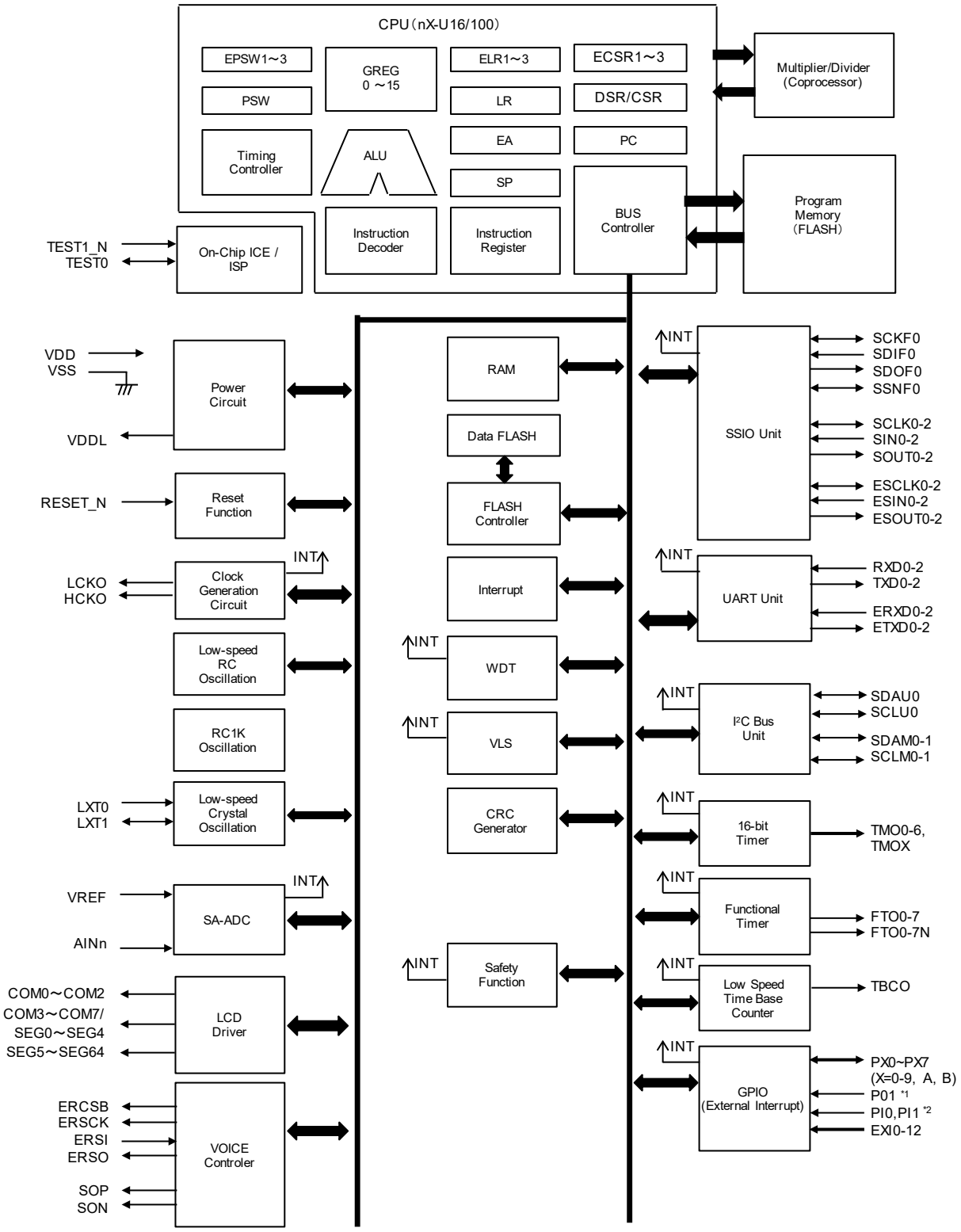
Main Function List

Table 2 Main Function List

Part number	Pin										Interrupt			Timer					Communication					Analog		Other
	Total pin count	Power pin	Reset Input pin	Debug Input port	General purpose Input pin *1	General purpose I/O pin (LED drive is supported)	LCD common/segment shared pin *2*3	LCD common pin *3	LCD segment pin *3	LCD bias pin	External interrupt pin	External interrupt source	Non maskable interrupt source	Internal maskable interrupt source	16bit Timer [ch]	16bit Functional Timer [ch]	16bit Functional Timer [Port]	Watchdog Timer [ch]	Time base counter [ch]	Synchronous serial (without FIFO) [ch]	Synchronous serial (with FIFO) [ch]	Full-duplex UART [ch]	I²C bus interface (Master only) [ch]	I²C bus unit (Master/Slave) [ch]	12bit Successive type A/D converter [ch]	Voltage Level Supervisor [ch]	Audio playback function
ML62Q2702	48	3	1	1	3	35	5	3	24	5	20	9	1	32	6	6	12	1	2	2	1	2	2	1	12	1	1
ML62Q2703																											
ML62Q2712	52					39			27		23																
ML62Q2713																											
ML62Q2722	64					51			35		32			41	8	8	16			6	1	6			16		
ML62Q2723																											
ML62Q2725																											
ML62Q2726																											
ML62Q2727																											
ML62Q2735	80	4				65			45		36																
ML62Q2736																											
ML62Q2737																											
ML62Q2745	100					85			60																16		
ML62Q2746																											
ML62Q2747																											

*1: Shared with pins for crystal oscillation and debug input.
*2: The LCD common/segment shared pins are shared for common or segment, selectable by setting a SFR
*3: All LCD drive pins are shared with general purpose I/O ports.

BLOCK DIAGRAM



*1 : Not available as the input port w hen connecting to the on-chip debug emulator.

*2 : Not available as the input port w hen connecting to the crystal resonator.

Figure 2 Block Diagram

PIN CONFIGURATION

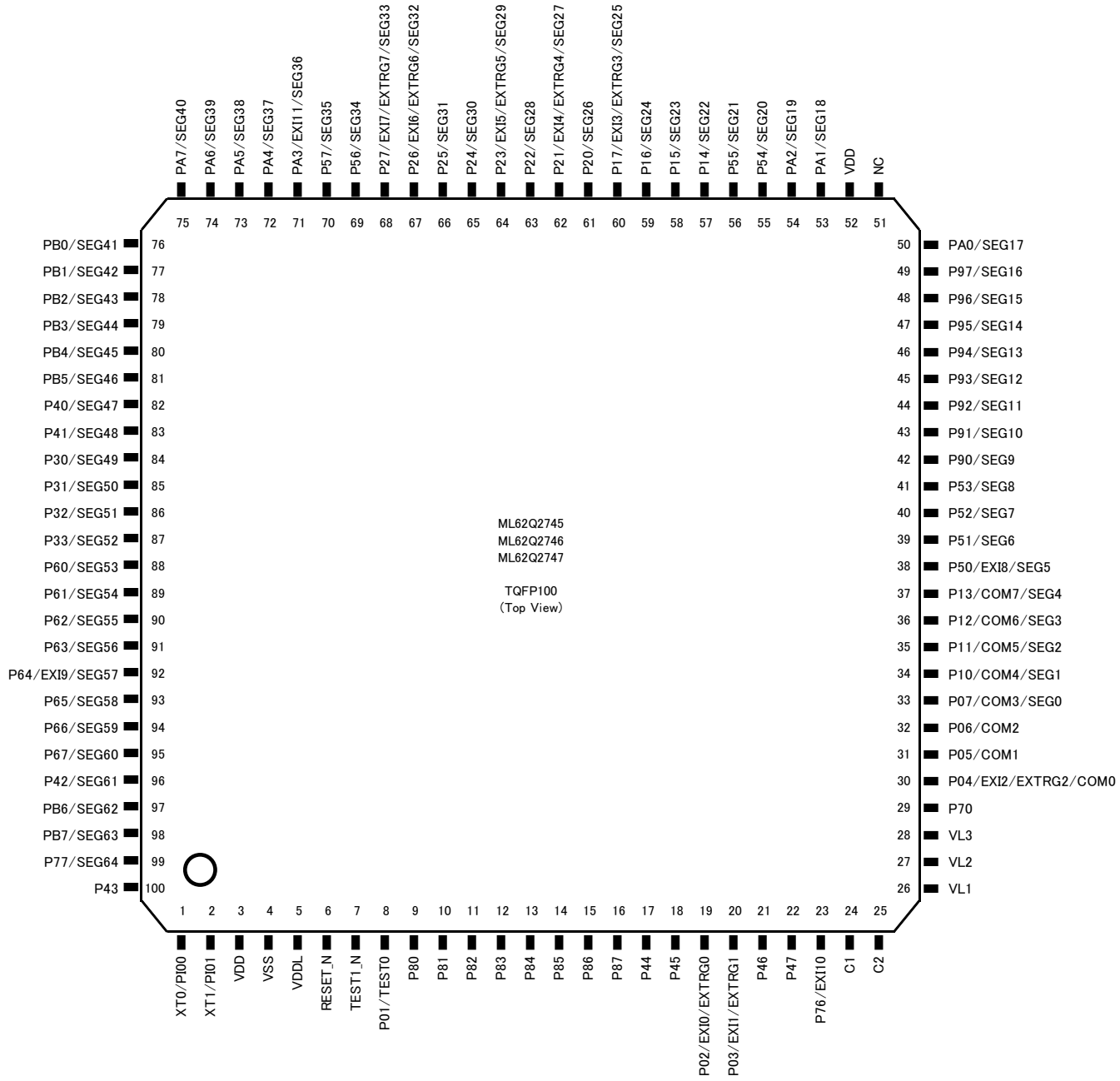


Fig.3-1 100 pin TQFP

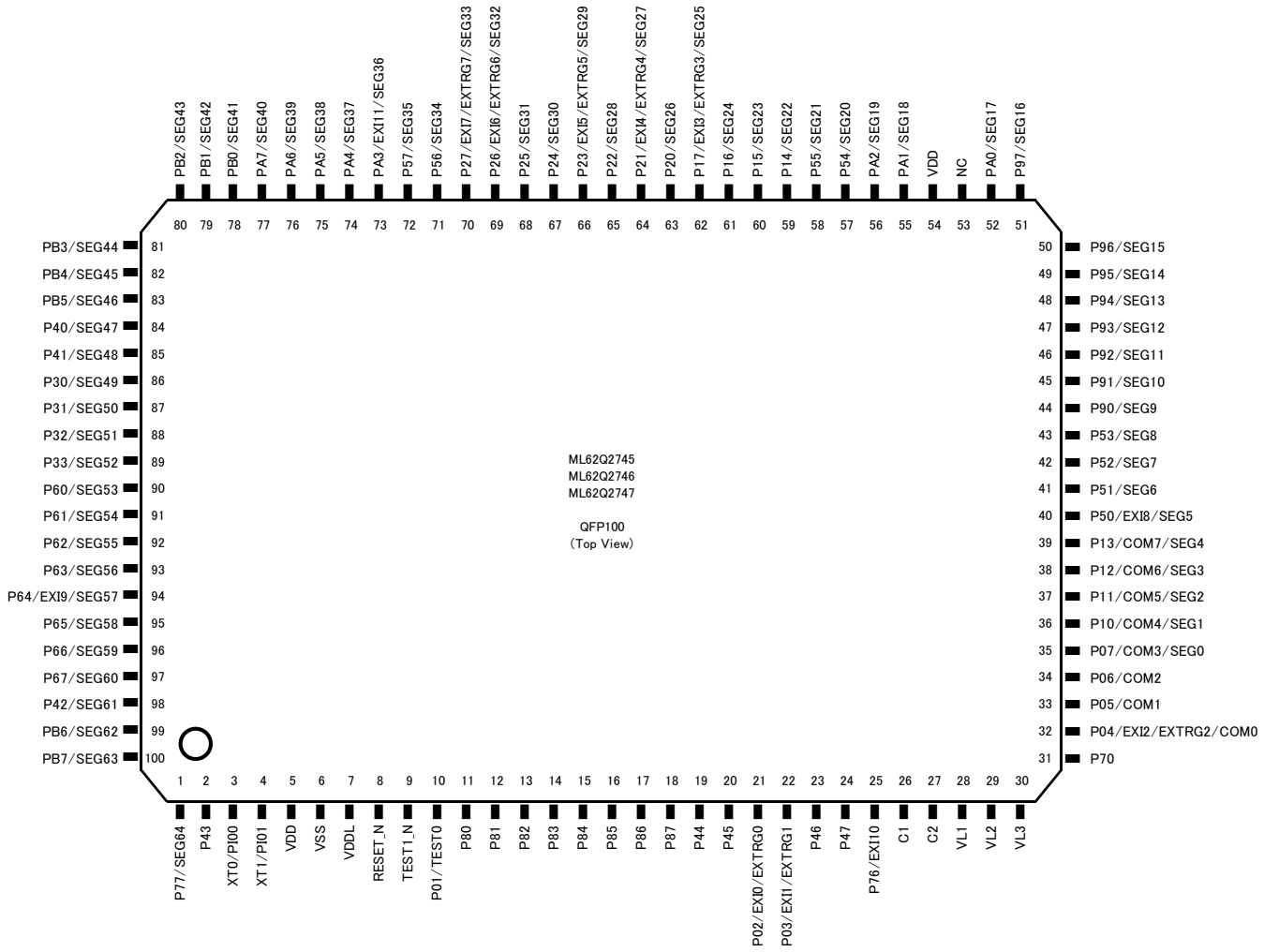


Fig.3-2 100 pin QFP

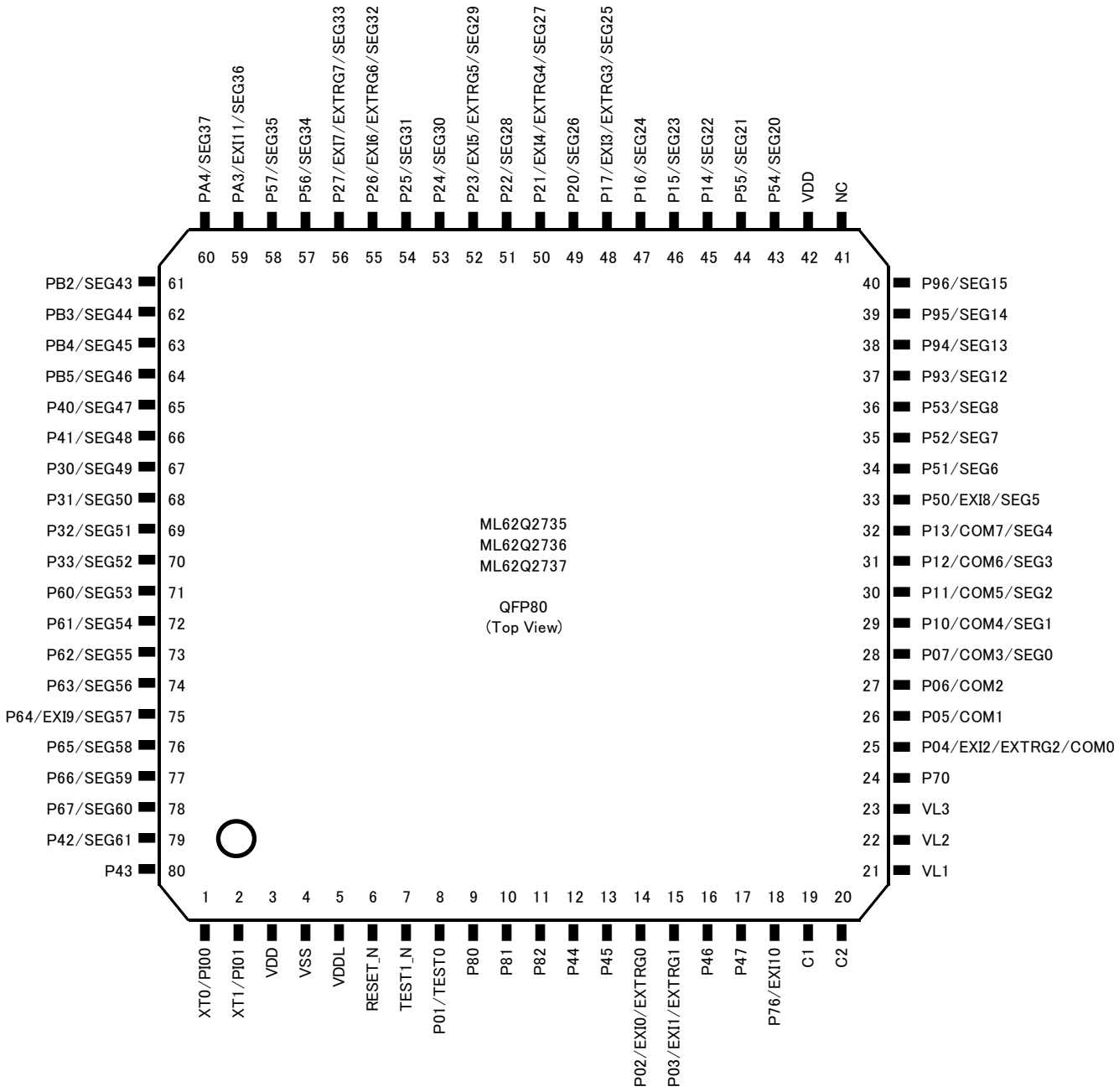


Fig.3-3 80 pin QFP

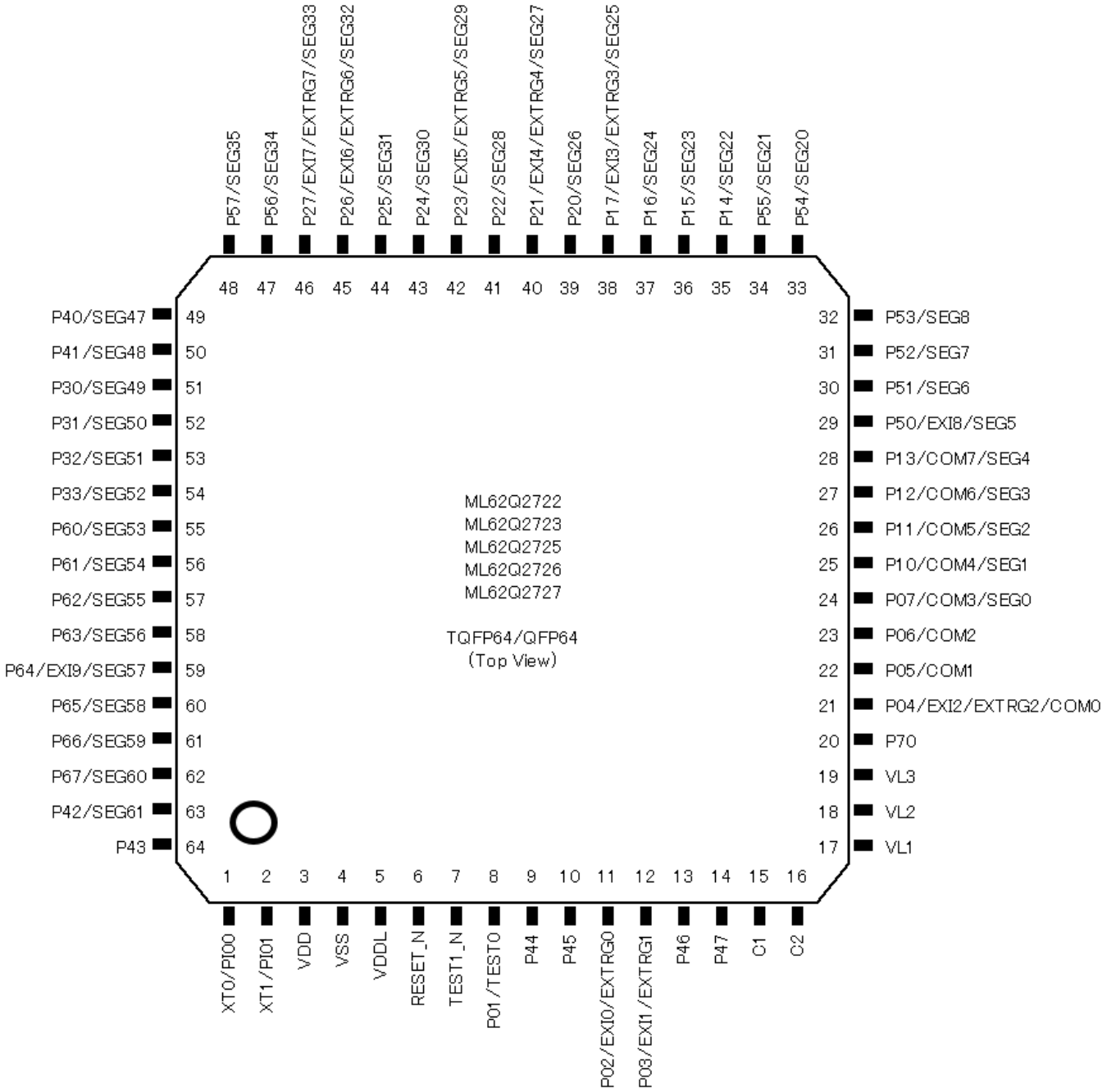


Fig.3-4 64 pin TQFP/QFP

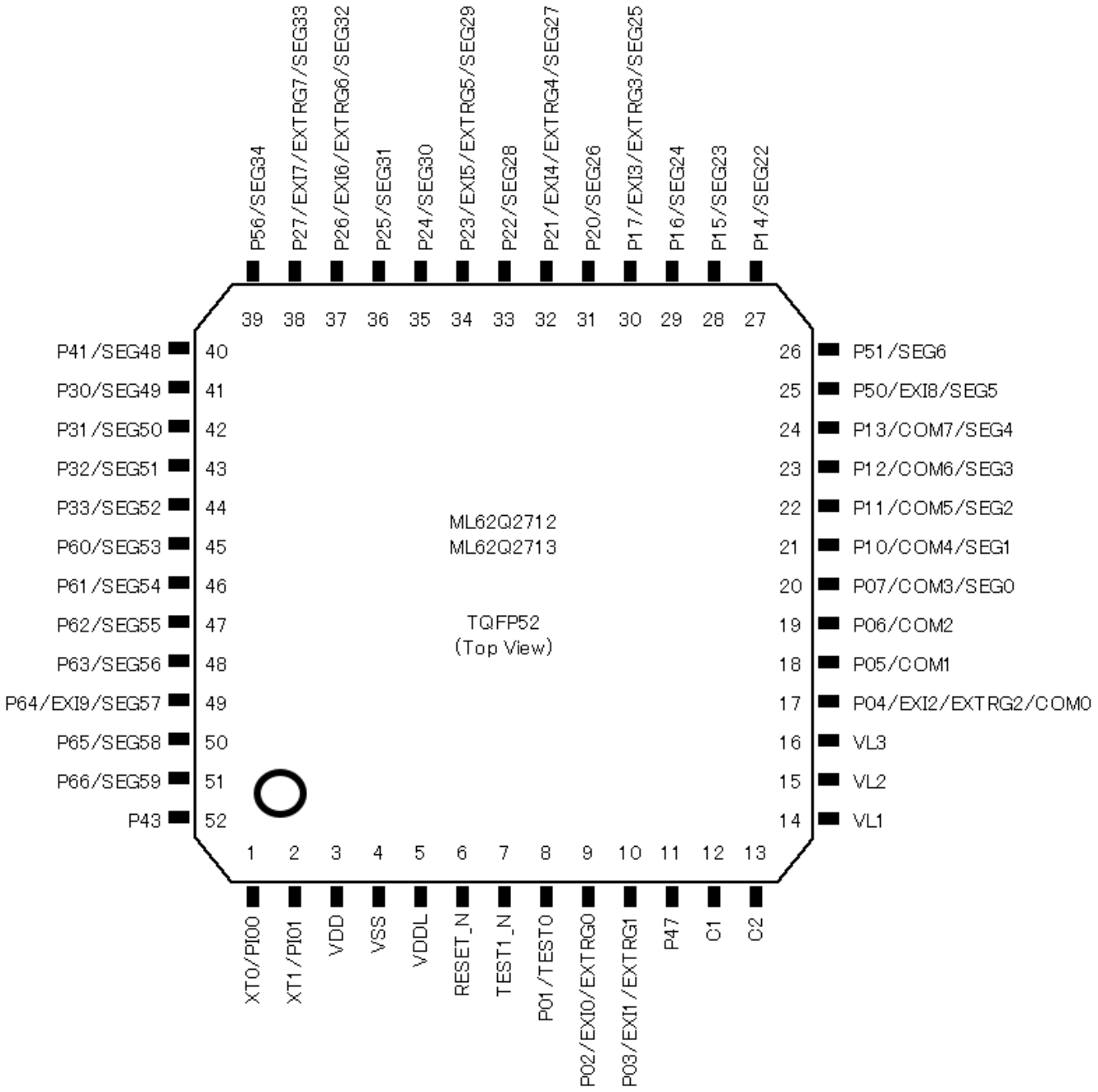


Fig.3-5 52 pin TQFP

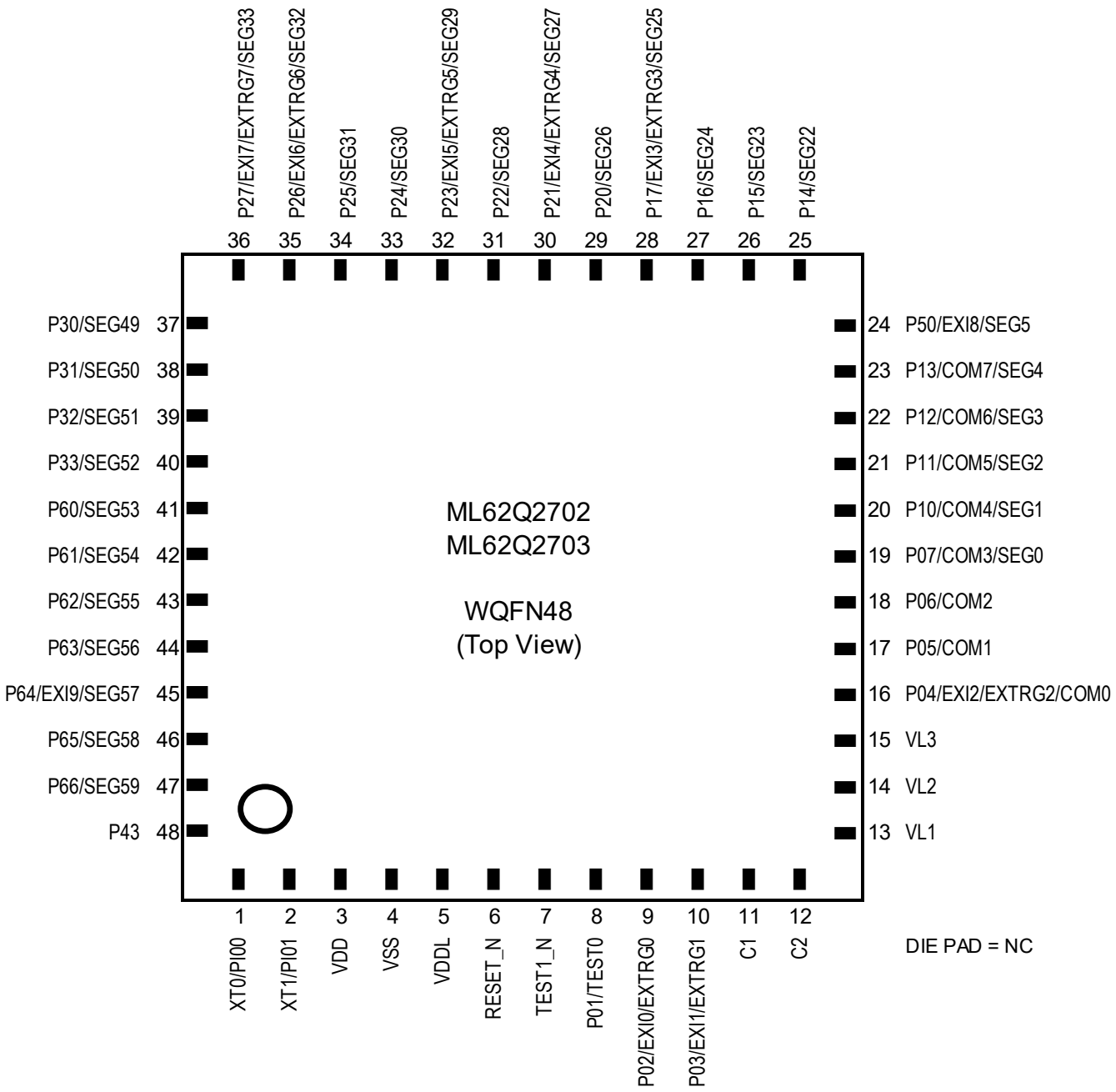


Fig.3-6 48 pin WQFN

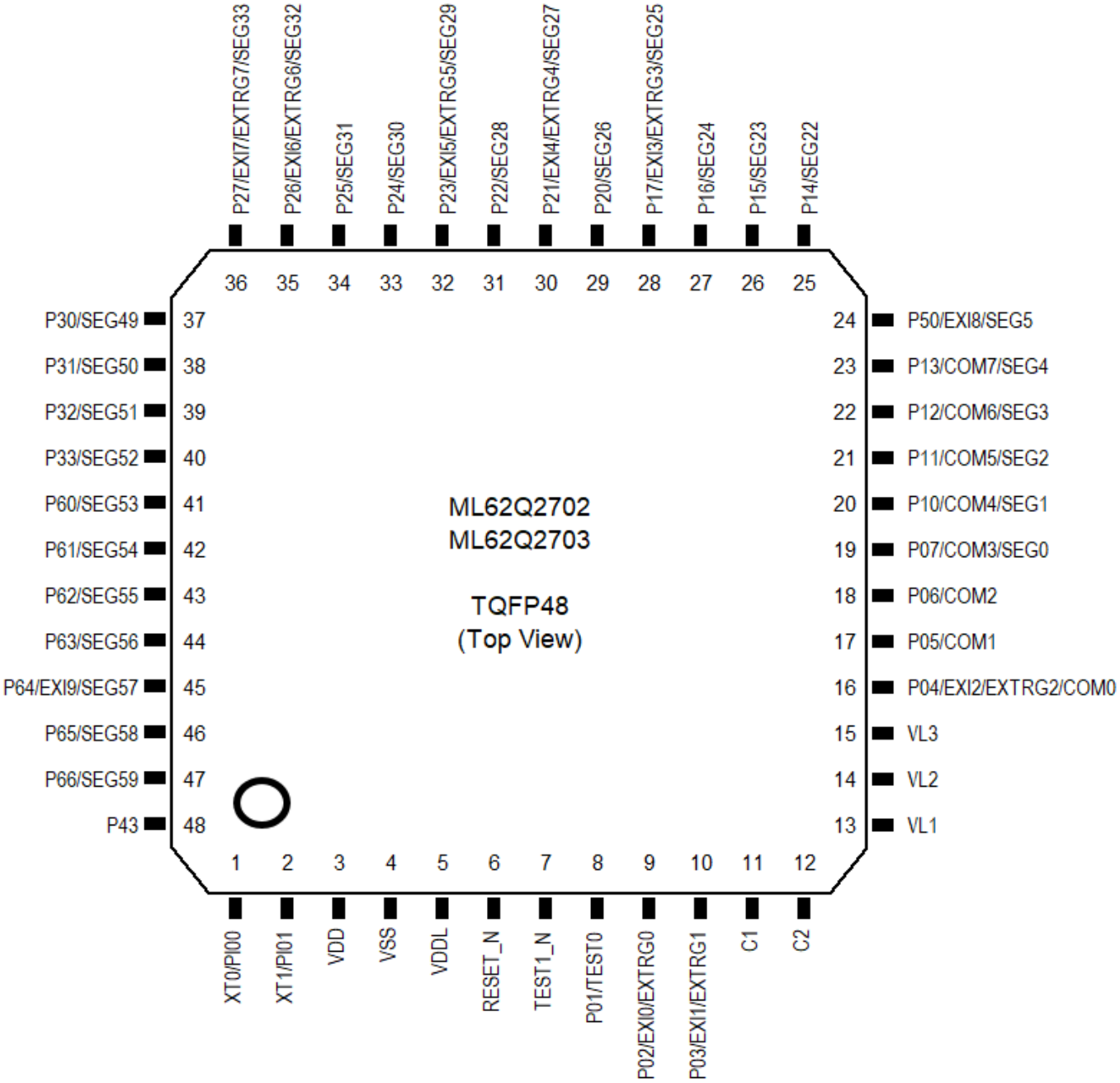


Fig.3-7 48 pin TQFP

PIN LIST

Table 3 Pin List (1/3)

Pin No.						LSI Pin name	Career frequency output	1st function	2nd function	3rd function	4th function	5th function	6th function	7th function
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100			EXI/ LCD/ ADC	SSIO	UART	I^2C	FTM	Timer	CLKOUT/ LTBC
3	3	3	3	3	5	VDD	-	-	-	-	-	-	-	-
-	-	-	42	52	54	VDD	-	-	-	-	-	-	-	-
4	4	4	4	4	6	VSS	-	-	-	-	-	-	-	-
-	-	-	41	51	53	NC	-	-	-	-	-	-	-	-
5	5	5	5	5	7	VDDL	-	-	-	-	-	-	-	-
1	1	1	1	1	3	XT0	-	PI00	-	-	-	-	-	-
2	2	2	2	2	4	XT1	-	PI01	-	-	-	-	-	-
6	6	6	6	6	8	RESET_N	-	-	-	-	-	-	-	-
7	7	7	7	7	9	TEST1_N	-	-	-	-	-	-	-	-
8	8	8	8	8	10	P01/TEST0	-	-	-	-	-	-	-	-
9	9	11	14	19	21	P02	-	EXI0	SIN0	RXD0	SCLU0	FTO0	-	LCKO
10	10	12	15	20	22	P03	●	EXI1 AIN11	SOUT0	TXD0	SDAU0	FTO0N	-	HCKO*1
16	17	21	25	30	32	P04	-	EXI2 COM0	SCLK0	-	SCLU0	-	TMO0	-
17	18	22	26	31	33	P05	-	COM1	SIN2*3	-	-	-	-	-
18	19	23	27	32	34	P06	-	COM2	SOUT2*3	-	SDAM0	-	-	-
19	20	24	28	33	35	P07	-	COM3 SEG0	SCLK2*3	RXD0	SCLM0	-	-	-
20	21	25	29	34	36	P10	-	COM4 SEG1	-	TXD0	-	-	-	-
21	22	26	30	35	37	P11	●	EXI1 COM5 SEG2	SCLK0	-	-	-	-	-
22	23	27	31	36	38	P12	-	EXI6 COM6 SEG3	SIN0	RXD0	-	-	TMO4	-
23	24	28	32	37	39	P13	●	EXI7 COM7 SEG4	SOUT0	TXD0	-	-	TMO1	TMO3
25	27	35	45	57	59	P14	-	EXI2 SEG22	SDIF0	-	-	-	-	ERSI*2
26	28	36	46	58	60	P15	-	SEG23	SSNF0	-	SDAU0	-	-	ERCSB*2
27	29	37	47	59	61	P16	-	SEG24	SCLK1	SDOF0*2	SCLU0	-	TMO5*3	ERSO*2
28	30	38	48	60	62	P17	-	EXI3 SEG25 AIN0	-	RXD0	-	FTO1	-	-
29	31	39	49	61	63	P20	●	SEG26 AIN1	-	TXD0	-	FTO1N	-	TBCO
30	32	40	50	62	64	P21	-	EXI4 SEG27 AIN2	SIN1	RXD1	-	FTO2	-	LCKO
31	33	41	51	63	65	P22	●	AIN3 SEG28	SOUT1	TXD1	SDAM0	FTO2N	-	HCKO*1
32	34	42	52	64	66	P23	-	EXI5 SEG29 VREF	SCLK1	-	SCLM0	-	TMO2	-
33	35	43	53	65	67	P24	-	SEG30 AIN4	SIN1	RXD1	-	-	-	-
34	36	44	54	66	68	P25	●	SEG31 AIN5	SOUT1	TXD1	-	-	-	-
35	37	45	55	67	69	P26	-	EXI6 SEG32 AIN6	-	RXD1	SDAU0	FTO3	-	-
36	38	46	56	68	70	P27	●	EXI7 SEG33 AIN7	-	TXD1	SCLU0	FTO3N	-	TBCO

*1: Assign each function; HCKO to only one LSI pin.
*2: No assignment to ML62Q2747/ML62Q2746/ML62Q2745/ML62Q2737/ML62Q2736/ML62Q2735/M62Q2727/ ML62Q2726/ML62Q2725.
*3: No assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.

Table 3 Pin List (2/3)

Pin No.						LSI Pin name	Career frequency output	1st function	2nd function	3rd function	4th function	5th function	6th function	7th function
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100			EXI/ LCD/ ADC	SSIO	UART	I^2C	FTM	Timer/ SOUND	CLKOUT/ LTBC/ SFMIF
37	41	51	67	84	86	P30	-	SEG49	ESIN1*3	-	-	-	-	-
38	42	52	68	85	87	P31	-	EXI1 SEG50	ESOUT1*3	-	-	-	-	TBCO
39	43	53	69	86	88	P32	-	SEG51	ESCLK1*3	RXD1	-	-	-	-
40	44	54	70	87	89	P33	●	EXI2 SEG52	-	TXD1	-	-	TMO3	-
-	-	49	65	82	84	P40	-	SEG47	-	ETXD2*3	-	-	-	-
-	40	50	66	83	85	P41	-	EXI0 SEG48	-	ERXD2*3	-	-	-	-
-	-	63	79	96	98	P42	-	SEG61	-	ETXD0*3	-	-	-	-
48	52	64	80	100	2	P43	-	EXI7 AIN10	-	-	-	-	-	TBCO
-	-	9	12	17	19	P44	-	EXI2	-	ERXD1*3	-	FTO3N	-	-
-	-	10	13	18	20	P45	-	EXI3	-	ETXD1*3	-	-	-	-
-	-	13	16	21	23	P46	-	EXI4	-	-	SDAU0	FTO1N	-	-
-	11	14	17	22	24	P47	-	EXI5	SCLK0	-	SCLU0	FTO1	-	-
24	25	29	33	38	40	P50	-	EXI8 SEG5	SCKF0	-	-	-	-	ERSCK
-	26	30	34	39	41	P51	-	EXI3 SEG6	SDOF0	-	-	-	-	ERSO
-	-	31	35	40	42	P52	-	EXI4 SEG7	SDIF0	ERXD1*3	-	-	-	ERSI
-	-	32	36	41	43	P53	-	EXI5 SEG8	SSNF0	ETXD1*3	-	-	-	ERCSB
-	-	33	43	55	57	P54	-	EXI0 SEG20	SCKF0	RXD2*3	-	FTO7*3	TMOX	-
-	-	34	44	56	58	P55	-	EXI1 SEG21	SDOF0	TXD2*3	-	FTO7N*3	-	-
-	39	47	57	69	71	P56	-	SEG34 AIN12*4	SIN2*3	RXD2*3	-	-	-	-
-	-	48	58	70	72	P57	-	SEG35 AIN13*4	SOUT2*3	TXD2*3	-	-	-	-
41	45	55	71	88	90	P60	-	SEG53	ESIN2*3	-	SCLM1	-	-	-
42	46	56	72	89	91	P61	-	EXI3 SEG54	ESOUT2*3	-	SDAM1	-	SOP	-
43	47	57	73	90	92	P62	-	SEG55	ESCK2*3	-	-	FTO4N	SON	-
44	48	58	74	91	93	P63	-	EXI4 SEG56	-	-	-	FTO4	-	-
45	49	59	75	92	94	P64	-	EXI9 SEG57	ESIN0*3	ERXD0*3	-	FTO5	-	-
46	50	60	76	93	95	P65	-	EXI5 SEG58 AIN8	ESOUT0*3	ETXD0*3	-	FTO5N	-	-
47	51	61	77	94	96	P66	-	SEG59 AIN9	ESCLK0*3	-	-	FTO6*3	-	-
-	-	62	78	95	97	P67	-	EXI6 SEG60	-	ERXD0*3	-	FTO6N*3	-	-
-	-	20	24	29	31	P70	-	EXI0	-	-	-	-	TMO6*3	-
15	16	19	23	28	30	VL3	-	-	-	-	-	-	-	-
14	15	18	22	27	29	VL2	-	-	-	-	-	-	-	-
13	14	17	21	26	28	VL1	-	-	-	-	-	-	-	-
12	13	16	20	25	27	C2	-	-	-	-	-	-	-	-
11	12	15	19	24	26	C1	-	-	-	-	-	-	-	-
-	-	-	18	23	25	P76	-	EXI10	-	-	-	-	-	-
-	-	-	-	99	1	P77	-	SEG64	-	-	-	-	-	-

*3: No assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.
*4: No assignment to ML62Q2727/ML62Q2726/ML62Q2725/ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ ML62Q2712/ML62Q2702.

Table 3 Pin List (3/3)

Pin No.						LSI Pin name	Career frequency output	1st function	2nd function	3rd function	4th function	5th function	6th function	7th function
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100			EXI/ LCD/ ADC	SSIO	UART	I^2C	FTM	Timer	CLKOUT/ LTBC
-	-	-	9	9	11	P80	-	EXI6	ESIN1*3	ERXD1*3	-	-	-	-
-	-	-	10	10	12	P81	-	EXI7	ESOUT1*3	ETXD1*3	-	-	-	-
-	-	-	11	11	13	P82	-	-	ESCLK1*3	-	-	-	-	-
-	-	-	-	12	14	P83	-	-	-	ERXD2*3	-	-	-	-
-	-	-	-	13	15	P84	-	-	-	ETXD2*3	-	-	-	-
-	-	-	-	14	16	P85	-	-	-	-	-	-	-	-
-	-	-	-	15	17	P86	-	-	-	-	-	FTO7*3	-	-
-	-	-	-	16	18	P87	-	-	-	-	-	FTO7N*3	-	-
-	-	-	-	42	44	P90	-	SEG9	-	-	-	-	-	-
-	-	-	-	43	45	P91	-	SEG10	-	-	-	-	-	-
-	-	-	-	44	46	P92	-	SEG11	-	-	-	-	-	-
-	-	-	37	45	47	P93	-	SEG12	ESIN1*3	ERXD1*3	-	FTO6*3	-	-
-	-	-	38	46	48	P94	-	SEG13	ESOUT1*3	ETXD1*3	-	FTO6N*3	-	-
-	-	-	39	47	49	P95	-	SEG14	ESCLK1*3	-	-	-	-	-
-	-	-	40	48	50	P96	-	SEG15	-	-	-	-	-	-
-	-	-	-	49	51	P97	-	SEG16	-	-	-	-	-	-
-	-	-	-	50	52	PA0	-	SEG17	-	-	-	-	-	-
-	-	-	-	53	55	PA1	-	SEG18	-	-	-	-	-	-
-	-	-	-	54	56	PA2	-	SEG19	-	-	-	-	-	-
-	-	-	59	71	73	PA3	-	EXI11 SEG36 AIN14	SCLK2*3	-	-	FTO7*3	-	-
-	-	-	60	72	74	PA4	-	SEG37 AIN15	-	-	-	FTO7N*3	-	-
-	-	-	-	73	75	PA5	-	SEG38	-	-	-	-	-	-
-	-	-	-	74	76	PA6	-	SEG39	-	-	-	-	-	-
-	-	-	-	75	77	PA7	-	SEG40	-	-	-	-	-	-
-	-	-	-	76	78	PB0	-	SEG41	-	-	-	-	-	-
-	-	-	-	77	79	PB1	-	SEG42	-	-	-	-	-	-
-	-	-	61	78	80	PB2	-	SEG43	ESIN2*3	ERXD2*3	-	-	-	-
-	-	-	62	79	81	PB3	-	SEG44	ESOUT2*3	ETXD2*3	-	-	-	-
-	-	-	63	80	82	PB4	-	SEG45	ESCLK2*3	-	-	-	-	-
-	-	-	64	81	83	PB5	-	SEG46	-	ERXD2*3	-	-	-	-
-	-	-	-	97	99	PB6	-	SEG62	-	-	-	-	-	-
-	-	-	-	98	100	PB7	-	SEG63	-	-	-	-	-	-

*3: No assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.

PIN DESCRIPTION

"I/O" Field in the below table define the pin type ("-" : power supply pin, "I" : Input pin, "O" : Out put pin, "I/O" bi-directional pin)

Table 4 Pin Description (1/5)

Function	Functional pin name	LSI pin name	I/O	Description
Power	-	VSS	-	Negative power supply pin (-) Define this terminal potential as V_{SS}.
	-	VDD	-	Positive power supply pin (+). Connect a capacitor C_V (more than 1µF) between this pin and VSS. Define this terminal potential as V_{DD}.
	-	VDDL	-	Power supply for internal logic (internal regulator's output). Connect a capacitor C_L (1µF) between this pin and VSS.
Debug ISP	TEST0	P01/ TEST0	I/O	Input/output for testing This pin which is shared with P01 is used as on-chip debug interface and ISP function. and is initialized as pull-up input mode by the system reset.
	TEST1_N	TEST1_N	I	Input for testing This pin is used as on-chip debug interface, ISP function, and is initialized as pull-up input mode by the system reset.
Reset	RESET_N	RESET_N	I	Reset input. Appling this pin "L" level shifts MCU to system reset mode. Appling this pin "H" level shifts MCU to program running mode. No pull-up resistor is built-in.
Not used	NC	NC	-	Open
General input port (GPI)	PI00, PI01	XT0, XT1	I	General purpose input. - High-impedance (initial value) - Input without Pull-up
	P01	P01/ TEST0	I	General purpose input. - Input with Pull-up (initial value) - Input without Pull-up Not available as general inputs when using the on-chip debug interface or ISP function.
General port (GPIO)	P02 to P07	P02 to P07	I/O	General purpose input/output - High-impedance (initial value) - Input with Pull-up - Input without Pull-up - CMOS output - N channel (N-ch) open drain output
	P10 to P17	P10 to P17		
	P20 to P27	P20 to P27		
	P30 to P33	P30 to P33		
	P40 to P47	P40 to P47		
	P50 to P57	P50 to P57		
	P60 to P67	P60 to P67		
	P70, P76 to P77	P70, P76 to P77		
	P80 to P87	P80 to P87		
	P90 to P97	P90 to P97		
	PA0 to PA7	PA0 to PA7		
	PB0 to PB7	PB0 to PB7		
Clock Input	XT0	XT0	I	Connect a Low speed (32.768kHz) crystal resonator and connect capacitors between the pin and VSS. When inputting a square wave clock, input from XT1 pin
	XT1	XT1	I/O	
Clock Output (7^{th} function)	HCKO	P03 P22	O	High-speed clock output.
	LCKO	P02 P21	O	Low-speed clock output.
	TBCO	P20 P27 P31 P43	O	Low-speed time base counter output.
Career frequency output	-	P03 P11 P13 P20 P22 P25 P27 P33	O	Career frequency output

Table 4 Pin Description (2/5)

Function	Functional pin name	LSI pin name	I/O	Description
External Interrupt (1st function)	EXI0	P02 P41 P54 P70	I	External Maskable Interrupt 0 Input
	EXI1	P03 P11 P31 P55	I	External Maskable Interrupt 1 Input
	EXI2	P04 P33 P14 P44	I	External Maskable Interrupt 2 Input
	EXI3	P17 P61 P51 P45	I	External Maskable Interrupt 3 Input
	EXI4	P21 P63 P52 P46	I	External Maskable Interrupt 4 Input
	EXI5	P23 P65 P53 P47	I	External Maskable Interrupt 5 Input
	EXI6	P26 P67 P12 P80	I	External Maskable Interrupt 6 Input
	EXI7	P27 P43 P13 P81	I	External Maskable Interrupt 7 Input
	EXI8	P50	I	External Maskable Interrupt 8 Input
	EXI9	P64	I	External Maskable Interrupt 9 Input
	EXI10	P76	I	External Maskable Interrupt 10 Input
	EXI11	PA3	I	External Maskable Interrupt 11 Input
16bit General Timer (6th function)	TMO0	P04	O	16bit General Timer 0 output
	TMO1	P13	O	16bit General Timer 1 output
	TMO2	P23	O	16bit General Timer 2 output
	TMO3	P13 P33	O	16bit General Timer 3 output
	TMO4	P12	O	16bit General Timer 4 output
	TMO5	P16	O	16bit General Timer 5 output
	TMO6	P70	O	16bit General Timer 6 output
	TMOX	P54	O	16bit General Timer X output
Functional Timer (5th function)	FTO0	P02	O	Functional Timer0 P output
	FTO0N	P03	O	Functional Timer0 N output
	FTO1	P17 P47	O	Functional Timer1 P output
	FTO1N	P20 P46	O	Functional Timer1 N output
	FTO2	P21	O	Functional Timer2 P output
	FTO2N	P22	O	Functional Timer2 N output
	FTO3	P26	O	Functional Timer3 P output
	FTO3N	P27 P44	O	Functional Timer3 N output
	FTO4	P63	O	Functional Timer4 P output
	FTO4N	P62	O	Functional Timer4 N output
	FTO5	P64	O	Functional Timer5 P output
	FTO5N	P65	O	Functional Timer5 N output
	FTO6	P66 P93	O	Functional Timer6 P output
	FTO6N	P67 P94	O	Functional Timer6 N output
	FTO7	P54 P86 PA3	O	Functional Timer7 P output
	FTO7N	P55 P87 PA4	O	Functional Timer7 N output
I2C Bus (4th function)	SCLU0	P02	I/O	I2C Unit0 Clock input/output
		P04		
		P16		
		P27		
		P47		
	SDAU0	P03	I/O	I2C Unit0 Data input/output
		P15		
		P26		
		P46		
	SCLM0	P07	I/O	I2C Master0 Clock input/output
		P23		
	SDAM0	P06	I/O	I2C Master0 Data input/output
		P22		
	SCLM1	P60	I/O	I2C Master1 Clock input/output
	SDAM1	P61	I/O	I2C Master1 Data input/output

Table 4 Pin Description (3/5)

Function	Functional pin name	LSI pin name	I/O	Description
UART (3rd function)	RXD0	P02 P07 P12 P17	I	UART0 received data input
	TXD0	P03 P10 P13 P20	O	UART0 transmission data output
	RXD1	P21 P24 P26 P32	I	UART1 received data input
	TXD1	P22 P25 P27 P33	O	UART1 transmission data output
	RXD2	P54 P56	I	UART2 received data input
	TXD2	P55 P57	O	UART2 transmission data output
	ERXD0	P64 P67	I	Expanded UART0 received data input
	ETXD0	P42 P65	O	Expanded UART0 transmission data output
	ERXD1	P44 P52 P80 P93	I	Expanded UART1 received data input
	ETXD1	P45 P53 P81 P94	O	Expanded UART1 transmission data output
	ERXD2	P41 P83 PB2 PB5	I	Expanded UART2 received data input
	ETXD2	P40 P84 PB3	O	Expanded UART2 transmission data output
Synchronous Serial Port (2nd function)	SCKF0	P50 P54	I/O	Synchronous serial0 (with FIFO) clock input/output
	SDIF0	P14 P52	I	Synchronous serial0 (with FIFO) data input
	SDOF0	P51 P55	O	Synchronous serial0 (with FIFO) data output
	SSNF0	P15 P53	I/O	Synchronous serial0 (with FIFO) slave select input/output
	SCLK0	P04 P11 P47	I/O	Synchronous serial0 clock input/output
	SIN0	P02 P12	I	Synchronous serial0 data input
	SOUT0	P03 P13	O	Synchronous serial0 data output
	SCLK1	P16 P23	I/O	Synchronous serial1 clock input/output
	SIN1	P21 P24	I	Synchronous serial1 data input
	SOUT1	P22 P25	O	Synchronous serial1 data output
	SCLK2	P07 PA3	I/O	Synchronous serial2 clock input/output
	SIN2	P05 P56	I	Synchronous serial2 data input
	SOUT2	P06 P57	O	Synchronous serial2 data output
	ESCLK0	P66	I/O	Expanded Synchronous serial0 clock input/output
	ESIN0	P64	I	Expanded Synchronous serial0 data input
	ESOUT0	P65	O	Expanded Synchronous serial0 data output
	ESCLK1	P32 P82 P95	I/O	Expanded Synchronous serial1 clock input/output
	ESIN1	P30 P80 P93	I	Expanded Synchronous serial1 data input
	ESOUT1	P31 P81 P94	O	Expanded Synchronous serial1 data output
	ESCLK2	P62 PB4	I/O	Expanded Synchronous serial2 clock input/output
	ESIN2	P60 PB2	I	Expanded Synchronous serial2 data input
	ESOUT2	P61 PB3	O	Expanded Synchronous serial2 data output
Audio Playback Function (6th function)	SOP	P61	O	P-side output of PWM for audio
	SON	P62	O	N-side output of PWM for audio
Serial Memory Interface (7th function)	ERSCK	P50	O	Serial clock output of external serial flash memory for audio
	ERSO	P16*1	O	Serial data output of external serial flash memory for audio
		P51		
	ERSI	P14	I	Serial data input for external serial flash memory for audio
		P52		
	ERCSB	P15	I/O	Chip select input/output of external serial flash memory for audio
		P53		
Successive approximation type A/D converter (SA-ADC) (1st function)	VREF	P23	I	SA-ADC external reference voltage input Define the potential of reference voltage for SA-ADC as V_{REF}
	AIN0 to AIN15	P17 P20 P21 P22 P24 P25 P26 P27 P65 P66 P43 P03 P56*2 P57*2 PA3 PA4	I	SA-ADC channel 0 to 15 analog input

*1: Assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.
Use the 3rd-func of P16.

*2: Assignment to ML62Q2747/ML62Q2737/ML62Q2746/ML62Q2736/ML62Q2745/ML62Q2735.

Table 4 Pin Description (4/5)

Function	Functional pin name	LSI pin name	I/O	Description
LCD Driver	COM0	P04	-	Common output
	COM1	P05	-	Common output
	COM2	P06	-	Common output
	COM3/SEG0	P07	-	Common/Segment output shared
	COM4/SEG1	P10	-	Common/Segment output shared
	COM5/SEG2	P11	-	Common/Segment output shared
	COM6/SEG3	P12	-	Common/Segment output shared
	COM7/SEG4	P13	-	Common/Segment output shared
	SEG5	P50	-	Segment output
	SEG6	P51	-	Segment output
	SEG7	P52	-	Segment output
	SEG8	P53	-	Segment output
	SEG9	P90	-	Segment output
	SEG10	P91	-	Segment output
	SEG11	P92	-	Segment output
	SEG12	P93	-	Segment output
	SEG13	P94	-	Segment output
	SEG14	P95	-	Segment output
	SEG15	P96	-	Segment output
	SEG16	P97	-	Segment output
	SEG17	PA0	-	Segment output
	SEG18	PA1	-	Segment output
	SEG19	PA2	-	Segment output
	SEG20	P54	-	Segment output
	SEG21	P55	-	Segment output
	SEG22	P14	-	Segment output
	SEG23	P15	-	Segment output
	SEG24	P16	-	Segment output
	SEG25	P17	-	Segment output
	SEG26	P20	-	Segment output
	SEG27	P21	-	Segment output
	SEG28	P22	-	Segment output
	SEG29	P23	-	Segment output
	SEG30	P24	-	Segment output
	SEG31	P25	-	Segment output
	SEG32	P26	-	Segment output
	SEG33	P27	-	Segment output
	SEG34	P56	-	Segment output
	SEG35	P57	-	Segment output
	SEG36	PA3	-	Segment output
	SEG37	PA4	-	Segment output
	SEG38	PA5	-	Segment output
	SEG39	PA6	-	Segment output
	SEG40	PA7	-	Segment output
	SEG41	PB0	-	Segment output
	SEG42	PB1	-	Segment output
	SEG43	PB2	-	Segment output

Table 4 Pin Description (5/5)

Function	Functional pin name	LSI pin name	I/O	Description
LCD Driver	SEG44	PB3	-	Segment output
	SEG45	PB4	-	Segment output
	SEG46	PB5	-	Segment output
	SEG47	P40	-	Segment output
	SEG48	P41	-	Segment output
	SEG49	P30	-	Segment output
	SEG50	P31	-	Segment output
	SEG51	P32	-	Segment output
	SEG52	P33	-	Segment output
	SEG53	P60	-	Segment output
	SEG54	P61	-	Segment output
	SEG55	P62	-	Segment output
	SEG56	P63	-	Segment output
	SEG57	P64	-	Segment output
	SEG58	P65	-	Segment output
	SEG59	P66	-	Segment output
	SEG60	P67	-	Segment output
	SEG61	P42	-	Segment output
	SEG62	PB6	-	Segment output
	SEG63	PB7	-	Segment output
	SEG64	P77	-	Segment output
	C1, C2	C1, C2	-	LCD bias power source generation capacitor connection Connect a capacitor
	VL1 to VL3	VL1 to VL3	-	LCD bias power source. Connect the capacitors (C_{L1}, C_{L2}, C_{L3}) between the pin and VSS.

TERMINATION OF UNUSED PINS

Table 5 shows the processing of unused pins.

Table 5 Termination of unused pins

Pin	pin termination
NC	Open
RESET_N	Connect to VDD
TEST1_N	Connect to VDD
P01/TEST0	Open with the initial condition of pulled-up input mode
XT0, XT1	Open with the initial condition of Hi-impedance (input/output invalid) mode.
P02 to P07 P10 to P17 P20 to P27 P30 to P33 P50 to P57 P60 to P67 P70, P76, P77 P80 to P87 P90 to P97 PA0 to PA7 PB0 to PB7	
C1, C2	Open
VL1, VL2	Open
VL3	Connect to VDD Connect a resistor (1kΩ or more) between VL3 and VDD is recommended.

[Note]

- **Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.**

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}			-0.3 to +2.0	
Power supply voltage 3	V_{L3}			-0.3 to +6.5	
Power supply voltage 4	V_{L1}, V_{L2}			-0.3 to V_{L3}+0.3*1	
Input voltage	V_{IN}			-0.3 to V_{DD}+0.3*1	
Output voltage1	V_{OUT1}			-0.3 to V_{DD}+0.3*1	
Output voltage2 (COM0 to COM7, SEG0 to SEG64)	V_{OUT2}			-0.3 to +6.5	
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*2	mA
			Total	-180*2	
"L" level output current	I_{OUTL}		1pin	+40	
			Total	+180	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	-		-55 to +150*3	°C

*1: 6.5V or lower
*2: The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*3: Please observe a storage conditions shown in the document "Board Mounting (soldering)" about the storage conditions until implementation.

[Note]

- **Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device.**
  These are stress ratings only and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambient)	Ta	-	-40 to +105	°C
Operating temperature (Chip-Junction)	Tj		-40 to +115	
Operating voltage 1	V_{DD}		1.8 to 5.5	V
Operating voltage 2	V_{L3}	External supply method	2.7 to 5.5	
Operating voltage 3	V_{L2}		2/3 x V_{L3}	
Operating voltage 4	V_{L1}		1/3 x V_{L3}	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.8 to 5.5V	30k to 25M	Hz
VDDL pin external capacitance	C_L	-	1.0 ±30%	µF
VL1, VL2, VL3 pin external capacitance	C_{L1}, C_{L2}, C_{L3}		0.47 ±30% or 1.0 ±30%	
C1 and C2 pin external capacitance	C_{12}		0.47 ±30% or 1.0 ±30%	

Thermal characteristics

The maximum chip-junction temperature, T_{jmax}, is estimated using the following equation.

$T_{j\,max} = T_{a\,max} + P_{D\,max} \times \theta_{ja}$
$T_{a\,max}$: maximum ambient temperature
$P_{D\,max}$: LSI maximum power dissipation
θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Parameter	Symbol	Package type	PCB condition		Unit
			L1	L2	
Thermal resistance	θ_{ja}	TQFP48	60.2	56.9	°C/W
		WQFN48	31.1	27.4	
		TQFP52	61.7	56.7	
		TQFP64	63.2	58.2	
		QFP64	47.2	43.3	
		QFP80	55.5	51.6	
		TQFP100	48.0	43.3	
		QFP100	104.7	101.3	

PCB conditions:

PCB name	L1	L2	Unit
PCB size (L / W / T)	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layers	1	2	layer
Wiring density	60% (top layer)	60% (top and bottom layer)	-
Wind condition	Windlessness (0m/s)		-

Current Consumption 1

Applicable Product: ML62Q2725, ML62Q2726, ML62Q2727, ML62Q2735, ML62Q2736, ML62Q2737, ML62Q2745, ML62Q2746, ML62Q2747

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Condition		Rating				Unit	Measuring circuit
	Operating mode	Status of clocks *1	Min.	Typ.*2	Max.			
					Tj≤+95°C	Tj≤+115°C		
IDD0	STOP-D	All clocks are stopped.	-	0.55	30	65	μA	1
IDD1	STOP	All clocks are stopped.	-	0.7	45	90		
IDD2-0R	HALT-D	RC32K is oscillating. XT32K/PLL are stopped.	-	0.9	30	65		
IDD2-0X	HALT-D	XT32K is oscillating in LP mode without noise-filter. RC32K/PLL are stopped.	-	1.25	30	70		
IDD2-1R	HALT (High speed oscillation off)	RC32K is oscillating. XT32K/PLL are stopped.	-	1.1	45	100		
IDD3	CPU running in wait-mode SYSCLK = 32.768kHz	RC32K is oscillating. XT32K/PLL are stopped.	-	11	-	110		
IDD4-H1	CPU running in wait-mode SYSCLK = 1MHz	PLL is oscillating as PLL1M mode. HSCLK = 1MHz	-	0.23	-	0.48	mA	
IDD4-H16		PLL is oscillating as PLL16M mode. HSCLK = 1MHz	-	0.33	-	0.63		
IDD5-H16	CPU running in wait-mode SYSCLK = 16MHz	PLL is oscillating as PLL16M mode. HSCLK = 16MHz	-	2.4	-	3.3		
IDD5-H24	CPU running in wait-mode SYSCLK = 24MHz	PLL is oscillating as PLL24M mode. HSCLK = 24MHz	-	3.5	-	4.8		

*1: LTBC0(ch0) and WDT is operating except IDD0/1, and all clock supply to peripheral circuits are stopped by block control.
LSCLK1 is stopped. The code option VLMD is "1".

*2: On the condition of V_{DD} = 3.0V, Ta = +25°C

Current Consumption 2

Applicable Product: ML62Q2702, ML62Q2703, ML62Q2712, ML62Q2713, ML62Q2722, ML62Q2723

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Condition		Rating				Unit	Measuring circuit
	Operating mode	Status of clocks *1	Min.	Typ.*2	Max.			
					Tj≤+95°C	Tj≤+115°C		
IDD0	STOP-D	All clocks are stopped.	-	0.4	25	60	μA	1
IDD1	STOP	All clocks are stopped.	-	0.5	40	85		
IDD2-0R	HALT-D	RC32K is oscillating. XT32K/PLL are stopped.	-	0.7	25	60		
IDD2-0X	HALT-D	XT32K is oscillating with LP mode, without noise-filter. RC32K/PLL are stopped.	-	1.1	25	65		
IDD2-1R	HALT (High speed oscillation off)	RC32K is oscillating. XT32K/PLL are stopped.	-	1	40	70		
IDD3	CPU running in wait-mode SYSCLK = 32.768kHz	RC32K is oscillating. XT32K/PLL are stopped.	-	10	-	80		
IDD4-H1	CPU running in wait-mode SYSCLK = 1MHz	PLL is oscillating as PLL1M mode. HSCLK = 1MHz	-	0.23	-	0.38	mA	
IDD4-H16		PLL is oscillating as PLL16M mode. HSCLK = 1MHz	-	0.34	-	0.5		
IDD5-H16	CPU running in wait-mode SYSCLK = 16MHz	PLL is oscillating as PLL16M mode. HSCLK = 16MHz	-	2.4	-	3.3		
IDD5-H24	CPU running in wait-mode SYSCLK = 24MHz	PLL is oscillating as PLL24M mode. HSCLK = 24MHz	-	3.4	-	4.8		

*1: LTBC0 and WDT is operating except IDD0/1, and all clock supply to peripheral circuits are stopped by block control. LSCLK1 is stopped. The code option VLMD is "1".

*2: On the condition of V_{DD} = 3.0V, Ta = +25°C

Low speed Crystal Oscillation

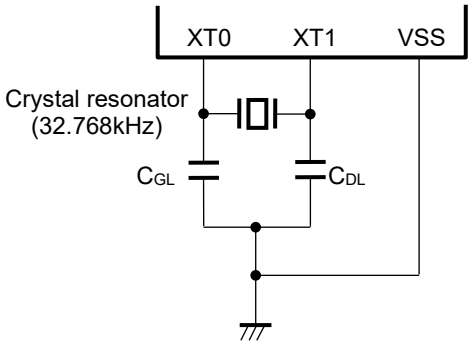
(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequency *1 *2	f_{XTL}	-	-	32.768	-	kHz
Crystal oscillation start time	T_{XTL}	-	-	-	2	s

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator, and the external capacitance (C_{GL}/C_{DL}). As those parameters changes depending the crystal resonator, The matching evaluation using the actual PCB is required . Ask crystal resonator manufacture the matching evaluation to confirm the oscillation characteristics.

*2: In order to obtain the expected oscillation characteristics, it is necessary to design a PCB that considers the material and wiring pattern of the circuit board, as well as the wiring capacitance and parasitic capacitance of quartz crystals and terminals, etc. See below as reference for a PCB design.
- Keep the wiring layout for configuring the external circuit as short as possible.
- In order to shorten the wiring to the crystal unit and the crystal oscillator external capacitance as much as possible, place the crystal unit and the crystal oscillator external capacitance in close proximity to the MCU.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
- The oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

Example of external circuit for Low speed Crystal Oscillation



External Clock Input

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	-	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input pulse width	t_{EXCKW}	-	14.5	-	-	µs

On-chip Oscillator 1

Applicable Product: ML62Q2725, ML62Q2726, ML62Q2727, ML62Q2735, ML62Q2736, ML62Q2737, ML62Q2745, ML62Q2746, ML62Q2747

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
RC32K frequency	f_{RCL1}	Ta = -40 to +85°C except HALT-D mode	Typ.-1.5%	32.768	Typ.+1.5%	kHz	1
	f_{RCL2}	HALT-D mode	Typ.-10%		Typ.+10%		
PLL oscillation frequency	f_{PLL1}	Ta = -40 to +85°C with RC32K PLL 24MHz mode	Typ.-1.5%	24.002560	Typ.+1.5%	MHz	
		Ta = -40 to +85°C with RC32K PLL 16MHz mode		16.007168			
		Ta = -40 to +85°C with RC32K PLL 1MHz mode		0.999424			
PLL oscillation stabilization time	T_{PLL}	-	-	-	2	ms	
		wake-up from HALT-H VLMD = 0 no temperature variation between before/after HALT-H	-	-	300	µs	
RC1K oscillation frequency (for WDT)	f_{RC1K}	Ta = -20 to +85°C	Typ.-15%	1.024	Typ.+15%	kHz	
		Ta = -40 to +105°C	Typ.-25%		Typ.+25%		

*: The frequency is the factory default specification. It may vary depending on the board mounting.

On-chip Oscillator 2

Applicable Product: ML62Q2702, ML62Q2703, ML62Q2712, ML62Q2713, ML62Q2722, ML62Q2723

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
RC32K frequency	f_{RCL1}	Ta = -40 to +85°C except HALT-D mode	Typ.-1.5% (Typ.-2.0%)*1	32.768	Typ.+1.5% (Typ.+2.0%)*1	kHz	1
	f_{RCL2}	HALT-D mode	Typ.-10%		Typ.+10%		
PLL oscillation frequency	f_{PLL1}	Ta = -40 to +85°C with RC32K PLL 24MHz mode	Typ.-1.5% (Typ.-2.0%)*1	24.002560	Typ.+1.5% (Typ.+2.0%)*1	MHz	
		Ta = -40 to +85°C with RC32K PLL 16MHz mode		16.007168			
		Ta = -40 to +85°C with RC32K PLL 1MHz mode		0.999424			
PLL oscillation stabilization time	T_{PLL}	-	-	-	2	ms	
		wake-up from HALT-H VLMD=0 no temperature variation between before/after HALT-H	-	-	300	µs	
RC1K oscillation frequency (for WDT)	f_{RC1K}	Ta = -20 to +85°C	Typ.-15%	1.024	Typ.+15%	kHz	
		Ta = -40 to +105°C	Typ.-25%		Typ.+25%		

*: The frequency is the factory default specification. It may vary depending on the board mounting.
*1 : 48pin WQFN package

Input / Output pin 1

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage1 "H"/"L" level (all input/output port)	VOH1	IOH1 = -10mA V_{DD} ≥ 4.5V		V_{DD} -1.5	-	-	V	2
		IOH1 = -1mA V_{DD} ≥ 1.8V		V_{DD} -0.5	-	-		
	VOL1	IOL1 = +10mA V_{DD} ≥ 4.5V		-	-	1.5		
		IOL1 = +1mA V_{DD} ≥ 1.8V		-	-	0.5		
Output voltage2 "L" level (all input/output port except P01/TEST0)	VOL2	When N-ch open drain output mode is selected	IOL2 = +15mA V_{DD} ≥ 4.5V	-	-	0.7		
			IOL2 = +8mA V_{DD} ≥ 3.0V	-	-	0.5		
			IOL2 = +3mA V_{DD} ≥ 2.0V	-	-	0.4		
			IOL2 = +2mA V_{DD} ≥ 1.8V	-	-	0.4		
Output voltage 3 LCD COM/SEG (COM0 to COM7) (SEG0 to SEG64)	VOH3M	V_{L3} = 3V, V_{L2} = 2V, V_{L1} = 1V	IOH3M = -0.03mA V_{L3} output	V_{L3} -0.2	-	-		
	VOMH3P		IOMH3P = +0.03mA V_{L2} output	-	-	V_{L2} +0.2		
	VOMH3M		IOMH3M = -0.03mA V_{L2} output	V_{L2} -0.2	-	-		
	VOML3P		IOML3P = +0.03mA V_{L1} output	-	-	V_{L1} +0.2		
	VOML3M		IOML3M = -0.03mA V_{L1} output	V_{L1} -0.2	-	-		
	VOL3P		IOL3P = +0.03mA V_{SS} output	-	-	0.2		

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current1 (RESET_N)	IIH1	VIH1 = V_{DD}	-	-	1	µA	4
	IIL1	VIL1 = V_{SS}	-1*1	-	-		
Input current2 (P01/TEST0, TEST1_N)	IIL2	VIL2 = V_{SS} (pull-up mode) *2	-1500*1	-300*1	-20*1		
	V/IIL2	VIL2 = V_{SS} (pull-up mode) *2	3.7	10	80	kΩ	
	IIH2Z	VIH2 = V_{DD} (High impedance mode)	-	-	1	µA	
	IIL2Z	VIL2 = V_{SS} (High impedance mode)	-1*1	-	-		
Input current3 (all input port except RESET_N, P01/TEST0, input/output port)	IIL3	VIL1 = V_{SS} (pull-up mode) *2	-250*1	-30*1	-2*1		
	V/IIL3	VIL1 = V_{SS} (pull-up mode) *2	22	100	800	kΩ	
	IIH3Z	VIH1 = V_{DD} (High impedance mode)	-	-	1	µA	
	IIL3Z	VIL1 = V_{SS} (High impedance mode)	-1*1	-	-		
Input current4 (PI00, PI01)	IIH4	VIH1 = V_{DD}	-	-	1		
	IIL4	VIL1 = V_{SS}	-1*1	-	-		
Input voltage1 (all input port, input/output port)	VIH1	-	0.7 × V_{DD}	-	V_{DD}	V	5
	VIL1	-	0	-	0.3 × V_{DD}		
Pin capacitance 1 (RESET_N, all input port, input/output port except P23)	CPIN1	f = 10kHz Ta = 25°C	-	-	10	pF	-
Pin capacitance 2 (P23)	CPIN2	f = 10kHz Ta = 25°C	-	-	20		-

*1: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*2: Measurement conditions: Typ.: V_{DD} = 3.0V, Max: V_{DD} = 1.8V, Min: V_{DD} = 5.5V

Input / Output pin 2

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V_{DD} ≥ 4.5V	-10*3*5	-	-	mA	3
			V_{DD} ≥ 1.8V	-1*3*5	-	-		
"H" level output total current1 *1*4	IOH3	Total of group A or B ** (duty ≤ 50%)	V_{DD} ≥ 4.5V	-90*5	-	-		
			V_{DD} ≥ 1.8V	-20*5	-	-		
		All pin total (duty ≤ 50%)	V_{DD} ≥ 4.5V	-180*5	-	-		
			V_{DD} ≥ 1.8V	-40*5	-	-		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V_{DD} ≥ 4.5V	-	-	10*3		
			V_{DD} ≥ 1.8V	-	-	1*3		
"L" level output current2 *6	IOL2	1pin (N-ch open drain output mode)	V_{DD} ≥ 4.5V	-	-	15*3		
			V_{DD} ≥ 3.0V	-	-	8*3		
			V_{DD} ≥ 2.0V	-	-	3*3		
			V_{DD} ≥ 1.8V	-	-	2*3		
"L" level output total current *2*4	IOL3	Total of group A or B ** (N-ch open drain output mode, duty ≤ 50%)	V_{DD} ≥ 4.5V	-	-	90		
			V_{DD} ≥ 3.0V	-	-	40		
			V_{DD} ≥ 2.0V	-	-	15		
			V_{DD} ≥ 1.8V	-	-	10		
		All pins total (N-ch open drain output mode, duty ≤ 50%)	V_{DD} ≥ 4.5V	-	-	180		
			V_{DD} ≥ 1.8V	-	-	20		
Output leak (all input/output port)	IOOH	VOH = V_{DD} (High impedance mode)		-	-	+1	μA	
	IOOL	VOL = V_{SS} (High impedance mode)		-1*5	-	-		

**: Group A is "P02 to P07, P10 to P13, P44 to P47, P50 to 53, P70, P76, P80 to 87, P90 to 97, PA0",
Group B is "P14 to P17, P20 to P27, P30 to P33, P40 to P43, P54 to P57, P60 to P67, P77, PA1 to PA7, PB0 to PB7"

*1: Sink-out current from VDD to the output pin, which can guarantee the device operation.

*2: Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.

*3: Do not exceed total current.

*4: The total current is on the condition of Duty ≤ 50% (same applies to IOH1).
When the duty > 50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
[Example] When IOL3 = 100mA and n = 80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.

*5: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

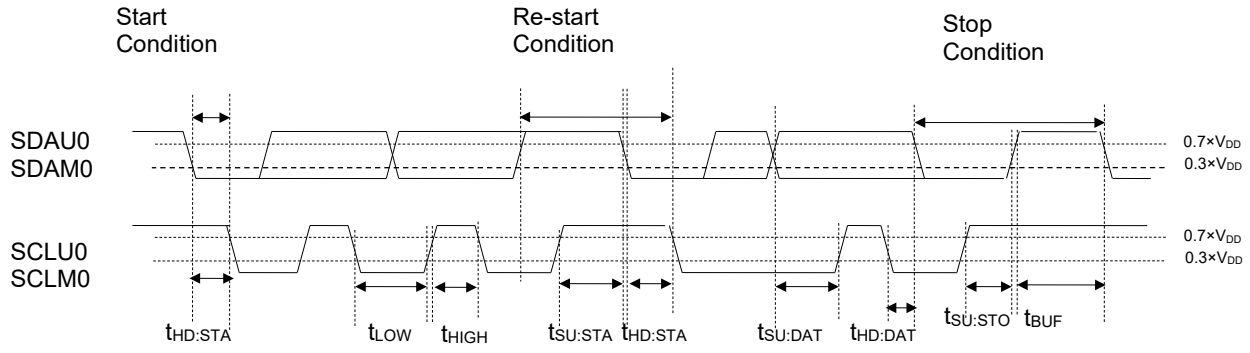
*6: These values are satisfied with VOH1, VOL1 and VOL2.

I²C Bus Interface

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Rating									Unit
		Standard Mode			Fast Mode			1Mbps Mode			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Voltage	V_{DD}	1.8	-	5.5	1.8	-	5.5	2.7	-	5.5	V
SCL clock frequency	f_{SCL}	0	-	100	0	-	400	0	-	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	4.0	-	-	0.6	-	-	0.26	-	-	μs
SCL "L" level time	t_{LOW}	4.7	-	-	1.3	-	-	0.5	-	-	
SCL "H" level time	t_{HIGH}	4.0	-	-	0.6	-	-	0.26	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	4.7	-	-	0.6	-	-	0.26	-	-	
SDA hold time	$t_{HD:DAT}$	0	-	-	0	-	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	0.25	-	-	0.1	-	-	0.1	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	4.0	-	-	0.6	-	-	0.26	-	-	
Bus-free time	t_{BUF}	4.7	-	-	1.3	-	-	0.5	-	-	

When using the I²C as the master, configure the I²C master 0 mode register (I2M0MOD) and I²C bus 0 mode register (master side, I2U0MOD) so that meet these specifications.



Synchronous Serial Port

Slave mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle	t_{SCYC}	-	1*1	-	-	µs
SCLK input pulse width	t_{SW}	-	t_{SCYC} x 0.4	-	-	
SOUT output delay time	t_{SD}	V_{DD} ≥ 2.4V	-	-	100	ns
		V_{DD} ≥ 1.8V	-	-	200	
SIN input setup time	t_{SS}	-	80	-	-	
SIN input hold time	t_{SH}	-	50	-	-	

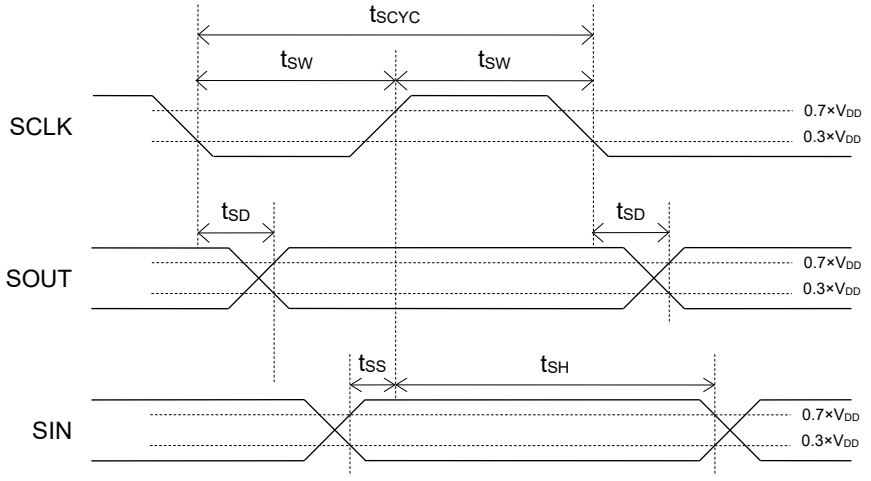
*1: Need input cycles of SYSCLK x 4 or longer

Master mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK output cycle	t_{SCYC}	V_{DD} ≥ 2.4V	250	SCLK*2	-	ns
		V_{DD} ≥ 1.8V	500	SCLK*2	-	
SCLK output pulse width	t_{SW}	-	t_{SCYC}×0.4	t_{SCYC}×0.5	t_{SCYC}×0.6	
SOUT output delay time	t_{SD}	V_{DD} ≥ 2.4V	-	-	100	
		V_{DD} ≥ 1.8V	-	-	160	
SIN input setup time	t_{SS}	V_{DD} ≥ 2.4V	120	-	-	
		V_{DD} ≥ 1.8V	180	-	-	
SIN input hold time	t_{SH}	V_{DD} ≥ 2.4V	80	-	-	
		V_{DD} ≥ 1.8V	100	-	-	

*2: Clock cycle selected by bit12 to 8 (S0CK4 to 0) of the serial port 0 mode register (SIO0MOD)



Synchronous Serial Port with FIFO

Slave mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCKF input cycle	t_{SCYC}	-	1*1	-	-	µs
SCKF input pulse width	t_{SW}	-	t_{SCYC} x 0.4	-	-	
SDOF output delay time	t_{SD}	V_{DD} ≥ 2.4V	-	-	100	ns
		V_{DD} ≥ 1.8V	-	-	200	
SDIF input setup time	t_{SS}	-	80	-	-	
SDIF input hold time	t_{SH}	-	50	-	-	

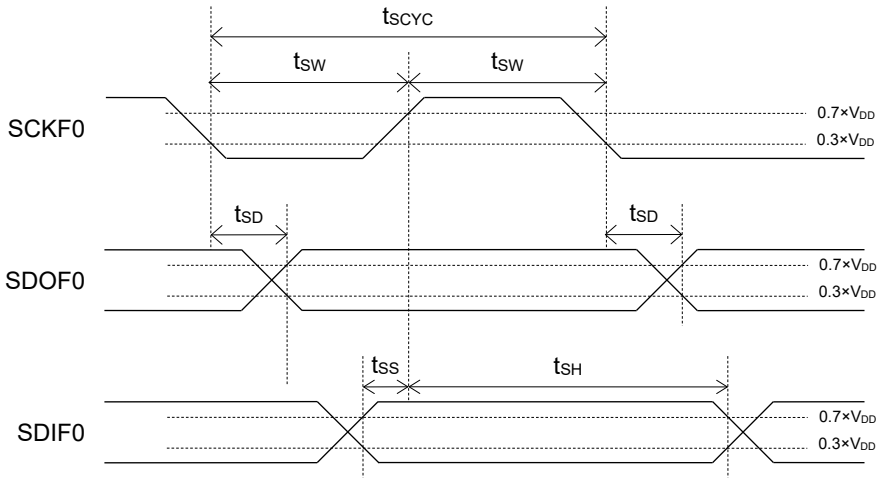
*1: Need input cycles of SYSCLK x 4 or longer

Master mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCKF output cycle	t_{SCYC}	V_{DD} ≥ 2.4V	250	SCLK*2	-	ns
		V_{DD} ≥ 1.8V	500	SCLK*2	-	
SCKF output pulse width	t_{SW}	-	t_{SCYC}×0.4	t_{SCYC}×0.5	t_{SCYC}×0.6	
SDOF output delay time	t_{SD}	V_{DD} ≥ 2.4V	-	-	100	
		V_{DD} ≥ 1.8V	-	-	160	
SDIF input setup time	t_{SS}	V_{DD} ≥ 2.4V	120	-	-	
		V_{DD} ≥ 1.8V	180	-	-	
SDIF input hold time	t_{SH}	V_{DD} ≥ 2.4V	80	-	-	
		V_{DD} ≥ 1.8V	100	-	-	

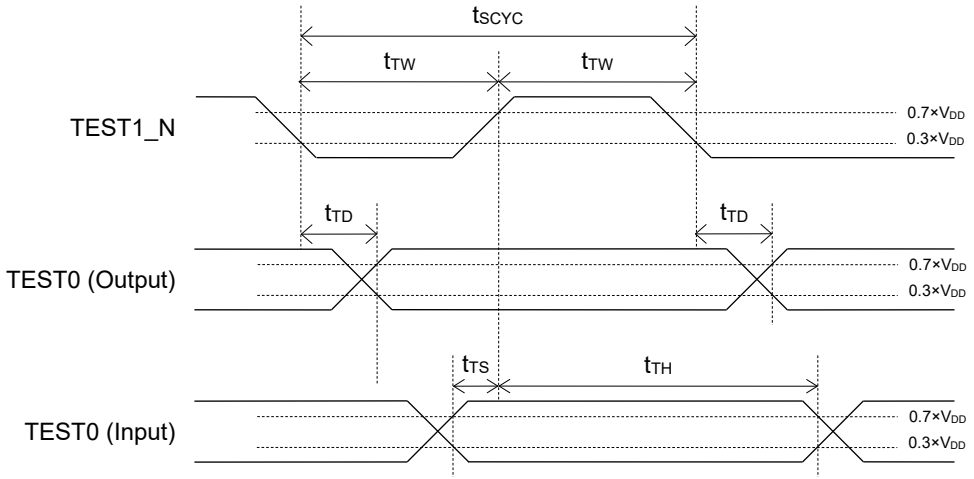
*2: Clock cycle selected by bit9 to 0 (SF0BR9 to 0) of the SIOF0 baud rate register (SF0BRR)



ISP interface

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
TEST1_N clock input cycle	t_{TCYC}	-	400	-	660	ns
TEST1_N clock input pulse width	t_{TW}	-	t_{TCYC} x 0.4	-	-	
TEST0 output delay time	t_{TD}	$V_{DD} \geq 2.4V$	-	-	80	
		$V_{DD} \geq 1.8V$	-	-	200	
TEST0 input setup time	t_{TS}	-	80	-	-	
TEST0 input hold time	t_{TH}	-	50	-	-	



EXI0 to 7 Timer Clock Input

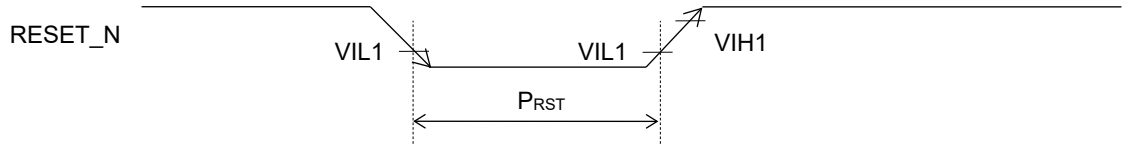
(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXI}	-	-	-	3	MHz
Input pulse width	t_{WEXI}	-	135	-	-	ns

Reset

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Reset pulse width*1	P_{RST}	-	10	-	-	µs	1

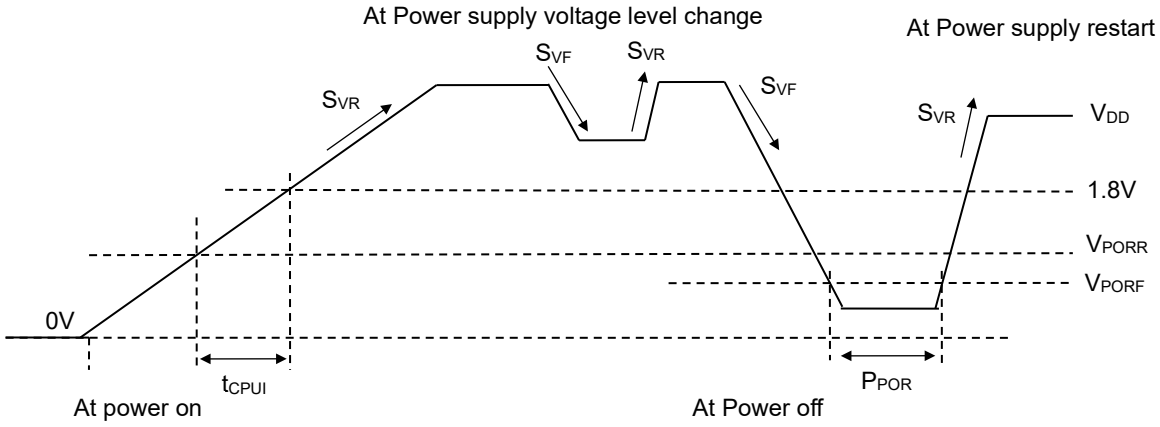


[Note]
- **RESET_N input shorter pulse than the Reset pulse width (P_{RST}) valid time should be avoided. The shorter pulse input may cause unexpected behavior.**

Slope of Power supply and Power On Reset

(V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Power supply voltage rising inclination	S_{VR}	-	-	-	60	V/ms	1
Power supply voltage falling inclination	S_{VF}	-	-	-	2		
Power on reset detection voltage	V_{PORR}	At Power up (rising)	1.50	1.63	1.80	V	
	V_{PORF}	At Power down (falling)	1.35	1.60	1.75		
Power on reset minimum pulse width	P_{POR}	-	500	-	-	µs	
CPU operation start time (from the release of reset to the CPU starts to run)	t_{CPUI}	-	13	21	35	ms	-



[Note]
- **If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction. Apply prevent measurement such as bypass capacitors or external reset input, and so on.**
- **Set V_{DD} to 1.8V or higher before starting CPU operation.**

VLS

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating						Unit	Measuring circuit
			Falling			Rising				
			V_{VLSF}			V_{VLSR}				
		VLS0LV[*1]	Min.	Typ.	Max.	Min.	Typ.	Max.		
VLS threshold voltage	V_{VLSR} V_{VLSF}	0H	3.83	3.99	4.15	3.84	4.05	4.26	V	1
		1H	3.53	3.68	3.83	3.55	3.74	3.93		
		2H	2.92	3.05	3.18	2.94	3.10	3.26		
		3H	2.84	2.96	3.08	2.85	3.01	3.17		
		4H	2.72	2.84	2.96	2.74	2.89	3.04		
		5H	2.65	2.76	2.87	2.66	2.80	2.94		
		6H	2.55	2.66	2.77	2.56	2.70	2.84		
		7H	2.43	2.54	2.65	2.45	2.58	2.71		
		8H	2.35	2.45	2.55	2.36	2.49	2.62		
		9H	2.25	2.35	2.45	2.27	2.39	2.51		
		AH	2.15	2.24	2.33	2.16	2.28	2.40		
		BH	2.07	2.16	2.25	2.08	2.19	2.30		
		CH	1.96	2.05	2.14	1.98	2.09	2.20		
		DH	1.87	1.95	2.03	1.89	1.99	2.09		
		EH	1.77	1.85	1.93	1.78	1.88	1.98		

[*1]: Bit3 to Bit0 of voltage level detection circuit 0 level register (VLS0LV).

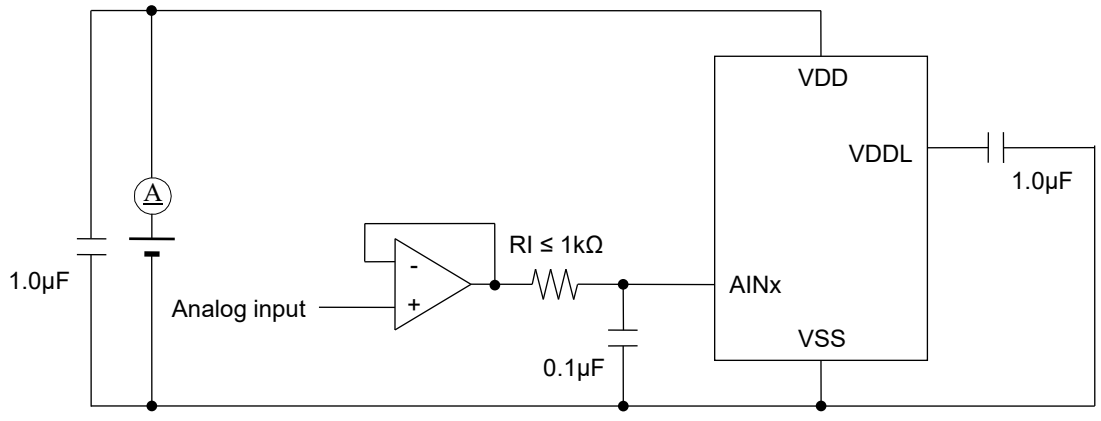
(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS current consumption	I_{VLS}	-	-	10	-	nA	1

Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit
Resolution	n_{AD}	-		-	-	12	bit
Conversion clock	f_{ADCLK}	nominal value, V_{DD} ≥ 2.7V, V_{REF} ≥ 2.7V		32.768	-	16000	kHz
		nominal value, V_{DD} ≥ 2.4V, V_{REF} ≥ 2.4V		32.768	-	8000	
		nominal value, V_{DD} ≥ 1.8V, V_{REF} ≥ 1.8V		32.768	-	1000	
Conversion time	t_{CONV}	f_{ADCLK} = 16MHz		1.375	-	-	µs
		f_{ADCLK} = 32.768kHz		-	518.799	-	
SA-ADC reference potential	V_{REF}	V_{DD} ≥ V_{REF}		1.8	-	V_{DD}	V
Overall error	-	4.5V ≤ V_{REF} ≤ 5.5V		-6.5	-	+6.5	LSB
Integral non-linearity error	INL_{AD}	f_{ADCLK} = 16MHz	2.7V ≤ V_{REF}	-4	-	+4	
		f_{ADCLK} = 8MHz	2.4V ≤ V_{REF}	-6	-	+6	
		f_{ADCLK} = 1MHz	1.8V ≤ V_{REF}	-8	-	+8	
		f_{ADCLK} = 32.768kHz	1.8V ≤ V_{REF}	-8	-	+8	
Differential non-linearity error	DNL_{AD}	f_{ADCLK} = 16MHz	2.7V ≤ V_{REF}	-3	-	+3	
		f_{ADCLK} = 8MHz	2.4V ≤ V_{REF}	-5	-	+5	
		f_{ADCLK} = 1MHz	1.8V ≤ V_{REF}	-7	-	+7	
		f_{ADCLK} = 32.768kHz	1.8V ≤ V_{REF}	-7	-	+7	
Zero-scale error	ZSE	f_{ADCLK} = 16MHz		-6	-	+6	
		f_{ADCLK} = 8MHz		-8	-	+8	
		f_{ADCLK} = 1MHz		-10	-	+10	
		f_{ADCLK} = 32.768kHz		-10	-	+10	
Full-scale error	FSE	f_{ADCLK} = 16MHz		-6	-	+6	
		f_{ADCLK} = 8MHz		-8	-	+8	
		f_{ADCLK} = 1MHz		-10	-	+10	
		f_{ADCLK} = 32.768kHz		-10	-	+10	



The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1µF capacitor on the ADC input pin is recommended for noise reduction.

Flash Memory

(V_{SS}= 0V)

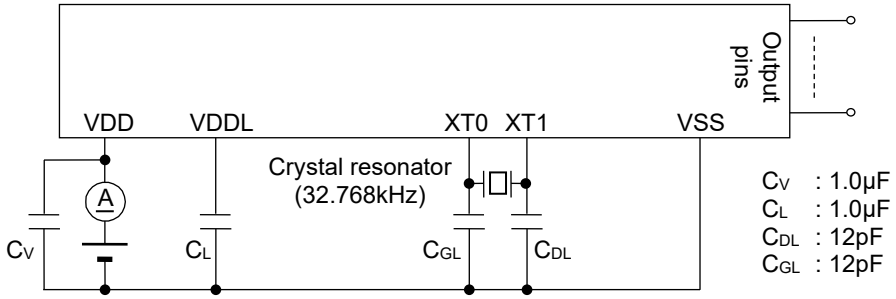
Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+1.8 to +5.5	V
Number of times of Maximum rewriting	CEPD	Data Flash area		10000	times
	CEPP	Program Flash area		100	
Erasion unit	-	Block erasion	Program Flash area	16K	Byte
			Data Flash area	all area	
	-	Sector erasion	Program Flash area	1K	
			Data Flash area	128	
Erasure time (Max.)	-	Block erasion /Sector erasion		50	ms
Writing unit	-	Program Flash area		4	Byte
		Data Flash area		1	
Writing time (Max.)	-	Program Flash area		80	µs
	-	Data Flash area		40	
Data retention period	YDR	rewriting count 100 times		15	years

LCD Driver

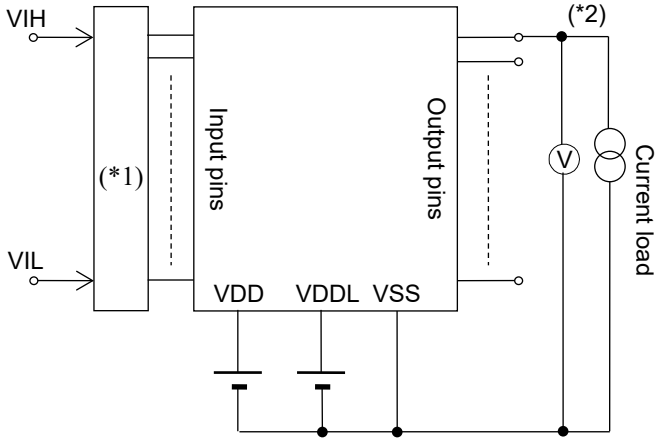
Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
			LCN[*1]	Min.	Typ.	Max.		
V_{L1} Voltage	V_{L1}	Ta = +25°C C_{L1}, C_{L2}, C_{L3} = 1.0µF	00H	Typ. -0.10	0.95	Typ. +0.10		6
			02H		1.00			
			04H		1.05			
			06H		1.10			
			08H		1.15			
			0AH		1.20			
			0CH		1.25			
			0EH		1.30			
			10H		1.35			
			12H		1.40			
			14H		1.45			
			16H		1.50			
			18H		1.55			
			1AH		1.60			
			1CH		1.65			
			1EH		1.70			
V_{L2} Voltage	V_{L2}	Ta = +25°C C_{L1}, C_{L2}, C_{L3} = 1.0µF C_{12} = 1.0µF		V_{L1} x 1.8	V_{L1} x 2	-		
V_{L3} Voltage	V_{L3}			V_{L1} x 2.7	V_{L1} x 3	-		
Bias generation circuit start-up time	t_{BIAS}			-	-	200	ms	

Measuring circuit

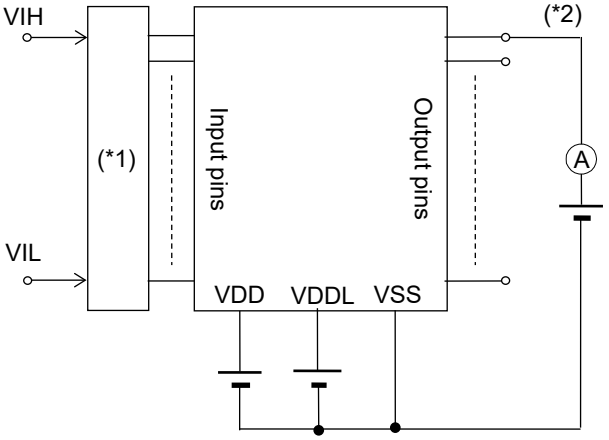
Measuring circuit 1



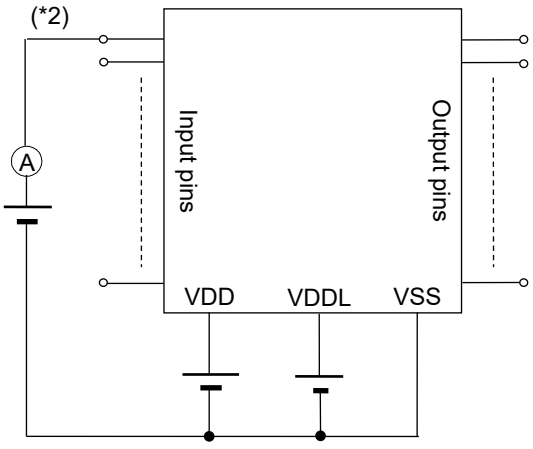
Measuring circuit 2



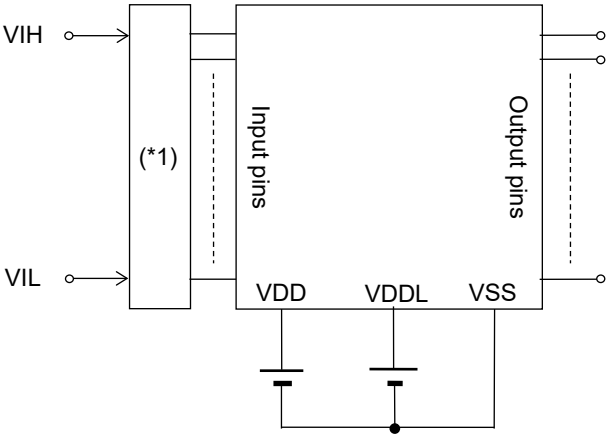
Measuring circuit 3



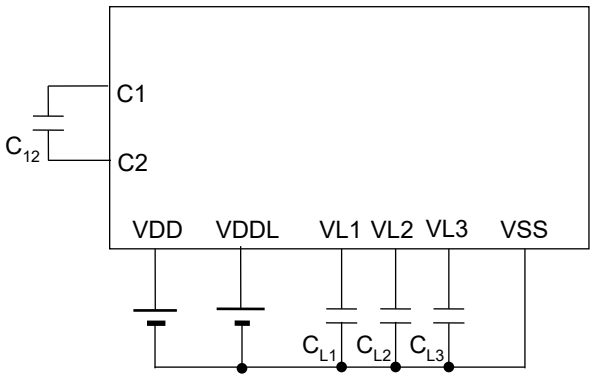
Measuring circuit 4



Measuring circuit 5



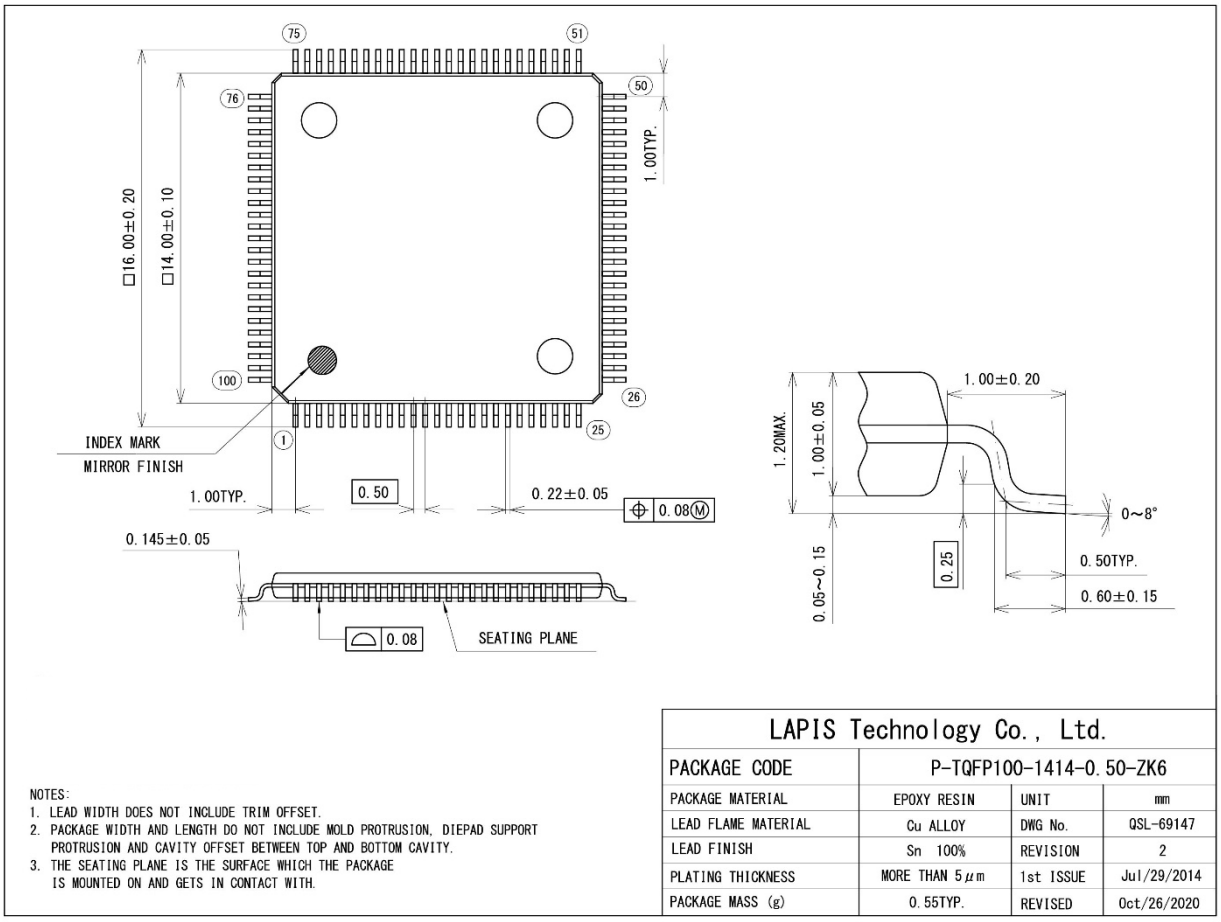
Measuring circuit 6



(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

PACKAGE DIMENSIONS

100pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

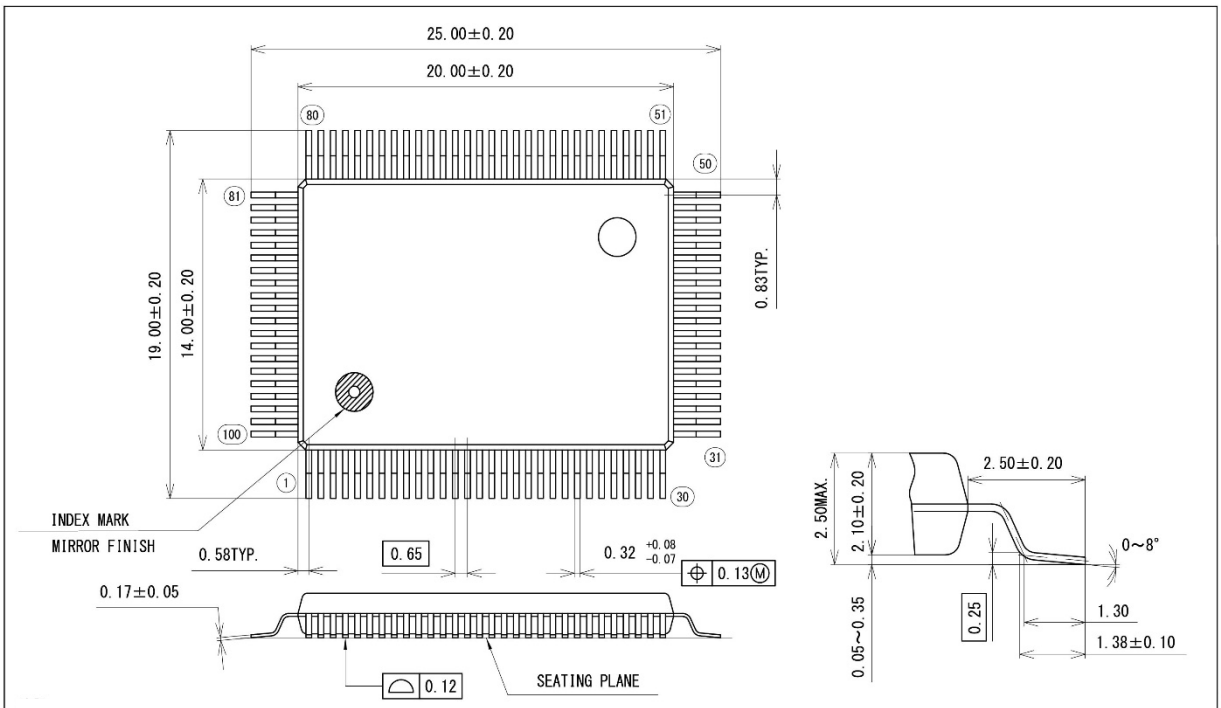
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP100-1414-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69147
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.55TYP.	REVISED	Oct/26/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

100pin QFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

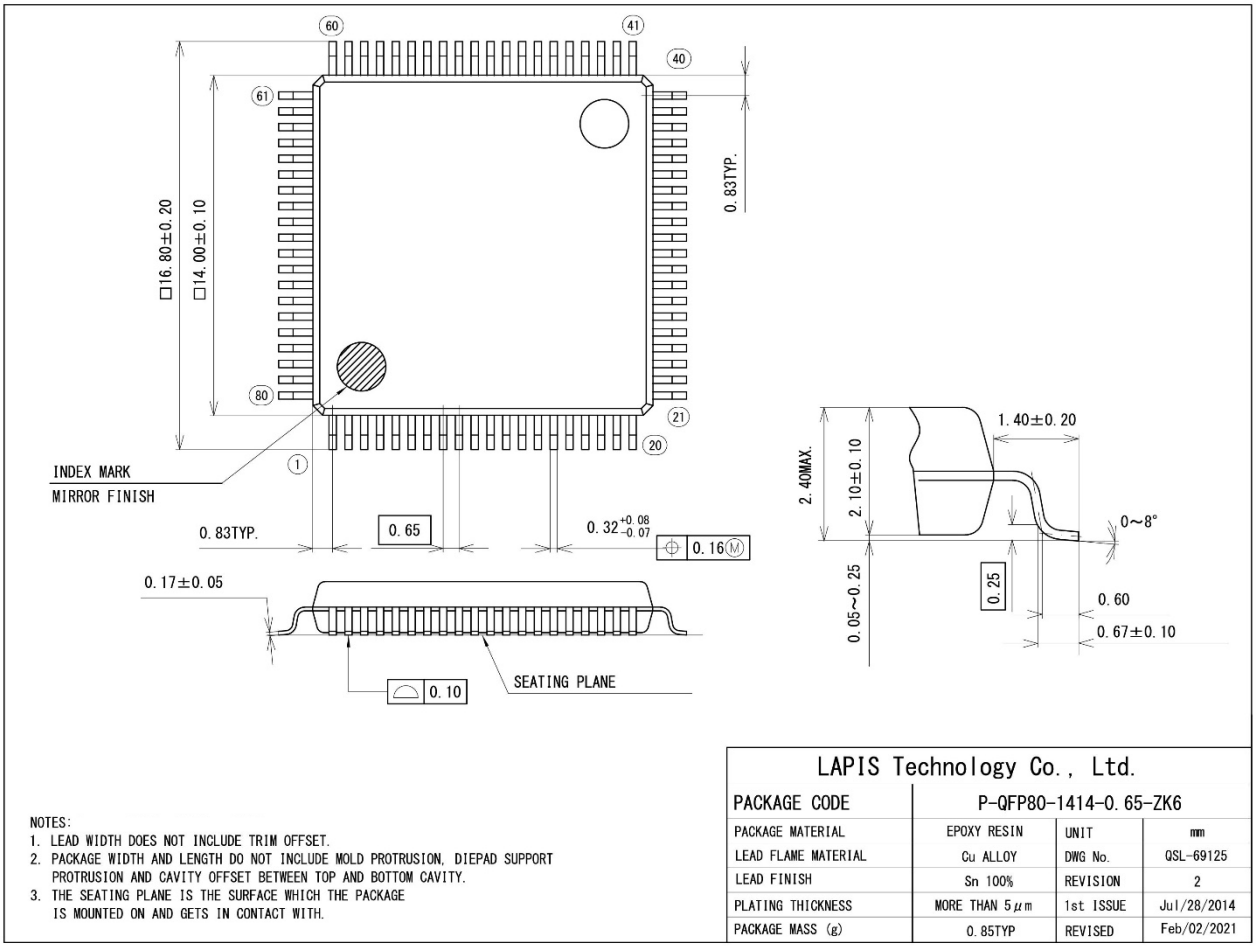
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP100-1420-0.65-BK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	42ALLOY	DWG No.	QSL-68760
LEAD FINISH	Sn 100%	REVISION	3
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	May/10/2012
PACKAGE MASS (g)	1.29TYP.	REVISED	Nov/16/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

80pin QFP Package



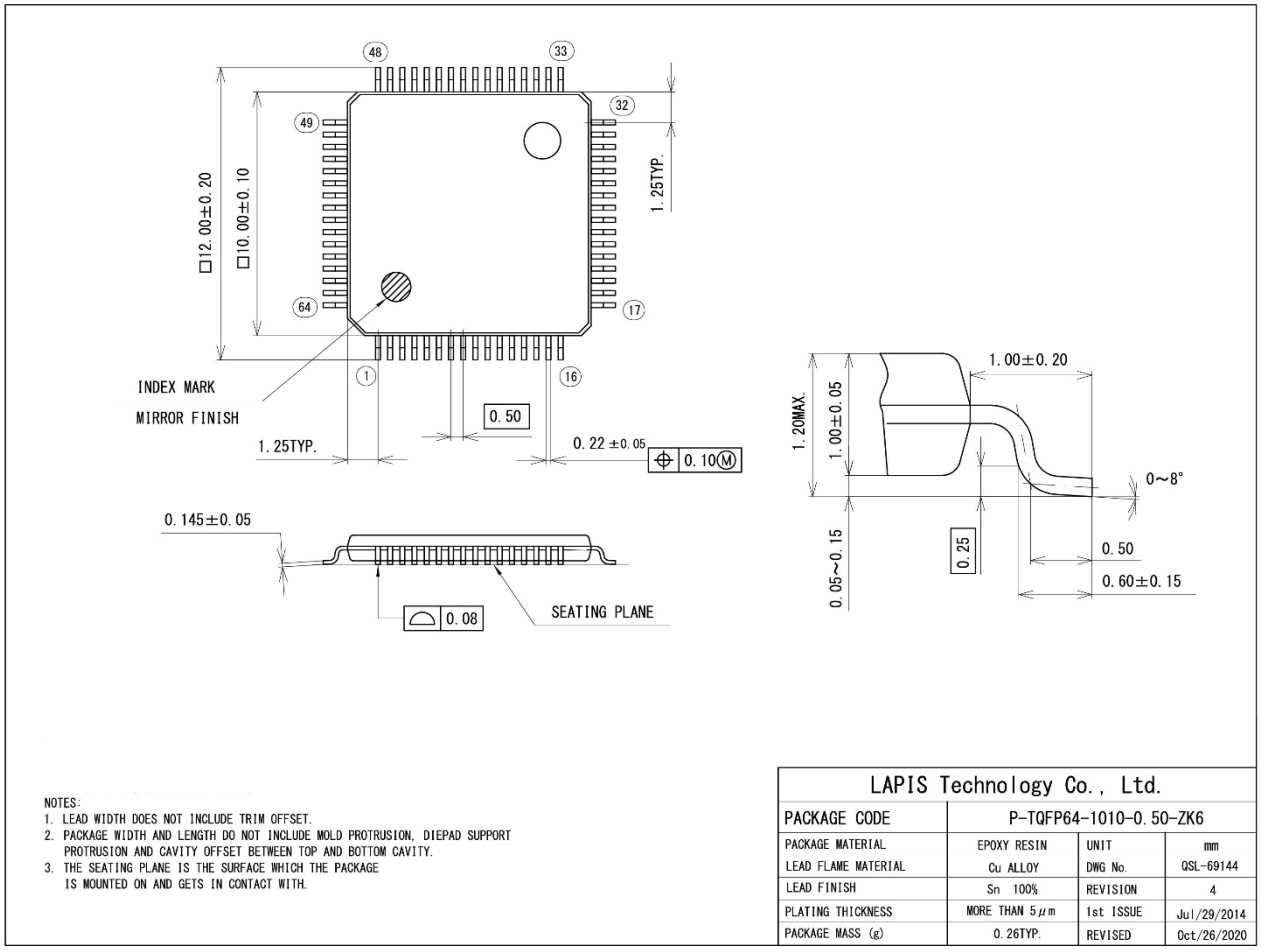
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP80-1414-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69125
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.85TYP	REVISED	Feb/02/2021

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin TQFP Package



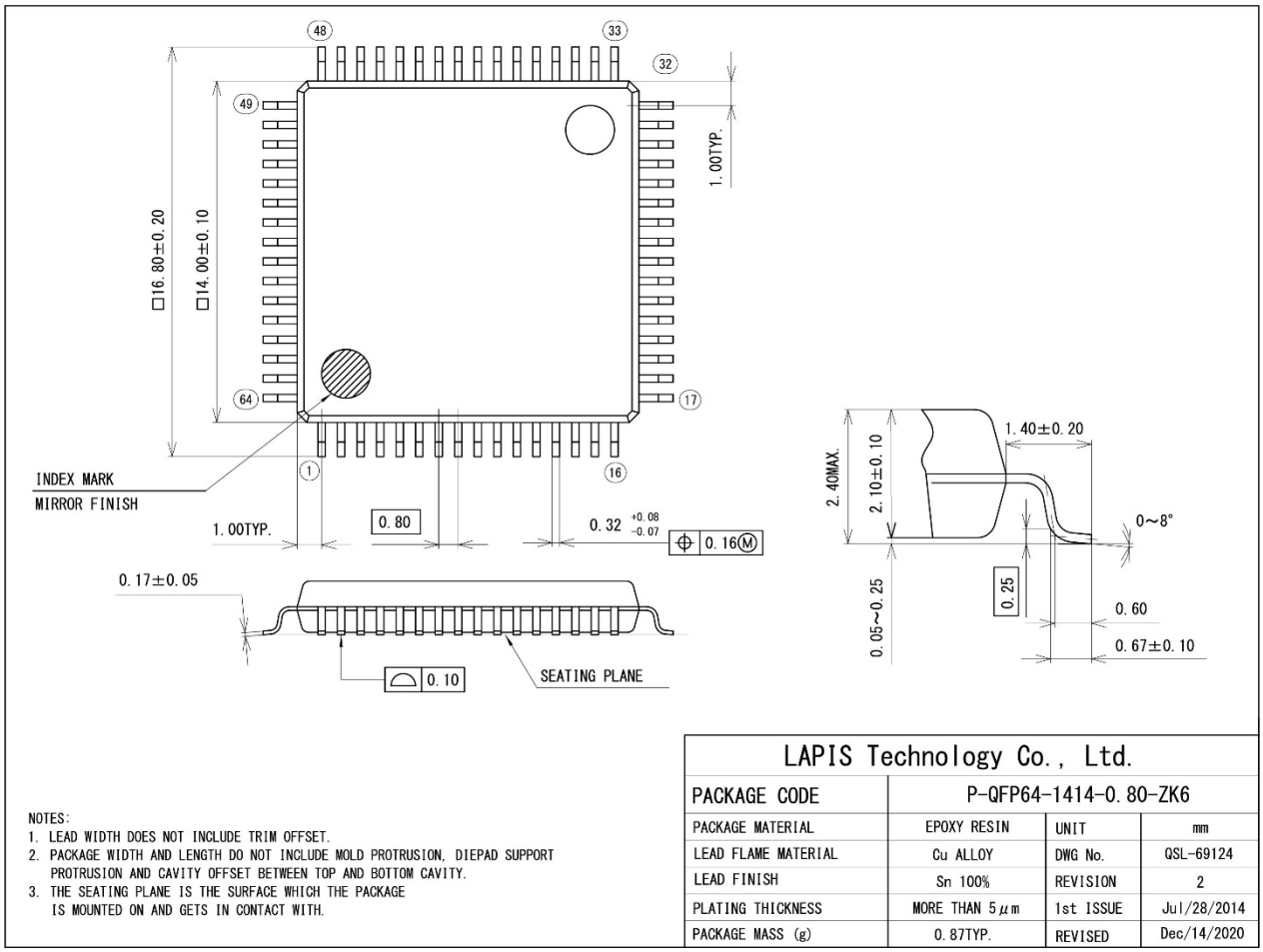
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP64-1010-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69144
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.26TYP.	REVISED	Oct/26/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin QFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

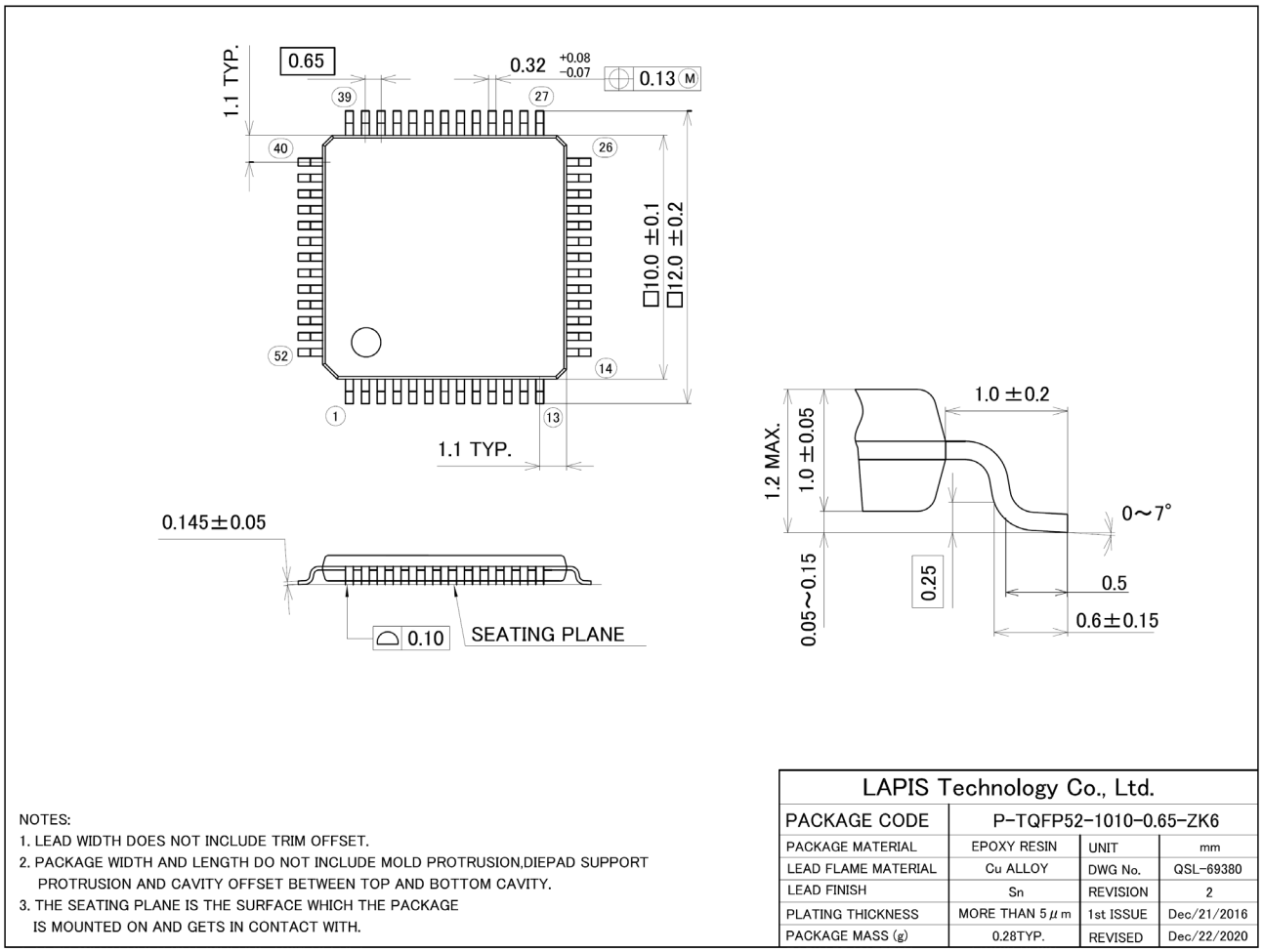
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP64-1414-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69124
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.87TYP.	REVISED	Dec/14/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

52pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION,DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

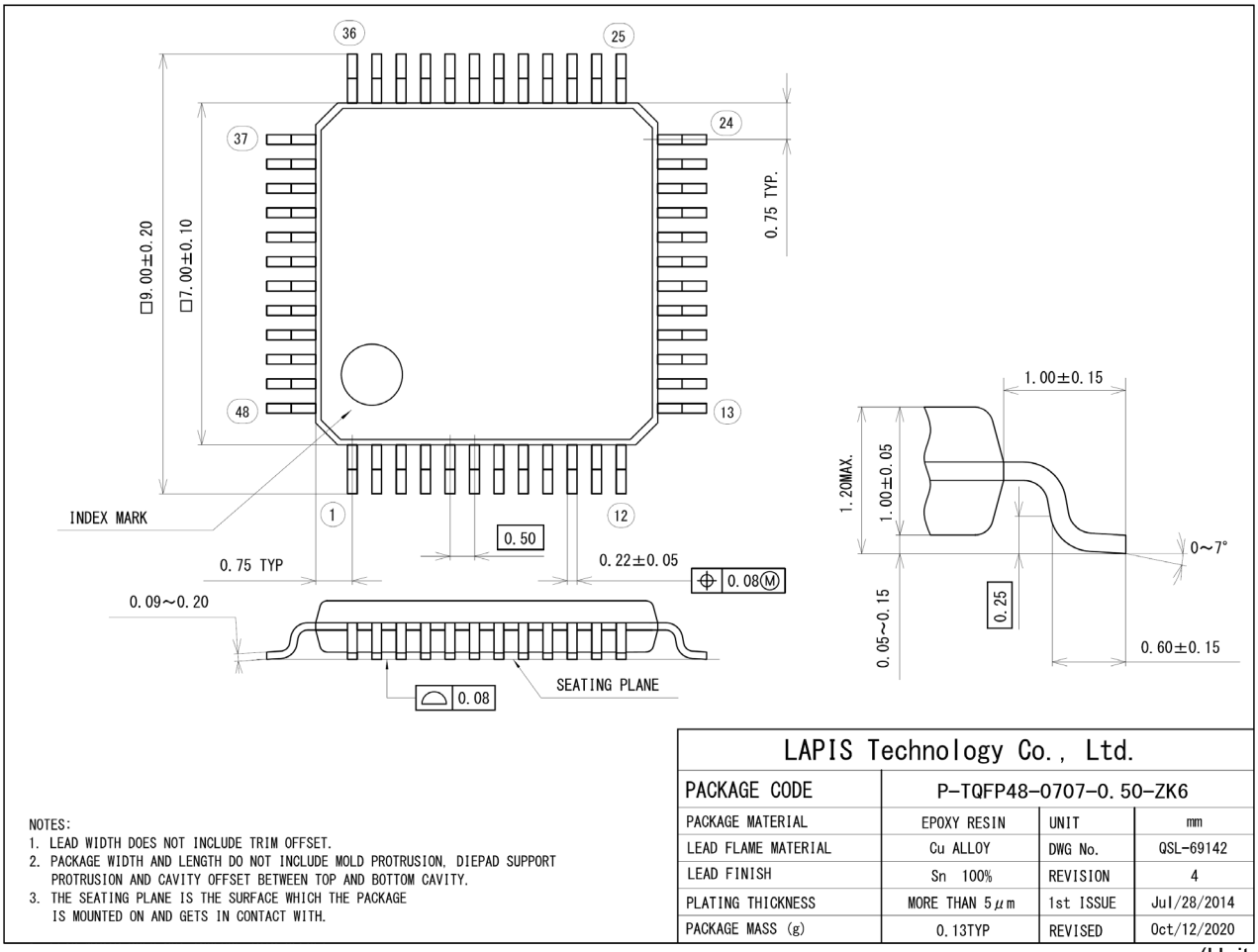
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP52-1010-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69380
LEAD FINISH	Sn	REVISION	2
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Dec/21/2016
PACKAGE MASS (g)	0.28TYP.	REVISED	Dec/22/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

48pin TQFP Package



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

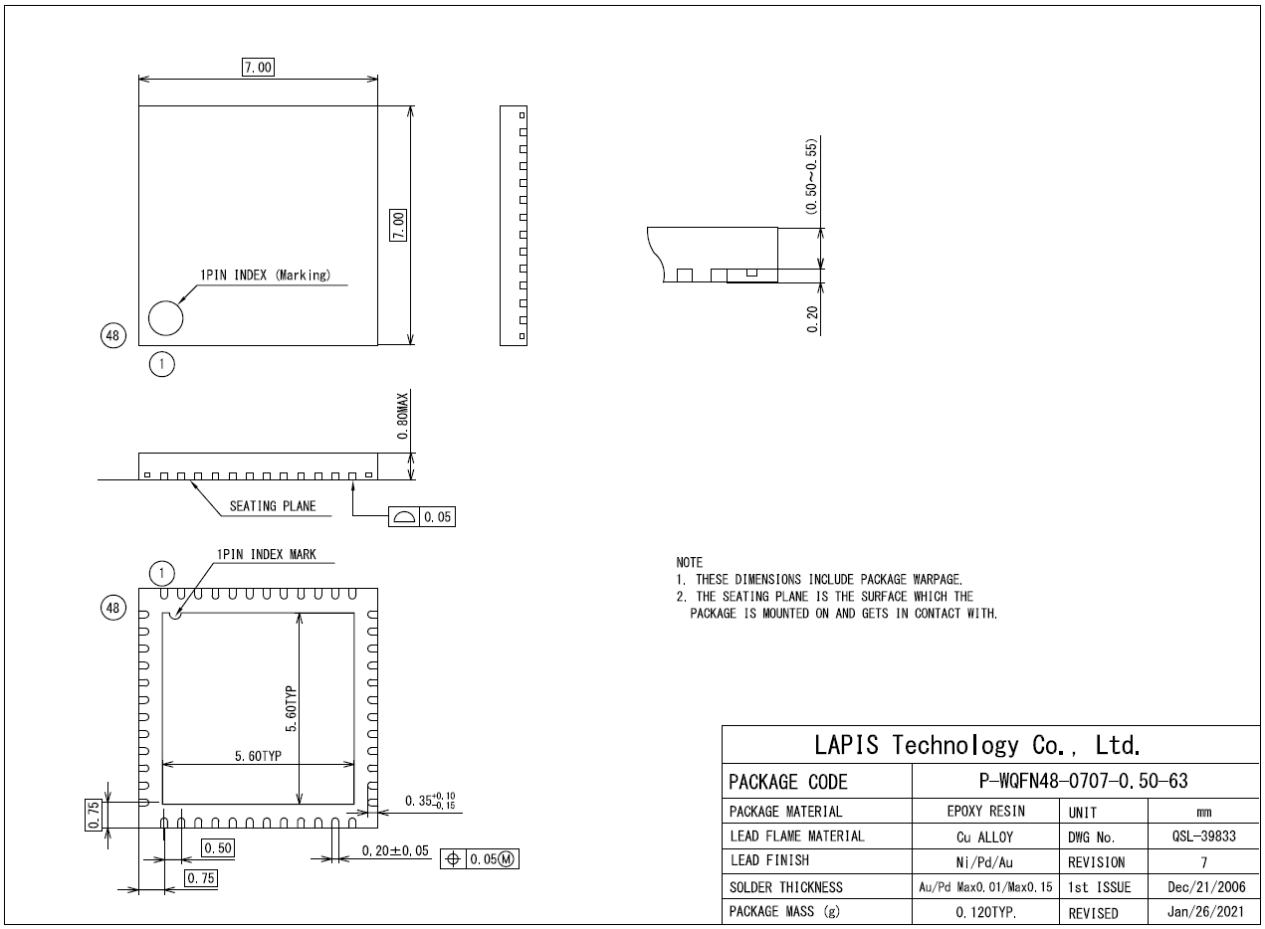
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/12/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

48pin WQFN Package



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN48-0707-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39833
LEAD FINISH	Ni/Pd/Au	REVISION	7
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Dec/21/2006
PACKAGE MASS (g)	0.120TYP.	REVISED	Jan/26/2021

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q2700-01	Feb. 17, 2023	-	-	1st Edition
FEDL62Q2700-02	Jul. 18, 2023	-	-	Made the total revision
FEDL62Q2700-03	Oct. 25. 2023	-	-	Made the total revision
		1	1	Removed under development indication from 6prodcuts in the Table 1
		-	32	Added On-chip Oscillator 2 page
FEDL62Q2700-04	Mar. 26. 2024	1	1	Added application information and the note
		6	6	Corrected WQFN Part Number
		7	7	Updated “How To Read The Part Number”
		57	57	Revised the Notes

Notes for product usage

Notes on this page are applicable to the all LAPIS Technology microcontroller products.
For individual notes on each LAPIS Technology microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS
   Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON
   At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
   On LAPIS Technology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
   Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY
   If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCT
   Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
   When replacing from other product to LAPIS Technology microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS Technology microcontroller products.

5. USE ENVIRONMENT
   When using LAPIS Technology microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

Notes

1) When using LAPIS Technology Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings*1, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
*1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore, LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) LAPIS Technology intends our Products to be used in a way indicated in this document. Please be sure to contact a ROHM sales office if you consider the use of our Products in different way from original use indicated in this document. For use of our Products in medical systems, please be sure to contact a LAPIS Technology representative and must obtain written agreement. Do not use our Products in applications which may directly cause injuries to human life, and which require extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us without our prior written consent.

6) All information contained in this document is subject to change for the purpose of improvement, etc. without any prior notice. Before purchasing or using LAPIS Technology Products, please confirm the latest information with a ROHM sales office. LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document, however, LAPIS Technology shall have no responsibility for any damages, expenses or losses arising from inaccuracy or errors of such information.

7) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

8) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

9) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

10) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) “LAPIS Technology” as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.
2-4-8 Shinyokohama, Kouhoku-ku,Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

LTSZ08023・01・002