FEDL63Q2500-02
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ML63Q2500 Group

ML63Q2557/ML63Q2554
ML63Q2537/ML63Q2534

32-bit MCU built-in Solist-AI™ Accelerator & CAN controller

GENERAL DESCRIPTION

This LSI is a high-performance low power 32-bit microcontroller. Equipped with a 32-bit CPU core Arm®Cortex®-M0+, it implements peripheral circuits, such as the Solist-AI™ accelerator and CAN controller.

- Applications

Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

Note:
This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems. Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product list

The ML63Q2500 group has products as show in the Table1 with multiple package and memory size combinations.

Table 1 Product List

Program memory	Data memory (RAM)	Data Flash	48pin TQFP48 WQFN48*	64pin TQFP64 WQFN64*
256Kbyte	16Kbyte	8Kbyte	ML63Q2537	ML63Q2557
128Kbyte			ML63Q2534	ML63Q2554

* WQFN48 and WQFN64 package product is under development.

Please see the last 3 pages “Notes for product usage” and “Notice” in this document on use with this product.

FEATURES

- CPU
  - 32-bit RISC CPU (CPU name: Arm®Cortex®-M0+)
  - Arm®Thumb®/Thumb®-2 instruction supported
  - Serial Wire Debug Port
  - Minimum instruction execution time
    - 30.5 μs (@32.768 kHz system clock)
    - 20.83ns (@48 MHz system clock)
  - System timer (SysTick)
    - 24 bits × 1 channel, counting by System clock (SYSCLK) (Initial clock: LSCLK) External reference clock is not provided

- Internal memory
  - Re-writing the program memory area by software
  - Background Operation (CPU can work while erasing and rewriting to the Data Flash memory area.)
  - Flash ROM
    - Program area: 128/256KB
    - Data area: 8KB
  - Data RAM
    - Work memory 16KB

- Solist-AI™ Acceralator (AxICORE-ODL)
  - Not only prediction but also learning can be performed on the device. (No need for server/cloud/network connection)
    - Detect anomaly conditions by learning normal conditions for each individual.
  - Capable of high-speed execution of calculations used in AI processing.
    - Addition, subtraction and multiplication of scalars, vectors, and (non-square) matrices are possible.
    - Enables FFT calculation processing useful for vibration sensor data processing.
    - Calculations can be executed without CPU load.
  - Data format: bFloat16 (Built-in integer to bFloat16 conversion function.)
  - Low power consumption/low cost. (Compared to FPGA/GPU etc.), High-speed processing. (Compared to software processing.)
  - One-stop utility using model-based technology.
    Provides software library.
  - Built-in bFloat16-format uniform distribution pseudo-random number generator that can be used as a fixed table.
  - Application example.
    - Motor + acceleration sensor + AI: Early detection of bearing damage.
    - Motor + current sensor + AI: Detection of poor lubrication/contamination of foreign objects.
    - Thermography camera + AI: Accurate detection of abnormal heat generation.
    - FA sensor + AI: Early detection of random failures and abnormal conditions.

- CAN controller
  - 1 channel
  - Equipped with one channel of CAN_FD and 2.0B protocol compliant controller
  - Ability of real time communication control with up to 5Mbps
  - ISO 11898-1:2015 compliant
  - SAE J1939 is supported
  - CAN FD up to 64 data bytes is supported
  - Up to 64 proprietaries receive buffers
  - Up to 32 proprietaries transmit buffers
  - Equipped with CAN error log function
  - Equipped with reception filter
  - Individual signals are transmitted when a high-priority message is received

- Interrupt controller (NVIC)
  - 1 non-maskable interrupt source and 31 maskable interrupt sources
  - Priority level (4-level) can be set for each interrupt

- DMA controller (DMAC)
  - 2 channels
  - Enable to allocate multiple DMA transfer request sources for each channel.
  - Channel priority: fixed mode/round robin mode
  - DMA transfer mode: cycle steal mode/burst mode
  - DMA request type: software requests/hardware requests
  - Maximum transfer count: 65,536
  - Data transfer size: 8 bits/16 bits/32 bits
  - Transfer request source: SSIOF, UARTF, I2CF, SA-ADC

- Time base counter (TBC)
  - Low-speed time base counter × 1 channel with interrupt, × 1 channel for RTC.
  - The clock frequency adjustment in a range approx. -488ppm to +488ppm with 0.119ppm step.

- Real Time Clock (RTC)
  - 99 years calendar, alarm, adjustment of the clock

- 1 kHz Timer (TM1K)
  - 80Hz/60Hz/40Hz/20Hz/10Hz/1Hz interrupt function

- Timers (TMR)
  - 16-bit × 6 channels
  - 32-bit configuration available by using 2 channels
  - Selection of one-shot timer mode is possible
  - External clock can be selected as timer clock.

- Function Timers (FTM)
  - 16-bit × 2 channels
  - Equipped with the timer/capture/PWM functions using a 16-bit counter

  - An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3φ)
  - 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input selectable as timer clock
  - Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Watchdog timer (WDT)
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Three-phase motor control PWM (NTMS)
  - 16-bit × 3 channels, 2 outputs each; total 6 outputs
  - Center-aligned waveform output with up-down counter
  - Generatable a trigger of the SA-ADC conversion starting
  - Emergency stop with analog-comparator or pin input

- Synchronous serial port (SSIOF)
  - 2 channels
  - 4-stage FIFO for each transmission and reception
  - Master/slave selectable
  - LSB first/MSB first selectable
  - Clock polarity and phase selectable
  - Supports slave-select signal

- UART (UARTF)
  - 4 channels
  - 4-stage FIFO for each transmission and reception
  - Full duplex buffer system
  - Communication speed: up to 115200bps.
  - Programmable interface (data length, parity, stop bits selectable)

- I^2C bus interface (I2CF)
  - 1 channel
  - 4-stage FIFO for each transmission and reception
  - Master/slave function
  - Fast mode (400 kHz), standard mode (100 kHz)

- General-purpose ports (GPIO)
  - Input/output port × up to 49 channels (including secondary or tertiary or quaternary).
  - Port interrupt: 8 sources selectable from all GPIOs

- Successive approximation type A/D converter (SA-ADC)
  - 2 units
  - Input × 12 channels
  - 12-bit resolution
  - Conversion time minimum 1μs/ channel @conversion clock is 24MHz
  - Simultaneous conversion of 2 inputs with 2 units is possible
  - Sampling time can be chosen
  - Consecutive scan conversion function for target input channels
  - Consecutive scan conversion with a specific interval time
  - One conversion result register for each channel
  - Upper /Lower limit is configurable for the conversion result, generates an interrupt
  - A/D converter self test function (full scale, zero scale, internal reference voltage)
  - Following triggers is available to start the A/D conversion
    16-bit timer interrupt requests, functional timer trigger and three-phase motor control PWM ADC conversion staring trigger.

- Analog comparator (CMP)
  - 3 units
  - Common-mode input voltage range: 0.1 to V_{DD}-1.2V
  - Propagation delay: Typ. 0.5μs

- Voltage Level Supervisor (VLS)
  - Monitoring V_{DD} level.
  - Threshold voltage: selectable from 10 level

- Functional Voltage level detection reset or interrupt is generatable

- Reset
  - RESET_N pin reset
  - Power-on reset
  - Watchdog timer (WDT) overflow reset
  - Voltage Level Supervisor (VLS) reset
  - Crystal oscillation stop detection reset
  - SYSRESETREQ of Arm® Cortex®-M0+ (software reset)

- Clock
  - Low-speed clock:
    - Crystal oscillation (32.768kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - PLL (48MHz) generated from Low-speed clock
    - Crystal oscillation (40/20MHz) for system or CAN

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.
  -
- Guaranteed operating range
  - Operating temperature: (ambient) -40°C to +105°C, (junction) -40°C to +115°C
  - Operating voltage: V_{DD}=2.3 to 5.5V

- Supply current (Typ.)
  - High-speed operation (48MHz): 10mA
  - Low-speed operation (32.768kHz): 27μA
  - HALT mode: 3.5μA
  - STOP mode: 2μA

- Shipping package

Table 2 Product name list

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Packing form and Product name	
			Tray	Tape & Reel
48 pin plastic WQFN	7.0 × 7.0 (-)	0.5	ML63Q2534-NNNGDZW5AY ML63Q2537-NNNGDZW5AY	ML63Q2534-NNNGDZW5BY ML63Q2537-NNNGDZW5BY
48 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.5	ML63Q2534-NNNTBZWAY ML63Q2537-NNNTBZWAY	ML63Q2534-NNNTBZWBY ML63Q2537-NNNTBZWBY
64 pin plastic WQFN	9.0 × 9.0 (-)	0.5	ML63Q2554-NNNGDZW5AY ML63Q2557-NNNGDZW5AY	ML63Q2554-NNNGDZW5BY ML63Q2557-NNNGDZW5BY
64 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.5	ML63Q2554-NNNTBZWAY ML63Q2557-NNNTBZWAY	ML63Q2554-NNNTBZWBY ML63Q2557-NNNTBZWBY

FUNCTION LIST

Table 3 Product Specification

Category		ML63Q2534	ML63Q2537	ML63Q2554	ML63Q2557
CPU		Arm®Cortex®-M0+			
Memory	Program FLASH	128KB	256KB	128KB	256KB
	Data RAM	16KB			
	Data FLASH	8KB			
Pins	Total	48	48	64	64
	Power	4			
	Reset	1			
	GPIO	34		49	
interrupt	Non maskable	1			
	Maskable (External pin input)	31 (8)			
Timer	TMR	6 ch			
	FTM	2 ch			
	NTMS	1 ch			
	TBC	2 ch			
	RTC	1 ch			
	TM1K	1 ch			
	WDT	1 ch			
Communication	SSIOF	2 ch			
	UARTF	4 ch			
	I2CF	1 ch			
	CAN	1 ch			
Analog	VLS	1 unit			
	SA-ADC	2 unit 12 input			
	CMP	3 unit			
Other	DMAC	2 ch			
	Solist-AI™ Accelerator	1 ch			
Clock	Low speed	32.768kHz (built-in RC oscillation, crystal oscillation)			
	High speed	PLL (Up to 48MHz), crystal oscillation (20 or 40MHz)			
Reset	cause	Pin / POR / WDT / VLS / crystal oscillation stop detection / software			
Operating Condition	Temperature	Ta: -40°C to +105°C (Tj < +115°C)			
	Voltage	V_{DD}=2.3 to 5.5V			
Package		WQFN48, TQFP48		WQFN64, TQFP64	

How To Read The Part Number

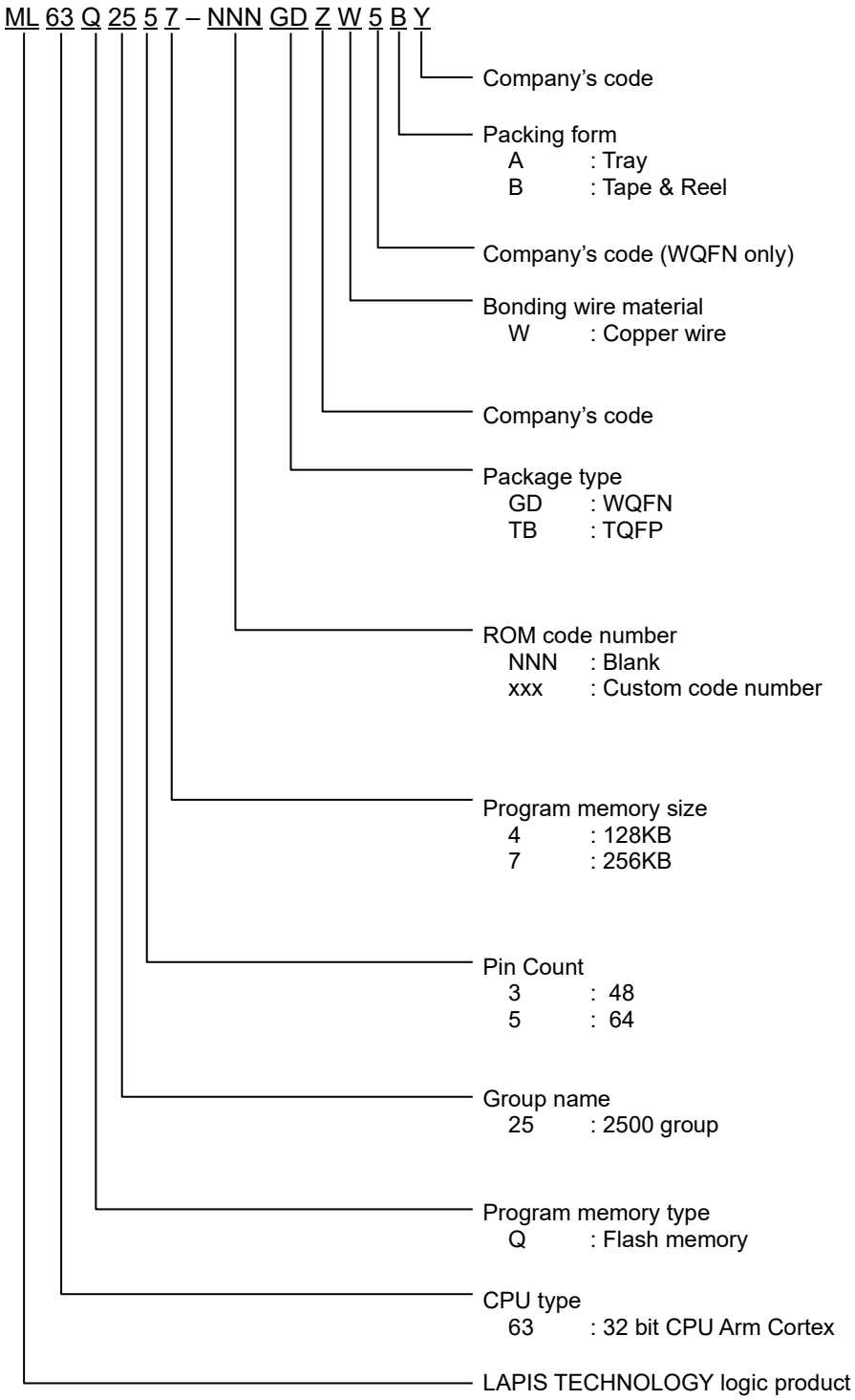


Figure 1 Part Number

BLOCK DIAGRAM

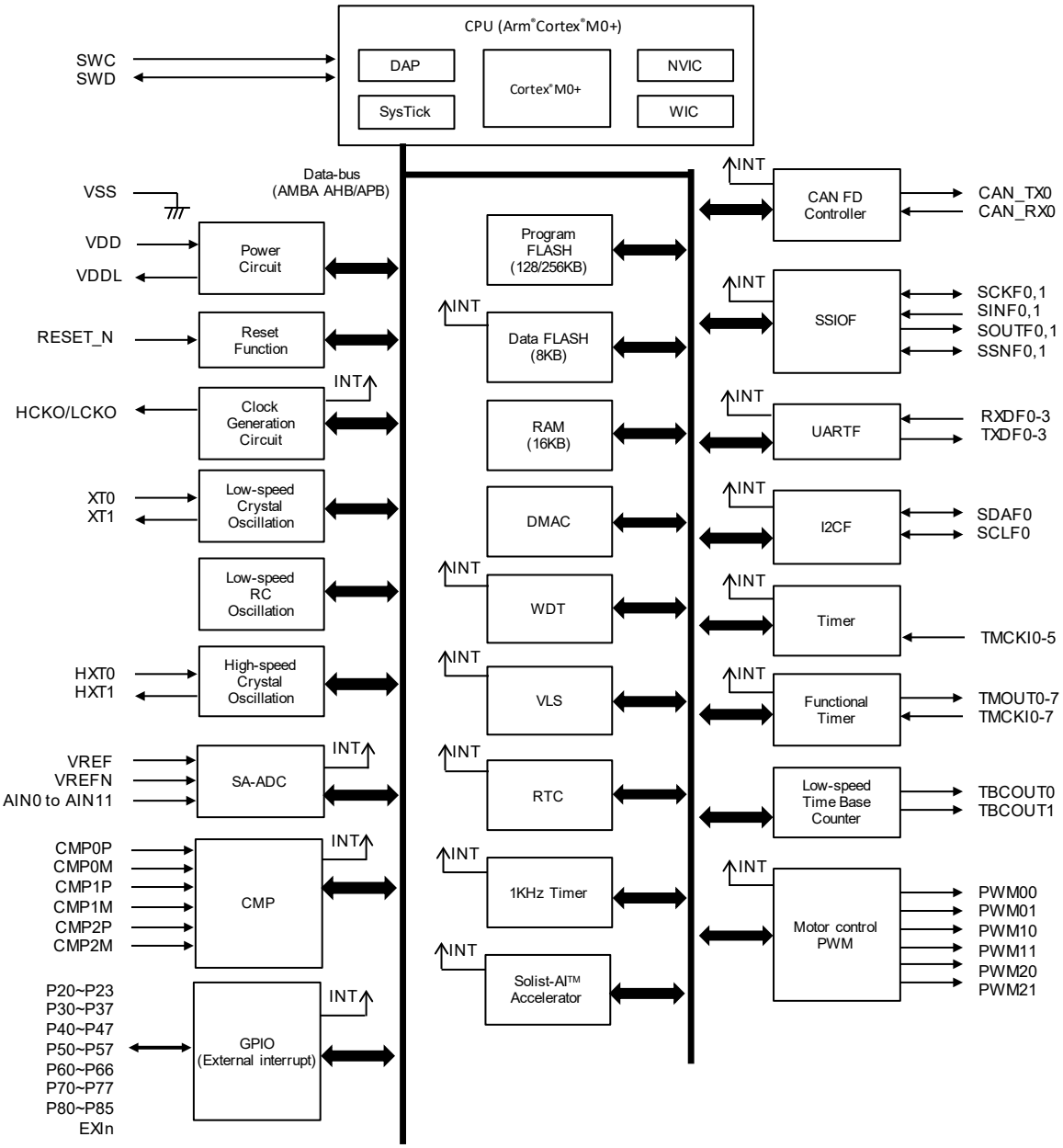


Figure 2 BLOCK DIAGRAM

PIN CONFIGURATION

48pin WQFN Package

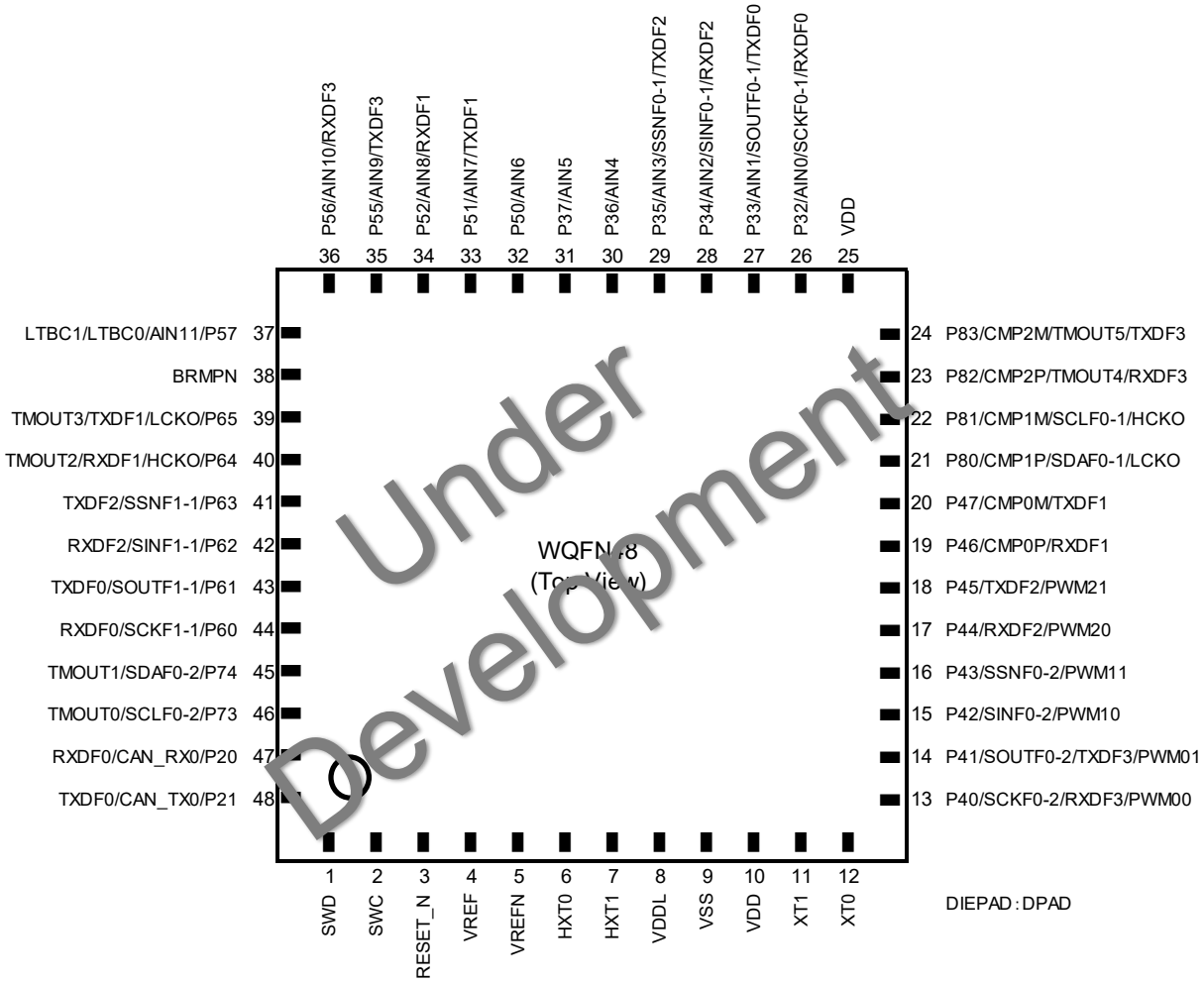


Figure 3 48pin WQFN Package

48pin TQFP Package

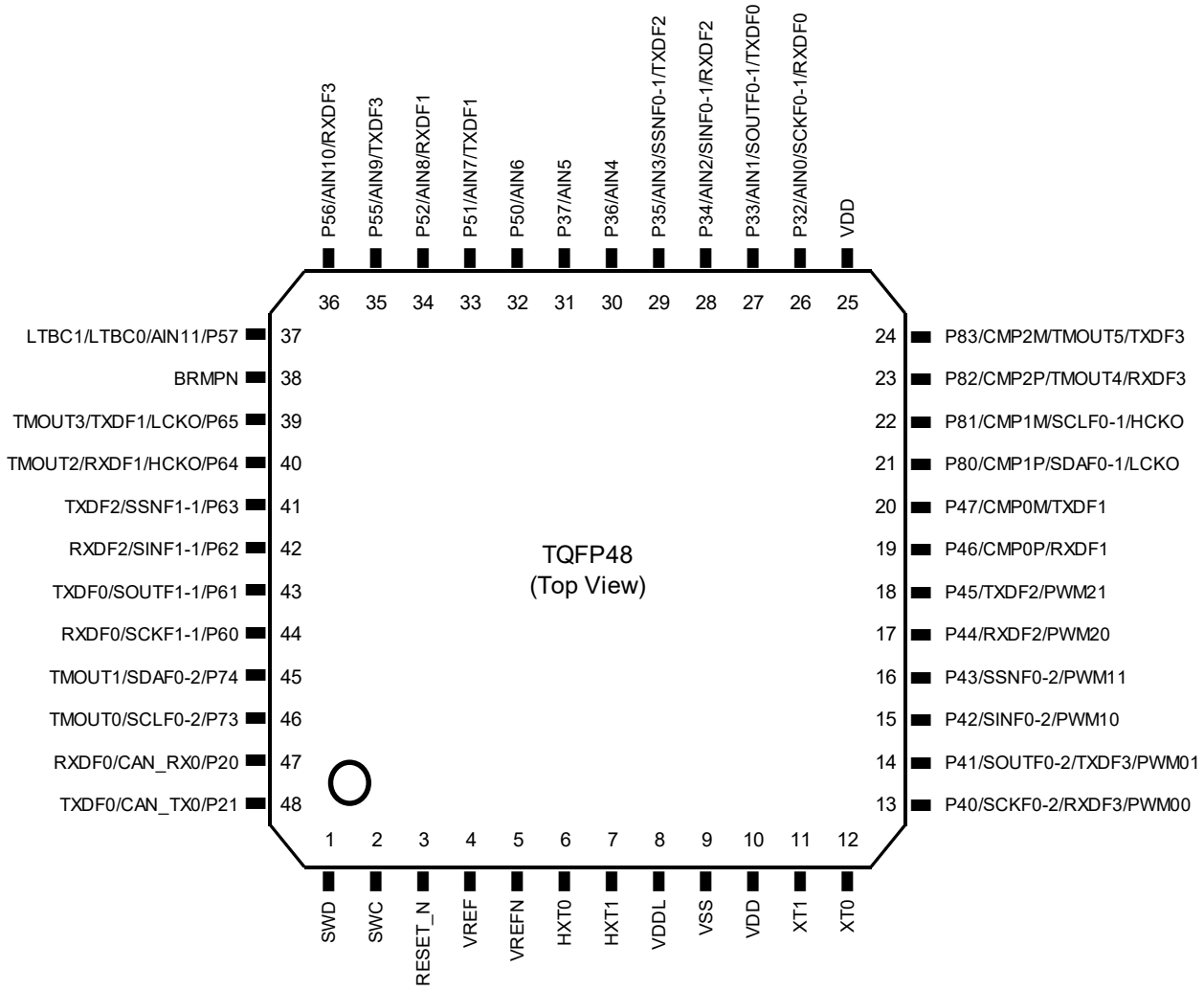


Figure 4 48pin TQFP Package

64pin WQFN Package

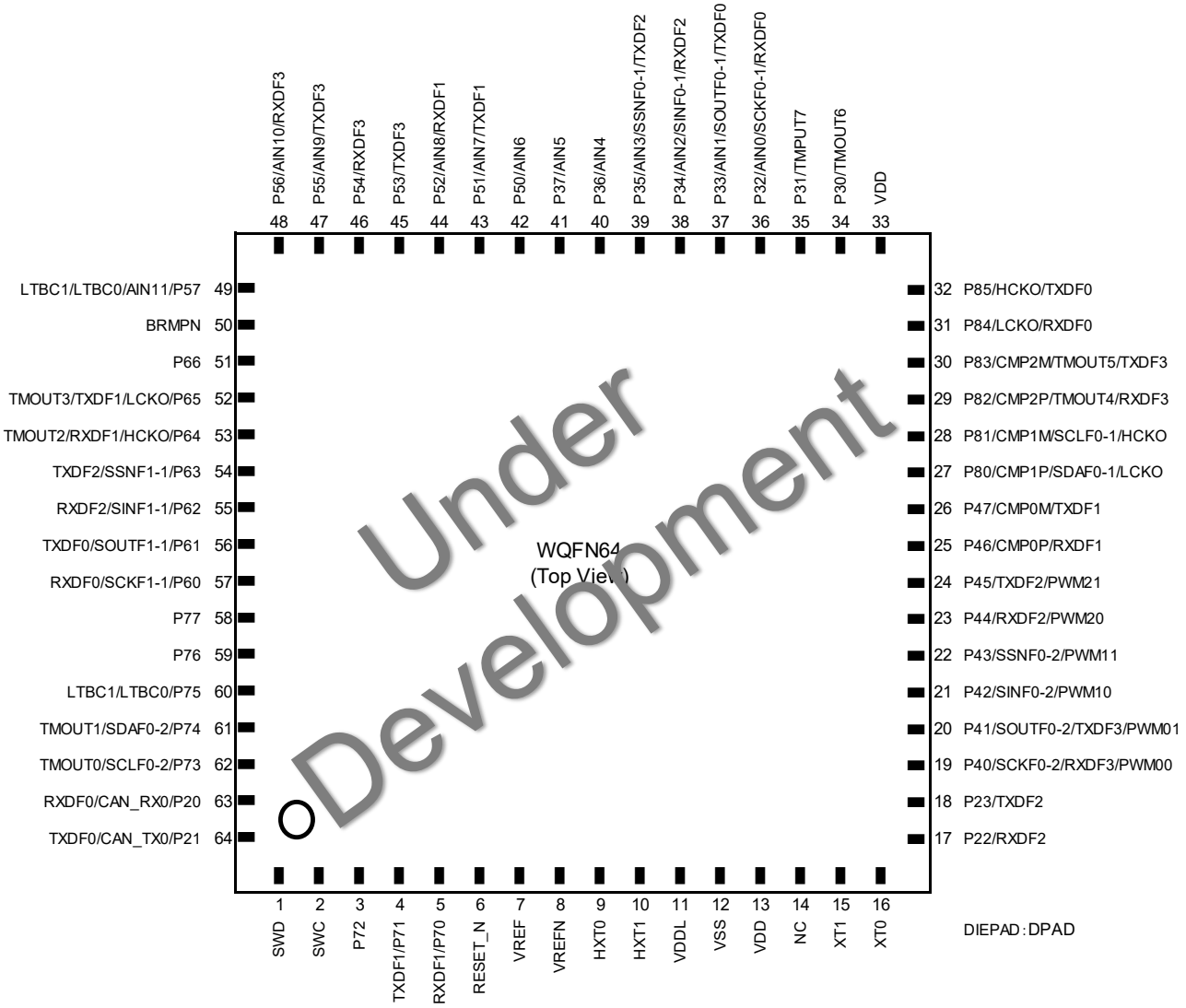


Figure 5 64pin WQFN Package

64pin TQFP Package

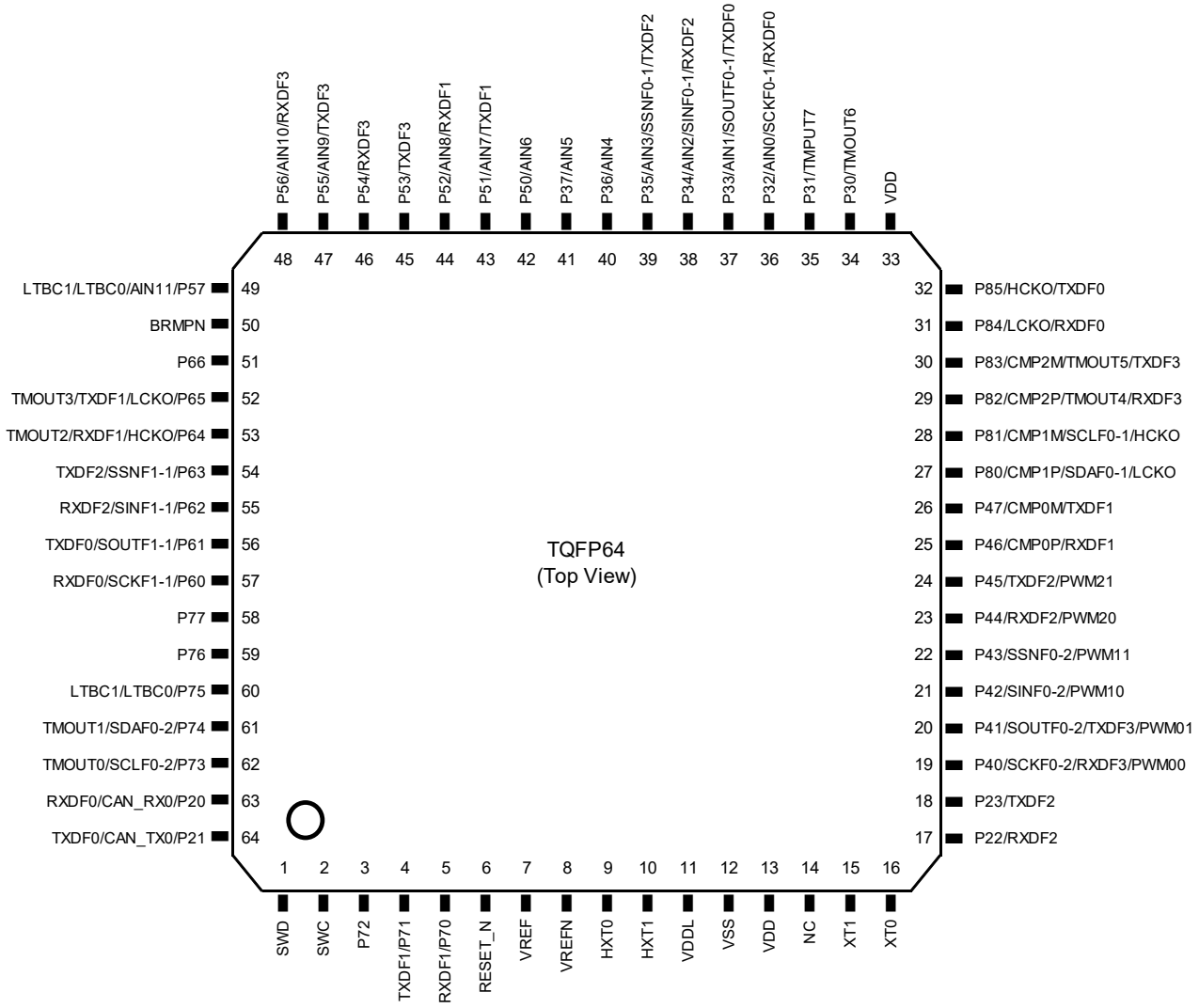


Figure 6 64pin TQFP Package

PIN LIST

Table 4 Pin List

PIN No.		LSI Pin name	Reset state	Primary Function		Secondary Function		Tertiary Function		Quaternary Function	
ML63Q253x	ML63Q255x			Functional pin name	I/O	Functional pin name	I/O	Functional pin name	I/O	Functional pin name	I/O
1	1	SWD	Pull-up input	SWD	I/O	–	–	–	–	–	–
2	2	SWC	Pull-up input	SWC	I	–	–	–	–	–	–
–	3	P72	Hi-Z output	P72	I/O	–	–	–	–	–	–
–	4	P71	Hi-Z output	P71	I/O	–	–	TXDF1	O	–	–
–	5	P70	Hi-Z output	P70	I/O	–	–	RXDF1	I	–	–
3	6	RESET_N	Hi-Z input	RESET_N	I	–	–	–	–	–	–
4	7	VREF	Hi-Z	VREF	I	–	–	–	–	–	–
5	8	VREFN	Hi-Z	VREFN	I	–	–	–	–	–	–
6	9	HXT0	High output	HXT0	I	–	–	–	–	–	–
7	10	HXT1	Hi-Z	HXT1	O	–	–	–	–	–	–
8	11	VDDL	–	VDDL	–	–	–	–	–	–	–
9	12	VSS	–	VSS	–	–	–	–	–	–	–
10	13	VDD	–	VDD	–	–	–	–	–	–	–
–	14	NC	–	NC	–	–	–	–	–	–	–
11	15	XT1	Hi-Z	XT1	I/O	–	–	–	–	–	–
12	16	XT0	Hi-Z	XT0	I	–	–	–	–	–	–
–	17	P22	Hi-Z output	P22	I/O	–	–	RXDF2	I	–	–
–	18	P23	Hi-Z output	P23	I/O	–	–	TXDF2	O	–	–
13	19	P40	Hi-Z output	P40	I/O	SCKF0-2	I/O	RXDF3	I	PWM00	O
14	20	P41	Hi-Z output	P41	I/O	SOUTF0-2	O	TXDF3	O	PWM01	O
15	21	P42	Hi-Z output	P42	I/O	SINF0-2	I	–	–	PWM10	O
16	22	P43	Hi-Z output	P43	I/O	SSNF0-2	I/O	–	–	PWM11	O
17	23	P44	Hi-Z output	P44	I/O	–	–	RXDF2	I	PWM20	O
18	24	P45	Hi-Z output	P45	I/O	–	–	TXDF2	O	PWM21	O
19	25	P46	Hi-Z output	P46/CMP0P	I/O	–	–	RXDF1	I	–	–
20	26	P47	Hi-Z output	P47/CMP0M	I/O	–	–	TXDF1	O	–	–
21	27	P80	Hi-Z output	P80/CMP1P	I/O	LCKO	O	SDAF0-1	I/O	–	–
22	28	P81	Hi-Z output	P81/CMP1M	I/O	HCKO	O	SCLF0-1	I/O	–	–
23	29	P82	Hi-Z output	P82/CMP2P	I/O	–	–	RXDF3	I	TMOUT4	O
24	30	P83	Hi-Z output	P83/CMP2M	I/O	–	–	TXDF3	O	TMOUT5	O
–	31	P84	Hi-Z output	P84	I/O	LCKO	O	RXDF0	I	–	–
–	32	P85	Hi-Z output	P85	I/O	HCKO	O	TXDF0	O	–	–
25	33	VDD	–	VDD	–	–	–	–	–	–	–
–	34	P30	Hi-Z output	P30	I/O	–	–	–	–	TMOUT6	O
–	35	P31	Hi-Z output	P31	I/O	–	–	–	–	TMOUT7	O
26	36	P32	Hi-Z output	P32/AIN0	I/O	SCKF0-1	I/O	RXDF0	I	–	–
27	37	P33	Hi-Z output	P33/AIN1	I/O	SOUTF0-1	O	TXDF0	O	–	–
28	38	P34	Hi-Z output	P34/AIN2	I/O	SINF0-1	I	RXDF2	I	–	–
29	39	P35	Hi-Z output	P35/AIN3	I/O	SSNF0-1	I/O	TXDF2	O	–	–
30	40	P36	Hi-Z output	P36/AIN4	I/O	–	–	–	–	–	–
31	41	P37	Hi-Z output	P37/AIN5	I/O	–	–	–	–	–	–
32	42	P50	Hi-Z output	P50/AIN6	I/O	–	–	–	–	–	–
33	43	P51	Hi-Z output	P51/AIN7	I/O	–	–	TXDF1	O	–	–
34	44	P52	Hi-Z output	P52/AIN8	I/O	–	–	RXDF1	I	–	–

PIN No.		LSI Pin name	Reset state	Primary Function		Secondary Function		Tertiary Function		Quaternary Function	
ML63Q253x	ML63Q255x			Functional pin name	I/O	Functional pin name	I/O	Functional pin name	I/O	Functional pin name	I/O
-	45	P53	Hi-Z output	P53	I/O	–	–	TXDF3	O	–	–
-	46	P54	Hi-Z output	P54	I/O	–	–	RXDF3	I	–	–
35	47	P55	Hi-Z output	P55/AIN9	I/O	–	–	TXDF3	O	–	–
36	48	P56	Hi-Z output	P56/AIN10	I/O	–	–	RXDF3	I	–	–
37	49	P57	Hi-Z output	P57/AIN11	I/O	LTBC0	O	LTBC1	O	–	–
38	50	BRMPN	Pull-up input	BRMPN	I	–	–	–	–	–	–
-	51	P66	Hi-Z output	P66	I/O	–	–	–	–	–	–
39	52	P65	Hi-Z output	P65	I/O	LCKO	O	TXDF1	O	TMOUT3	O
40	53	P64	Hi-Z output	P64	I/O	HCKO	O	RXDF1	I	TMOUT2	O
41	54	P63	Hi-Z output	P63	I/O	SSNF1-1	I/O	TXDF2	O	–	–
42	55	P62	Hi-Z output	P62	I/O	SINF1-1	I	RXDF2	I	–	–
43	56	P61	Hi-Z output	P61	I/O	SOUTF1-1	O	TXDF0	O	–	–
44	57	P60	Hi-Z output	P60	I/O	SCKF1-1	I/O	RXDF0	I	–	–
-	58	P77	Hi-Z output	P77	I/O	–	–	–	–	–	–
-	59	P76	Hi-Z output	P76	I/O	–	–	–	–	–	–
–	60	P75	Hi-Z output	P75	I/O	LTBC0	O	LTBC1	O	–	–
45	61	P74	Hi-Z output	P74	I/O	–	–	SDAF0-2	I/O	TMOUT1	O
46	62	P73	Hi-Z output	P73	I/O	–	–	SCLF0-2	I/O	TMOUT0	O
47	63	P20	Hi-Z output	P20	I/O	CAN_RX0	I	RXDF0	I	–	–
48	64	P21	Hi-Z output	P21	I/O	CAN_TX0	O	TXDF0	O	–	–
DIEPAD		DPAD	–	DPAD	–	–	–	–	–	–	–

Pxx can be used as GPIO, EXI and TMCKI.
The I^2C and SSIO interface use pins with a combination of the same suffix number after hyphen.

PIN DESCRIPTION

The table below shows the pin descriptions for each function.
"I/O" Field in the below table define the pin type ("-" : power supply pin, "I" : Input pin, "O" : Out put pin, "I/O" bi-directional pin)

Table 5 Pin Description

Function	Functional pin name	LSI pin name	I/O	Description
Power	—	VSS	—	Negative power supply pin (-) Define this terminal potential as V_{SS}
	—	VDD	—	Positive power supply pin (+). Connect a capacitor C_V (more than 1μF) between this pin and VSS. Define this terminal potential as V_{DD}.
	—	VDDL	—	Power supply for internal logic (internal regulator's output). Connect a capacitor C_L (1μF) between this pin and VSS.
System	SWC	SWC	I	Debugger clock input
	SWD	SWD	I/O	Debugger data input/output
	BRMPN	BRMPN	I	Remapping control input (for firmware update) Based on the BRMPN pin setting at the time of the reset release, Bank0 is remapped.
	RESET_N	RESET_N	I	Reset input. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is NOT internally connected.
General-purpose input/output port (GPIO)	P20～P23	P20～P23	I/O	General purpose input/output - High-impedance (initial value) - Input with Pull-up - Input without Pull-up - CMOS output - N channel (N-ch) open drain output
	P30～P37	P30～P37		
	P40～P47	P40～P47		
	P50～P57	P50～P57		
	P60～P66	P60～P66		
	P70～P77	P70～P77		
	P80～P85	P80～P85		
Clock input	XT0	XT0	I	32.768kHz crystal connection pin for low-speed clock. The oscillation unit is connected across XT0 and XT1. Capacitors C_{DL} and C_{GL} are connected across this pin and VSS as required. The XT1 is also used as an external clock input.
	XT1	XT1	I/O	
	HXT0	HXT0	I	20MHz or 40MHz crystal connection pin to use for CAN interface or high-speed clock. The oscillation unit is connected across HXT0 and HXT1. Capacitors C_{DL2} and C_{GL2} are connected across this pin and VSS as required. An external clock input is not supported.
	HXT1	HXT1	O	
Clock output	HCKO	P81 P64 P85	O	High-speed clock output
	LCKO	P80 P65 P84	O	Low-speed clock output
	LTBC0 /LTBC1	P57 P75	O	LTBC 1Hz/2Hz output
External interrupt	EXI0~EXI7	P20～P85	I	External maskable interrupt input. Select and assign from all GPIOs. There are also used for trigger of functional timers.
External timer clock	TMCKI0~TMCKI7	P20～P85	I	External timer clock input Select and assign from all GPIOs. There are used for clock of 16 bit timers and functional timers.
Functional timer	TMOUT0	P73	O	Functional timer output
	TMPUT1	P74	O	
	TMOUT2	P64	O	
	TMOUT3	P65	O	
	TMOUT4	P82	O	
	TMOUT5	P83	O	
	TMOUT6	P30	O	
	TMOUT7	P31	O	

Function	Functional pin name	LSI pin name	I/O	Description
Three phase motor control PWM	PWM00	P40	O	PWM output
	PWM01	P41	O	
	PWM10	P42	O	
	PWM11	P43	O	
	PWM20	P44	O	
	PWM21	P45	O	
I^2C	SCLF0	P73 P81	I/O	I2CF0 clock input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.
	SDAF0	P74 P80	I/O	I2CF0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.
CAN	CAN_RX0	P20	I	Serial data input of CAN bus 0
	CAN_TX0	P21	O	Serial data output pin of CAN bus 0
UART	RXDF0	P20 P84 P32 P60	I	UARTF0 reception data input
	TXDF0	P21 P85 P33 P61	O	UARTF0 transmission data output
	RXDF1	P70 P46 P52 P64	I	UARTF1 reception data input
	TXDF1	P71 P47 P51 P65	O	UARTF1 transmission data output
	RXDF2	P22 P34 P44 P62	I	UARTF2 reception data input
	TXDF2	P23 P35 P45 P63	O	UARTF2 transmission data output
	RXDF3	P40 P54 P56 P82	I	UARTF3 reception data input
	TXDF3	P41 P53 P55 P83	O	UARTF3 transmission data output
Synchronous serial port (SIOF)	SCKF0	P32 P40	I/O	SIOF0 clock input/output
	SOUTF0	P33 P41	O	SIOF0 data output
	SINF0	P34 P42	I	SIOF0 data input
	SSNF0	P35 P43	I/O	SIOF0 select input/output
	SCKF1	P60	I/O	SIOF1 clock input/output
	SOUTF1	P61	O	SIOF1 data output
	SINF1	P62	I	SIOF1 data input
	SSNF1	P63	I/O	SIOF1 select input/output
Successive approximation type A/D converter (SA-ADC)	VREF	VREF	I	Reference voltage positive input for SA-ADC
	VREFN	VREFN	I	Reference voltage negative input for SA-ADC
	AIN0	P32	I	SA-ADC analog input channel 0
	AIN1	P33	I	SA-ADC analog input channel 1
	AIN2	P34	I	SA-ADC analog input channel 2
	AIN3	P35	I	SA-ADC analog input channel 3
	AIN4	P36	I	SA-ADC analog input channel 4
	AIN5	P37	I	SA-ADC analog input channel 5
	AIN6	P50	I	SA-ADC analog input channel 6
	AIN7	P51	I	SA-ADC analog input channel 7
	AIN8	P52	I	SA-ADC analog input channel 8
	AIN9	P55	I	SA-ADC analog input channel 9
	AIN10	P56	I	SA-ADC analog input channel 10
	AIN11	P57	I	SA-ADC analog input channel 11
CMP	CMP0P	P46	I	Input (+) for analog comparator 0
	CMP0M	P47	I	Input (-) for analog comparator 0
	CMP1P	P80	I	Input (+) for analog comparator 1
	CMP1M	P81	I	Input (-) for analog comparator 1
	CMP2P	P82	I	Input (+) for analog comparator 2
	CMP2M	P83	I	Input (-) for analog comparator 2
Other	—	NC	—	Not connected anywhere. Do connect nothing.
	—	DPAD	—	This is pad on the bottom of WQFN package. Do connect nothing.

TERMINATION OF UNUSED PINS

Table 6 Termination of unused pins

Pin	Pin termination
RESET_N	Connect to V_{DD}
BRMPN	Open
SWC	Connect a pull-up resistor.
SWD	Connect a pull-up resistor.
VREF	Connect to V_{DD}
VREFN	Connect to V_{SS}
HXT0, HXT1	Open
XT0, XT1	Open
P20 ~ P23 P30 ~ P37 P40 ~ P47 P50 ~ P57 P60 ~ P66 P70 ~ P77 P80 ~ P85	Open
DPAD	Open
NC	Open

[Note]

- **For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.**

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta=+25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta=+25°C		-0.3 to +2.0	V
Input voltage 1 (except HXT0, HXT1 and power supply pins)	V_{IN1}	Ta=+25°C		-0.3 to V_{DD}+0.3 *1	V
Input voltage 2 (HXT0, HXT1 pins)	V_{IN2}	Ta=+25°C		-0.3 to +2.0	V
Output voltage 1	V_{OUT1}	Ta=+25°C		-0.3 to V_{DD}+0.3 *1	V
"H" level output current	I_{OUTH}	Ta=25°C	1pin	-12 *2	mA
			Total	-60 *2	
"L" level output current	I_{OUTL}		1pin	+16	mA
			Total	+60	
Power dissipation	PD	Ta=+25°C		0.9	W
Storage temperature	T_{STG}	–		-55 to +150 *3	°C

*1: 6.5V or lower
*2: The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*3: Please observe a storage conditions shown in the document "Board Mounting (soldering)" about the storage conditions until implementation.

[Note]
- **Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied.**

Recommended Operating Conditions

(V_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambient)	T_a	–	-40 to +105	°C
Operating temperature (Chip-Junction)	T_j	–	-40 to +115	°C
Operating voltage 1	V_{DD}	–	2.3 to 5.5	V
Operating frequency (CPU)	f_{OP}	–	LSCLK: 32.768k HSCLK: up to 48M	Hz
Low speed crystal oscillation frequency *1	f_{XTL}	–	32.768k	Hz
High speed crystal oscillation frequency *1	f_{OSC}	–	20 or 40	MHz
VDDL pin external capacitance	C_L	–	1.0 ± 30%	µF

*1: See "Operation confirmed oscillator" as for crystal oscillation unit. It is necessary to evaluate the matching in the mounting circuit. Please ask the oscillator manufacturer for a matching evaluation and check the oscillation characteristics.

Thermal characteristics

The maximum chip-junction temperature, T_{jmax}, is estimated using the following equation.

$T_{j\,max} = T_{a\,max} + P_{D\,max} \times \theta_{ja}$
$T_{a\,max}$: maximum ambient temperature
$P_{D\,max}$: LSI maximum power dissipation
θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Table 7 Package's Thermal Resistance

Parameter	Symbol	Package type	Value		Unit
			L1	L2	
Thermal resistance	θ_{ja}	TQFP48	45.8	42.6	°C/W
		WQFN48	27.6	23.9	
		TQFP64	43.1	40.4	
		WQFN64	26.1	22.6	

PCB conditions:

PCB name	L1	L2	Unit
PCB size (L / W / T)	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layers	1	2	layer
Wiring density	60% (top layer)	60% (top and bottom layer)	—
Wind condition	No wind (0m/s)		—

Current Consumption

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Condition		Rating			Unit	Measuring circuit
	Operating mode	Status of clocks *1	Min.	Typ.*2	Max. Tj ≤ +115°C		
IDD1	STOP	All clocks are stopped.	—	2	450	μA	1
IDD2-1R	HALT (High speed oscillation off)	RC32K is oscillating. XT32K is stopped.	—	3.5	460	μA	
IDD3	CPU running SYSCLK=32.768kHz (High speed oscillation off)	RC32K is oscillating. XT32K is stopped.	—	27	500	μA	
IDD5-H40	CPU running SYSCLK=40MHz	High speed crystal oscillation 40MHz mode HSCLK = 40MHz	—	9	12	mA	
IDD5-H48	CPU running SYSCLK=48MHz	PLL mode HSCLK = 48MHz High speed crystal oscillation is stopped.	—	10	12	mA	

*1: LTBC and WDT is operating except IDD1, and all clock supply to peripheral circuits are stopped by block control.
*2: On the condition of VDD=3.0V, Ta=+25°C

Input / Output pin 1

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage1 "H"/"L" level (all input/output port)	VOH1	IOH1=-10mA V_{DD} ≥ 4.5V		V_{DD} -1.5	—	—	V	2
		IOH1=-1mA V_{DD} ≥ 2.3V		V_{DD} -0.5	—	—		
	VOL1	IOL1=+10mA V_{DD} ≥ 4.5V		—	—	1.5		
		IOL1=+1mA V_{DD} ≥ 2.3V		—	—	0.5		
Output voltage2 "L" level (all input/output port)	VOL2	When N-ch open drain output mode is selected	IOL2=+15mA V_{DD} ≥ 4.5V	—	—	0.7		
			IOL2=+8mA V_{DD} ≥ 3.0V	—	—	0.5		
			IOL2=+3mA V_{DD} ≥ 2.3V	—	—	0.4		
Input current1 (RESET_N)	IIH1	VIH1=V_{DD}		—	—	1	μA	4
	IIL1	VIL1=V_{SS}		-1[*1]	—	—		
Input current3 (all input/output port)	IIL3	VIL1=V_{SS}(pull-up mode)[*2]		-250[*1]	-30[*1]	-2[*1]		
	V/IIL3	VIL1=V_{SS}(pull-up mode)[*2]		22	100	800	kΩ	
	IIH3Z	VIH1=V_{DD}(High impedance mode)		—	—	1	μA	
	IIL3Z	VIL1=V_{SS}(High impedance mode)		-1[*1]	—	—		
Input voltage1 (all input port, input/output port)	VIH1	—		0.7 × V_{DD}	—	V_{DD}	V	5
	VIL1	—		0	—	0.3 × V_{DD}		
Pin capacitance (all input port, input/output port)	CPIN	f=10kHz Ta=25°C		—	—	10	pF	—

*1: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*2: Measurement conditions: Typ: V_{DD} = 3.0V, Max: V_{DD} = 2.3V, Min: V_{DD} = 5.5V

Input / Output pin 2

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V_{DD} ≥ 4.5V	-10*3*5	—	—	mA	3
			V_{DD} ≥ 2.3V	-1*3*5	—	—		
"H" level output total current1 *1*4	IOH3	Total of group C or D ** (duty ≤ 50%)	V_{DD} ≥ 4.5V	-20*5	—	—		
			V_{DD} ≥ 2.3V	-10*5	—	—		
		All pin total (duty ≤ 50%)	V_{DD} ≥ 4.5V	-40*5	—	—		
			V_{DD} ≥ 2.3V	-20*5	—	—		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V_{DD} ≥ 4.5V	—	—	10*3		
			V_{DD} ≥ 2.3V	—	—	1*3		
"L" level output current2 *6	IOL2	1pin (N-ch open drain output mode)	V_{DD} ≥ 4.5V	—	—	15*3		
			V_{DD} ≥ 3.0V	—	—	8*3		
			V_{DD} ≥ 2.3V	—	—	3*3		
"L" level output total current *2*4	IOL3	Total of group A or B ** (N-ch open drain output mode, duty≤50%)	V_{DD} ≥ 4.5V	—	—	23		
			V_{DD} ≥ 3.0V	—	—	16		
			V_{DD} ≥ 2.3V	—	—	10		
		All pin total (N-ch open drain output mode, duty≤50%)	V_{DD} ≥ 4.5V	—	—	46		
			V_{DD} ≥ 2.3V	—	—	20		
Output leak (all input/output port)	IOOH	VOH=V_{DD} (High impedance mode)		—	—	+1	μA	
	IOOL	VOL=V_{SS} (High impedance mode)		-1*5	—	—		

** : Group A is "P22 to P23, P30 to P37, P40 to P47, P80 to P85",
group B is "P20 to P21, P50 to P57, P60 to P66, P70 to P77",
group C is "P20 to P23, P40 to P44, P60 to P62, P70 to P77",
group D is "P30 to P37, P45 to P47, P50 to P57, P63 to P66, P80 to P85".

*1: Tolerable current what can flow out from VDD pin to the output pin
*2: Tolerable current what can flow in from the output pin to VSS pin
*3: The total output current need to be within the rated range of IOH3 and IOL3.
*4: The total current is on the condition of Duty≤50% (same applies to IOH1).
When the duty ＞50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3=100mA and n=80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*5: The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*6: These values are satisfied with VOH1, VOL1 and VOL2.

On-chip Oscillator

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
RC32K frequency	f_{RCL1}	—	Typ. -2.0%	32.768	Typ. +2.0%	kHz	1
PLL oscillation frequency	f_{PLL1}	Tj=-40 to +95ºC with RC32K	Typ. -1.5%	48	Typ. +1.5%	MHz	
		Tj=-40 to +115ºC with RC32K	Typ. -2.0%		Typ. +2.0%		
PLL oscillation stabilization time	T_{PLL}	—	—	—	5	ms	

The frequency is the factory default specification. It may vary depending on the board mounting.

High speed Crystal Oscillation

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequency *1 *2	f_{OSC}	—	—	20 or 40	—	MHz
Crystal oscillation start time	T_{OSC}	—	—	—	3	ms

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator, and the external capacitance (C_{GL2}/C_{DL2}). As those parameters changes depending the crystal resonator, The matching evaluation using the actual PCB is required. Ask crystal resonator manufacture the matching evaluation to confirm the oscillation characteristics.

*2: In order to obtain the expected oscillation characteristics, it is necessary to design a PCB that considers the material and wiring pattern of the circuit board, as well as the wiring capacitance and parasitic capacitance of quartz crystals and terminals, etc. See below as reference for a PCB design.
- Keep the wiring layout for configuring the external circuit as short as possible.
- In order to shorten the wiring to the crystal unit and the crystal oscillator external capacitance as much as possible, place the crystal unit and the crystal oscillator external capacitance in close proximity to the MCU.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

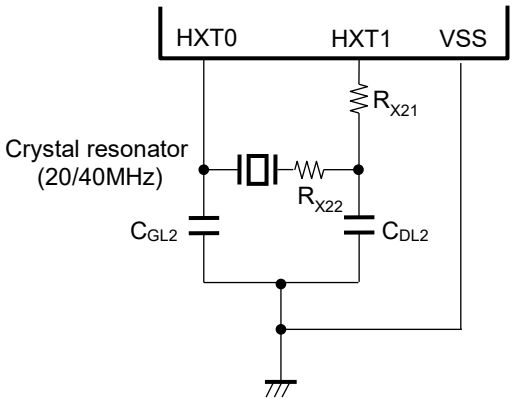


Figure 7 Example of external circuit for High speed Crystal Oscillation

Low speed Crystal Oscillation

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequency *1 *2	f_{XTL}	—	—	32.768	—	kHz
Crystal oscillation start time	T_{XTL}	—	—	—	2	s

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator, and the external capacitance (C_{GL}/C_{DL}). As those parameters changes depending the crystal resonator, The matching evaluation using the actual PCB is required. Ask crystal resonator manufacture the matching evaluation to confirm the oscillation characteristics.

*2: In order to obtain the expected oscillation characteristics, it is necessary to design a PCB that considers the material and wiring pattern of the circuit board, as well as the wiring capacitance and parasitic capacitance of quartz crystals and terminals, etc. See below as reference for a PCB design.
- Keep the wiring layout for configuring the external circuit as short as possible.
- In order to shorten the wiring to the crystal unit and the crystal oscillator external capacitance as much as possible, place the crystal unit and the crystal oscillator external capacitance in close proximity to the MCU.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

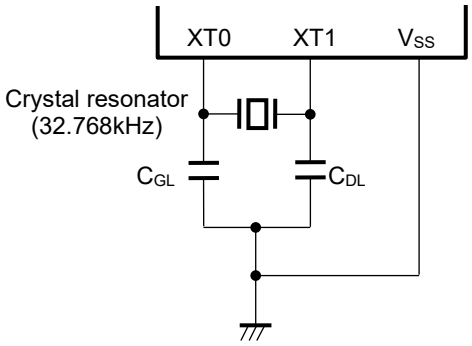


Figure 8 Example of external circuit for Low speed Crystal Oscillation

External Clock Input

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	—	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input pulse width	t_{EXCKW}	—	14.5	—	—	µs

EXI/TMCKI input

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXI}	—	—	—	4	MHz
Input pulse width	t_{WPI1}	When the analog filter is disabled	50	—	—	ns
	t_{WPI2}	When the analog filter is enabled	250	—	—	ns
Filterd pulse width	t_{WFI2}	When the analog filter is enabled	—	—	50	ns

I²C Bus Interface

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Rating						Unit
		Standard Mode			Fast Mode			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Voltage	V_{DD}	2.3	—	5.5	2.3	—	5.5	V
SCL clock frequency	f_{SCL}	0	—	100	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	4.0	—	—	0.6	—	—	µs
SCL “L” level time	t_{LOW}	4.7	—	—	1.3	—	—	µs
SCL “H” level time	t_{HIGH}	4.0	—	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	4.7	—	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	0	—	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	0.25	—	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	4.0	—	—	0.6	—	—	µs
Bus-free time	t_{BUF}	4.7	—	—	1.3	—	—	µs

Configure the I2F Transfer Rate Setup Counter (I2F0BC) so that meet these specifications.

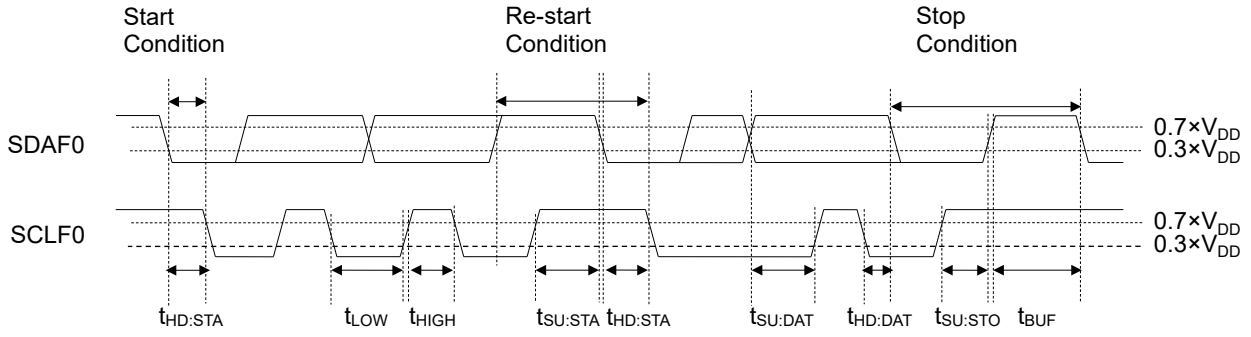


Figure 9 I²C Bus timing

Synchronous Serial Port

Slave mode

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCKF input cycle	t_{SCYC}	—	500*1	—	—	ns
SCKF input pulse width	t_{SW}	—	200	—	—	ns
SOUTF output delay time	t_{SD}	—	—	—	180	ns
SINF input setup time	t_{SS}	—	50	—	—	ns
SINF input hold time	t_{SH}	—	50	—	—	ns

*1: It is more than 2 cycles of the HSCLK.

Master mode

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCKF output cycle	t_{SCYC}	—	166*2	SCLK*2	—	ns
		V_{DD} > 2.7	83*2			
SCKF output pulse width	t_{SW}	—	t_{SCYC}×0.4	t_{SCYC}×0.5	t_{SCYC}×0.6	ns
SOUTF output delay time	t_{SD}	—	—	—	80	ns
		V_{DD} > 2.7			30	
SINF input setup time	t_{SS}	—	50	—	—	ns
		V_{DD} > 2.7	20			
SINF input hold time	t_{SH}	—	50	—	—	ns
		V_{DD} > 2.7	20			

*2: The clock period which is selected by the SF0BR9-0 of SIOFn port register (SFnBRR). The minimum value is at HSCLK = 48MHz without an accuracy of frequency.

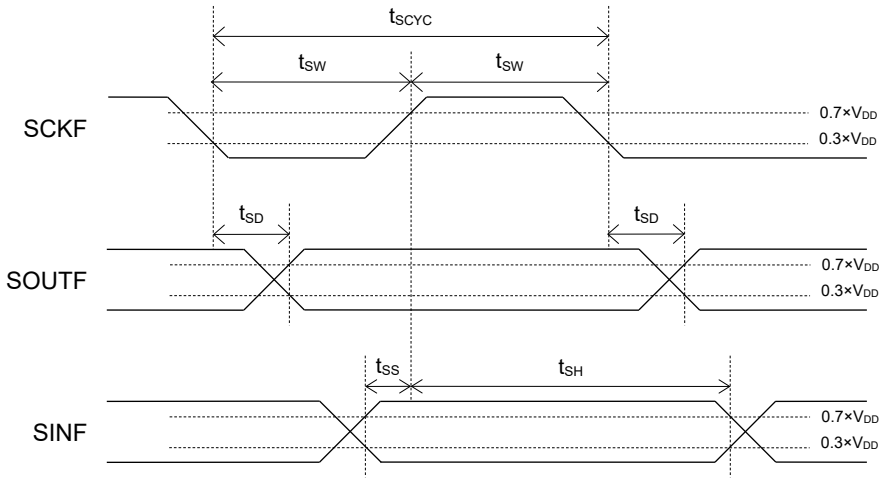


Figure 10 synchrpmpis serial port timing

Reset

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Reset pulse width	P_{RST}	—	10	—	—	µs	1

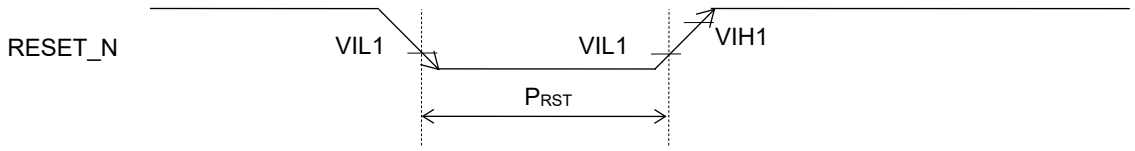


Figure 11 Reset input timing

[Note]
- **RESET_N input shorter pulse than the Reset pulse width (P_{RST}) valid time should be avoided. The shorter pulse input may cause unexpected behavior.**

Slope of Power supply and Power On Reset

(V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
V_{DD} Power on rising slope	S_{VR}	—	—	—	60	V/ms	1
V_{DD} Power on falling slope	S_{VF}	—	—	—	2	V/ms	
Power on reset detection voltage	V_{PORR}	At Power up (rising)	1.50	1.67	2.10	V	
	V_{PORF}	At Power down (falling)	1.45	1.65	2.05	V	
Power on reset minimum pulse width	P_{POR}	—	500	—	—	µs	
CPU operation start time (from the release of reset to the CPU starts to run)	t_{CPUI}	—	13	21	35	ms	—

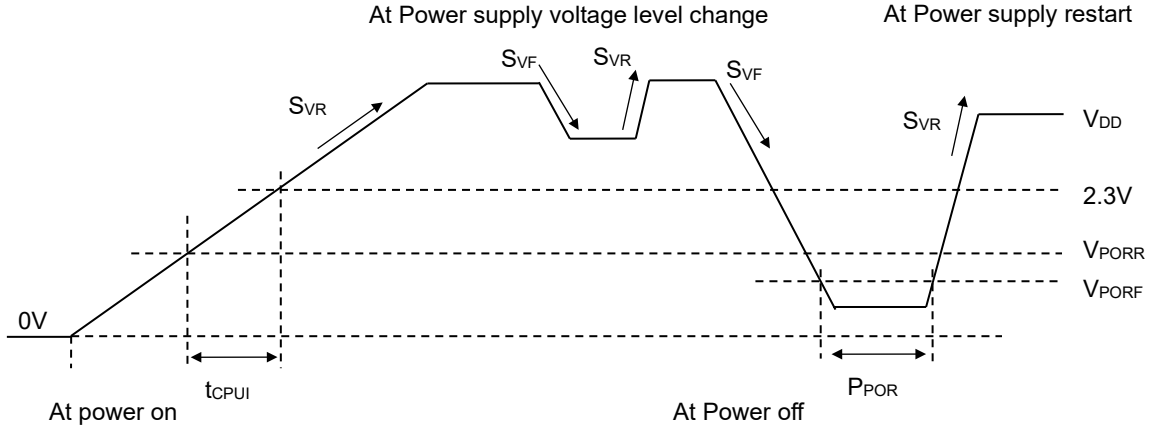


Figure 12 Power supply

[Note]
- **If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction. Apply prevent measurement such as bypass capacitors or external reset input, and so on.**
- **Set VDD to 2.3V or higher before starting CPU operation.**

VLS

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating						Unit	Measuring circuit
			Falling V_{VLSF}			Rising V_{VLSR}				
		VLS0LV[*1]	Min.	Typ.	Max.	Min.	Typ.	Max.		
VLS threshold voltage	V_{VLSR} V_{VLSF}	0H	3.83	3.99	4.49	3.84	4.05	4.65	V	1
		1H	3.53	3.68		3.55	3.74			
		2H	2.92	3.05	4.14	2.94	3.10	4.28		
		3H	2.84	2.96		2.85	3.01			
		4H	2.72	2.84	3.42	2.74	2.89	3.54		
		5H	2.65	2.76		2.66	2.80			
		6H	2.55	2.66	3.31	2.56	2.70	3.44		
		7H	2.43	2.54		2.45	2.58			
		8H	2.35	2.45	3.18	2.36	2.49	3.30		
		9H	2.25	2.35		2.27	2.39			

[*1]: Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS current consumption	I_{VLS}	—	—	10	—	nA	1

Analog Comparator

(V_{DD}=2.3 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Same phase input voltage range	V_{CMR}	—	0.1	—	V_{DD} -1.2	V	1
Input offset	V_{CMOF}	Ta=+25 °C, V_{DD}=5.0V	—	±5	—	mV	
Propagation delay	V_{CTS}	Input amplitude ±100mV	—	0.5	1.2	μs	

Successive Approximation Type A/D Converter

(V_{DD}=2.3 to 5.5V, V_{SS}=V_{REFN}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit
Resolution	n_{AD}	—		—	—	12	bit
Conversion clock (nominal value)	f_{ADCLK}	V_{DD} ≥ 4.5V, V_{REF} ≥ 4.5V		32.768	—	24000	kHz
		V_{DD} ≥ 2.7V, V_{REF} ≥ 2.7V		32.768	—	16000	kHz
		V_{DD} ≥ 2.4V, V_{REF} ≥ 2.4V		32.768	—	8000	kHz
		V_{DD} ≥ 2.3V, V_{REF} ≥ 2.1V		32.768	—	2500	kHz
Conversion time	t_{CONV}	f_{ADCLK} = 24MHz		0.917	—	—	µs
		f_{ADCLK} = 32.768kHz		518.799	—	—	µs
SA-ADC reference potential	V_{REF}	V_{DD} ≥ V_{REF}		2.1	—	V_{DD}	V
Overall error	—	4.5V ≤ VREF ≤ 5.5V		-6.5	—	+6.5	LSB
Integral non-linearity error	INL_{AD}	f_{ADCLK}=24MHz	4.5V ≤ V_{REF}	-4	—	+4	LSB
		f_{ADCLK}=16MHz	2.7V ≤ V_{REF}	-4	—	+4	
		f_{ADCLK}=8MHz	2.4V ≤ V_{REF}	-6	—	+6	
		f_{ADCLK} ≤ 2.5MHz	2.1V ≤ V_{REF}	-8	—	+8	
Differential non-linearity error	DNL_{AD}	f_{ADCLK}=24MHz	4.5V ≤ V_{REF}	-3	—	+3	
		f_{ADCLK}=16MHz	2.7V ≤ V_{REF}	-3	—	+3	
		f_{ADCLK}=8MHz	2.4V ≤ V_{REF}	-5	—	+5	
		f_{ADCLK} ≤ 2.5MHz	2.1V ≤ V_{REF}	-7	—	+7	
Zero-scale error	ZSE	f_{ADCLK}=16, 24MHz		-6	—	+6	
		f_{ADCLK}=8MHz		-8	—	+8	
		f_{ADCLK} ≤ 2.5MHz		-10	—	+10	
Full-scale error	FSE	f_{ADCLK}=16, 24MHz		-6	—	+6	
		f_{ADCLK}=8MHz		-8	—	+8	
		f_{ADCLK} ≤ 2.5MHz		-10	—	+10	

The current flows during the SA-ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1µF capacitor on the ADC input pin is recommended for noise reduction.

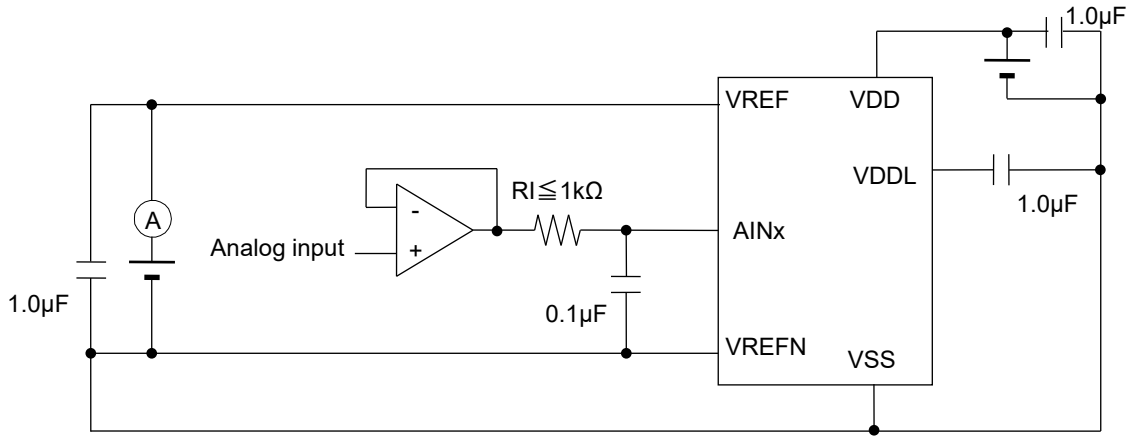


Figure 13 SA-ADC connection

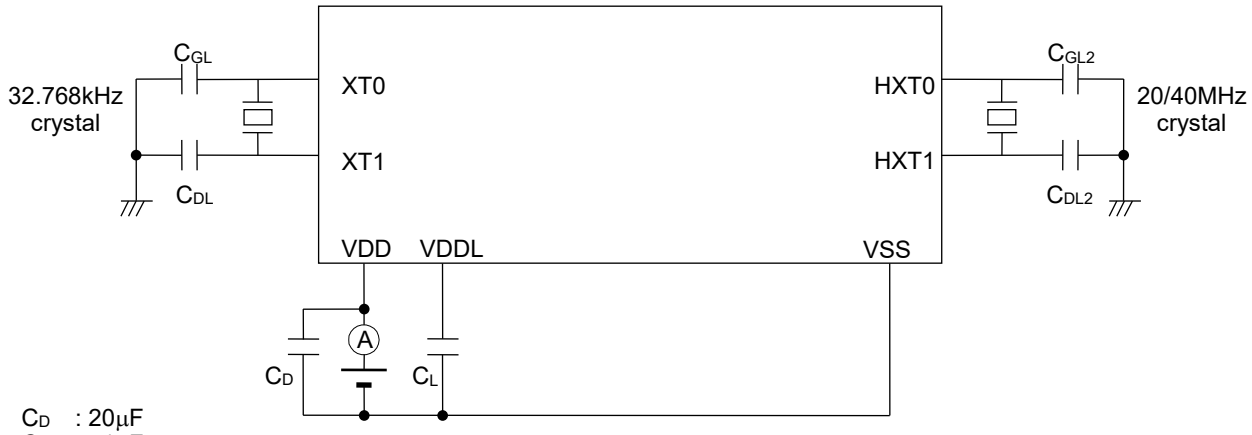
Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At writing/erasing		-40 to +85	°C
		Flash ROM, At writing/erasing		0 to +40	°C
Operating voltage	V_{DD}	At writing/erasing		2.3 to 5.5	V
Maximum rewrite count	C_{EPD}	Data Flash		10,000	times
	C_{EPP}	Program Flash		100	
Erasing unit	–	Block erasing	Program Flash	Byte	Byte
			Data Flash	8K	
		Sector erasing	Program Flash	Byte	Byte
			Data Flash	256	
Erasing time (Max.)	–	Block erasing / Sector erasing		50	ms
Writing unit	–	Program Flash		4	Byte
		Data Flash		1	
Writing time (Max.)	–	Program Flash		80	µs
		Data Flash		40	
Data retention period	YDR	rewriting count 100 times		15	years

Measuring circuit

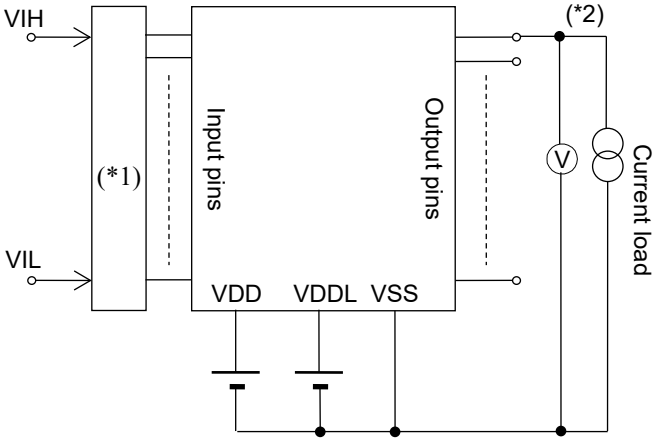
Measuring circuit 1



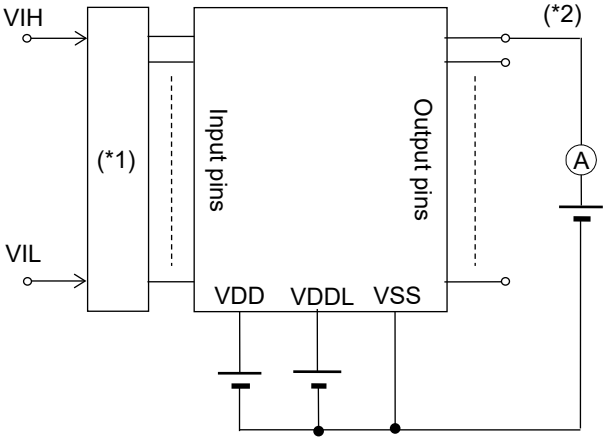
C_D : 20µF
C_L : 1µF
C_{GL} : 12pF
C_{DL} : 12pF
C_{GL2} : 16pF
C_{DL2} : 16pF

32.768kHz crystal unit: VT-200-F, SII
40MHz crystal unit: CX2016SA, Kyocera

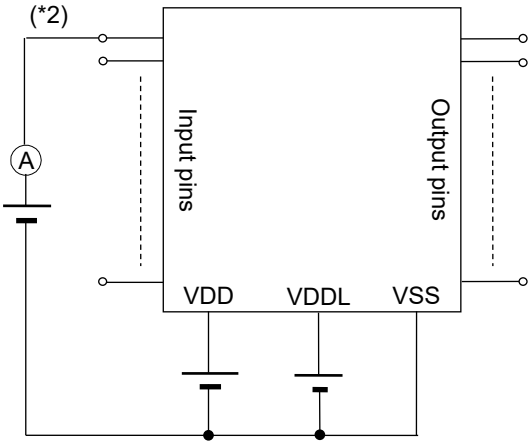
Measuring circuit 2



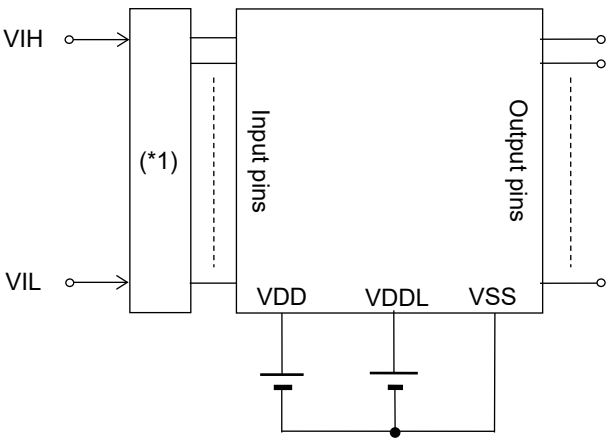
Measuring circuit 3



Measuring circuit 4



Measuring circuit 5



(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

OPERATION CONFIRMED OSCILLATOR

The operation of the following oscillation circuit constants has been confirmed by matching evaluation using our reference board and the following oscillator. However, consider the following oscillation circuit constants as reference values because the wiring capacitance differs from the actual application circuit.
Contact each oscillator manufacturer for the latest information on each oscillator.
We do not take any responsibility for damages caused by defects in the oscillator itself, matching between the oscillator and this product, or the termination of production of the following oscillators. Please contact the relevant oscillator manufacturer.

Table 7 Low-speed oscillator (32.768kHz)

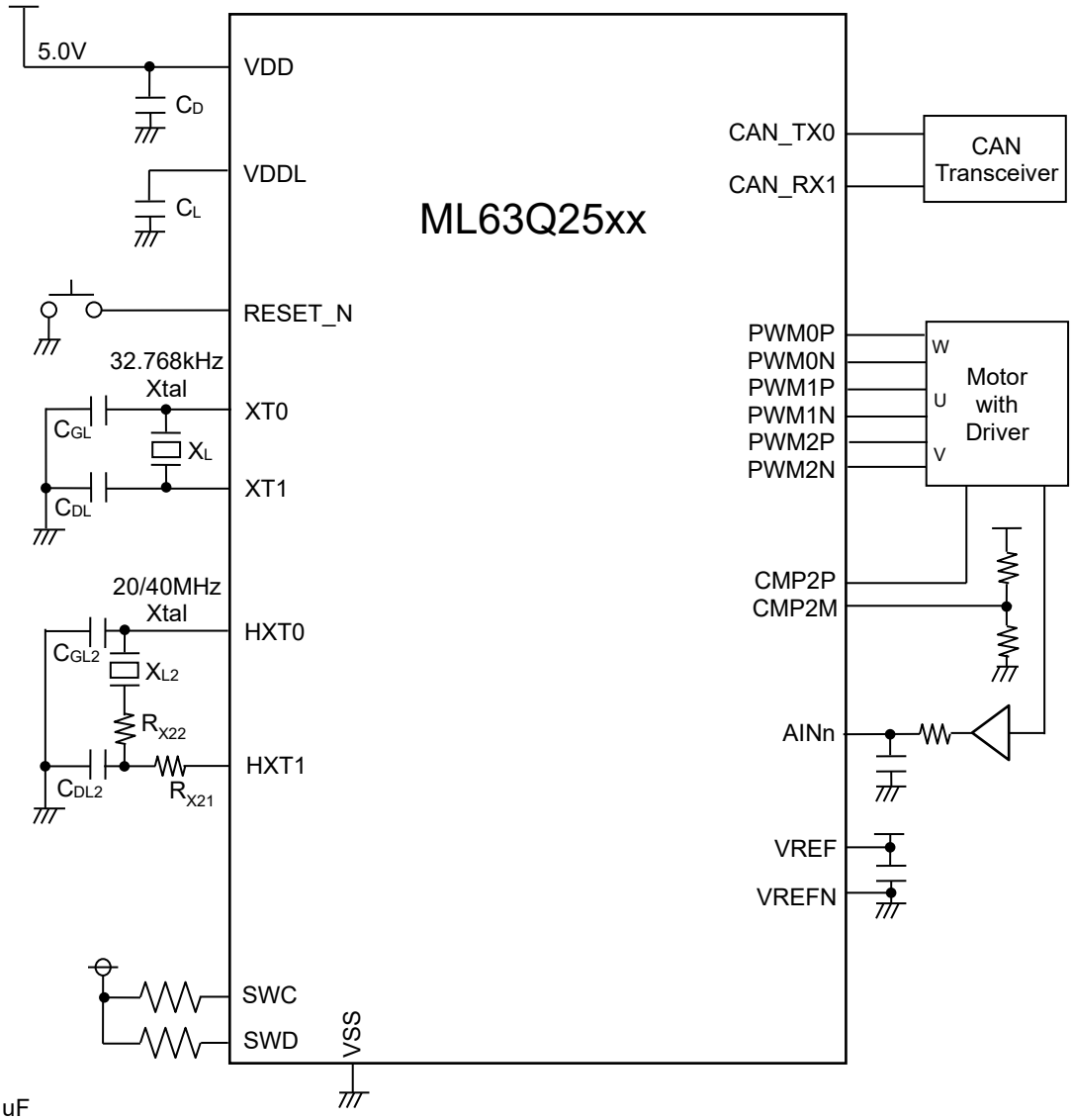
Oscillator manufacturer	Product name	Oscillator type	Load capacity	Oscillation mode*1			Oscillator circuit constant (reference value) *2*3	
			C_L [pF]	LP	STD	TOUGH	C_{DL} [pF]	C_{GL} [pF]
Seiko Instruments Inc.	SSP-T7-F	Crystal unit	7	●	-	-	15	12
			9	-	●	-	20	20
			12.5	-	-	●	27	27
	SC-32S	Crystal unit	7	●	-	-	15	15
			9	-	●	-	20	20
			12.5	-	-	●	27	27
	SC-20S	Crystal unit	7	●	-	-	15	15
			9	-	●	-	22	20
			9	-	-	●	22	20
	SC-16S	Crystal unit	6	●	-	-	15	12
			7	-	●	-	16	16
			9	-	-	●	22	22
DAISHINKU CORP.	DST1610A	Crystal unit	6	●	●	●	15	15
NIHON DEMPA KOGYO CO., LTD	NX3215SA / CHP-MUA-16	Crystal unit	6	●	●	●	12	12
	NX2012SA / CHP-MUB-18	Crystal unit	6	●	●	●	12	12
	NX1610SA / CHP-MUD-2	Crystal unit	6	●	●	●	12	12

Table 8 High-speed oscillator

Oscillator manufacturer	Product name	Oscillator type	Frequency	Load capacity	Oscillator circuit constant (reference value) *2*3			
			F [MHz]	C_L [pF]	C_{DL} [pF]	C_{GL} [pF]	R_{X21} [Ω]	R_{X22} [Ω]
DAISHINKU CORP.	DSX321G	Crystal unit	40	8	9	9	0	15
			20	8	9	9	0	15
KYOCERA Corporation	CX2016SA	Crystal unit	40	8	8	8	0	0
			20	8	8	8	0	0
NIHON DEMPA KOGYO CO., LTD	NX2016SA / CHP-CZS-87	Crystal unit	40	8	8	8	100	0
	NX2016SA / CHP-CZS-86	Crystal unit	20	8	12	12	560	0
	NX1612SA / CHP-CIS-29	Crystal unit	40	8	8	8	100	0

Comments:
*1 : For each Oscillation mode, "●" is marked where matching is confirmed. "-" is marked where matching is not confirmed.
*2 : These oscillation circuit constants are reference values. It is necessary to optimize the capacity value in your environment. For details, contact each oscillator manufacturer.
*3 : These results vary depending on the wiring capacitance and parasitic capacitance.

APPLICATION CIRCUIT EXAMPLE

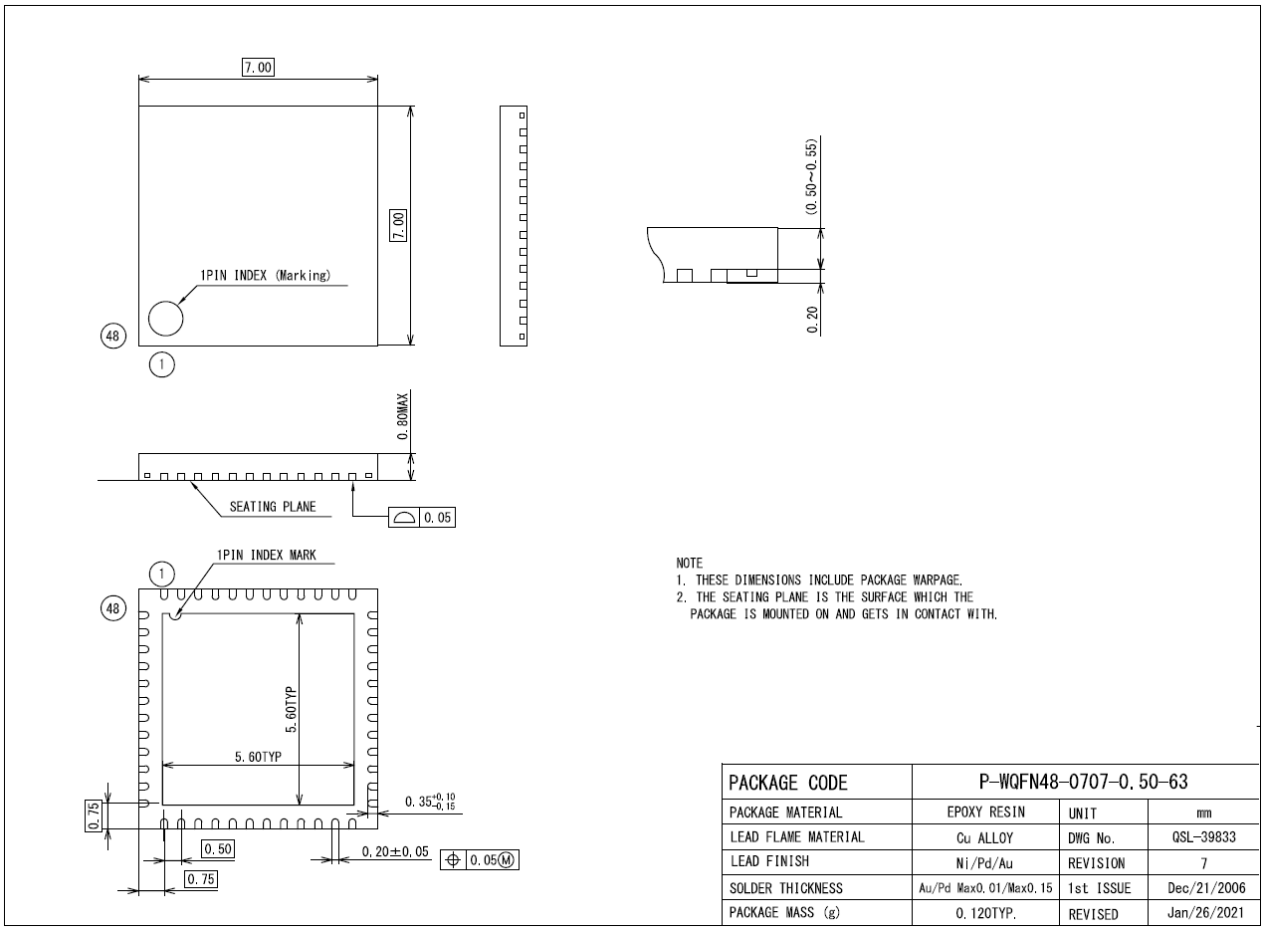


C_D : 1uF
C_L, : 1uF
X_L,C_{GL},C_{DL} : See Table 7 in 'OPERATION CONFIERMD OSCILLATOR'
X_{L2},C_{GL2},C_{DL2} ,R_{X2}: See Table 8 in 'OPERATION CONFIERMD OSCILLATOR'

Figure 14 Application Circuit Example

PACKAGE DIMENSIONS

48PIN WQFN



PACKAGE CODE	P-WQFN48-0707-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39833
LEAD FINISH	Ni/Pd/Au	REVISION	7
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Dec/21/2006
PACKAGE MASS (g)	0.120TYP.	REVISED	Jan/26/2021

Figure 15 48PIN WQFN

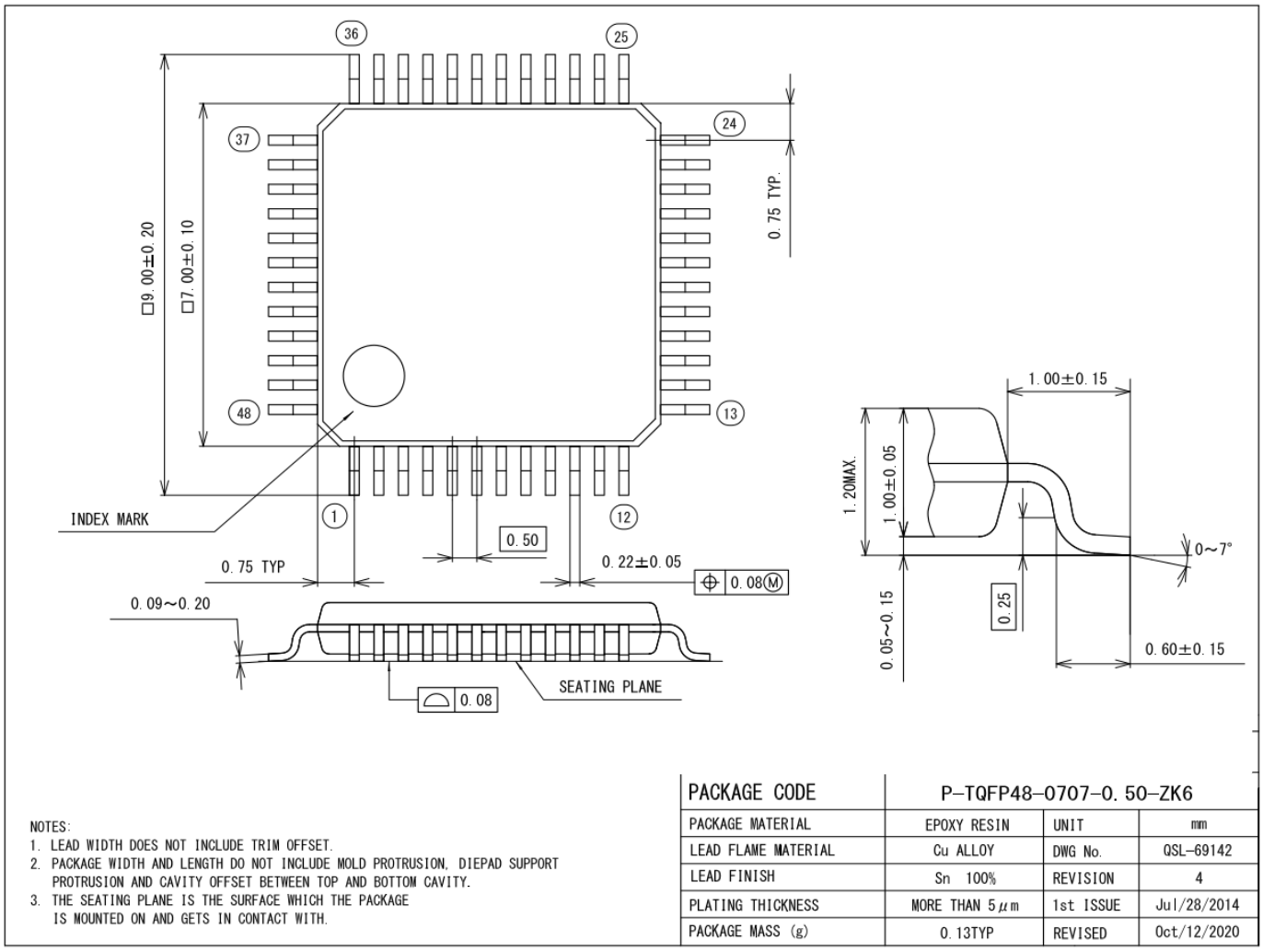
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

48PIN TQFP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

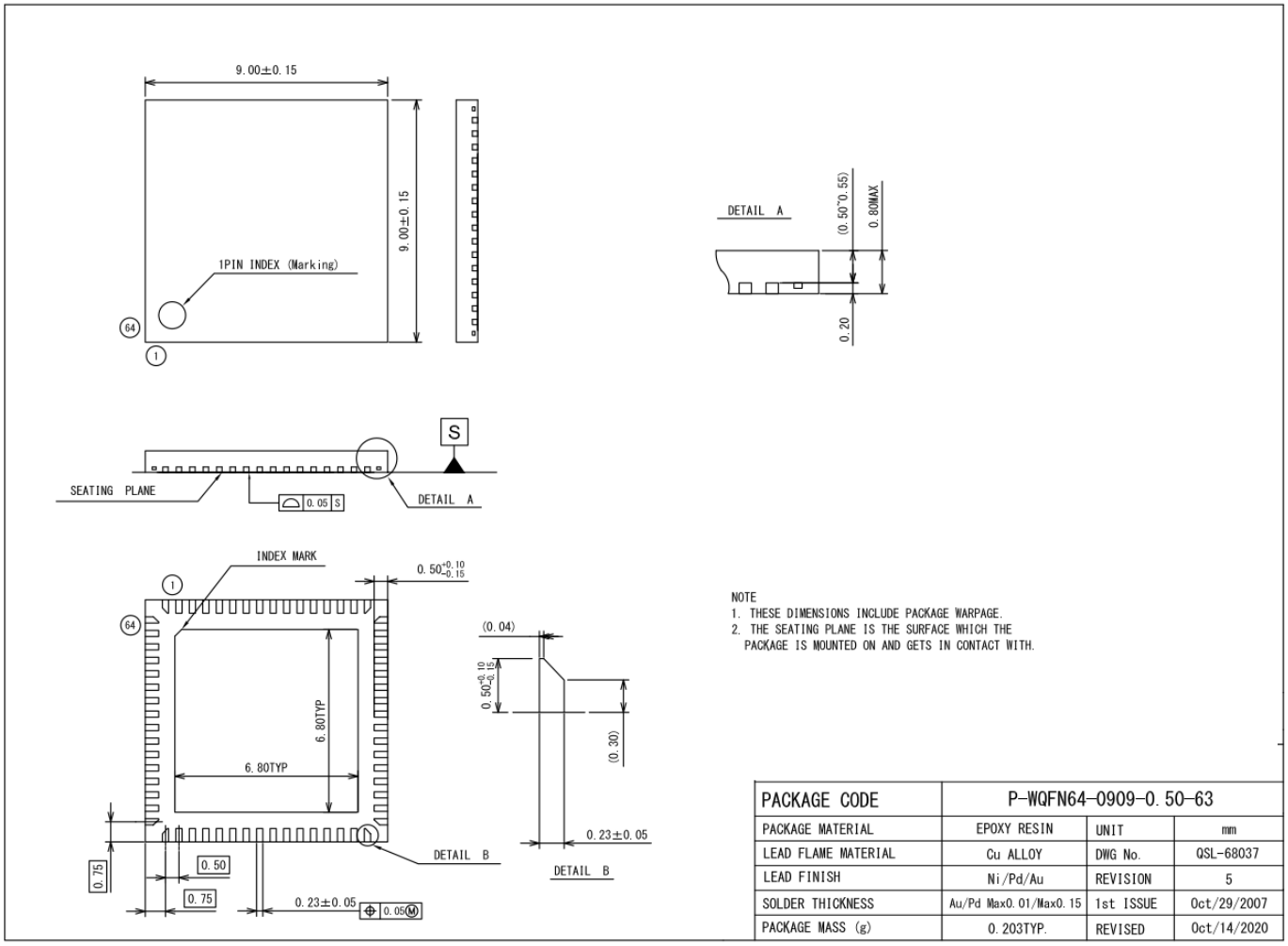
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/12/2020

Figure 16 48PIN TQFP

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64PIN WQFN



PACKAGE CODE	P-WQFN64-0909-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68037
LEAD FINISH	Ni/Pd/Au	REVISION	5
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Oct/29/2007
PACKAGE MASS (g)	0.203TYP.	REVISED	Oct/14/2020

Figure 17 64PIN WQFN

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

64PIN TQFP

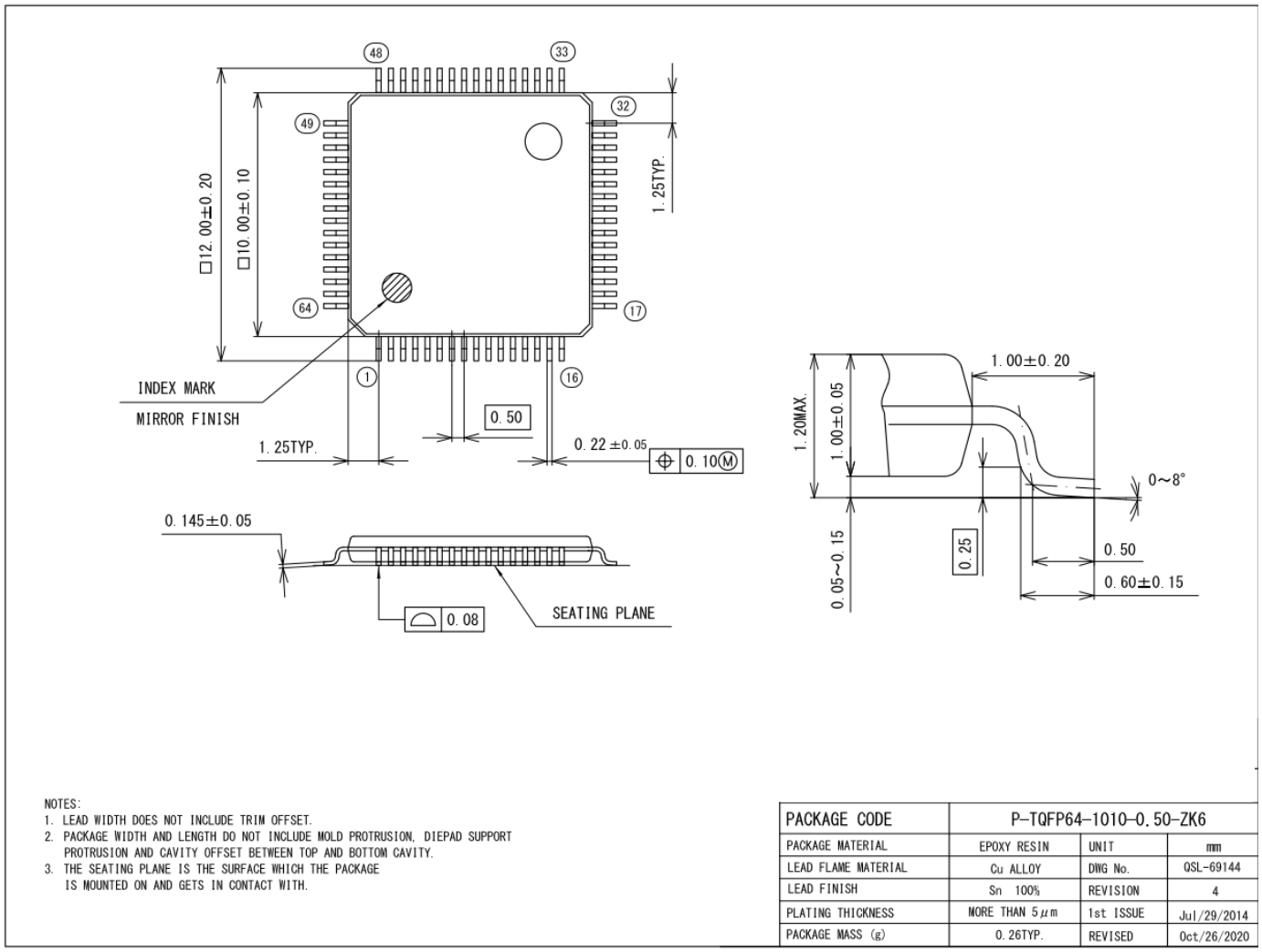


Figure 18 64PIN TQFP

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL63Q2500-01	2025/01/20	-	-	Final edition 1st Revision
FEDL63Q2500-02	2025/03/18	22, 31, 32	22, 31, 32	Added the resistor R_{X21} for the high-speed oscillator
		31	31	Updated information in “OPERATION CONFIRMED OSCILLATOR”; (Mainly adding part numbers)

Notes for product usage

Notes on this page are applicable to the all LAPIS TECHNOLOGY microcontroller products.
For individual notes on each LAPIS TECHNOLOGY microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS
   Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON
   At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
   On LAPIS TECHNOLOGY microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
   Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY
   If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCT
   Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
   When replacing from other product to LAPIS TECHNOLOGY microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS TECHNOLOGY microcontroller products.

5. USE ENVIRONMENT
   When using LAPIS TECHNOLOGY microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

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2) The Products specified in this document are not designed to be radiation tolerant.

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