Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL7396A/B/E/D-12
Issue Date: Jan. 10, 2024

ML7396A/B/E/D

Sub GHz band short range wireless transceiver IC

■Overview

The ML7396 family (ML7396A (915MHz band), ML7396B/ML7396D (920MHz band), and ML7396E (868MHz band)) are ICs for transmitting/receiving data which integrate the RF, IF, MODEM and HOST interface sections into one chip for the specified low power radio communication. The ML7396 family is used for FCC PART15, ARIB STD-108(specified low-power radio station, 920MHz-band telemeter, telecontrol and data transmission radio equipment), ETSI EN 300 220 compliant radio station, and uses a packet transmission function of IEEE802.15.4d and IEEE802.15.4g.
The ML7396D sensitivity is better than ML7396B. The ML7396D has same functions with ML7396B, and is used for same standard.

●Product Name ML7396DGD

●Application Remote control
Home, Building Security
Sensor Network
Smart Meters

■Features

- Compliant to ARIB STD T-108 (ML7396B/ML7396D)
- Compliant to FCC Part15 (ML7396A)
- Compliant to ETSI EN 300-220 (ML7396E)
- High resolution modulation by using fractional-N PLL direct modulation.
- Modulation: GFSK / GMSK, FSK / MSK
  (MSK is FSK transmission of modulation index: m=0.5)
- Data rates: 10 / 20 / 40 / 50 / 100 / 150 / 200 kbps and 400 kbps (option)
- Data coding: NRZ and Manchester codes
- Programable channel filter suited to data rates
- Programmable frequency deviation function
- TX and RX data inverse function
- 36MHz oscillator circuit
- TCXO direct inputs available
- Oscillator capacitance fine tuning function
- Frequency fine tuning function (using fractional-N PLL)
- Synchronous serial peripheral interface (SPI)
- On chip TX PA (20mW/10mW/1mW selectable)
- External TX PA control function
- RSSI indicator and threshold judgement function
- AFC function
- Antenna diversity function
- Test pattern generator (PN9, CW, 01 pattern, all"1", all"0")
- FEC function
- CRC32 (Note: This function is not compliant to IEEE802.15.4g.)
- IEEE802.15.4d/g support
  - Two 256-byte FIFOs (TX/RX common use)
  - Max packet length 2047 byte (IEEE802.15.4g mode)
  - RX Preamble pattern detection function (Programmable between 1 to 15 byte)
  - Programmable TX preamble length (Max 255 byte)
  - SFD generation and detection function (Max 4 byte)
  - Programmable CRC function (CRC32, CRC16-IBM, CRC16, CRC8 or no-CRC)
  - Whitening function

ROHM SEMICONDUCTOR

- Address filtering function
- Automatic Acknowledge (Ack TX or RX) function
- FEC function (IEEE802.15.4g mode)
  Note; Interleaving mode is not compliant to IEEE802.15.4g.

- Supply voltage: 1.8 to 3.6V (TX power 1mW mode)
  2.3 to 3.6V (TX power 10mW mode)
  2.6 to 3.6V (TX power 20mW mode)
- Operating temperature: -40 to +85 ˚C
- Current consumption (920MHz)

Sleep mode		0.6 μA (Typ.) (registor value retention)
Idle mode		1.4mA (Typ.)
TX	20mW	32 mA (Typ.)
	10mW	24 mA (Typ.)
	1mW	13 mA (Typ.)
RX		15 mA (Typ.) (@100kbps, ML7396A/B)
		16 mA (Typ.) (@100kbps, ML7396D/E)

- Package
  40 pin WQFN P-WQFN40-0606-0.50
  Pb free, RoHS compliant

■Description Convention

1) Numbers description
'0xnn' indicates hexa decimal. '0bnn' indicates binary.

Example: 0x11= 17(decimal), 0b11= 3(decimal)

2) Registers description
[<register name>: B<Bank No> <register address>] register

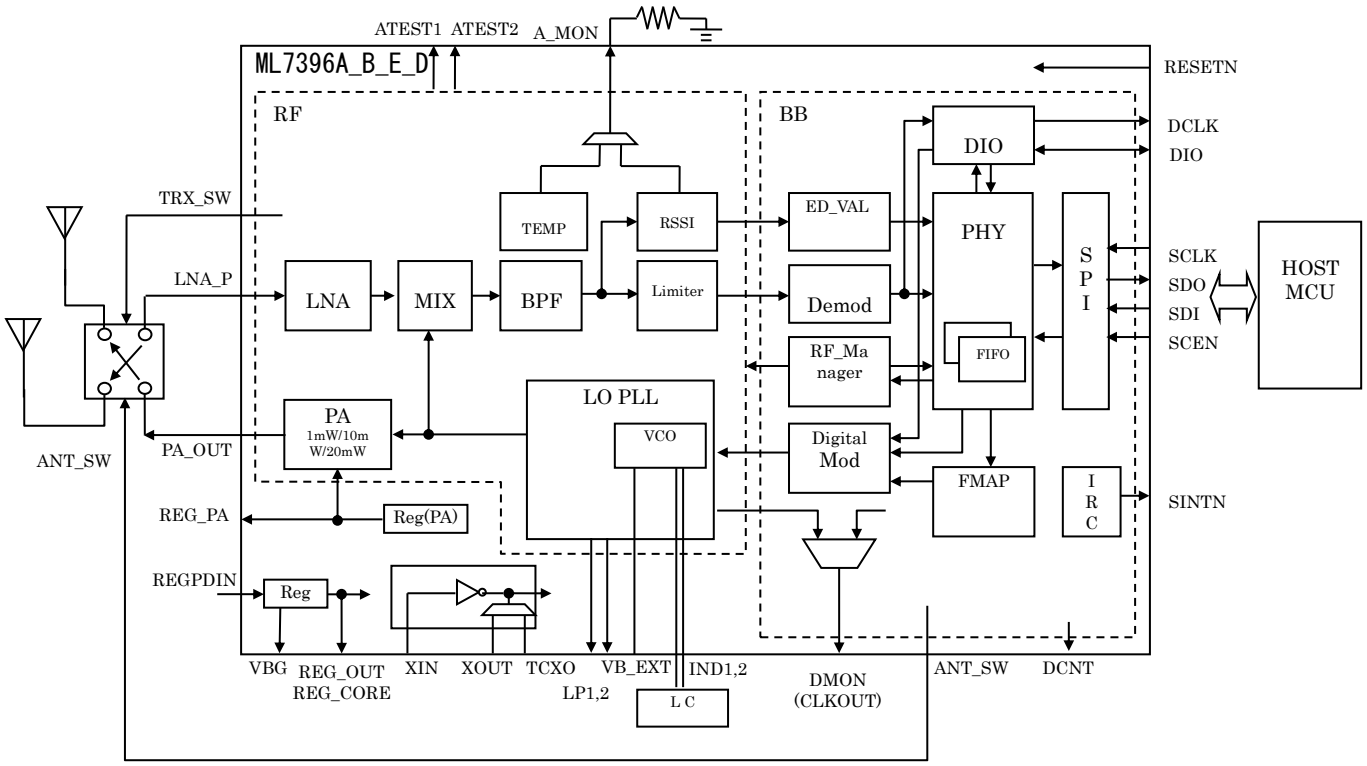
Example: **[CLK_SET:B0 0x02] register**
Register name: CLK_SET
Bank No: 0
Register address: 0x02

3) Bir name description
<bit name> ([<register name>: B<Bank No> <register address>(<bit location>)])

Example: **RATE[2:0] ([DATA_SET:B0 0x47(2-0)])**
Bit name: RATE[2:0]
Register name: DATA_SET
Bank No: 0
Register address: 0x47
Bit location: bit2 to bit0

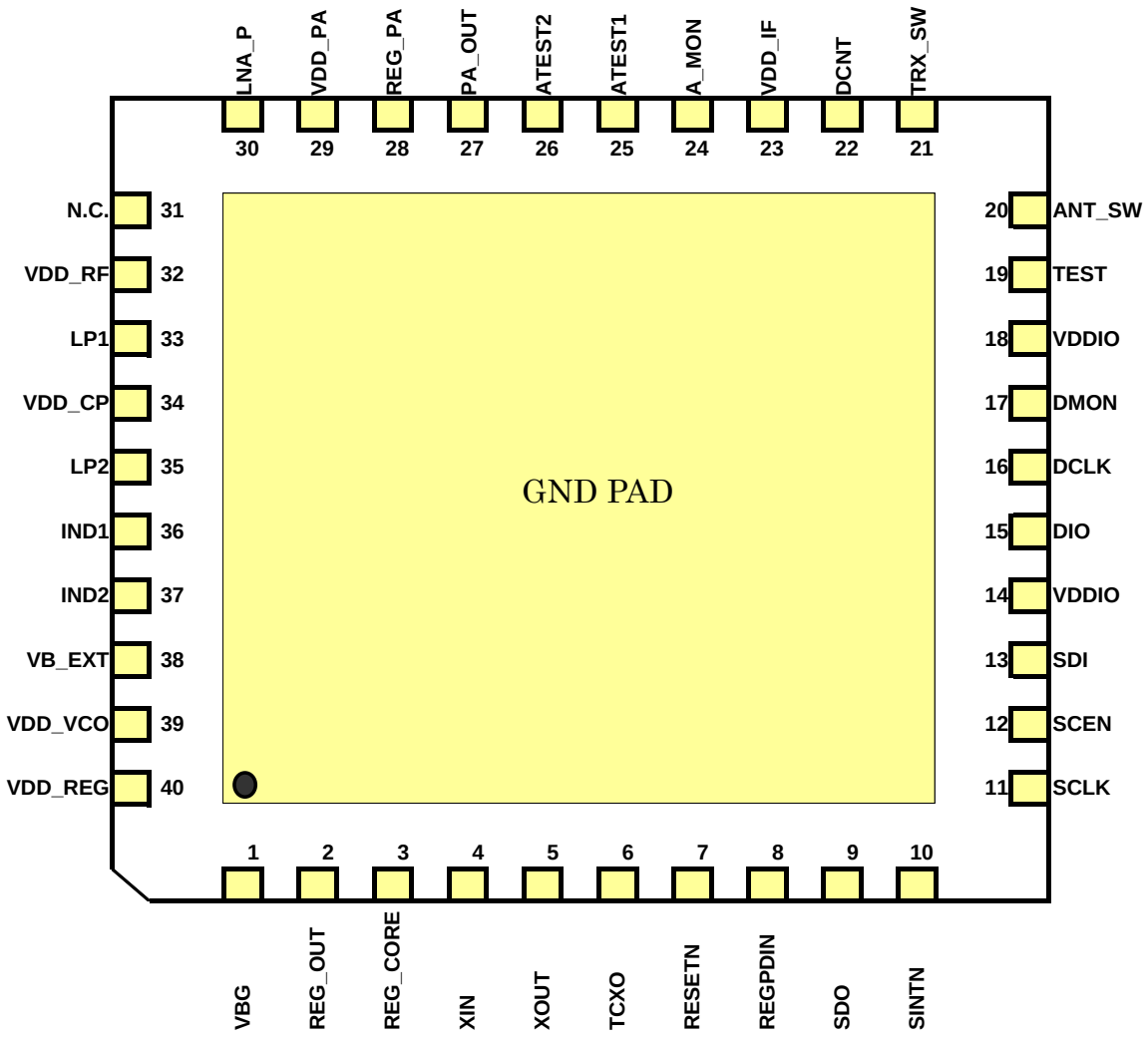
4) In this document
"TX" stands for transmittion.
"RX" stands for reception.

■Block Diagram



■PIN Configuration

40 Pin WQFN



NOTE) GND pad in the middle of the IC is reverse side (name: GND PAD)

■PIN Definitions

Symbols

I_{RF}	: RF input
O_{RF}	: RF output
I_A	: Analog input
I_{OS}	: Oscillator input
O_{OS}	: Oscillator output
I	: Digital input
O	: Digital output
I/O	: Digital inout
Is	: Schmitt Trigger input

●RF and Analog pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
30	LNA_P	I	I_{RF}	-	RF antenna input
27	PA_OUT	O	O_{RF}	-	RF antenna output
36	IND1	-	-	-	Pin for VCO inductor
37	IND2	-	-	-	Pin for VCO inductor
33	LP1	-	-	-	Pin for PLL loop filter
38	VB_EXT	-	-	-	Pin for smoothing capacitor for internal bias
25	ATEST1	Hi-Z	O_{RF}	-	Test pin for analog circuit. *Left open when in normal use
26	ATEST2	Hi-Z	O_{RF}	-	Test pin for analog circuit. *Left open when in normal use
24	A_MON	Hi-Z	O_{RF}	-	Analog monitor pin (*1)

[Description]

*1 Analog monitor signal can be configured by [RSSI/TEMP_OUT:B1 0x03] register, no signal assigned as default condition.

PIN DEFINITION(continued)

●SPI interface pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
9	SDO	O/L	O	H or L	SPI data output
13	SDI	I	Is	H or L	SPI data input
11	SCLK	I	Is	P or N	SPI clock input
12	SCEN	I	Is	L	SPI chip enable L: enable H: disable
10	SINTN	O/H	O	L	SPI interrupt output L: interrupt occurs H: -

●DIO interface pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
15	DIO	O/L	I/O	H or L	DIO data input/output
16	DCLK	O/L	O	P or N	DIO clock output

●Regulator pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
2	REG_OUT	-	-	-	Regulator output (typ.1.5V) (Cap 10uF) Note: This pin will output 0V in the sleep state
3	REG_CORE	-	-	-	Monitor pin for power supply to digital core(typ.1.5V) (Cap 10uF)
1	VBG	-	-	-	Pin for decoupling capacitor pin (Cap 0.1uF)
8	REGPDIN	I	I	H	Power down pin for regulator * Fix to “L” for normal use
28	REG_PA	-	-	-	Regulator output for PA block Note: This pin will output 0V in the sleep state

PIN DEFINITION(continued)

●Miscellaneous pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
7	RESETN	I	Is	L	Hardware reset L: Hardware reset enable H: normal operation
4	XIN	I	Ios	P or N	36MHz crystal pin1 *Fixed to GND in case of using external clock
5	XOUT	O	Oos	P or N	36MHzcristal pin2 *Fixed to GND in case of using external clock
6	TCXO	I	I_A	-	External clock (TCXO) input pin. *Fixed to GND in case of using crystal oscillator
20	ANT_SW	O/L	O	H or L or OD	Diversity control signal
21	TRX_SW	O/L	O	H or L or OD	TX-RX switch signal
19	TEST	I	I	H	Test mode input Fixed to “L” for normal use
17	DMON*1	O	O	H	Digital monitor pin Primary function: Clock output (6MHz) Secondary function: PLL_LD output Third function: FIFO trigger output
22	DCNT	O/L	O	H or L or OD	External TX PA control signal
31,35	N.C.	-	-	-	Non connection

[Description]

*1 Function of DMON pin can be selected by following condition. Clock output as a default. However, the clock is not output from DMON pin until TCXO_EN([CLK_SET:B0 0x02(6)]) is enabled, in case of using TCXO.
If clock output is not used, please select another function. Please refer to each register description for more details.
Primary function will have higher priority when multiple function are configured simultaneously.

Configuration of DMON output

Function Name	Configuration register name	Address	Bit position (bit symbol)
CLK output	CLK_SET	B0 0x02	bit4 (CLKOUT_EN)
PLL_LD output	PLL_MON/DIO_SEL	B0 0x69	bit4 (PLL_LD)
FIFO trigger output	CRC_AREA/FIFO_TRG	B0 0x77	bit0 (FIFO_TRG_EN)

●Power supply pins

Pin No	Pin name	Reset state	I/O	Active Level	Detail function
14,18	VDDIO	-/-	PWR	-	Power supply for digital IOs (Input voltage: 1.8V to 3.3V)
40	VDD_REG	-/-	PWR	-	Power supply for regulator input (Input voltage: 1.8V to 3.3V)
29	VDD_PA	-/-	PWR	-	Power supply for PA block (Input voltage: 1.8V to.3.3V, depending on TX mode)
32	VDD_RF	-/-	PWR	-	Power supply for RF blocks (REG_OUT is connected, typ.1.5V)
23	VDD_IF	-/-	PWR	-	Power supply for IF block (REG_OUT is connected, typ.1.5V)
34	VDD_CP	-/-	PWR	-	Power supply for charge pump (REG_OUT is connected, typ.1.5V)
39	VDD_VCO	-/-	PWR	-	Power supply for VCO (REG_OUT is connected, typ.1.5V)
EL	-	-/-	GND	-	GND PAD

●Unused pins

Unused pins treatments are as follows:

Pin Name	Pin number	Recommended treatment
XIN	4	Fixed to GND (When TCXO is used)
XOUT	5	Fixed to GND (When TCXO is used)
TCXO	6	Fixed to GND (When crystal OSC is used)
ATEST1	25	Left OPEN
ATEST2	26	Left OPEN
A_MON	24	Left OPEN
ANT_SW	20	Left OPEN
DMON	17	Left OPEN *1
DCNT	22	Left OPEN

*1 If not using DMON, it is necessary to stop clock out (default output on DMON) by CLKOUT_EN ([CLK_SET:B0 0x02(4)]). Left open with enableing clock out causes the perfoemance down on RX sensitivity.

Note: If input pins are high-impedence state and leave open, excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.

■Electrical Characteristics

●Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Power Supply (I/O) (*1)	V_{DDIO}	Ta=-40 to 85 ˚C GND=0V	-0.3 to +4.6	V
Power Supply (RF) (*2)	V_{DDRF}		-0.3 to +2.0	V
Digital Input Voltage	V_{DIN}		-0.3 to V_{DDIO}+0.3	V
RF Input Voltage	V_{RFIN}		-1.0 to +2.0	V
Analog Input Voltage	V_{AIN}		-0.3 to V_{DDIO}+0.3	V
Analog Input Voltage2 (*3)	V_{AIN2}		-0.3 to V_{DDRF}+0.3	V
TCXO Input Voltage	V_{TCXO}		-0.3 to +1.75	V
Digital Output Voltage	V_{DO}		-0.3 to V_{DDIO}+0.3	V
RF Output Voltage	V_{RFO}		-0.3 to V_{DDRF}+1.9	V
Analog Output Voltage	V_{AO}		-0.3 to V_{DDIO}+0.3	V
Analog Output Voltage2 (*4)	V_{AO2}		-0.3 to V_{DDRF}+0.3	V
Digital Input Current	I_{DI}		-10 to +10	mA
RF Input Current	I_{RF}		-2 to +2	mA
Analog Input Current	I_{AI}		-2 to +2	mA
Analog Input Current2 (*3)	I_{AI2}		-2 to +2	mA
TCXO Input Current	I_{TCXO}		-2 to +2	mA
Digital Output Current	I_{DO}		-8 to +8	mA
RF Output Current	I_{RFO}		-2 to +60	mA
Analog Output Current	I_{AO}		-2 to +2	mA
Analog Output Current2 (*4)	I_{AO2}		-2 to +2	mA
Power Dissipation	P_d	Ta=+25 ˚C	300	mW
Storage Temperature	T_{stg}	-	-55 to +150	˚C

*1 VDD_IO, VDD_REG, VDD_PA pins
*2 VDD_RF, VDD_IF, VDD_VCO, VDD_CP pins
*3 XIN, TCXO pins
*4 XOUT pin

●Recommended operating conditions

Item	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply (I/O)	V_{DDIO}	VDD_IO, VDD_REG pins	1.8	3.3	3.6	V
Power Supply (PA)	V_{DDPA}	VDD_PA pin TX power 1mW mode	1.8	3.3	3.6	V
		VDD_PA pin TX power 10mW mode	2.3	3.3	3.6	V
		VDD_PA pin TX power 20mW mode	2.6	3.3	3.6	V
Power Supply (RF) (*2)	V_{DDRF}	VDD_RF, VDD_IF, VDD_VCO, VDD_CP pins	1.4	1.5	1.6	V
Operating Temperature	T_a	-	-40	+25	+85	˚C
Digital Input Rising Time	T_{IR}	Digital input pins (*1)	-	-	20	ns
Digital Input Falling Time	T_{IF}	Digital Input pins (*1)	-	-	20	ns
Digital Output Loads	C_{DL}	All Digital Output pins	-	-	20	pF
Master Clock1 Accuracy (Crystal)	F_{MCK1}	XIN, XOUT pins	-20ppm (*3)	36	+20ppm (*3)	MHz
Master Clock2 Accuracy (TCXO)	F_{MCK2}	TCXO pin	-20ppm (*3)	36	+20ppm (*3)	MHz
TCXO Input Voltage	V_{TCXO}	DC cut	0.8	-	1.5	Vpp
SPI clock frequency	F_{SCLK}	SCLK pin	0.032	2	16	MHz
SPI clock duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF channel frequency	F_{RF}	LNA_P,PA_OUT pins	863	-	960	MHz

*1 Those pins with symbol I, Is at pin definition section
*2 Use REG_OUT output of this LSI.
*3 It's max.+10ppm and min.-10ppm at 10kbps setting.

[Note]
Electrical characteristics are in the above recommended operating conditions without special instruction.

* Following “Typ” value is not guaranteed value studied variation of IC but typical centre value.

●Power consumption

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Power Consumption (*1)	IDD1	Sleep state (Retaining register values)	-	0.6	3.0(*3)	µA
	IDD2	Idle state	-	1.4	3.0	mA
	IDD3	RF RX state (*4) ML7396A/B	-	15.0	20.0	mA
		RF RX state (*4) ML7396D/E	-	15.8	20.0	mA
	IDD4	RF TX state (1mW) (*4)	-	13.0	20.0	mA
	IDD5	RF TX state (10mW) (*4)	-	24.0	35.0	mA
	IDD6	RF TX state (20mW) (*4)	-	32.0	43.0	mA

*1 Power consumption is sum of current consumption of all power supply pins
*2 “Typ” value is centre value under condition of VDDIO=3.3V, 25 ˚C.
*3 This “Max” value is under condition of 25 ˚C. Other “Max” values are defind under recommended operating coditions.
*4 Current consumption when the data rate is 100kbps and the RF frequency is 920MHz.

●DC characteristics

Item	Symbol	Conditions	Min	Typ (*2)	Max	Unit
Voltage Input High	VIH1	Digital input/inout pins	V_{DDIO} * 0.75	-	V_{DDIO}	V
	VIH2	XIN pin	V_{DDRF} *0.9	-	V_{DDRF}	V
Voltage Input Low	VIL1	Digital input/inout pins	0	-	V_{DDIO} *0.18	V
	VIL2	XIN pin	0	-	V_{DDRF} *0.1	V
Schmitt trigger Threshold High level	VT+	RESETN pin SDI, SCLK, SCEN pins	-	1.2	V_{DDIO} *0.75	V
Schmitt Trigger Threshold Low level	VT-	ESETN pin SDI, SCLK, SCEN pins	V_{DDIO} *0.18	0.8	-	V
Input Leakage Current	IIH1	Digital input/inout pins	-1	-	1	µA
	IIH2	XIN pin	-0.3	-	0.3	µA
	IIL1	Digital input/inout pins	-1	-	1	µA
	IIL2	XIN pin	-0.3	-	0.3	µA
Tri-state Output Leakage Current	IOZH1	Digital inout pins	-1	-	1	µA
	IOZL1	Digital inout pins	-1	-	1	µA
Voltage Output Level H	VOH	IOH=-4mA /-2mA (*1)	V_{DDIO} *0.8	-	V_{DDIO}	V
Voltage Output Level L	VOL	IOL=4mA /2mA (*1)	0	-	0.3	V
Regulator output Voltage	REG_CORE (*2)	Sleep state	0.95	1.3	1.65	V
		Other states	1.40	1.5	1.60	V
Pin Capacitance	CIN	Input pins	-	6	-	pF
	COUT	Output pins	-	9	-	pF
	CRFIO	RF inout pins	-	9	-	pF
	CAI	Analog input pins	-	9	-	pF

*1 DMON pin is IOH=-2mA/2mA
*2 REG_CORE pin and REG_OUT pin. REG_OUT pin becomes 0V when in sleep state.

●RF characteristics

Data Rate : 10kbps/ 20kbps/ 40kbps/ 50kbps/100kbps/ 150kbps/200kbps/ 400kbps
Modulation scheme : GFSK
Channel spacing : 200kHz/400kHz/600kHz
Frequency : Support 750MHz to 1GHz by changing L/C components between IND1 and IND2 pins
Others : Definition point is a antenna connector in the reference circuit.
: RF characteristics out of below table include 400kbps (option) are available as reference data separately.

[TX]

Item	Condition	Min	Typ	Max	Unit
TX Power	20mW (13dBm) mode	9	13	15	dBm
	10mW (10dBm) mode	6	10	12	dBm
	1mW (0dBm) mode	-4	0	2	dBm
Frequency deviation setting range [Fdev] (*1)		-	-	2,250	kHz
920MHz band (920.5MHz to 928.1MHz)					
Occupied bandwidth	n : number of channel	-	-	200 * n	kHz
Power at channel edge	20mW mode (920.5MHz to 922.3MHz)	-	-	-7	dBm
	10mW mode	-	-	-10	dBm
	1mW mode	-	-	-20	dBm
Adjacent Channel Power	20mW mode ±1ch, bandwidth 200kHz)	-	-33	-15	dBm
	10mW mode +/-1ch bandwidth: 200kHz	-	-39	-18	dBm
	1mW mode +/-1ch bandwidth: 200kHz	-	-47	-26	dBm
Spurious emission level (20mW mode)	710MHz or lower, 100kHz band	-	-79	-36	dBm
	Higher than 710MHz to 900MHz, 1MHz band	-	-70	-55	dBm
	Higher than 900MHz to 915MHz, 100kHz band	-	-72	-55	dBm
	Higher than 915MHz to 930MHz, 100kHz band (Excluding within 200 + 100*n kHz above and below the channel frequency, however, within 100 + 100*n kHz above and below for 920.5MHz to 922.3MHz. n is the number of concurrently used channels)	-	-51	-36	dBm
	Higher than 930MHz to 1000MHz, 100kHz band	-	-70	-55	dBm
	Higher than 1000MHz to 1215MHz, 1MHz band	-	-75	-45	dBm
	Higher than 1215MHz, 1MHz band (2nd harmonics or higher)	-	-40	-30	dBm
915MHz band (902MHz to 928MHz)					
6dB bandwidth	Frequency deviation=171kHz	500	-	-	kHz
Power spectrum density	20mW mode, frequency deviation = 171kHz, 3kHz band	-	-	8	dBm
Spurious emission level (20mW mode)	900MHz or lower	-	-65	-56	dBm
	Higher than 960MHz (2nd harmonics or higher)	-	-50	-41	dBm
868MHz band (863MHz to 870MHz) (*2)					
Spurious emission level (10mW mode)	Higher than 1000MHz (2nd harmonics or higher)	-	-35	-30	dBm

*1 While the setting range is described as above, the possible maximum value depends on the RF channel frequency to be used. RF channel frequency ± frequency deviation should not include a multiple of 36MHz (864MHz, 900MHz, 936MHz, and so on).
Example) For 902MHz, 2,000kHz is a possible maximum frequency deviation value.

*2 863.5MHz to 866.2MHz cannot be used. For details, refer section "Programing Channel Frequency."

[RX]

Item	Condition	Min	Typ	Max	Unit
920MHz band (920.5MHz to 928.1MHz)					
Minimum RX sensitivity BER<0.1% ML7396B	50kbps mode (*1)	-	-107	-102	dBm
	100kbps mode (*1)	-	-105	-100	dBm
	200kbps mode (*1)	-	-102	-97	dBm
Minimum RX sensitivity BER<0.1% ML7396D	50kbps mode (*1)	-	-109	-104	dBm
	100kbps mode (*1)	-	-107	-102	dBm
	200kbps mode (*1)	-	-104	-99	dBm
Maximum input level	50kbps mode/100kbps mode/200kbps mode	0	-	-	dBm
Adjacent channel selectivity	50kbps mode	20	35	-	dB
	100kbps mode	20	35	-	dB
	200kbps mode	20	35	-	dB
Alternate channel selectivity	50kbps mode	30	45	-	dB
	100kbps mode	30	45	-	dB
	200kbps mode	30	45	-	dB
Minimum energy detection level [ED value]		-	-	-100	dBm
Energy detection range	Dynamic range	60	70	-	dB
Energy detection accuracy		-6	-	+6	dB
Spurious emission level ARIB T108 measurement condition 915.9MHz~916.9MHz 920.5MHz~929.7MHz	710MHz or lower, 100kHz band	-	<-93	-54	dBm
	Higher than 710MHz to 900MHz, 1MHz band	-	<-83	-55	dBm
	Higher than 900MHz to 915MHz, 100kHz band	-	<-93	-55	dBm
	Higher than 915MHz to 930MHz, 100kHz band	-	-63	-54	dBm
	Higher than 930MHz to 1000MHz, 100kHz band	-	<-93	-55	dBm
	Higher than 1000MHz	-	-57	-47	dBm
915MHz band (902MHz to 928MHz)					
Minimum receiver sensitivity BER<0.1%	100kbps mode (modulation index = 1) (*1)	-	-106	-99	dBm
	150kbps mode (modulation index = 0.5) (*1)	-	-102	-96	dBm
	200kbps mode (modulation index = 1) (*1)	-	-102	-96	dBm
	100kbps mode (frequency shift: 171kHz)	-	-100	-87	dBm
	150kbps mode (frequency shift: 171kHz)	-	-97.5	-84	dBm
	200kbps mode (frequency shift: 171kHz)	-	-96.5	-83	dBm
868MHz band (863MHz to 870MHz) (*2)					
Minimum receiver sensitivity BER<0.1% ML7396E	50kbps mode (*1)	-	-109	-104	dBm
	100kbps mode (*1)	-	-107	-102	dBm
	200kbps mode (*1)	-	-104	-99	dBm
Collateral emission level	1000MHz or lower (local frequency)	-	-63	-57	dBm
	Higher than 1000MHz	-	-57	-47	dBm

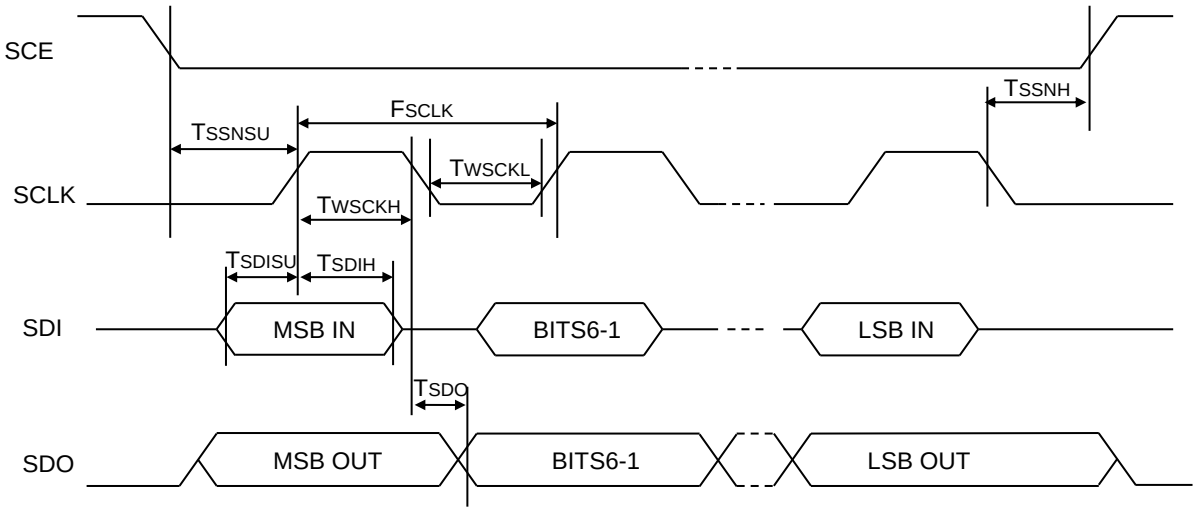
*1 When NBO_SEL([DATA_SET:B0 0x47(7)])=0b0.

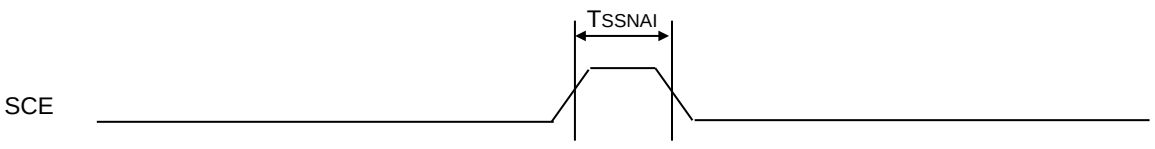
*2 863.5MHz to 866.2MHz cannot be used. For details, refer section "Programing Channel Frequency."

●SPI interface characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	TSSNSU		30	-	-	ns
SCEN input hold time	TSSNH		30	-	-	ns
SCLK high pulse width	TWSCKH		28	-	-	ns
SCLK low pulse width	TWSCKL		28	-	-	ns
SDI input setup time	TSDISU		5	-	-	ns
SDI input hold time	TSDIH		15	-	-	ns
SCEN negate interval	TSSNAI		60	-	-	ns
SDO output delay time	TSDO		-	-	22	ns

[Note]
All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.



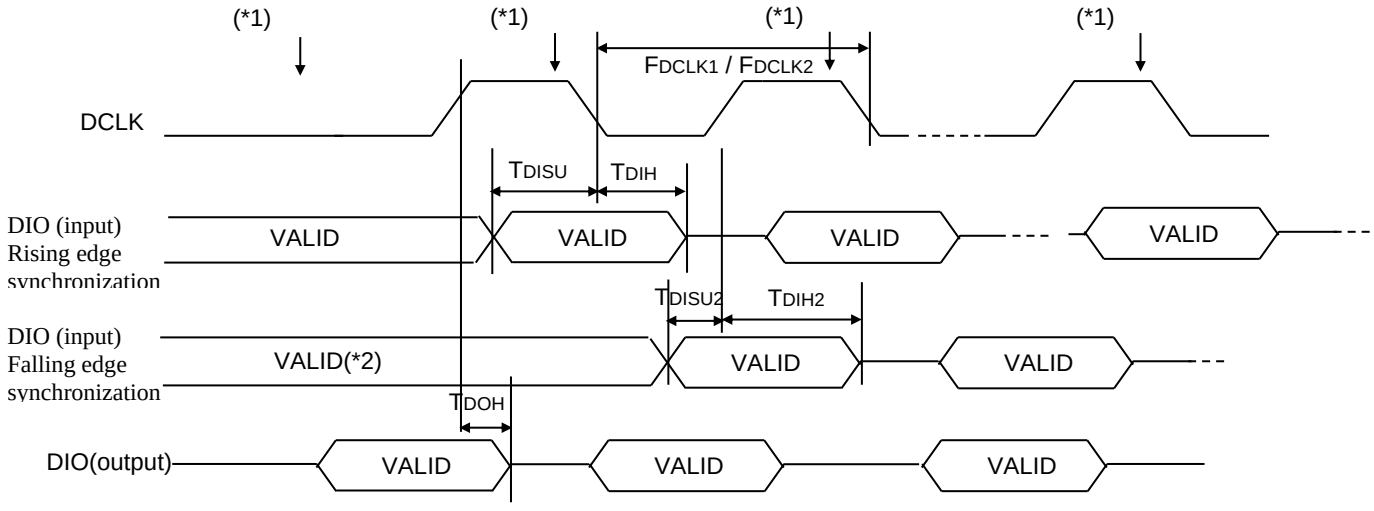


●DIO interface characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
DIO input setup time (Rising edge synchronization)	T_{DISU}	Load capacitance CL=20pF	1	-	-	µs
DIO input setup time (Falling edge synchronization)	T_{DISU2}		0	-	-	µs
DIO input hold time (Rising edge synchronization)	T_{DIH}		0	-	-	ns
DIO input hold time (*3) (Falling edge synchronization)	T_{DIH2}		10 5 2.5	-	-	µs
DIO Output hold time	T_{DOH}		20	-	-	ns
DCLK frequency (*1) (*3) (TX)	F_{DCLK1}		-20ppm	50 100 200	+20ppm	kHz
DCLK frequency (*2) (*3) (RX)	F_{DCLK2}		-4%	50 100 200	+4%	kHz
DCLK output duty ratio (TX)	D_{DCLK}		-	50	-	%
DCLK output duty ratio (RX)	D_{DCLK}		40	-	60	%

*1 DCLK clock frequency in TX mode will be varied depending on the variance of master clock frequency.
*2 DCLK clock frequency in RX mode will be varied by reproduced clock and its jitter.
*3 These characteristics are depend on the setting to the RATE [2:0] ([DATA_SET:B0 0x47(2-0)].
(upper: 50kbps, mid: 100kbps, lower: 200kbps)

[Note]
All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%



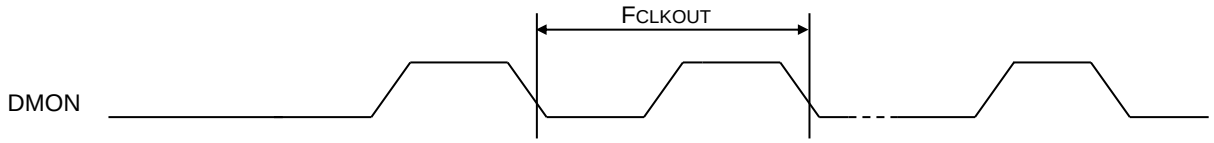
(*1) Timing when ML7396 takes the DIO input.
(*2) For the falling edge synchronization, the first two bits of DIO input have the same data, refer section "TX mode (with DIO mode)"

●Clock output characteristics

Clock output can be controled by [CLK_SET:B0 0x02] register (Initial value:enable), Clock output from DMON pin.

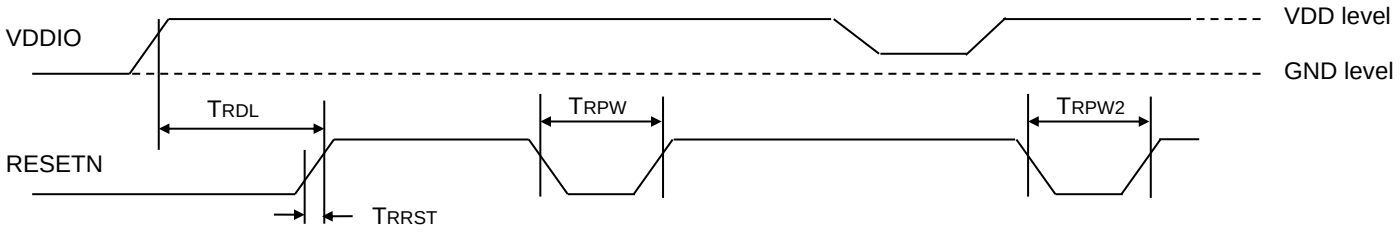
Item	Symbol	Condition		Min	Typ	Max	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20pF	-	0.0088	6	36	MHz
Clock output duty ratio (*1)	D_{CLKOUT}		12MHz	30	-	70	%
			Other than above	48	50	52	%

*1 Duty ratio will be H:L = 1:2 when output frequency is 12MHz.. Refer [CLK_OUT: B0 0x03] register ().



●Reset

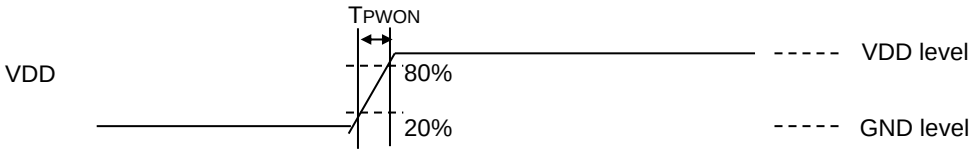
Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN delay time (Power on)	T_{RDL}	All power supply pins (After power on)	1.5	-	-	ms
RESETN pulse period (When starting from VDDIO=0V)	T_{RPW}		200	-	-	ns
RESETN pulse period 2 (*1) (When starting from VDDIO≠0V)	T_{RPW2}	VDD>1.8V	1.5	-	-	ms
RESETN rising period	T_{RRST}		-	-	1	ms



(*1) When starting from VDDIO≠.0V, input a pulse to the RESETN signal after VDDIO exceeds 1.8V.

●Power on sequence

Item	Symbol	Condition	Min	Typ	Max	Unit
Power on time	T_{PWON}	Power on state (All power supply pins)	-	-	5	ms



■Registers

●Register map

It is consist of 3bank, BANK0, BANK1, BANK2. Each BANK has address space of 0x00 to 0x7F, 128 byte in total.
The space shown as gray highlighted part is not implemented in LSI or reserved bits. TX/RX FIFO is implemented in PHY block, those register except for FIFO is implemented in SPI block. The address not exist in the memory map is not accessible. Also, the address is not accessible during the VCO calibration.

In each BANK, there are some registers that can not be access unless give access allowance by TST_ACEN ([BANK_SEL: B0/B1/B2 0x00(7)] =0b1. Such registers are marked with "#" in the following list. The TST_ACEN enable setting is required in the initial setting or test mode setting, but it is recommended to set disable when in normal operation to avoid miss-setting.

For registers whose setting value is specified by the "ML7396Family_InitialRegisterSetting" file, please set the value shown in the file.

: Implemented as functionable register
: Implemented as reserved bits

BANK0

Address	Symbol (# test register)	Bit 7	6	5	4	3	2	1	0	Description
0x00	BANK_SEL									Register access bank selection
0x01	RST_SET									Software reset setting
0x02	CLK_SET									Clock configuration
0x03	CLKOUT									CLKOUT frequency setting
0x04	RATE_SET1									Data rate conversion setting 1
0x05	RATE_SET2									Data rate conversion setting 2
0x06-0x07	Reserved									Reserved
0x08	#ADC_CLK_SET									RSSI ADC clock frequency setting
0x09-0x0a	Reserved									Reserved
0x0b	#OSC_ADJ									Load capacitor adjustment for oscillation circuit
0x0c	#RF_TEST_MODE									TX test pattern setting
0x0d-0x0e	Reserved									Reserved
0x0f	# PHY_STATE									PHY status indication
0x10	#FIFO_BANK									FIFO bank indication
0x11	#PLL_LOCK_DETECT									PLL lock detection configuration
0x12	CCA_IGNORE_LEVEL									ED threshold level setting for excluding CCA judgement
0x13	CCA_LEVEL									CCA threshold level setting
0x14	CCA_ABORT									Timing setting for forced termincation of CCA operation
0x15	CCA_CNTRL									CCA control setting and result indication
0x16	ED_RSLT									ED (Energy Detection) value indication
0x17	IDLE_WAIT_L									IDLE detection period setting during CCA (low 8bits)
0x18	IDLE_WAIT_H									IDLE detection period setting during CCA (high 2bits)
0x19	CCA_PROG_L									IDLE judgement elapsed time indication during CCA (low byte)
0x1a	CCA_PROG_H									IDLE judgement elapsed time indication during CCA (high 2bits)
0x1b	ED_CNTRL									ED detection control setting
0x1c	GAIN_MtoL									Threshold level setting for switching middle gain to low gain
0x1d	GAIN_LtoM									Threshold level setting for switching low gain to middle gain
0x1e	GAIN_HtoM									Gain update setting and threshold level setting for switching high gain to middle gain
0x1f	GAIN_MtoH									Threshold level setting for switching middle gain to high gain
0x20	RSSI_ADJ_M									RSSI offset value setting during middle gain operation
0x21	RSSI_ADJ_L									RSSI offset value setting during low gain operation
0x22	RSSI_STABLE_TIME									Time parameter for RSSI value become stable after gain switch
0x23	RSSI_VAL_ADJ									RSSI scale factor setting for ED value conversion.
0x24	INT_SOURCE_GRP1									FIFO clear setting and interrupt status for INT00 to INT05
0x25	INT_SOURCE_GRP2									Interrupt status for INT08 to INT15
0x26	INT_SOURCE_GRP3									Interrupt status for INT16 to INT23
0x27	INT_SOURCE_GRP4									Interrupt status for INT24 and INT25
0x28	PD_DATA_REQ									Data transmission request status indication
0x29	PD_DATA_IND									Data reception status indication
0x2a	INT_EN_GRP1									Interrupt mask for INT00 to INT05
0x2b	INT_EN_GRP2									Interrupt mask for INT08 to INT15
0x2c	INT_EN_GRP3									Interrupt mask for INT16 to INT23
0x2d	INT_EN_GRP4									Interrupt mask for INT24 and INT25
0x2e	CH_EN_L									RF channel enable setting for low 8ch
0x2f	CH_EN_H									RF channel enable setting for high 8ch
0x30	IF_FREQ_AFC_H									IF frequency setting during AFC operation (high byte)
0x31	IF_FREQ_AFC_L									IF frequency setting during AFC operation (low byte)
0x32	BPF_AFC_ADJ_H									Bandpass filter capacitance adjustment during AFC operation (high 2bits)
0x33	BPF_AFC_ADJ_L									Bandpass filter capacitance adjustment during AFC operation (low byte)
0x34	AFC_CNTRL									AFC control setting
0x35	TX_ALARM_LH									TX FIFO full level setting
0x36	TX_ALARM_HL									TX FIFO empty level setting
0x37	RX_ALARM_LH									RX FIFO full level setting

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x38	RX_ALARM_HL									RX FIFO empty level setting
0x39	PREAMBLE_SET									Preamble pattern setting
0x3a	SFD1_SET1									SFD pattern #1 1st byte setting (max 4byte)
0x3b	SFD1_SET2									SFD pattern #1 2nd byte setting (max 4byte)
0x3c	SFD1_SET3									SFD pattern #1 3rd byte setting (max 4byte)
0x3d	SFD1_SET4									SFD pattern #1 4th byte setting (max 4byte)
0x3e	SFD1_SET1									SFD pattern #2 1st byte setting (max 4byte
0x3f	SFD2_SET2									SFD pattern #2 2nd byte setting (max 4byte)
0x40	SFD2_SET3									SFD pattern #2 3rd byte setting (max 4byte)
0x41	SFD2_SET4									SFD pattern #2 4th byte setting (max 4byte)
0x42	TX_PR_LEN									TX preamble length setting
0x43	RX_PR_LEN/SFD_LEN									RX preamble setting and SFD length setting
0x44	SYNC_CONDITION									Bit error tolerance setting in RX preamble and SFD detection
0x45	PACKET_MODE_SET									Packet configuration
0x46	FEC/CRC_SET									FEC and CRC configuration
0x47	DATA_SET									Data configuration
0x48	CH0_FL									Channel #0 frequency (F-counter) setting (low byte)
0x49	CH0_FM									Channel #0 frequency (F-counter) setting (middle byte)
0x4a	CH0_FH									Channel #0 frequency (F-counter) setting (high 4bits)
0x4b	CH0_NA									Channel #0 frequency (N-counter and A-counter) setting
0x4c	CH_SPACE_L									Channel space setting (low byte)
0x4d	CH_SPACE_H									Channel space setting (high byte)
0x4e	F_DEV_L									GFSK frequency deviation setting (low byte)
0x4f	F_DEV_H									GFSK frequency deviation setting (high byte)
0x50	ACK_TIMER_L									Ack timer setting (low byte)
0x51	ACK_TIMER_H									Ack timer setting (high byte)
0x52	ACK_TIMER_EN									Ack timer control setting
0x53	ACK_FRAME1									Ack Frame Control Field (2bytes) setting (low byte)
0x54	ACK_FRAME2									Ack Frame Control Field (2bytes) setting (high byte)
0x55	AUTO_ACK_SET									Auto_Ack function setting
0x56-x58	Reserved									Reserved
0x59	GFIL00 / FSK_FDEV1									Gaussian filter coefficient setting 1 / FSK 1st frequency deviation setting
0x5a	GFIL01 / FSK_FDEV2									Gaussian filter coefficient setting 2 / FSK 2nd frequency deviation setting
0x5b	GFIL02 / FSK_FDEV3									Gaussian filter coefficient setting 3 / FSK 3rd frequency deviation setting
0x5c	GFIL03 / FSK_FDEV4									Gaussian filter coefficient setting 4 / FSK 4th frequency deviation setting
0x5d	GFIL04									Gaussian filter coefficient setting 5
0x5e	GFIL05									Gaussian filter coefficient setting 6
0x5f	GFIL06									Gaussian filter coefficient setting 7
0x60	GFIL07									Gaussian filter coefficient setting 8
0x61	GFIL08									Gaussian filter coefficient setting 9
0x62	GFIL09									Gaussian filter coefficient setting 10
0x63	GFIL10									Gaussian filter coefficient setting 11
0x64	GFIL11									Gaussian filter coefficient setting 12
0x65	FSK_TIME1									FSK 3rd frequency deviation (FDEV3) hold time setting
0x66	FSK_TIME2									FSK 2nd frequency deviation (FDEV2) hold time setting
0x67	FSK_TIME3									FSK 1st frequency deviation (FDEV1) hold time setting
0x68	FSK_TIME4									FSK no-deviation frequency (carrier frequency) hold time setting

BANK0 (continued)

Address	Symbol (# test register)	Bit 7	6	5	4	3	2	1	0	Description
0x69	PLL_MON/DIO_SEL									PLL lock detection signal output control and DIO mode configuration
0x6a	FAST_TX_SET									TX trigger level setting in FAST_TX mode
0x6b	CH_SET									RF channel setting
0x6c	RF_STATUS									RFstate setting and status indication
0x6d	2DIV_ED_AVG									Average number setting for ED calculation during 2 diversity
0x6e	2DIV_GAIN_CNTRL									Gain control setting during 2 diversity
0x6f	2DIV_SEARCH									2 diversity search mode and search time setting
0x70	2DIV_FAST_LV									ED threshold level setting during 2 diversity FAST mode
0x71	2DIV_CNTRL									2 diversity setting
0x72	2DIV_RSLT									2 diversity resurt indication and forced antenna control setting
0x73	ANT1_ED									Acquired ED value by antenna 1
0x74	ANT2_ED									Acquired ED value by antenna 2
0x75	RF_CNTRL_SET									RF control pin configuration (ANT_SW, TRX_SW,DCNT)
0x76	Reserved									Reserved
0x77	CRC_AREA/FIFO_TRG									CRC calculation field and FIFO trigger setting
0x78	RSSI_MON									RSSI value indication
0x79	TEMP_MON									Temperature indication
0x7a	PN9_SET_L									PN9 initialized status setting / randum number indication (low byte)
0x7b	PN9_SET_H									PN9 initialized status setting / randum number indication (high 1bit) and PN9 enable control
0x7c	RD_ FIFO_LAST									FIFO remaining size or FIFO address indication
0x7d	Reserved									Reserved
0x7e	WR_TX_FIFO									TX FIFO
0x7f	RD_RX_FIFO									RX FIFO

BANK1

Address	Symbol	Bit 7	6	5	4	3	2	1	0	Description
0x00	BANK_SEL									Register access bank selection
0x01	DEMOD_SET									Demodulator setting
0x02	RSSI_ADJ									RSSI value adjustment
0x03	RSSI/TEMP_OUT									RSSI and Temperature data output setting
0x04	PA_ADJ1									PA adjustment 1st setting
0x05	PA_ADJ2									PA adjustment 2nd setting
0x06	PA_ADJ3									PA adjustment 3rd setting
0x07	PA_CNTRL									External PA control and PA mode setting
0x08	SW_OUT/RAMP_ADJ									ANT_SW/TRX_SW configuration and PA ramping up adjustment
0x09	PLL_CP_ADJ									PLL charge pump current adjustment
0x0a	IF_FREQ_H									IF frequency setting (high byte)
0x0b	IF_FREQ_L									IF frequency setting (low byte)
0x0c	IF_FREQ_CCA_H									IF frequency setting during CCA operation (high byte)
0x0d	IF_FREQ_CCA_L									IF frequency setting during CCA operation (low byte)
0x0e	BPF_ADJ_H									Bandpass filter bandwidth adjustment (high 2bits)
0x0f	BPF_ADJ_L									Bandpass filter bandwidth adjustment (low byte)
0x10	BPF_CCA_ADJ_H									Bandpass filter bandwidth adjustment during CCA operation (high 2bits)
0x11	BPF_CCA_ADJ_L									Bandpass filter bandwidth adjustment during CCA operation (low byte)
0x12	RSSI_LPF_ADJ									RSSI lowpass filter adjustment
0x13	PA_REG_FINE_ADJ									PA regulator fine adjustment
0x14	IQ_MAG_ADJ									IF I/Q amplitude balance adjustment
0x15	IQ_PHASE_ADJ									IF I/Q phase balance adjustment
0x16	VCO_CAL_MIN_FL									VCO calibration low limit frequency setting (low byte)

BANK1 (continued)

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x17	VCO_CAL_MIN_FM									VCO calibration low limit frequency setting (middle byte)
0x18	VCO_CAL_MIN_FH									VCO calibration low limit frequency setting (high 4bits)
0x19	VCO_CAL_MAX_N									VCO calibration upper limit frequency setting
0x1a	VCO_CAL_MIN									VCO calibration low limit value indication and setting
0x1b	VCO_CAL_MAX									VCO calibration upper limit value indication and setting
0x1c	VCO_CAL									VCO calibration value indication and setting
0x1d	VCO_CAL_START									VCO calibration execution
0x1e	BPF_ADJ_OFFSET									BPF adjustment offset value indication
0x1f-0x2a	Reserved									Reserved
0x2b	# ID_CODE									ID code indication
0x2c-0x32	Reserved									Reserved
0x33	# PA_REG_ADJ1									PA regulator adjustment (1st setting)
0x34	# PA_REG_ADJ2									PA regulator adjustment (2nd setting)
0x35	# PA_REG_ADJ3									PA regulator adjustment (3rd setting)
0x36-0x39	Reserved									Reserved
0x3a	# PLL_CTRL									PLL setting
0x3b-0x3e	Reserved									Reserved
0x3f	# RX_ON_ADJ2									RX_ON timing adjustment #2
0x40-0x48	Reserved									Reserved
0x49	# LNA_GAIN_ADJ_M									LNA gain adjustment during middle gain operation
0x4a	# LNA_GAIN_ADJ_L									LNA gain adjustment during low gain operation
0x4b-0x4c	Reserved									Reserved
0x4d	# MIX_GAIN_ADJ_H									Mixer gain adjustment during high gain operation
0x4e	# MIX_GAIN_ADJ_M									Mixer gain adjustment during middle gain operation
0x4f	# MIX_GAIN_ADJ_L									Mixer gain adjustment during low gain operation
0x50-0x54	Reserved									Reserved
0x55	#TX_OFF_ADJ1									TX_OFF ramping down adjustment
0x56-0x59	Reserved									Reserved
0x5a	# RSSI_SLOPE_ADJ									RSSI slope adjustment
0x5b-0x7f	Reserved									Reserved

BANK2

Address	Symbol	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access bank selection
0x01-0x11	Reserved									Reserved
0x12	# SYNC_MODE									Bit synchronization mode setting
0x13-0x1d	Reserved									Reserved
0x1e	# PA_ON_ADJ									PA_ON timing adjustment
0x1f	# DATA_IN_ADJ									DATA enable timing adjustment
0x20-0x21	Reserved									Reserved
0x22	# RX_ON_ADJ									RX_ON timing adjustment
0x23	Reserved									Reserved
0x24	# RXD_ADJ									RXD timing adjustment
0x25-0x29	Reserved									Reserved
0x2a	RATE_ADJ1									Demodulator adjustment for optional data rate (low byte)
0x2b	RATE_ADJ2									Demodulator adjustment for optional data rate (high 2 bits)
0x2c	#RAMP_CNTRL									Ramp control enable setting
0x2d-0x5f	Reserved									Reserved
0x60	ADDFILCNTRL									Address filtering function setting
0x61	PANID_L									PANID setting for address filtering function (low byte)
0x62	PANID_H									PANID setting for address filtering function (high byte)
0x63	64ADDR1									64bit address setting for address filtering function (1st byte)
0x64	64ADDR2									64bit address setting for address filtering function (2nd byte)
0x65	64ADDR3									64bit address setting for address filtering function (3rd byte)
0x66	64ADDR4									64bit address setting for address filtering function (4th byte)
0x67	64ADDR5									64bit address setting for address filtering function (5th byte)
0x68	64ADDR6									64bit address setting for address filtering function (6th byte)
0x69	64ADDR7									64bit address setting for address filtering function (7th byte)
0x6a	64ADDR8									64bit address setting for address filtering function (8th byte)
0x6b	SHT_ADDR0_L									Short address #0 setting for address filtering function (low byte)
0x6c	SHT_ADDR0_H									Short address #0 setting for address filtering function (high byte)
0x6d	SHT_ADDR1_L									Short address #1 setting for address filtering function (low byte)
0x6e	SHT_ADDR1_H									Short address #1 setting for address filtering function (high byte)
0x6f	DISCARD_COUNT_L									Discarded packet number indication by address filtering (low byte)
0x70	DISCARD_COUNT_H									Discarded packet number indication by address filtering (high byte)
0x71-0x7f	Reserved									Reserved

●Register BANK0

0x00[BANK_SEL]

Function: Register access bank selection
Address: 0x00 (Bank0)
Default value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	TST_ACEN	Test register access enable (*2) 0: Access disable 1: Access enable	0	R/W
6-2	Reserved	Reserved	000_00	R/W
1-0	BANK[1:0]	BANK selection 0b00: Bank0 access 0b01: Bank1 access 0b10: Bank2 access 0b11: prohibit (*1)	00	R/W

[Note]
*1 When writing 0b11, avilable to return corrent bank by this register. Writing and reading registers are not available except fot this register.*2 Regarding accessible registers by this bit, please refer the “register map” section.

0x01[RST_SET]

Function: Software reset setting
Address: 0x01 (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	RST3_EN	Reset enable setting 0: reset disable 1: reset enable	0	R/W
6	RST2_EN		0	R/W
5	RST1_EN		0	R/W
4	RST0_EN		0	R/W
3	RST_3	PHY function reset (reset execution by setting 0b1)	0	R/W
2	RST_2	RF function reset (reset execution by setting 0b1)	0	R/W
1	RST_1	MODEM function reset (reset execution by setting 0b1)	0	R/W
0	RST_0	SPI function reset (reset execution by setting 0b1) (*1) All register value return to “Default Value”	0	R/W

[Description]
1. Please set enablebit (bit7 to bit4) and execution bit (bit3 to bit0) s at same time.
   After reser, status are not retained and automatically written to 0b0.
2. 2μs after writing to the execution bit (bit3 to bit0), reset operation will complete. However, if executing reset in SLEEP state (while SLEEP_EN ([CLK_SET:B0 0x02(5)]) =0b1), reset will be executed at Clock stabilizzation completion interrupt (INT[00] group1) from SLEEP release and each bit turned to 0b0. If chnaging set value before reset execution, last setting is valid.

The following table shows the software reset operations for each state.

	TX_ON/RX_ON state	SLEEP state	IDLE state (TRX_OFF state)
RST_3:PHY	The FIFO pointer is cleared. The state once transitions to IDLE, and restart the RF with the SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3-0)]) setting state. During CCA or diversity search, it is initialized and restarted. Do not execute RST_3 during transmission.	The FIFO pointer is cleared after SLEEP is released (internal clock is supplied).	The FIFO pointer is cleared. During VCO_CAL, it is initialized and restarted.
RST_2:RF	The PLL circuit is cleared, and the PLL lock is released. Do not execute RST_2 during transmission and reception.	The PLL circuit is cleared after SLEEP is released (internal clock is supplied). (This does not affect the operation.)	The PLL circuit is cleared. (This does not affect the operation.)
RST_1:MODEM	The synchronization is cleared at reception. The continuous wave (CW) is output at transmission. Do not execute RST_1 during transmission and reception.	The modem circuit is cleared after SLEEP is released (internal clock is supplied). (This does not affect the operation.)	The modem circuit is cleared. (This does not affect the operation.)
RST_0:SPI	All registers are initialized.(* 1) RF status will be TRX_OFF, since [RF_STATUS:b0 0x6C] register is initialized.	All registers are initialized after SLEEP is released (internal clock is supplied).(* 1)	All registers are initialized.(* 1)

* 1 : Only TCXO_EN ([CLK_SET:B0 0x02(6)]) is not initialized by the software reset.

0x02[CLK_SET]

Function: Clock configuration
Address: 0x02 (Bank0)
Default Value: 0x9F

Bit	Symbol	Description	Default Value	R/W
7	CLK_Done	Clock stabilization flag 0: stop or starting up status 1: stabilized	1	R
6	TCXO_EN (*2)	TCXO input control 0: disable 1: enable	0	R/W
5	SLEEP_EN (*1)	Sleep mode control 0: Normal mode 1: Sleep mode	0	R/W
4	CLKOUT_EN	CLKOUT output control 0: output disable 1: output enabled	1	R/W
3	CLK3_EN	RF function clock control 0: clock stop 1: clock enable	1	R/W
2	CLK2_EN	TX function (MOD) clock control 0: clock stop 1: clock enable	1	R/W
1	CLK1_EN	RX function (DEMOD) clock control 0: clock stop 1: clock enable	1	R/W
0	CLK0_EN	PHY function clock control 0: clock stop 1: clock enabled	1	R/W

[Description]

1. SPI access will be available while CLK_Done=0b0, but RF operation bit must be done after CLK_Done=0b1. Do not access the BANK1 registers during VCO calibration.

[Note]

*1: In case of using TCXO, set TCXO_EN= 0b1.
In case of using Sleep mode (SLEEP_EN=0b1), CLK*_EN(bit 0 to bit3) must NOT be set to 0b0.
(ML7396 can not enter sleep mode withoug clock.)

*2: In case of using TCXO, this bit must be programmed first. If other resisters are set before programming this bit, values set to other resisters are not valid.

0x03[CLK_OUT]

Function: CLKOUT frequency setting
Address: 0x03 (Bank0)
Default Value: 0x04

Bit	Symbol	Description	Default Value	R/W
7-0	CLK_DIV	CLKOUT frequency setting	0000_0100	R/W

[Description]
Output clock frequency from DMON pin (#17) can be configured by table shown below.
It is available when CLKOUT_EN ([CLK_SET:B0 0x02(4)])=0b1.

Register value	Output frequency
0x00	36 MHz
0x01	18 MHz
0x02	12 MHz (*1)
0x03	9 MHz
0x04	6 MHz (Default Value)
0x05	4.5 MHz
0x06	3.6 MHz
0x07	1.2 MHz
0x08	600 kHz
0x09	246.5 kHz

Following formula is applied after 0x09 setting.

Output frequency = 36/ (16* [set value]+2) (MHz)

For example (value=0x09)
36 / (16 * 9+2) = 0.2465 MHz

[Note]
*1 Duty ratio will be High:Low = 1:2 when output frequency is 12MHz.

0x04[RATE_SET1]

Function: Data rate conversion setting 1
Address: 0x04 (Bank0)
Default value: 0x00

Bit	Register Name	Description	Default Value	R/W
7-0	RATE_SET1	Data rate multiplier setting	0000_0000	R/W

[Detail description]
Combined with [RATE_SET2:B0 0x05] register, any data rate can be programmed.
10kbps, 20kbps, 40kbps, or 150kbps are set by these registers. For details of the data rate conversion, please refer the [RATE_SET2:B0 0x05] register.
50kbps, 100kbps, 200kbps and 400kbps are set by RATE[2:0] ([DATA_SET:B0 0x47(2-0)].
If lower data rate than 50kbps is used, this register and [RATE_SET2:B0 0x05] register are set after VCO calibration.

0x05[RATE_SET2]

Function: Data rate conversion setting 2
Address: 0x05 (Bank0)
Default value: 0x00

Bit	Register Name	Description	Default Value	R/W
7-0	RATE_SET2	Data rate divisor setting	0000_0000	R/W

[Description]
Combined with [RATE_SET1:B0 0x04] register, any data rate can be programmed.
10kbps, 20kbps, 40kbps, or 150kbps are set by these registers. For details of the data rate conversion, please refer the [RATE_SET2:B0 0x05] register.
50kbps, 100kbps, 200kbps and 400kbps are set by RATE[2:0] ([DATA_SET:B0 0x47(2-0)].

●Data rate conversion
Use this function to set a data rate that is not supported by RATE[2:0] ([DATA_SET:B0 0x47(2-0)].

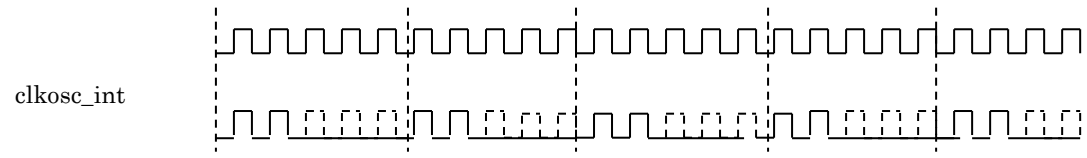
The data rate is defined in the following formula.

Data rate = (RATE[2:0] set) * (RATE_SET1+1) / (RATE_SET2+1) (RATE_SET2 > RATE_SET1)

[Example]
When set data rate to 32.768kbps, it is 50kbps multiplied by 40/61.
Setting values = RATE[2:0]=0b000, [RATE_SET1:B0 0x04]= 0x27, [RATE_SET2:B0 0x05]= 0x3C
The resulting transmission rate is 32.787kbps (50 * 40 / 61).
The “data rate error” is 1.00058 (0.058%) (32.787 /32.768).

[Note] Jitter will be generated because it is not controlled by PLL. Maximum jitter = RATA_SET2 period - RATE_SET1 period.

[Example of time chart]
[RATE_SET1:B0 0x04]=0x01
[RATE_SET2:B0 0x05]=0x04



Place the “RATE_SET2” counter for clock delivery up to the count value of “RATE_SET1+1”.

Example: Set to 150kbps
RATE[2:0] ([DATA_SET:B0 0x47(2:0)])=0b010 (200kbps)
[RATE_SET1:B0 0x04]=0x02
[RATE_SET2:B0 0x05]=0x03

Example: Set to 40kbps
RATE[2:0] ([DATA_SET:B0 0x47(2:0)])=0b010 (200kbps)
[RATE_SET1:B0 0x04]=0x00
[RATE_SET2:B0 0x05]=0x04

Example: Set to 20kbps
RATE[2:0] ([DATA_SET:B0 0x47(2:0)])=0b010 (200kbps)
[RATE_SET1:B0 0x04]=0x00
[RATE_SET2:B0 0x05]=0x09

0x08[ADC_CLK_SET]

Function: RSSI ADC clock frequency setting
Address: 0x08
Default Value 0xC3

Bit	Symbol	Description	Default Value	R/W
7-6	OSC_W_SET	Clock stabilization waiting time setting 00: 2ms 01: 1.3ms 10: 1ms 11: 0.6ms	11	R/W
5	Reserved	Reserved	0	
4	ADC_CLK_SET	RSSI ADC clock setting 0: 1.8 MHz 1: 2.0 MHz	0	R/W
3-0	Reserved	Reserved	0011	R/W

0x09-0A[Reserved]

0x0B[OSC_ADJ]

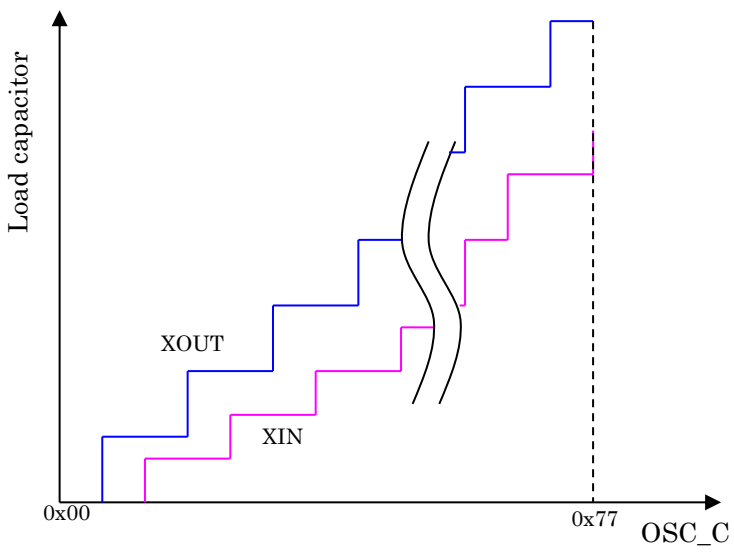
Function: Load capacitor adjustment for oscillation circuit
Address: 0x0b (Bank0)
Default Value: 0x40

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-0	OSC_C	Load capacitor adjustment (*1) (setting range : 0x00 to 0x77)	100_000	R/W

[Description]

1. Adjusting load capacitance of XIN pin (#4) and XOUT pin (#5).

*1 Adjusted step is 0.02pF/2step at XIN pin, 0.03pF/2step at XOUT pin.



0x0C[RF_TEST_MODE]

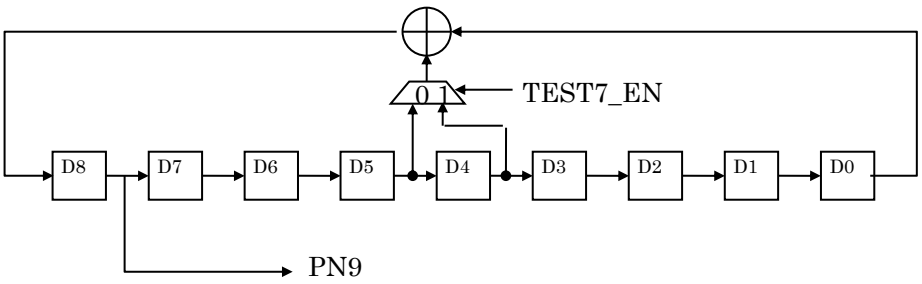
Function: TX test pattern setting
Address: 0x0c (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	TEST7	PN9 output for bit error rate meter (valid if set to 0b1) *1	0	R/W
6	TEST6	Reserved	0	R/W
5	TEST5	CW output (valid if set to 0b1)	0	R/W
4	TEST4	"01" pattern output (valid if set to 0b1)	0	R/W
3	TEST3	All "0" output (valid by if set to 0b1)	0	R/W
2	TEST2	All "1" output (valid if set to 0b1)	0	R/W
1	TEST1	PN9 output (valid if set to 0b1)	0	R/W
0	TEST_EN	Test mode enable control 0: disable test mode 1: enable test mode	0	R/W

[Description]

1. During normal operation, all bits have to be 0b0.
2. More than one bits are enabled at the same time, lowest bit is valid.
3. Data rate will be configured by the RATE[2:0] ([DATA_SET:B0 0x47(2-0)]).

*1 PN9 output sequence implemented in most of bit error rate meter is different from the one defined by IEEE. If TEST7=0b1, D4 output is input to EX_OR as following polynomial.



0x0D-0E[Reserved]

0x0F[PHY_STATE]

Function: PHY status indication / Preamble detection status indication (for debugging)
Address: 0x0f (Bank0)
Default value: 0xC0

Bit	Register name	Description	Default Value	R/W
7-6	Reserved	Reserved	11	R/W
5	PB_DET	Preamble detection status indication (*1) 0: not detected 1: detected	0	R/W
4-0	PHY_STATE	PHY status indication (*2)	0_0000	R/W

[Description]

*1 Indicating preamble detection status. The preamble detection status shows 0b1 when it matches or does not match all of the PR[7:0] ([PREAMBLE_SET:B0 0x39(7-0)] setting independent of PR_SYNC[3:0] ([SYNC_CONDITION:B0 0x44(3-0)]) setting.

*2 Indicating PHY state machine. This bit is linked with [RF_STATUS:B0 0x6C] register.

PHY_STATE[4:0]	State name	Description	Remarks
0x00	IDLE	Transmission/reception instruction wait state	After executing TRX_OFF and PHY reset
0x01	TX_TXD	Transmitted data wait state	
0x02	TX_PB	Preamble transmission state	
0x03	TX_SFD	SFD transmission state	
0x04	TX_LEN	Length transmission state	
0x05	TX_DATA	DATA transmission state	
0x06	TX_CRC	CRC transmission state	
0x07	TX_WAIT	Transmission wait state	after packet transmission completion
0x08	TX_OFF	Transmission OFF state	
0x09	TX_DIO	DIO transmission state	
0x0B	TX_MOD	Transmission completion wait state	
0x11	RX_RXD	SFD detection wait state	
0x14	RX_LEN	Length reception state	
0x15	RX_DATA	DATA reception state	
0x16	RX_CRC	CRC reception state	
0x17	RX_RXD2	Reception wait state	after packet reception completion
0x18	RX_OFF	Reception OFF state	
0x19	RX_DIO	DIO reception state	
0x1C	RX_DIV1	Diversity search state 1	
0x1D	RX_DIV2	Diversity search state 2	
0x1F	RX_FEC_WAIT	FEC process wait state	

[Note] PHY_STATE is provided only for debugging. Do not use it for other purposes.
If a PHY_STATE value other than above is read in debugging opperation, please try to read it again.

0x10[FIFO_BANK]

Function: FIFO bank indication
Address: 0x10 (Bank0)
Default value: 0x00

Bit	Register name	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R
3	SPI_TX_B	SPI-FIFO write bank monitor 0: FIFO0 1: FIFO1	0	R
2	SPI_RX_B	SPI-FIFO read bank monitor 0: FIFO0 1: FIFO1	0	R
1	PHY_TX_B	PHY-FIFO write bank monitor 0: FIFO0 1: FIFO1	0	R
0	PHY_RX_B	PHY-FIFO read bank monitor 0: FIFO0 1: FIFO1	0	R

[Description]
These bits transit from “0” (FIFO bank0) to “1” (FIFO bank1) or from “1” (FIFO bank1) to “0” (FIFO bank0) under the following conditions. The default value is always “0” (FIFO bank0).
SPI_TX_B ...When SPI completes writing a whole length of transmitting data to a FIFO
SPI_RX_B ...When SPI completes reading a whole length of received data from a FIFO
PHY_TX_B ...When PHY completes writing a whole length of received data to a FIFO
PHY_RX_B ...When PHY starts reading a whole length of transmitting data from a FIFO

0x11[PLL_LOCK_DETECT]

Function: PLL lock detection configuration
Address: 0x11 (Bank0)
Default Value: 0x83

Bit	Symbol	Description	Default Value	R/W
7	PLL_LD_EN (*1)	PLL unlock detection enable control 0: disable PLL unlock detection 1: enable PLL unlock detection	1	R/W
6-0	TIM_PLL_LD[6:0]	PLL unlock detection time Detection time = [set value] * 8.88 μs + 8.88μs Default value = 3 * 8.88 + 8.88 = 35.52μs	000_0011	R/W

[Description]
*1: After PLL unlock detection, ML7396 performs following action;
During RX_ON state: Generates INT[25] (group4), and keep RX_ON state.
During TX_ON state: Generates INT[25] (group4), and move to IDLE state.

[Note]
1. When move to IDLE state due to PLL unlock detection, please execute PHY reset ([RST_SET:B0 0x01]=0x88), and clear INT[25] ([INT_SOOURCE_GRP4:B0 0x27(1)) before transmitting next data.
2. Wait more than 5μs from PLL unlock detection before accessing the [RF_STATUS:B0 0x6C] register.

0x12[CCA_IGNORE_LEVEL]

Function: ED threshold level setting for excluding CCA judgement
Address: 0x12 (Bank0)
Default Value: 0xFE

Bit	Symbol	Description	Default Value	R/W
7-0	IGNORE_LV[7:0]	ED threshold level setting for excluding CCA running average.	1111_1110	R/W

[Description]

1. For details operation of CCA, please refer to the “CCA (Clear Channel Assesment)”.
2. If an acquired ED value exceeding this threshold, is excluded from averaging process defined by ED_AVG[2:0] ([ED_CNTRL:B0 0x1b(2-0)]). And CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) indicates 0b11 (evaluation on going).

0x13[CCA_LEVEL]

Function: CCA threshold level setting
Address: 0x13 (Bank0)
Default Value: 0x08

Bit	Symbol	Description	Default Value	R/W
7-0	CCA_TH_LV[7:0]	CCA threshold level setting (setting range: 0 to 255)	0000_1000	R/W

[Description]

1. For details operation of CCA, please refer to the “CCA (Clear Channel Assesment)”.
2. If an acquired ED value exceeding this threshold, CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) indicates 0b01 (carrier detected)

0x14[CCA_ABORT]

Function: Timing setting for forced termination of CCA operation during AUTO_ACK case.
Address: 0x14 (Bank0)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	CCA_ABORT[6:0]	CCA forced termination timing setting (setting range: 0 to 255)	1111_1111	R/W

[Description]

1. Time out function for avoiding in competion of Auto_Ack transmission by carrier detection.
   For details operation of CCA, please refer to the “CCA (Clear Channel Assesment)”.
2. If CCA operation period becomes the value defined by “[set value] * 17.8μs, IDLE detection is terminated, and packet data will be aborted, RF state becomes TRX_OFF state.
   (Note: time length given above is in case of ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)]=0b0 (1.8MHz: default). If ADC_CLK is configured 2MHz, the termination time will be “[set value] * 16μs.)

0x15[CCA_CNTRL]

Function: CCA control setting and result indication
Address: 0x15 (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	CCA_AUTO_EN	CCA execution setting during AUTO_ACK mode 0: disable 1: enable	0	R/W
6	CCA_LOOP_STOP	CCA continuous mode termination setting 0: not terminates CCA continuous mode 1: terminates CCA continuous mode	0	R/W
5	CCA_LOOP_START	CCA continuous mode enable setting (*1) 0: disable 1: enable	0	R/W
4	CCA_EN	CCA execution setting (*2) 0: not perform CCA 1: perform CCA	0	R/W
3	CCA_IDLE_EN	CCA idle detection mode enable setting 0: disable 1: enable	0	R/W
2	CCA_DONE	CCA complete flag (*4) 0: CCA is busy (or not started) 1: CCA completed	0	R
1-0	CCA_RSLT[1:0]	CCA result indication (*3) 0b11: CCA evaluation on-going (ED value excluding CCA judgement acquisition) 0b10: CCA evaluation on-going (Evaluating IDLE) 0b01: carrier detected 0b00: no carrier	00	R

[Description]

1. For details operation of CCA, please refer to the “CCA (Clear Channel Assesment)”.

*1 CCA operation will continue until terminated by CCA_LOOP_STOP bit.
*2 After completion of CCA, reset to 0b0 automatically.
*3 CCA_RSLT[1:0] are not cleared automatically. Every time CCA detects carrier, 0b00 should be set to clear these bits. Only 0b00 are valid for writing.
*4 CCA_DONE is linked with INT08 [INT_SOURCE_GRP2:B0 0x25(0)]).
CCA_DONE transitions to 0b1 (CCA completed) only when CCA_RSLT[1:0]=0b00 or 0b01.

[Note]

1. If CCA_AUTO_EN=0b1, do not write access to the [RF_STATUS:B0 0x6C] register, until it becomes 0x99 after CCAno carrier detection. (prohibited the acceess during state transition)

0x16[ED_RSLT]

Function: ED (Energy Detection) value indication
Address: 0x16 (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ED_Value[7:0]	ED value	0000_0000	R

[Description]

1. For details of ED value acqiosition operation, please refer to the “Energy Detection value (ED value) function”.
2. ED vlaue will be updated when RF state move to RX_ON state. By setting SET_TRX[3:0] ([RF_STATUS: B0 0x6C (3-0)])=0b0110, RF status move to RX_ON state.

0x17[IDLE_WAIT_L]

Function: IDLE detection period setting during CCA (low byte)
Address: 0x17 (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	IDLE_WAIT[7:0]	IDLE judgement maximum wait time setting (low byte)	0000_0000	R/W

[Description]

1. In CCA IDLE judjement, it is used for detecting long IDLE (no carrier) period. Combined together with [IDLE_WAIT_H:B0 0x18] register.
   For details operation of CCA, please refer to “CCA (Clear Channel Assesment)”.
2. IDLE detection period is programmed as follows.
   ED value averaging period (default 8 times =142.4μs) + (“IDLE_WAIT[9:0]” * 17.8) [μs]
   (Note: the period given above is in case of ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)]=0b0 (1.8MHz: default).
   If ADC_CLK is configured 2MHz, it becomes
   ED value averaging period (default 8 times =128μs) + (“IDLE_WAIT[9:0]” * 16) [μs]

0x18[IDLE_WAIT_H]

Function: IDLE detection period setting during CCA (high 2bits)
Address: 0x18 (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	IDLE_WAIT[9:8]	IDLE judgement maximum wait time setting (high 2bits)	00	R/W

[Description]

1. Regaring this register, please refer the[IDLE_WAIT_L:B0 0x17] register.

0x19[CCA_PROG_L]

Function: IDLE judgement elapsed time indication during CCA (low byte)
Address: 0x19 (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	CCA_PROG [7:0]	IDLE judgement elapsed time indication (low byte)	0000_0000	R

[Description]

1. Indicating elapsed time of CCA IDLE detection. Combined together with [CCA_PROG_H:B0 0x1A] register. For details operation of CCA, please refer to "CCA (Clear Channel Assesment)".
2. The elapsed time is indicated as follows;
   ED value averaging period (default 8 times =142.4μs) + ("IDLE_WAIT[9:0]" * 17.8) [μs]
   (Note: the period given above is in case of ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)]=0b0 (1.8MHz: default).
   If ADC_CLK is configured 2MHz, it becomes
   ED value averaging period (default 8 times =128μs) + ("IDLE_WAIT[9:0]" * 16) [μs]

0x1A[CCA_PROG_H]

Function: IDLE judgement elapsed time indication during CCA (high 2bits)
Address: 0x1a (Bank0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R
1-0	CCA_PROG[9:8]	IDLE judgement elapsed time indication (high 2bits)	00	R

[Description]

1. Regarding this register, please refer to the [CCA_PROG_L:B0 0x09] register.

0x1B[ED_CNTRL]

Function: ED detection control setting
Address: 0x1b (Bank0)
Default Value: 0x83

Bit	Symbol	Description	Default Value	R/W
7	ED_CALC_EN	ED value calculation enable setting 0: disable ED value calculation 1: enable ED value calculation	1	R/W
6-5	Reserved	Reserved	00	R/W
4	ED_DONE	ED value calculation completion flag 0: calculation on going 1: calculation completion	0	R
3	Reserved	Reserved	0	R/W
2-0	ED_AVG[2:0]	ED value calculation average times setting (*1)	011	R/W

[Description]

1. For details operation of ED value acqiosition, please refer to the “Energy Detection value (ED value) function”.

*1 The averaging number of times are shown in below table.

ED_AVG[2:0]	averaging times
0b000	1
0b001	2
0b010	4
0b011 (Default Value)	8
0b100	15
0b101	16
Otherwise	8

[Note] ED_AVG[2:0] must be set when ED value calculation stop. (TRX_OFF state or TX_ON state or ED_CALC_EN=0b0).

0x1C[GAIN_MtoL]

Function: Threshold level setting for switching middle gain to low gain
Address: 0x1c (Bank0)
Default Value: 0x1E

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_ML[5:0]	Gain switching threshold level (middle gain to low gain)	01_1110	R/W

[Description]

1. For details, please refer to the “Energy Detection value (ED value) adjustment”.

[Note]

1. Please use the value specified in the “Initial register setting” file.
2. This register value and [GC_TRIM_LtoM:B0 0x1D] value have to be;
   GC_TRM_ML[5:0] > GC_TRIM_LM[5:0]

0x1D[GAIN_LtoM]

Function: Threshold level setting for switching low gain to middle gain
Address: 0x1d (Bank0)
Default Value: 0x03

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_LM[5:0]	Gain switching threshold level (low gain to middle gain)	00_0011	R/W

[Description]
1. For details, please refer to the “Energy Detection value (ED value) adjustment”.

[Note]
1. Please use the value specified in the “Initial register setting” file.
2. This register value and [GC_TRIM_MtoL:B0 0x1C] value have to be;
   GC_TRMML[5:0] > GC_TRIM_LM[5:0]

0x1E[GAIN_HtoM]

Function: Gain update setting and threshold level setting for switching high gain to middle gain
Address: 0x1e (Bank0)
Default Value: 0x9E

Bit	Symbol	Description	Default Value	R/W
7	GC_FIX_EN	Gain switching setting (*1) 0: constantly updating 1: after synchronization established, gain will be fixed.	1	R/W
6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_HM[5:0]	Gain switching threshold level (high gain to middle gain)	1_1110	R/W

[Description]
1. For details, please refer to the “Energy Detection value (ED value) adjustment”.

[Note]
1. Please use the value specified in the “Initial register setting” file.
2. This register value and [GC_TRIM_MtoH:B0 0x1F] value have to be;
   GC_TRIM_HM[5:0] > GC_TRIM_MH[5:0]

*1 During BER measurement, GC_FIX_EN has to be 0b0.

0x1F[GAIN_MtoH]

Function: Threshold level setting for switching middle gain to high gain
Address: 0x1f (Banl0)
Default Value: 0x03

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	GC_TRIM_MH[5:0]	Threshold level for gain control	00_0011	R/W

[Description]
1. For details, please refer to the “Energy Detection value (ED value) adjustment”.

[Note]
1. Please use the value specified in the “Initial register setting” file.
2. This register value and [GC_TRIM_HtoM:B0 0x1E] value have to be;
   GC_TRIM_HM[5:0] > GC_TRIM_MH[5:0]

0x20[RSSI_ADJ_M]

Function: RSSI offset value setting during middle gain operation
Address: 0x20 (Bank0)
Default Value: 0x19

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	RSSI_OFFSET_M[5:0]	RSSI offset value during middle gain operation	01_1001	R/W

[Description]
1. For details, please refer to the “Energy Detection (ED) value adjustment”.

[Note]
1. Please use the value specified in the “Initial register setting” file

0x21[RSSI_ADJ_L]

Function: RSSI offset value setting during low gain operation
Address: 0x21 (Bank0)
Default Value: 0x37

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	RSSI_OFFSET_L[5:0]	RSSI offset value during low gain operation	11_0111	R/W

[Description]
1. For details, please refer to “Energy Detection value (ED value) adjustment”.

[Note]
1. Please use the value specified in the “Initial register setting” file

0x22[RSSI_STABLE_TIME]

Function: RSSI stabilization wait time setting
Address: 0x22 (Bank0)
Default Value: 0x03

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-4	AD_MASK_SET[1:0]	RSSI convergence wait time setting (*2)	00	R/W
3-0	RSSI_STABLE[3:0]	RSSI stabilization wait time after gain switching. (setting range: 1 to 15) (*1)	0011	R/W

[Description]

*1 This period is RSSI stabilization time after gain switching. During this period, RSSI value is not used for ED value calculation.
Wait time = ([set value] + 1) * ADC clock setting (default 17.8μs[at 1.8MHz], 16μs[at 2MHz])
This function is valid during ED value acquisition and diversity operation, but invalid during CCA operation.

*2 Waiting time until RSSI value becomes stable. During this period, not executing the next gain switching.
Wait time = ([Set value] + 2) * ADC clock setting (default 17.8μs[at 1.8MHz], 16μs[at 2MHz]).

[Note]

1. Do not set 0x00 to this register. Please use the value specified in the “Initial register setting” file

0x23[RSSI_VAL_ADJ]

Function: RSSI scale factor setting for ED value conversion.
Address: 0x23 (Bank0)
Default Value: 0x50

Bit	Symbol	Description	Default Value	R/W
7-4	RSSI_VAL_M[3:0]	RSSI multiply value setting (setting range: 0 to 15) (Default Value x5)	0101	R/W
3	RSSI_VAL_D3	RSSI division value 1/8 setting (applied when set to 0b1)	0	R/W
2	RSSI_VAL_D2	RSSI division value 1/4 setting (applied when set to 0b1)	0	R/W
1	RSSI_VAL_D1	RSSI division value 1/2 setting (applied when set to 0b1)	0	R/W
0	RSSI_VAL_D0	RSSI division value 1/1 setting (applied when set to 0b1)	0	R/W

[Note]

1. For details, please refer to “Energy Detection value (ED value) adjustment”.
2. Please use the value specified in the “Initial register setting” file
3. Division setting can be selected one bit from bit3 to bit0. If multiple bits are set, only MSB is valid.
(i.e. If both bit3and bit 1 are set to 0b1, 1/8 setting is valid.)
4. If both multiplication and division are set, complex calculation is performed However if bit[3-0]=0b0000, 1/1 will be set.
(i.e. If bit[7:4]=0b0100 (*4) and bit 1=0b1(1/2) are set, result will be *2.)
5. If 0x00 in written to this register, *1 setting

0x24[INT_SOURCE_GRP1]

Function: FIFO clear setting and interrupt status for INT00 to INT05
Address: 0x24 (Bank 0)
Default Value: 0x01

Bit	Symbol	Description	Default Value	R/W
7	FIFO_CLR1	FIFO bank1 clear in RX (*1)0: no data in FIFO (execute FIFO clear) 1: FIFO has data to clear	0	R/W
6	FIFO_CLR0	FIFO bank0 clear in RX (*2)0: no data in FIFO (execute FIFO clear)1: FIFO has data to clear	0	R/W
5	INT[05]	FIFO-Full interrupt (*3) 0: no interrupt 1: interrupt	0	R/W
4	INT[04]	FIFO-Empty interrupt (*4) 0: no interrupt 1: interrupt	0	R/W
3	INT[03]	Packet discard completion interrupt in address filtering function (*5) 0: no interrupt 1: interrupt	0	R/W
2	INT[02]	VCO calibration completion interrupt 0: no interrupt 1: interrupt	0	R/W
1	INT[01]	Reserved	0	R/W
0	INT[00]	Clock stabilization completion interrupt 0: no interrupt 1: interrupt	1	R/W

[Description]

*1 If executing this bit (set 0b0), FIFO bank1 will be cleared. Next received data will be written into FIFO bank1, and stored data can be read via SPI interface. If reading start, this bit becomes '0b1'. By writing '0b0', it will be cleared.

*2 If executing this bit (set 0b0), FIFO bank0 will be cleared. Next received data will be written into FIFO bank0, and stored data can be read by SPI interface. If reading start, this bit becomes '0b1'. By writing '0b0', it will be cleared.

*3 Interrupt will generate, if FIFO usage becomes the threshold defined by [TX_ALARM_LH:B0 0x35] register in TX or [RX_ALARM_LH:B0 0x37] register in RX.

*4 Interrupt will generate if FIFO usage is below threshold defined by [TX_ALARM_HL:B0 0x36] register in TX or [RX_ALARM_HL:B0 0x38] register in RX.
If once FIFO usage exceeds FIFO-Full threshold and then data reception is completed, this interrupt will be generated just before generating FIFO * RX completion interrupt (INT[18] or INT[19]).

*5 Interrupt will generate after received packet abort completion by Address filtering function.

[Note]

1. Regardless of [INT_EN_GRP1:B0 0x2A] register setting, this register value reflect internal status. For writing only 0b0 is valid, writing 0b1 is ignored.
2. Bit7(FIFO_CLR1) and bit6(FIFO_CLR0) are independent from [INT_EN_GRP1:B0 0x2A] register. Interruption is not generated.
3. Do not clear FIFO (FIFO_CLR0/1=0b0) if FIFO read process is completed properly. When receiving 2 packet and CRC error interrupt (INT[20]/[21] group3) occurs, do not clear FIFO and RX data with CRC error should be read out from FIFO.
4. If one of unmasked interrupt event occurs, SINTN (Pin #10) keeps output "Low".

0x25[INT_SOURCE_GRP2]

Function: Interrupt status for INT8 to INT15
Address: 0x25 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	INT[15]	TX FIFO access error interrupt (*1) 0: no interrupt 1: interrupt	0	R/W
6	INT[14]	RX FIFO access error interrupt (*2) 0: no interrupt 1: interrupt	0	R/W
5	INT[13]	TX Length error interrupt (*3) 0: no interrupt 1: interrupt	0	R/W
4	INT[12]	RX Length error interrupt (*4) 0: no interrupt 1: interrupt	0	R/W
3	INT[11]	SFD detection interrupt (*5) 0: no interrupt 1: interrupt	0	R/W
2	INT[10]	RF state transition completion interrupt (*6) 0: no interrupt 1: interrupt	0	R/W
1	INT[09]	Diversity search completion interrupt 0: no interrupt 1: interrupt	0	R/W
0	INT[08]	CCA completion interrupt 0: no interrupt 1: interrupt	0	R/W

[Description]

*1 During TX, if FIFO overrun (writing data size exceeds FIFO size (256byte)), under run (FIFO has no data to be transmitted), or the 3rd packed data is written to a FIFO when the transmitting data remain in both FIFO0 and FIFO1, interrupt will generate

*2 During RX, if FIFO overrun (PHY writes received data exceeding FIFO size (256byte)), under run (reading from empty FIFO, or receiving the 3rd packed when the receiving data remain in both FIFO0 and FIFO1, interrupt will generate.

*3 Interrupt will generate, if setting more than 128(byte) to the TX Length field. This interrupt will be valid only if IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) = 0b0 (IEEE802.15.4d).

*4 Interrupt will generate, if the RX Length field has more than 128 (byte). This interrupt will be valid only if EEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) = 0b0 (IEEE802.15.4d).

*5 Interrupt will generate, when receiving preamble data and SFD data that include smaller amount of error bits defined by [SYNC_CONDITION:B0 0x44] register.

*6 Interrupt will generate when state transition specified by SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3-0)] setting), are completed.

[Note]

RF state transition completion interrupt (hereafter INT[10]) might occur at unwilling timing when FEC operation, Diversity operation and CCA operation during diversity. And INT[10] might not occur after unmasking INT[10] in some case.

1. If INT[10] occurs before [RF_STATUS:B0 0x6C] register setting, please clear INT[10].
2. If INT[10] will not occur after [RF_STATUS:B0 0x6C] register setting, please confirm the RF state by reading GET_TRX[3:0] ([RF_STATUS:B0 0x6C87-4]]), 0b0110 indicates RX_ON, 0b1001 indicates TX_ON and 0b1000 indicates TRX_OFF or Force_TRX_OFF

[Note]

1. Regardless of [INT_EN_GRP2:B0 0x2B] register setting, this register value reflect internal status. For writing only 0b0 is valid, writing 0b1 is ignored.

0x26[INT_SOURCE_GRP3]

Function: Interrupt status for INT16 to INT23
Address: 0x26 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	INT[23]	FIFO1 TX data request accept completion interrupt (*1) 0: no interrupt 1: interrupt	0	R/W
6	INT[22]	FIFO0 TX data request accept completion interrupt (*2) 0: No interrupt 1: Interrupt	0	R/W
5	INT[21]	FIFO1 CRC error interrupt(*3) 0: no interrupt 1: interrupt	0	R/W
4	INT[20]	FIFO0 CRC error interrupt(*4) 0: no interrupt 1: interrupt taken place	0	R/W
3	INT[19]	FIFO1 RX completion interrupt (*5) 0: no interrupt 1: interrupt taken place	0	R/W
2	INT[18]	FIFO0 RX completion interrupt (*6) 0: no interrupt 1: interrupt taken place	0	R/W
1	INT[17]	FIFO1 TX completion interrupt (*7) 0: no interrupt 1: interrupt taken place	0	R/W
0	INT[16]	FOFO0 TX completion interrupt (*8) 0: no interrupt 1: interrupt taken place	0	R/W

[Description]

*1 Interrupt will generate, when a TX Length of transmitted data is written to the FIFO1.
This bit will also be cleared when setting PD_DATA_REQ1 ([PD_DATA_REQ:B0 0x28(5)]) =0b0.

*2 Interrupt will generate when a TX Length of transmitted data is written to the FIFO0.
This bit will also be cleared when setting PD_DATA_REQ0 ([PD_DATA_REQ:B0 0x28(1)]) =0b0..

*3 Interrupt will generate when received data written to the FIFO1 has CRC error.
This bit will also be cleared when setting CRC_RSLT1 ([PD_DATA_IND:B0 0x29(4)]) =0b0
If bit synchronization is lost during data reception following SFD field due to drastic RF signal strength change and so on, this interrupt will also generate.

*4 Interrupt will generate when received data written to the FIFO0 has CRC error.
This bit will also be cleared when setting CRC_RSLT0 ([PD_DATA_IND:B0 0x29(0)]) =0b0.
If bit synchronization is lost during data reception following SFD field due to drastic RF signal strength change and so on, this interrupt will also generate.

*5 Interrupt will generate when whole received packet data are written into the FIFO1.
This bit will also be cleared when setting PD_DATA_IND1 ([PD_DATA_IND: B0 0x29(5)]) =0b0.

*6 Interrupt will generate when whole received packet data are written into the FIFO0.
This bit will also be cleared when setting PD_DATA_IND0 ([PD_DATA_IND: B0 0x29(1)]) =0b0.

*7 Interrupt will generate when completing transmission of packet data stored in the FIFO1.
This bit will also be cleared when setting PD_DATA_CFM1 ([PD_DATA_REQ:B0 0x29(4)]) =0b0.

*8 Interrupt will generate when completing transmission of packet data stored in the FIFO0.
This bit will also be cleared when setting PD_DATA_CFM0 ([PD_DATA_REQ:B0 0x29(0)]) =0b0.

[Note]

1. Regardless of [INT_EN_GRP3:B0 0x2C] register setting, this register value reflect internal status. For writing only 0b0 is valid, writing 0b1 is ignored.

0x27[INT_SOURCE_GRP4]

Function: Interrupt status for INT24 and INT25
Address: 0x27 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1	INT[25]	PLL unlock interrupt (*1) 0: no interrupt 1: interrupt (unlock)	0	R/W
0	INT[24]	Auto_Ack ready interrupt (*2) 0: no interrupt 1: interrupt	0	R/W

[Description]
*1 Interrupt will generate if PLL unlock is detected during TX_ON state or RX_ON state.
*2 When receiving Ack request packet, if TX ack packet is ready to send (Ack data is stored into FIFO and RF status becomes TX_ON state), interrupt will generate. This bit will be valid when setting AUTO_ACK_EN [AUTO_ACK_SET:B0 0x55(4)]) =0b1.

[Note]
1. Regardless of [INT_EN_GRP4:B0 0x2D] register setting, this register value reflect internal status. For writing only 0b0 is valid, writing 0b1 is ignored.

0x28[PD_DATA_REQ]

Function: Data transmission request status indication
Address: 0x28 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	PD_DATA_REQ1	FIFO1 data transmission request status (*1) 1: request existing (FIFO1 has data to be transmitted)	0	R/W
4	PD_DATA_CFM1	FIFO1 data transmission status0: not transmitted transmission on going 1: transmission completion	0	R/W
3-2	Reserved	Reserved	00	R/W
1	PD_DATA_REQ0	FIFO 0 data transmission request status (*1) 1: request existing (FIFO0 has data to be transmitted)	0	R/W
0	PD_DATA_CFM0	FIFO0 data transmission status 0: not transmitted or transmission on going 1: transmission completion	0	R/W

[Note]
*1 This bit will become 0b0 when a TX Length of transmitted data is written to the FIFO.

Only 0b0 setting is valid to this register.

0x29[PD_DATA_IND]

Function: Data reception status indication
Address: 0x29 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	PD_DATA_IND1	FIFO1 data reception status *1 0: reception on going or no reception 1: reception completion	0	R/W
4	CRC_RSLT1	FIFO1 CRC result *2 0: CRC error detected 1: no CRC error	0	R/W
3-2	Reserved	Reserved	00	R/W
1	PD_DATA_IND0	FIFO0 data reception status *1 0: reception on going or no reception 1: reception completion	0	R/W
0	CRC_RSLT0	FIFO0 CRC results *2 0: CRC error detected 1: no CRC error	0	R/W

[Note]
*1 This bit will not be cleared automatically even when reading out whole received packet data from the FIFO.
Please clear this bit (set 0b0) after receiving RX completion interrupt (INT[18] or INT[19]), Writing 0b1 is ignored.
*2 This bit will not be cleared automatically. Please clear this bit (set 0b0) at every packet reception, since CRC result is overwritten when next packet data is written into the FIFO, Writing 0b1 is ignored.
Even if clearing this bit, CRC error interrupt (INT[20] or INT[21] (group3)) is retained. Need to clear the CRC error interrupt in [INT_SOURCE_dGRP3:B0 0x26] register.

0x2A[INT_EN_GRP1]

Function: Interrupt mask for INT00 to INT05
Address: 0x2a (Bank 0)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	11	R/W
5-0	INT_EN [05:00]	Enabling interrupt 00 event to interrupt 05 event 0: masking interrupt 1: generate interrupt	11_1111	R/W

[Description]
1. For interrupt event details, please refer to the [INT_SOURCE_GRP1:B0 0x24] register.

0x2B[INT_EN_GRP2]

Function: Interrupt mask for INT08 to INT15
Address: 0x2b (Bank 0)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	INT_EN[15:08]	Enabling interrupt 08 event to interrupt 15 event 0: masking interrupt 1: generate interrupt	1111_1111	R/W

[Description]

1. For interrupt event details, please refer to the [INT_SOURCE_GRP2:B0 0x25] register.

0x2C[INT_EN_GRP3]

Function: Interrupt mask for INT16 to INT23
Address: 0x2c (Bank 0)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	INT_EN[23:16]	Enabling interrupt 16 event to interrupt 23 event 0: masking interrupt 1: generate interrupt	1111_1111	R/W

[Description]

1. For interrupt event details, please refer to the [INT_SOURCE_GRP3:B0 0x26] register.

0x2D[INT_EN_GRP4]

Function: Interrupt mask for INT24 and INT25.
Address: 0x2d (Bank 0)
Default Value: 0x03

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1	INT_EN[25]	Enabling interrupt 25 event 0: masking interrupt 1: generate interrupt	1	R/W
0	INT_EN[24]	Enabling interrupt 24 event 0: masking interrupt 1: generate interrupt	1	R/W

[Description]

1. For interrupt event details, please refer to the [INT_SOURCE_GRP4:B0 0x27] register.

0x2E[CH_EN_L]

Function: RF channel enable setting for low 8ch.
Address: 0x2e (Bank 0)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7	CH7_EN	Channel #7 enable setting (1: enable)	1	R/W
6	CH6_EN	Channel #6 enable setting (1: enable)	1	R/W
5	CH5_EN	Channel #5 enable setting (1: enable)	1	R/W
4	CH4_EN	Channel #4 enable setting (1: enable)	1	R/W
3	CH3_EN	Channel #3 enable setting (1: enable)	1	R/W
2	CH2_EN	Channel #2 enable setting (1: enable)	1	R/W
1	CH1_EN	Channel #1 enable setting (1: enable)	1	R/W
0	CH0_EN	Channel #0 enable setting (1: enable)	1	R/W

[Description]
1. For details, please refer to the “Programming Channel frequency”
2. Using RF channnel is set by [CH_SET:B0 0x6B] register.

0x2F[CH_EN_H]

Function: RF channel enable setting for high 8ch.
Address: 0x2f (Bank 0)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7	CH15_EN	Channel #15 enable setting (1: enable)	1	R/W
6	CH14_EN	Channel #14 enable setting (1: enable)	1	R/W
5	CH13_EN	Channel #13 enable setting (1: enable)	1	R/W
4	CH12_EN	Channel #12 enable setting (1: enable)	1	R/W
3	CH11_EN	Channel #11 enable setting (1: enable)	1	R/W
2	CH10_EN	Channel #10 enable setting (1: enable)	1	R/W
1	CH9_EN	Channel #9 enable setting (1: enable)	1	R/W
0	CH8_EN	Channel #8 enable setting (1: enable)	1	R/W

[Description]
1. For details, please refer to the “Programming Channel frequency”
2. Using RF channel is set by [CH_SET:B0 0x6B] register.

0x30[IF_FREQ_AFC_H]

Function: IF frequency setting during AFC operation (high byte)
Address: 0x30 (Bank 0)
Default Value: 0x1C

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_AFC[15:8]	IF frequency setting during AFC operation (high byte)	0001_1100	R/W

[Description]

1. Setting IF frequency during AFC operation. Combined together with [IF_FREQ_AFC_L:B0 0x31] register. These registers will be valid when AFC_EN ([AFC_CNTRL:B0 0x34(0)]) =0b1
2. After AFC completion, the setting specified by [IF_FREQ_H:B1 0x0A] and [IF_FREQ_L:B1 0x0B] registers are applied.
3. Depends on the RATE[2:0] ([DATA_SET:B0, 0x47(2-0)]) setting IF frequency will be updated automatically.

[Note]

1. For details of IF frequency setting, please refer to the “Programmin IF Frequency”.

0x31[IF_FREQ_AFC_L]

Function: IF frequency setting during AFC operation (low byte)
Address: 0x31 (Bank 0)
Default Value: 0x71

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_AFC[7:0]	IF frequency setting during AFC operation (low byte)	0111_0001	R/W

[Description]

1. Regarding this register, please refer to the [IF_FREQ_AFC_H:B0 0x30] register.

0x32[BPF_AFC_ADJ_H]

Function: Bandpass filter capacitance adjustment during AFC operation (high 2bits)
Address: 0x32 (Bank 0)
Default Value: 0x01

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	BPF_C_AFC[9:8]	Bandpass filter capacitance adjustment during AF C operation (high 2bits)	01	R/W

[Description]

1. Adjusting bandwidth of BPF during AFC operation. Combined together with [BPF_AFC_ADJ_L:B0 0x33] register. These registers will be valid when AFC_EN ([AFC_CNTRL:B0 0x34(0)]) =0b1.
2. After AFC completion, the setting specified by [BPF_ADJ_H:B1 0x0E] and [BPF_ADJ_L:B1 0x0F] registers are applied.

[Note]

1. For details, please refer to the “Programming BPF band width”.

0x33[BPF_AFC_ADJ_L]

Function: Bandpass filter capacitance adjustment during AFC operation (low byte)
Address: 0x33 (Bank 0)
Default Value: 0x9c

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_C_AFC[7:0]	Bandpass filter capacitance adjustment during AFC operation (low byte)	1001_1100	R/W

[Description]
1. Regarding this register, please refer to the [BPF_AFC_ADJ_H:B0 0x32] register.

0x34[AFC_CNTRL]

Function: AFC control setting
Address: 0x34 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6	AFC_UPDATE_EN	AFC updating enable setting 0: disable updating 1: enable updating	0	R/W
5-4	UPDATE_TERM[1:0]	AFC update period setting(*1) 0b00: 8 symbols 0b01: 16 symbols 0b10: 32 symbols 0b11: 64 symbols	00	R/W
3-1	Reserved	Reserved	000	R/W
0	AFC_EN	AFC enable setting 0: disable AFC 1: enable AFC	0	R/W

[Description]
*1 Update timing depends on the data rate specified by [DATA_SET:B0 0x47] register.

[Note]
1. Please use the value specified in the "Initial register setting" file.

0x35[TX_ALARM_LH]

Function: TX FIFO Full-level setting
Address: 0x35 (Bank 0)
Default Value: 0xF0

Bit	Symbol	Description	Default Value	R/W
7-0	TX_ALARM_LH[7:0]	TX FIFO full level setting (setting range: 0-255 byte) (Default Value 240 bytes)	1111_0000	R/W

[Description]

1. For details, please refer to the “TX FIFO usage notification function”.
2. When TX FIFO data size exceeds the full level, INT[05] (group1) interrupt will generat and SINTN (pin #10) outputs “Low”.

0x36[TX_ALARM_HL]

Function: TX FIFO empty level setting
Address: 0x36 (Bank 0)
Default Value: 0x0F

Bit	Symbol	Description	Default Value	R/W
7-0	TX_ALARM_HL[7:0]	TX FIFO empty level setting (setting range 0-255 byte) (Default Value 31bytes)	0000_1111	R/W

[Description]

1. For details, please refer to the “TX FIFO usage notification function”.
2. When TX FIFO data size becomes below the empty level, INT[04] (group1) interrupt will generate and SINTN (pin #10) outputs ”Low”.

0x37[RX_ALARM_LH]

Function: RX FIFO full level setting
Address: 0x37 (Bank 0)
Default Value: 0x05

Bit	Symbol	Description	Default Value	R/W
7-0	RX_ALARM_LH[7:0]	RX FIFO full level setting (setting range 0-255 byte) (Default Value 5 bytes)	000_0101	R/W

[Description]

1. For details, please refer to the “RX FIFO usage notification function”.
2. When RX FIFO data size exceeds the full level, INT[05] (group1) interrupt will generate and SINTN (pin #10) outputs “Low”.

0x38[RX_ALARM_HL]

Function: RX FIFO empty level setting
Address: 0x38 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	RX_ALARM_HL[6:0]	RX FIFO empty level setting (setting range 0-255 byte) (Default Value 0byte)	000_0000	R/W

[Description]

1. For details, please refer to the "RX FIFO usage notification function".
2. When RX FIFO data size becomes below the empty level, INT[04] (group1) interrupt will generate and SINTN (pin #10) outputs "Low".

0x39[PREAMBLE_SET]

Function: Preamble pattern setting
Address: 0x39 (Bank 0)
Default Value: 0x55

Bit	Symbol	Description	Default Value	R/W
7-0	PR[7:0]	Preamble pattern setting (Fixed 1 byte pattern)	0101_0101	R/W

[Description]

1. Preamble pattern has to be repetitive pattern which can be used for synchronization. Either 0xAA or 0x55 is used. 0xAA should be set when using IEEE802.15.4d/g,mode.
2. LSB first
3. In TX, the length of preamble pattern is specified by the [TX_PR_LEN:B0 0x42] register. In Rx, the preamble checking length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x3A[SFD1_SET1]

Function: SFD pattern #1 1st byte setting (max 4bytes)
SFD: Start of Frame Delimiter
Address: 0x3a (Bank 0)
Default Value: 0xA7

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[7:0]	SFD pattern #1 setting (bit0 to bit7)	1010_0111	R/W

[Description]

1. For details, please refer to the "SFD detection function".
2. 1st pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b0.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x3B[SFD1_SET2]

Function: SFD pattern #1 2nd byte setting (max 4byte)
Address: 0x3b (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[15:8]	SFD pattern #1 setting (bit8 to bit 15)	0000_0000	R/W

[Description]

1. For details, please refer to the “SFD detection function”.
2. 1st pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b0.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x3C[SFD1_SET3]

Function: SFD pattern #1 3rd byte setting (max 4byte)
Address: 0x3c (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[23:16]	SFD pattern #1 setting (bit16 to bit23)	0000_0000	R/W

[Description]

1. For details, please refer to the “SFD detection function”.
2. 1st pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b0.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x3D[SFD1_SET4]

Function: SFD pattern #14th byte setting (max 4byte)
Address: 0x3d (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD1[31:24]	Frame synchronization pattern (max 4bytes) of 4th byte of 1st pattern	0000_0000	R/W

[Description]

1. For details, please refer to the “SFD detection function”.
2. 1st pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b0.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x3E[SFD2_SET1]

Function: SFD pattern #2 1st byte setting (max 4byte)
SFD: Start of Frame Delimiter
Address: 0x3e (Bank 0)
Default Value: 0xA7

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[7:0]	SFD pattern#2 setting (bit0 to bit7)	1010_0111	R/W

[Description]
1. For details, please refer to the “SFD detection function”.
2. 2nd pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b1.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x3F[SFD2_SET2]

Function: SFD pattern #2 2nd byte setting (max 4byte)
Address: 0x3f (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[15:8]	SFD pattern #2 setting (bit8 to bit15)	0000_0000	R/W

[Description]
1. For details, please refer to the “SFD detection function”.
2. 2nd pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b1.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x40[SFD2_SET3]

Function: SFD pattern #2 3rd byte setting (max 4byte)
Address: 0x40 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[23:16]	SFD pattern #2 setting (bit16 to bit23)	0000_0000	R/W

[Description]
1. For details, please refer to the “SFD detection function”.
2. 2nd pattern of SFD is valid if MRFSKFSD [PACKET_MODE_SET:B0 0x45(6)]) =0b1.
3. LSB first
4. Valid SFD length is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x41[SFD2_SET4]

Function: SFD pattern #2 4th byte setting (max 4byte)
Address: 0x41 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SFD2[31:24]	SFD pattern #2 setting (bit24 to bit31)	0000_0000	R/W

[Description]

1. For details, please refer to the “SFD detection function”.
2. 2nd pattern of SFD is valid if MRFSKFSD ([PACKET_MODE_SET:B0 0x45(6)]) =0b1.
3. LSB first
4. Valid length of SFD field is specified by the [RX_PR_LEN/SFD_LEN:B0 0x43] register.

0x42[TX_PR_LEN]

Function: TX preamble length setting (max 255 byte)
Address: 0x42 (Bank 0)
Default Value: 0x04

Bit	Symbol	Description	Default Value	R/W
7-0	TXPR_LEN[7:0]	TX preamble length setting (setting range 0-255 bytes) (Default Value 4 bytes)	0000_0100	R/W

[Note]

Please do not set below 4, since IEEE 802.15.4g standard defines “phyFSKPreambleRepetitions” parameter is set from 4.

Setting value depends on the data rate setting when using diversity function. Please use the value specified in the "Initial register setting" file.

0x43[RX_PR_LEN / SFD_LEN]

Function: RX preamble setting (max 15byte) and SFD length setting
Address: 0x43 (Bank 0)
Default Value: 0x02

Bit	Symbol	Description	Default Value	R/W
7-4	RX_PR_LEN[3:0]	RX preamble setting. (setting range: 1 to 4 byte) Note: The initial value 0b0000 is handled as 1byte length. More than 0b0100 values are handled as 4 byte length.)	0000	R/W
3	2PB_DET_EN (*2)	Two preamble search setting 0: search pattern specified by the [PREAMBLE_SET: B0 0x39] register 1: search both 0xAA or 0x55 pattern	0	R/W
2-0	SFD_LEN[2:0]	SFD field length setting (transmitted from LSB) (*1) 0b001: SFD[7:0] enable 0b010: SFD[15:0] enable (default) 0b011: SFD[23:0] enable 0b100: SFD[31:0] enable	010	R/W

[Note]
- *1 If other values are set, SFD transmission and checking function is invalid.
- *2 When enabling two SFD search (set 0b1), the setting of bit error tolerance specified by PB_SYNC[3:0] [SYNC_CONDITION:B0 0x44(3-0)]) are invalid, and assumed as 0 bit tolerance and RX_PR_LEN[3:0] should be set 2 bytes or less value.
- *3 When AFC_EN ([AFC_CNTRL:B0 0x34(0)]) =0b1, AFC convergence time (maximum 24 bits) should be required. If overlapping RX_PR_LEN[3:0] and AFC convergence time, SFD detection is not possible. Therefore RX_PR_LEN[3:0] setting value should be leass than the value subtracting AFC convergence time (3byte) from TXPR_LEN[7:0] ([TX_PR_LEN:B0 0x42]).

0x44[SYNC_CONDITION]

Function: Bit error tolerance setting in RX preamble and SFD detection (max 15bits)
Address: 0x44 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	SFD_SYNC[3]	Error tolerance value (bits) in SFD detection (setting range 0 to 15bits)	0	R/W
6	SFD_SYNC[2]		0	R/W
5	SFD_SYNC[1]		0	R/W
4	SFD_SYNC[0]		0	R/W
3	PR_SYNC[3]	Error tolerance value (bits) in RX preamble detection (setting range 0 to 15bits)	0	R/W
2	PR_SYNC[2]		0	R/W
1	PR_SYNC[1]		0	R/W
0	PR_SYNC[0]		0	R/W

[Note]
1. These setting are invalid when Manchester coding is selected at [DATA_SET:B0 0x47] register.

0x45[PACKET_MODE_SET]

Function: Packet configuration (FIFO mode)
Address: 0x45 (Bank 0)
Default Value: 0x1B

Bit	Symbol	Description	Default Value	R/W
7	FIFO_ADR_EN	FIFO address indication setting (*1) 0: disable address indication 1: enable address indication	0	R/W
6	MRFSKSFD	SFD pattern selection (*2) 0: SFD#1 1: SFD#2	0	R/W
5	ADDFIL_NG_SET	Data processing after address mismatch detection 0: abort data immediately. 1: abort data after RX completion	0	R/W
4	WHITENING	Whitening enable setting (*6) 0: disable Whitening 1: enable Whitening	1	R/W
3	ED_NOTICE	ED value indication enable setting in RX packet 0: ED value is not attached to the RX packet 1: ED value (1byte) is attached to the RX packet	1	R/W
2	AUTO_TX	Automatic TX mode setting (*4) 0: disable automatic TX mode 1: enable automatic TX mode	0	R/W
1	IEEE_MODE	IEEE 802.15.4 packet mode selection (*5) 0: IEEE802.15.4d packet format 1: IEEE802.15.4g packet format	1	R/W
0	ADDFIL_IDLE_DET	IDLE detection mode setting after address mismatch detection (*3) 0: After data abort, interrupt will generate without IDLE detection 1: After data abort, interrupt will generate if IDLE is detected.	1	R/W

[Description]

*1 When enabling, [RD_FIFO_LAST:B0 0x7C] register indicates the address next to be written.

*2 For details, please refer to the “SFD detection function”.

*3 For details, please refer to the “Address filtering function”.

*4 If enable, RF state move to TX_ON state automatically without setting SET_TRX [RF_STATUS:B0 0x6c(3-0)]) = 0b1001(TX_ON). Transmission starts automatically in the following cases.

1. TX data specified by Length field are written to the TX FIFO.
2. Amount of written TX data is reached to the trigger level specified by the [FAST_TX_SET:B0 0x6A] register. (Length field is included in the amount of TX data.)

If switching RF state to RX_ON or TRX_OFF immediately after TX completion, the following two methods exist;.

a. Issuing RX_ON or TRX_OFF command and set 0b0 to this bit during data transmission.
b. Keep 0b1 setting and set TX_DONE_RX ([ACK_TIMER_EN:B0 0x52(5)]) =0b1 or TX_DONE_OFF ([ACK_TIMER_EN:B0 0x52(4)]) =0b1. For details , please refer to the [ACK_TIMER_EN:B0 0x52] register.

*5 Valid when packet mode (FIFO mode) is selected. Packet mode is selected by register [PLL_MON/DIO_SEL: B0 0x69] register. (default setting is packet mode.)

*6 Data Whitening will be applied in the following cases;

1. In IEEE802.15.4d mode (bit1=0b0), Whitening function is activated by enabling this bit.
2. In IEEE802.15.4g mode (bit1=0b1), Whitening function is activated by enabling this bit and Whitening bit in PHR data is set to 0b1. However, in RX with activating FEC function, dewhitening is activated by enabling this bit regardless of the whitening bit setting in PHR data.

[Note]

1. If enabling AUTO_TX, wait more than 150µs after the FIFO write completion before accessing the [RF_STATUS:B0 0x6C] register.

0x46[FEC/CRC_SET]

Function: FEC and CRC configuration
Address: 0x46 (Bank 0)
Default Value: 0x03

Bit	Symbol	Description	Default Value	R/W
7	INTLV_EN	Interleave enable setting (*1) 0: disable interleave 1: enable interleave	0	R/W
6	FEC_EN	FEC enable setting 0: disable FEC 1: enable FEC	0	R/W
5	FEC_SCHEME	FEC scheme selection 0: NRNSC 1: RSC	0	R/W
4	CRC_INIT	CRC initialized state setting 0: all “0” setting 1: all “1” setting	0	R/W
3	CRC_EN	CRC scheme information source (*3) 0: use information from FCS Length Field 1: use information from CRC_MODE[1:0] setting	0	R/W
2-1	CRC_MODE[1:0]	CRC mode setting (*2) 0b00: CRC8 0b01: CRC16 (Default Value) 0b10: CRC32 0b11: CRC16 -IBM	01	R/W
0	CRC_DONE	CRC execution command (1: execute CRC calculation)	1	R/W

[Description]

1. When IEEE802.15.4g mode is selected by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b1, CRC is calculated according to the CRC_MODE[1:0] setting in TX mode.
   In RX mode, if 0b0 is set to this bit, CRC is calculated according to the FCS Length setting in Frame Control Field.
   If 0b1, CRC is calculated according to the CRC_MODE [1:0] setting.
   For more details of FCS Length, please refer to the chapter 6.3.2a of IEEE 802.15.4g standard.
2. When IEEE802.15.4d mode is selected by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b0, CRC is calculated according to the CRC_MODE[1:0] setting in both TX and RX mode.

Each CRC polynomials is shown as below.

CRC8 $= X^8 + X^2 + X + 1$
CRC16 $= X^{16} + X^{12} + X^5 + 1$
CRC16-IBM $= X^{16} + X^{12} + X^2 + 1$
CRC32 $= X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

The following table shows the CRC settings.

IEEE_MODE [PACKET_MODE_SET: B0 0x45(1)]	CRC_DONE	CRC_EN	CRC_MODE [1:0]	Description of CRC Operation
0 (4g Mode)	1	0	00/01/10/11	Calculating according to FCS Length setting. FCS Length = 0b0: CRC32 FCS Length = 0b1: CRC16
		1	00/01/10/11	Calculating according to CRC_MODE[1:0] setting.
	0	0/1	00/01/10/11	No CRC calculation
1 (4d Mode)	1	0/1	00/01/10/11	Calculating according to CRC_MODE [1:0] setting.
	0	0/1	00/01/10/11	No CRC calculation

[Note]

*1 This bit is valid when FEC_EN=0b1.

*2 When AUTO_ACK function is enabled by AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)]) =0b1, please set 0b1 to both CRC_EN and CRC_DONE, and set proper CRC mode to the CRC_MODE[1:0] (bit2-1) before transmitting the Ack packet.

*3 When **CRC calculation is using the FCS Length setting in the packet by setting CRC_EN = 0b0**, the CRC setting in TX/RX is valid in the following cases. If CRC_EN = 0b1, please ignore the following description

TX:

The CRC setting for TX data is valid when SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3-0)]) is other than 0x6. Therefore,

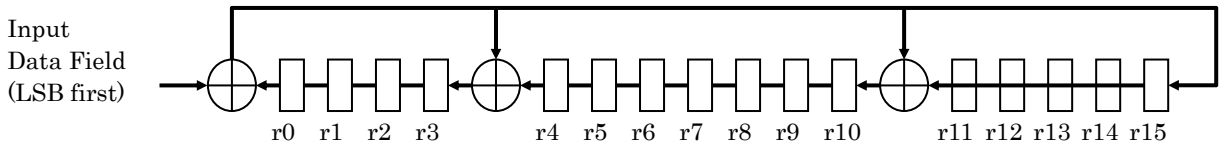
1. When in RX_ON state, please issuing TRX_OFF or Force_TRX_OFF command before writing the TX data to the TX FIFO. Or,
2. Please writ the TX data to the TX FIFO after issuing TX_ON command. However if FAST_TX mode is valid by the [FAST_TX_SET:B0 0x6A] register, this operation is not necessary.

RX:

The CRC setting for RX data is valid only when SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3:0)]) =0x6. Therefore, all received data stored in the RX FIFO should be read out during RX_ON state (before issuing TRX_OFF or Force_TRX_OFF command). When reading the received data after issuing TRX_OFF or Force_TRX_OFF command, please set 0b1 to the CRC_EN and set proper CRC mode to the CRC_MODE[1:0] before reading data.

*4 When IEEE802.15.4g mode is selected, if CRC32 is set, Ack packet cannot be received since the minimum packet length is 4 bytes. For Ack packet, CRC16 setting or disable CRC is necessary..

Example: CRC16 polynomial circuit



In TX mode, defining the PSDU field from the length information, and executing CRC calculation to the PSDU field according to the CRC_MODE[1:0] setting. Following TX data, CRC result is added. The length information should include FCS(CRC) field length.

In RX mode, regardless of CRC_EN setting, Length and PSDU field are detected automatically and generate CRC. And generated CRC is compared with the CRC data located in FCS field of RX packet. The result will be indicated by CRC_RSLT1/0 ([PD_DATA_IND:B0 0x29(4/0)]).

0x47[DATA_SET]

Function: Data configuration
Address: 0x47 (Bank 0)
Default Value: 0x11

Bit	Symbol	Description	Default Value	R/W
7	NBO_SEL	Narrow band option setting (*1) 0: normal mode 1: narrow band mode (optional function)	0	R/W
6	TX_POL	TX data polarit settingy 0: data “1”= deviated to high frequency, data “0”=low frequency 1: data “1”= deviated to low frequency, data “0”=high frequency	0	R/W
5	RX_POL	RX data polarity setting 0: data “1” = deviated to high frequency, data “0”=low frequency 1: data “1” = deviated to low frequency, data “0”=high frequency	0	R/W
4	GFSK_EN	GFSK mode setting 0: disable (FSK) 1: enable (GFSK)	1	R/W
3	FORMAT	Coding mode setting 0: NRZ coding 1: Manchester coding (*2)	0	R/W
2-0	RATE[2:0]	Data rate setting 0b000: 50 kbps 0b001: 100 kbps (Default Value) 0b010: 200 kbps 0b011: 400 kbps Others: Reserved	001	R/W

[Note]

*1 If enabling this bit, RF relative registers should be changed. For details, please refer to the “Programming narrow band option setting”

Following table shows the occupied bandwidth in each data rate defined by RATE[2:0].

NBO_SEL	50 kbps	100 kbps	150 kbps	200 kbps	400 kbps
“0”	200 kHz	400 kHz (default value)	400 kHz (default value)	600 kHz	800 kHz
“1”	200 kHz	200 kHz	-	400 kHz	-

When using 150kbps please set registers according to the following table.

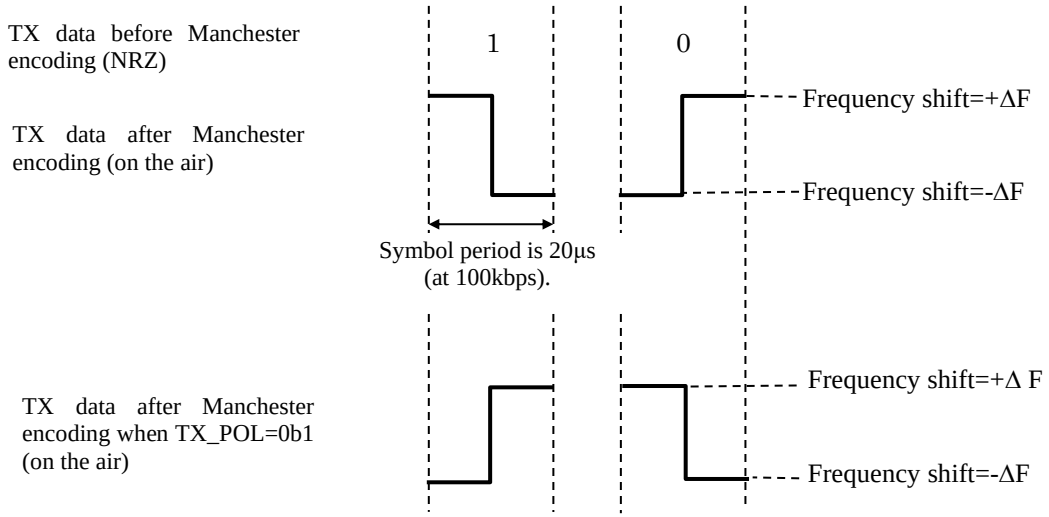
Register or bit name	Setting value
[RATE_SET1:B0 0x04]	0x02
[RATE_SET2:B0 0x05]	0x03
RATE[2:0] ([RATE_SET: B0 0x47 (2-0)])	0b010

When using 10kbps, 20kbps or 40kbps, please refer to the "Initial register setting" file.

*2. Manchester encoding is applied to the data following the preamble (SFD/Length/user data(PSDU)/CRC field). For details, please refer to the "Packet Format."
For details on the Manchester coding, please refer to the following "Manchester coding". The Manchester coding is not applied to the ACK packet during AutoAck. The FEC function does not support the Manchester code.

Manchester coding

Following figure shows the relation between input TX data and the Manchester encoded data on the air when setting FORMAT=0b1 (Manchester coding). The Manchester encoded data rate on the air (baud rare) is half of the data rate setting specified by RATE[2:0]. For example, when setting 100kbps (RATE[2:0]=0b001), the baud rate becomes 50kbps. If set TX_POL=0b1 or RX_POL=0b1, the data polarity is inverted as following figure.



0x48[CH0_FL]

Function: Channel #0 frequency (F-counter) setting (low byte)
Address: 0x48 (Bank 0)
Default Value: 0x44
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH0_F[7:0]	Channel #0 F-counter (bit0 to bit7)	0100_0100	R/W

[Description]

1. For details, please refer to the “Programming Channel#0 Frequency”.

0x49[CH0_FM]

Function: Channel #0 frequency (F-counter) setting (middle byte)
Address: 0x49 (Bank 0)
Default Value: 0x44
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH0_F[15:8]	Channel #0 F-counter (bit8 to bit15)	0100_0100	R/W

[Description]

1. For details, please refer to the “Programming Channel#0 Frequency”.

0x4A[CH0_FH]

Function: Channel #0 frequency (F-counter) setting (high 4bits)
Address: 0x4a (Bank 0)
Default Value: 0x0A
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	CH0_F[19:16]	Channel #0 F-counter (bit16 to bit19)	1010	R/W

[Description]
1. For details, please refer to the “Programming Channel#0 Frequency”.

0x4B[CH0_NA]

Function: Channel #0 frequency (N-counter and A-counter) setting
Address: 0x4b (Bank 0)
Default Value: 0x61
923.100MHz (Xtal frequency: 36MHz)

Bit	Symbol	Description	Default Value	R/W
7-4	CH0_N[3:0]	Channel #0 N-counter	0110	R/W
3-2	Reserved	Reserved	00	R/W
1-0	Ch0_A[1:0]	Channel #0 A-counter	01	R/W

[Description]
1. For details, please refer to the “Programming Channel#0 Frequency”.

0x4C[CH_SPACE_L]

Function: Channel space setting (low byte)
Address: 0x4c (Bank 0)
Default Value: 0x82 (Channel space = 400 kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH_SP_F[7:0]	Channel space setting (bit0 to bit7)	1000_0010	R/W

[Description]
1. Setting the channel space. Combined together with [CH_SPACE_H:B0 0x4D] register.
2. For details, please refer to the “Programming Channel space”.

0x4D[CH_SPACE_H]

Function: Channel space setting (high byte)
Address: 0x4d (Bank 0)
Default Value: 0x2D (Channel space= 400 kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	CH_SP_F[15:8]	Channel space setting (bit8 to bit15)	0010_1101	R/W

[Description]
1. Regarding this register, please refer to the [CH_SPACE_L:B0 0x4C] register.

0x4E[F_DEV_L]

Function: GFSK frequency deviation setting (low byte)
Address: 0x4e (Bank 0)
Default Value: 0xB0 (Fdev=50 kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	F_DEV[7:0]	GFSK frequency deviation setting (bit0 to bit7)	1011_0000	R/W

[Description]
1. Setting frequency deviation during GFSK modularion. Combined together with [F_DEV_H:B0 0x4F] register.
2. For details, please refer to the “Programming GFSK frequency deviation”.

[Note]
1. Frequency deviation of FSK modulation is decided by register values of [FSK_FDEV1] to [FSK_FDEV4].
2. If using 400kbps, and 100kbps or 200kbps with NBO_SEL ([DATA_SET:B0 0x47(7)]) = 0b1, the modulation index should be less than 0.6.

0x4F[F_DEV_H]

Function: GFSK frequency deviation setting (high byte)
Address: 0x4f (Bank 0)
Default Value: 0x05 (Fdev=50 kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	F_DEV[15:8]	GFSK frequency deviation setting (bit8 to bit15)	0000_0101	R/W

[Description]
1. Regarding this register, please refer to the [F_DEV_L:B0 0x4E] register.

0x50[ACK_TIMER_L]

Function: Ack timer setting (low byte)
Address: 0x50 (Bank 0)
Default Value: 0x08

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_TIMER[7:0]	Ack timer setting (bit0 to bit7)	0000_1000	R/W

[Description]

1. Combined together with the [ACK_TIMER_H:B0 0x51] register.
   These registers are valid when ACK_TIMER_EN ([ACK_TIMER_EN:B0 0x52(0)]) = 0b1.
2. For details of AUTO_ACK function, please refer to the "AUTO_ACK function".
3. Timer clock source will depend on data rate setting.

Data rate	Timer clock
10kbps	0.18 MHz
20kbps	0.36 MHz
40kbps	0.72 MHz
50kbps	0.9 MHz
100kbps	1.8 MHz
150kbps	2.7 MHz
200kbps	3.6 MHz
400kbps	7.2 MHz

Example: If ACK_TIMER[15:0]= 0x708 (Default, 1800) with 100kbps setting.
Timer duration = 1800 / 1.8MHz = 1ms

0x51[ACK_TIMER_H]

Function: Ack timer setting (high byte)
Address: 0x51 (Bank 0)
Default Value: 0x07

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_TIMER[15:8]	Ack timer setting (bit8 to bit15)	0000_0111	R/W

[Description]

1. Regarding this register, please refer to the [ACK_TIMER_L:B0 0x50] register.

0x52[ACK_TIMER_EN]

Function: Auto_Ack timer control setting
Address: 0x52 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	TX_DONE_RX	RX state transition enable setting after TX completion (*1 to *4) 0: disable 1: enable When enabling this bit, RF state automatically move to RX_ON after transmission completion.	0	R/W
4	TX_DONE_OFF	TRX_OFF state transition enable setting after TX completion (*1to *4) 0: disable 1: enable When enabling this bit, RF state automatically move to TRX_OFF after reception completion.	0	R/W
3-1	Reserved	Reserved	000	R/W
0	ACK_TIMER_EN	Ack timer enable setting 0: disable Ack timer 1: enable Ack timer	0	R/W

[Description]

1. For details of AUTO_ACK function, please refer to the “AUTO_ACK function”.
2. When AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)]) =0b1and ACK_TIMER_EN=0b l, ACK packet will be transmitted automatically after Ack timer expired.

[Note]

*1 If both TX_DONE_RX and TX_DONE_OFF are set to 0b1, TX_DONE_RX has priority.

*2 The following table shows the RF state trnsition priority among TX_DONE_RX setting, TX_DONE_OFF setting and RF state setting command specified by SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3-0)]). However, if once RF state transition is completed due to TX_DONE_RX or TX_DONE_OFF setting, Any RF state setting command has priority regadless of following priority.
Priority : Force_TRX_OFF > TRX_DONE_RX > TX_DONE_OFF > (TRX_OFF/TX_ON/RX_ON)

TX_DONE_RX	TX_DONE_OFF	SET_TRX[3:0] [RF_STATUS:B0 0x6C]	RF state after TX completion
0	1	Force_TRX_OFF	TRX_OFF immediately after issuing Force_TRX_OFF command.
		TRX_OFF	TRX_OFF.
		TX_ON	TRX_OFF.
		RX_ON	TRX_OFF.
1	0	Force_TRX_OFF	TRX_OFF immediately after issuing Force_TRX_OFF command.
		TRX_OFF	RX_ON.
		TX_ON	RX_ON.
		RX_ON	RX_ON.
1	1	Force_TRX_OFF	TRX_OFF immediately after issuing Force_TRX_OFF command.
		TRX_OFF	RX_ON.
		TX_ON	RX_ON.
		RX_ON	RX_ON.

*3 When TX_DONE_RX is enabled, after TX completion, wait until the [RF_STATUS:B0 0x6C] register becomes 0x66 before write accessing to the register.
*4 When TX_DONE_OFF is enabled, after TX completion, wait until the [RF_STATUS:B0 0x6C] register becomes 0x88 before write accessing to the register.

0x53[ACK_FRAME1]

Function: Ack Frame Control Field (2bytes) setting (low byte)
Address: 0x53 (Bank 0)
Default Value: 0x02

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_FRAME[7:0]	Ack Frame Control Field (bit0 to bit7)	0000_0010	R/W

[Description]
1. Combined together with [ACK_FRAME2] register. ACK_FRAME[15:0] wll be transmitted with LSB first.
2. For details of AUTO_ACK function, please refer to the “AUTO_ACK function”.
3. For detail of Ack packet, please refer to the IEEE 802.15.4i standard.

The following table shows the format of the Frame Control Field.

Register	bit	Ack frame
ACK_FRAME2	7-6	Source Addressing Mode
	5-4	Frame Version
	3-2	Dest Addressing Mode
	1-0	Reserved
ACK_FRAME1	7	Reserved
	6	PAN ID Compression
	5	Ack Request
	4	Frame Pending
	3	Security Enabled
	2-0	Frame Type

Note; When transmitting Ack frame, the Frame Control field (2byte) uses this register setting, the Sequence Number field (1byte) is achieved from received data, and FCS (2byte) is calculated automatically.

0x54[ACK_FRAME2]

Function: Ack Frame Control Field (2bytes) setting (high byte)
Address: 0x54 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ACK_FRAME[15:8]	Ack Frame Control Field (bit8 to bit15)	0000_0000	R/W

[Description]
1. Regarding this register, please refer to the [ACK_FRAME1:B0 0x53] register.

0x55[AUTO_ACK_SET]

Function: Auto_Ack function setting
Address: 0x55 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	RX_ACK_CANCEL	ACK packet forced cancelation enable setting (*4) 0: disable 1: enable (discarding received ACK packet)	0	R/W
6	AUTO_RX_EN	Automatic ACK reception enable setting (*1),(*4) 0: disable ACK reception 1: enable ACK reception	0	R/W
5	Reserved	Reserved	0	R/W
4	AUTO_ACK_EN	Auto_Ack enable setting (*2) 0: disable Auto_Ack 1: enable Auto_Ack	0	R/W
3-2	Reserved	Reserved	00	R/W
1	ACK_SEND	Execute ACK packet transmission (1: transmit) (*3)	0	R/W
0	ACK_STOP	Ack packet abort/receive stop (1: stop) (*3)	0	R/W

[Description]

1. For details of AUTO_ACK function, please refer to the "AUTO_ACK function".

*1 The function that enable RX_ON immediately after transmitting a packet with Ack request.
*2 The function that ready to send ACK packet (including TX_ON execution) after receiving a packet with Ack request.
*3 By setting ACK_SEND or ACK_STOP, following operations are executed.
If set ACK_SEND=0b1
Transmit ACK packet.
If set ACK_STOP=0b1
TX mode: Discards ACK packet (will not be transmitted) and RF_STATUS keeps TX_ON state.
RX mode: Stop receiving operation and RF_STATUS moves to TRX_OFF state.
*4 For Ack packet detection, Address Filtering function should be valid by setting 0b1 to one of bit from bit[4:0] in [ADDFIL_CNTRL:B2 0x60] register. When AUTO_RX_EN=0b1, received ACK packet just after transmitting a packet with ACK request as below table. Following table operation is independent from address matching.

Bit7(RX_ACK_CANCEL)	Bit6(AUTO_RX_EN)	Operation
0b1	0b1	Receive first packet only ACK request bit is transmitted.
0b1	0b0	Remove all received ACK packets.
0b0	any	Receive all ACK packets.

[Note]

1. Either ACK_SEND or ACK_STOP should be 0b1. If set 0b1 to both bits, ACK_STOP has priority.
2. When AUTO_RX_EN is enabled, after TX completion, wait until the [RF_STATUS:B0 0x6C] register becomes 0x66 before write accessing to the register.
3. When AUTO_ACK_EN is enabled, after RX completion, wait until the [RF_STATUS:B0 0x6C] register becomes 0x99 before write accessing to the register.
4. When using AUTO_ACK function (AUTO_ACK_EN=0b1), [TX_ALARM_LH:B0 0x35] register should be 0x00 before ACK packet transmission.

0x56-58[Reserved]

0x59[GFIL00/FSK_FDEV1]

Function: Gaussian filter coefficient setting 0 / FSK 1st frequency deviation setting

Address: 0x59
Default Value: 0x00 (GFSK Modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL001[7:0] FSK_FDEV1[7:0]	Gaussian filter coefficient setting 0 FSK 1st frequency deviation setting [register value * 33.4 * 2 (Hz)]	0000_0000	R/W

[Description]

1. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
   If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation will be selected, otherwise FSK modulation.
   For details of GFSK setting, please refer to the "Programming Gaussian Filter".
2. In FSK modulation, this register sets the 1st frequency deviation. (set as the deviation from the centre frequency.)
   For details, please refer to the "Programming FSK modulation".

0x5A[GFIL01/FSK_FDEV2]

Function: Gaussian filter coefficient setting 1 / FSK 2nd frequency deviation setting
Address: 0x5a (Bank 0)
Default Value: 0x00 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL01[7:0] FSK_FDEV2[7:0]	Gaussian filter coefficient setting 1 FSK 2nd frequency deviation setting (*2) [registrer value * 33.4 * 2 (Hz)]	0000_0000	R/W

[Description]

1. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
   If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation will be selected, otherwise FSK modulation.
   For details of GFSK setting, please refer to the "Programming Gaussian Filter".
2. In FSK modulation, this register sets the 2nd frequency deviation. (set as the deviation from the 1st frequency deviation.)
   For details, please refer to the "Programming FSK modulation".

0x5B[GFIL02/FSK_FDEV3]

Function: Gaussian filter coefficient setting 2 / FSK 3rd frequency deviation setting
Address: 0x5b (Bank 0)
Default Value: 0x10 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL02[7:0] FSK_FDEV3[7:0]	Gaussian filter coefficient setting 2 FSK 3rd frequency deviation setting *2 [registrer value * 33.4 * 2 (Hz)]	0001_0000	R/W

[Description]

1. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
   If GFSK_EN [DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation will be selected, otherwise FSK modulation.
   For details, please refer to the "Programming Gaussian Filter".
2. In FSK modulation, this register offsets the 3rd frequency deviation. (set the deviation from the 2nd frequency deviation.)
   For details, please refer to the "Programming FSK modulation".

0x5C[GFIL03/FSK_FDEV4]

Function: Gaussian filter coefficient setting 3 / FSK 4th frequency deviation setting
Address: 0x5c (Bank 0)

Default Value: 0x01 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL03[7:0] F_DEV3[7:0]	Gaussian filter coefficient setting 3 FSK 4th frequency deviation setting *2 [registrer value * 33.4 * 2 (Hz)]	0000_0001	R/W

[Description]

1. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
   If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation will be selected, otherwise FSK modulation.
   For details, please refer to the “Programming Gaussian Filter”.
2. In FSK modulation, this register offsets the 4th frequency deviation. (set as the deviation from the 3rd frequency deviation.)
   For details, please refer to the “Programming FSK modulation”.

0x5D[GFIL04]

Function: Gaussian filter coefficient setting 4
Address: 0x5d (Bank 0)
Default Value: 0x03 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL04[7:0]	Gaussian filter coefficient setting 4	0000_0011	R/W

[Description]

1. This register will be valid when GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1.
2. For details, please refer to the “Programming Gaussian Filter”.

0x5E[GFIL05]

Function: Gaussian filter coefficient setting 5
Address: 0x5e (Bank 0)
Default Value: 0x05 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL05[7:0]	Gaussian filter coefficient setting 5	0000_0101	R/W

[Description]

1. If GFSK_EN [DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x5F[GFIL06]

Function: Gaussian filter coefficient setting 6
Address: 0x5f (Bank 0)
Default Value: 0x09 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL06[7:0]	Gaussian filter coefficient setting 6	0000_1001	R/W

[Description]

1. If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x60[GFIL07]

Function: Gaussian filter coefficient setting 7
Address: 0x60 (Bank 0)
Default Value: 0x0F (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL07[7:0]	Gaussian filter coefficient setting 7	0000_1111	R/W

[Description]

1. If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x61[GFIL08]

Function: Gaussian filter coefficient setting 8
Address: 0x61 (Bank 0)
Default Value: 0x15 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL08[7:0]	Gaussian filter coefficient setting 8	0001_0101	R/W

[Description]

1. If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x62[GFIL09]

Function: Gaussian filter coefficient setting 9
Address: 0x62 (Bank 0)
Default Value: 0x1A (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL09[7:0]	Gaussian filter coefficient setting 9	0001_1010	R/W

[Description]

1. If GFSK_EN ([DATA_SET:B0 0x47) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x63[GFIL10]

Function: Gaussian filter coefficient setting 10
Address: 0x63 (Bank 0)
Default Value: 0x1F (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL10[7:0]	Gaussian filter coefficient setting 10	0001_1111	R/W

[Description]

1. If GFSK_EN ([DATA_SET:B0 0x47(4)]) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x64[GFIL11]

Function: Gaussian filter coefficient setting 11
Address: 0x64 (Bank 0)
Default Value: 0x20 (GFSK modulation BT=0.5)

Bit	Symbol	Description	Default Value	R/W
7-0	GFIL11[7:0]	Gaussian filter coefficient setting 11	0010_0000	R/W

[Description]

1. If GFSK_EN ([DATA_SET:B0 0x47) =0b1, GFSK modulation scheme will be used, otherwise FSK modulation scheme will be used.
2. For details, please refer to the “Programming Gaussian Filter”.

0x65[FSK_TIME1]

Function: FSK 3rd frequency deviation (FDEV3) hold time setting
Address: 0x65 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME1[7:0]	FSK 3rd frequency deviation hold time [register value * clk (4MHz)]	0000_0000	R/W

[Description]

1. Setting the hold time of 3rd frequency deviation defined by [FSK_FDEV3:B0 0x5B] register.
2. For details, please refer to the “Programming FSK modulation”.

0x66[FSK_TIME2]

Function: FSK 2nd frequency deviation (FDEV2) hold time setting
Address: 0x66 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME2[7:0]	FSK 2nd frequency deviation hold time [register value * clk (4MHz)]	0000_0000	R/W

[Description]

1. Setting hold time of 2nd frequency deviation defined by [FSK_FDEV2:B0 0x5A] register.
2. For details, please refer to the “Programming FSK modulation”.

0x67[FSK_TIME3]

Function: FSK 1st frequency deviation (FDEV1) hold time setting
Address: 0x67 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME3[7:0]	FSK 1st frequency deviation hold time [register value * clk (4MHz)]	0000_0000	R/W

[Description]

1. Setting hold time of 1st frequency deviation defined by [FSK_FDEV2:B0 0x59] register.
2. For details, please refer to the “Programming FSK modulation”.

0x68[FSK_TIME4]

Function: FSK no-deviation frequency (carrier frequency) hold time setting
Address: 0x68 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FDEV_TIME4[7:0]	FSK no-deviation frequency hold time [register value * clk (4MHz)]	0000_0000	R/W

[Description]

1. Setting no deviation frequency hold time.
2. For details, please refer to the “Programming FSK modulation”.

0x69[PLL_MON/DIO_SEL]

Function: PLL lock detection signal output control and DIO mode configuration
Address: 0x69 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	000	R/W
6	INT_TIM_CTRL	Interrupt timing selection during Address filtering mode (*4) 0: The interrupt timing is same as ML7396. 1: The interrupt timing defined in ML7396B.	0	R/W
5	Reserved	Reserved	0	R/W
4	PLL_LD	DMON pin (#17), PLL lock signal output enable setting(*1) 0: disable 1: enable (output PLL lock signal)	0	R/W
3-2	Reserved	Reserved	00	R/W
1	DIO_EN	DIO mode enable setting (*2) 0: disable DIO mode (FIFO mode) 1: enable DIO mode	0	R/W
0	RX_FIFO_MON	RX data bit output mode enable setting(*3) 0: disable bit output mode 1: enable bit output mode	0	R/W

[Description]

*1 When output PLL lock signal from DMON pin (#17), please set CLKOUT_EN ([CLK_SET:B0 0x02(4)]) =0b0.

*2 If enabling this bit, the data interface with HOST MCU becomes DIO interface (DCLK pin (#16) and DIO pin (#15)) instead of TX/RX FIFO. In DIO mode the processing of preamble (defined by Bank0 0x39 register) and SFD (defined by Bank0 0x3A to 0x41 registers) are done automatically, and input/output the data following SFD field. DCLK output frequency depends on the data rate. Data input and output should be synchronized with DCLK output signal.
Dummy write access to the TX_FIFO is required in order to output TX DCLK. For details, please refer to the "TX mode (with DIO mode)" in the “Flow Charts”
When this bit is disabled, operating as FIFO and IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) setting will be valid.

*3 If enable this bit, demodulated data is output from DIO interface. However if setting DIO_EN=Ob1, demodulated data following SFD field are output.
During BER measurement, set DIO_EN=0b0 and RX_FIFO_MON=0b1.

*4 For details of the interrupt timing, please refer to the "Address filtering function."

0x6A[FAST_TX_SET]

Function: TX trigger level setting in FAST_TX mode
Address: 0x6a (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FAST_TX_TRG[7:0]	TX trigger level setting in FAST_TX mode Bit7=0b1: 128byte Bit6=0b1: 64byte Bit5=0b1: 32byte Bit4=0b1: 16byte Bit3=0b1: 8byte Bit2=0b1: 4byte Bit1=0b1: 2byte Bit0=0b1: 1byte if set 0x00: No FAST_TX mode	0000_0000	R/W

[Description]

1. FAST_TX mode is operating mode that will start transmission before FIFO is filled with TX data specified by Length field. The ML7396 will start transmission when FIFO is filled by amount of data specified by this register.
2. This function will be available if AUTO_TX ([PACKET_MODE_SET: B0 0x45(2)]) =0b1. If AUTO_TX=0b0, FAST_TX mode will be invalid.

[Note]

1. When transmitting over 256bytes TX data, FAST_TX mode should be used and this register should be set except for 0x00.
2. When using FAST_TX mode, FIFO writing speed should be faster than the data rate in order to avoid FIFO empty.
3. Setting value includes Length field.
4. When two or more bits are set enable, the most significant bit has priority.
5. When using FAST_TX mode, the period from transmission start (after writing data specified by FAST_TX_TRG[7:0]) to completion of data writing (negating SCEN), should be more than 150μs. If SCEN negate timing can not meet this condition, it might cause PLL unlock or unnecessary spurious emission.

0x6B[CH_SET]

Function: RF channel setting
Address: 0x6b (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	RF_CH[3:0]	RF channel setting (setting range: 0 to 15)	0000	R/W

[Note]

1. Please set the channel number enabled by [CH_EN_L:B0 0x2E] and [CH_EN_H:B0 0x2F] registers.

0x6C[RF_STATUS]

Function: RF state setting and status indication
Address: 0x6c (Bank 0)
Default Value: 0x88

Bit	Symbol	Description	Default Value	R/W
7-4	GET_TRX[3:0]	RF status indication 0110: RX_ON (receiving state) 1000: TRX_OFF (RF OFF state) 1001: TX_ON (transmitting state) Others: Reserved	1000	R
3-0	SET_TRX[3:0]	RF state setting 0011: Force_TRX_OFF (Force RF OFF) 0110: RX_ON (Enable RX) (*1) 1000: TRX_OFF (RF OFF) (*2) 1001: TX_ON (Enable TX) (*3) Others: Ignored, and no RF state transition.	1000	R/W

[Description]
*1 During TX operation, setting RX_ON is possible. In this case, after TX completion, move to RX_ON state automatically.
*2 If TRX_OFF is executed during TX or RX operation, RF will be turned OFF after TX or RX completion.
If Force_TRX_OFF is executed during TX or RX operation, RF will be turned OFF immediately.
*3 During RX operation, setting TX_ON is possible. In this case, after RX completion, move to TX_ON state automatically.
Regarding automatic TX mode setting, please refer to the description of AUTO_TX ([PACKET_MODE_SET:B0 0x45(2)]).

[Note]
1. If SFD is detected during TRX_OFF state transition, RX_ON is retained automatically.

0x6D[2DIV_ED_AVG]

Function: Average number setting for ED calculation during 2 diversity
Address: 0x6d (Bank 0)
Default Value: 0x01

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	2DIV_ED_AVG[2:0]	Average number of ED calculation during 2 diversity (*1)	001	R/W

[Description]
*1 Averaging number of times are shown in below table.

2DIV_ED_AVG[2:0]	averaging times
0b000	1
0b001 (Default Value)	2
0b010	4
0b011	8
0b100	15
0b101	16
others	8

0x6E[2DIV_GAIN_CNTRL]

Function: Gain control setting during 2 diversity
Address: 0x6e (Bank 0)
Default Value: 0x02

Bit	Symbol	Description	Default Value	R/W
7-2	TIM_TX_OFF2[5:0]	Ramp down timing adjustment when transitioning to RX_ON following TX_ON (*2) ([Set value] + 1) * 2.22μs	0000_00	R/W
1-0	2DIV_GAIN[1:0]	Gain control during 2 diversity (*1) 0b00: Fix High gain mode 0b01: Enable gain transition between High and Middle 0b10: Enable gain transition among High, Middle and Low 0b11: Fix High gain mode	10	R/W

[Description]
*1 Each gain switching threshold level are defined by register [GAIN_MtoL:B0 0x1C], [GAIN_LtoM:B0 0x1D], [GAIN_HtoM:B0 0x1E] and [GAIN_MtoH:B0 0x1F] registers .
*2 Valid when TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b1.
For details, please refer to the "Ramp control function"

[Note]
1. Please use the value specified in the “Initial register setting” file

0x6F[2DIV_SEARCH]

Function: 2 diversity search mode and search time setting
Address: 0x6f (Bank 0)
Default Value: 0x20

Bit	Symbol	Description	Default Value	R/W
7	SEARCH_MODE	2 diversity search mode. 0: Normal search 1: FAST search	0	R/W
6-0	SEARCH_TIME[6:0]	2 diversity search time setting (*1) Search period = ([set value] +1) * 1 [unit: bit]	010_0000	R/W

[Description]
1. In normal search, ED value detection will be performed for 2 antennas and select one of an antenna which has better ED value. In FAST search mode, if an antenna acquired ED value exceeds the ED threshold value specified by [2DIV_FAST_LV:B0 0x70] register, antenna searching will be terminated and the antenna will be selected.
2. Default value of 0x20 (=0d32) is 330μs in 100kbps setting.
3. For details of diversity operation, please refer to the “Diversity Function”.

[Note]
*1 SEARCH_TIME[6:0] should be greater than 0b010110(22 bit). Preamble length in TX packet is required minimum 12bytes (In 100kbps mode). Search time needs to be changed according to the data rate setting when the diversity function is used. Please use the value specified in the “Initial register setting” file.

0x70[2DIV_FAST_LV]

Function: Threshold level setting in 2 diversity mode.
Address: 0x70 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	2DIV_FAST_LV[7:0]	2 diversity FAST mode ED threshold level (0 to 255)	0000_0000	R/W

[Description]

1. This register will be valid if SEARCH_MODE ([2DIV_SERCH:B0 0x6F(7)]) =0b1.
2. When an antenna acquired ED value exceeds this threshold, the antenna will be selected and stop the search on the other antenna.

0x71[2DIV_CNTRL]

Function: 2 diversity setting
Address: 0x71 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	ANT_CTRL1	ANT control bit1	0	R/W
4	ANT_CTRL0	ANT control bit0	0	R/W
3	INV_ANT_SW	ANT_SW signal polarity setting 0: positive logic 1: negative logic	0	R/W
2	INV_TRX_SW	TRX_SW signal polarity setting 0: positive logic 1: negative logic	0	R/W
1	2PORT_SW	ANT_SW configuration setting 0: SPDT switch is used 1: DPDT switch is used	0	R/W
0	2DIV_EN	2 diversity enable setting 0: disable 2 diversity 1: enable 2 diversity	0	R/W

[Description]

1. For details, please refer to the “Diversity Function”.

The following table shows the output status of TRX_SW pin (#21) and ANT_SW pin (#20).

INV_TRX_SW (bit2)	2PORT_SW (bit1)	RF status	When TX_ANT_EN = 0b0 * 1		When TX_ANT_EN = 0b1 * 1	
			TRX_SW pin	ANT_SW pin	TRX_SW pin	ANT_SW pin
0b0	0b0 (SPDT)	RX(during CCA)	L	2DIV_RSLT *3	L	TX_ANT *2
		RX (not during CCA)				2DIV_RSLT *3
		TX	H		H	
	0b1 (DPDT)	RX (during CCA)	inverted ANT_SW	2DIV_RSLT *3	inverted ANT_SW	TX_ANT *2
		RX (not during CCA)				2DIV_RSLT *3
		TX		inverted 2DIV_RSLT		inverted 2DIV_RSLT
0b1	0b0 (SPDT)	RX (during CCA)	H	2DIV_RSLT *3	H	TX_ANT *2
		RX (not during CCA)				2DIV_RSLT *3
		TX	L		L	
	0b1 (DPDT)	RX (during CCA)	inverted ANT_SW	inverted 2DIV_RSLT	inverted ANT_SW	TX_ANT *2
		RX (not during CCA)				Inverted 2DIV_RSLT
		TX		2DIV_RSLT *3		2DIV_RSLT *3

* 1: please refer to the bit 5 in [2DIV_RSLT:B0 0x72] register.
* 2: Output depends on the TX_ANT ([2DIV_RSLT:B0 0x72(4)]) setting.
* 3: Output depend on the diversity result indicated by 2DIV_RSLT1/2 ([2DIV_RSLT:B0 0x72(1-0)]).
  If ANT1 is selected, output “L”, otherwise output “H”.

The antenna specified by diversity is cleared when one of the following conditions is satisfied.

- Clearing the RX completion interrupt (either INT[18] or INT[19] group3) after the packet reception.
- Clearing the diversity search completion interrupt. (INT[09] group2)
- After diversity search completion, diversity search is restarted due to fail of synchronization on selected antenna.

Therefore, when the diversity function is enabled, after packet reception is completed, clear the both RX completion interrupt and the diversity search completion interrupt. When reading the diversity search result, it must be done before clearing interrupts. When disabling the diversity search (set 2DIV_EN=0b0) before clearing the RX completion interrupt, the antenna status keeps the diversity result. When executing the TRX_OFF command, antenna status becomes the state specified by “RX (not during CCA)” in the above table.

The ANT_SW, TRX_SW, and DCNT (pin#22) functions are switched by the bit 5-3 settings as shown in below table.

ANT_CTRL[0] (bit4)	DCNT pin
0b0	External PA control signal (default function)
0b1	ANT control signal (ant_sw internal signal)

ANT_CTRL[1] (bit5)	TRX_SW pin	ANT_SW pin
0b0	Default function (refer the above table)	Default function (refer the above table)
0b1	ANT control signal (exclusive OR of internal signals trx_sw and ant_sw)	ANT control signal (ant_sw internal signal)

For details, please refer to the "Antenna switching function" in the “Diversity Function”.

[Note]
When enabling diversity function and execute RX_ON, the write access to this register is inhibited until generating the INT[11] ([INT_SOURCE_GRP2:B0 0x25(3)]).

0x72[2DIV_RSLT]

Function: 2 diversity result indication and forced antenna control setting
Address: 0x72 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	2DIV_DONE	2 diversity search completion status 0: on going (not started yet) 1: completion	0	R
6	Reserved	Reserved	0	R/W
5	TX_ANT_EN	Forced CCA/TX antenna enable setting (*1) 0: disable 1: enable	0	R/W
4	TX_ANT	CCA/TX antenna setting (*1) 0: Antenna1 1: Antenna2	0	R/W
3-2	Reserved	Reserved	00	R/W
1	2DIV_RSLT2	Antenna2 selected (*2) 1: selected	0	R/W
0	2DIV_RSLT1	Anternna1 selected (*2) 1: selected	0	R/W

[Note]

*1 When set TX_ANT_EN= 0b1, the antenna is selected by TX_ANT setting during TX_ON or CCA operation. This function is valid in TX_ON state or executing CCA by CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1. However, this function is invalid when moving to TX_ON state due to AutoAck function and CCA execution due to AutoAck function or address filtering function. By setting AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)])=0b0, this invalid state will be cleared.

*2 These two bits indicates the selected antenna status during diversity (Read only) or forced antenna setting (Write only). When setting to the 2DIV_RSLT2, the ANT_SW pin is set to the specified antenna. For details on the forced antenna setting, please refer to the following "About forced ANT_SW and TRX_SW pin setting."
Note: When using forced antenna setting, the setting value cannot be read.

The following table shows the antenna status indication without forced antenna setting.

Antenna status indication for each operation status

2DIV_EN (B0 0x71)	TX_ANT_EN	RF status	Antenna status indication
0b0	0b0	RX (not during CCA)	RX antenna (Default: antenna1)
		RX (during CCA)	RX antenna (Default: antenna1)
		TX	TX antenna (Default: antenna1)
	0b1	RX (not during CCA)	RX antenna (Default: antenna1)
		RX (during CCA)	Antenna set by TX_ANT
		TX	Antenna set by TX_ANT
0b1	0b0	RX (not during CCA)	Diversity result
		RX (during CCA)	Diversity result
		TX	TX antenna (Default: antenna1)
	0b1	RX (not during CCA)	Diversity result
		RX (during CCA)	Antenna set by TX_ANT
		TX	Antenna set by TX_ANT

The definitions of ANT1 and ANT2 are shown in the following antenna switch truth table. And INV_TRX_SW (bit2)=0b0, INV_ANT_SW (bit3)=0b0 and ANT_CTRL1 (bit5)=0b0) in the [2DIV_CNTRL:B0 0x71] register, are premised on the truth table.

SPDT switch

ANT_SW pin	Antenna
0	ANT1
1	ANT2

DPDT switch

TRX_SW (Pin #21)	ANT_SW (Pin #20)	ANT1-LNA_P connection	ANT1-PA_OUT connection	ANT2-LNA_P connection	ANT2-PA_OUT connection	antenna status
0	1	ON	OFF	OFF	ON	Receive: ANT1 Transmit: ANT2
1	0	OFF	ON	ON	OFF	Receive: ANT2 Transmit: ANT1

About forced ANT_SW and TRX_SW pin setting

When controlling the ANT_SW and TRX_SW pins forcibly, 2DIV_EN ([2DIV_CNTRL:B0 0x71(0)]) =0b0 and 2PORT_SW ([2DIV_CNTRL:B0 0x71(0)])=0b0 regardless of the used RF_SW type are required. And INT[09] ([INT_SOURCE_GRP2: B0 0x25(1)] should be 0b0. Under the above setting, the force settings shown in following tables are defined. Otherwise, out of scope for this function.

The ANT_SW pin output can be set by TX_ANT_EN (bit5) and 2DIV_RSLT2 (bit1) as shown in the following table.

Forced ANT_SW setting (with 2DIV_EN=0b0, 2PORT_SW=0b0, and INT[09]=0b0)

TX_ANT_EN	2DIV_RSLT2 (*1)	ANT_SW pin (Pin#20)
0	0b0	L
	0b1	H
1	0b0	L/ TX_ANT (bit4) setting (during TX or CCA operation)
	0b1	H/ TX_ANT(bit4) setting (during TX or CCA operation)

(*1) Any value written to 2DIV_RSLT1 (bit0) does not affect this setting.

The TRX_SW pin output can be set by INV_TRX_SW ([2DIV_CNTRL:B0 0x71(2)]) as shown in the following table.

Forced TRX_SW setting (with 2DIV_EN=0b0, 2PORT_SW=0b0, and INT[09]=0b0)

INV_TRX_SW [B0 0x71(2)]	TRX_SW pin (Pin #21)
0	L
1	H

[RF_CNTRL_SET:B0 0x75] register can also be used for forced setting. However, any forced setting function is disabled if 2PORT_SW ([2DIV_CNTRL:B0 0x71(1)]) =0b1. Here is the priority of the forced settings.

[RF_CNTRL_SET:B0 0x75] > INV_TRX_SW [B0 0x71(2)] > TX_ANT_EN/TX_ANT (during TX or CCA) > 2DIV_RSLT2

[Note]

Even if 2DIV_EN=0b1, 2DIV_RSLT2 can be written. However, if writing after diversity search completion, the antenna specified by the diversity search is changed. Forced setting is prohibited during RX.

0x73[ANT1_ED]

Function: Acquired ED value by antenna 1
Address: 0x73 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ED_ANT1[7:0]	Acquired ED value by antenna 1	0000_0000	R

[Description]

1. This register will be valid if 2DIV_EN ([2DIV_CONTL:B0 0x71(0)]) =0b1.
2. This register will be cleared when the diversity detection completion interrupt ([INT_SOURCE_GRP2:B0 0x25(1)]) is cleared or when the diversity search is restarted automatically.

0x74[ANT2_ED]

Function: Acquired ED value by antenna 2
Address: 0x74 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	ED_ANT2[7:0]	Acquired ED value by antenna 2	0000_0000	R

[Description]

1. This register will be valid if 2DIV_EN ([2DIV_CONTL:B0 0x71(0)]) =0b1
2. This register will be cleared when the diversity detection completion interrupt ([INT_SOURCE_GRP2:B0 0x25(1)]) is cleared or when the diversity search is restarted automatically.

0x75[RF_CNTRL_SET]

Function: RF control pin configuration (ANT_SW, TRX_SW, DCNT)
Address: 0x75 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserve	Reserved	0	R/W
6	DCNT_SET	DCNT pin (#22) forced output value setting. 0: “L” output 1: ”H” output	0	R/W
5	ANT_SW_SET	ANT_SW pin (#20) forced output value setting. 0: “L” output 1: ”H” output	0	R/W
4	TRX_SW_SET	TRX_SW pin (#21) forced output value setting 0: “L” output 1: ”H” output	0	R/W
3	Reserve	Reserved	0	R/W
2	DCNT_EN	DCNT forced control enable setting (1: enable)	0	R/W
1	ANT_SW_EN	ANT_SW forced control enable setting(1: enable)	0	R/W
0	TRX_SW_EN	TRX_SW forced control enable setting (1: enable)	0	R/W

[Description]

1. This register enables to set forced output value to ANT_SW pin (#20), TRX_SW pin (#21) and DCNT pin (#22). The forced setting by this register has priority and other control functions are ignored.
2. When controlling DCNT pin, please set EXT_PA_OUT ([PA_CNTRL:B1 0x07(5)]) =0b0 (CMOS output: Default Value).
3. When controlling ANT_SW pin, please set ANTSW_OUT ([SW_OUT/RAMP_ADJ:B1 0x08(7)]) =0b0 (CMOS output: Default Value).
4. When controlling TRX_SW pin, please set TRXSW_OUT ([SW_OUT/RAMP_ADJ:B1 0x08(6)]) =0b0 (CMOS output: Default Value).

0x76[Reserved]

0x77[CRC_AREA/FIFO_TRG]

Function: CRC calculation field and FIFO trigger setting
Address: 0x77 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-2	Reserve	Reserved	0000_00	R/W
1	CRC_AREA	CRC calculation field (*1) 0: following Length field (PHR excluded) 1: following SFD field (PHR included)	0	R/W
0	FIFO_TRG_EN	DMON pin (#17) FIFO trigger signal output enable setting. 0: disable 1: enable	0	R/W

[Note]

*1 It should beset 0b1when IEEE802.15.4d mode is selected by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b0.
*2 When output FIFO trigger signal from DMON pin (#17), please set CLKOUT_EN ([CLK_SET:B0 0x02(4)]) =0b0.

0x78[RSSI_MON]

Function: RSSI value indication
Address: 0x78 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R
5-0	RSSI[5:0]	RSSI A/D conversion value	00_0000	R

[Note]
1. ADC is shared with the temperature monitoring, this register value is undefined during the temperature information is being acquired.
2. Update cycle of this register is 17.8µs. 17.8µs is in case of ADC clock is 1.8MHz. if 2MHz is selected, update cycle will be 16.0µs. Please refer the [ADC_CLK_SET:B0 0x08] register.

0x79[TEMP_MON]

Function: Temperature indication
Address: 0x79 (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	TEMP[7:0]	Temperature A/D conversion value	0000_0000	R

[Note]
1. In case of measuring temperature, 75kohm of load resistance has to be attached to A_MON pin (#24), and set TEMP_ADC_OUT ([RSSI/TEMP_OUT:B1 0x03(5)]) =0b1.
2. Temperature measurement result can be acquired at all operating state except for sleep state.

0x7A[PN9_SET_L]

Function: PN9 initialized status setting/generated random number indication (low byte)
Address: 0x7a (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	PN9[7:0]	PN9 initialized status setting / random number indication (bit0 to bit7)	0000_0000	R/W

[Description]
1. Combined with together [PN9_SET_H:B0 0x7B] register, setting initialized status for whitening. Regarding this register, please refer to the [PN9_SET_H:B0 0x7B] register.

0x7B[PN9_SET_H]

Function: PN9 initialized status setting /generated random number indication (high 1bit) and PN9 enable control
Address: 0x7b (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	PN9_EN	PN9 enable control 0: stop PN9 generation 1: execute PN9 generation	0	R/W
6-1	Reserved	Reserved	000_000	R
0	PN9[8]	PN9 initialized status setting / random number indication (bit8)	0	R/W

[Description]

1. If PN9_EN=0b1, the PN9 circuit is used as the random number generator. The PN9 circuit generates random number synchronized with PHY_CLK. (PHY clock will be activated when CLK0_EN ([CLK_SET:B0 0x02(1)]) =0b1.
2. When reading random number (PN9[8:0]), please read them with burst access mode, please refer to the “SPI”.

[Note]

1. In the Whitening operation, initialized status of 0x1FF is applied automatically according to the IEEE 802.15.4g standard. There is no need to set these register.
   However, if set initial status with PN9_EN=0b0, the Whitening function uses the setting value as the initialized status.
2. The PN9 circuit shares setting with the Whitening function. While the Whitening function is running, please do not enable PN9 circuit (PN9_EN=0b1).

0x7C[RD_FIFO_LAST]

Function: FIFO remaining size or FIFO address indication
Address: 0x7c (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	FIFO_LAST[7:0]	FIFO remaining size (up to 255) or FIFO address	0000_0000	R

[Description]

1. Packet length (2bytes) will be read and written via FIFO, but Length field stored area is separated from data FIFO (256bytes), remaining size of FIFO will not count Length field size.
2. If FIFO_ADR_EN ([PACKET_MODE_SET:B0 0x45(7)]) =0b1, this register will indicate FIFO address.
3. Address of FIFO shows next address to write in TX, and next address to read in RX.
4. Remaining size of TX FIFO is only available during TX. Similarly, remaining size of RX FIFO is only available during RX.

[Note]

1. In the case of receiving over 256byte packet data, when reading a portion of data from the RX FIFO, please control the FIFO_LAST[7:0] must be more than or equal 0x01. After RX completion, do not care such procedure.

0x7D[Reserved]

0x7E[WR_TX_FIFO]

Function: TX FIFO
Address: 0x7e (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	TX_FIFO[7:0]	TX FIFO (bit0 to bit7)	0000_0000	W

[Note]

1. ML7396 has two 256byte FIFOs. However if IEEE 802.15.4d mode is selected by setting IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) = 0b0, the FIFO size will be fixed to 128 byte.
2. FIFO0 will be used at first. After that, ML7396 will manage which bank will be available to write.
3. Maximam 2 packets data will be stored independe from packet length. If both banks stores the data and the 3rd packet data is writteh to the FIFO, the TX FIFO access error interrupt (INT[15], group2) wil generate. If an access error occurs, please discard both FIFO data.
4. If writing TX data while receiving data, the TX data will be written in other bank of FIFO used for RX data.

0x7F[RD_RX_FIFO]

Function: RX FIFO
Address: 0x7f (Bank 0)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	RX_FIFO[7:0]	RX FIFO (bit0 to bit7)	0000_0000	R

[Note]

1. ML7396 has two 256byte FIFOs. However if IEEE 802.15.4d mode is selected by setting IEEE_MODE [PACKET_MODE_SET:B0 0x45(1)]) =0b0, the FIFO size will be fixed to 128 byte.
2. FIFO0 will be used at first. After that ML7396 will manage which bank will be available to write.
3. Maximum 2 packets data will be stored independent from packet length. If both banks stores the data and the 3rd packet data is stored into FIFO, the RX FIFO access error interrupt (INT[14] group2) will generate. If an access error occurs, please discard both FIFO data.

●Register BANK1

0x00[BANK_SEL]

Function: Register access bank selection
Address: 0x00 (Bank1)
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	TST_ACEN	Test register access enable (*2) 0: Access disable 1: Access enable	0	R/W
6-2	Reserved	Reserved	000_00	R/W
1-0	BANK[1:0]	BANK selection 0b00: Bank0 access 0b01: Bank1 access 0b10: Bank2 access 0b11: prohibit (*1)	00	R/W

[Note]

*1 When writing 0b11, avilable to return corrent bank by this register. Writing and reading registers are not available except fot this register.

*2 Regarding accessible registers by this bit, please refer the “register map” section.

0x01[DEMOD_SET]

Function: Demodulator setting
Address: 0x01 (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	BER_MODE_ON	BER measurement mode setting 0: normal reception mode 1: BER measurement mode	0	R/W
6-4	Reserved	Reserved	000	R/W
3	STR_HOLD_ON	Symbol timming recovery setting 0: constantly tracking symbol timing 1: after SFD detection, keeping symbol timing.	0	R/W
2	AFC_LIM_OFF	AFC limitter setting 0: turn on AFC limitter 1: turn off AFC limitter	0	R/W
1	AFC_HOLD_ON	AFC mode setting 0: constantly performing AFC 1: after SFD detection, turning off AFC	0	R/W
0	AFC_OFF	AFC_OFF enable setting 0: disable (performing AFC) 1: enable (not performing AFC)	0	R/W

0x02[RSSI_ADJ]

Function: RSSI value adjustment
Address: 0x02 (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	RSSI_ADD	Adjustment direction setting 0: decrease (set -) 1: increase (set +)	0	R/W
6-5	Reserved	Reserved	00	R/W
4-0	RSSI_ADJ[4:0]	RSSI adjustment value setting	0_0000	R/W

[Detail description]

1. For details, please refer to the “Energy Detection value (ED value) adjustment”.

0x03[RSSI/TEMP_OUT]

Function: Output setting for RSSI and Temperature data
Address: 0x03 (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	TEMP_ADC_OUT	Temperature digital output enable setting (*1) 0: disable 1: enable	0	R/W
4	TEMP_OUT	A_MON pin (#24), temperature analog output enable setting (*2) 0: disable 1: enable	0	R/W
3-1	Reserved	Reserved	000	R/W
0	RSSI_OUT	A_MON pin (#24), RSSI analog output enable setting (*2) 0: disable 1: enable	0	R/W

[Description]
*1 If set enable, temperature digital output can be read from [TEMP_MON:B0 0x79] register. Packet data is not able to recieve normally.
*2 If set enable, output signal can be monitored at A_MON pin (#24)

[Note]
1. Please do not set 0b1 at same time, correct value will not be output.

0x04[PA_ADJ1]

Function: PA adjustment 1st setting
Address: 0x04 (Bank1)
Default Value: 0x77

Bit	Symbol	Description	Default Value	R/W
7-4	PA_ADJ1_H[4:0]	20mW PA output gain adjustment setting.	0111	R/W
3-0	PA_ADJ1_L[4:0]	1mW PA output gain adjustment setting	0111	R/W

[Description]
1. For details, please refer to the “PA adjustment”
2. This register will be valid if PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]) =0b01.
3. When 20mW PA adjsutemnt, output power can be adjusted 0.1dB to 0.7dB per step and 2.5 to 3.5 dB in total range.
   When 1mW PA adjustment, output power can be adjusted 0.3 to 1.2dB per step and 10dB in total range.
   Coarse adjustment (approx. 0.5dB step) is available by [PA_REG_ADJ1:B1 0x33] register and fine adjustment (less than 0.1dB step) is also available by [PA_REG_FINE_ADJ:B1 0x13] register.
4. Adjustment step will depends on the supply voltage set by [PA_REG_ADJ1:B1 0x33] register.

0x05[PA_ADJ2]

Function: PA adjustment 2nd setting
Address: 0x05 (Bank1)
Default Value: 0x77

Bit	Symbol	Description	Default Value	R/W
7-4	PA_ADJ2_H[4:0]	20mW PA output PA gain adjustment setting	0111	R/W
3-0	PA_ADJ2_L[4:0]	1mW PA output gain adjustment setting	0111	R/W

[Description]

1. For details, please refer to the “PA adjustment”
2. This register will be valid if PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]) =0b10.
3. When 20mW PA adjustment, output power can be adjusted 0.1dB to 0.7dB per step and 2.5 to 3.5 dB in total range.
   When 1mW PA adjustment, output power can be adjusted 0.3 to 1.2dB per step and 10dB in total range.
   Coarse adjustment (approx. 0.5dB step) is available by [PA_REG_ADJ2:B1 0x34] register and fine adjustment (less than 0.1dB step) is also available by [PA_REG_FINE_ADJ:B1 0x13] register.
4. Adjustment step will dependes on the supply voltage set by [PA_REG_ADJ2:B1 0x34] register.

0x06[PA_ADJ3]

Function: PA adjustment 3rd setting
Address: 0x06 (Bank1)
Default Value: 0x77

Bit	Symbol	Description	Default Value	R/W
7-4	PA_ADJ3_H[4:0]	20mW PA output gain adjustment setting	0111	R/W
3-0	PA_ADJ3_L[4:0]	1mW PA output gain adjustment setting	0111	R/W

[Description]

1. For details, please refer to the “PA adjustment”
2. This register will be valid if PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]) =0b11.
3. When 20mW PA adjustment, output power can be adjusted 0.1dB to 0.7dB per step and 2.5 to 3.5 dB in total range.
   When 1mW PA adjustment, output power can be adjusted 0.3 to 1.2dB per step and 10dB in total range.
   Coarse adjustment (approx. 0.5dB step) is available by [PA_REG_ADJ2:B1 0x35] register and fine adjustment (less than 0.1dB step) is also available by [PA_REG_FINE_ADJ:B1 0x13] register.
4. Adjustment step will depends on the supply voltage set by [PA_REG_ADJ3:B1 0x35] register.

0x07[PA_CNTRL]

Function: External PA control and PA mode setting
Address: 0x07 (Bank1)
Default Value: 0x13

Bit	Symbol	Description	Default Value	R/W
7	EXT_PA_CNT	DCNT signal output timing setting 0: synchronized to TX_ON timing 1: synchronized to PA_ON timing	0	R/W
6	EXT_PA_INV	DCNT output polarity (*1) 0: postive logic 1: negative logic	0	R/W
5	EXT_PA_OUT	DCNT pin (#22) output mode setting 0: CMOS output 1: Open Drain output	0	R/W
4	PA_SEL	PA circuit selection (*2) 0: select 1mW PA 1: select 20mW PA	1	R/W
3-2	Reserves	Reserved	00	R/W
1-0	PA_ADJ_SEL[1:0]	PA adjustment register selection (*2) 0b00: Prohibited 0b01: Select PA_ADJ1/PA_REG_ADJ1 register setting 0b10: Select PA_ADJ2/PA_REG_ADJ2 register setting 0b11: Select PA_ADJ3/PA_REG_ADJ3 register setting	11	R/W

[Description]

1. External PA control signal will output from DCNT pin (#22).

*1 Thr polarity is applied to the setting of EXT_PA_EN ([SW_OUT/RAMP_ADJ:B1 0x08(4)]).
*2 For details of usage, please refer to the “PA adjustment”.

0x08[SW_OUT/RAMP_ADJ]

Function: ANT_SW/TRX_SW configuration and PA ramping up adjustment
Address: 0x08 (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	ANTSW_OUT	ANT_SW pin (#20) output mode setting 0: CMOS output 1:Open Drain output	0	R/W
6	TRXSW_OUT	TRX_SW pin (#21) output mode setting 0: CMOS output 1:Open Drain output	0	R/W
5	Reserved	Reserved	0	R/W
4	EXT_PA_EN	DCNT pin (#21) control settign 0: fixed to "L" 1: Control as EXT_PA Ouput "H" during TX_ON state, otherwise output "L"	0	R/W
3-0	RAMP_ADJ[3:0]	PA ramping up adjustment setting (*1) 0b0000: OFF (9μs) 0b0001: +10.1 μs : : 0b1111: +25.1 μs	0000	R/W

[Description]

*1 PA ramp up time can be adjusted approximately 1.1μs per step. At default (0b0000), pre-programmed timing (9 μs) is applied. By increasing value, ramping time will be extended.

0x09[PLL_CP_ADJ]

Function: PLL charge pump current adjustment
Address: 0x09 (Bank1)
Default Value: 0x44

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-4	PLL_CP_TX[2:0]	PLL charge pump current during TX	100	R/W
3	Reserved	Reserved	0	R/W
2-0	PLL_CP_RX[2:0]	PLL chage pump current during RX	100	R/W

0x0A[IF_FREQ_H]

Function: IF frequency setting (high byte)
Address: 0x0a (Bank1)
Default Value: 0x14 (IF frequency: 178.22kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ[15:8]	IF frequency setting (bit85 to bit15)	0001_0100	R/W

[Description]

1. Setting IF frequency. Combined together with [IF_FREQ_L:B1 0x0B] register.
2. According to the data rate defined by RATE[2:0] ([DATA_SET:B0 0x47(2-0)]), automatically multiplied. For details, please refer to the “Programing IF Frequency”.

[Note]

1. Inhibited NBO_SEL ([DATA_SET:B0 0x47(7)]) =0b1, except for 50/100/200kbps setting

0x0B[IF_FREQ_L]

Function: IF frequency setting (low byte)
Address: 0x0b (Bank1)
Default Value: 0x47 (IF Frequency: 178.22kHz)

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ[7:0]	IF frequency setting (bit0 to bit7)	0100_0111	R/W

[Description]

1. Regarding this register, please refer to the [IF_FREQ_H:B1 0x0A] register.

0x0C[IF_FREQ_CCA _H]

Function: IF frequency setting during CCA operation (high byte)
Address: 0x0c (Bank1)
Default Value: 0x14

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_CCA[15:8]	IF frequency setting during CCA operation (bit8 to bit15)	0001_0100	R/W

[Description]

1. Setting IF frequency during CCA operation. Combined together with [IF_FREQ_CCA_L:B1 0x0D] register.
2. According to the data rate defined by RATE[2:0] ([DATA_SET:B0 0x47(2-0)]), automatically multiplied. For details, please refer to the “Programing IF Frequency”.

0x0D[IF_FREQ_CCA_L]

Function: IF frequency setting during CCA operation (low byte)
Address: 0x0d (Bank1)
Default Value: 0x47

Bit	Symbol	Description	Default Value	R/W
7-0	IF_FREQ_CCA[7:0]	IF frequency setting during CCA operation (bit0 to bit7)	0100_0111	R/W

[Description]
1. Regarding this register, please refer to the [IF_FREQ_CCA_H:B1 0x0C] register.

0x0E[BPF_ADJ_H]

Function: Bandpass filter bandwidth adjustment (high 2bits)
Address: 0x0e (Bank1)
Default Value: 0x02

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	BPF_C[9:8]	Bandpass filter Bandwidth adjustment (bit8,bit9)	10	R/W

[Description]
1. Adjusting bandwidth of BPF during normal operation. Combined together with [BPF_ ADJ_L:B1 0x0F] register. For details, please refer to the “Programing BPF bandwidth”.

[Note]
1. Inhibited NBO_SEL ([DATA_SET:B0 0x47(7)]) =0b1, except for 50/100/200kbps setting

0x0F[BPF_ADJ_L]

Function: Bandpass filter bandwidth adjustment (low byte)
Address: 0x0f (Bank1)
Default Value: 0x04

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_C[7:0]	Bandpass filter bandwidth adjustment (bit0 to bit7)	0000_0100	R/W

[Description]
1. Regarding this register, please refer to the [BPF_ADJ_H:B1 0x0E] register.

0x10[BPF_CCA_ADJ_H]

Function: Bandpass filter bandwidth adjustment during CCA operation (high 2bits)
Address: 0x10 (Bank1)
Default Value: 0x01

Bit	Symbol	Description	Default Value	R/W
7-2	Reserved	Reserved	0000_00	R/W
1-0	BPF_C_CCA[9:8]	Bandpass filter Bandwidth adjustment during CCA operation (bit8, bit9)	01	R/W

[Description]

1. Adjusting bandwidth of BPF during CCA operation. Combined together with [BPF_CCA_ADJ_L:B1 0x11] register. For details, please refer to the “Programing BPF bandwidth”.

[Note]

1. Inhibited NBO_SEL ([DATA_SET:B0 0x47(7)]) =0b1, except for 50/100/200kbps setting

0x11[BPF_CCA_ADJ_L]

Function: Bandpass filter bandwidth adjustment during CCA operation (low byte)
Address: 0x11 (Bank1)
Default Value: 0x10

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_C_CCA[7:0]	Bandpass filter bandwidth adjustment during CCA operation (bit7 to bit0)	0001_0000	R/W

[Description]

1. Regarding this register, please refer to the [BPF_CCA_ADJ_H:B1 0x10] register.

0x12[RSSI_LPF_ADJ]

Function: RSSI lowpass filter adjustment
Address: 0x12 (Bank1)
Default Value: 0x1F

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	RSSI_LPF_R[5:0]	RSSI lowpass filter adjustment	01_1111	R/W

0x13[PA_REG_FINE_ADJ]

Function: PA regulator fine adjustment
Address: 0x13 (Bank1)
Default Value: 0x10

Bit	Symbol	Description	Default Value	R/W
7-5	Reserved	Reserved	0	R/W
4-0	PA_REG_ADJ[4:0]	PA regulator output voltage fine adjustment setting	001_0000	R/W

[Description]

1. PA output power can be adjusted less than 0.1dB per step. Fine adjustment function absorbs device variation with high accuracy.
2. 1step is corresponding to approximately 14mV.

0x14[IQ_MAG_ADJ]

Function: IF IQ amplitude balance adjustment
Address: 0x14 (Bank1)
Default Value: 0x08

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	IQ_CAL_LNA_EN	I/Q calibration test pattern enable setting for LNA block. 0: disable 1: enable	0	R/W
4	IQ_CAL_MIX_EN	I/Q calibration test pattern enable setting for Mixer block 0: disable 1: enable	0	R/W
3-0	MAG_TRM[4:0]	IQ signal amplitude balance adjustment	1000	R/W

[Description]

1. Image rejection can be adjusted by MAG_TRM[4:0]. For details, please refer to the “I/Q adjustment”.

0x15[IQ_PHASE_ADJ]

Function: IF I/Q phase balance adjustment
Address: 0x15 (Bank1)
Default Value: 0x20

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	IF_Q[5:0]	IQ signal phase balance adjustment	10_0000	R/W

[Description]

1. Image rejection can be adjusted by this register. For details, please refer to the “I/Q adjustment”.

0x16[VCO_CAL_MIN_FL]

Function: VCO calibration low limit frequency setting (F-counter low byte)
Address: 0x16 (Bank1)
Default Value: 0x55

Bit	Symbol	Description	Default Value	R/W
7-0	VCO_CAL_MIN_F[7:0]	VCO calibration low limit frequency (F-counter bit0 to bit7)	0101_0101	R/W

[Description]
1. For details of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO low limit frequency setting”.

[Note]
1. For low limit frequency, please set the frequency 2MHz lower than actual operating frequency.

0x17[VCO_CAL_MIN_FM]

Function: VCO calibration low limit frequency setting (F-counter middle byte)
Address: 0x17 (Bank1)
Default Value: 0x55

Bit	Symbol	Description	Default Value	R/W
7-0	VCO_CAL_MIN_F[15:8]	VCO calibration low limit frequency (F-counter bit8 to bit15)	0101_0101	R/W

[Description]
1. Regarding this register, please refer to the [VCO_CAL_MIN_FL:B1 0x16] register.

0x18[VCO_CAL_MIN_FH]

Function: VCO calibration low limit frequency setting (F-counter high 4bits)
Address: 0x18 (Bank1)
Default Value: 0x09

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	VCO_CAL_MIN_F[19:16]	VCO calibration low limit frequency (F-counter bit16 to bit19)	1001	R/W

[Description]
1. Regarding this register, please refer to the [VCO_CAL_MIN_FL:B1 0x16] register.

0x19[VCO_CAL_MAX_N]

Function: VCO calibration upper limit frequency setting
Address: 0x19 (Bank1)
Default Value: 0x07

Bit	Symbol	Description	Default Value	R/W
7-5	Reserved	Reserved	000	R/W
4-0	VCO_CAL_MAX_N[4:0]	VCO calibration upper limit frequency (ΔF) (*1) 0b0_0000: 1.125 MHz 0b0_0001: 2.25 MHz 0b0_0011: 4.5 MHz 0b0_0111: 9 MHz 0b0_1111: 18 MHz 0b1_1111: 36 MHz (*2) Others: 0 MHz	0_0111	R/W

[Description]
1. For details of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO upper limit frequency setting”.

[Note]
*1. For upper limit frequency, please set the frequency range that includes operating frequencies.
*2. It can be used only when VCO low limit frequency is “36MHz * n”.
(When set 0x00 to [VCO_CAL_MIN_FL:B1 0x16], [VCO_CAL_MIN_FM:B1 0x17], and [VCO_CAL_MIN_FH:B1 0x18] registers.)

0x1A[VCO_CAL_MIN]

Function: VCO caliburation low limit value indication and setting
Address: 0x1A (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-0	VCO_CAL_MIN[6:0]	VCO calibration low limit value	000_0000	R/W

[Description]
1. For details of VCO calibration usage, please refer to the “VCO adjustment”
2. After calibratio by [VCO_CAL_START:B1 0x1D] register, value will be saved automaticallyr.

0x1B[VCO_CAL_MAX]

Function: VCO caliburation upper limit value indication and setting
Address: 0x1b (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-0	VCO_CAL_MAX[6:0]	VCO calibration upper limit value	000_0000	R/W

[Description]
1. For details of VCO calibration usage, please refer to the “VCO adjustment”
2. After calibratio by [VCO_CAL_START:B1 0x1D] register, value will be saved automatically.

0x1C[VCO_CAL]

Function: VCO caliburation value indication or setting
Address: 0x1c (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7	CAL_WR_EN	VCO calibratiom mode setting0: automatic setting mode 1: forced writing mode	0	R/W
6-0	VCO_CAL[6:0]	Current VCO calibration value	000_0000	R/W

[Description]

1. For details of VCO calibration usage, please refer to the “VCO setting”
2. In automatic setting mode, current calibration value is indicated, VCO_CAL[6:0] value will be updated after issuing TX_ON or RX_ON by [RF_STATUS:B0 0x6c] register.
3. In forced writing mode (CAL_WR_EN=1b1), the value set to VCO_CAL[6:0] will be applied. (if CAL_WR_EN=0b0, the set value is ignored.

0x1D[VCO_CAL_START]

Function: VCO caliburation execution
Address: 0x1d (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-1	Reserved	Reserved	0000_000	R/W
0	VCO_CAL_START	Execute VCO calibration 0: execution completed 1: execution start	0	R/W

[Description]

1. For details of VCO calibration usage, please refer to the “VCO adjustment”

0x1E[BPF_ADJ_OFFSET]

Function: BPF adjustment offset value indication
Address: 0x1e (Bank1)
Default Value: 0xxx

Bit	Symbol	Description	Default Value	R/W
7-0	BPF_OFFSET_POL	Adjustment direction indication 0: decrease (set -) 1: increase (set +)	x	R
6:0	BPF_OFFSET[6:0]	BPF adjustment offset value	xxx_xxxx	R

[Description]

1. This register indicates the individual BPF adjustment offset value.
2. For details of this register usage, please refer to the “Programing BPF bandwidth”

0x1F-2A[Reserved]

0x2B[ID_CODE]

Function: ID code indication
Address: 0x2b (Bank1)
Default Value: 0x11 (Ml7396) / 0x12 (ML7396A/B) / 0x13 (ML7396D/E)

Bit	Symbol	Description	Default Value	R/W
7-0	LSI_ID[7:0]	ID code (LSI version) indication 0x11: ML7396 0x12: ML7396B, ML7396A 0x13: ML7396D, ML7396E	0001_0001 0001_0010 0001_0011	R

0x2C-32[Reserved]

0x33[PA_REG_ADJ1]

Function: PA regulator adjustment (1st setting)
Address: 0x33 (Bank1)
Default Value: 0x07

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	PA_REG_ADJ1 [2:0]	PA regulator adjustment	111	R/W

[Description]
1. For details, please refer to the “PA adjustment”.
2. This register will be valid if PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]) =0b01.
3. PA output can be adjusted approximately 0.5dB per step.
4. The output volatge from REG_PA (#28) will be adjusted approximately 0.1V per step.

[Note]
1. The minimum supply voltage to maintain TX power will be “REG_PA voltage +0.3V”.

0x34[PA_REG_ADJ2]

Function: PA regulator adjustment (2nd setting)
Address: 0x34 (Bank1)
Default Value: 0x07

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	PA_REG_ADJ2 [2:0]	PA regulator adjustment	111	R/W

[Description]
1. For details, please refer to the “PA adjustment”.
2. This register will be valid if PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]) =0b10.
3. PA output can be adjusted approximately 0.5dB per step.
4. The output volatge from REG_PA (#28) will be adjusted approximately 0.1V per step.

[Note]
1. The minimum supply voltage to maintain TX power will be “REG_PA voltage +0.3V”.

0x35[PA_REG_ADJ3]

Function: PA regulator adjustment (3rd setting)
Address: 0x35 (Bank1)
Default Value: 0x07

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2-0	PA_REG_ADJ3 [2:0]	PA regulator adjustment	111	R/W

[Description]

1. For details, please refer to the “PA adjustment”.
2. This register will be valid if PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]) =0b11.
3. PA output can be adjusted approximately 0.5dB per step.
4. The output volatge from REG_PA (#28) will be adjusted approximately 0.1V per step.

[Note]

1. The minimum supply voltage to maintain TX power will be “REG_PA voltage +0.3V”.

0x36-39[Reserved]

0x3A[PLL_CTRL]

Function: PLL setiing
Address: 0x3A (Bank1)
Initial value: 0x9F

Bit	Register Name	Description	Initial value	R/W
7-5	Reserved	Reserved	100	R/W
4	PLL_SD_PS	PLL frequency setting timing selection 0: falling edge of VCO clock 1: rising edge of VCO clock	1	R/W
3-0	Reserved	Reserved	1111	R/W

[Note]

1. When using one unit channel (200kHz) specified in ARIB STD-T108, set 0b0 in order to improve the ACP characteristics. When using more than two unit channels, both 0b0 and 0b1 can be set.

0x3B-3E[Reserved]

0x3F[RX_ON_ADJ2]

Function: RX_ON timing adjustment #2
Address: 0x3F (Bank1)
Defaultl value: 0x02

Bit	Register Name	Description	Default Value	R/W
7	Reserved	Reserved	0	R/W
6-4	TIM_RX_ON2[2:0]	State transition timing adjustment when transitioning from TX_ON to RX_ON. Transition timing = ([set value] + 1) * 8.88μs	000	R/W
3-0	Reserved	Reserved	0010	R/W

[Description]
1. For details, please refer to the "Ramp control function.

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x40-48[Reserved]

0x49[LNA_GAIN_ADJ_M]

Function: LNA gain adjustment during middle gain operation
Address: 0x49 (Bank1)
Default Value: 0x0E

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	LNA_MGAIN[5:0]	LNA gain adjustment during middle gain operation	00_1110	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x4A[LNA_GAIN_ADJ_L]

Function: LNA gain adjustment during low gain opration
Address: 0x4a (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5-0	LNA_LGAIN[5:0]	LNA gain adjustment during low gain operation	00_0000	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x4B-4C[Reserved]

0x4D[MIX_GAIN_ADJ_H]

Function: Mixer gain adjustment during high gain operation
Address: 0x4E (Bank1)
Initial value: 0xFF

Bit	Register Name	Description	Initial value	R/W
7-0	MIX_HGAIN[7:0]	Mixer gain adjustment during high gain operation	1111_1111	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x4E[MIX_GAIN_ADJ_M]

Function: Mixer gain adjustment during middle gain operation
Address: 0x4E (Bank1)
Default Value: 0xFF

Bit	Symbol	Description	Default Value	R/W
7-0	MIX_MGAIN[7:0]	Mixer gain adjustment during middle gain operation	1111_1111	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x4F[MIX_GAIN_ADJ_L]

Function: Mixer gain adjustment during low gain operation
Address: 0x4F (Bank1)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	MIX_LGAIN[7:0]	Mixer gain adjustment during low gain operation	0000_0000	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x50-54[Reserved]

0x55[TX_OFF_ADJ1]

Function: TX_OFF ramping down adjustment
Address: 0x55 (Bank1)
Initial value: 0x00

Bit	Register Name	Description	Initial value	R/W
7-0	TIM_TX_OFF1[7:0]	Ramp down timing adjustment when transitioning from TX_ON to TX_OFF ([set value] + 1) * 2.22µs	0000_0000	R/W

[Description]
1. This register will be valid when TXOFF_RAMP_EN ([RAMP_CNTRL: B2 0x2C(4)]) =0b1.
2. For details, please refer to the "Ramp control function.

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x56-59[Reserved]

0x5A[RSSI_SLOPE_ADJ]

Function: RSSI slope adjustment
Address: 0x5A (Bank1)
Default Value: 0x07

Bit	Symbol	Description	Default Value	R/W
7-4	Reserved	Reserved	0000	R/W
3-0	RSSI_SLOPE[3:0]	RSSI slope adjustment	0111	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x5B-7F[Reserved]

●Register BANK2

0x00[BANK_SEL]

Function: Register access bank selection
Address: 0x00 (Bank2)
Default Value 0x00

Bit	Symbol	Description	Default Value	R/W
7	TST_ACEN	Test register access enable (*2) 0: Access disable 1: Access enable	0	R/W
6-2	Reserved	Reserved	000_00	R/W
1-0	BANK[1:0]	BANK selection 0b00: Bank0 access 0b01: Bank1 access 0b10: Bank2 access 0b11: prohibit (*1)	00	R/W

[Note]
*1 When writing 0b11, avilable to return corrent bank by this register. Writing and reading registers are not available except fot this register.
*2 Regarding accessible registers by this bit, please refer the “register map” section.

0x01-11[Reserved]

0x12[SYNC_MODE]

Function: Bit synchronization mode setting
Address: 0x12 (Bank2)
Default Value: 0x04

Bit	Symbol	Description	Default Value	R/W
7-3	Reserved	Reserved	0000_0	R/W
2	SYNC_MODE	Bit synchronization mode setting*1 0: for BER measurement or enabling diversity 1: for disable diversity	1	R/W
1-0	Reserved	Reserved	00	R/W

[Description]
*1 During BER measurement or diversity search, bit synchronization mode should be changed since enough preamble length might not be achieved. Duting BER measurement or enabling diversity, SYNC_MODE should be set to 0b0, When diversity search is not used, even if SYNC_MODE=0b0, ML7396 set to 0b1automatically.

0x13-1D[Reserved]

0x1E[PA_ON_ADJ]

Function: PA_ON (internal signal) timing adjustment
Address: 0x1E (Bank2)
Default Value: 0x0A

Bit	Symbol	Description	Default Value	R/W
7-0	PA_ON_ADJ[7:0]	PA_ON signal timing adjustment ([set value] +1) * 8.88μs	0000_1010	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x1F[DAT_IN_ADJ]

Function: DATA enable (internal signal) timing adjustment
Address: 0x1F (Bank2)
Initial value: 0x1A

Bit	Register Name	Description	Initial value	R/W
7-0	DAT_IN_ADJ[7:0]	Data enable signal timing adjustment ([set value] + 1) * 1.11μs	0001_1010	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file. This setting is necessary only for 400kbps.

0x20-21[Reserved]

0x22[RX_ON_ADJ]

Function: RX_ON (internal signal) timing adjustment
Address: 0x22 (Bank2)
Default Value: 0x01

Bit	Symbol	Description	Default Value	R/W
7-0	RX_ON_ADJ[7:0]	RX_ON signal timing adjustment ([set value]+1) * 8.88μs	0000_0001	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x23[Reserved]

0x24[RXD_ADJ]

Function: RXD (internal signal) timing adjustment
Address: 0x24 (Bank2)
Default Value: 0x59

Bit	Symbol	Description	Default Value	R/W
7-0	RXD_ADJ[7:0]	RXD signal timing adjustment ([set value]+1) * 1.11μs	0101_1001	R/W

[Note]
1. Please use the value specified in the “Initial register setting” file.

0x25-29[Reserved]

0x2A[RATE_ADJ1]

Function: Demodulator adjustment for Optional data rate (other than 50/100/200/400kbps) (low byte)
Address: 0x2A (Bank2)
Initial value: 0x01

Bit	Register Name	Description	Initial value	R/W
7-0	RATE_ADJ[7:0]	Demodulator adjustment for optional data rate setting (low byte)	0000_0001	R/W

[Description]
1. Adjusting demodulator during optional data rate operation. Combined together with [RATE_ ADJ2:B2 0x2B] register.
2. Adjusting will be valid if RATE_ADJ_EN [RATE_ADJ2:B2 0x2B(4)]) =0b1.
3. Set as follows for 150kbps operation.

Receiving state	RATE_ADJ[9:0]
Not during CCA	0x2BE
During CCA	0x17C

[Note]
1. Please use the value specified in the “Initial register setting” file.
2. For 10kbps/20kbps/40kbps operation setting, please refer to the "Initial register setting" file.

0x2B[RATE_ADJ2]

Function: Optional data rate (other than 50/100/200/400kbps) setting and enable control (high 2 bits)
Address: 0x2B (Bank2)
Initial value: 0x01

Bit	Register Name	Description	Initial value	R/W
7-5	Reserved	Reserved	000	R/W
4	RATE_ADJ_EN	Demodulator adjustment for optional data rate enable setting 0: disable 1: enable	0	R/W
3-2	Reserved	Reserved	11	R/W
1-0	RATE_ADJ[9:8]	Demodulator adjustment for optional data rate setting (high 2 bits)	11	R/W

[Description]
1. Regarding this register, please refer to the [RATE_ADJ1:B2 0x2A] register.

0x2C[RAMP_CNTRL]

Function: Ramp control enable setting
Address: 0x2c (Bank2)
Default value: 0x00

Bit	Register Name	Description	Default Value	R/W
7-6	Reserved	Reserved	00	R/W
5	Reserved	Reserved	0	R/W
4	TXOFF_RAMP_EN	Ramp control enable 0: disable 1: enable	0	R/W
3-0	Reserved	Reserved	0000	R/W

[Description]

1. When enabling (TXOFF_RAMP_EN=0b1), the lamp down timing after the transmission will apply the value set to the TIM_TX_OFF2[5:0] ([2DIV_GAIN_CNTRL:B0 0x6E(7-2)]), and TIM_TX_OFF1[7:0] ([TX_OFF_ADJ1:B1 0x55(7-0)]).
2. For details, please refer to the "Ramp control function.

0x2D-5F[Reserved]

0x60[ADDFIL_CNTRL]

Function: Address filtering function setting
Address: 0x60 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-5	MASK_SET[2:0]	Byte mask setting during 64bit address mode (*1) [set value] bytes from the LSB are not taken into account in address checking.	000	R/W
4	SHT_ADD1_EN	Short address1 check enable setting (*2) 0: disable 1: enable	0	R/W
3	SHT_ADD0_EN	Short address 0 check enable setting (*3) 0: disable 1: enable	0	R/W
2	EXT_ADD_EN	64bit address check enable setting (*4) 0: disable 1: enable	0	R/W
1	PANID_EN	PANID check enable setting (*5) 0: disable 1: enable	0	R/W
0	IGB_EN	I/G bit check enable setting (*6) 0: disable 1: enable	0	R/W

[Description]

1. For details of adrress filtering function, please refer to the ”Address filtering function”.

*1 MASK_SET[2:0] will be valid whne EXT_ADD_EN=0b1. From the low byte of 64bit address, setting bytes are not taken into account in address checking.
*2 Receiving a packet only when its destination short address is match to the setting value to [SHT_ADDR1_L/H:B2 0x6D/6E] registers. When using short addrss checking, PANID_EN should be 0b1.
*3 Receiving a packet only when its destination short address is match to the setting value to [SHT_ADD0_L/H:B2 0x6B/6C] registers. When using short addrss checking, PANID_EN should be 0b1.
*4 Packet receiving on ly when its 64bit distination address is match to the setting vale to [64ADDR1:B2 0x63] to [64ADDR8:B2 0x6A] registers. Lower bytes can be masked by MASK_SET[2:0] setting.
*5 Receiving a packet only when its PANID is match to the setting value to [PANID_L:B2 0x61] and [PANID_H:B2 0x62] registers.
(Note: If PANID=0xxFFFF (Broadcasting), all packets are received)
*6 Valid when EXT_ADD_EN=0b1, receiving packet which I\G bit is set to 0b1(multicast).

[Remarks]

1. For more detail about I/G bit, please refere to the IEEE802.3 standard. I/G: Individula/Group
2. I/G bit is allocated at bit0 of 1st octet in OUI field of MAC address. (57th bits in 64bit address). It will indicate following MAC address type. (0: unicast, 1: multicast)

0x61[PANID_L]

Function: PANID setting for address filtering function (low byte)
Address: 0x61 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	PANID[7:0]	PANID setting (bit0 to bit7)	0000_0000	R/W

[Description]

1. Setting PANID using for address checking function. Combined together with [PANID_H:B2 0x62] register.
2. These register will be valid if PANID_EN ([ADDFIL_CNTRL:B2 0x60(1)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x62[PANID_H]

Function: PANID setting for address filtering function (high byte)
Address: 0x62 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	PANID[7:0]	PANID setting (bit8 to bit15)	0000_0000	R/W

[Description]

1. Regarding this register, please refer to the [PANID_L:B2 0x61] register.

0x63[64ADDR1]

Function: 64bit address setting for address filtering function (1st byte lowest byte)
Address: 0x63 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[7:0]	64 bitAddress setting (bit0 to bit7)	0000_0000	R/W

[Description]

1. Setting 1st octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x64[64ADDR2]

Function: 64bit address setting for address filtering function (2nd byte)
Address: 0x64 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[15:8]	64 bitAddress setting (bit8 to bit15)	0000_0000	R/W

[Description]

1. Setting 2nd octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x65[64ADDR3]

Function: 64bit address setting for address filtering function (3rd byte)
Address: 0x65 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[23:16]	64 bitAddress setting (bit16 to bit23)	0000_0000	R/W

[Description]

1. Setting 3rd octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x66[64ADDR4]

Function: 64bit address setting for address filtering function (4th byte)
Address: 0x66 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[31:24]	64 bitAddress setting (bit24 to bit31)	0000_0000	R/W

[Description]

1. Setting 4th octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x67[64ADDR5]

Function: 64bit address setting for address filtering function (5th byte)
Address: 0x67 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[39:32]	64 bit address setting (bit32 to bit39)	0000_0000	R/W

[Description]

1. Setting 5th octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x68[64ADDR6]

Function: 64bit address setting for address filtering function (6th byte)
Address: 0x68 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[47:40]	664 bit address setting (bit40 to bit47)	0000_0000	R/W

[Description]

1. Setting 6th octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x69[64ADDR7]

Function: 64bit address setting for address filtering function (7th byte)
Address: 0x69 (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[55:47]	64 bit address setting (bit48 to bit55)	0000_0000	R/W

[Description]

1. Setting 7th octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x6A[64ADDR8]

Function: 64bit address setting for address filtering function (8th byte)
Address: 0x6A (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	64ADDR[63:56]	64 bit address setting (bit55 to bit63)	0000_0000	R/W

[Description]

1. Setting 8th octet of 64bit address.
2. This register will be valid if EXT_ADD_EN ([ADDFIL_CNTRL:B2 0x60(2)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x6B[SHT_ADDR0_L]

Function: Short address #0 (16bits) setting for address filtering function (low byte)
Address: 0x6b (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR0[7:0]	Short address #0 setting (bit0 to bit7)	0000_0000	R/W

[Description]

1. Setting short address #0 using for address checking function. Combined together with [SHT_ADDR0_H:B2 0x6C] register.
2. These register will be valid if SHT_ADD0_EN ([ADDFIL_CNTRL:B2 0x60(3)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x6C[SHT_ADDR0_H]

Function: Short address #0 (16bits) setting for address filtering function (high byte)
Address: 0x6c (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR0[15:8]	Short address #0 setting (bit8 to bit15)	0000_0000	R/W

[Description]

1. Regarding this register, please refer to the [SHT_ADDR0_L:B2 0x6B] register.

0x6D[SHT_ADDR1_L]

Function: Short address #1 (16bits) setting for address filtering function (low byte)
Address: 0x6d (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR1[7:0]	Short address1 setting (bit0 to bit7)	0000_0000	R/W

[Description]

1. Setting short address #1 using for address checking function. Combined together with [SHT_ADDR1_H:B2 0x6E] register.
2. These register will be valid if SHT_ADD1_EN [ADDFIL_CNTRL:B2 0x60(4)]) =0b1.
3. For details of adrress filtering function, please refer to the “Address filter function”.

0x6E[SHT_ADDR1_H]

Function: Short address1 (16bits) setting for address filtering function (high byte)
Address: 0x6e (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	SHT_ADDR1[15:8]	Short address1 setting (bit8 to bit15)	0000_0000	R/W

[Description]

1. Regarding this register, please refer to the [SHT_ADDR1_L:B2 0x6D] register.

0x6F[DISCARD_COUNT_L]

Function: Discarded packet number indication by address filtering (low byte)
Address: 0x6f (Bank2)
Default Value: 0x00

Bit	Symbol	Description	Default Value	R/W
7-0	DISCARD[7:0]	Discarded packet number by address filtering (bit0 to bit7)	0000_0000	R

[Description]

1. Indicating the number of discarded packets by address checking function. Combined together with [DISCARD_COUNT_H:B2 0x70] register. Maximum count is 1023.
2. Count value can be cleared by RST_3 ([RST_SET:B0 0x01(3)]) =0b1.(PHY reset execution)
   Count value is also cleared by disabling the address filter function. (set [ADDFIL_CTRL:B0 0x60] = 0x00)
3. For details of adrress filtering function, please refer to the “Address filter function”.
   When the address filter is disabled, this register is cleared to 0.

0x70[DISCARD_COUNT_H]

Function: Discarded packet number indication by address filtering (high byte)
Address: 0x6f (Bank2)
Default Value: 0x00

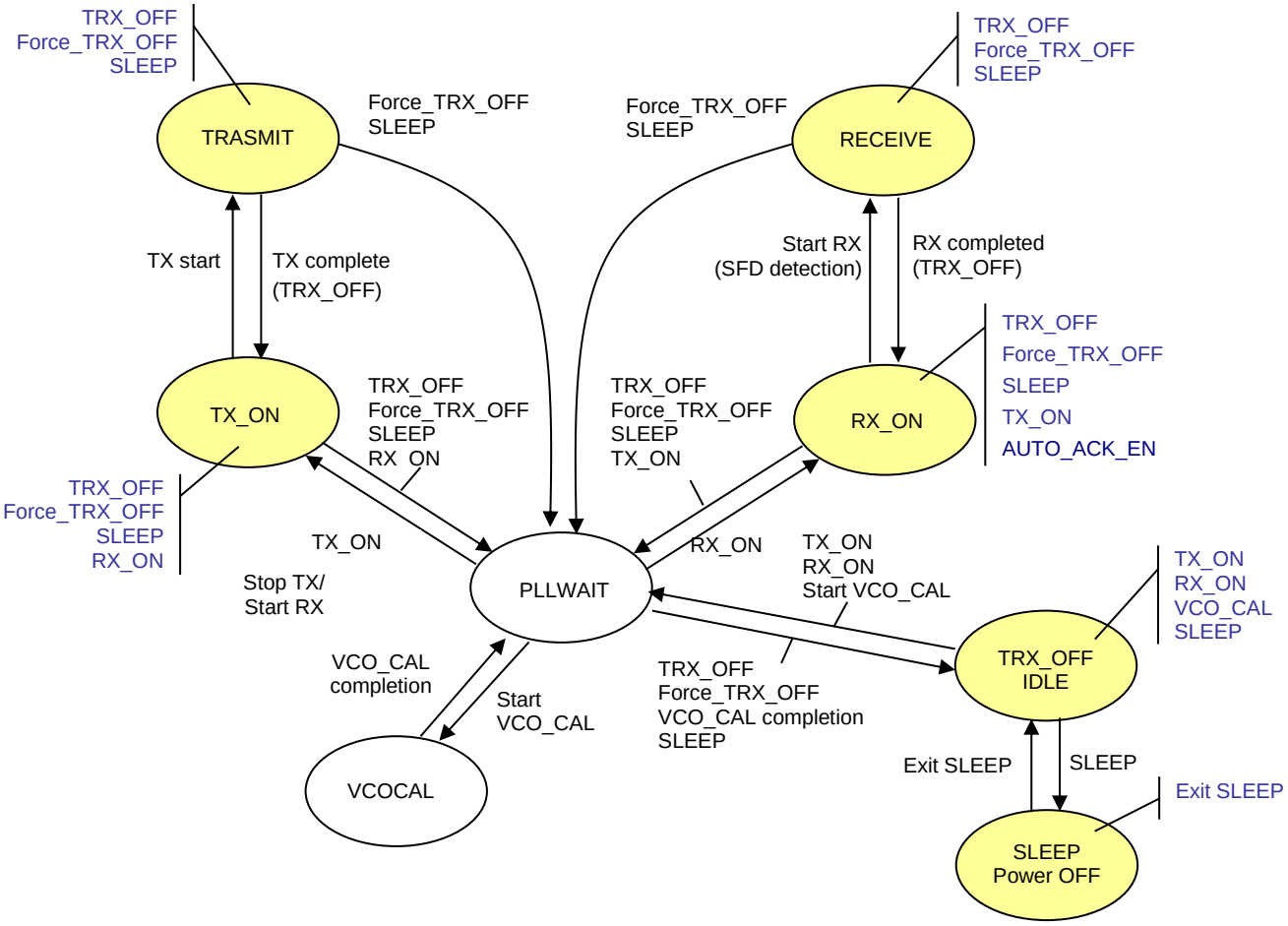
Bit	Symbol	Description	Default Value	R/W
7-0	DISCARD[15:8]	Discarded packet number by address filtering (bit8 to bit15)	0000_0000	R

[Description]

1. Regarding this register, please refer to the [DISCARD_COUNT_L:B2 0x6F] registe”

0x71-7F[Reserved]

■State Diagram



[State]

SLEEP/Power OFF	:SLEEP
TRX_OFF/IDLE	:IDLE (TX-RX stand-by)
PLL_WAIT	:PLL stand-by
TX_ON	:TX ready (TX data waiting)
TRANSMIT	:TX on-going
RX_ON	:RX readt (RX data waiting)
RECEIVE	:RX in process
VCO_CAL	:VCO calibration on going

State Transition instruction

Normal sequence
(State transition)

Control from upper layer

ML7396 self controlled
state transition

■Functional Description

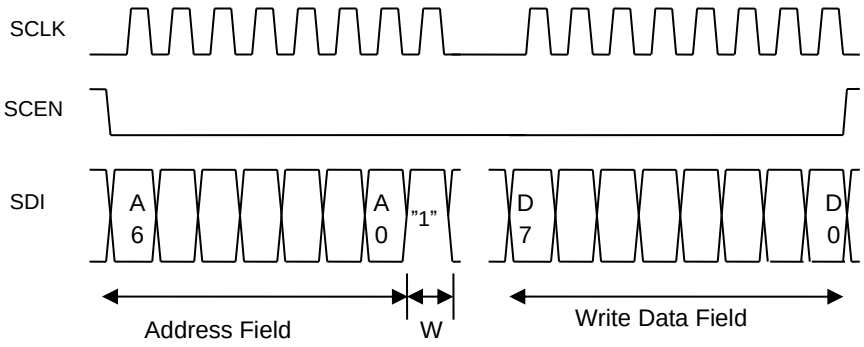
●SPI

ML7396 family has a Serial Peripheral Interface (SPI), which supports slave mode. Host MCU can read/write to the ML7396 registers and on-chip FIF using MCU clock. Single access mode and burst access mode are also supported.

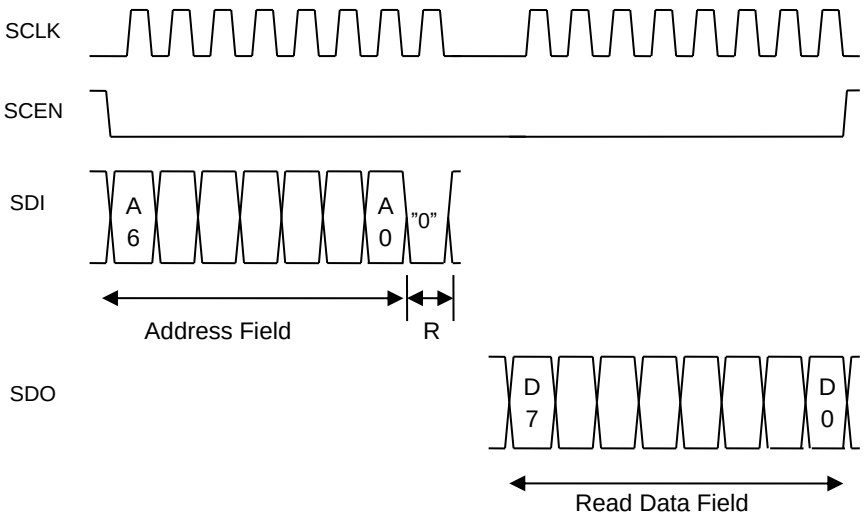
[Single access mode]

In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 data. During write operation, if setting SCEN line to “H”, the data will not be sotred into register.

[Write]



[Read]



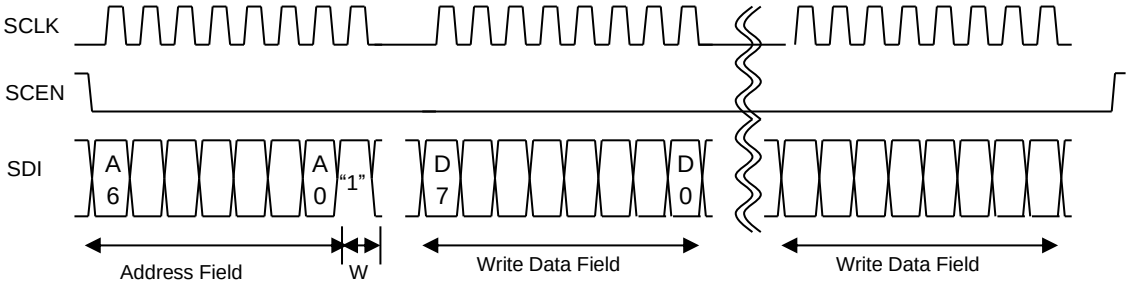
[Note]

When using IEEE802.15.4d mode, it is need to read “Length+1” bytes of data from RX FIFO for switching the FIFO banks correctly. After reading Lngth bytes of data, need to access [RD_RX_FIFO:B0 0x7F] register once more. (The last byte is invalid data.)

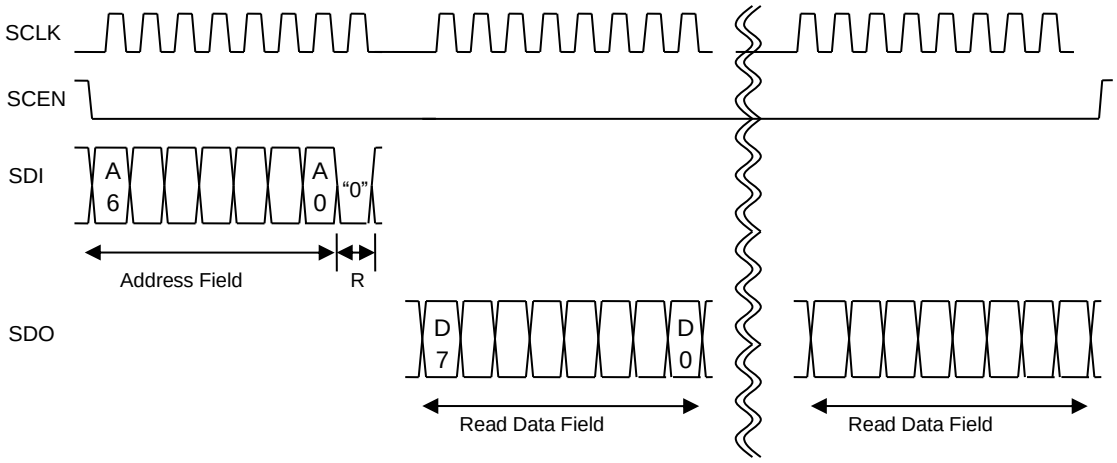
[Burst access mode]
By maintaining SCEN as L, Burst access mode will be active. By setting SCEN line to “H”, exiting from the burst access mode. During burst access mode, address will be automatically incremented.
When SCEN become H before Clock for D0 is input, data transaction will be aborted.

[Note]
If destination is [WR_TX_FIFO:B0 0x7E] or [RD_RX_FIFO:B0 0x7F] register, address will not be incremented. And continuous FIFO access is possible.

[Write]



[Read]



[Note]
When using IEEE802.15.4d mode, it is need to read “Length+1” bytes of data from RX FIFO for switching the FIFO banks correctly. (The last byte is invalid data.)

●AFC function

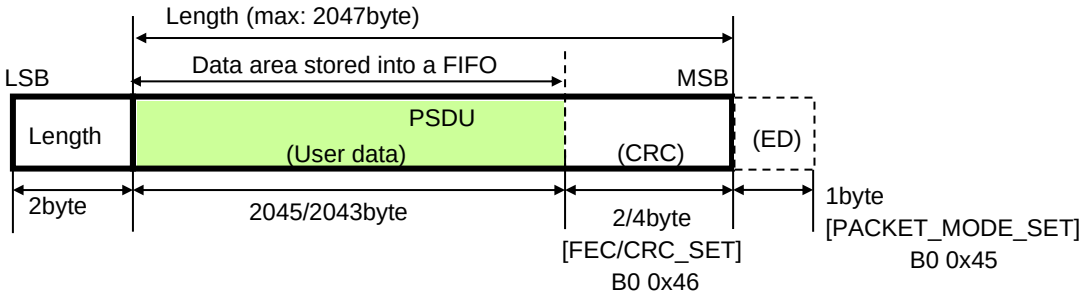
ML7396 family supports AFC function during RX operation. Frequency deviation (max +/- 20ppm) between remote device and local device can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved.
This function can be activated by setting AFC_EN ([AFC_CNTRL:B0 0x34(0)]) =0b1
This is not supported for optional data rate. (other than 50/100/150/200/400kbps) When using optional data rate, AFC_EN should be set to 0b0.

●FIFO

ML7396 family has on-chio two 256byte FIFOs as TX -RX buffer. However, one FIFO can store only one packet. (one packet cannot use two FIFOs).
During RX, RX data is stored in a FIFO (byte by byte), and the host MCU wil read RX data through SPI. Duting TX, the host MCU write TX data to a FIFO (byte by byte) through SPI and tenasmitting through RF.

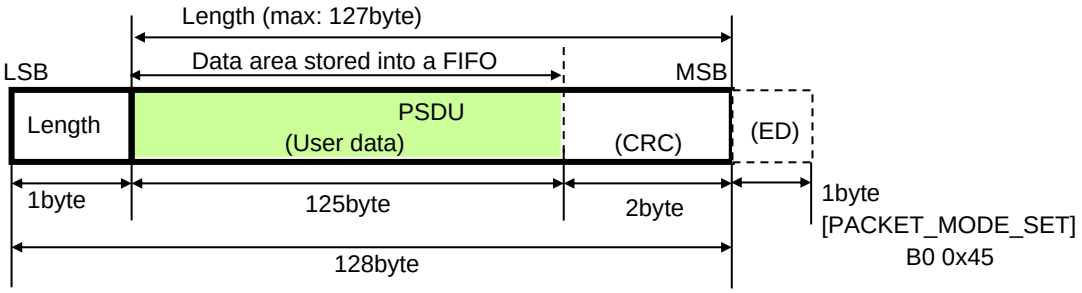
Followings show the data format stored in FIFO.
As described below, input data format will be different according to the setting value to IEEE_MODE ([PACKET MODE_SET:B0 0x45(1)]). (Regardless of IEEE_MODE, preamble and SFD bits are not stored into FIFOs)

[IEEE802.15.4g mode] (IEEE_MODE =0b1)



[Note; Length, CRC and ED value will be stored into data strage area other than FIFO.]

[IEEE802.15.4d mode] (IEEE_MODE =0b0)



[Note; Length, CRC and ED value will be stored into data strage area other than FIFO.]

Writeing or reading FIFO will be done through SPI with burst access. TX data is written to [WR_TX_FIFO:B0 0x7E] register, and RX data is read from [RD_RX_FIFO:B0 0x7F] register. Continuous access increments internal FIFO address automatically. If burst access is suspended during write or read operation, address will be kept until the packet will beagain.

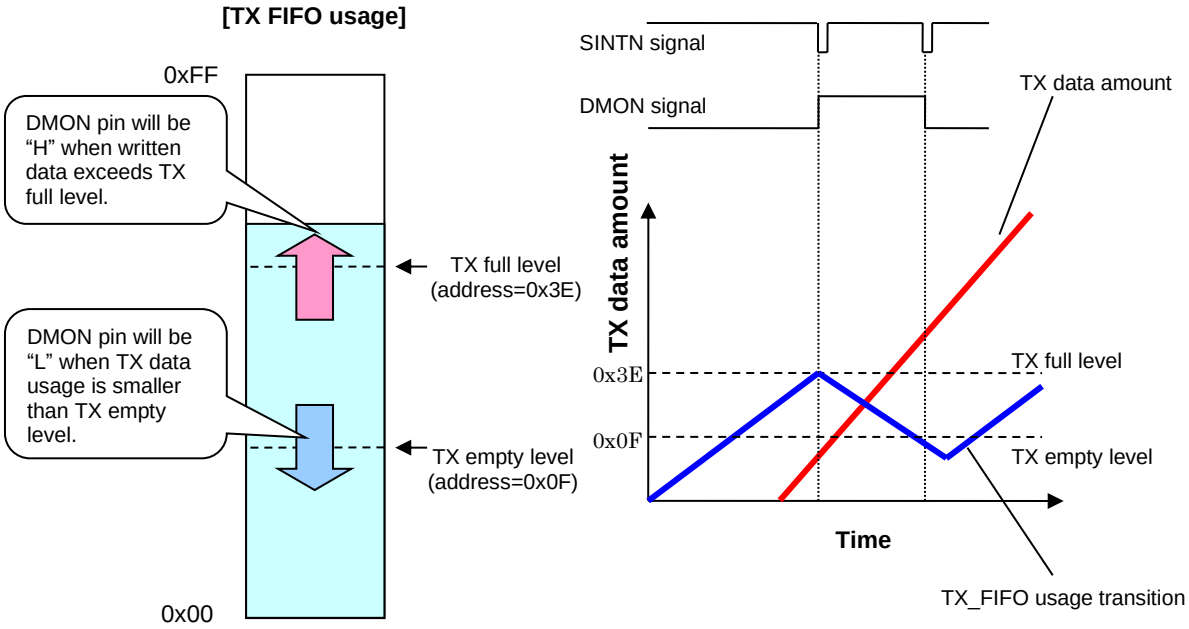
Two FIFOs (bank0, bank1) will be accessed one by another. If the host MCU writes TX data to a FIFO during RX, RX FIFO will use only single FIFO. Control of switching FIFO banks will be done automatically. FIFO status can be checked by [PD_DATA_REQ:B0 0x28] or [PD_DATA_IND:B0 0x29] register.

[Note]
1. When using IEEE802.15.4d mode, it is need to read "Length+1" bytes of data from RX FIFO for switching the FIFO banks correctly. (The last byte is invalid data.)
2. In both TX and RX, Length indicates PSDU length including CRC field. (not including ED fieled if selected)
   However during TX, the host MCU writes PSDU excluding CRC field to a FIFO. During RX, the host MCU should read Lngth field, user data field and CRC fieled from a FIFO.

○TX FIFO usage notification function

This function is to notice un-transmitted data in TX_FIFO (FIFO usage) to the MCU using SINTN (interrupt) pin (#10) and/or DMON pin (#17). If un-transmitted data in TX_FIFO (FIFO usage) exceeds the full level threshold set by [TX_ALARM_LH:B0 0x35] register, SINTN pin will become “L” (FIFO-Full interrupt) and/or DMON pin will become “H”. And if the TX_FIFO usage is equal to or less than the empty threshold level set by [TX_ALARM_HL:B0 0x36] register, SINTN will become “L” (FIFO-Empty interrupt) and/or DMON pin will become ”L”.

If re-generating the FIFO-Full interrupr (INT[05], group1), after clearing the interrupt, once the TX_FIFO usage should be equal or less than the empty level. If re-generating the FIFO-Empty interrupt (INT[04], group1), after clearing the interrupt, one the TX_FIFO usage excceds the full level threshold.



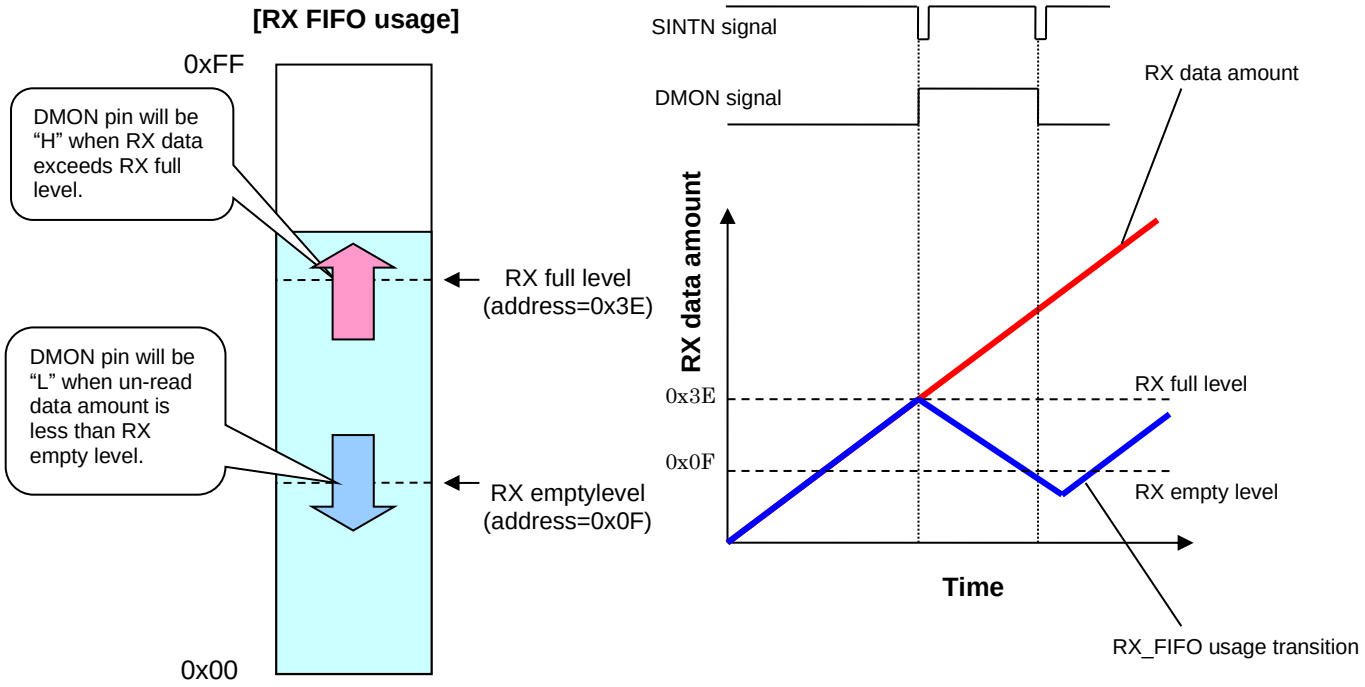
[Note]

1. At default setting, DMON pin is configured as CLKOUT output. If using DMON pin as this function, CLKOUT_EN ([CLK_SET:B0 0x02(4)]) =0b0 and FIFO_TRG_EN ([CRC_AREA/FIFO_TRG:B0 0x77(0)])=0b1 are required.
2. Each threshold should set as [TX_ALARM_LH:B0 0x35] (full level) > [TX_ALARM_HL:B0 0x36] (empty level).

○RX FIFO usage notification function

This function is to notice un-read data in RX_FIFO (FIFO usage) to the MCU using SINTN (interrupt) pin (#10) and/or DMON pin (#17). If un-read data in RX_FIFO (FIFO usage) exceeds the full level threshold set by [RX_ALARM_LH:B0 0x37] register, SINTN pin will become “L” (FIFO-Full interrupt) and/or DMON pin will become “H”. And if the RX_FIFO usage is equal to or less than the empty threshold level set by [RX_ALARM_HL:B0 0x38] register, SINTN will becom “L” (FIFO-Empty interrupt) and/or DMON pin will become “L”.

If re-generating the FIFO-Full interrupr (INT[05], group1), after clearing the interrupt, once the RX_FIFO usage should be equal or less than the empty level. If re-generating the FIFO-Empty interrupt (INT[04], group1), after clearing the interrupt, one the RX_FIFO usage excceds the full level threshold.



[Note]

1. At default setting, DMON pin is configured as CLKOUT output. If using DMON pin as this function, CLKOUT_EN ([CLK_SET:B0 0x02(4)]) =0b0 and FIFO_TRG_EN ([CRC_AREA/FIFO_TRG:B0 0x77(0)]) =0b1 are required.
2. Each threshold should set as [RX_ALARM_LH:B0 0x37] (full level) > [RX_ALARM_HL:B0 0x38] (empty level).
3. If reading a portion of RX data from a FIFO before receiving RX completion interrupt (INT[18]/INT[19] group3), please keep the FIFO remaining size indicated by [RD_FIFO_LAST:B0 0x7C] should be more than 0x01.
4. This function is valid only when data receiving. After RX completion, FIFO-Empty interrupt (INT[04] group1) is not generated.

○FIFO control method when using FIFO address

(1) TX

Condition: AUTO_TX ([PACKET_MODE_SET:B0 0x45(2)]) =0b1 and FIFO access size is 128 bytes.① Set [FAST_TX_SET;B0 0x6A] register and FIFO_ADR_EN ([PACKET_MODE_SET:B0 0x45(7)]) =0b1.

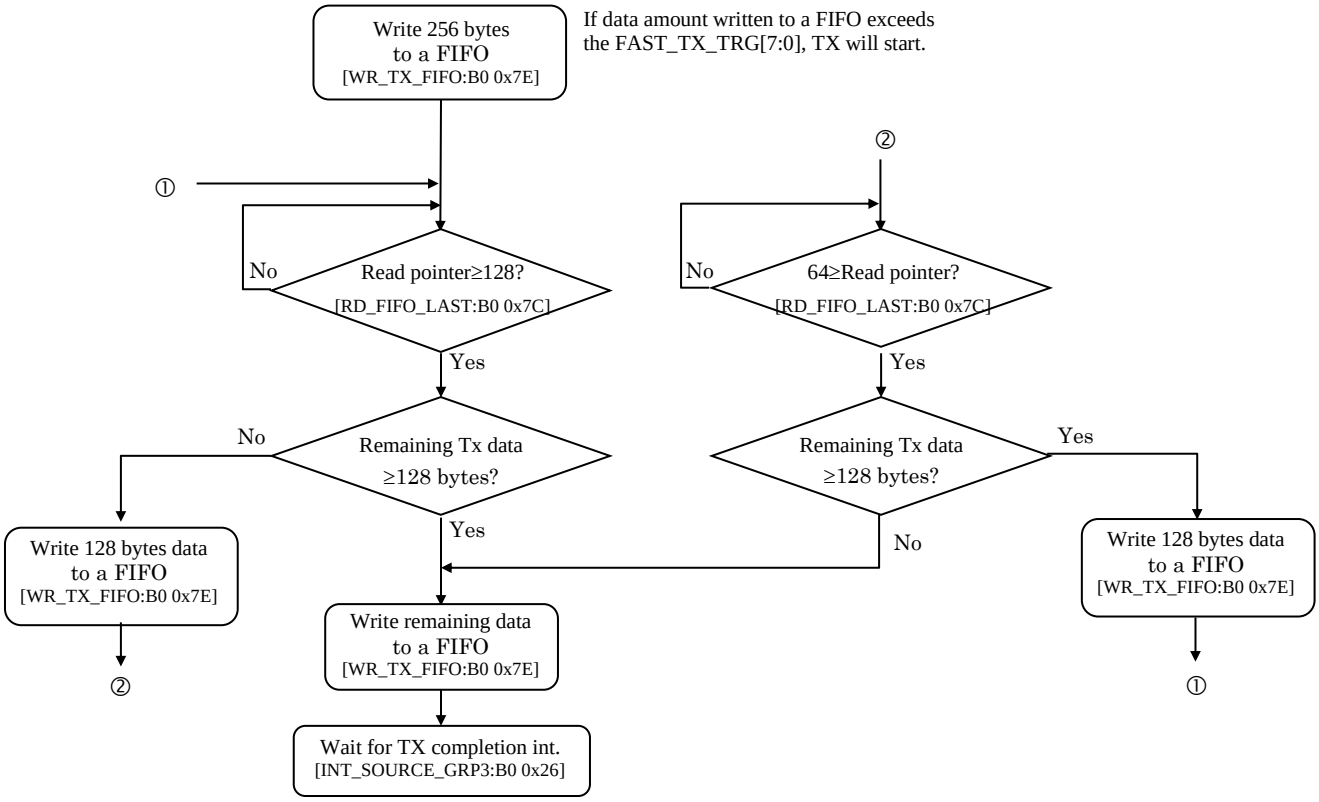
② Write256 bytesdata to FIFO ([WR_TX_FIFO:B0 0x7E] register) via SPI interface.

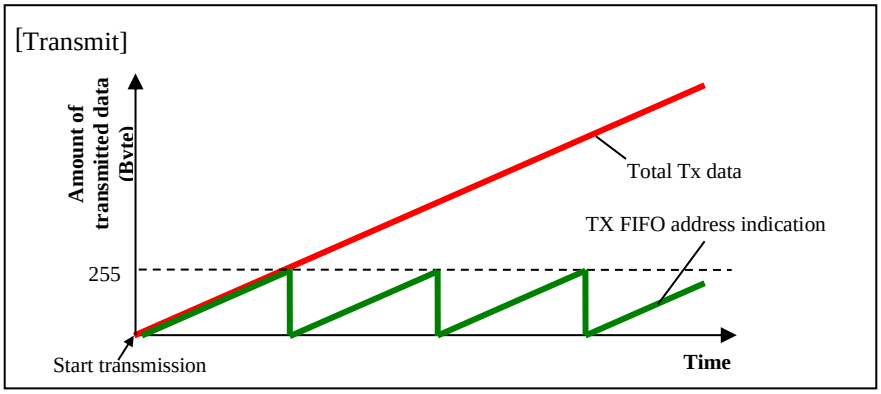
* When the amount of written data reaches [FIFO_TX_SET:B0 0x6A] register, transmission starts.③ Read [RD_FIFO_LAST:B0 0x7C] register. When FIFO address indication (hereafter, Read pointer) is 128 or more and the remaining TX data is 128 bytes or more, writing 128 bytes data to FIFO. If remaining TX data is less than 128 bytes, go to ⑥.

④ Read [RD_FIFO_LAST] register. When Read pointer is 64 or less and the remaining Tx data is 128 bytes or more, writing 128 bytes data to FIFO. If remaining TX data is less than 128 bytes, go to ⑥.

⑤ Repeat ③ and ④ until for the necessary amount of TX data.

⑥ Writing whole remaining data to FIFO and wait TX completion interrupt (INT[16] / INT[17], group3) notification.





TX FIFO address indication (read pointer) increments after Tx start.
After transimitting 256th byte data, the address indication is turned to 0 and increments again.

(2) RX (FIFO access size is 128 bytes)

① Set FIFO_ADR_EN ([PACKET_MODE_SET:B0 0x45(7)]) =0b1, and issuing RX_ON by [RF_STATUS:B0 0x6C] register. (RX start)

② Read [RD_FIFO_LAST:B0 0x7C] register. When FIFO address indication (hereafter, Write pointer) is 5 or more, read 5 bytes from FIFO ([RD_RX_FIFO:B0 0x7F] register). At this time, if the Length field is less than 5, this paclet does not meet IEEE802.15.4 requirement of the minimum packet length, the the packet might be discarded. (* It is not applied when using an original packet format other than IEEE802.15.4.) When it is equal to or more than 5 and less than 128, wait RX completion interrupt (INT[18]/[19] group3) and then read out the remaining data from FIFO.

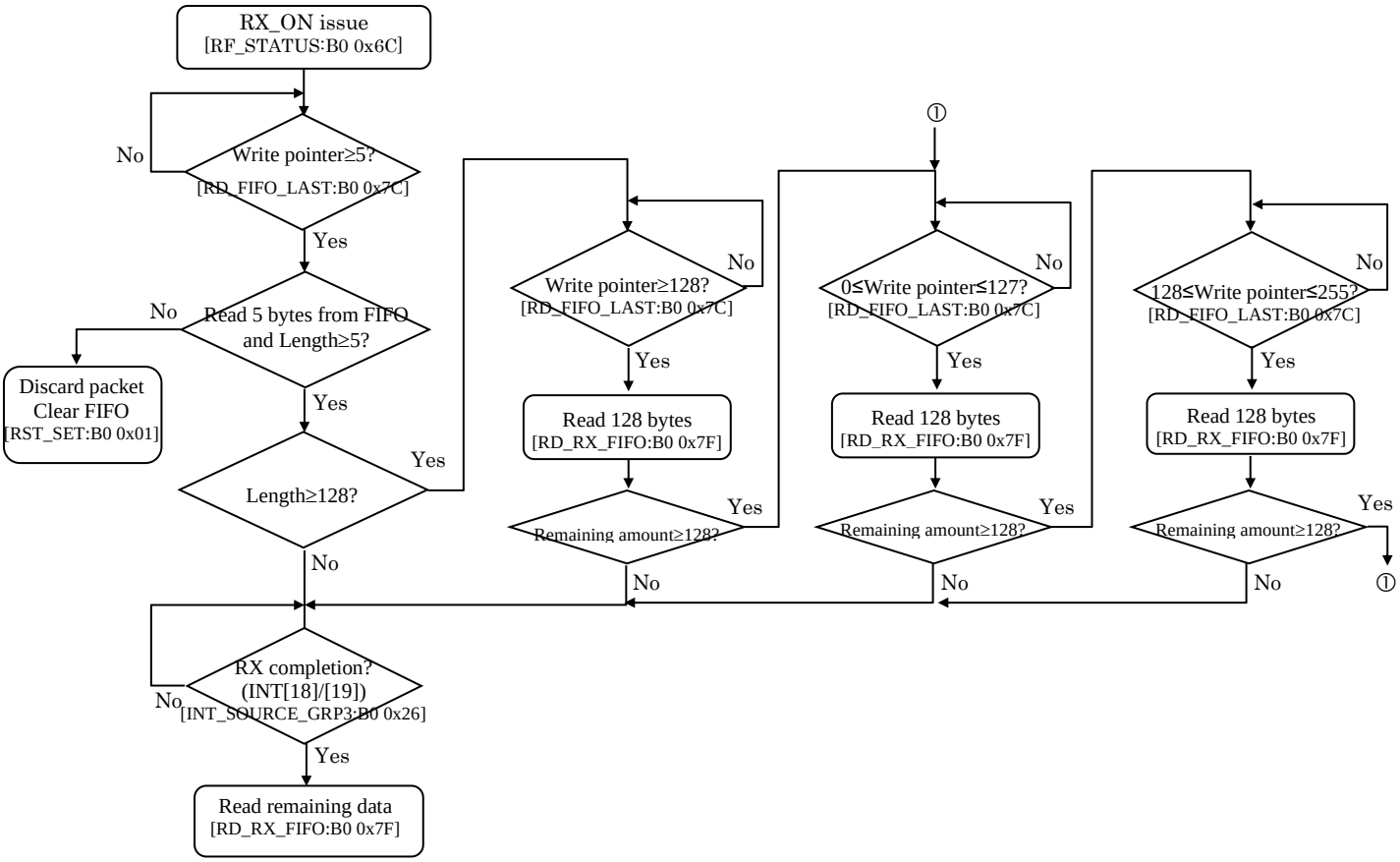
③ At ②, if the Length field is 128 or more, after Write pointer is 128 or more, read 123 bytes from FIFO. After that, if the remaining RX data size is less than 128, go to ⑦.

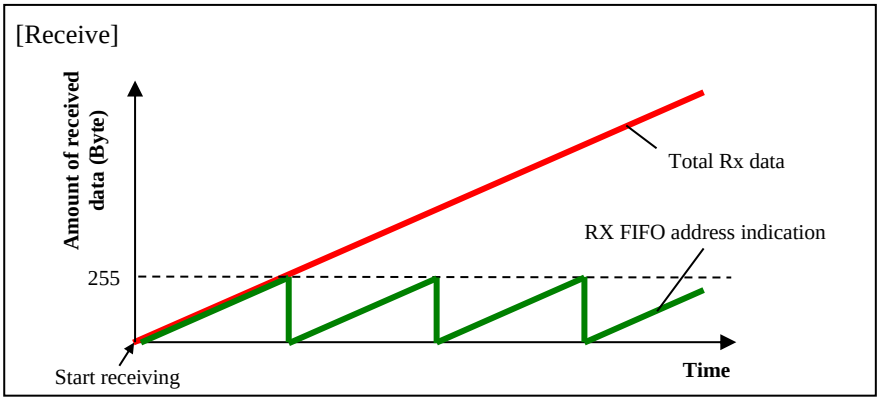
④ At ③, if the remaining RX data size is 128 or more, after Write pointer is 0 to 127, read 128 bytes from FIFO. After that, if the remaining RX data size is less than 128, go to ⑦.

⑤ At ④, if the remaining RX data size is 128 or more, after Write pointer is 128 to 255, read 128 bytes from FIFO. After that, if the remaining RX data size is less than 128, go to ⑦.

⑥ Repeat ④ and ⑤ until for the necessary amount of Rx data.

⑦ After RX completion interrupt (INT[18]/INT[19], group3) notification, read out the remaining RX data from FIFO.



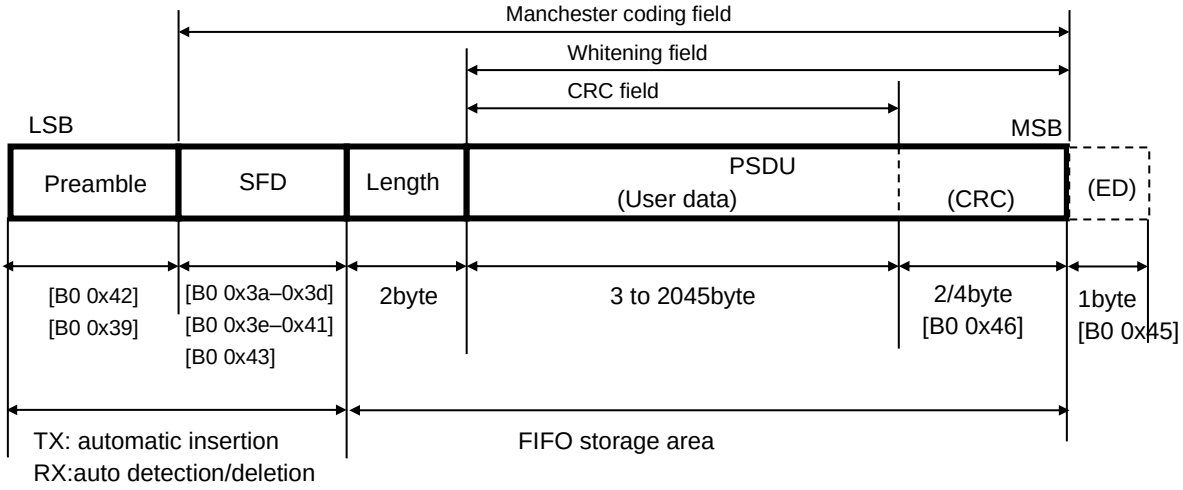


RX FIFO address indication (read pointer) increments after Rx start.
After receiving 256th byte data, the address indication is turned to 0 and increments again.

●Packet format

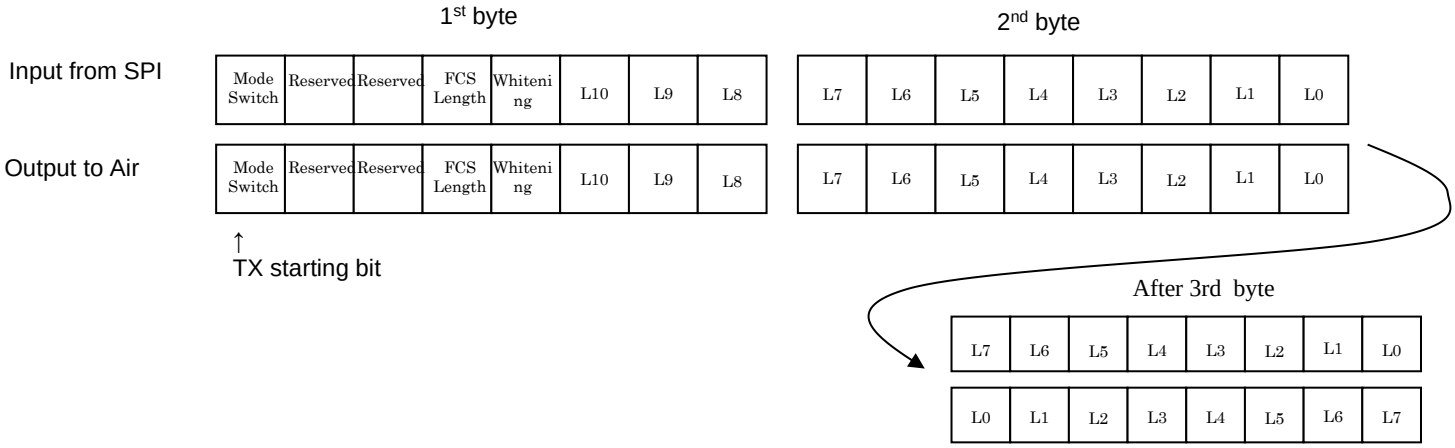
ML7396 family supports following packet format. (In DIO mode, the packet format is Preamble, SFD+DIO data)
Preamble and SFD field are automatically inserted in TX, and automatically detected and deleted in RX. The host MCU need not concern those packet handling.

[IEEE802.15.4g mode] (IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b1)

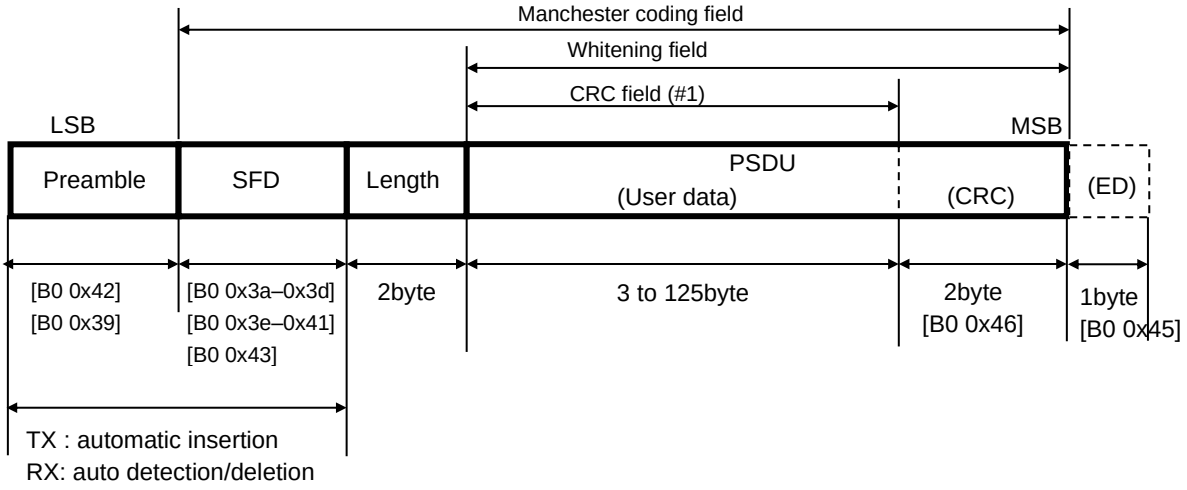


[Note]

1. The following shows the bit assignment of Length field (PHR) in IEEE802.15.4g format. It is different from IEEE802.15.4d format. User dara fieled (after 3rd byte) will be output with LSB first.
2. When using CRC32, the minimum user data length is 4 bytes. When transmitting/receiving 3-bytes data, CRC16 should be used. ACK packet cannot be received under CRC32 setting.



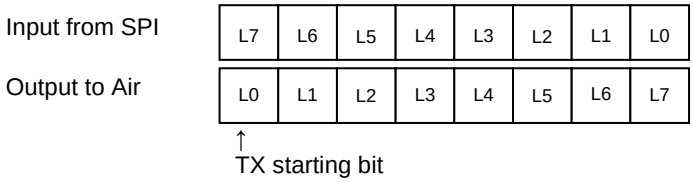
[IEEE802.15.4d mode] (IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b0)



[Note]

#1 When in 802.15.4d mode, if setting CRC_AREA ([CRC_AREA/FIFO_TRG:B0 0x77(1)] bit (PHYSET101 bit1) =0b1, CRC calculationn area will be extended to Length field (Length+PSDU).

1. The following shows the bit assignment of Length field (PHR) in IEEE802.15.4d format. It is different from IEEE802.15.4g format. User dara fieled (after 2nd byte) will be output with LSB first.



●Data whitening function

ML7396 family supports data whitening function specified in IEEE 802.15.4g standard. The following figure shows the PN9 pattern generator. The generated pattern will be "XOR" with data located in PSDU area.
Initialization value can be configured by [PN9_SET_L:B0 0x7A] and [PN9_SET_H:B0 0x7B] registers.
When setting PN9_EN ([PN9_SET_H:B0 0x7B(7)]) =0b1, this generator can be used as random number generator.
When WHITENING ([PACKET_MODE_SET:B0 0x45(4)]) =0b1, whitening condition is set by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)] setting. Please refer to the "Packet format".

- In IEEE802.15.4d mode (IEEE_MODE=0b0), data whitening applied to every TX or RX packet
- In IEEE802.15.4g mode (IEEE_MODE=0b1), data whitening will be applied to the packet which whitening bit in PHR fieled is set to 0b1

[Note]

1. The PN9 pattern generator shares setting with the Whitening function. While the Whitening function is running, PN9_EN should be set to 0b0.

TX: En = Rn $\oplus$ PN9n
RX: Rn = REn $\oplus$ PN9n

En:	Whitening bits as TX data
Rn:	data bits
REn:	Whitening bits as RX data
PN9n:	PN9 pattern (Initialization value 0b111111111)

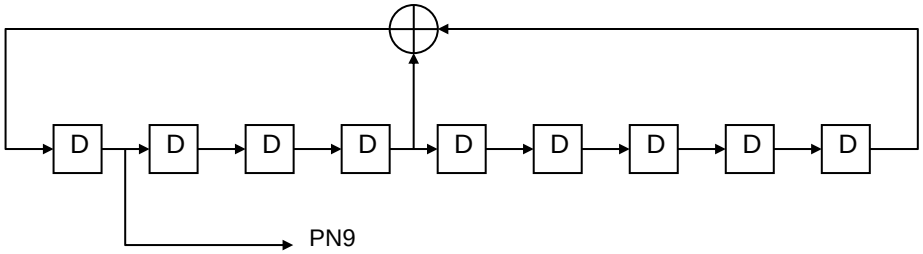
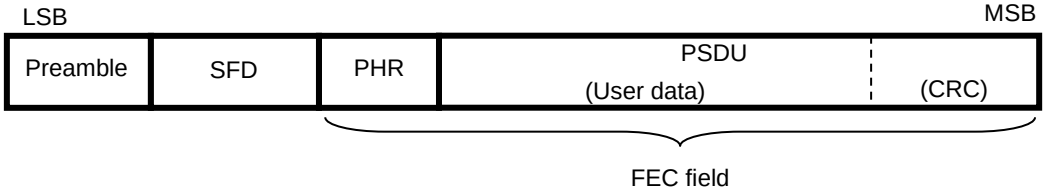


Fig. PN9 pattern generator

●FEC function

ML7396 family supports FEC function. FEC function will be applied to PHR and PSDU field as shown in below.



[Note]

1. Length in PHR fieled should be set the length before FEC encoding.
2. When using whitening function at same time, whitening will apply to the FEC encoded data. For more details of whitening field, please refer to the "Packet format".
3. Interleaving mode is not compliant to IEEE802.15.4g.
4. Interleaving mode is available for packet length 255 bytes or less (CRC is excluded).TX completion interrupt does not occur, in case of packet length 255 bytes of more.
5. PHY reset ([RST_SET:B0 0x03]) should be executed after recieved packet data in interleaving mode. If PHY reset does not executed, the first byte of TX data after recieving is not transmitted definitely.

●Energy Detection value (ED value) Function

ML7396 family supports calculating Energy detection value (here in after ED value) based on Received signal strength indicator (RSSI). ED value acquisition can be enabled by ED_CALC_EN ([ED_CNTRL:B0 0x1B(7)])=0b1, and as soon as transition to RX_ON state. And acquired ED value will be indicate at [ED_RSLT:B0 0x16] register. When ED_CALC_EN=1, ED value will be updated constantly during RX_ON state. Even if ED_CALC_EN=1, While CCA operation or diversity search operation, ED value will not be updated. After completion of CCA operation, diversity search, ED value will be updated.

ED value is not RSSI value at given timing, but average values. The number of average times can be specified by register ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)]). During diversity operation, 2DIV_ED_AVG[2:0] ([2DIV_ED_AVG:B0 0x6D(2-0)]) is used for setting. After acquiring specified average ED value, ED_DONE [ED_CNTRL:B0 0x1B(4)] becomes "0b1", and [ED_RSLT:B0 0x16] register is updated.

ED_DONE bit will be cleared if one of the following conditions is met.

1. Gain is switched.
2. Suspend ED value acquisition and then resume it.
3. Antenna is switched. (When diversity is enabled)

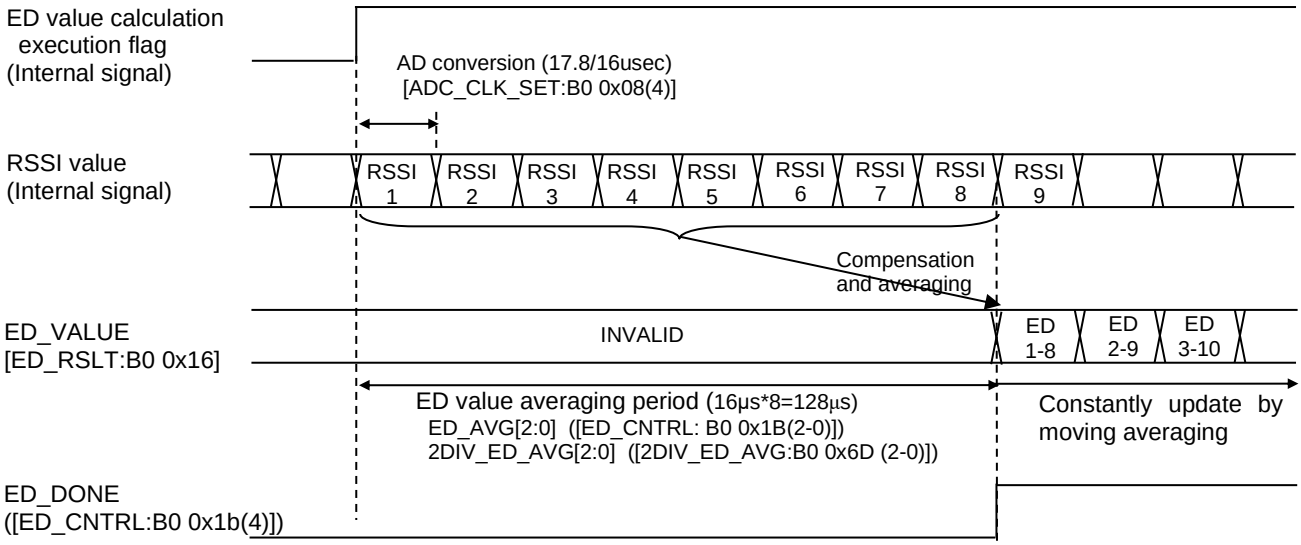
Timing from ED value starting point ot ED value acquisition is calculated as following formula.

ED value averaging time = AD conversion time (17.7μs/16μs) * number of average times

Note; AD conversion time can be set by ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)])
Default value is 1.8MHz and SDC conversion time is 17.7μs

[Timechart]

[Condition]
Set ADC_CLK_SET([ADC_CLK_SET: B1 0x08(4)])=0b1 (2MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x1B(2-0)])=0b011 (8 times averaging)



○ED value calculation

Input level and ED value are descrived in the following formula. During CCA operation, ED value is bigger than normal case, since the BPF setting is modified. Therefore, CCA compensation value should be attached to the normal case.

Input level is defined at antenna connector in the ciruit described in the “Application Circuit Example”. And antenna SW loss is assumed 0.5dB.

[≤200kbps]
ED value = 255/70 * (107 + input level [dBm] - variation - other loss) + CCA cpmpensation

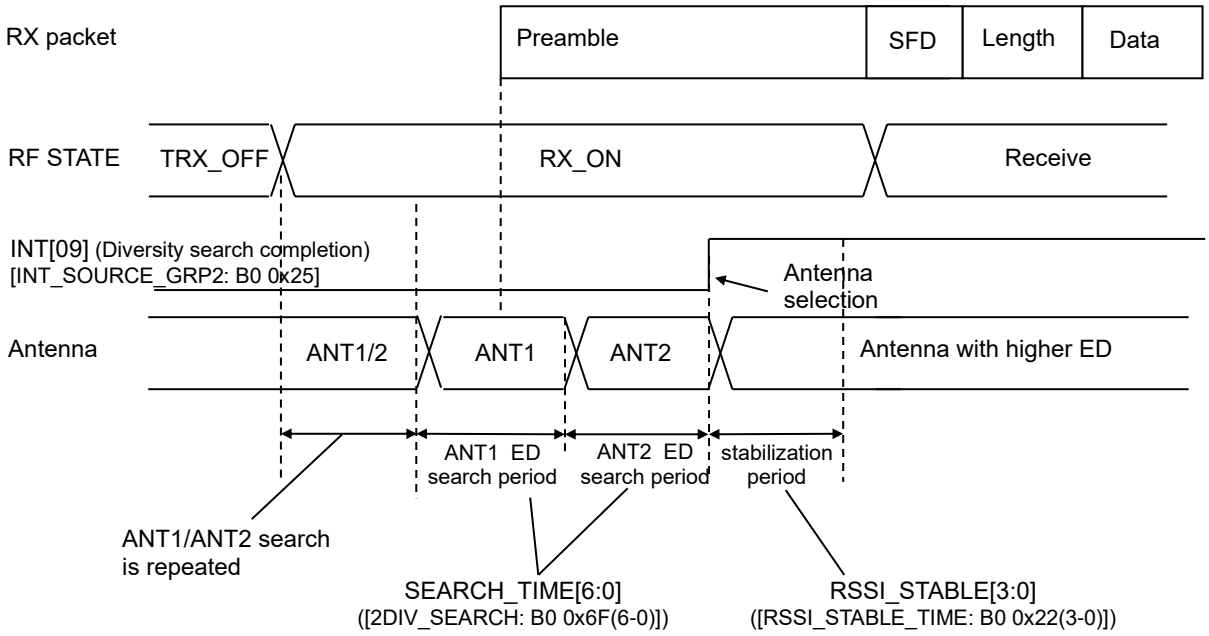
[400kbps]
ED value = 255/62 * (99 + input level [dBm] - variation - other loss)

Parameter	Value
Variations (individual, temp.)	6dB
Other loss	Antenna, matching circuit loss
CCA compensation	12@100kbps, 16@200kbps, 0@other rates [Note] 0@any rate of ML7396D

●Diversity Function

ML7396 family supports two antenna diversity function.
While setting 2DIV_EN ([2DIV_CNTRL: B0 0x71(0)])=0b1, as soon as RX_ON is set, diversity mode will start. When diversity mode is started, and upon RX data detection, each ED value will be acquired by switching two antennas. And then antenna with higher ED value will be selected automatically. As diversity uses preamble data for ED value acquisition, longer preamble length is desirable. If preamble is too short, accurate ED values may not be obtained.

The timing example is as below.



ED values and antenna diversity result will be cleared when as below:

1. Diversity search completion interrupt (INT[09] group2) is cleard.
2. FIFO* RX competion interrupt (INT[18] or INT[19] group3) is cleared
3. Diversity resume by errounous detection

ED values and diversity result should be read before clearing Diversity search completion or FIFO* RX completion interrupt.
During receiving state, clearing Diversity search completion interrupt causes the data error since diversity operation wlll resume by the interrupt clearance. Diverstiy search completion interrupt should be cleared at same timing of FIFO* RX completion interrupt clearance.
ML7396 supports recovering function from incorrect diversity completion caused by errornous detection due to thermal noize, After dicersity search completion, if preamble can not be detected until antenna search timer expiration, ML7396 judges the previous diversity search completion is incorrect and resume diversity operation automatically.
When resume diversity operation for next packet receiving, please clear RX completion interrupt and Diversity search completion interrupt.

(Note)

1. When an incorrect diversity completion caused by errornous detection due to thermal noize, ML7396 resume antenna diversity automatically. But when receiving a desired signal during the process of errounous detection, ED value obtained by [ANT1_ED:B0 0x73] or [ANT2_ED:B0 0x74] may indicate a low value different from the actual input level.
   If this event occures, the actual ED value of desired signal can be achibed by reading [ED_RSLT:B0 0x16] registers after SFD detection interrupt (INT[11] group2) generation.
2. When RF state is changed to TX_ON state immediately after an incorrect diversity completion caused by errornous detection, ML7396 judges Diversity search is done. Then, Diversity search is not operated at next receiving. In this case, please clear Diversity search completion interrupt (INT[09] group2) by next receiving.

○Antenna switching function

By using [2DIV_CTRL: B0 0x71], [RF_CTRL_SET: B0 0x75] registers, ML7396 can support both SPDT and DPDT antena swith control. ANT_SW pin (#20) and TRX_SW pin (#21) output considion for each antenna switch are explained below.

DPDT switch

Set 2PORT_SW([2DIV_CTRL:B0 0x71(1)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x71(5)])=0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL:B0 0x71(2)])=0b1, polarity of ANT_SW pin (#20) and TRX_SW pin (#21) are reversed.

TX/RX state	INV_TRX_SW=0b0 (default setting)		INV_TRX_SW=0b1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	H	L	L	H	Idle state
TX	L	H	H	L	TX state
RX	H	L	L	H	When Diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x71(0)]=0b1).
	L/H	H/L	H/L	L/H	If diversity enable is set, during searching, (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternatively. After diversity completion, fix to one of the condition.

SPDT switch

Set 2PORT_SW([2DIV_CTRL:B0 0x71(1)])=0b0, ANT_CTRL1([2DIV_CTRL: B0 0x71(5)])=0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x71(2)])=0b1, polarity of TRX_SW pin (#21) is reversed.

TX/RX condition	INV_TRX_SW=0b0 (default setting)		INV_TRX_SW=0b1 (polarity reverse)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idel state
TX	L	H	L	L	TX state
RX	L	L	L	H	When diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x71(0)]=0b1).
	H/L	L	H/L	H	If diversity enable is set,during searching (TRX_SW=H) and (TRX_SW=L) is switched alternatively. After diversity completion , fix to one of the condition.

In the above setting, If INV_ANT_SW([2DIV_CTRL: B0 0x71(3)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x71(5)])=0b1 are set, polarity of ANT_SW pin (#20)is reversed.

TX/RX state	INV_ANT_SW=0b0 ANT_CTRL1=any (default setting)		INV_ANT_SW=0b1 ANT_CTRL1=0b1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	When diversity disable or intial codition when diversity enable is set ([2DIV_CTRL: B0 0x71(0)]=0b1).
	H/L	L	L/H	L	If diversity enable is set, during searching (ANT_SW=H) and (ANT_SW=L) is switched alternatively. After diversity completion, fix to one of the condition.

○Antenna switch forced setting

ANT_SW pin (#20) and TRX_SW pin (#21) output conditions can be set to fix by [RF_CNTRL_SET: B0 0x75] register, or 2DIV_RSLT2 ([2DIV_RSLT:B0 0x72(1)]) and INV_TRX_SW ([2DIV_CNTRL:B0 0x71(2)]) when diversity fuction is diabled.

1. Forced setting by [RF_CNTRL_SET] register

   ANT_SW pin: By ANT_SW_EN (bit1)=0b1, ANT_SW_SET (bit5) condition will be output.
   TRX_SW pin: By TRX_SW_EN (bit0)=0b1, TRX_SW_SET (bit4) condition will be output.

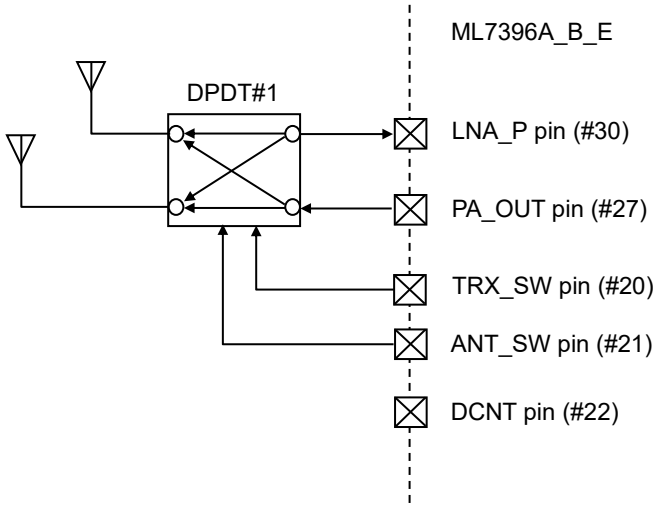
2. Forced setting by 2DIV_RSLT2 bit and INV_TRX_SW bit when diversity function is disabled
   (2DIV_EN ([2DIV_CNTRL:B0 0x71(0)])=0b0)

   ANT_SW pin: When 2DIV_RSLT2=0b0, output “L”. When 0b1, output “H”.
   TRX_SW pin: When INV_TRX_SW=0b0, output “L”. When 0b1, output “H”.

Output defined by [RF_CNTRL_SET:B0 0x75] registers setting has higer priority.
When diversity is enable (2DIV_EN=0b1), output definced by 2DIV_RSLT2 and INV_TRX_SW are ignored.
Any antenna switch setting is inhibited to avoid out-of-synchronization during RECEIVE state.

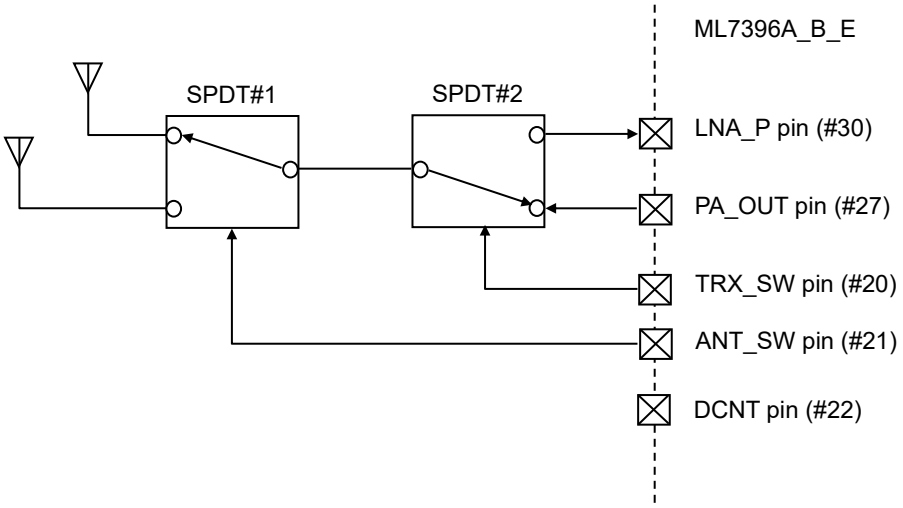
Antenna switching control signals can be also used as below.

Example 1) using one DPDT switch
Please set 2PORT_SW([2DIV_CTRL: B0 0x71(1)])=0b1.



(Note) altenate external PA control signal exists (DCNT pin).
(Note) external circuits around LNA_P pin, PA_OUT pin and antenna switch (DPDT#1) are omitted in this example.

Example 2) using 2 SPDT switches
Please set 2PORT_SW([2DIV_CTRL: B0 0x71(1)])=0b0.



(Note) altenate external PA control signal exsits. (DCNT pin)
(Note) external circuits around LNA_P pin, PA_OUTpin and antenna switch(SPDT#2) are omitted in this example.

●CCA (Clear Channel Assessment) Function

ML7396 family has CCA function that will check availability of certain channel. 3 type of modes are available, normal mode, continuous mode, IDLE detection mode.

[CCA mode setting]
At normal operation

CCA mode	[CCA_CNTRL:B0 0x15]		
	Bit4 (CCA_EN)	Bit3 (CCA_IDLE_EN)	Bit5 (CCA_LOOP_START)
Normal mode	0b1	0b0	0b0
Continuous mode	0b1	0b0	0b1
IDLE detection mode	0b1	0b1	0b0

When using AUTO_ACK

CCA mode	[AUTO_ACK_SET:B0 0x55]	[CCA_CNTRL:B0 0x15]
	Bit4 (AUTO_ACK_EN)	Bit7 (CCA_AUTO_EN)
IDLE detection mode	0b1	0b1

When using address filtering

CCA mode	[ADDFIL_CNTRL:B2 0x60]	[PACKET_MODE_SET:B0 0x45]
	Bit0 to Bit4	Bit0 (ADDFIL_IDLE_DET)
IDLE detection mode	Set 0b1 to any bits	0b1

○Normal mode

Normal mode determines IDLE or BUSY. CCA (normal mode) will be executed when RX_ON is issued while CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0 are set.

The judgement of CCA is determined by average ED value in [ED_RSLT:B0 0x16] and threshold value defined by [CCA_LEVEL:B0 0x13] register. If average ED value exceeds CCA threshold value, it is determined as “BUSY”. And set CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) =0b01 is set. If ED value is smaller than CCA threshold, and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L:B0 0x17], [IDLE_WAIT_H:B0 0x18] resisters, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long period”.

If “BUSY” or “IDLE” is determined, CCA_DONE [CCA_CNTRL:B0 0x15(2)] will become 0b1 and CCA completion interrupt (INT[08] group2) is generated. CCA_EN bit will be cleared to 0b0 automatically.
When CCA completion interrupt is cleared, CCA_RSLT[1:0] are reset to 0b00. Therefore CCA_RSLT[1:0] need to be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LEVEL:B0 0x12] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if average ED value exceeds CCA threshold value, it is determined as “BUSY” and CCA operation is terminated. However, if average ED value is smaller than CCA threshold value, IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. CCA operation continues until “BUSY” is ditermined or the given ED value is out of the averaging target and “IDLE” is determined. For detail operation of ED value exceeding [CCA_IGNORE_LEVEL:B0 0x12] register, please refer to "IDLE determination exclusion under strong signal input".

Timing from CCA command issue to the CCA completion is calculated as the following formula.

[IDLE detection]
CCA execution time = (ED value average times + IDLE_WAIT setting) * A/D conversion time +
filter stabilization time (A/D conversion time* 2)

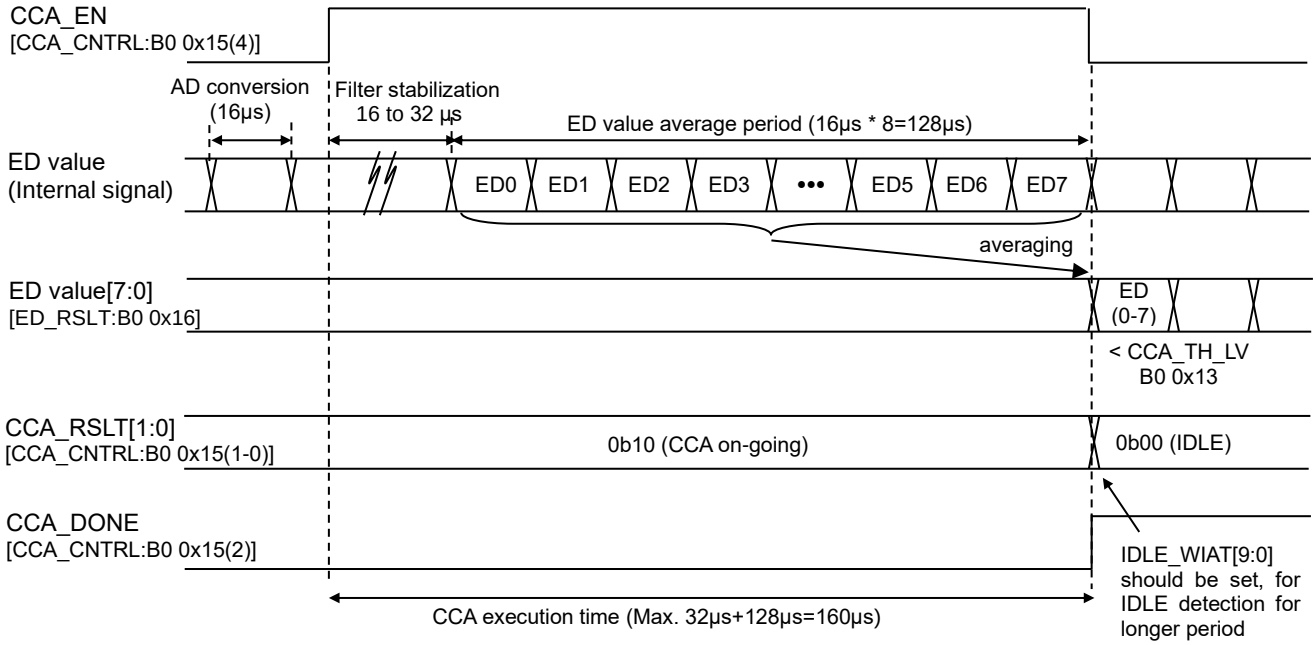
[BUSY detection]
CCA execution time = ED value average times * A/D conversion time+ filter stabilization time (A/D conversion time* 2)

[Note]
1. Above formula does not consider IDLE judgment exclusion based on [CCA_IGNORE_LEVEL:B0 0x12] register. For details, please refer to "DLE determination exclusion under strong signal input ".
2. A/D conversion time can be selected by ADC_CLK_SET ([ADC_CLK_SET:B0 0x08(4)]). ADC_CLK_SET=0b0: 17.8µs, 0b1: 16µs

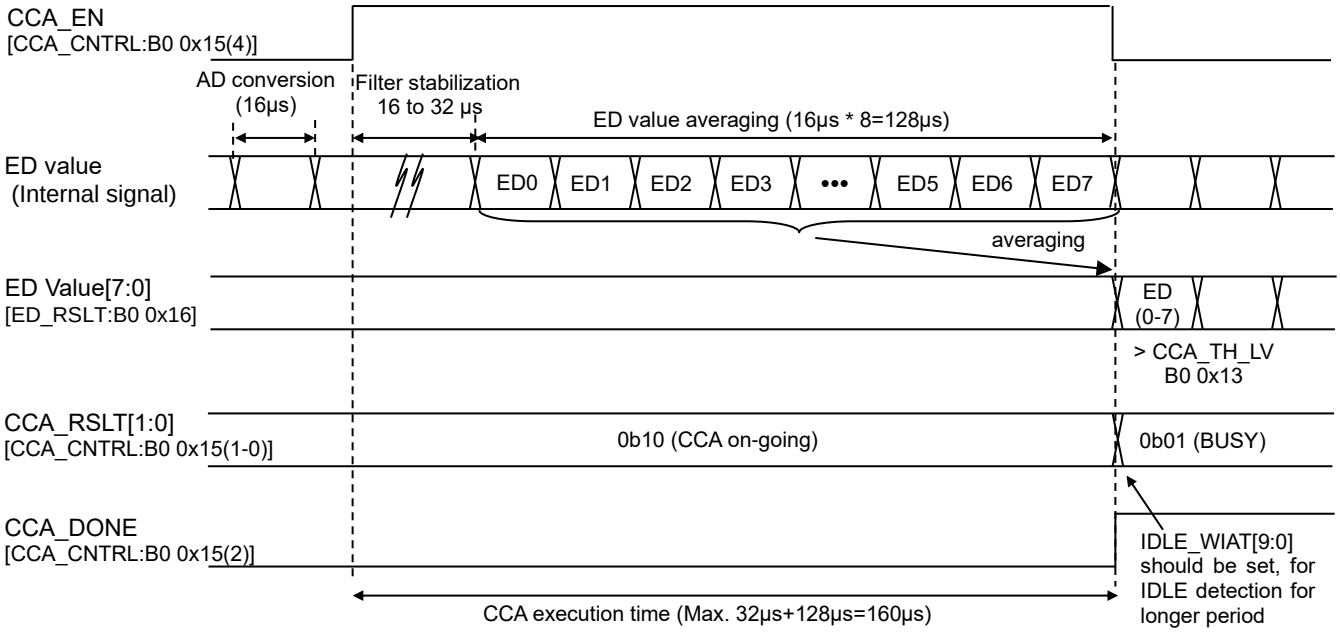
The following is timing chart for normal mode.

[Conditions]
ADC_CK_SET ([ADC_CLK_SET:B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x17/0x18(1-0)])=0b00_0000_0000 (IDLE detection 0µs)

[IDLE detection case]



[BUSY detection case]



[Note]
1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 µs for indicating -80dBm ED value.

○Continuous mode

Continuous mode continues CCA operation until terminated by the host MCU. CCA continuous mode will be executed when RX_ON is issued while CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b1 are set.

Like normal mode, CCA is determined by average ED value in [ED_RSLT:B0 0x16] register and threshold value defined by [CCA_LEVEL:B0 0x13] register. If average ED value exceeds CCA threshold, it is determined as “BUSY”, set CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) =0b01. If ED value is smaller than CCA threshold, and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L:B0 0x17], [IDLE_WAIT_H:B0 0x18] resisters, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long period”.

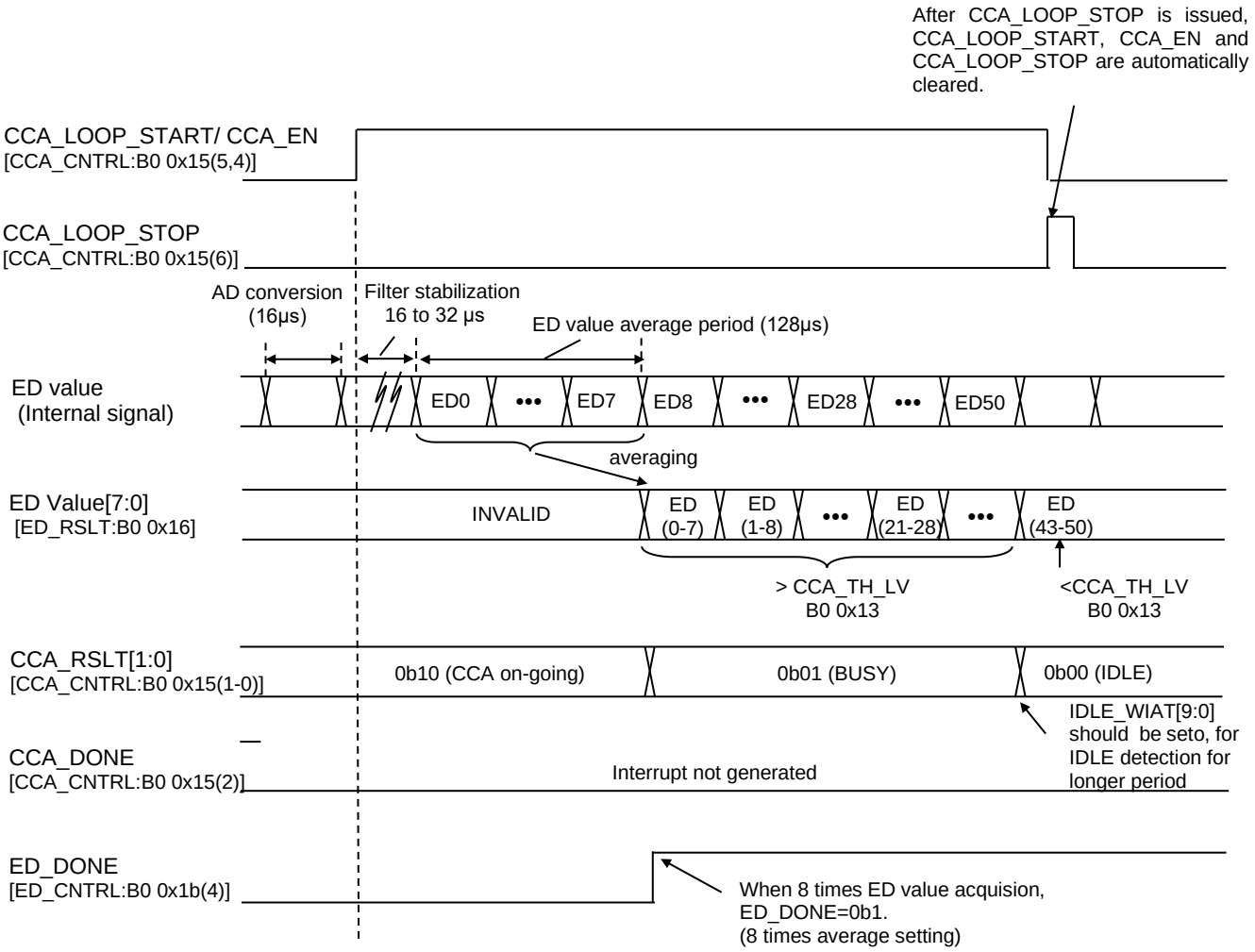
If an ED value exceeds the value defined by [CCA_IGNORE_LEVEL:B0 0x12] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if average ED value exceeds CCA threshold value, it is determined as “BUSY” and CCA operation is terminated. However, if average ED value is smaller than CCA threshold value, IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. For detail operation of ED value exceeding [CCA_IGNORE_LEVEL:B0 0x12] register, please refer to "IDLE determination exclusion under strong signal input".

Continuous mode does not stop when “BUSY” or “IDLE” is determined. CCA operation continues until 0b1 is set to CCA_LOOP_STOP ([CCA_CNTRL:B0 0x15(6)]). Result is updated every time ED value is acquired. CCA_DONE ([CCA_CNTRL:B0 0x15(2)]) will not be 0b1, and CCA completion interrupt (INT[08] group2) will not be generated.

The following is timing chart for continuous mode.

[Conditions]
ADC_CK_SET ([ADC_CLK_SET:B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x17/0x18(1-0)])=0b00_0000_0000 (IDLE detection 0µs)

[BUST to IDLE transitions, terminated with CCA_LOOP_STOP]



[Note]
1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 µs for indicating -80dBm ED value.

○IDLE detection mode

IDLE detection mode continues CCA until IDLE detection. IDLE detection CCA will be executed when RX_ON is issued while CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b1 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0 are set.

When AUTO_ACK function is enabled by AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)])=0b1, if CCA_AUTO_EN ([CCA_CTRL:B0 0x15(7)]) =0b1, CCA IDLE detection mode is performed before transsmitting ACK packet.
And when Address filtering function is enable by setting 0b1 to any bit0 to bit4 of [ADDFIL_CNTRL:B2 0x60] register, if ADDFIL_IDLE_DET ([PACKET_MODE_SET:B0 0x45(0)])=0b1, CCA IDLE detection mode is performed after address mismatch detection.

Like normal mode, CCA is determined by average ED value in [ED_RSLT:B0 0x16] register and threshold value defined by [CCA_LEVEL:B0 0x13] register. If average ED value exceeds CCA threshold, it is determined as “BUSY”, set CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) =0b01. If ED value is smaller than CCA threshold, and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L:B0 0x17], [IDLE_WAIT_H:B0 0x18] resisters, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long period”.

In IDLE detection mode, only when IDLE is detected, CCA_DONE ([CCA_CNTRL:B0 0x15(2)]) wil be set to 0b1 and CCA completion interrupt (INT[08] group2) is generated. If CCA operation is performed by CCA_EN=0b1, after IDLE detection, CCA_EN and CCA_IDLE_EN are reset to 0b0.

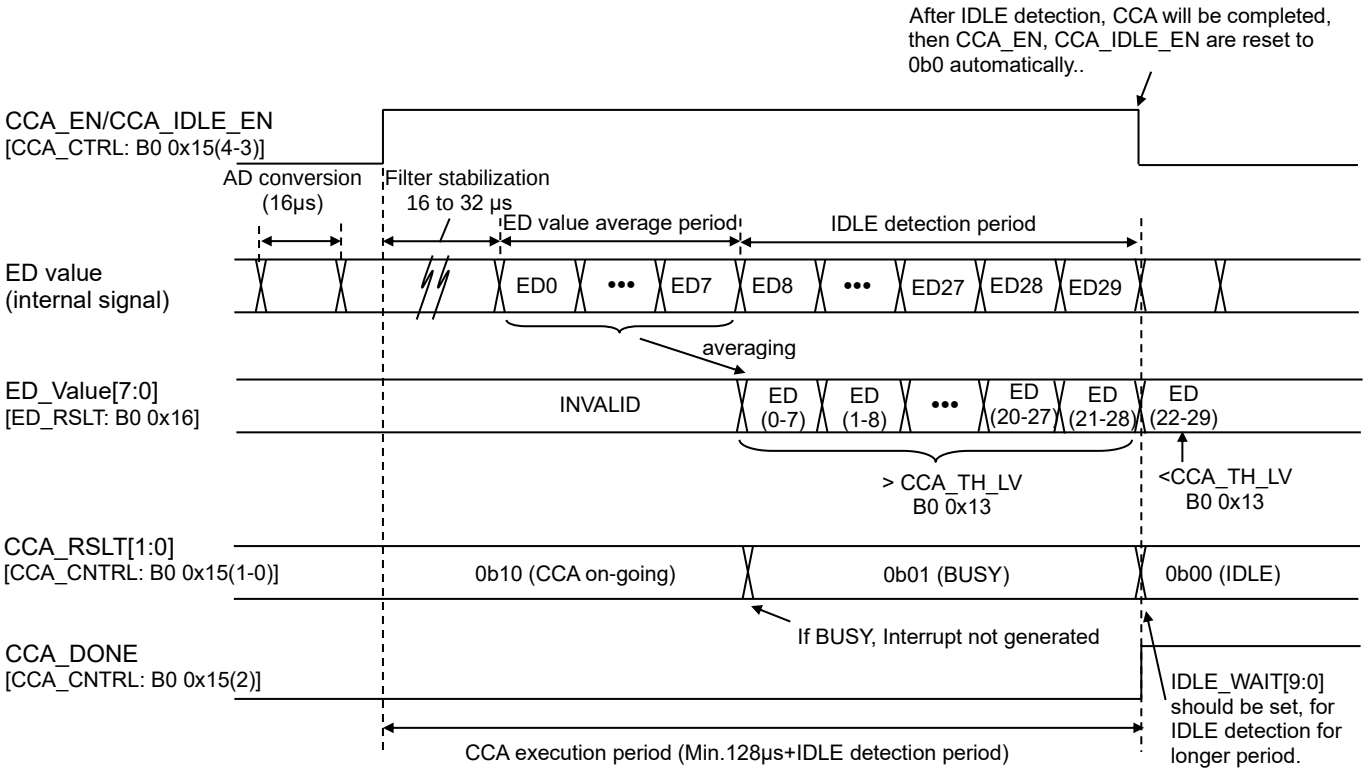
Upon clearing CCA completion interrupt, CCA_RSLT[1:0] are reset to 0b00. CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LEVEL:B0 0x12] register, and as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if average ED value is smaller than CCA threshold value, IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. CCA operation continues until given ED value is out of averaging target and “IDLE” is determined. For details of ED value exceeding [CCA_IGNORE_LEVEL: B0 0x12] register, please refer to ”IDLE determination exclusion under strong signal input”.

The follwing is timing chart for IDLE detection.

[Upon BUSY detection, continue CCA and IDLE detection case]

[Conditions]
ADC_CK_SET ([ADC_CLK_SET:B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CNTRL:B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x17/0x18(1-0)])=0b00_0000_0000 (IDLE detection 0μs)



[Note]
1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 μs for indicating -80dBm ED value.

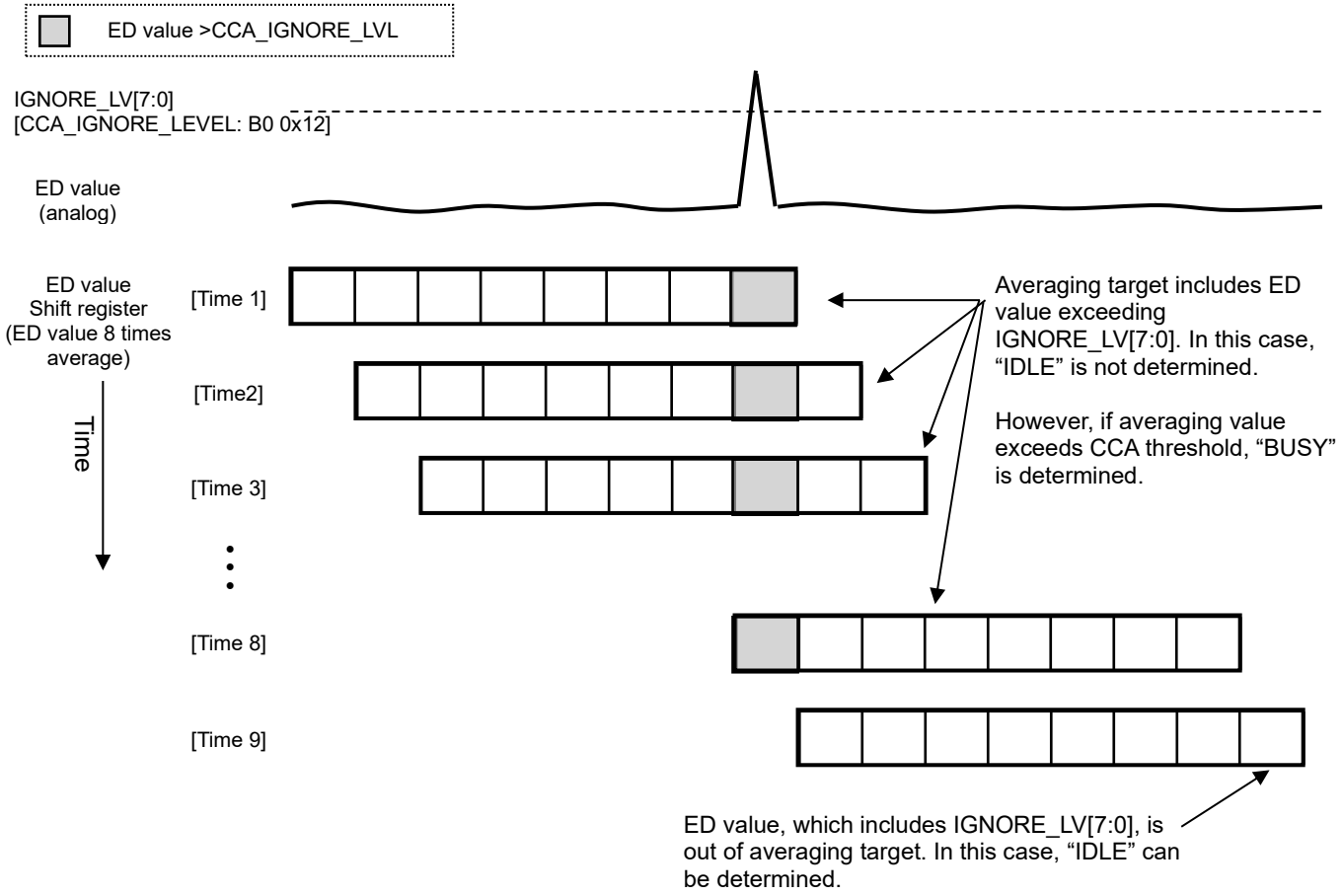
○IDLE determination exclusion under strong signal input

If acquired ED value exceeds [CCA_IGNORE_LVL: B0 0x12] register, IDLE dertermination is not performed as lon as a given ED value is included in the averaging target range. If average ED value including this strong ED value indicated in [ED_RSLT: B0 0x16] register exceeds the CCA threshold value defined by [CCA_LEVEL: B0 0x13] register, it is considered as ”BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x15(1-0)])=0b01 is set.

If average ED value is smaller than CCA threshold value, IDLE determination is not performed and CCA_RSLT[1:0] indicates 0b11 ”CCA evaluation on-going (ED value excluding CCA judgement acquisition)”. CCA will continue until “IDLE” or “BUSY” determination (in case of IDLE detection mode, “IDLE2 is determined. In case of continuous mode, CCA_LOOP_STOP([CCA_CTRL: B0 0x15(6)]) is issued.)

[Note]
CCA completion interrupt (INT[08] group2) is generated only when “IDLE” or “BUSY” is determined. Therefore, if data whose ED value exceeds IGNORE_LV[7:0] ([CCA_IGNORE_LEVEL:B0 0x12(7-0)]) are input intermittently, neither “IDLE” or “BUSY” can be determined and CCA may continues.

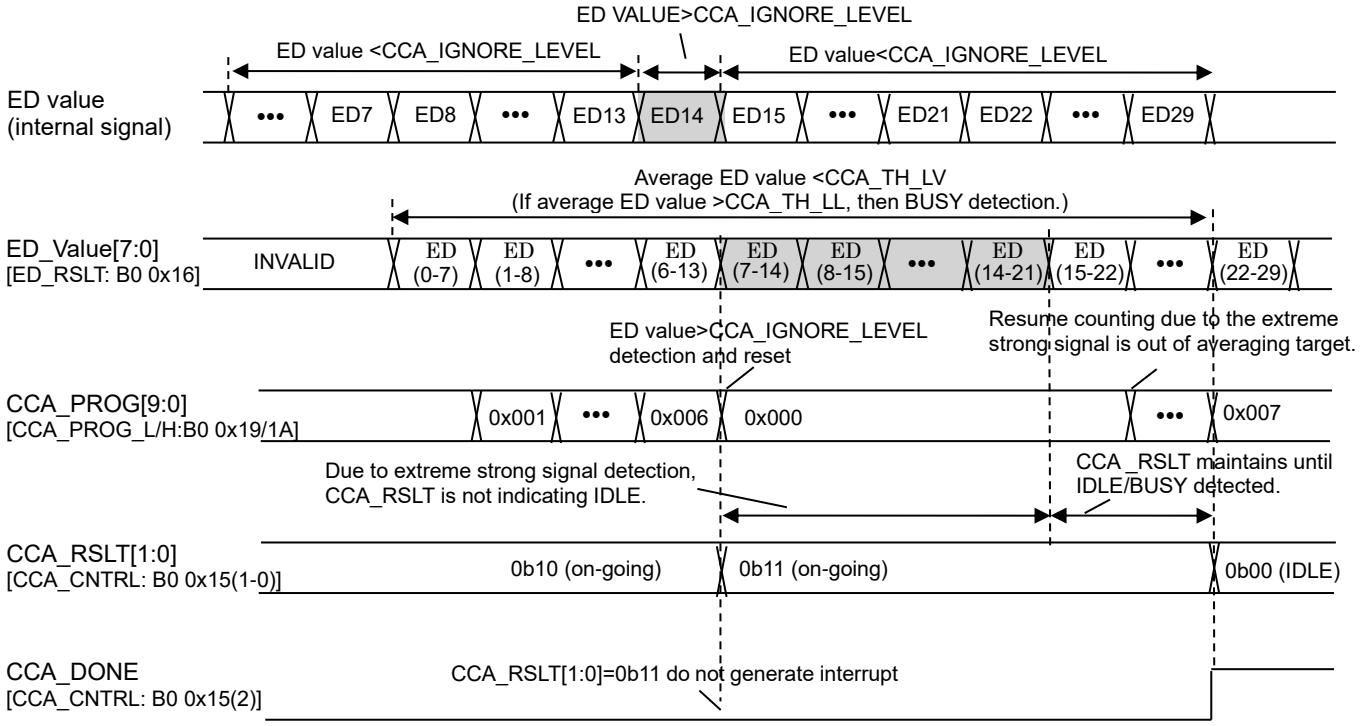
[ED value acquisition under extrem strong signal]



The follwing is timing chart for CCA determination exclusion under strong signal.

[During IDLE_WAIT counting, detected extremly strong signal. After the given signal is out of averaging target, IDLE detection case]

[Condition]
CCA normal mode
ADC_CK_SEL ([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x17/18(1-0)])=0b00_0000_0111(IDLE detection period 112μs)



[Note]
1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 μs for indicating -80dBm ED value.

○IDLE detection for long period

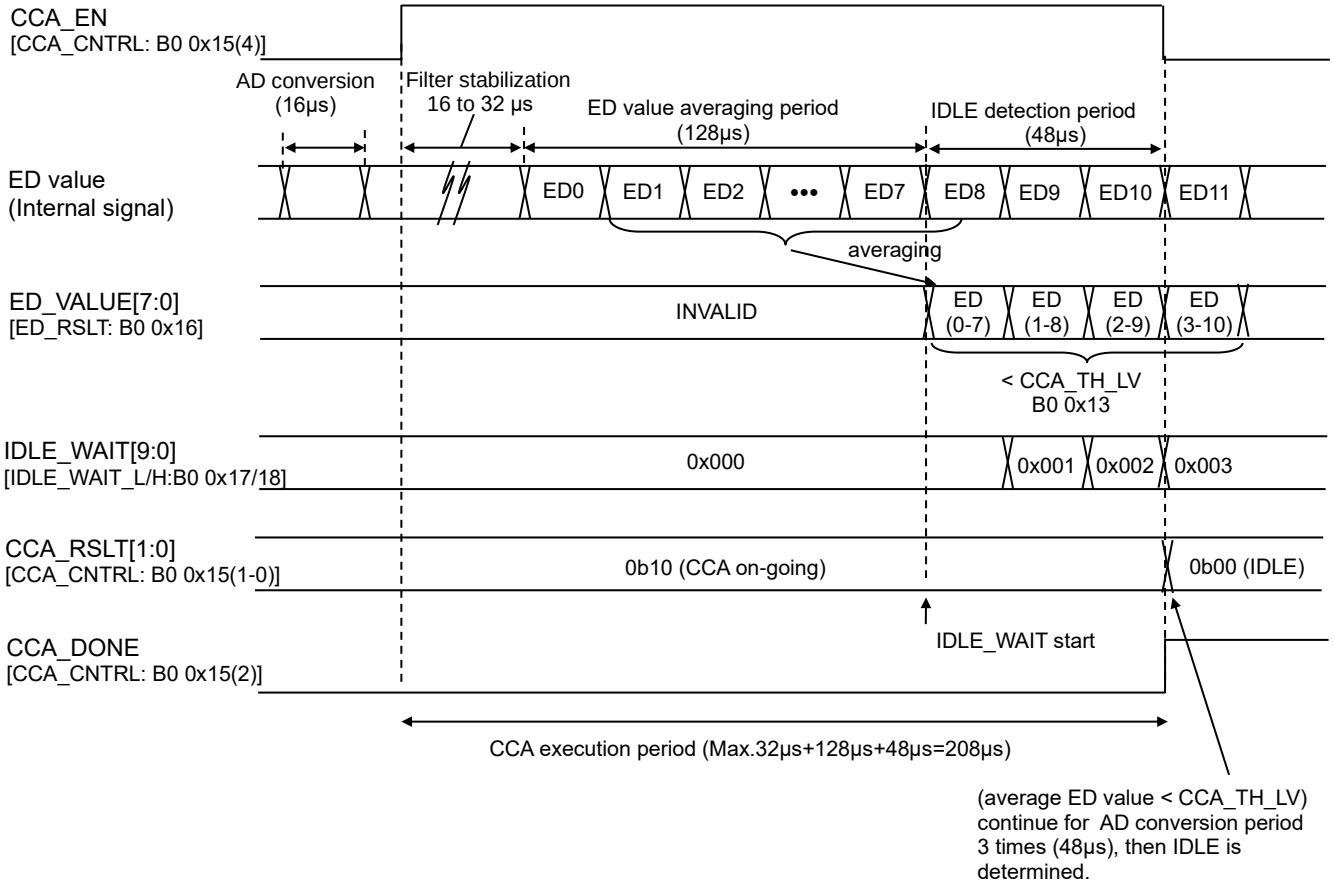
When CCA IDLE detection is performed for longer time period, IDLE_WAIT[9:0]([IDLE_WAIT_L/H:B0 0x17/18(1-0)] can be used. By setting IDLE_WAIT [9:0], averaging period longer than the period (for example, AD conversion16μs, 8 times average setting 128μs) can be possible.

This function can be used for IDLE determination – by counting times when average ED value becomes smaller than CCA threshold defined by [CCA_LEVEL: B0 0x13] register. When counting exceed IDLE_WAIT [9:0], IDLE is determined. If average ED value exceeds CCA threshold level, imemediately "Busy" is determined without wait for IDLE_WAIT [9:0] period.

The following timing chart is IDLE detection setting IDLE_WAIT[9:0].

[ED value 8 timesv average IDLE detection case]

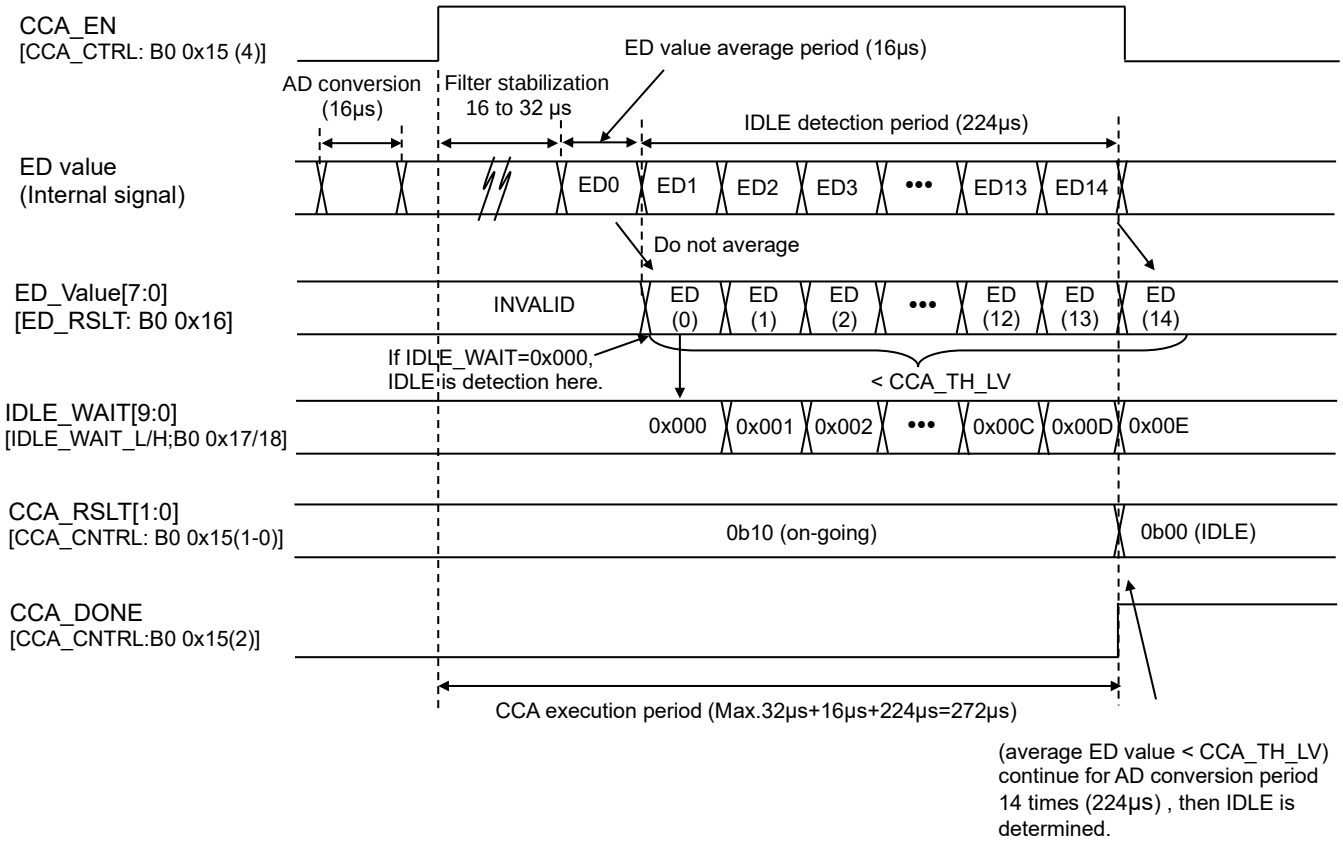
[Condition]
CCA normal mode
ADC_CK_SEL ([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz)
ED_AVG[2:0] ([ED_CTRL: B0 0x1B(2-0)])=0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x17/18(1-0)])=0b00_0000_0011 (IDLE detection period 48μs)



[Note]
1. After issuing CCA command, transit into no-input state, and exit this state after filter stbilization.
2. When the iput level chnge from no-input to -80dBm, it takes around 32 μs for indicating -80dBm ED value.

[ED value 1time IDLE detection case]

[Condition] CCA normal mode ADC_CK_SEL ([ADC_CLK_SET: B0 0x08(4)])=0b1 (2MHz) ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b000 (ED value 1 time average) IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x1718(1-0)])=0b00_0000_1110 (IDLE detection period 224µs)



(average ED value < CCA_TH_LV) continue for AD conversion period 14 times (224µs) , then IDLE is determined.

○CCA operation during diversity

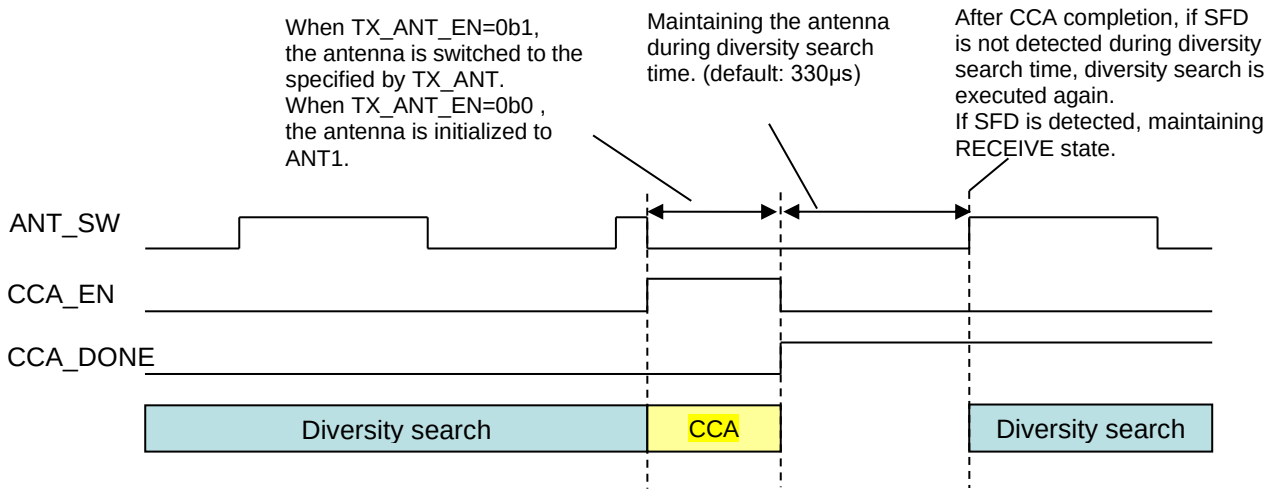
(1) CCA operation during diversity search

During diversity search, If CCA command is issued, diversity terminated and CCA starts.

Upon CCA starting, antenna is fixed to the default value (*1), maintaining until next diversity search. However, if TX_ANT_EN ([2DIV_RSLT:B0 0x72(5)])=0b1 is set, antenna is specified by TX_ANT ([2DIV_RSLT:B0 0x72(4)]) and maintaining until next diversity search.

After CCA completion, if SFD is not detected during diversity search time specified by SEARCH_TIME[6:0] ([2DIV_SEARCH:B0 0x6F(6-0)]) (default approx. 330µs), diversity search will be executed again. If SFD is detected during CCA or after CCA completion, continuing RECEIVE state and diversity search is not executed.

* 1 : Please refer the each table of “Antenna switching function” in “Diversity Function”.
(Upper setting in the "RX" state column)



[Note]

When executing CCA during diversity search, set the waiting taimer for waiting for CAA completion interrupt (INT[08] group2). Since CCA executing timing is same as the diversity search completion, CCA completion interrupt may not be notified. When timeout occurs, the latest result is stored into CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]). In this case, if executing CCA again, set CCA_LOOP_STOP ([CCA_CNTRL:B0 0x15(6)])=0b1 before issuing CCA command.

For waiting timer setting, please refer to the CCA execution time described in "Normal mode".

For details of the CCA execution flow during diversity search, please refer to "CCA operation during diversity" in the “Flow Charts”.

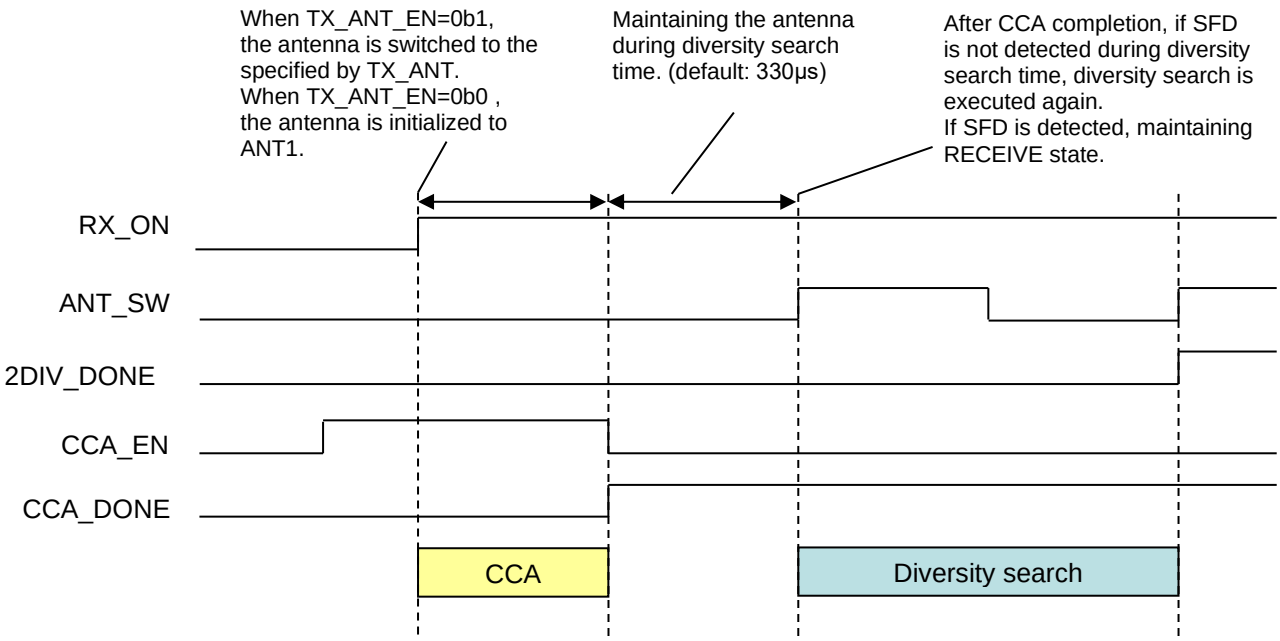
During CCA operarion, RX operation is performed at the same time. Even if CCA_DONE is not notified, SFD detection interrupt (INT[11] group2), RX FIFO access error interruption (INT[14] group2), FIFO-Full interrupt (INT[05] group1), FIFO0/1 RX completion interrupt (INT[18]/[19] group3), or FIFO0/1 CRC error interrupt (INT[20]/[21] group3) may be notified.

For details of the diversity function, please refer to "Diversity Function".

(2) During diversity search, before RX_ON state, CCA is performed

If diversity ON setting and CCA operation setting are enabled before RX_ON state, after RX_ON state transition, diversity search will not perform, but CCA will start.

After CCA completion, if SFD is not detected during diversity search time specified by SEARCH_TIME[6:0] ([2DIV_SEARCH:B0 0x6F(6-0)]) (default approx. 330µs), diversity search wil be executed. If SFD is detected during CCA or after CCAcompletion, continuing RECEIVE state and diversity search is not executed.



●SFD detection function

ML7396 family supports the “Start Frame of Delimiter” (SFD) recognition function. By having 2 sets of SFD pattern strage area, it is possible to detect IEEE 802.15.4g SFD patterns valied by “MRFSKFSD setting” and “FEC scheme”. For more details, please refer to IEEE 802.15.4g standard.

Note: The default value of both SFD#1 and SFD#2 (Bank0 0x3A to 0x41) are set to the IEEE 802.15.4d SFD (1byte:0xA7).

In IEEE802.15.4g standard, 4 SFD pattern (each 2 bytes) is defined according to SFD group defined by phyMRFSKSFD and FEC scheme (coded, uncoded).
According to the setting to MRFSKSFD ([PACKET_MODE_SET:B0 0x45(6)]) and FEC_EN ([FEC_CRC_SET:B0 0x46(6)]), SFD pattern to be added TX packet and SFD pattern to be received in RX packet are selected from SDF pattern #1 and SFD pattern #2 as following tables. SFD pattern #1 is defined by [SFD1_SET1:B0 0x3A] to [SFD1_SET4:B0 0x3D] registers and SFD pattern #2 is defined by [SFD2_SET1:B0 0x3E] to [SFD2_SET4:B0 0x41] registers.

(1) TX

①SFD length is shorter than or equal to 2 bytes. (IEEE 802.15.4g format)

FEC_EN	MRFSKSFD	
	0	1
0	SFD1[15:0]	SFD2[15:0]
1	SFD1[31:16]	SFD2[31:16]

②SFD length is longer than or equal to 3 bytes. (Original format

FEC_EN	MRFSKSFD	
	0	1
0/1	SFD1 [31:0]	SFD2 [31:0]

(2) RX

If SFD length is shorter than or equal to 2 bytes and FEC_EN=0b1, it is possible to serach two SFD patterns. According to the matching pattern, FEC is performed. Otherwise serach one pattern and the data following SFD are processed as uncoded.

①SFD length shorter than or equal to 2bytes. (IEEE 802.15.4g format)

FEC_EN	MRFSKSFD	SFD pattern		SFD detect	Data process after SFD
		uncoded	coded		
1	0	SFD1 [15:0]	SFD1 [31:16]	Uncoded or coded	If pattern match with coded pattern, FEC is performed. If pattern match with uncoded pattern, FEC is not performed
1	1	SFD2 [15:0]	SFD2 [31:16]	Uncoded or coded	If pattern match with coded pattern, FEC is performed. If pattern match with uncoded pattenr, FEC is not performed.
0	0	SFD1 [15:0]	-	Uncoded	Determined as uncoded
0	1	SFD2 [15:0]	-	Uncoded	Determined as uncoded

②SFD length is longer than or equal to 3bytes. (Original format)

FEC_EN	MRFSKSFD	SFD pattern		SFD detect	Process following to SFD
		uncoded	Coded		
1	0	SFD1 [31:0]	-	Uncoded	Determined as uncoded
1	1	SFD2 [31:0]	-	Uncoded	Determined as uncoded
0	0	SFD1 [31:0]	-	Uncoded	Determined as uncoded
0	1	SFD2 [31:0]	-	Uncoded	Determined as uncoded

When using IEEE 802.15.4g (2bytes SFD), recommended configuration will be as following table.

Register name	Address (Bank 0)	Setting value
SFD1_SET1	0x3a	0x09
SFD1_SET2	0x3b	0x72
SFD1_SET3	0x3c	0xF6
SFD1_SET4	0x3d	0x72
SFD2_SET1	0x3e	0x5E
SFD2_SET2	0x3f	0x70
SFD2_SET3	0x40	0xC6
SFD2_SET4	0x41	0xB4

●AUTO_ACK function

ML7396 family supports AUTO_ACK function to assist MCU operation in acknowledge packet (hereafter Ack packet) transmission. Followings are detail of the AUTO_ACK function.

[Notes when using AUTO_ACK function]

1. AUTO_ACK function can not be used with FEC function, please set FEC_EN ([FEC/CRC_SET:B0 0x46(6)])=0b1. When MCU handls Ack packet, FEC function can be used.
2. When TX packet and RX packet use diferent FCS length, especially note on the following;
   If transmissting Ack packet before reading out RX data from FIFO, TX packet FCS length will be applied to the unread RX data stored into FIFO. Therefore, RX data can not be read out correctly. Under this case, before start to read RX data, forcibly set RX packet FCS length by using [FEC/CRC_SET:B0 0x46] register.
   (Above condition will meet when the data packet uses 32bit FCS and Ack packet uses 16bit FCS. Since ML7396 fammily does not support 32bit FCS Ack packet.)

*Ack transmission (MCU requests transmitting Ack packet)

1) Analyzing Frame Control Field in RX data, and if Ack request bit is set to 0b1, then obtain Sequence Number from RX data.

2) After RX completion, performing CRC check and if FCS is OK, then transit to TX_ON state automatically for Ack packet transmission preparation. (At this time, RX completion interrupt (INT[18]/[19] group3) will be generated.)

3) MCU analyzes Address field and Pending data in received data, and it decide to transmit Ack packet, set Ack packet to [ACK_FRAME1:B0 0x53] and [ACK_FRAME2:B0 0x54] registers.
   Note: It is dpossible to determine Ack packet transmittion by reading MAC header. Therefore Ack packet setting is possible before RX completion.
   If there is a Pending data, the Frame Pending bit should be set to 0b1 by [ACK_FRAME1:B0 0x53] register.

4) After completing TX_ON state transition, Auto_Ack ready interrupt (INT[24] group4) will be generated.
   After confirming Ack_ready interrupt, set ACK_SEND ([AUTO_ACK_SET:B0 0x55(1)])=0b1 .

5) Transmitting Ack packet
   Frame Control Field is filled with the setting data into [ACK_FRAME1:B0 0x53] and [ACK_FRAME2:B0 0x54] registers.
   Sequence Number Field is automatically filled with sequence number obtained from received data.

6) After Ack packet transmission is completed, TX completion interrupt (INT[16]/[17] group 3) will be generated.
   Note: RF status keeps TX_ON state, If return to IDLE state, set SET_TRX ([RF_STATUS:B0 0x6C(3-0)]) =0b1000 (TRX_OFF).

*Ack transmission (MCU requests to stop Ack packet transmission)

1) Analyzing Frame Control Field in RX data, and if Ack request bit is set to 0b1, then obtain Sequence Number from RX data.

2) After RX completion, performing CRC check and if FCS is OK, then transit to TX_ON state automatically for Ack packet transmission preparation. (At this time, RX completion interrupt (INT[18]/[19] group3) will be generated.)

3) After completing TX_ON state transition, Auto_Ack ready interrupt (INT[24] group4) will be generated.

4) MCU analyzes Address field and Pending data in received data, and it decide not to send Ack packet, issuing PHY reset by [RST_SET:B0 0x01]=0x88 and then set ACK_STOP ([AUTO_ACK_SET:B0 0x55(0)])=0b1.
   ML7396 family aborts Ack packet and RF status will be back to TRX_OFF state automatically.

5) Set ACK_STOP ([AUTO_ACK_SET:B0 0x46(0)])=0b0. If AckAuto_Ack ready interrupt (INT[24] group4) is already generated, please clear the interrupt.

*Ack Transmission (Ack packet transmission using Ack timer)
Condition: AUTO_TIMER_EN ([ACK_TIMER_EN:B0 0x52(0)])=0b1.

1) Analyzing Frame Control Field in RX data, and if Ack request bit is set to 0b1, then obtain Sequence Number from RX data.

2) After RX completion, performing CRC check and if FCS is OK, then transit to TX_ON state automatically for Ack packet transmission preparation. (At this time, RX completion interrupt (INT[18]/[19]) will be generated.)

3) After Completing TX_ON state transition, Ack timer starts counting and Auto_Ack ready interrupt (INT[24] group4) will be generated.

4) After elapsing the period defined by [ACK_TIMER_L/H:B0 0x50/51] registers, Ack packet will be transmitted.

5) After Ack packet trnasumission is completed, TX completion interrupt (INT[]16)/[17] group3) will be generated.
Note: RF status keeps TX_ON state, If return to IDLE state, set SET_TRX ([RF_STATUS:B0 0x6C(3-0)]) =0b1000 (TRX_OFF).

[Additional Function]
• By setting CCA_AUTO_EN ([CCA_CNTRL:B0 0x15(7)])=0b1, it is possible to execute CCA operation automatically for Ack packet transmission.

*Ack Reception
Condition: AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)])=0b1.

1) After competing transmission of data packet with Ack request, TX completion interrupt (INT[16]/[17] group3) will be generated, then transit to RX_ON state automatically for Ack packet to reception.

2) After RX completion for Ack packet, RX completion interrupt (INT[18]/[19]) will be generated.
Note: RF status keeps RX_ON state, If return to IDLE state, set SET_TRX ([RF_STATUS:B0 0x6C(3-0)]) =0b1000 (TRX_OFF).

*Ack Reception (Terminate Ack packet waiting)
Condition: AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)])=0b1.

1) After competing transmission of data packet with Ack request, TX completion interrupt (INT[16]/[17] group3) will be generated, then transit to RX_ON state automatically for Ack packet to reception.

2) If MCU determined to terminate Ack packet waiting, set ACK_STOP ([AUTO_ACK_SET:B0 0x55(0)]) =0b1.
ML7396 family aborts Ack packet waiting and RF status will be back to TRX_OFF state automatically.

●Address filtering function:

ML7396 family has a function to receive RX packet which MAC header has specific code at yellow highlighted field in the MAC header (IEEE802.15.4) as below. By using [ADDFIL_CNTRL:B2 0x20] register, comparing field is selected from PANID, 64bit address, 16bit short address or I/G bit. Each specific code are defined by [PANID_L:B2 0x61] to [SHT_ADDR1_H:B2 0x6E] registers. Source address is out of comparing target.

Byte：2	1	0 / 2	0/2/8	0 / 2	0/2/8	variable	2
Frame Control	**Sequence Number**	**Destination PAN identifier**	**Destination Address**	**Source PAN identifier**	**Source address**	**Frame payload**	**Frame Chack sequence**
		Addressing fields					
MAC header						**MAC payload**	**MAC footer**

Bits：0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame type	**Security enabled**	**Frame pending**	**Ack. req.**	**PAN-ID Compression**	**Reserved**	**Dest. addressing mode**	**Frame Version**	**Source addressing mode**

Fig. MAC header and Frame Control Field

Destination Addressing Mode
- 00: Beacon or Ack Packet (Beacon packet is always received, Ack packet reception can be selectable)
- 01: Reserved (Does not receive)
- 10: 16 bits address
- 11: 64 bits address

Destination.PAN-ID
- 0xFFFF: Broadcasting, then always receive this packet regardless to address mode.
- 16 bits address mode: Receive packet if PAN_ID (setting vslue) is matched.
- 64 bits address mode: Ignoring this field.

Destination Address
- 16 bit address mode: Receive packet only if short address (setting value) is matched.
- 64 bit address mode: Receive packet only if 64 bits address is matched, or I/G bit is set to 0b1 (multicast).

References:

When Address Filtering function is enabled, packet analisis will be executed. Therefore when using RX_ACK CANCEL ([AUTO_ACK_SET:B0 0x55(7)]) function, Address Filtering function should be enabled, since packet anlisis is need uted to detect Ack packet. For details, please refer to [AUTO_ACK_SET:B0 0x55] register.

When address fields are mismatch with set value, following procedure is determined by the setting to ADDFIL_NG_SET ([PACKET_MODE_SET:B0 0x45(5)]) and packet discard completion interrupt (INT[03] group1) timing is defined by ADDFIL_IDLE_DET ([PACKET_MODE_SET:B0 0x45(0)]).

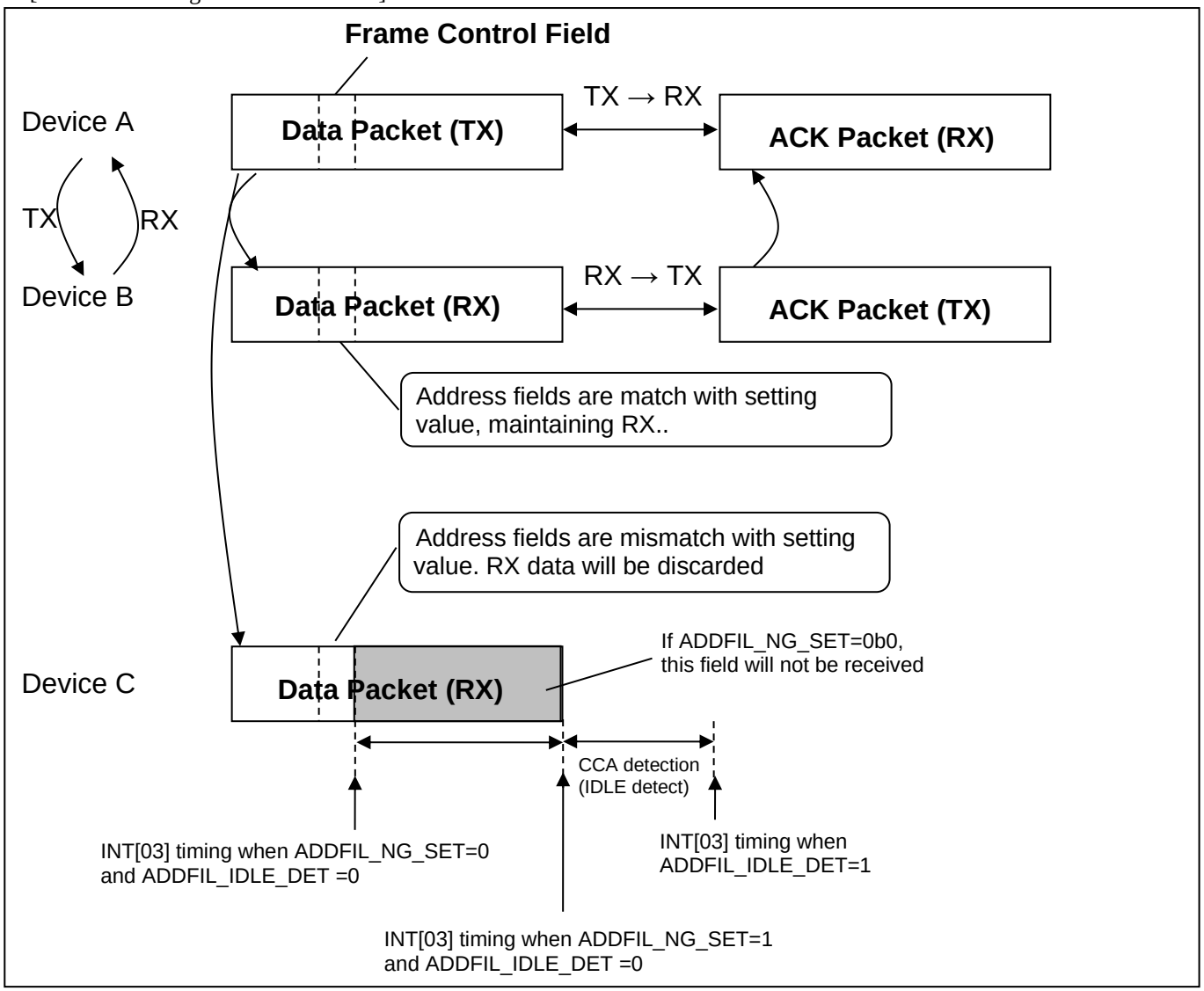
ADDFIL_NG_SET (bit5)
0b1: When address-mismatch is detected, discarding RX data after RX completetion.
0b0: When address-mismatch is detected, discarding RX data immediately.

ADDFIL_IDLE_DET (bit0)
0b1: After discarding RX data perform CCA and "IDLE" is detected, INT[03] will be generated.
0b0: After discarding RX data, INT[03] will be generated immediately.

When RX data is discarded, adding to INT[03] generation, discarded packet can be counted up to 1023 and result stored in [DISCARD_COUNT0:B2 0x6F] and [DISCARD_COUNT1:B2 0x70] registers.

[Note]
When using Address Filtering function while FEC function is enabled, if INT[03] is notified. PHY reset by [RST_SET:B0 0x01] should be required. If not issuing PHY reset, after that, ML7396 can not receive packet with address match also.

[Address Filtering function overview]

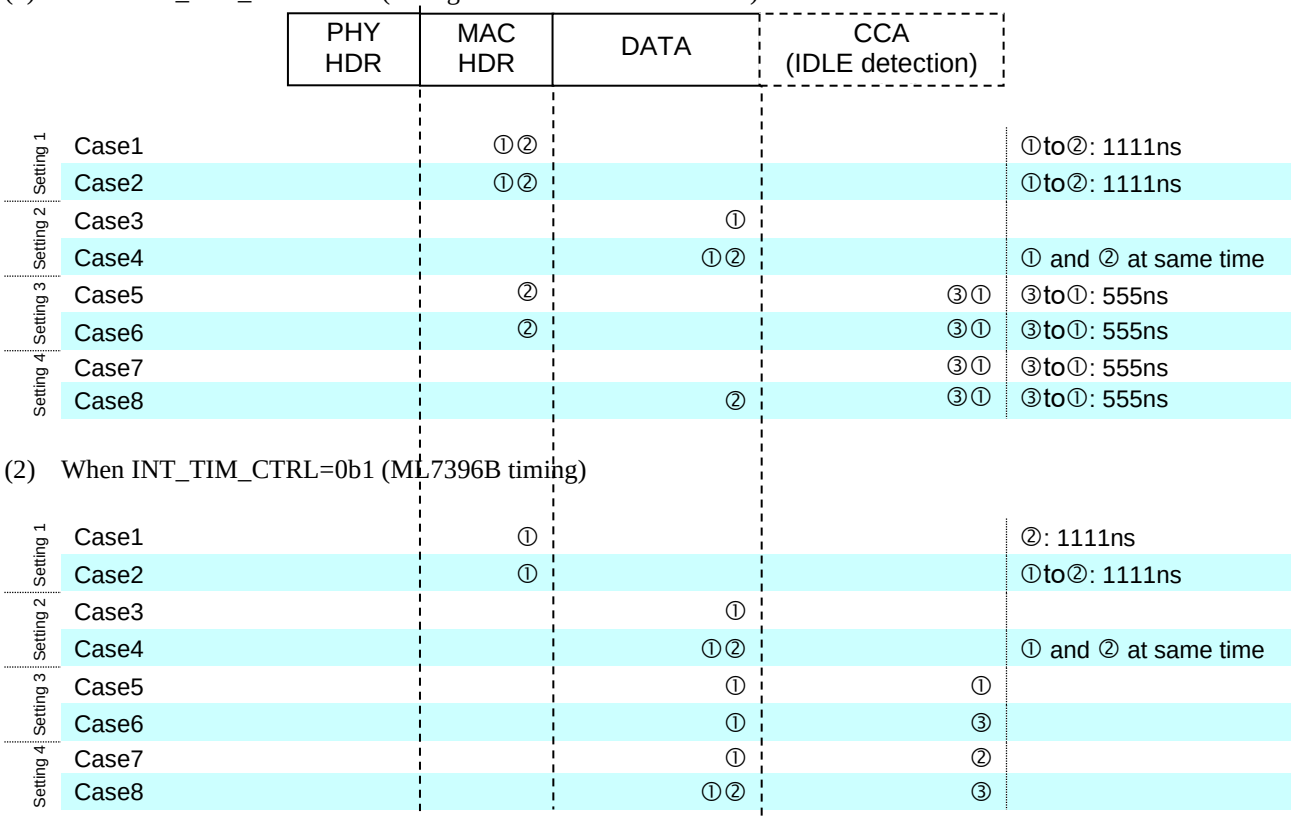


[Interrupts timing when using INT_TIM_CTRL]
By setting INT_TIM_CTRL ([PLL_MOD/DIO_SEL:B0 0x69(6)]), it is possible to select interrupt timing during Address filtering mode.

According to the ADDFIL_NG_SET or ADDFIL_IDLE_DET setting and CRC result in the RX packet, interrupt generation timings of ①Packet discard completion interrupt, ②CRC error interrupt, and ③CCA completion interrupt, will become as below figures.

			Setting 1		Setting 2		Setting 3		Setting 4	
	Setting	setting register	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8
Input	Discard packet after address mismatch	ADDFIL_NG_SET=0b0	O	O	-	-	O	O	-	-
	Discar packet after address mismatch and RX completion	ADDFIL_NG_SET=0b1	-	-	O	O	-	-	O	O
	Execute CCA after address mismatch	ADDFIL_IDLE_DET=0b 1	-	-	-	-	O	O	O	O
	CRC_OK	-	O	-	O	-	O	-	O	-
	CRC_NG	-	-	O	-	O	-	O	-	O
Interrupt result	Packet discard cpmpletion interrupt	INT[3] [INT_SOURCE_GRP1]	O	O	O	O	O	O	O	O
	CRC error interrupt	INT[21/20] [INT_SOURCE_GRP3]	O	O	-	O	O	O	-	O
	CCA completion interrupt	INT[8] [INT_SOURCE_GRP2]	-	-	-	-	O	O	O	O

(1) When INT_TIM_CTRL=0b0 (timing is comatible with ML7396)



(2) When INT_TIM_CTRL=0b1 (ML7396B timing)

●Interrupt generation function

ML7396 family supports intterupt generation function. When interrupt occurs, SINTN pin (#10) will become “Low” to notify interrupt to the host MCU.
Interrupt elements are divided into 4groups, [INT_SOURCE_GRP1:B0 0x24] to [INT_SOURCE_GRP4:B0 0x27]. Each interrupt elements can be masked by using [INT_EN_GRP1:B0 0x2A] to [INT_EN_GRP4] registers.

Note: If one of unmask interrupt event occurs, SINTN maintains “Low”.

○Interrupt events table

Each interrupt events is described as belo table.

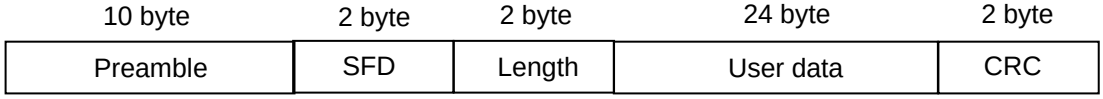
Group	Name	Function:
INT_SOURCE_GRP4	INT[25]	PLL unlock interrupt
	INT[24]	Auto_Ack ready interrupt
INT_SOURCE_GRP3	INT[23]	FIFO1 TX data request accept completion interrupt
	INT[22]	FIFO0 TX data request accept completion interrupt
	INT[21]	FIFO1 CRC error interrupt
	INT[20]	FIFO0 CRC error interrupt
	INT[19]	FIFO1 RX completion interrupt
	INT[18]	FIFO0 RX completion interrupt
	INT[17]	FIFO1 TX completion interrupt
	INT[16]	FIFO0 TX completion interrupt
INT_SOURCE_GRP2	INT[15]	TX FIFO access error interrupt
	INT[14]	RX FIFO access error interrupt
	INT[13]	TX Length error interrupt
	INT[12]	RX Length error interrupt
	INT[11]	SFD detection interrupt
	INT[10]	RF state transition completion interrupt
	INT[09]	Diversity search completion interrupt
	INT[08]	CCA completion interrupt
INT_SOURCE_GRP1	-	no function
	-	no function
	INT[05]	FIFO_Full interrupt
	INT[04]	FOFO_Empty interrupy
	INT[03]	Packet discard competion interrupt
	INT[02]	VCO calbration completion interrupt
	INT[01]	Reserved
	INT[00]	Clock stabilization completion interrupt

○Interrupt generation timing

In each interrupt generation, timing from reference point to interrupt interrupt generation (nitification) are described in the following table. Timeout procedure for interrupt notification waiting, are also described below.

[Note]
(1)The values are decribed in units of "symbol time" in the below table is the value at 100kbps. If using other data, please use 20, 5, and 2.5 for 50kbps, 200kbps, and 400kbps, respectively.

(2)Below table uses the following format of TX/RX data.



(3)Even if each interrupt notification is masked, in case of interrupt occurrence, interrupt elements are stored internnaly. Therefore, as soon as interrupt notification is unmasked, interrupt will generate.

Interrupt notification		Reference point	Time from reference point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	RESETN release (upon power-on)	660µs
		SLEEP release (recovered from SLEEP)	660µs
INT[1]			
INT[2]	VCO calibration completion	VCO calibration start	230µs
INT[3]	Packet discard completion during Address Filtering function	SFD detection	(1)If ADDFIL_NG_SET([PACKET_MODE_SET:B0 0x45(5)]) =0b0, the right timing to address mismatch detection. (2)If ADDFIL_NG_SET([PACKET_MODE_SET:B0 0x45(5)]) =0b1, (When FEC is disabled) 28byte (Length to CRC) * 8bit * 10(symbol time) + process delay(5.55µs) =2245.55µs (When FEC is enabled) 28byte (Length to CRC) * 2 * 8bit *10(symbol time) + process delay(315.55µs) =4795.55µs
INT[4]	FIFO-Empty detection	(TX) TX_ON command (* 1)	Empty trigger level is set to 0x02 (When FEC is disabled) 37 byte (preamble to 23th data) * 8bit * 10 (symbol time) =2960µs (When FEC is enabled) {12byte (preamble to SFD) + 25byte(Length to 23th data) * 2} * 8bit* 10(symbol time) + RF wake-up & process delay (106µs) =5066µs
		(RX)	By FIFO read, remaining FIFO data is under trigger level
INT[5]	FIFO-Full detection	(TX)	By FIDO write, FIFO usage exceeds trigger level
		(RX) SFD detection	Full trigger level is set to 0x05 (When FEC is disabled) 8byte (Length + 6th data) * 8bit * 10(symbol time) =640µs (Wwhen FEC is enabled) 8byte (Length + 6th data) * 8bit * 2 * 10(symbol time) + process delay(305µs) =1585µs
(INT[6])	-		
(INT[7])	-		

(* 1) Befor issuing TX_ON, writing full-length TX data into a FIFO.

Interrupt notification		Reference point	Time from reference point to interrupt generation or interrupt generation timing
INT[8]	CCA completion	CCA execution start	(1)Normal mode {ED value calculation averaging time + IDLE_WAIT setting [IDLE_WAIT_L/H:B0 0x17/18] + 2 (filter stbilization)} * A/D conversion time (2) IDLE detection mode ○ IDLE detection case {ED value calculation averaging time + IDLE_WAIT setting [IDLE_WAIT_L/H:B0 0x17/18] + 2(filter stbilization)} * A/D conversion time ○ BUSY detection case (ED value calculation averaging tim+ 2(filter stbilization)) * A/D conversion Note: A/D conversion time can be changed by ADC_CLK_SET (ADC_CLK_SET:B0 0x08(4)). ADC conversion time= 17.7µs (1.8MHz), 16µs (2.0MHz) Note: When executing CCA during diversity, set the abort timer for CCA completion notification. When CCA is run during diversity, since there is a case CCA completion is not notified.
INT[9]	Diversity search completion	-	diversity search completion
INT[10]	RF state transition completion	TX_ON command	(IDLE) 122µs (RX) 89µs
		RX_ON command	(IDLE) 136µs (TX) 142µs
		TRX_OFF command	(TX) 410µs (RX) 11µs
		Force_TRX_OFF command	(TX) 410µs (RX) 10µs
INT[11]	SFD detection	-	SFD detection
INT[12]	RX length error	SFD detection	80µs
INT[13]	TX length error	-	Writing TX data to a FIFO
INT[14]	RX FIFO access error	-	(1).receiving 3rd packet with remaining RX dara in both FIFO0 and FIFO1 (2) overfolow occurs because FIFO read is too slow (3) underflow occurs because too many FIFO data is read
INT[15]	TX FIFO access error	-	(1) writing 3rd packet with remaining TX data in both FIFO0 and FIFO1 (2) FIFO overflow when writing (3) FIFO underflow (or no data) when transmitting
INT[16] INT[17]	FIFO0/FIFO1 TX completion	TX_ON command (* 1)	(When FEC is disabled) 40byte (preamble to CRC) * 8bit * 10(symbol time) + RF wake-up & process delay(154µs) =3354µs (When FEC is enabled) {12byte (preamble to SFD) + 28byte (Length to CRC) * 2} * 8bit * 10(symbol time) + RF wake-up & process delay(224µs) =5664µs

(* 1) Befor issuing TX_ON, writing full-length TX data into a FIFO.

Interrupt notification		Reference point	Time from reference point to interrupt generation or interrupt generation timing
INT[18] INT[19]	FIFO0/FIFO1 RX completion	SFD detection	(When FEC is disabled) 28byte (Length to CRC) * 8bit * 10(symbol time + process delay(5μs) =2245μs (When FEC is enabled) 28byte (Length to CRC) * 2 * 8bit * 10(symbol time) + process delay(315μs) =4795μs
INT[20] INT[21]	FIFO0/FIFO1CRC error detection	SFD detection	(With FEC disabled) 28byte (Length to CRC) *8bit * 10(symbol time) + process delay(5μs) =2245μs (With FEC enabled) 28byte (Length to CRC) * 2 * 8bit * 10(symbol time + process delay(315μs) =4795μs
INT[22] INT[23]	FIFO0/FIFO1 TX data request accept completion	-	After full-length data are written into a FIFO
INT[24]	AutoAck ready	RX completion	92us
INT[25]	PLL unlock detection	-	(TX) during TX after PA enable (RX) during RX after RX enable

○Clearing interrupt condition

The following table shows the condition of clearing each interrupt.

Interrupt notification		Requirements for clearing interrupt
INT[0]	CLK stabilization completion	After the interrupt generation
INT[1]	Reserved	
INT[2]	VCO calibration completion	After the interrupt generation
INT[3]	Packet discard completion during Address Filtering function	After the interrupt generation
INT[4]	FIFO-Empty detection	After the interrupt generation (must clear before the next FIFO-Empty trigger timing)
INT[5]	FIFO-Full detection	After the interrupt generation (must clear before the next FIFO-Full trigger timing)
INT[6]	-	
INT[7]	-	
INT[8]	CCA completion	After the interrupt generation (must clear before the next CCA execution) * clearing interrupt erases CCA result as well
INT[9]	Diversity search completion	After RX completion interrupt(INT[18/19]), must cleare with RX completion interrupt * during RECEIVE stare, clearing is prohibited.
INT[10]	RF state transition completion	After the interrupt generation
INT[11]	SFD detection	After the interrupt generation
INT[12]	RX length error	After the interrupt generation
INT[13]	TX length error	After the interrupt generation
INT[14]	RX FIFO access error	After the interrupt generation
INT[15]	TX FIFO access error	After the interrupt generation (must clear before the next packet transmission)
INT[16/17]	FIFO0/FIFO1 TX completion	After the interrupt generation (must clear before the next packet transmission)
INT[18/19]	FIFO0/FIFO1 RX completion	After the interrupt generation (must clear before the next packet reception)
INT[20/21]	FIFO0/FIFO1CRC error detection	After the interrupt generation * clearing interrupt erases CRC result (CRC_RSLT1/0).
INT[22/23]	FIFO0/FIFO1 TX data request accept completed	After TX completion interrupt (INT[16/17]) (must clear before the next packet transmission) * during TRANSMIT state, clearing is prohibited.
INT[24]	AutoAck ready	After the interrupt generation
INT[25]	PLL unlock detection	After the interrupt generation (must clear before the next packet transmission or reception)

●Temperature Measurement Function

ML7396 family has temeperature measurement function. This temperature information can be from A_MON pin (#24) as analog output or digital information using [TEMP_MON:B0 0x79] register. Analog or digital can be switched by [RSSI/TEMP_OUT:B1 0x03] register.

Notes:
1) Please do not set TEMP_OUT ([RSSI/TEMP_OUT:B1 0x03(4)]) and TEMP_ADC_OUT ([RSSI/TEMP_OUT:B1 0x03(5)]) at the same time. Correct value reading may not be guaranteed.
2) When TEMP_ADC_OUT is set, packet data is not able to receive normally.

[Analog output]
ML7396 family has current source circuits and its current flow through 75kΩ to A_MON pin (#24). From voltage information, temperature information can be obtained.

Current from currwnt source circuits are 10μA at 25˚C. Following formula can be used to calculate temperature from the current.

Itemp = (273+ Temp) / (273+25) * 10 (μA)

Therefore, if 75kΩ resister is connected, temprature can be calculated usng following formula.

Vamon = (273+ Temp) / (275+25) * 10E-6 * 75000

If temprature is -40˚C to +85˚C, Vamon will be 0.59V to 0.9V.
Therefore temperature can be calculated from voltage using following formula.

Temp = Vamon * 397.3 - 273

[Digital output]
Digital temperature information is using 6bits ADC to convert from the above analog information. Internally, 4samples information are added and indicates as 8bits information in [TEMP_MON:B0 0x79] register. Ignorimg low 2 bits, upper 6bits are used for average temperature information.
Temperature information is updated every 17.8μs. (if 2MHz is selected in [ADC_CLK_SET:B0 0x08] register, it is updated every 16 μs)

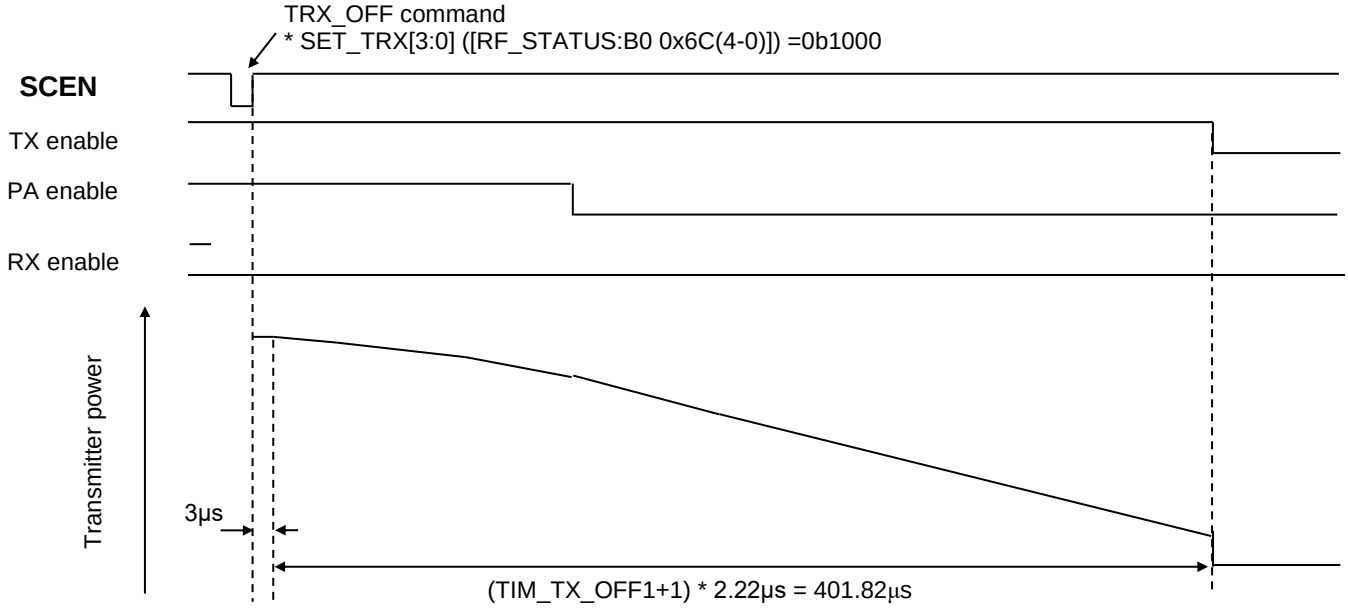
●Ramp control function

ML7396 has Ramp control function. This function will contribute reducing spurious emission when transmission is terminated. Ramp control will be executed when switching TX_ON to TRX_OFF state and TX_ON to RX_ON state.

The following are control bits retative with ramp control function.
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]): Ramp control enable bit
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]): Ramp down timing adjustment when transitioning from TX_ON to TRX_OFF.
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]): RX_ON timing adjustment when transitioning from TX_ON to RX_ON
TIM_TX_OFF2[5:0] [2DIV_GAIN_CONTRL:B0 0x6E(7-2)]): Ramp down timing adjustment when transitioning from TX_ON to RX_ON.

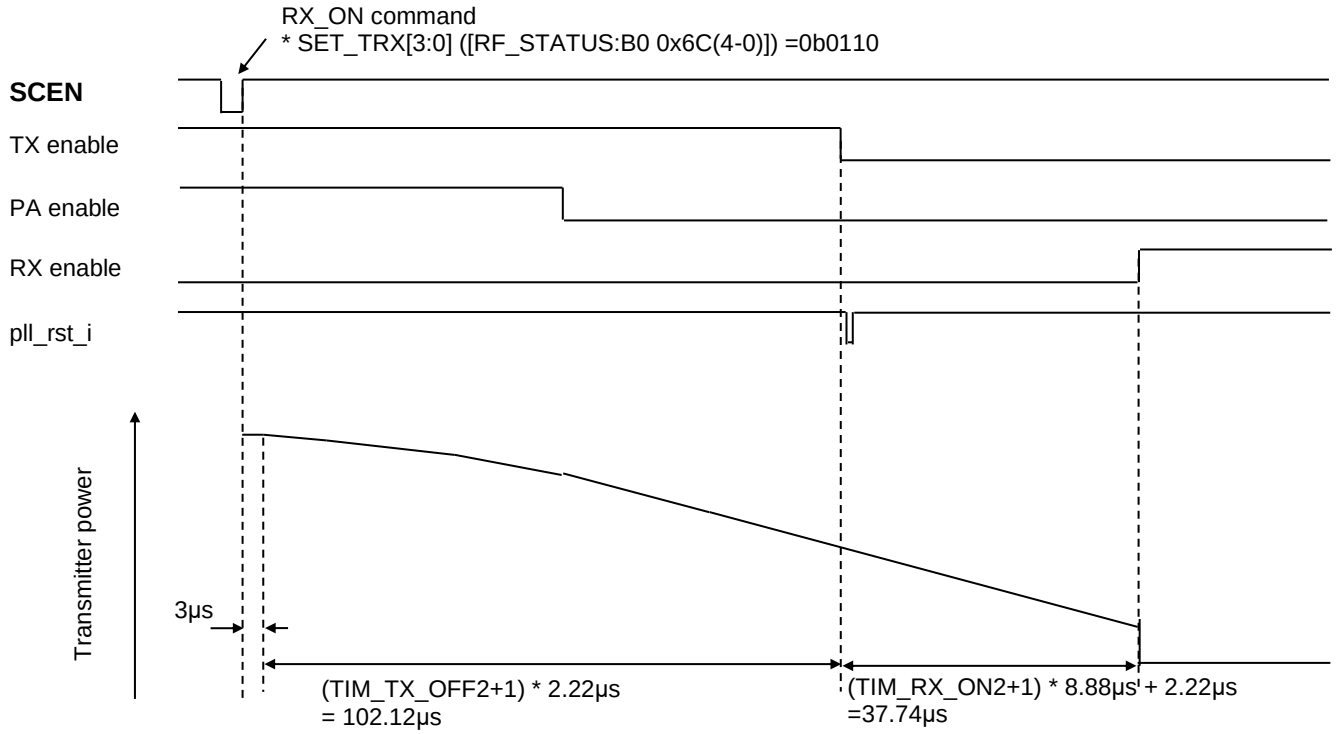
[Operation Overview]
(1) Ramp down timing when transitioning from TX_ON to TRX_OFF

[Condition]
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b1
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)] =0xb4(400 µs), 0x42 (150µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]) =0b011
TIM_TX_OFF2[5:0] ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01



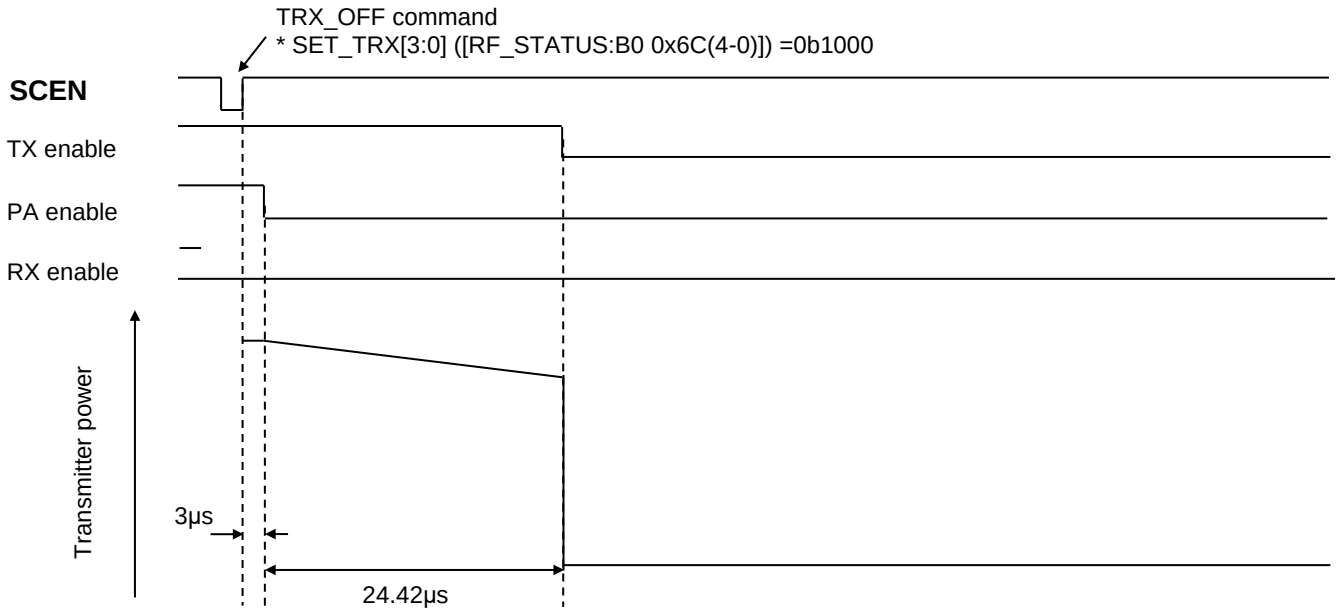
(2) Ramp down timing when transitioning from TX_ON to RX_ON

[Condition]
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) = 0b1
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]) =0xb4 (400 μs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-5)]) =0b011
TIM_TX_OFF2 ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01



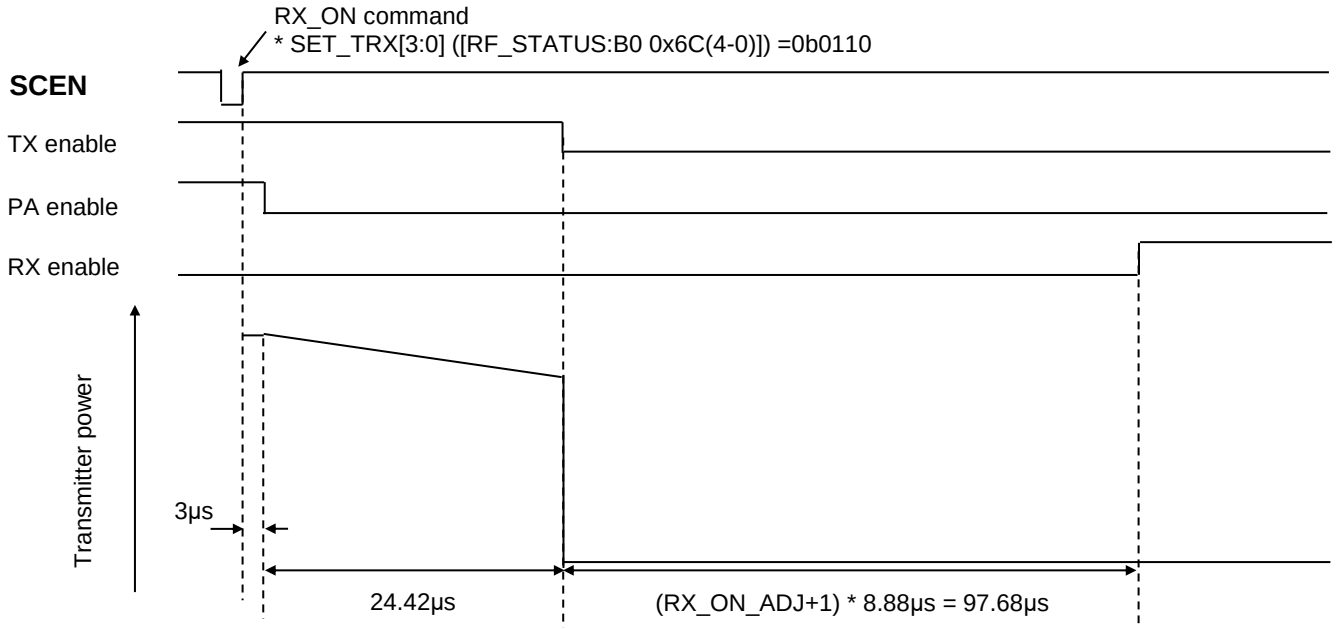
(3) Ramp down timing when transitioning from TX_ON to TRX_OFF (ramp control disabled)

[Condition]
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b0
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]) =0xb4 (400 µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]) =0b011
TIM_TX_OFF2 ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01



(4) Ramp down timing when transitioning from TX_ON to RX_ON (ramp control disabled)

[Condition]
TXOFF_RAMP_EN ([RAMP_CNTRL:B2 0x2C(4)]) =0b0
TIM_TX_OFF1[7:0] ([TX_OFF_ADD1:B1 0x55(7-0)]) =0xb4 (400 µs)
TIM_RX_ON2[2:0] ([RX_ON_ADJ2:B1 0x3F(6-4)]) =0b011
TIM_TX_OFF2[5:0] ([2DIV_GAIN_CONTRL:B0 0x6E(7-2)]) =0b1011_01
RX_ON_ADJ[7:0] ([RX_ON_ADJ:B2 0x22(7-0)]) =0x0A



■RF Configuration

●Programming Channel Frequency

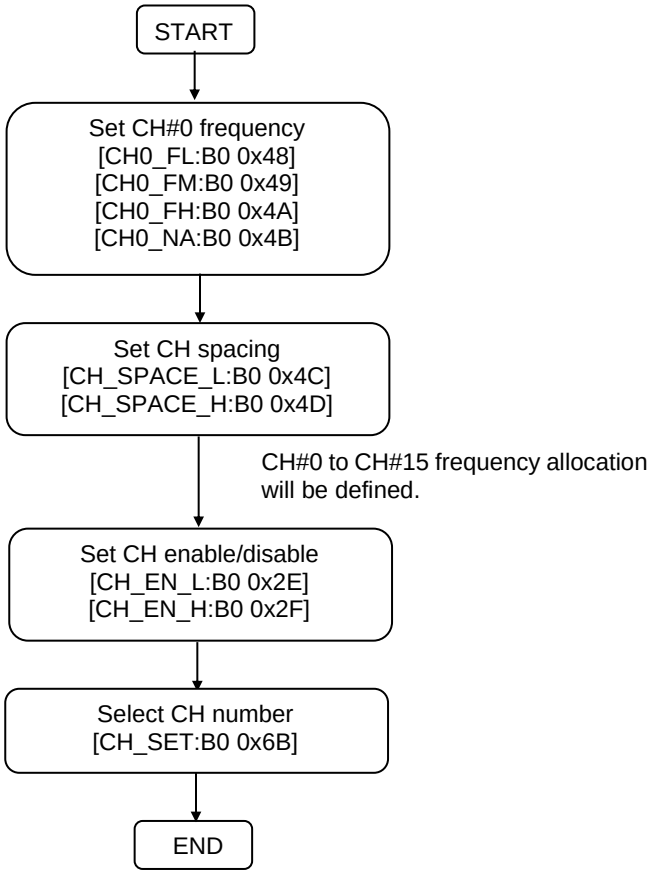
Maximum 16 channels can be selected. (CH#0 to CH#15) Cahnnel allocation is defined by channel #0 frequency specified by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49], [CH0_FH:B0 0x4A] and [CH0_NA:B0 0x4B] registers, and channel spacing specified by [CH_SPACE_L:B0 0x4C] and [CH_SPACE_H:B0 0x4D] registers.
16 channels can be enabled or disabled by [CH_EN_L:B0 0x2E] and [CH_EN_H:B0 0x2F] registers.
RF channel is set as channel number (#0 to #15) at [CH_SET:B0 0x6B] register

Notes:
1) Frequency range (from CH#0 to CH#15) can not include integer multiple of 36MHz. (ex: 900MHz, 936MHz)
2) The channel frequency must meet the following condition. If the following condition can not meet, please change the channel #0 frequency or disabling channels that can not meet the condition by [CH_EN_L:B0 0x2E] and [CH_EN_H:B0 0x2F] register.

   36MHz * n + 2.2MHz ≤ channel frequency < 36MHz * (n+1) – 500kHz * n=integer

3) If the above condition can not be met, expected channel frequency is not functional or PLL may not be locked.

[Channel frequency programming flow]



○Programming Channel#0 Frequency

Channel #0 frequency can be set by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49], [CH_FH:B0 0x4A] and [CH_NA:B0 0x4B] registers.

Each setting parameters for channel #0 can be calculated using the following formula.

$N = f / f_{REF} / P$ (Integer part)
$A = f / f_{REF} - N * P$ (Integer part)
$F = \{f / f_{REF} - (N * P + A)\} * 2^{20}$ (Integer part) [note: useing 20bit circuit]

Here

f : Channel #0 fequency
f_{REF} : PLL reference frequency (input clock=36MHz)
P : Dual modulus parameter (fixed to 4)
N : N-counter parameter
A : A-counter parameter
F : F-counter parameter

And frequency error can be calculated using the following formula.

$ferr = f - [f_{REF} * \{(N * P + A) + F/2^{20}\}]$

[Example] When set channel #0 frequecy to 923.1MHz, the calculations are as follows. (f_{REF} = 36MHz)

N = 923.1MHz / 36MHz / 4 (Integer part) = 6
A = 923.1MHz / 36MMHz- 6 * 4 (Integer part) = 1
$F = \{923.\ 1MHz / 36MHz - (6 *4 + 1)\} *2^{20}$ (Integer part) = 672836 (0xA4444)

Therefore

[CH0_FL:B0 0x48] = 0x44
[CH0_FM:B0 0x49] = 0x44
[CH0_FH:B0 0x4A] = 0x0A
[CH0_NA:B0 0x4B] = 0x61

Feuqency error will be $ferr = 923.\ 1MHz - [36MHz * \{(6 * 4 + 1) + 672836 / 2^{20}\}] = +31.7Hz$

○Programming Channel pace

Channel space can be set by [CH_SPACE_L:B0 0x4C] and [CH_SPACE_H:B0 0x4D] registers.
Channel space is frequency space between centre frequency of given channel and that of adjacent channel.

Channel space setting value can be calculated using the following formula.

$CH\_SP\_F = \{f_{SP} / f_{REF}\} * 2^{20}$ (Integr part) [note: using 20bit circuit]

Here

CH_SP_F : Channel space setting
f_{SP} : Channel space [MHz]
f_{REF} : PLL reference frequency (input clock=36MHz)

[Example] When set channel space is 400kHz, the calculation are as follow. (f_{REF} = 36MHz)

$CH\_SP\_F = \{0.4MHz / 36MHz\} * 2^{20}$ (Integer part) = 11650 (0x2D82)

Therefore

[CH_SPACE_L:B0 0x4C] = 0x82
[CH_SPACE_H:B0 0x4D] = 0x2D

●Programming IF Frequency

In order to support various data rate , RX filters have to be optimised. The RX filter can be selected according to the IF frequency. IF frequency can be set by using [IF_FREQ_H: B1 0x0A] and [IF_FREQ_L: B1 0x0B] registers. (default: 178.22kHz) According to the RATE[2:0] ([DATA_SET:B0 0x47(2-0)]) setting and NBO_SEL([DATA_SET:B0 0x47(7)]) setting, IF frequency will be multiplied automatically as following table.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	x2	x4	x4	x6	x6
0b1	x2	x2	-	x4	-

IF frequency value should be set as the multiplied IF frequency corresponding to each data rate becomes the values described in the following table.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	500kHz	720kHz	900kHz	1300kHz	2100kHz
0b1	500kHz	720kHz	-	1300kHz	-

[Notes]

1. NBO_SEL=0b1 can not be set for the data rate other than 50kbps, 100kbps and 200kbps.
2. For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file .

If AFC is used, IF frequency setting in [IF _FREQ_AFC_H: B0 0x30] and [IF_FREQ_AFC_L: B0 0x31] registers will be used. IF frequency setting for AFC operation is same as normal operation.

If CCA is used to detect channel carrier power, required RX filter bandwidth may be different. [IF _FREQ_CCA_H: B1 0x0C] and [IF_FREQ_CCA_L: B1 0x57] registers must be used for CCA purpose. During CCA operation IF frequency calculation becomes as below.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	x2	x6	x8	x8	x8
0b1	x2	x2	-	x6	-

IF frequency value for CCA operation should be set as the multiplied IF frequency corresponding to each data rate becomes the values described in the following table.

NBO_SEL	Data rate				
	50kbps	100kbps	150kbps	200kbps	400kbps
0b0	500kHz	1500kHz	1450kHz	2000kHz	2100kHz
0b1	500kHz	720kHz	-	1500kHz	-

[Notes]

1. NBO_SEL=0b1 can not be set for the data rate other than 50kbps, 100kbps and 200kbps.
2. For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file..

IF frequency setting value can be calculated using the following formula.

$$IF\_FREQ = \{f_{IF} / f_{REF}\} * 2^{20} \text{ (Integr part) [note: using 20bit circuit]}$$

Here

IF_FREQ : IF frequency setting
f_{IF} : IF frequency [MHz]
f_{REF} : PLL reference frequency (input clock=36MHz)

[Example] When set IF frequency is 178.22kHz, the calculation are as follow. (f_{REF} = 36MHz)

IF_FREQ = {0.17822MHz / 36MHz} * 2^{20} (Integer part) = 5191 (0x1447)

Therefore

[IF_FREQ_H] = 0x14
[IF_FREQ_L] = 0x47

●Programming BPF band width

For normal operation (including AFC) and CCA operation, optimized BPF setting are necessary. To compensating LSI variations, [BPF_ADJ_OFFSET:B1 0x1E] register indicates individual cpmpensation value.

According to the below table, multiplying BPF_OFFSET[6:0] ([BPF_ADJ_OFFSET:B1 0x1E(6-0)]) by the coefficient value corresponding to each data rate. If BPF_OFFSET_POL ([BPF_ADJ_OFFSET:B1 0x1E(7)] = 0b1, incraseing, otherwise (=0b0) decrasing to the default value corresponding each data rate.

Compensated value is set into [BPF_ADJ_H/L:B1 0x0E/0F] and [BPF_AFC_ADJ_H/L:B0 0x32/33] registers for normal operation. For CCA operation, set to [BF_CCA_ADJ_H/L:B1 0x10/11] register.

Following tables show coefficient value and default value corresponfding to RATE[2:0] ([DATA_SET:B0 0x47(2-0)]) setting and NBO_SEL([DATA_SET:B0 0x47(7)]) setting

[When NBO_SEL=0b1]

Data rate [kbps]	RATE[2:0] [B0 0x47]	Normal operation		CCA Operation	
		Coefficient value	Default value	Coefficient value	Default value
50	0b000	1.44	0x034B	1.44	0x034B
100	0b01	1	0x024A	0.48	0x0119
150	0b010	0.8	0x01D4	0.497	0x0122
200	0b010	0.554	0x0144	0.36	0x00D2
400	0b011	0.343	0x00C8	0.343	0x00C8

[When NBO_SEL=0b0]

Data rate [kbps]	RATE[2:0] [B0 0x47]	Normal operation		CCA Operation	
		Coefficient value	Default value	Coefficient value	Default value
50	0b000	1.44	0x034B	1.44	0x034B
100	0b01	1	0x024A	1	0x024A
150	0b010	-	-	-	-
200	0b010	0.554	0x0144	0.48	0x0119
400	0b011	-	-	-	-

[Example]

Condition: Data rate is 100kbps, and [BPF_ADJ_OFFSET:B1 0x1E] =0x91

[BPF_ADJ_H/L:B1 0x0E/0F] = 0x24A + 1 * (0x11) = 0x025B
[BPF_AFC_ADJ_H/L:B0 0x32/33] = 0x24A + 1 * (0x11) = 0x025B
[BF_CCA_ADJ_H/L:B1 0x10/11] = 0x119 + 0.48 * (0x11) = 0x0121

Note: For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file.

●Programming GFSK modulation

By setting GFSK_EN ([DATA_SET;B0 0x47(4)]) =0b1, GFSK modulation can be selected.

○Programming GFSK frequency deviation

In GFSK modulation, frequency deviation can be set by [F_DEV_L:B0 0x4E] and [F_DEV_H:B0 0x4F] registers.
Frequency deviation setting value can be calculated using the following formula.

$F\_DEV = \{f_{DEV} / f_{REF}\} * 2^{20}$ (Integer part) [note: using 20bit circuit]

Here

F_DEV : Frequency deviation setting
f_{DEV} : Frequency deviation [MHz]
f_{REF} : PLL reference frequency (input clock=36MHz)

[Example] When set frequency deviation is 50 kHz at 100kbps, the calculation are as follow. (f_{REF} = 36MHz)

$F\_DEV = \{0.05MHz / 36MHz\} * 2^{20}$ (Integer part) = 1456 (0x05B0)

Therefore

[F_DEV_L:B0 0x4E] = 0xB0
[CH_SPACE_H:B0 0x4D] = 0x05

Following table shows frequency deviation value for each data rate.

Register	Data rate			
	50kbps (m=1)	100kbps (m=1)	150kbps (m=0.5)	200kbps (m=1)
[F_DEV_L:B0 0x4E]	0xD8	0xB0	0x44	0x60
[F_DEV_H:B0 0x4F]	0x02	0x05	0x04	0x0B

Note: For 10kbps, 20kbps, 40kbps setting, please refer to the "Initial register setting" file.

○Programming Gaussian Filter

Gaussian filter can be set by [GFIL00/FSK_FDV1:B0 0x59] to [GFIL11:B0 0x64] registers. BT value of Gaussian filter and setting value to related registers are shown in the below tables. All setting values are described as hexadecimal value.

Remarks: Setting values for BT=0.5 at 100kbps are set as initial values in registers related to Gaussian filter, since initial values of [DATA_SET:B0 0x47] register is GFSK enable and 100kbps setting.

Gaussian filter register setting (for 10kbps/20kbps/40kbps/50kbps/100kbps/150kbps/200kbps)

(HEX)

Register	Address:	bit	BT=1.0	BT=0.5	BT=0.4	BT=0.3	BT=0.25
GFIL00	0x59	[1:0]	0	0	0	0	1
		[3:2]	0	0	0	0	1
		[5:4]	0	0	0	1	1
		[7:6]	0	0	0	1	2
GFIL01	0x5a	[3:0]	0	0	0	1	3
		[7:4]	0	0	1	2	4
GFIL02	0x5b	[3:0]	0	0	1	3	5
		[7:4]	0	1	2	5	6
GFIL03	0x5c	[7:0]	00	01	03	06	07
GFIL04	0x5d	[7:0]	00	03	05	08	09
GFIL05	0x5e	[7:0]	00	05	08	0A	0A
GFIL06	0x5f	[7:0]	00	09	0C	0C	0C
GFIL07	0x60	[7:0]	03	0F	0F	0E	0D
GFIL08	0x61	[7:0]	0B	15	13	10	0E
GFIL09	0x62	[7:0]	1D	1A	17	13	0F
GFIL10	0x63	[7:0]	35	1F	1A	14	10
GFIL11	0x64	[7:0]	40	20	1A	14	12

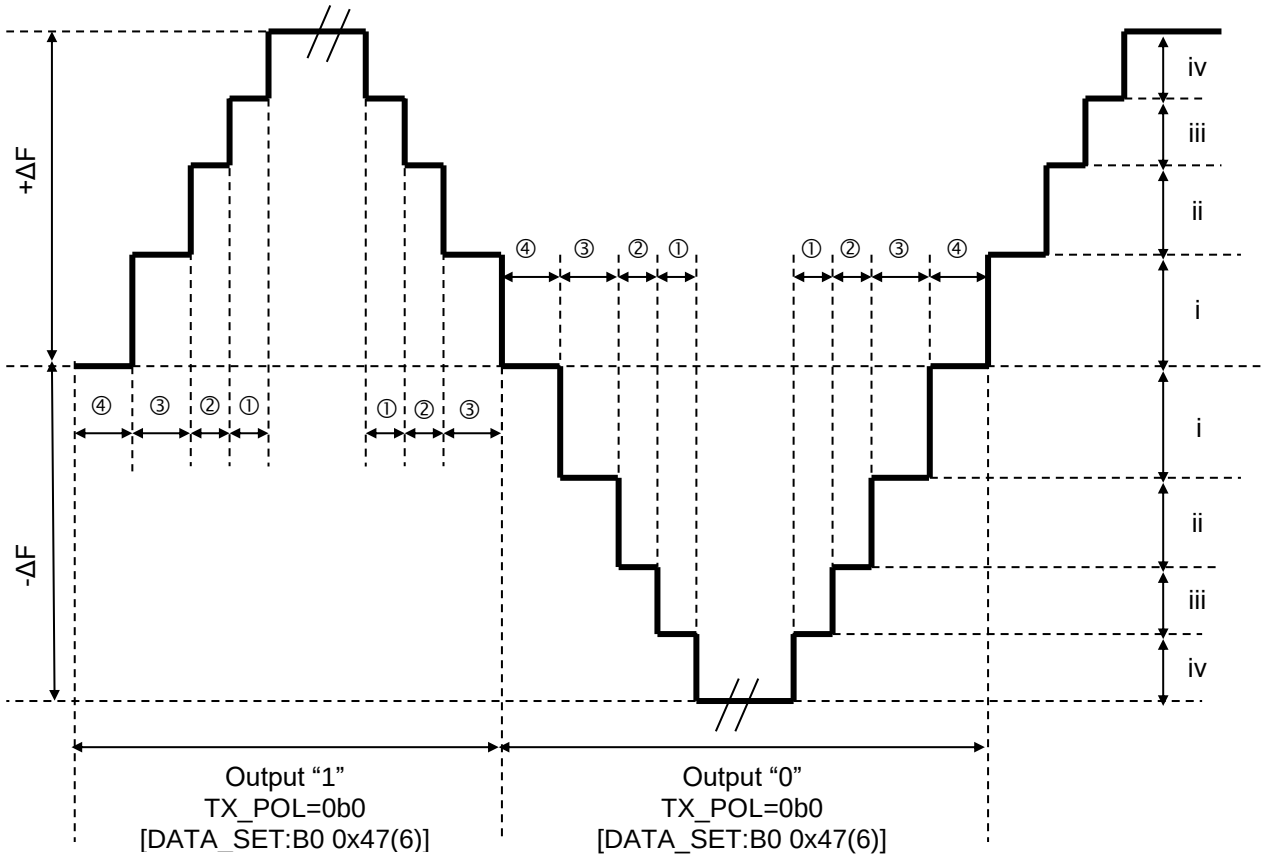
Gaussian filter register setting (for Optional 400kbps)

(HEX)

Register	Address:	bit	BT=1.0	BT=0.5	BT=0.4	BT=0.3	BT=0.25
GFIL00	0x59	[1:0]	0	0	0	0	0
		[3:2]	0	0	0	0	0
		[5:4]	0	0	0	0	0
		[7:6]	0	0	0	0	0
GFIL01	0x5A	[3:0]	0	0	0	0	0
		[7:4]	0	0	0	0	0
GFIL02	0x5B	[3:0]	0	0	0	0	0
		[7:4]	0	0	0	0	1
GFIL03	0x5C	[7:0]	00	00	00	00	01
GFIL04	0x5D	[7:0]	00	00	00	01	03
GFIL05	0x5E	[7:0]	00	00	01	03	05
GFIL06	0x5F	[7:0]	00	00	02	07	09
GFIL07	0x60	[7:0]	00	03	07	0C	0F
GFIL08	0x61	[7:0]	00	0B	10	14	15
GFIL09	0x62	[7:0]	05	1D	1F	1D	1A
GFIL10	0x63	[7:0]	3C	35	2D	24	1F
GFIL11	0x64	[7:0]	7E	40	34	28	20

●Programming FSK modulation

By setting GFSK_EN ([DATA_SET;B0 0x47(4)]) =0b0, FSK modulation can be selected.
In FSK modulation, fine frequency deviation can be set by [GFIL00/FSK_FDEV1:B0 0x59] to [GFIL03/FSK_FDEV4:B0 0x5C] registers. By setting [FSK_TIME1:B0 0x65] to [FSK_TIME4:B0 0x68] registers, FSK timing can be fine tuned.



Symbol	Register	Address	Function	Symbol	Register	Address	Function
i	FSK_FDEV1	0x59	Freq dev 33.4x2(Hz)	①	FSK_TIME1	0x65	Modulation timing by 4MHz counter
ii	FSK_FDEV2	0x5a		②	FSK_TIME2	0x66	
iii	FSK_FDEV3	0x5b		③	FSK_TIME3	0x67	
iv	FSK_FDEV4	0x5c		④	FSK_TIME4	0x68	

[Note]
1. FSK modulation does not support optional 400kbps.

●Programming Data rate changing

50kbps, 100kbps, 200kbps and 400kbps data rate can be chnaged by RATE[2:0] ([DATA_SET:B0 0x47(2-0)]). When changing data rate, below registers may have to be changed.

Note:

1. Depending on data rate, the following chage may not be necessary. For details, please refer to each register setting value corresponding to each data rate in "Initial register setting" file.
2. Please change data rate setting in TRX_OFF state.

[Bank0]

[RATE_SET1:B0 0x04] register (Note: setting is necessary only when changing to 150kbps.)
[RATE_SET2:B0 0x05] register (Note: setting is necessary only when changing to 150kbps.)

[IF_FREQ_AFC_H:B0 0x30] register
[IF_FREQ_AFC_L:B0 0x31] register
[BPF_AFC_ADJ_H:B0 0x32] register
[BPF_AFC_ADJ_L:B0 0x33] register
[TX_PR_LEN:B0 0x42] register
[CH_SPACE_FL:B0 0x4C] register
[CH_SPACE_FH:B0 0x4D] register
[F_DEV_L:B0 0x4E] register
[F_DEV_H:B0 0x4F] register
[2DIV_SEARCH:B0 0x6F] register

[Bank1]

[PLL_CFP_ADJ:B1 0x09] register
[IF_FREQ_H:B1 0x0A] register
[IF_FREQ_L:B1 0x0B] register
[IF_FREQ_CCA_H:B1 0x0C] register
[IF_FREQ_CCA_L:B1 0x0D] register
[BPF_ADJ_H:B1 0x0E] register
[BPF_ADJ_L:B1 0x0F] register
[BPF_CCA_ADJ_H:B1 0x10] register
[BPF_CCA_ADJ_L:B1 0x11] register

[Bank2 registers]

[RATE_ADJ1:B2 0x2A] register (Note: setting is necessary only when changing to 150kbps.)
[RATE_ADJ2:B2 0x2B] register (Note: setting is necessary only when changing to 150kbps.)

●Programming narrow band option setting

By setting NBO_SEL ([DATA_SET:B0 0x47(7)]) = 0b1, narrow bandwidth mode can be selected. The narrow band mode is applying 200 kHz channel spacing instead of 400 kHz defined in IEEE802.15.4g standard. When selecting the narrow bandwidth mode, below registers should be changed to narrow RX bandpass filter bandwidth.

[Bank0]
- [IF_FREQ_AFC_H:B0 0x30] register
- [IF_FREQ_AFC_L:B0 0x31] register
- [BPF_AFC_ADJ_H:B0 0x32] register
- [BPF_AFC_ADJ_L:B0 0x33] register

[Bank1]
- [PLL_CFP_ADJ:B1 0x09] register
- [IF_FREQ_H:B1 0x0A] register
- [IF_FREQ_L:B1 0x0B] register
- [IF_FREQ_CCA_H:B1 0x0C] register
- [IF_FREQ_CCA_L:B1 0x0D] register
- [BPF_ADJ_H:B1 0x0E] register
- [BPF_ADJ_L:B1 0x0F] register
- [BPF_CCA_ADJ_H:B1 0x10] register
- [BPF_CCA_ADJ_L:B1 0x11] register

■RF adjustment

●PA adjustment

ML7306 family has output circuits for 1mW and 20mW (10mW as well). Output circuits can be selected by PA_SEL ([PA_CNTRL:B1 0x07(4)]).

Each output power can be adjusted with 16 resolutions by using [PA_ADJ1:B1 0x04] to [PA_ADJ3:B1 0x06] registers and [PA_REG_ADJ1:B1 0x33] to [PA_REG_ADJ3:B1 0x35] registers. In each register, 20mW circuit is adjusted by upper 4bits and 1mW circuit is adjusted by lower 4bits. 3 setting value can be stored for each output power circuit. Applying setting can be selected by PA_ADJ_SEL[1:0] ([PA_CNTRL:B1 0x07(1-0)]).

When switching output power between 10mW and 20mW, 10mW adjustment setting valueis stored into [PA_ADJ1:B0 0x04] and those for 20mW is stored into [PA_ADJ2:B1 0x05]. After that, output power can be switched by PA_ADJ_SEL[1:0] setting. Maximum 3 settings can be stored for each output circuit.

Note: Output impedance at PA_OUT pin (#27) differs between 1mW output circuit and 20mW output circuit.
Therefore, the most optimized matching circuit will also be different.

Following table shows setting validity corresponfding to PA_SEL and PA_ADJ_SEL[1:0] setting.

PA_SEL (B1 0x07)	PA_ADJ_SEL [1:0] (B1 0x07)	PA adjustment registers						PA regulator adjustment registers		
		PA_ADJ1		PA_ADJ2		PA_ADJ3		PA_REG_ADJ1	PA_REG_ADJ2	PA_REG_ADJ3
		[7:4]	[3:0]	[7:4]	[3:0]	[7:4]	[3:0]	[2:0]	[2:0]	[2:0]
0b0	0b01		valid					valid		
0b0	0b10				valid				valid	
0b0	0b11						valid			valid
0b1	0b01	valid						valid		
0b1	0b10			valid					valid	
0b1	0b11					valid				valid

●I/Q adjustment

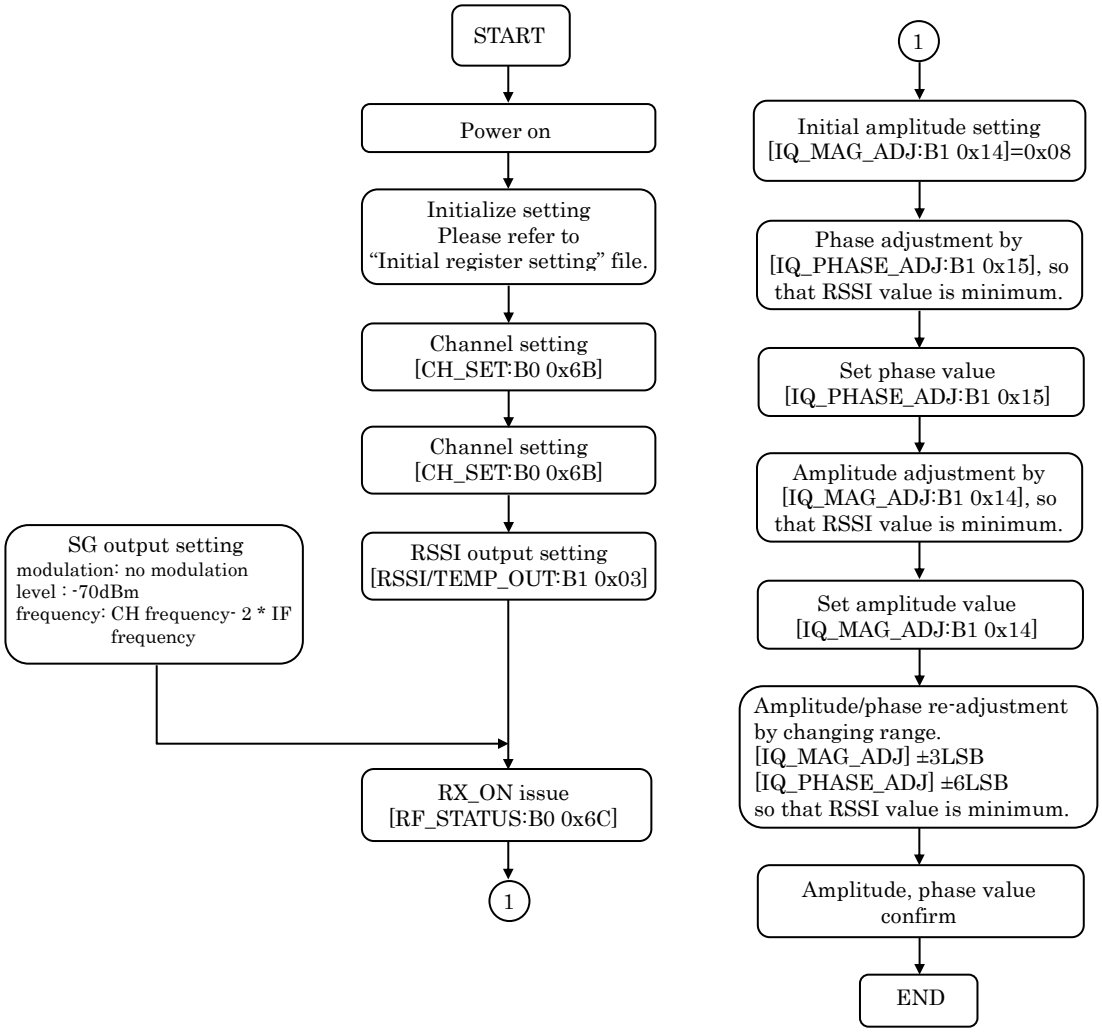
Image rejection ratio can be adjusted by tuning IQ signal balance. The adjustment procedure is as follows:

1. From SG, image frequency signal is input to ANT pin (#30).
   Input signal: no modulation.wave
   Input frequency: channel frequency - (2 * IF frequency)
   In case of 100kbps, IF frequency = 720kHz. please refer to the “Programing IF frequency”.
   Input level: -70dBm

2. By setting RSSI_OUT ([RSSI/TEMP_OUT:B1 0x03(0)]) =0b1, outputing RSSI from A_MON pin (#24).

3. Issuing RX_ON by [RF_STATUS:B0 0x6C] register, by adjusting [IQ_MAG_ADJ:B1 0x14] and [IQ_PHASE_ADJ: B1 0x15] registers, finding setting value so that RSSI value is minimum by measuring A_MON pin (#24).

[I\Q adjustment flow]



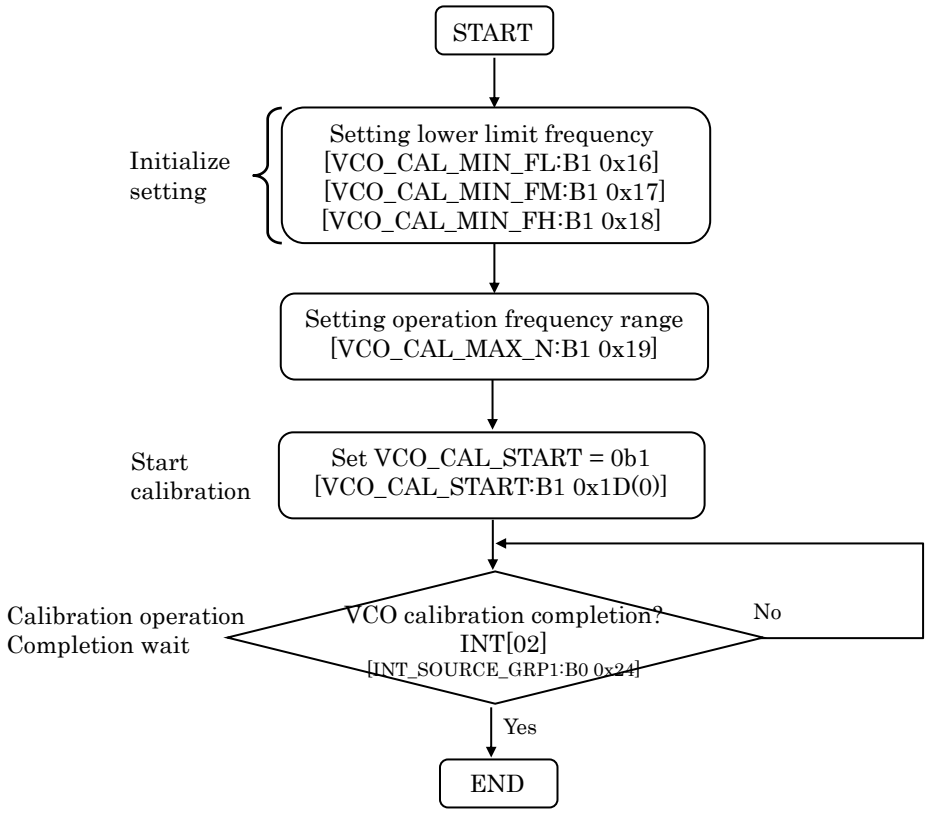
●VCO adjustment

In order to compensate VCO operation margin, optimized capacitance compensation value should be set in each operation frequency. This capacitance compensation value can be acquired by VCO calibration.

By performing VCO calibration when power-up or reset, acquired capacitance compensation values for upper limit and lower limit of operation frequency range (for both TX/RX), based on this value optimised capacitance value is applied during TX/RX operation. Lower limit frequency can be set by [VCO_CAL_MIN_FL:B1 0x16] to [VCO_CAL_MIN_FH:B1 0x18] registers. Upper frequency is definced by [VCO_CAL_MAX_N:B1 0x19] register as frequency range.

[VCO adjustment flow]

The following flow is the procedure for acquiring capacitance compensation value when power-up or reset.



Note: VCO calibration should be performed only during IDLE state.

VCO calibration is necessary every 0.9ms to 4.2ms.
After completion, capacitance compensation values are stored in the following registers.
Capacitance compensation value at lower limit frequency: [VCO_CAL_MIN:B1 0x1A]
Capacitance compensation value at upper limit frequency: [VCO_CAL_MAX:B1 0x1B]

In actual operation, based on the 2 compensation values, the most optimized capacitance value for the frequency is calculated and applied. The calculated value is stored in [VCO_CAL:B1 0x1C] register.

By evaluation stage, if below values are stored in the MCU memory and uses these values upon reset or power-up, calibration operation can be omitted.

Registers to be saved in the MCU memory.
[VCO_CAL_MIN_FL:B1 0x16]
[VCO_CAL_MIN_FM:B1 0x17]
[VCO_CAL_MIN_FH:B1 0x18]
[VCO_CAL_MAX_N:B1 0x19]
[VCO_CAL_MIN:B1 0x1A]
[VCO_CAL_MAX: B1 0x1B]

NOTE:
1. For lower limit frequency, please use frequency at least 2MHz lower than operation frequency
2. For upper limit frequency should be selected so that operation frequency is in the frequency range.
3. Frequency range should not include 36MHz multiplied frequency, i.e. 900MHz, 936MHz.
4. In case of like a channel change, if the setting frequency is outside of calibration frequency range, calibration process has to be performed again with proper frequency.

●VCO lower limit frequency setting

As described in the "Programing Channel #0 Frequency", VCO lower limit frequency can be set by setting F-counter parameter into [VCO_CAL_MIN_FL:B1 0x16], [VCO_CAL_MIN_FM:B1 0x17] and [VCO_CAL_MIN_FH:B1 0x18] registers. N-counter and A-counter parametrs are applied the valu stored in [CH0_NA:B0 0x4B] register.

Lower limit frequency setting value can be calculated using the following formula.

$$LOW\_F = \{F_{LOW} - (4 * N + A) * f_{REF}\} / f_{REF} * 2^{20} \text{ (Integer part)} \quad \text{[note: using 20bit circuit]}$$

Here
- LOW_F : Lower limit frequency F-counter setting
- F_{LOW} : Lower limit frequency [MHz]
- f_{REF} : PLL reference frequency (input clock=36MHz)
- N : N-counter parameter
- A : A-counter parameter

If operation low limit frequency is 923.1MHz, N= 6 and A=1. Setting value should be lower than 2MHz. Then in following example, lower limit frequency is set to 921.1MHz. (f_{REF} = 36MHz)

$$LOW\_F = \{921.1 - (4 * 6 + 1) * 36MHz\} / 36MHz * 2^{20} \text{ (Integer part)} = 614582 \text{ (0x960B6)}$$

Setting values for each register is as follows:
[VCO_CAL_MIN_FL:B1 0x16]= 0xB6
[VCO_CAL_MIN_FM:B1 0x17]= 0x60
[VCO_CAL_MIN_FL:B1 0x18]= 0x09

●VCO upper limit frequency setting

VCO upper limit frequency is calculated as following formula, based on low limit frequency values and VCO_CAL_MAX_N[4:0] ([VCO_CAL_MAX_N: B1 0x19(5-0)]).

VCO calibration upper limit frequency = VCO calibration lower limit frequency (B1 0x16-0x18) + ΔF(B1 0x51)

ΔF is defined in the table below.

VCO_CAL_MAX_N[4:0]	ΔF[MHz]
0b0_0000	1.125
0b0_0001	2.25
0b0_0011	4.5
0b0_0111	9
0b0_1111	18
0b1_1111	36
Other than aboev	Prohibited

●Energy Detection value (ED value) adjustment

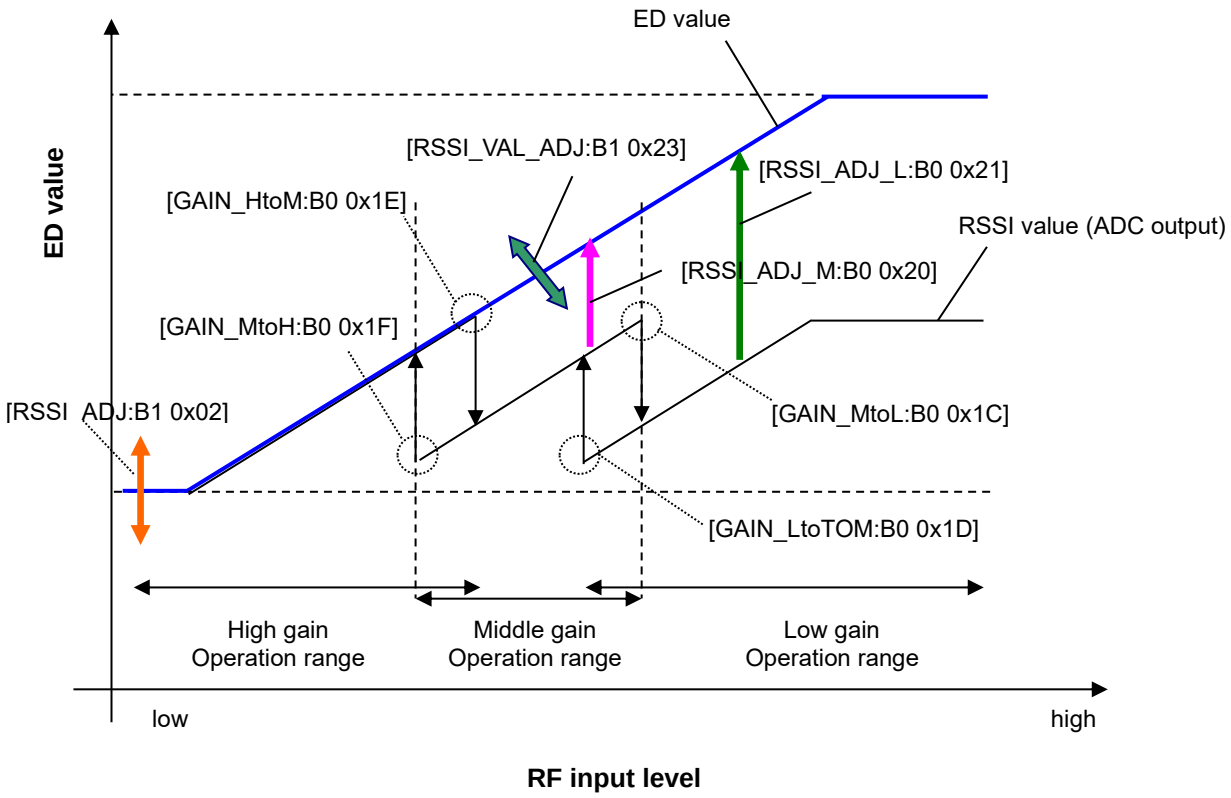
[ED value adjustment]

ED value is calculated by RSSI signal (analog signal) from RF part,. By performing the following adjustment, it is possible to correct the variation in LSIs.

The gain adjustment and related registers are described below.

In order to cover wider input range, gain should be changed at given point. Threshold for gain change points are set by [GAIN_MtoL:B1 0x1C] to [GAIN_MtoH:B0 0x1F]. [RSSI_ADJ_M:B1 0x20] and [RSSI_ADJ_L:B1 0x21] registers are used to addition values to maintain linearity when changing gain. RSSI slope can be set to [RSSI_VAL_ADJ:B1 0x23] register so that ED value can be between 0x00(min) and 0xFF(max). For thse register setting, please use the value specified in the "Initial register setting" file.

Adjusting the input level variation for the same input level can be set to [RSSI_ADJ:B1 0x02] register. It must compensate the slope before compensation defined by [RSSI_VAL_ADJ:B1 0x23] register. However, if positive value is set , ED value cannot be decreased down to 0x00 at low input signal level. If negative value is set, ED value cannot be increased up to 0xFF.



Operation in the High gain range:	RSSI value>GAIN_HtoM, and move to Middle gain.
Operation in the Middle gain range:	RSSI value>GAIN_MtoL, and move to Low gain.
	GAIN_MtoH≥RSSI value, and move to High gain.
Operation in the Low gain range:	GAIN_LtoM≥RSSIvalue, and move to Middle gain.

■Other Setting

●BER measurement setting

The following registers setting are necessary for RX side when measuring BER.

[PLL_MON/DIO_SEL:B0 0x69] = 0x01
[DEMOD_SET:B1 0x01] = 0x80
[DEMOD_SET2:B2 0x0A] = 0x10
[SYNC_MODE:B2 0x12] = 0x00

■Flow Charts

●Initialization

In initialization status, interrupt process, registers setting, VCO calibration are necessary.

(1) Interrupt process

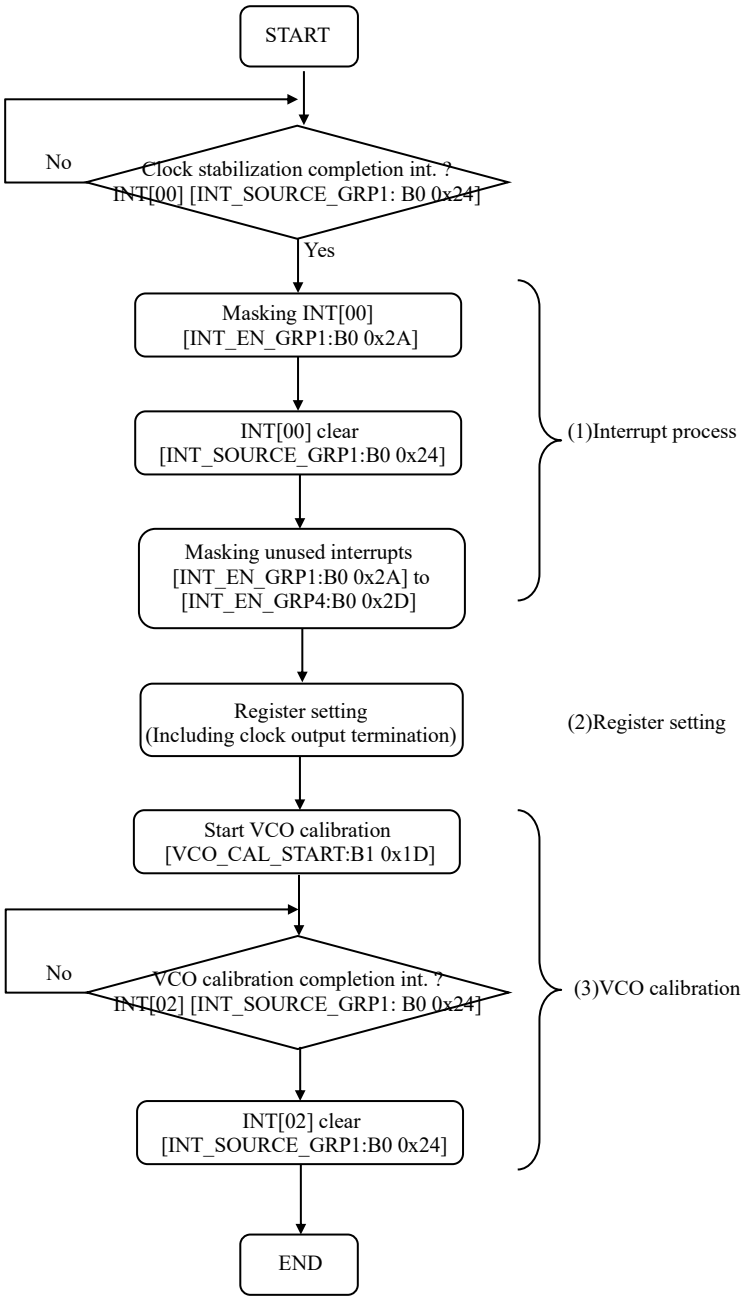
Upon reset, all interrupt notification settings ([INT_EN_GRP1-4:B0 0x2A-0x2D]) are enabled.
After hard reset is released, INT[00] (group 1: Clock stabilization completion interrupt) will be detected. After INT[00] notification, please mask unused interruput elements by using [INT_EN_GRP1:B0 0x2A] to [INT_EN_GRP4] registers.
If interrupt elements are stored internnaly, interrupt will generate as soon as interrupt is unmasked, unless clearing the interrpt. When clearing interrupt, it is recommended to clear interrput after masking the interrupt.

(2) Registers setting

In reset value setting, clock is output from DMON pin (#17). If clock output is not used, please assign another monitoring function to DMON pin and terminate clock output.
After hard reset is released, all registers are accesible except for FIFO access registers and BANK1 registers before INT[00] notification.

(3) VCO calibration

Executing VCO calibration after setting upper and lower limit of the operation frequency range. Operating frequency should be in the calibration frequency range. In case of using frequency which is outside of calibration frequency range, calibration process has to be performed again with proper frequency.
During VCO calibration, please register access is prohibited.


START
No
Clock stabilization completion int. ?
INT[00] [INT_SOURCE_GRP1: B0 0x24]
Yes
Masking INT[00]
[INT_EN_GRP1:B0 0x2A]
INT[00] clear
[INT_SOURCE_GRP1:B0 0x24]
Masking unused interrupts
[INT_EN_GRP1:B0 0x2A] to
[INT_EN_GRP4:B0 0x2D]
(1)Interrupt process
Register setting
(Including clock output termination)
(2)Register setting
Start VCO calibration
[VCO_CAL_START:B1 0x1D]
No
VCO calibration completion int. ?
INT[02] [INT_SOURCE_GRP1: B0 0x24]
INT[02] clear
[INT_SOURCE_GRP1:B0 0x24]
(3)VCO calibration
END

●TX mode (DIO mode)

DIO (TX) mode can be selected by setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b1. In DIO (TX) mode, when issuing TX_ON command, data input to DIO pin (#15) will be transmitted to the air. TX Data following SFD field should be input from host MCU and TX data should be synchronized with DCLK from DCLK pin (#16). After TX completion, TRX_OFF commnand should be issued.

TX data request accept completion interrupt (INT[22] or INT[23] group3) notification should be required to start DIO (TX) transmission. Before issuing TX_ON command, writing dummy data to a FIFO to generate TX data request accept completion interrupt. More than 4byte dummy data (excluding Lngth field) is required.

[Example: Setting minimum dummy packet]

Set CRC_DONE ([FEC/CRC_SEC:B0 0x46(0)]) =0b0, and write 0x00-01-02 (3byte) tp [WR_TX_FIFO:B0 0x7E] register.

Note: The first TX data input during DIO (TX) mode.

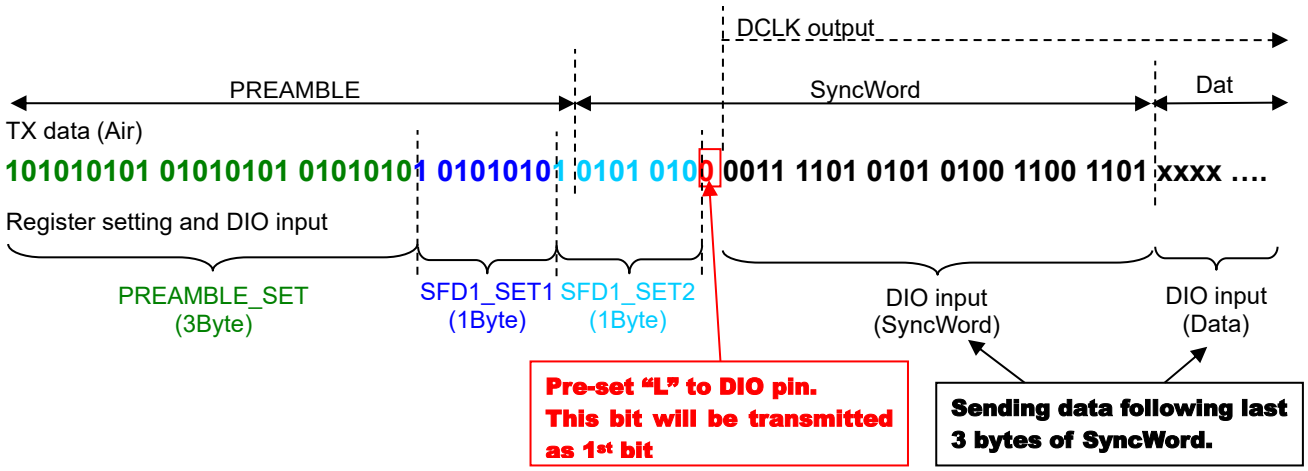
Initial status of DCLK pin (#16) is “L”. Therefore there is no falling edge for the 1st TX data, the 1st TX data should be pre-set to DIO pin (#15) before writing dummy packet.

For more details, please refer to the explanation in following page.

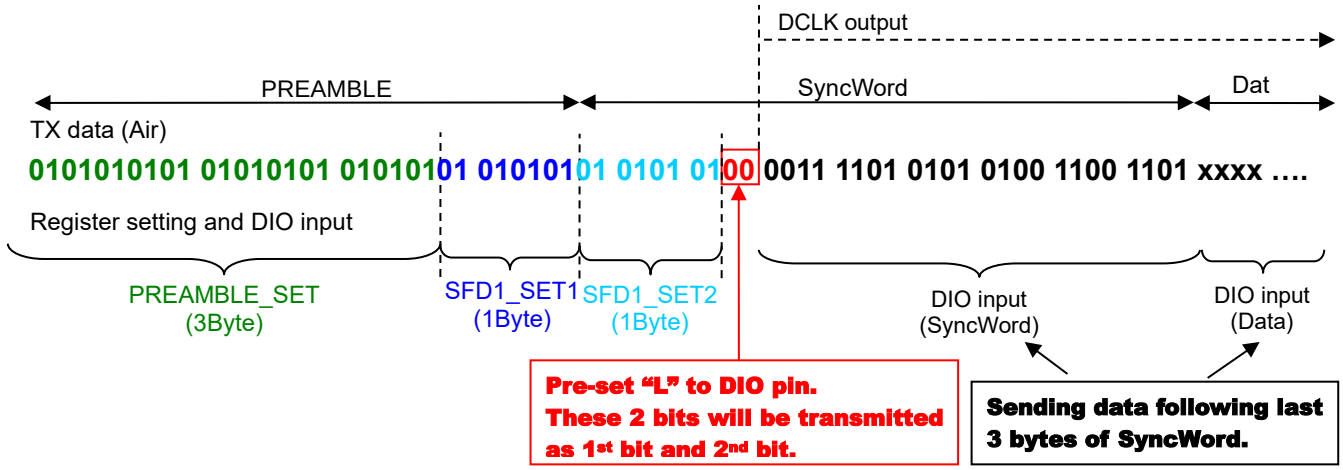
TX data corresponding to each register setting and DIO input is as below:

[Example] Transmitting prEN 13757-4rev Mode C format A packet (ML7396E)

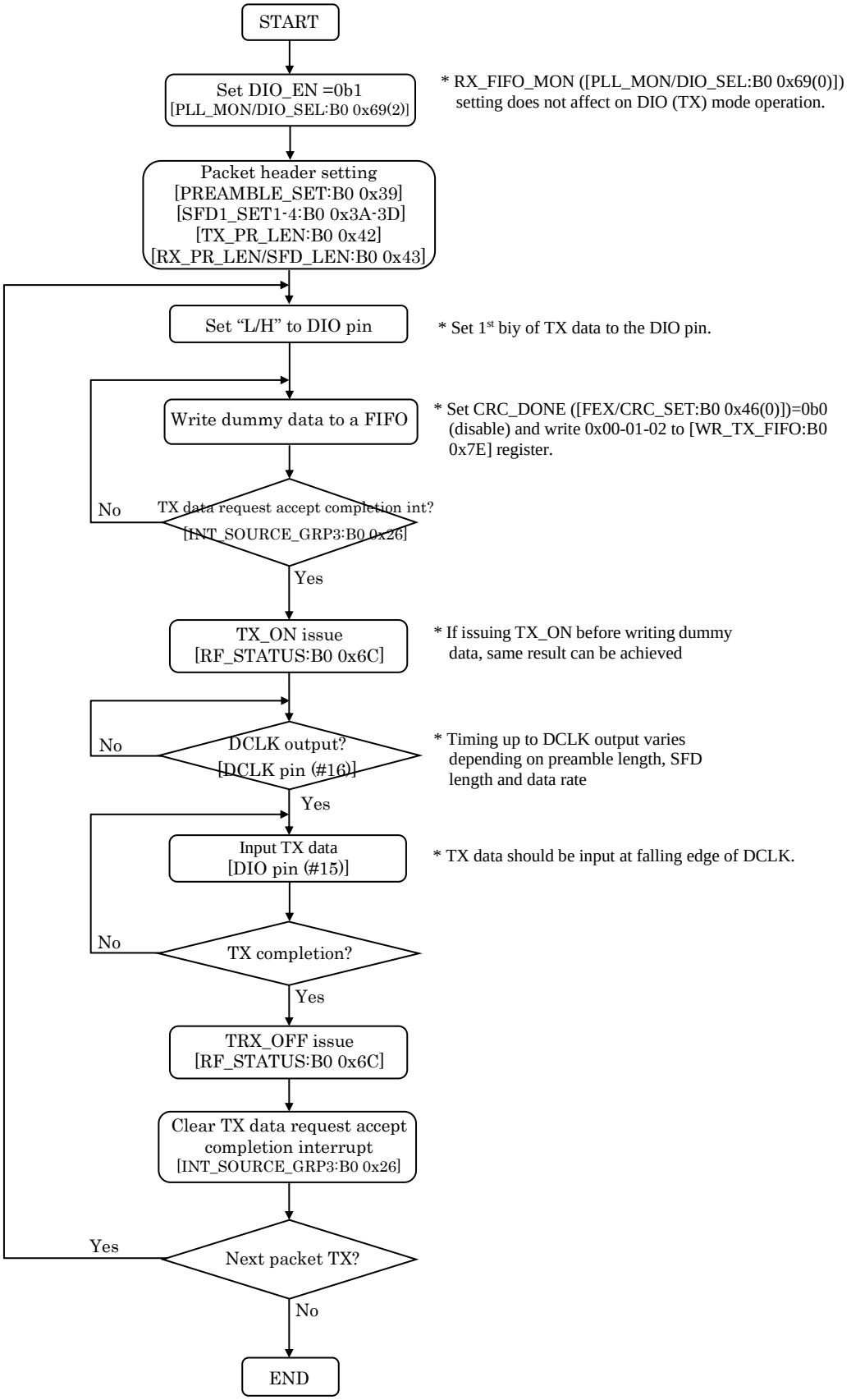
Case 1: Input TX data at rising edge of DCLK
[Conditions]
[PREAMBLE_SET:B0 0x39] =0x55
[SFD1_SET1:B0 0x3A] =0x55
[SFD1_SET2:B0 0x3B] =0x55
[TX_PB_LEN:B0 0x42] =0x03
[RX_PR_LEN/SFD_LEN:B0 0x43] =0x02



Case 2: Input TX data at falling edge of DCLK
[Conditions]
[PREAMBLE_SET:B0 0x39]=0xAA
[SFD1_SET1:B0 0x3A] =0xAA
[SFD1_SET2:B0 0x3B] =0xAA
[TX_PB_LEN:B0 0x42] =0x03
[RX_PR_LEN/SFD_LEN:B0 0x42] =0x02



[Flowchart]

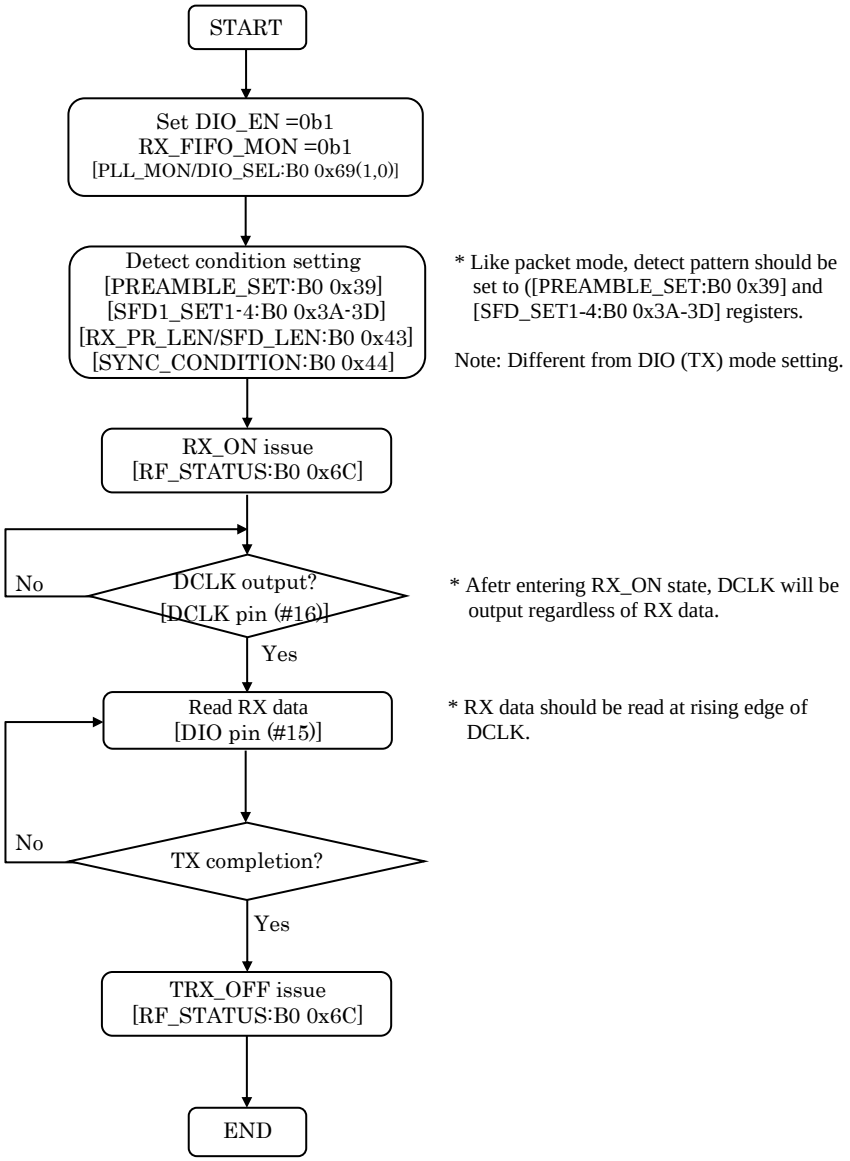

START
Set DIO_EN =0b1
[PLL_MON/DIO_SEL:B0 0x69(2)]
* RX_FIFO_MON ([PLL_MON/DIO_SEL:B0 0x69(0)]) setting does not affect on DIO (TX) mode operation.
Packet header setting
[PREAMBLE_SET:B0 0x39]
[SFD1_SET1-4:B0 0x3A-3D]
[TX_PR_LEN:B0 0x42]
[RX_PR_LEN/SFD_LEN:B0 0x43]
Set "L/H" to DIO pin
* Set 1st biy of TX data to the DIO pin.
Write dummy data to a FIFO
* Set CRC_DONE ([FEX/CRC_SET:B0 0x46(0)])=0b0 (disable) and write 0x00-01-02 to [WR_TX_FIFO:B0 0x7E] register.
No
TX data request accept completion int?
[INT_SOURCE_GRP3:B0 0x26]
Yes
TX_ON issue
[RF_STATUS:B0 0x6C]
* If issuing TX_ON before writing dummy data, same result can be achieved
No
DCLK output?
[DCLK pin (#16)]
* Timing up to DCLK output varies depending on preamble length, SFD length and data rate
Yes
Input TX data
[DIO pin (#15)]
* TX data should be input at falling edge of DCLK.
No
TX completion?
Yes
TRX_OFF issue
[RF_STATUS:B0 0x6C]
Clear TX data request accept completion interrupt
[INT_SOURCE_GRP3:B0 0x26]
Yes
Next packet TX?
No
END

●RX mode (DIO mode)

DIO (RX) mode can be selected by setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b1 and RX_FIFO_MON ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b1. In DIO (RX) mode, when issuing RX_ON command, preamble and SFD detection will be started. After preamble and SFD are detected, RX data is output through DIO pin (#15). RX Data following SFD field are output and RX data should be read at rising edge of DCLK from DCLK pin (#16). After RX completion, TRX_OFF commnand should be issued.

Like packet mode, preamble and SFD detection are done according to the settings of [PREAMBLE_SET:B0 0x39], [SFD1_SET1:B0 0x3A] to [SFD1_SET4:B0 0x3D], [RX_PR_LEN/SFD_LEN:B0 0x43] and [SYNC_CONDITION:B0 0x44] registers.After SFD is deteceted, SFD detection interrupt (INT[11] group2) will generate.

The first RX data is output at the first rising edge of DCLK after SFD detection interrupt notification.(Timing from SFD detection interrupt to the first DCLK rising edge is 9µs at 100kbps setting.)

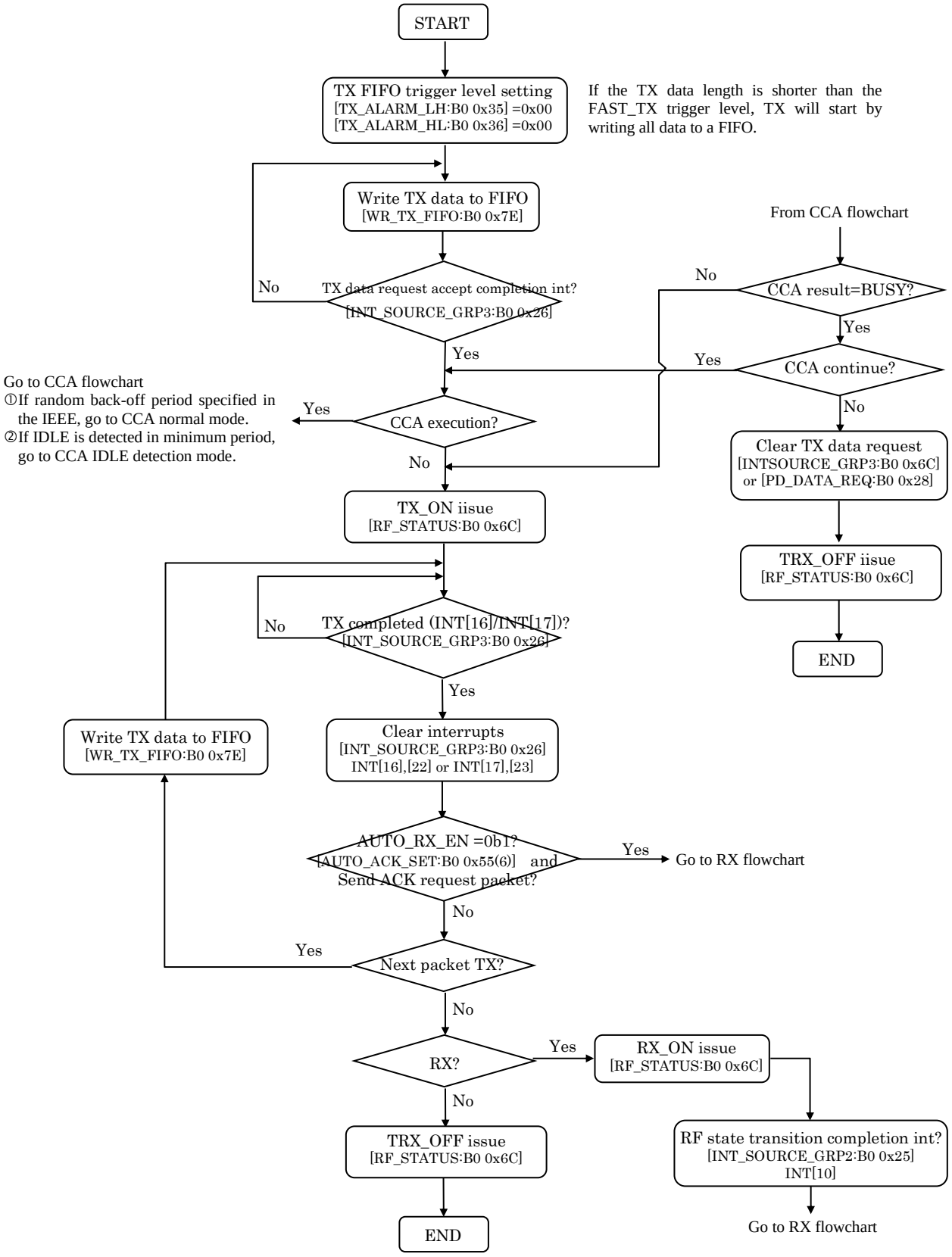


●TX mode (Packet mode, packet length ≤ 256byte)

Packet mode can be selected by setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b0. In Packet mode, each TX data is written into a FIFO by [WR_TX_FIFO:B0 0x7E] register. After writing full TX data of a packet, issuing TX_ON command. Following PB (preamble), SFD data, TX data is transmitted to the air. When CRC is enabled, the CRC calcuration will be done automatically and CRC result is set to FCS field and transmitted to the air.

After TX completion interrupt (INT[16]/[17] group3) occurs, the interrupt must be cleared. If the next TX packet is sent, the next TX packet data is written to a FIFO. If RX is expected after TX, RX_ON should be issued by [RF_STATUS:B0 0x6E] register. TX can be terminated by issuing TRX_OFF by [RF_STATUS:B0 0x6E] register.

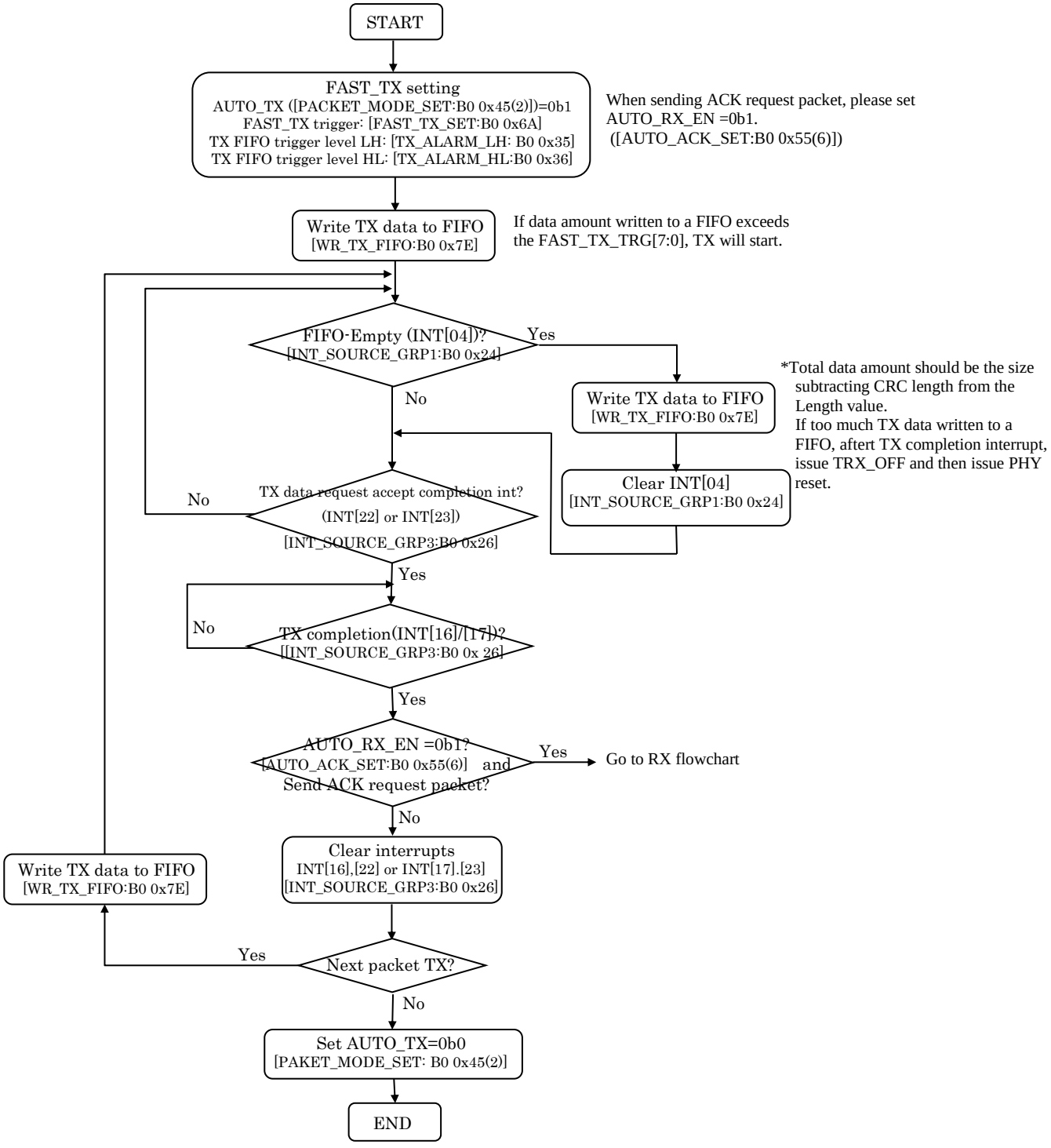
At every packet writing, FIFO0 and FIFO1 are switched automatically. (FIFO0 → FIFO1 → FIFO0)


START
TX FIFO trigger level setting
[TX_ALARM_LH:B0 0x35] =0x00
[TX_ALARM_HL:B0 0x36] =0x00
If the TX data length is shorter than the FAST_TX trigger level, TX will start by writing all data to a FIFO.
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
From CCA flowchart
No
TX data request accept completion int?
[INT_SOURCE_GRP3:B0 0x26]
No
CCA result=BUSY?
Yes
Yes
CCA continue?
Yes
Go to CCA flowchart
①If random back-off period specified in the IEEE, go to CCA normal mode.
②If IDLE is detected in minimum period, go to CCA IDLE detection mode.
Yes
CCA execution?
No
Clear TX data request
[INTSOURCE_GRP3:B0 0x6C]
or [PD_DATA_REQ:B0 0x28]
No
TX_ON iisue
[RF_STATUS:B0 0x6C]
TRX_OFF iisue
[RF_STATUS:B0 0x6C]
No
TX completed (INT[16]/INT[17])?
[INT_SOURCE_GRP3:B0 0x26]
END
Yes
Write TX data to FIFO
[WR_TX_FIFO:B0 0x7E]
Clear interrupts
[INT_SOURCE_GRP3:B0 0x26]
INT[16],[22] or INT[17],[23]
AUTO_RX_EN =0b1?
[AUTO_ACK_SET:B0 0x55(6)] and
Send ACK request packet?
Yes
Go to RX flowchart
No
Yes
Next packet TX?
No
RX?
Yes
RX_ON issue
[RF_STATUS:B0 0x6C]
No
TRX_OFF issue
[RF_STATUS:B0 0x6C]
RF state transition completion int?
[INT_SOURCE_GRP2:B0 0x25]
INT[10]
END
Go to RX flowchart

●TX mode (Packet mode, packet length ≥ 257byte)

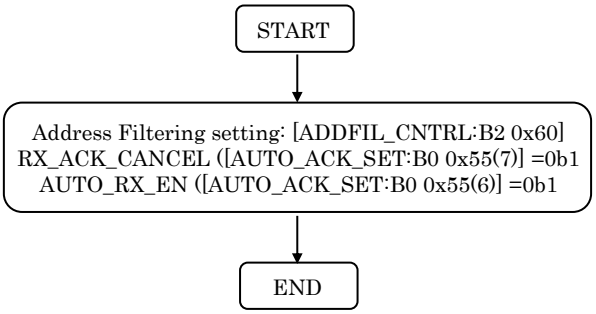
The host MCU should write TX data to a FIFO while checking FIFO-Full interrupt (INT[05] group1) and FIFO-Empty interrupt (INT[04] group1) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operation are same as packet mode (less than 256byte).

Enabling FAST_TX mode by setting AUTO_TX ([PACKET_MODE_SET:B0 0x45(2)] =0b1 and FAST_TX_TRG[7:0] ([FAST_TX_SET:B0 0x6A(7-0)], TX will start when data amount written to a FIFO exceeds the setting value of FAST_TX_TRG[7:0].



●TX mode (Ack receiving with address filter)

Even when Address Filtering function is enabled, Ack packet (or beacon packet) will be received. However dscarding Ack packet can be set by RX_ACK_CANCEL ([AUTO_ACK_SET:B0 0x55(7)]) =0b1.
And when AUTO_RX_EN ([AUTO_ACK_SET:B0 0x55(6)])=0b1, the Ack packet just after transmitting ACK request packet can be received without discarding.



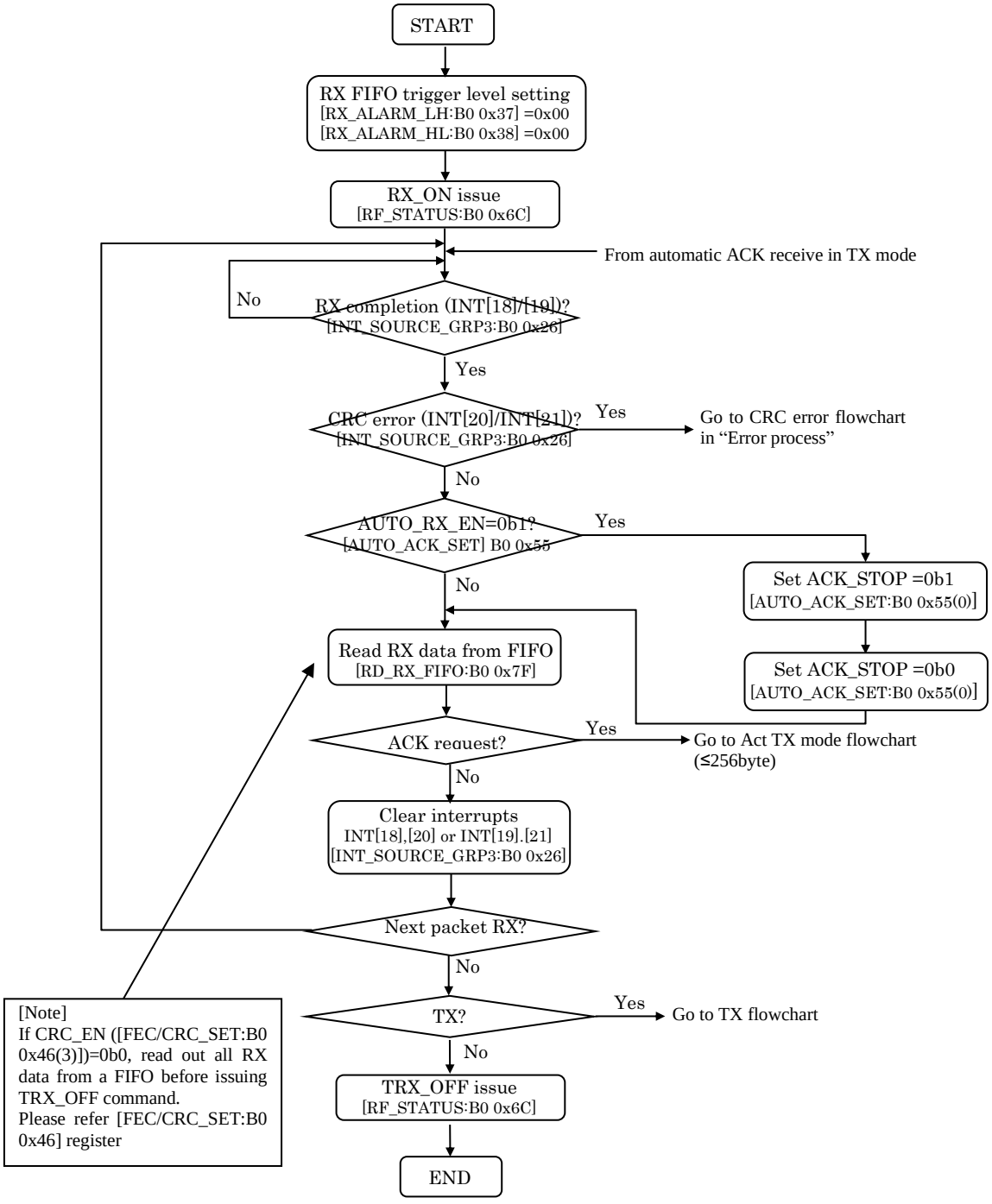
Note: Ack packet is detected by frame type only. Therefore even if the first Ack packet destination is different address, this Ack packet will be received. The following process is as below;

① Address match
Following 2nd packet will be discarded.
② Address mismatch
By setting RX_ACK_CANCEL=0b0, maintain RX until receiving Ack packet with right address.

●RX mode (Packet mode, packet length ≤ 256 bytes)

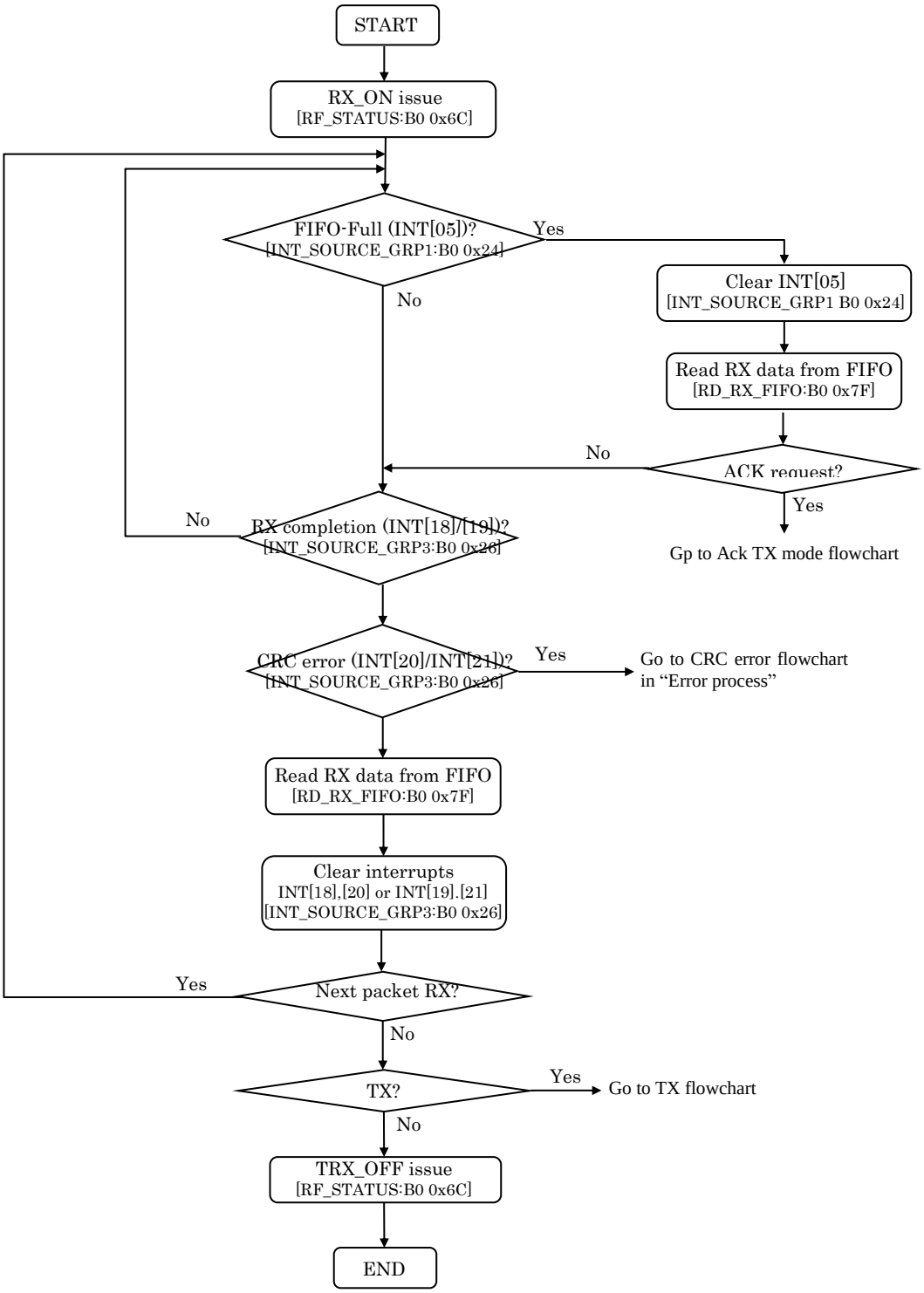
Packet mode can be selected setting DIO_EN ([PLL_MON/DIO_SEL:B0 0x69(1)]) =0b0. In DIO mode, when issuing RX_ON command, preamble and SFD detection will be started. After preamble and SFD are detected, RX data will be stored into a FIFO. After RX completion interrupt (INT[18]/[19] group3) occurs, the host MCU will read RX data from [RD_RX_FIFO:B0 0x7F] register. If CRC error interrupt (INT[20]/[21]) is generated, FIFO data has to be cleared by setting (FIFO_CLR1/0 ([INT_SOURCE_GRP1:B0 0x26(7/6)]) =0b0. After clearing RX retaive interrpts, if receiving the next packet, maintain RX_ON status and waiting for next RX completion interrupt. If TX is expected after RX, TX_ON should be issued by [RF_STATUS:B0 0x6E] register. If terminating RX, issuing TRX_OFF by [RF_STATUS:B0 0x6E] register.

If FIFO-Full trigger and FIFO-Empty trigger are not used, please set 0x00 to both [RX_ALARM_LH:B0 0x37]) and [RX_ALARM_HL:B0 0x38)] registers.



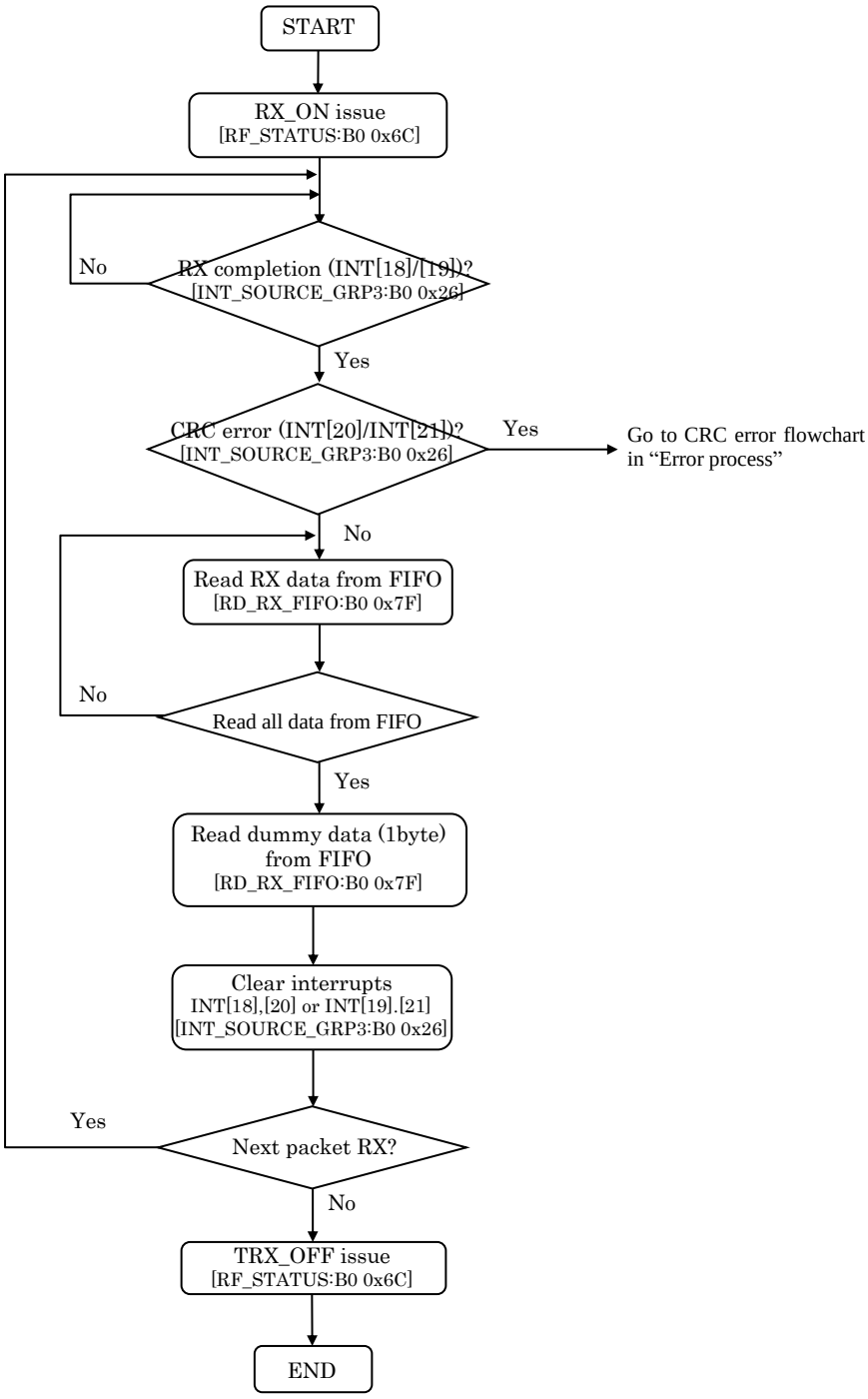
●RX mode (Packet mode, packet length ≥ 257 bytes)

The host MCU should read RX data from a FIFO while checking FIFO-Full interrupt (INT[05] group1) and FIFO-Empty interrupt (INT[04] group1) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operation are same as packet mode (less than 256byte).



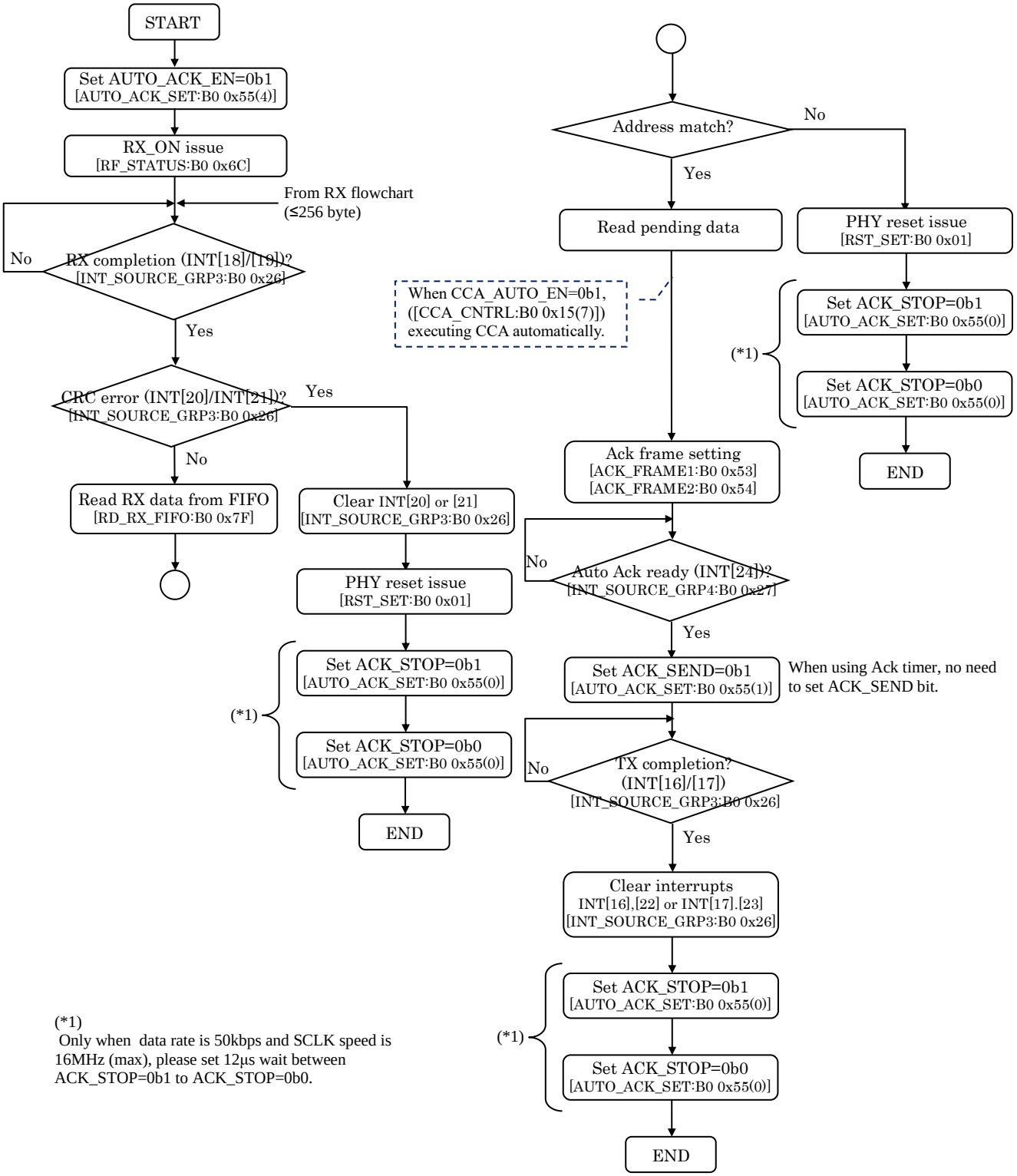
●RX mode (IEEE802.15.4d mode)

When using IEEE80.15.4d mode by IEEE_MODE ([PACKET_MODE_SET:B0 0x45(1)]) =0b0, Basic flowchart is same as IEEE 802.15.4g. However reading 1byte dummy data should be required after reading amount of data given by Length field.



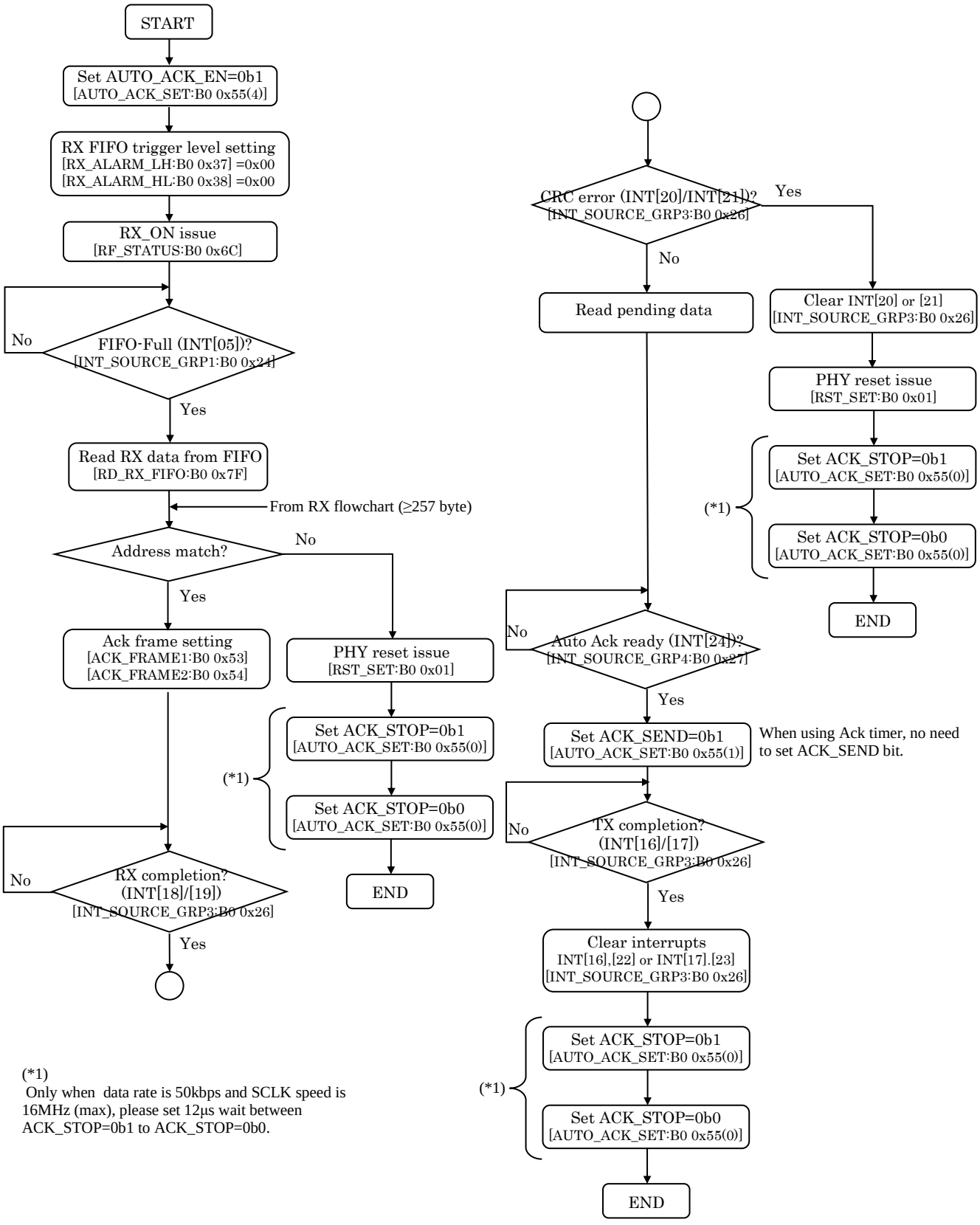
●ACK TX mode (AUTO_ACK, packet length ≤ 256 bytes)

When AUTO_ACK function is enabled by AUTO_ACK_EN ([AUTO_ACK_SET:B0 0x55(4)]) =0b1, if receiving TX packet with ACK request, preparing TX Ack packet (TX_ON) or transmitting Ack packet automatically (when using Ack timer).



(*1)
Only when data rate is 50kbps and SCLK speed is 16MHz (max), please set 12µs wait between ACK_STOP=0b1 to ACK_STOP=0b0.

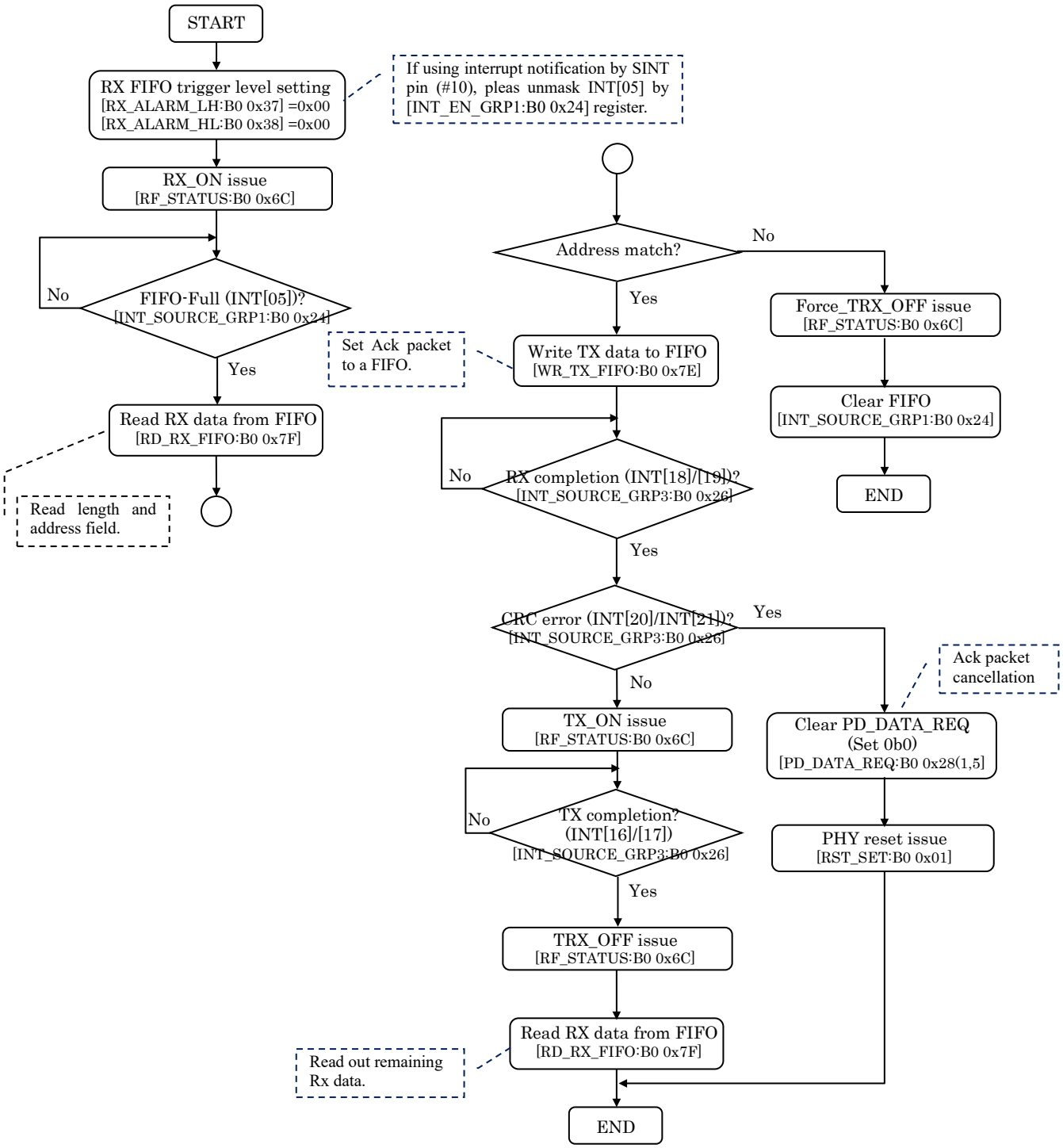
●ACK TX mode (AUTO_ACK, packet length ≥ 257 bytes)



(*1)
Only when data rate is 50kbps and SCLK speed is 16MHz (max), please set 12μs wait between ACK_STOP=0b1 to ACK_STOP=0b0.

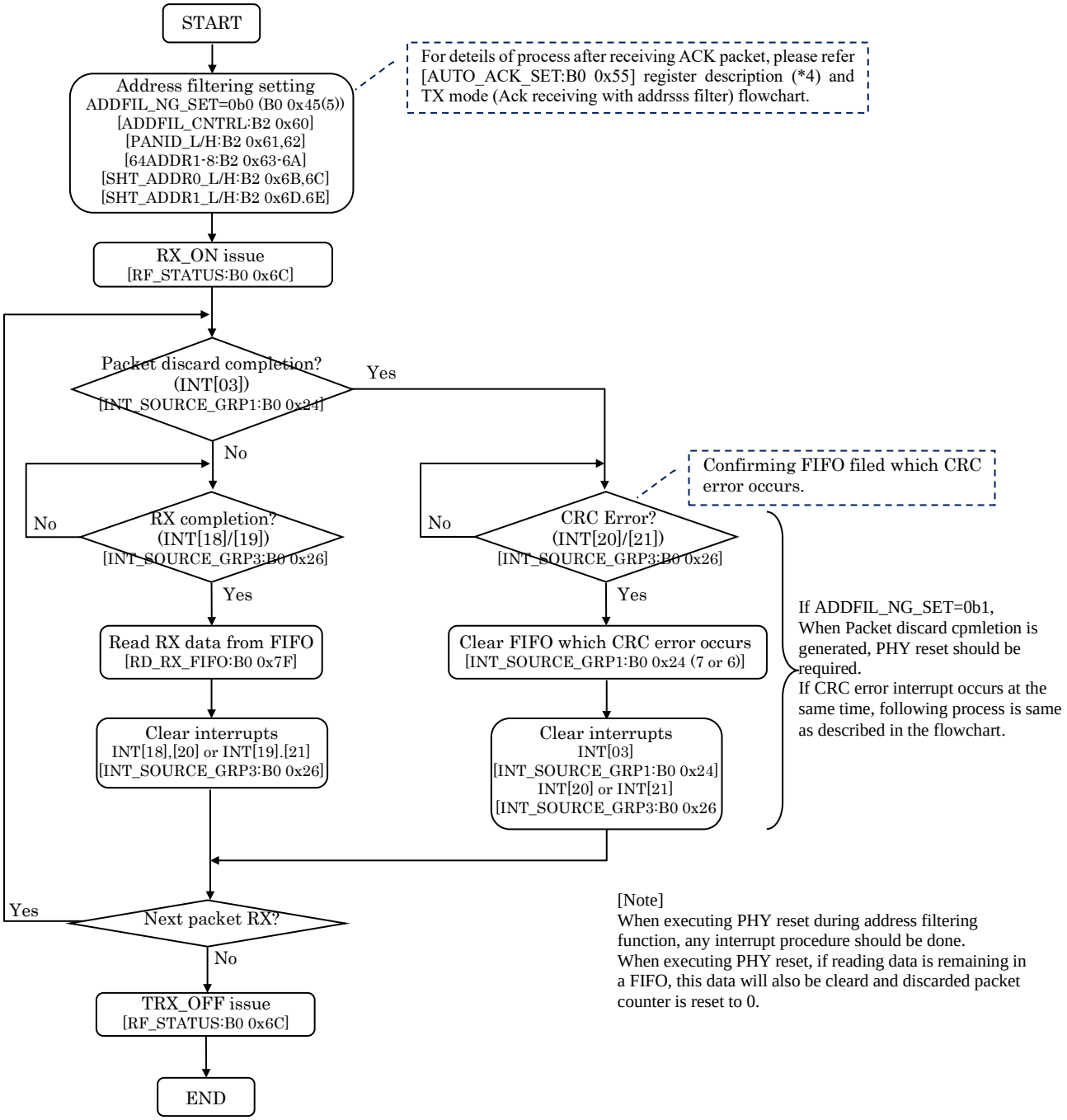
●ACK TX mode (without AUTO_ACK)

Below flowchart shows the Ack packet transmission without AUTO_AUK function. By using FIFO-Full interrupt (INT[05] gtoup1), the host MCU write Ack packet to a FIFO during RX. After RX completion, transmitting Ack paket.



●Address Filter

When Address filtering function is enabled, if receiving packet which address field are mismatch, Packet discard completion interrupt (INT[03] group1) will be generated. At this time, if ADDFIL_NG_SET ([PACKET_MODE_SET:B0 0x45(5)]) =0b0, aborting packet data immediately after address mismatch detection and CRC error interrupt (INT[20]/[21] group3) is also generated at the same time. (The details of interrupt notifiaction, please refer to the [Interrupts timing when using INT_TIM_CTRL] in "Address filtering function".) After notifying Packet discard completion interrupt and CRC error interrupt, it is need to clear FIFO by [INT_SOURCE_GRP1:B0 0x24] register or reading out data specified by Lngth field from the FIFO, in order to store next packet to right FIFO. After that, clearing Packet discard completion interrupt and CRC error interrupt, and then waiting next packet.

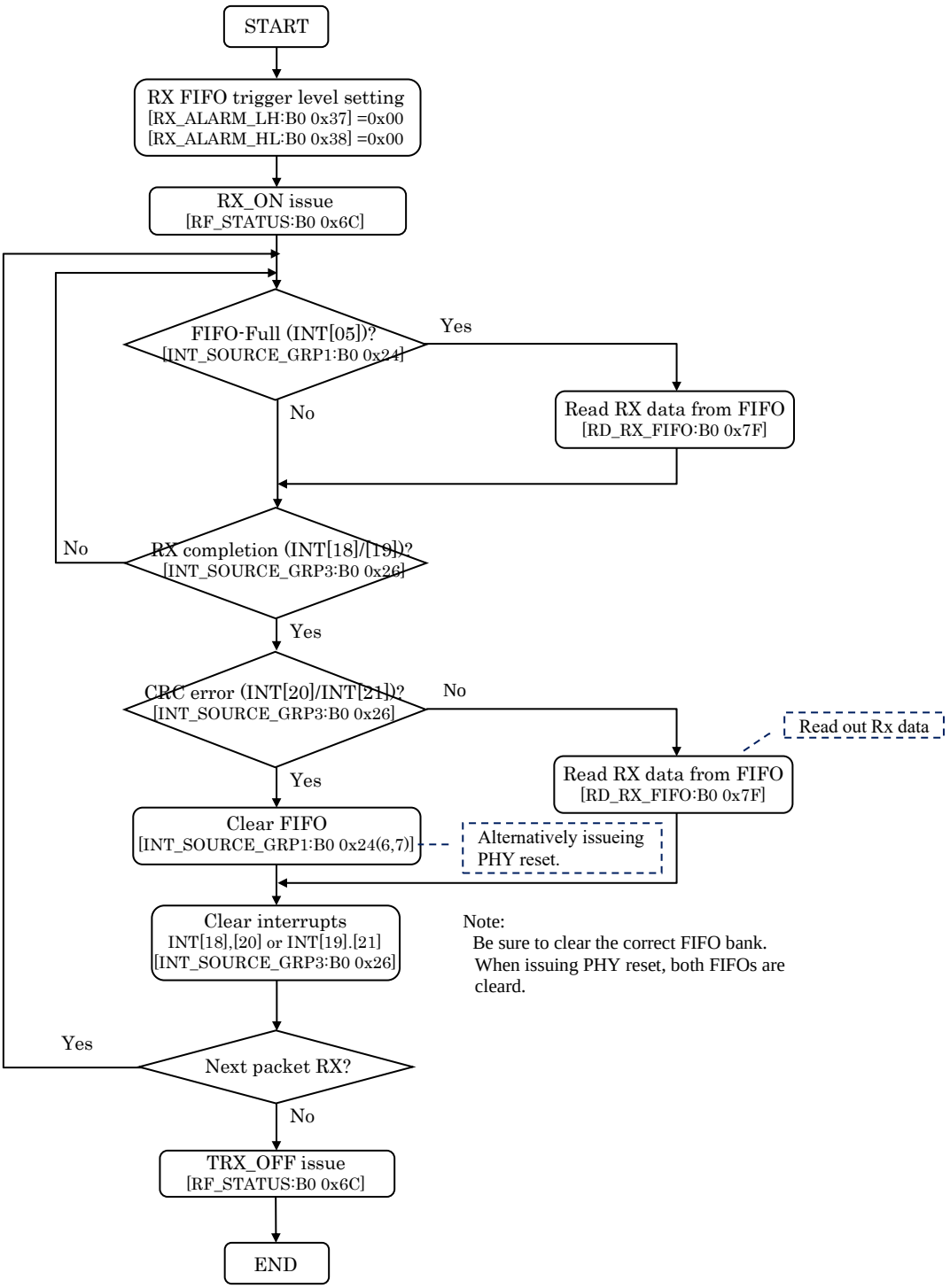


[Note]
When executing PHY reset during address filtering function, any interrupt procedure should be done.
When executing PHY reset, if reading data is remaining in a FIFO, this data will also be cleard and discarded packet counter is reset to 0.

●FIFO Clear (Rx)

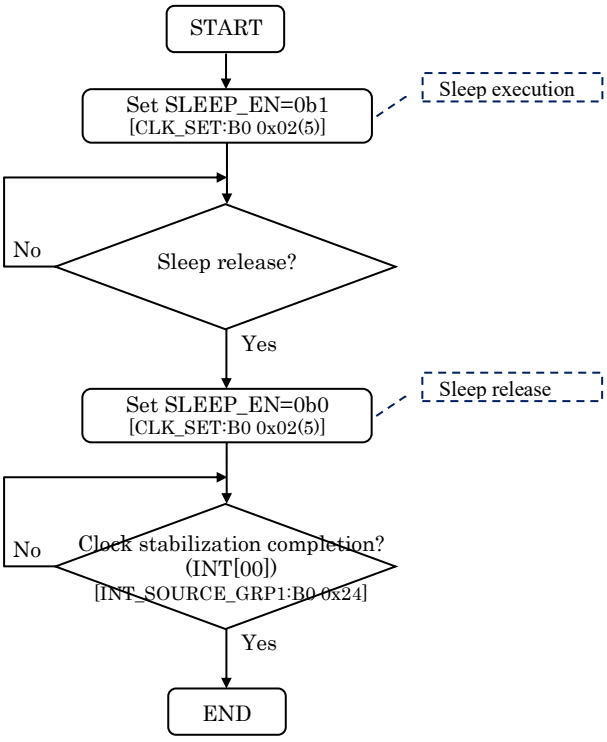
When RX completion interrupt (INT[18]/[19] group3) and CRC error interrupt (INT[20]/[21] group 3) is notified in the same time, clearing FIFO by set 0b0 to FIFO_CLR0/1 ([INT_SOURCE_GRP1:B0 0x24(6/7)]) if no need to read remaining RX data. And then clearing RX completion interript and CRC error interrupt.

If receiving next packet, keeping RX_ON state. If terminating RX_ON state, please issueing TRX_OFF command by [RF_STATUS:B0 0x6C] register. Be sure to clear the correct FIFO bank only. Alternatively, FIFO can be cleared by issueing PHY reset by using [RST_SET:B0 0x01] register.



●SLEEP

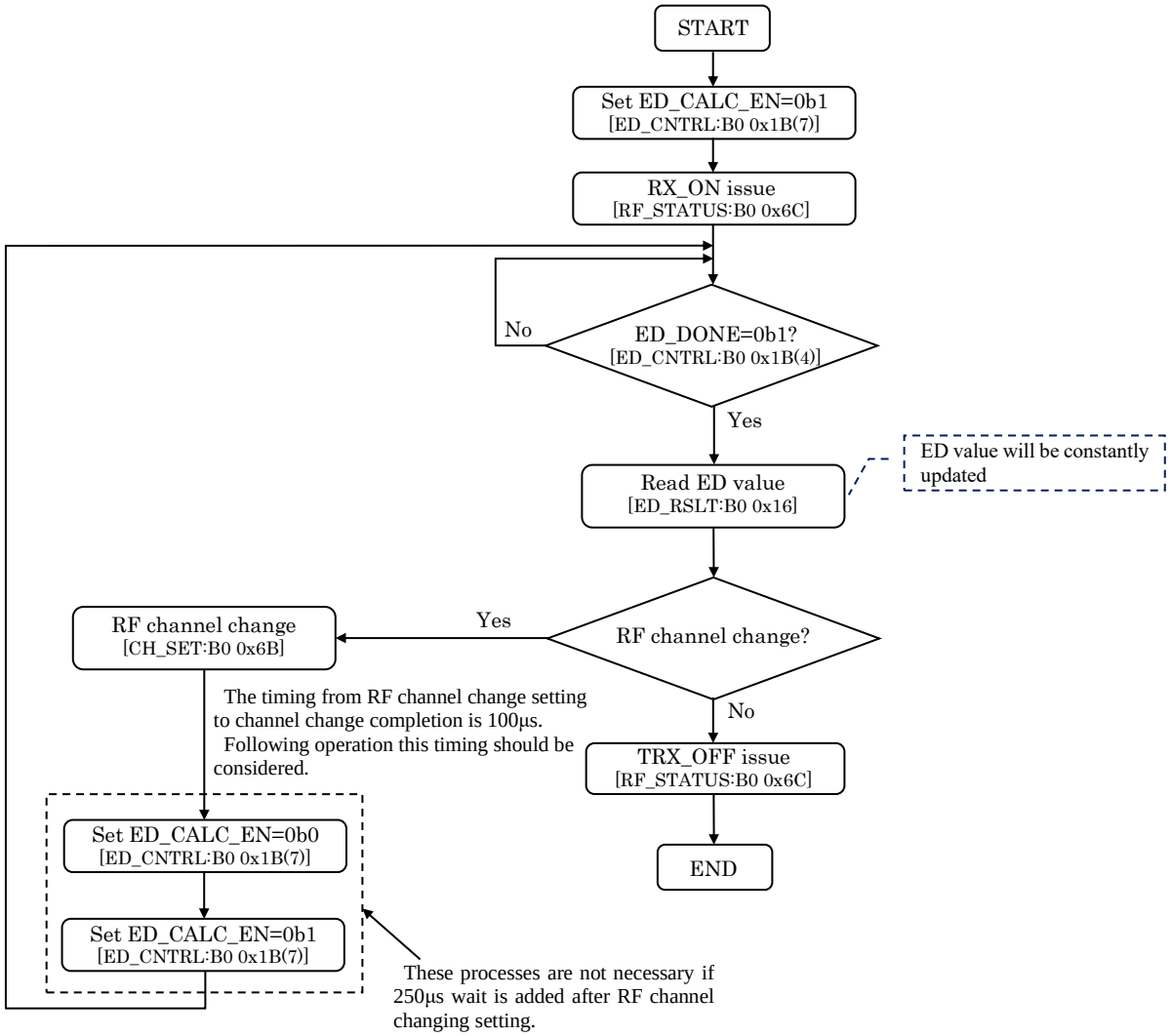
Set 0b1 to SLEEP_EN ([CLK_SET:B0 0x02(5)]) in order to enter into SLEEP state. SLEEP state can be released by setting SLEEP_EN=0b0.



●ED Scan

ED value will be automatically acquired by issuing RX_ON by [RF_STATUS:B0 0x6C] register after setting ED_CALC_EN [ED_CNTRL:B0 0x1B(7)]) =0b1. ED values is constantly updated when ED_CALC_EN=0b1 during RX_ON state.

When changing RF channel, once set ED_CALC_EN=0b0 and set 0b1 again after RF channel change completion. Except for RF channel change, please do not set 0b0 to ED_CALC_EN bit.



●CCA operation

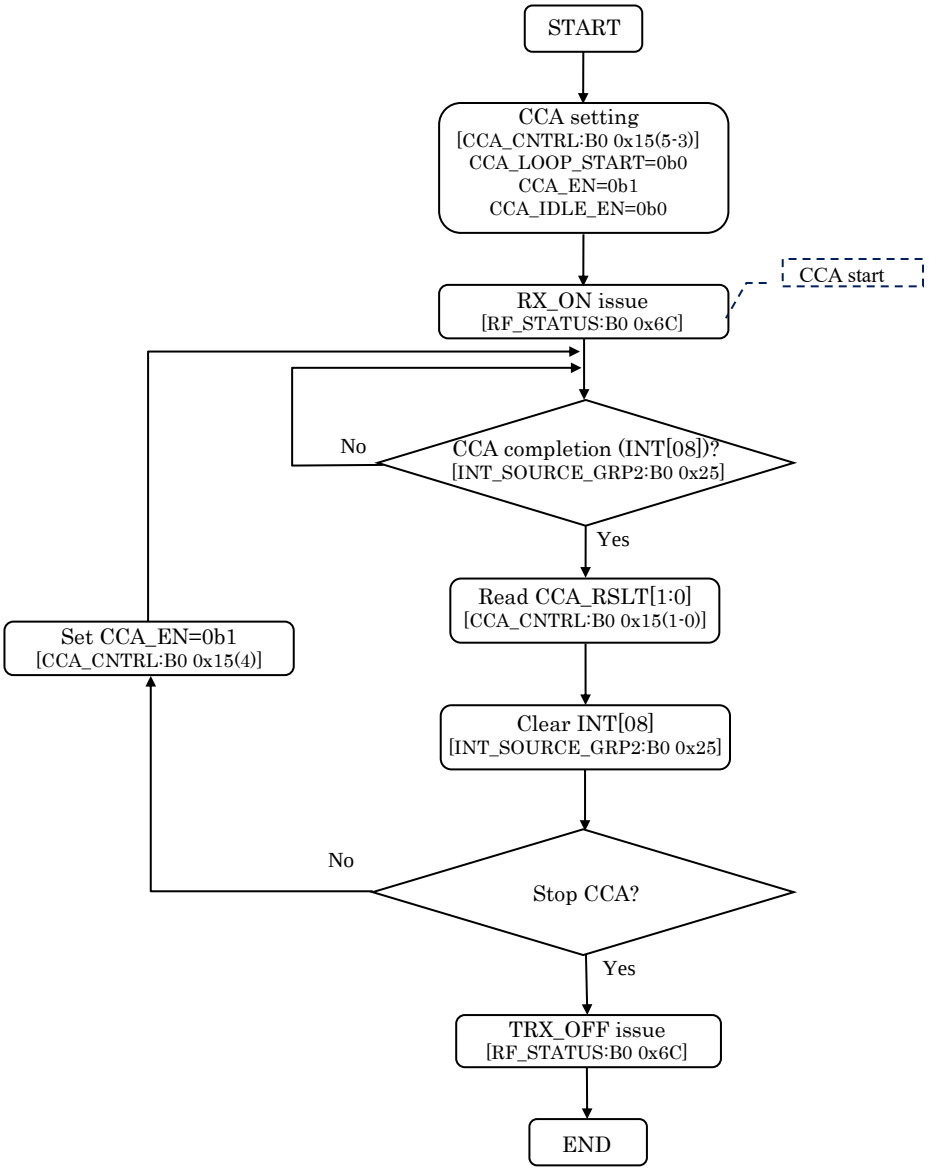
●Normal mode

CCA normal mode will be executed by issueing RX_ON by [RF_STATUS:B0 0x6C] register after setting CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0. Compariing acquired ED average value with CCA threshold value in [CCA_LEVEL:B0 0x13] register and notice the result. After CCA execution, CCA_EN is turned disabled, and RF maintains RX_ON state.

Even if set CCA_EN=0b1 during RX_ON state, CCA can be performed by. However, in this case, 16µs - 32µs (2 cycle of A/D conversion) WAIT is automatically added as the filter stabilization period before CCA execution. (If CCA_EN=0b1 is set before issuing RX_ON, WAIT is not added because filter stabilization period is included in RF transition period.)

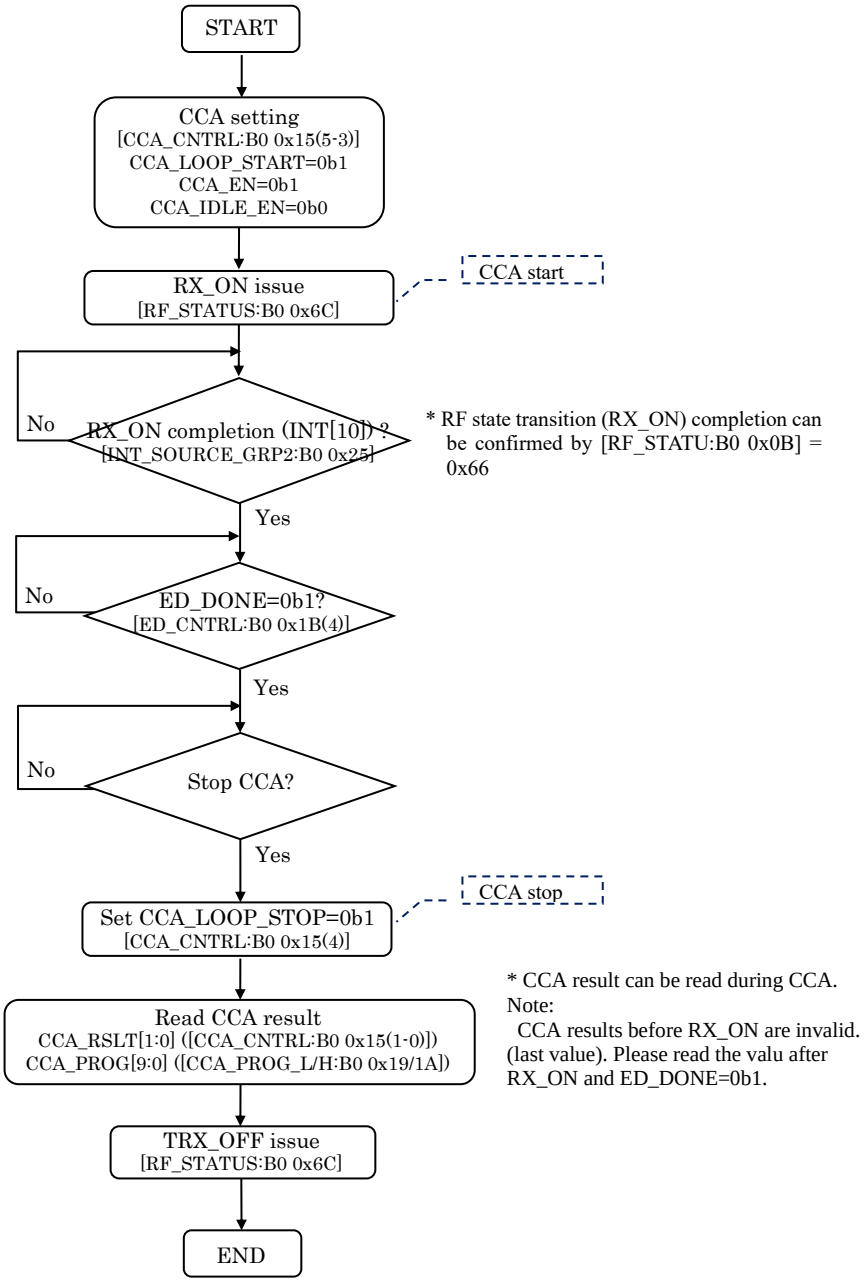
If bit synchronization is detected during CCA, keep receiving with wider BPF bandwidth for CCA operation. If CCA is executed after bit synchronization detection, CCA is executed with normal BPF bandwidth.

CCA execution is also possible during diversity search. In this case, after CCA completion diversity search will be resumed automatically.



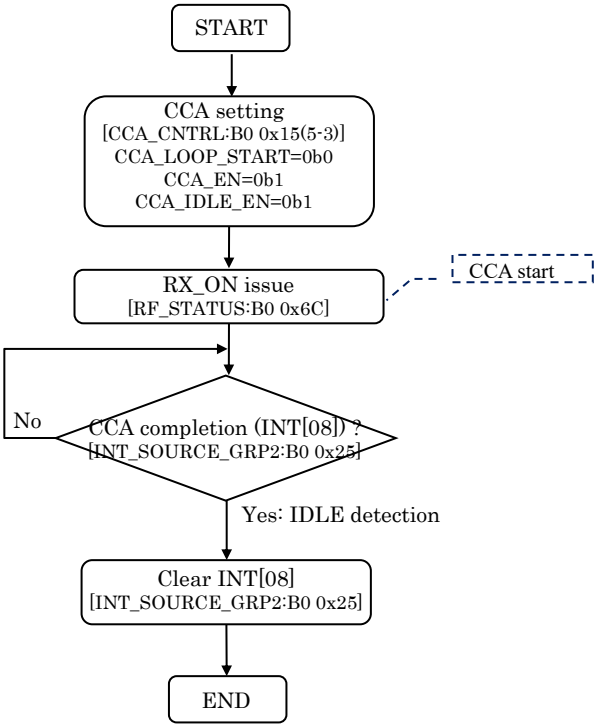
●Continuous mode

CCA continuous mode will be executed by issueing RX_ON by [RF_STATUS:B0 0x6C] register after setting CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b0 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b1. In this mode, CCA continues until CCA_LOOP_STOP ([CCA_CNTRL:B0 0x15(6)]) =0b1 is set. In this mode, CCA_DONE ([CCA_CNTRL: B0 0x15(2)]) will not be 0b1 and CCA completion interrupt (INT[08] group2) is not generated. During CCA execution, CCA_RSLT[1:0] ([CCA_CNTRL:B0 0x15(1-0)]) and CCA_PROG[9:0] ([CCA_PROG_L/H:B0 0x19(7-0)/1A(1-0)]) are constantly updated. The value will be kept by setting CCA_LOOP_STOP=0b1.



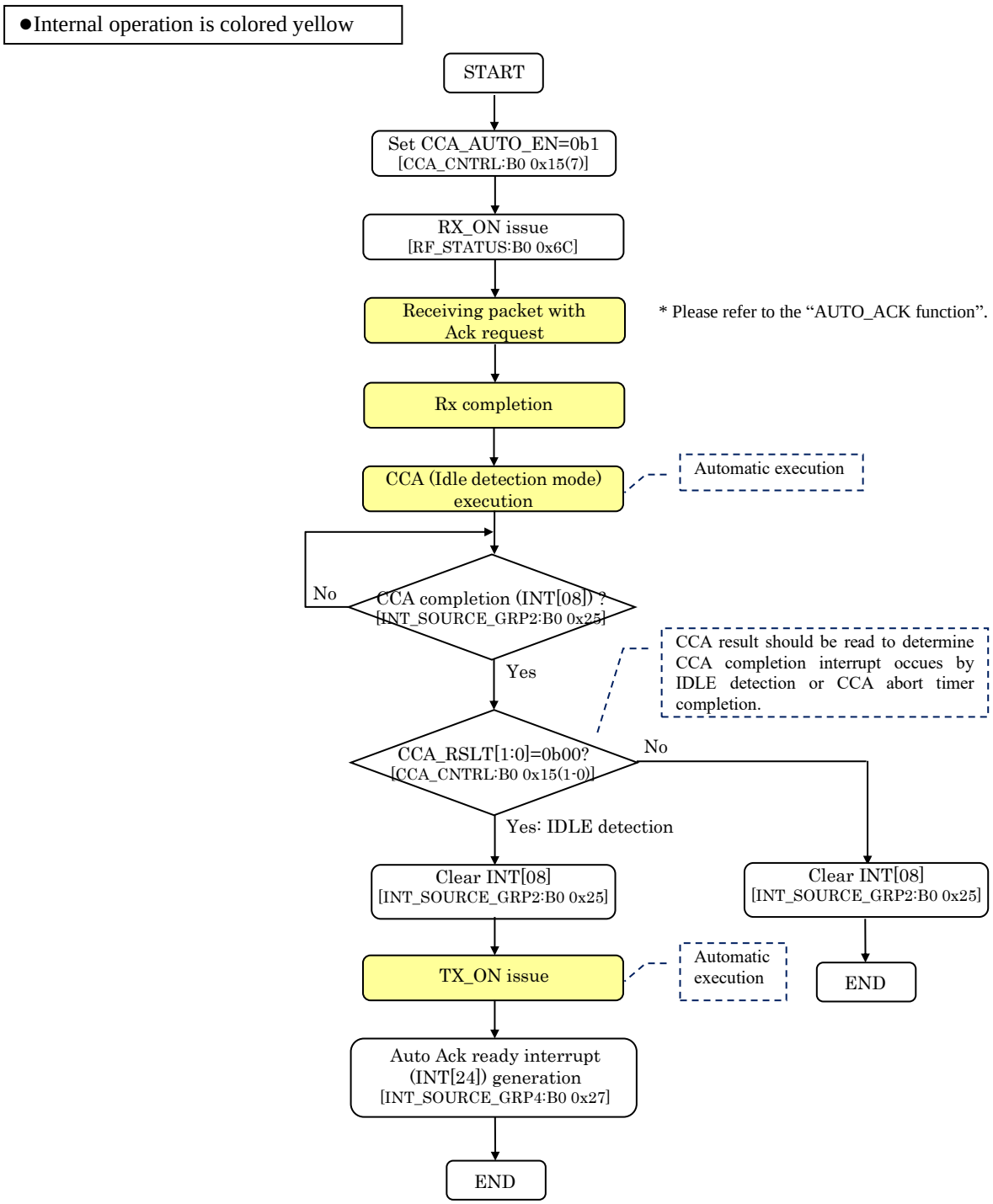
●IDLE detection mode

CCA is continuously executed until IDLE is detected. CCA (IDLE detection mode) will be executing by setting RX_ON by [RF_STATUS:B0 0x6C] register after setting CCA_EN ([CCA_CNTRL:B0 0x15(4)])=0b1, CCA_IDLE_EN ([CCA_CNTRL:B0 0x15(3)])=0b1 and CCA_LOOP_START ([CCA_CNTRL:B0 0x15(5)])=0b0..

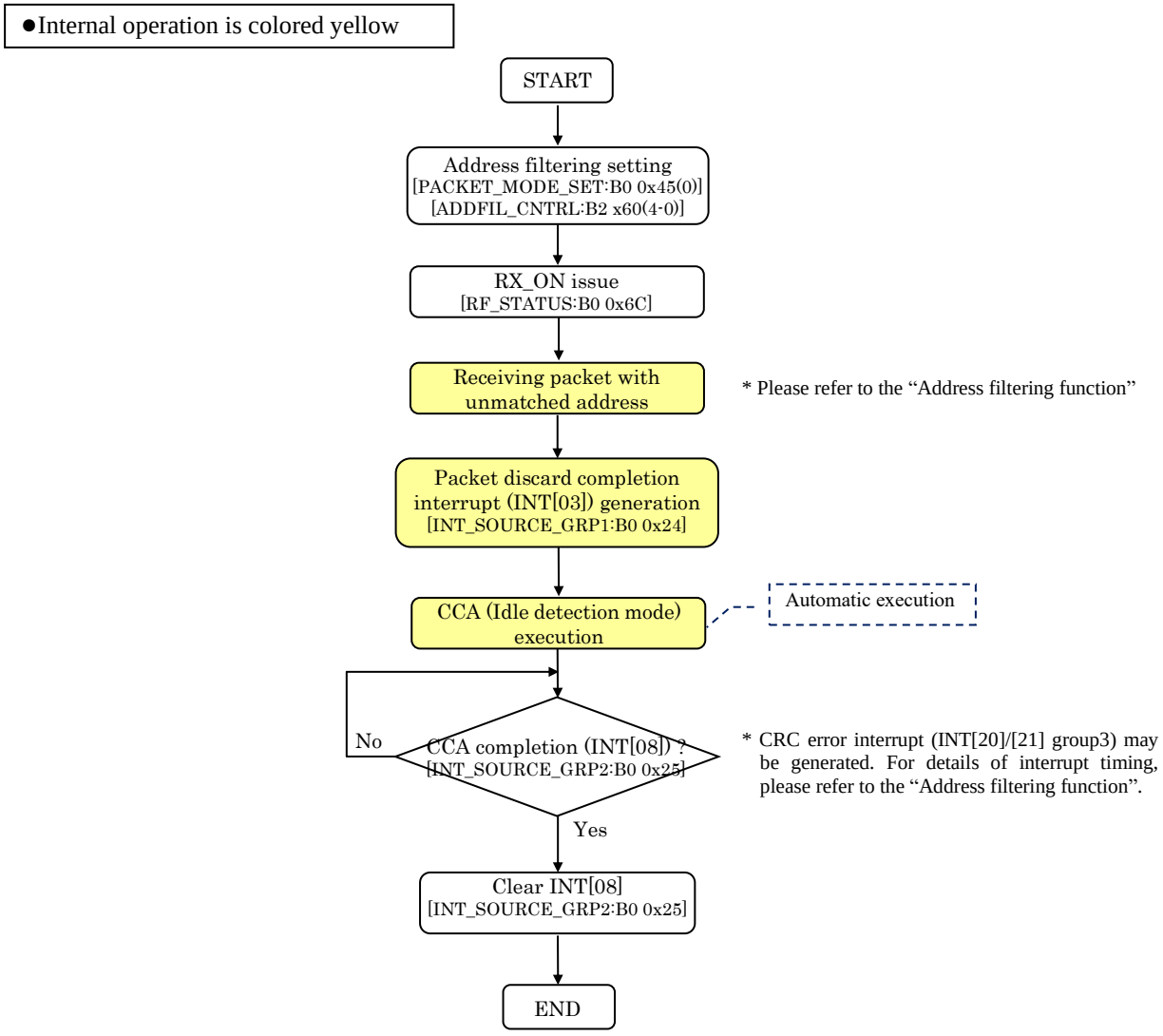


In the below condition, CCA (IDLE detection mode) will be executed automatically.

1. When set 0b1 to ting CCA_AUTO_EN ([CCA_CNTRL:B0 0x15(7)]), CCA (IDLE detection mode) will be executed after receiving Ack request packet.



2. When Address Filtering function is enabled by set 0b1 to one of bit4-0 in [ADDFIL_CNTRL:B2 0x60] register, and if ADDFIL_IDLE_DET ([PACKET_MODE_SET:B0 0x45(0)]) =0b1, CCA (IDLE detection mode) will be executed after discardingRx data.



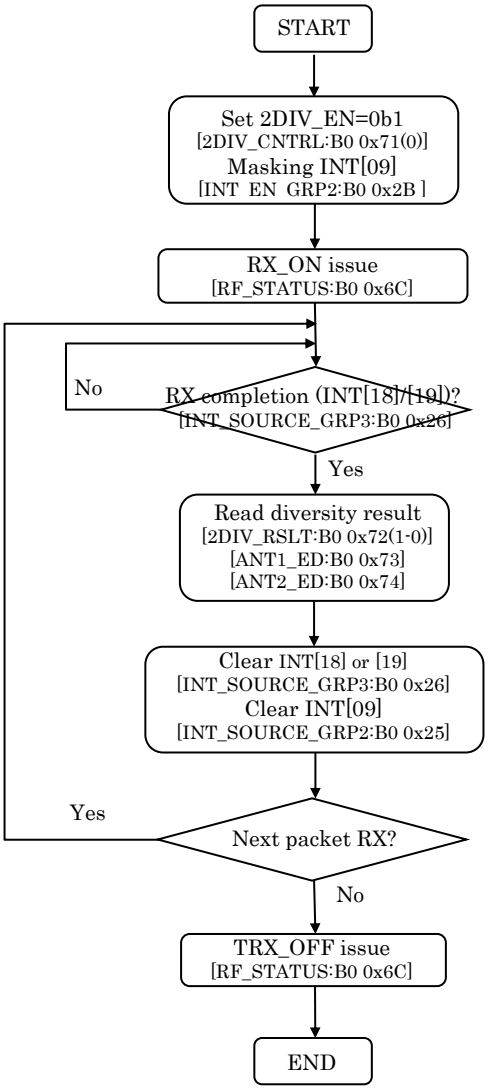
●2 diversity operation

After setting 2DIV_EN ([2DIV_CNTRL: B0 0x71(0)])=0b1, issuing RX_ON by [RF_STATUS:B0 0x6C] register. Antennas are switched to acquire each ED value, the antenna with higher ED value will be automatically selected.

ML7396 supports recovering function from incorrect diversity completion caused by errornous detection due to thermal noize, After dicersity search completion, if preamble can not be detected until antenna search timer expiration, ML7396 judges the previous diversity search completion is incorrect and resume diversity operation automatically.

When resume diversity operation for next packet receiving, please clear RX completion interrupt (INT[18]/[19] group3) and Diversity search completion interrupt (INT[09] group2). For details, please refer to "Diversity function".

ED values ([ANT1_ED:B0 0x73], [ANT2_ED:B0 0x74] registers) from diversityantennas and the diversity result ([2DIV_RSLT:B0 0x72(1-0)]) will be cleard when clearing Diversity search completion interrpy, clearing RX completion or Diversity resume by errornous detection. ED values and diversity result should be read before clearing RX completion interrupt.



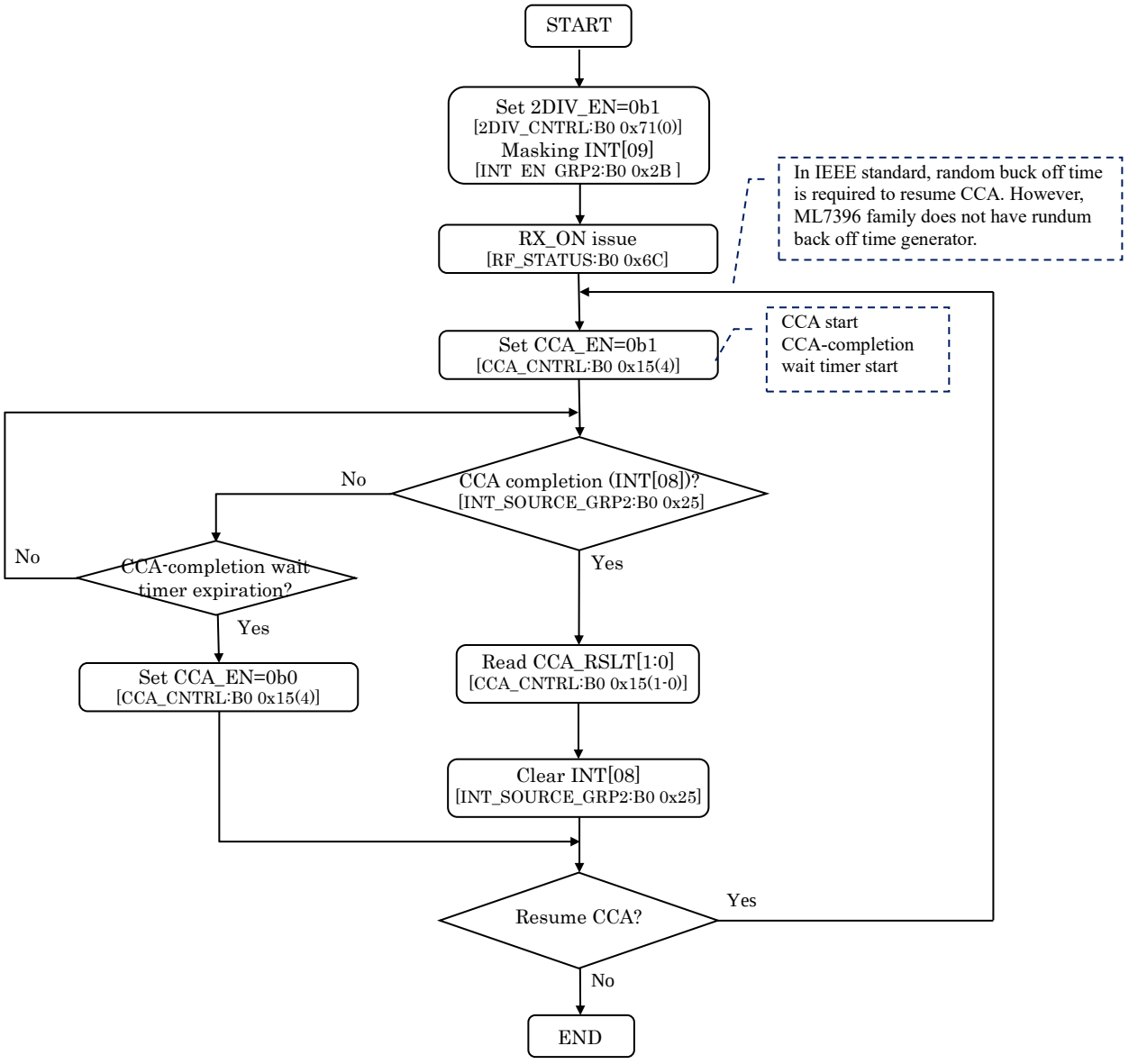
* If set 2DIV_EN=0b1 after issuing RX_ON, diversity will be executed after search timer completion defined by [2DIV_SEARCH:B0 0x6F] register. If SFD is detected while seatch timer counting, diversity will not be executed and keep receiving.

* Diversity search completion interrupt (INT[09] group2) should be cleard at same timing of RX completion interrupt clearance.

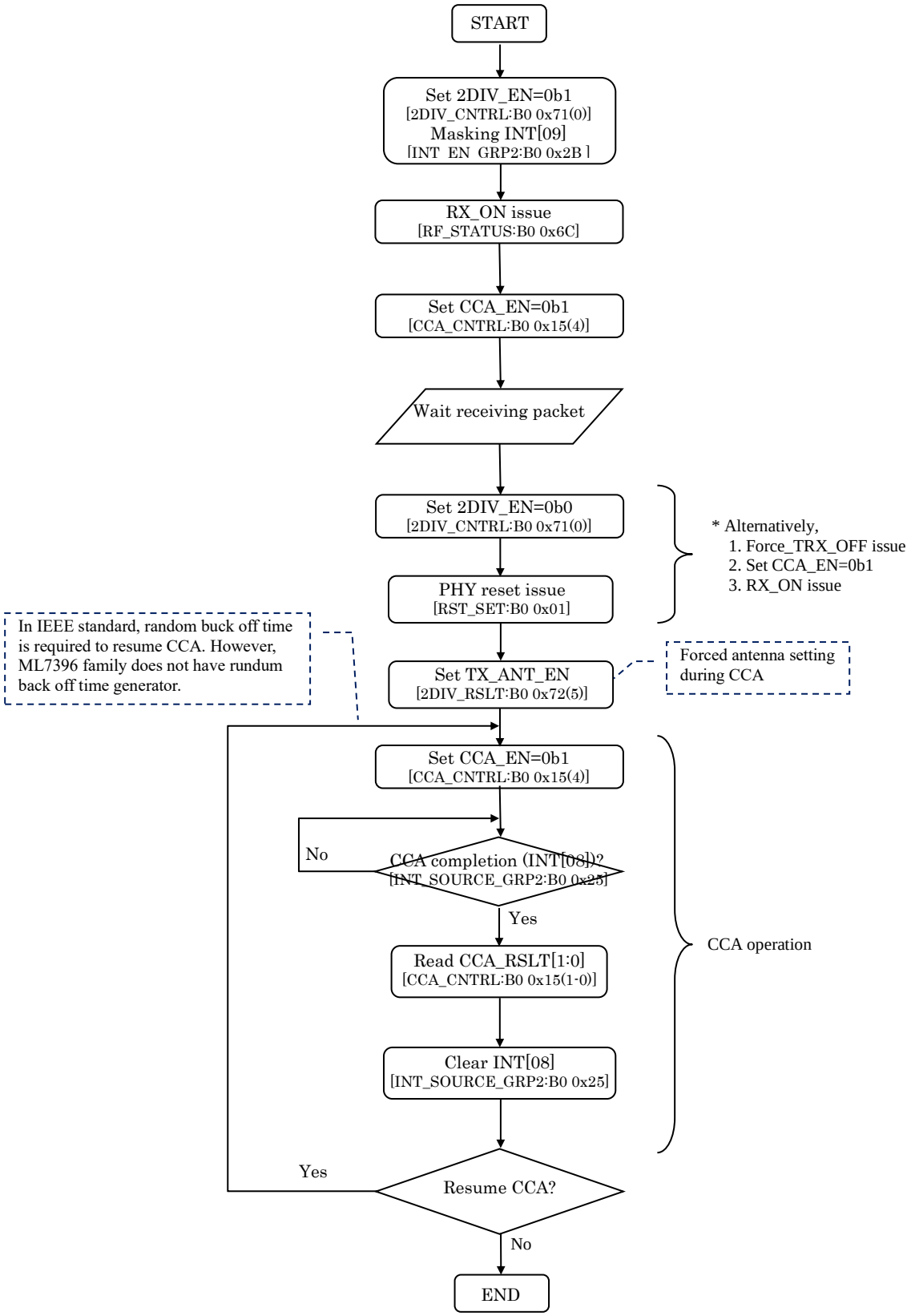
●CCA operation during diversity

If CCA is executed during diversity operation, there is a case CCA_DONE ([CCA_CNTRL:B0 0x15(2)]) is not notified and keep CCA operation. When executing CCA during diversity, set CCA-competion wait timer (case1), or once disabling diversity before CCA execution (case 2).

Case 1: Set CCA completion wait timer



Case 2: Disbleing diversity before CCA execution

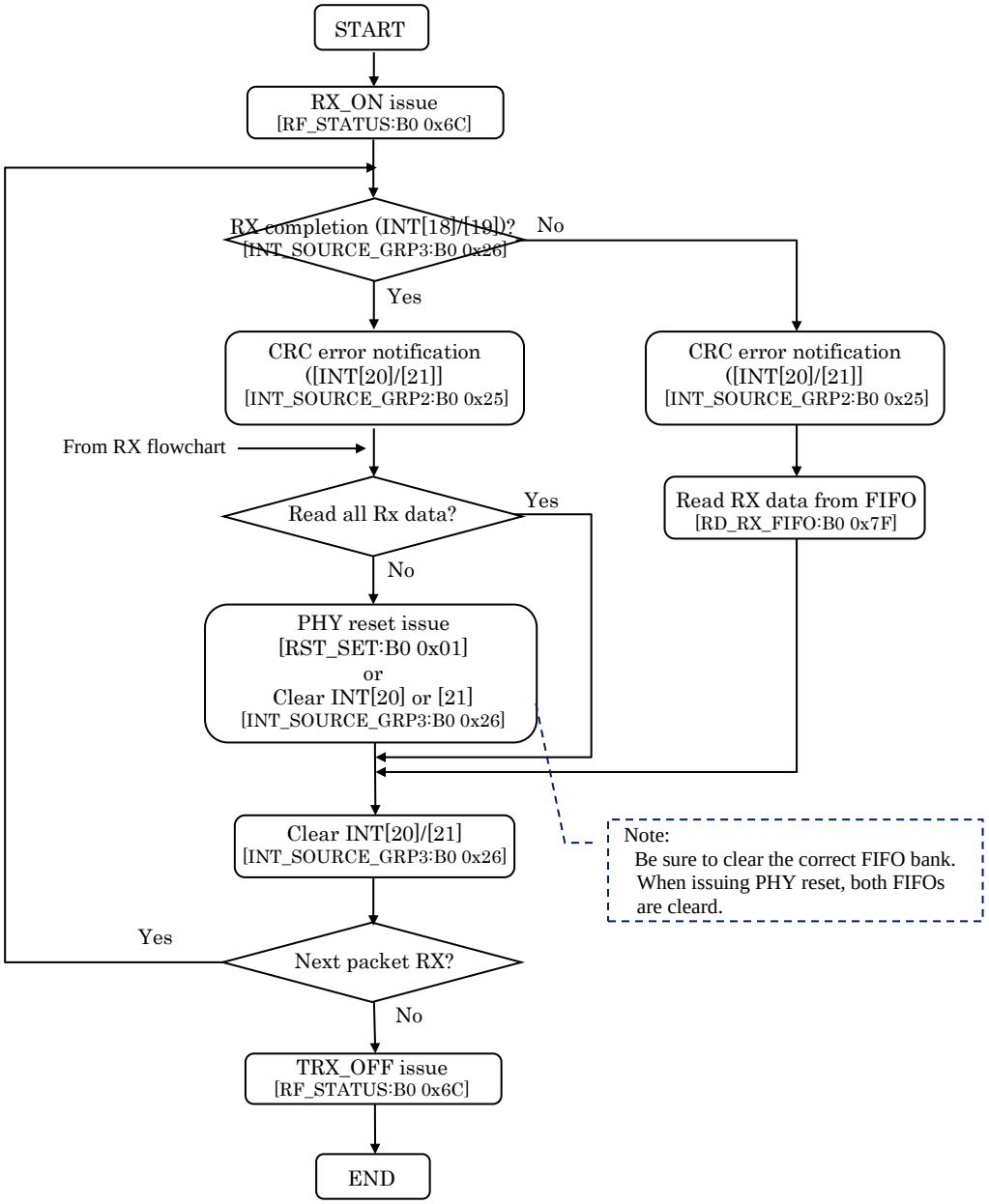


●Error process

●CRC Error

Case 1: CRC error occurs due to bit error
If CRC error occurs due to bit error, no need to read out Rx data from FIFO. By issuing PHY reset by [RST_SET:B0 0x01] register or FIFO clear by [INT_SOURCE_GRP1:B0 0x24] register, receiving status can be maintained.
For details of FIFO clear, please refer to “FIFO clear” in “Flow Charts”.

Case 2: Out-of-sync detection after SFD detection (During Length, Data, CRC field receiving)
If out-of-syn is detected after SFD detection, CRC error interrupt (INT[20]/[21] group3) will be notified. However RX completion interrput (INT[18]/[19] group3) will not be generated. If this case occurs, read Rx data that amount is specified Length field from FIFO and then clearing CRC error interrpt.



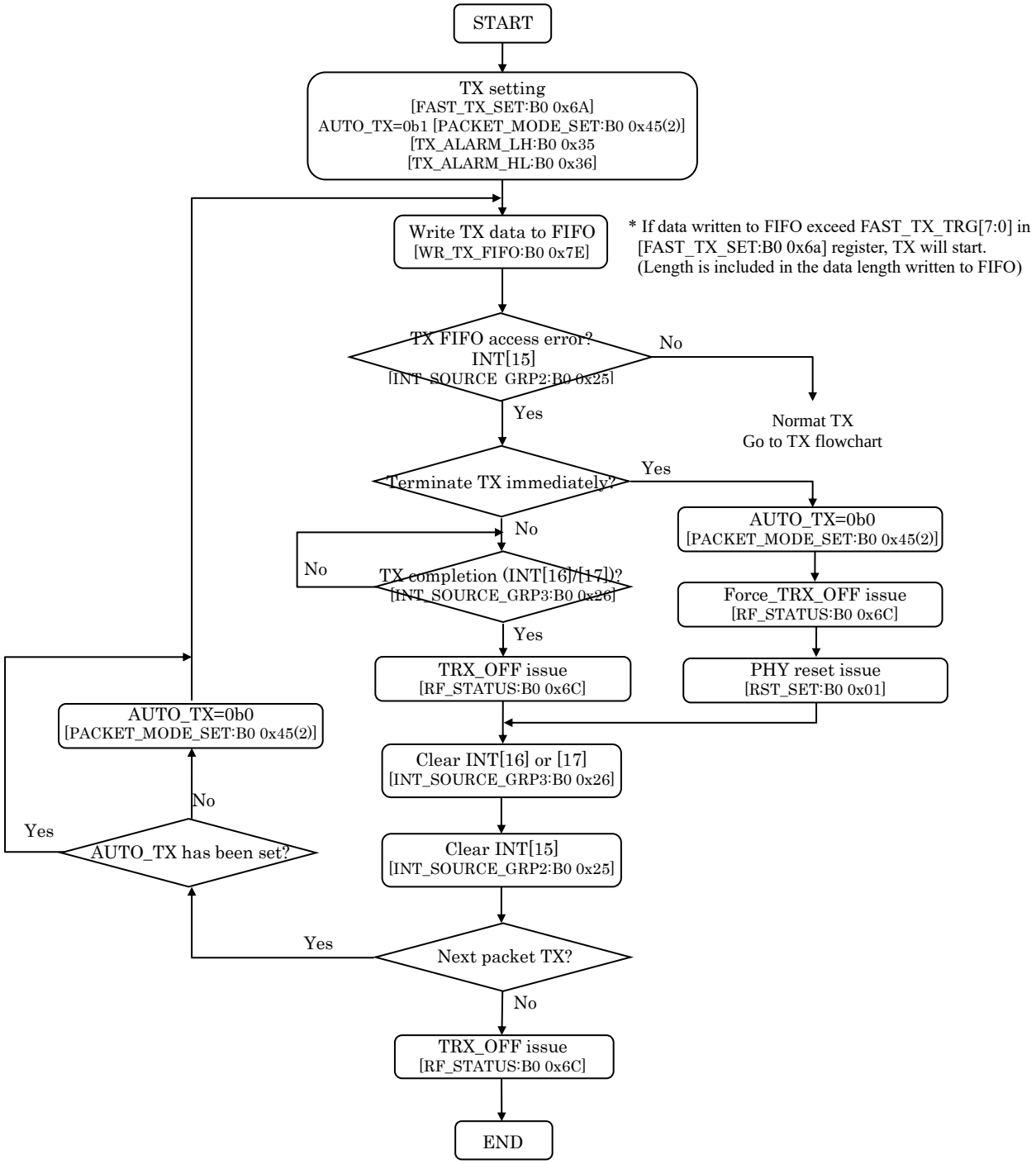
●TX FIFO Access Error

If one of the following conditions is met, TX FIFO access error interrupt (INT[15] group2) will be generated.

- The 3rd packet data is written to a FIFO when the transmitting data remain in both FIFO0 and FIFO1.
- Data write overflow occurs to a FIFO.
- No TX data in the TX_FIFO during TX data transimission.

When TX FIFO acccess error interrupt occurs, issuing TRX_OFF after TX completion interrupt(INT[16]/[17] group3) is recognized, or issueing Force_TRX_OFF by [RF_STATUS:B0 0x0A] register without waiting for TX completion interrupt. After that, clearing TX completion interrupt and TX FIFO access error interrrput..

If TX FIFO access error occurs, subquent TX data will be inverted. CRC error should be detected at rexeiver side even if TRX_OFF is issued when TX completion interrupt detected.



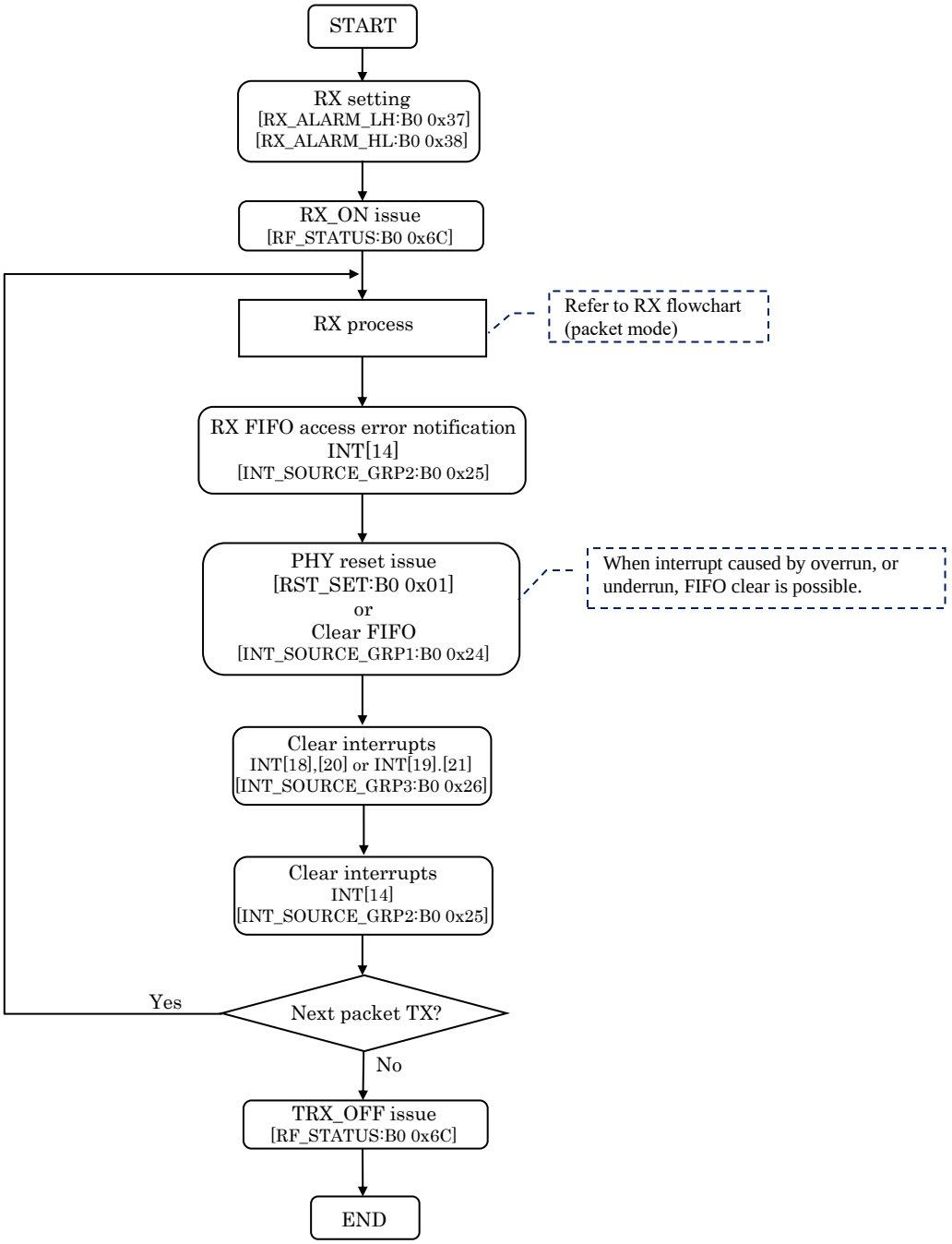
●RX FIFO Access Error

If one of the following conditions is met, RX FIFO access error interrupt (INT[14] group2) will be generated.

- Receiving the 3rd packet when the receiving data remain in both FIFO0 and FIFO1.
- RX data overflow occurs to RX_FIFO (Overrun)
- Read RX_FIFO during no data in the RX_FIFO (Underrun)

When RX FIFO access error interrupt occurs, after RX completion interrupt (INT[18]/[19] group3) is recognized, issuing PHY reset by [RST_SET:B0 0x01] register or FIFO clear by [INT_SOURCE_GRP1:B0 0x24] register. After that, clearing RX completion interrupt and RX FIFO access error interrupt.

After receiving 2 packets, by setting CLK1_EN ([CLK_SET:B0 0x02(1)] = 0b0, RX FIFO access error can be avoid.



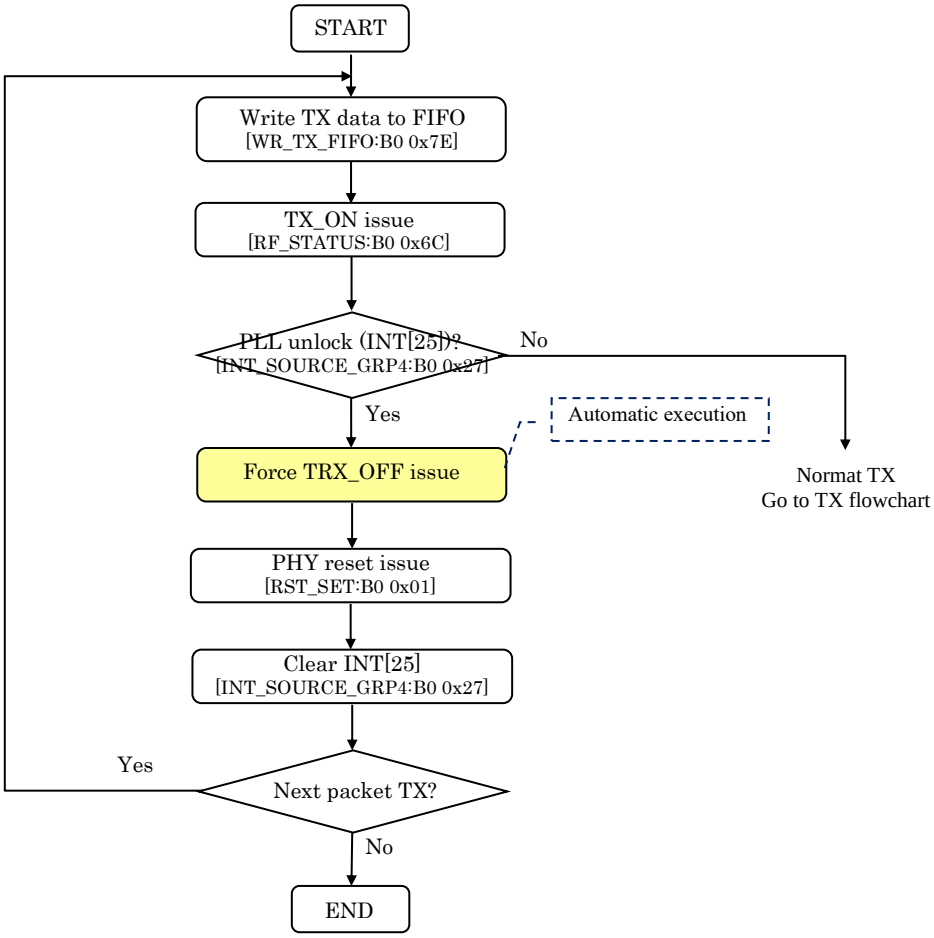
●PLL Unlock Detection

○ TX

During TX, if PLL unlock is detected, PLL unlock interrupt (INT[25] group4) will be generated. When PLL unlock interrupt occurs, Force_TRX_OFF is automaticcally issued and move to IDLE state.

Before next TX operation, issuing PHY reset by [RST_SET:B0 0x01] register and clearing PLL unlock interrupt should be required.

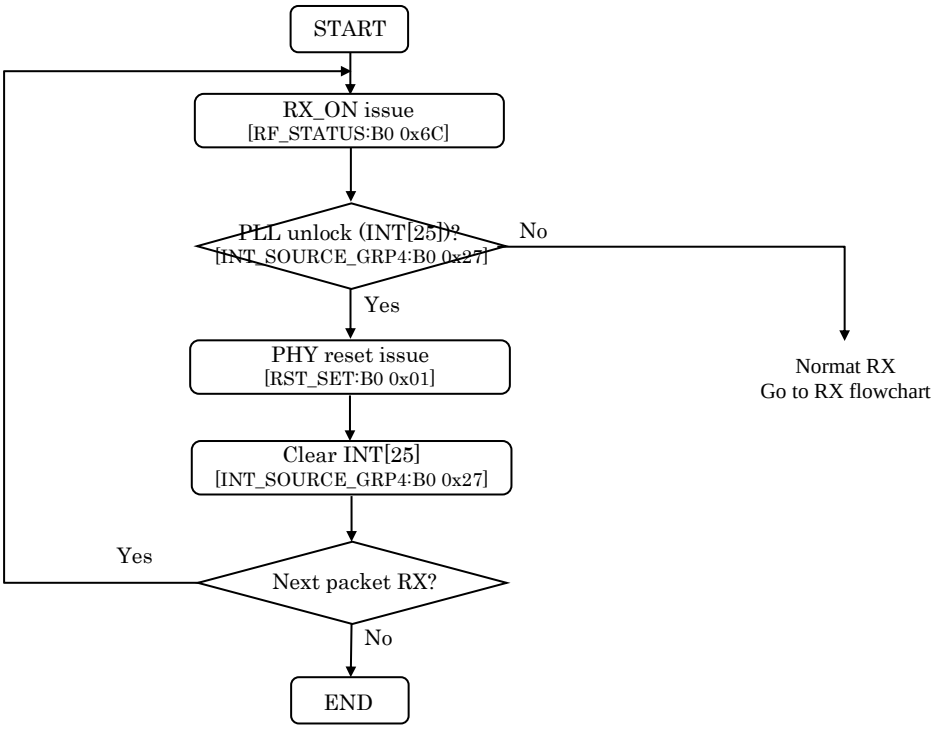
●Internal operation is colored yellow



○ RX

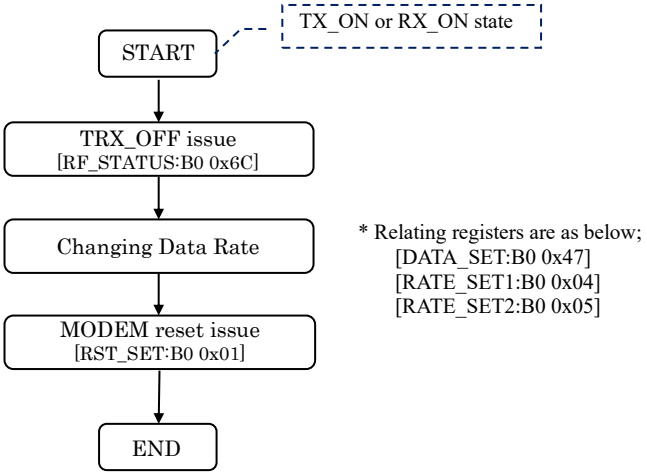
During RX, if PLL unlock is detected, PLL unlock interrupt (INT[25] group4) will be generated. During RX, even if PLL unlock is detected, RX_ON state is maintained (do not move to IDLE state).

Before next RX operation, issuing PHY reset by [RST_SET:B0 0x01] register and clearing PLL unlock interrupt should be required.



●Data Rate Change sequence

When changing data rate during operation, data rate should be set in TRX_OFF state. Issuing MODEM reset by [RST_SET: B0 0x01] register is required after data rate change. If not issuing MODEM reset, ML7396 can not transmit or receive correctlly.

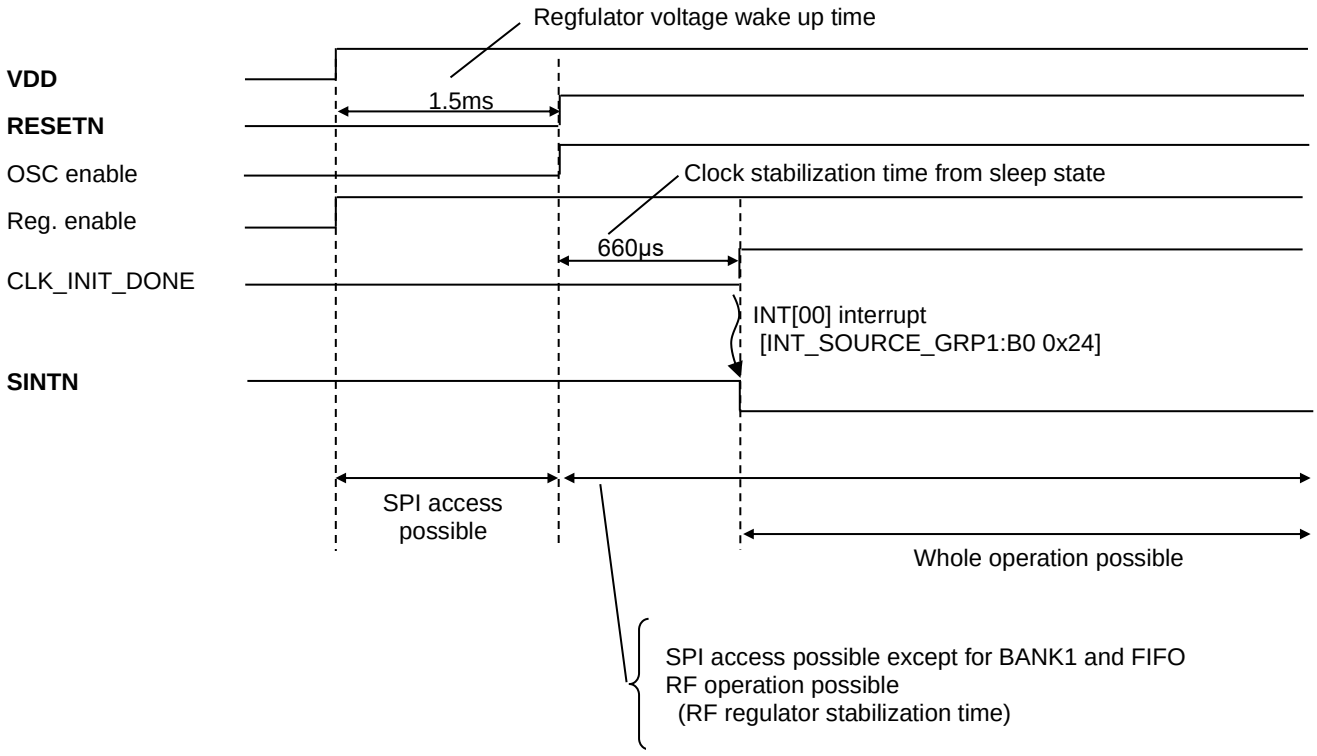


■Timing Chart

The followings are operation timing of major functions.

[Note]
Bold characters indicate pins relative signals. Non bold characters indicate internal signal.

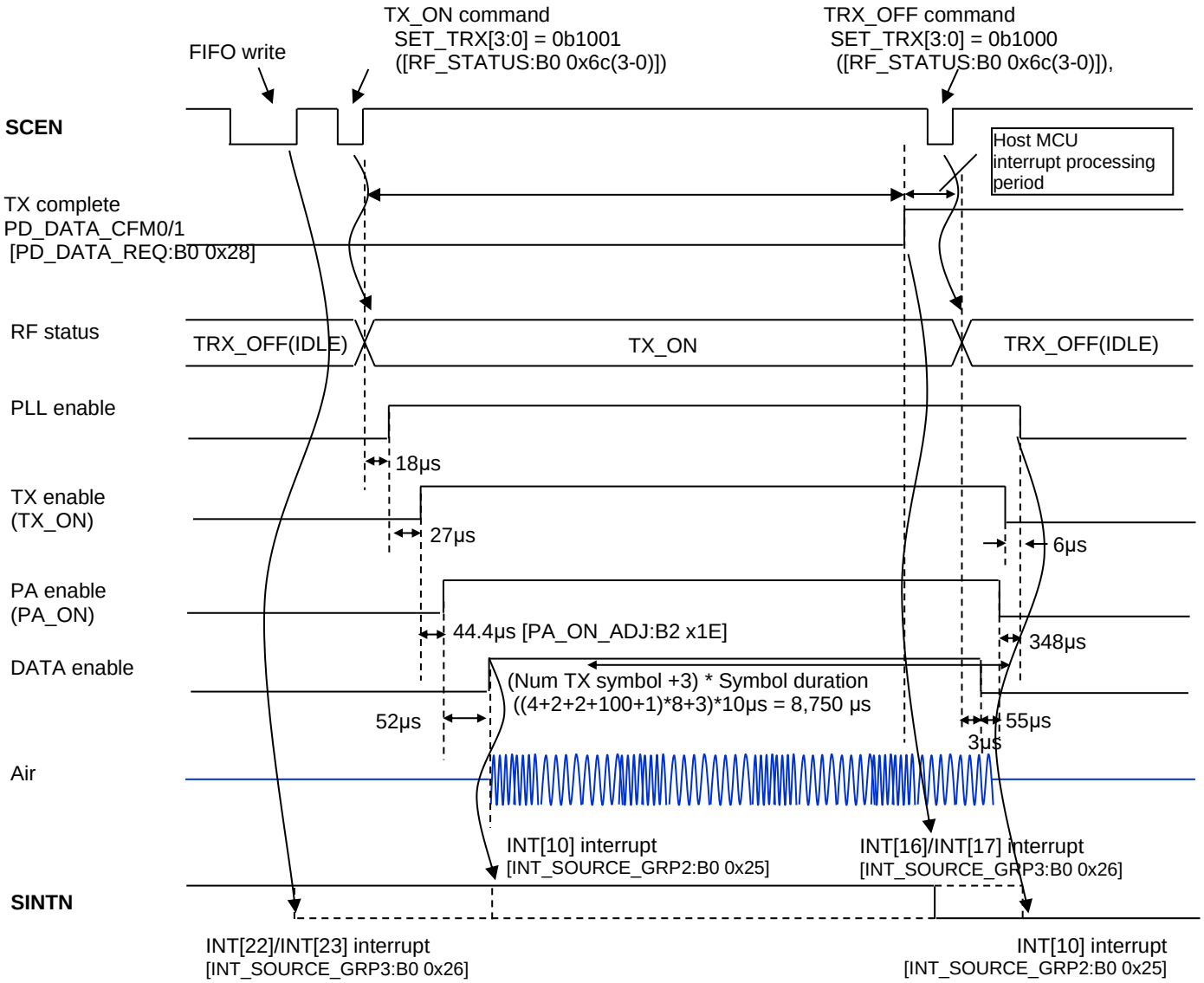
●Start up



●TX

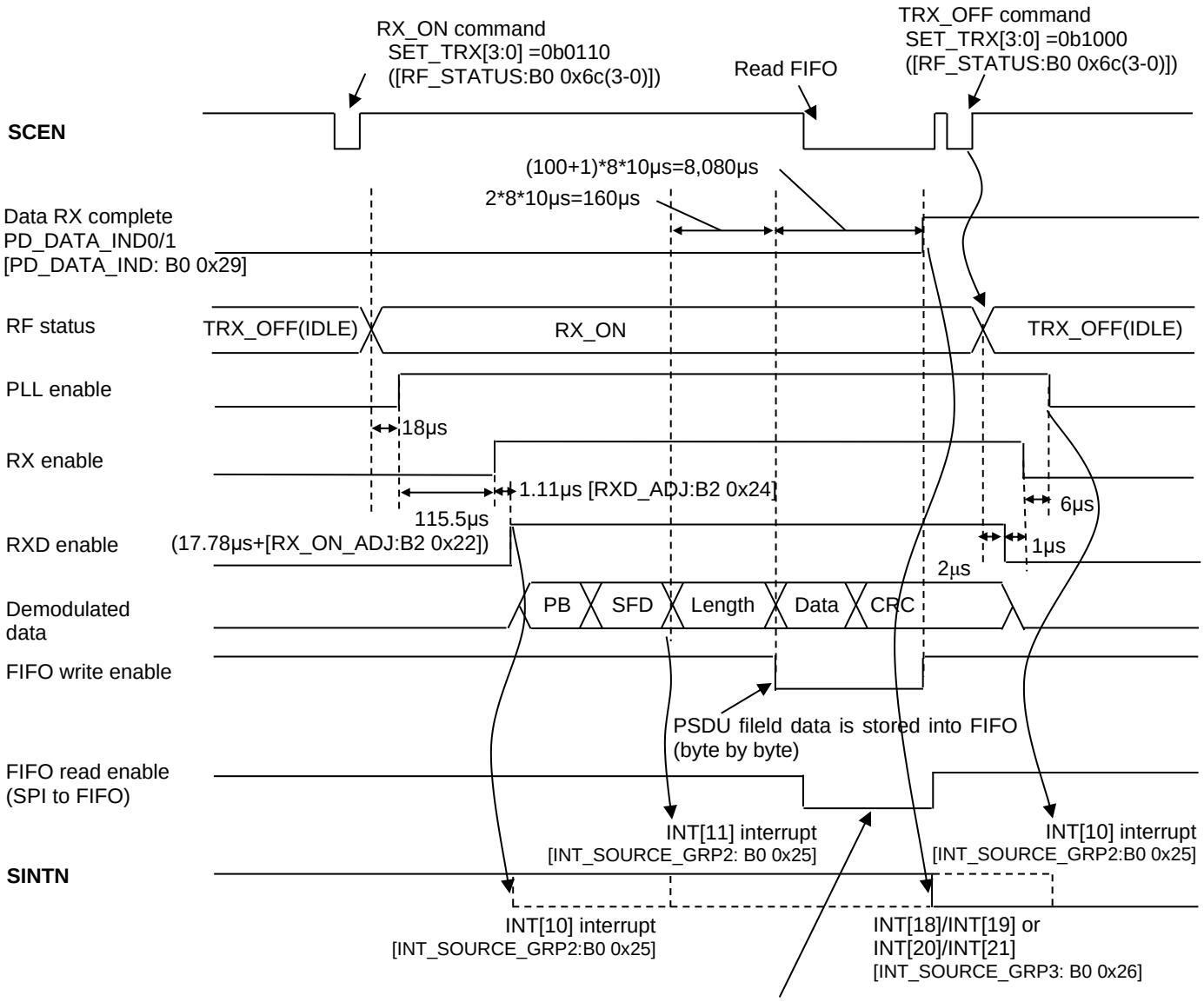
Conditions
•Symbol rate: 100 kbps
•Preamble length: 4 byte
•SFD length: 2 byte
•Length: 2 byte
•CRC: 8 bit (1 byte)
•Data length: 100 byte
•Ramp control: On

* Lamp control timing can be adjusted by the [2DIV_GAIN_CNTRL:B0 0x6E], [RX_ON_ADJ2:B1 0x3F] and [TX_OFF_ADJ1:B1 0x55] registers. For more details, please refer to the "Ramp control function".



●RX (without CCA)

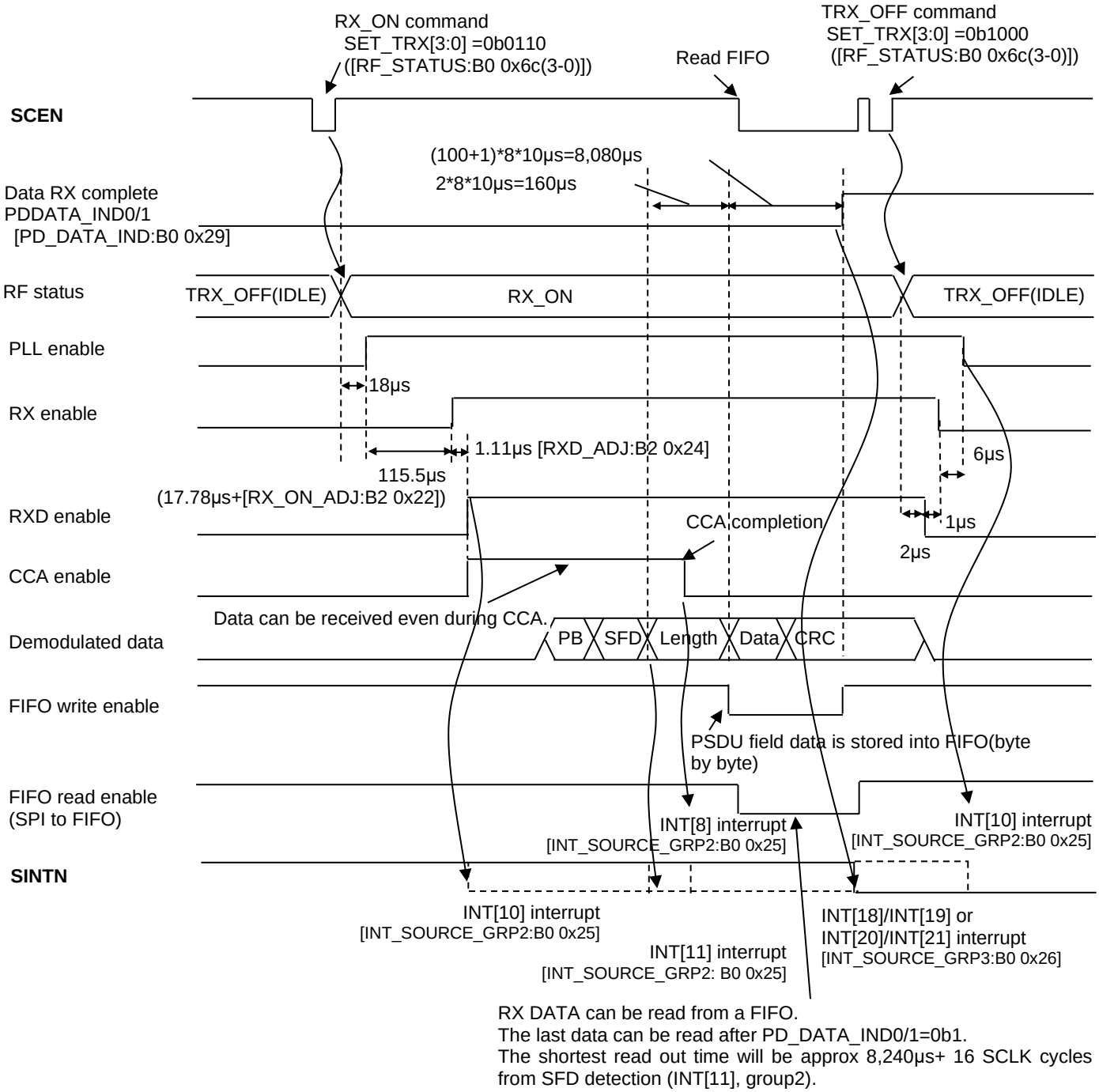
Conditions
•Symbol rate: 100 kbps
•Preamble length: 4 byte
•SFD length: 2 byte
•Length: 2 byte
•CRC: 8 bit (1 byte)
•Data length: 100 byte
•Ramp control: On



RX data can be read from a FIFO.
The last data can be read after PDDATA_IND0/1=0b1.
The shortest read out time will be approx 8,240µs+ 16 SCLK cycles from SFD detection (INT[11] , group2).

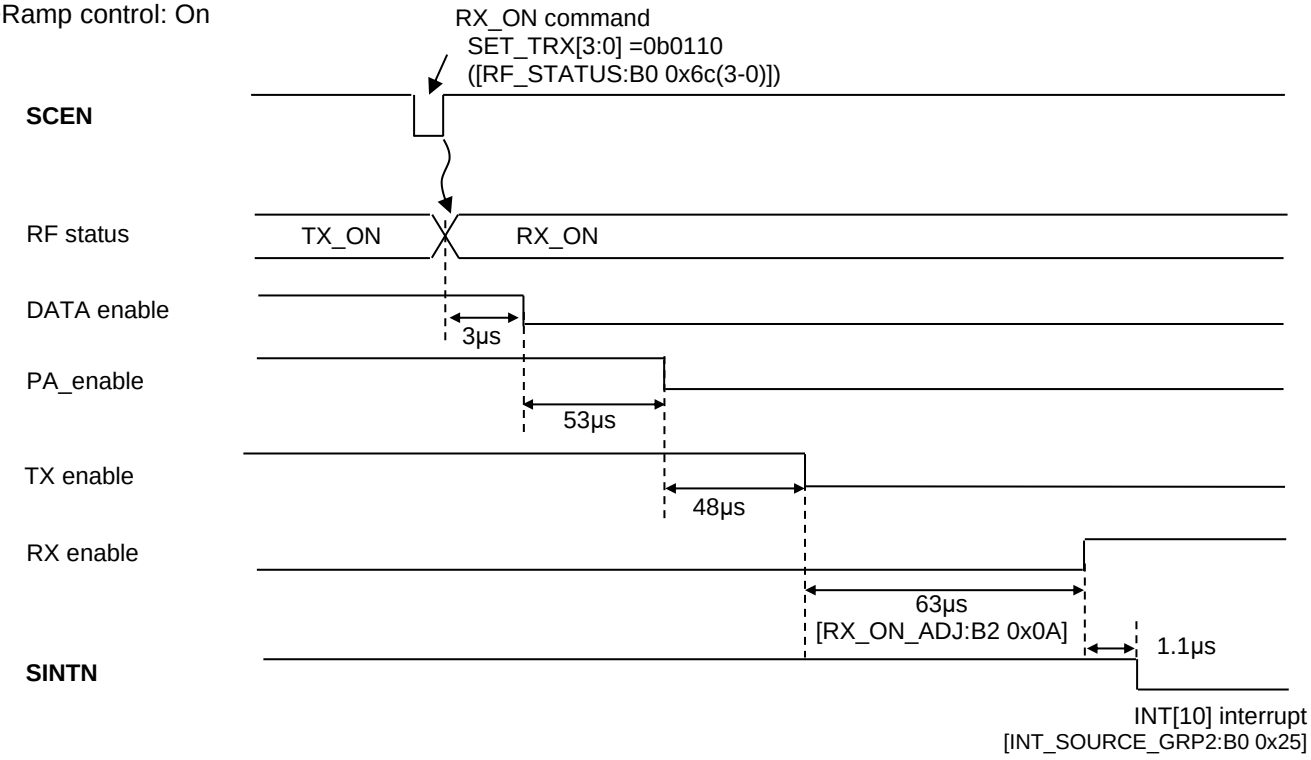
●RX (with CCA)

Conditions
•Symbol rate: 100 kbps
•Preamble length: 4 byte
•SFD length: 2 byte
•Length: 2 byte
•CRC: 8 bit (1 byte)
•Data length: 100 byte
•Ramp control: On



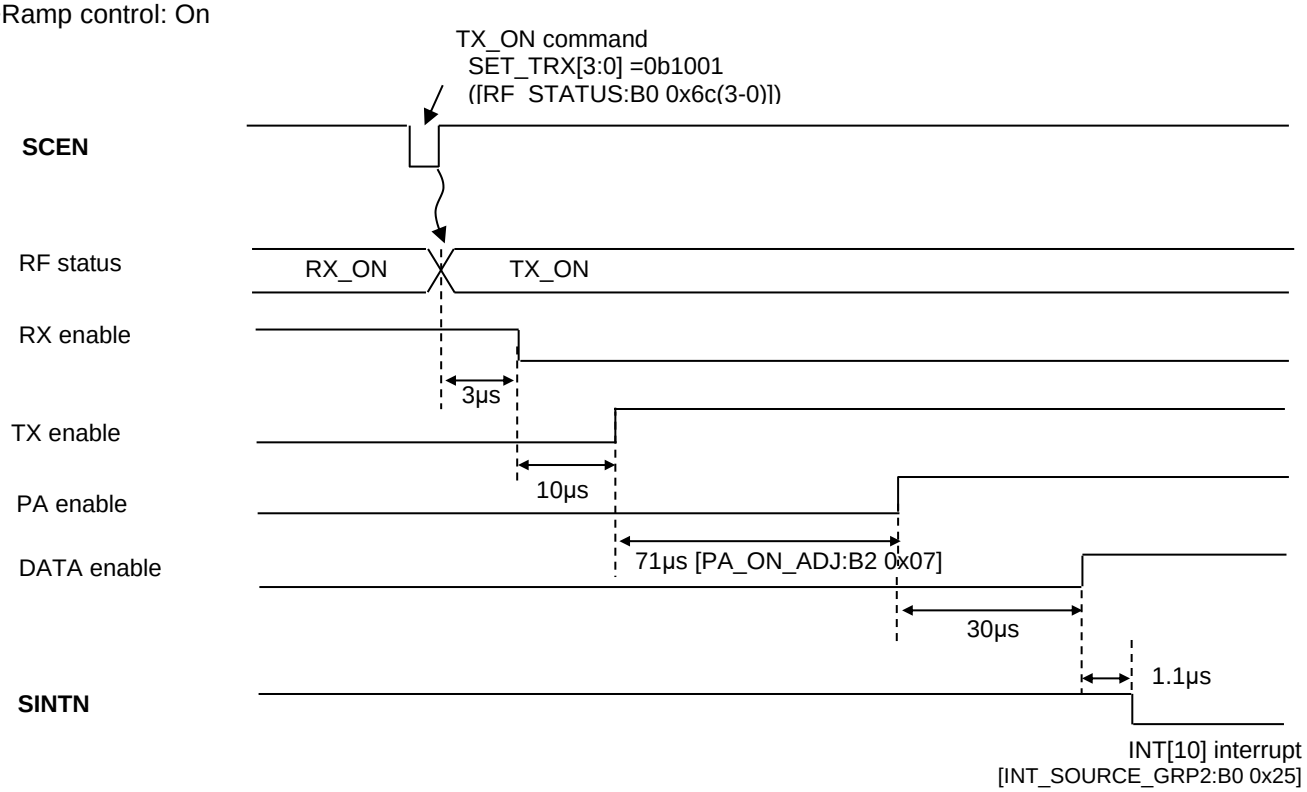
●Transition from TX to RX

Condition:
•Ramp control: On



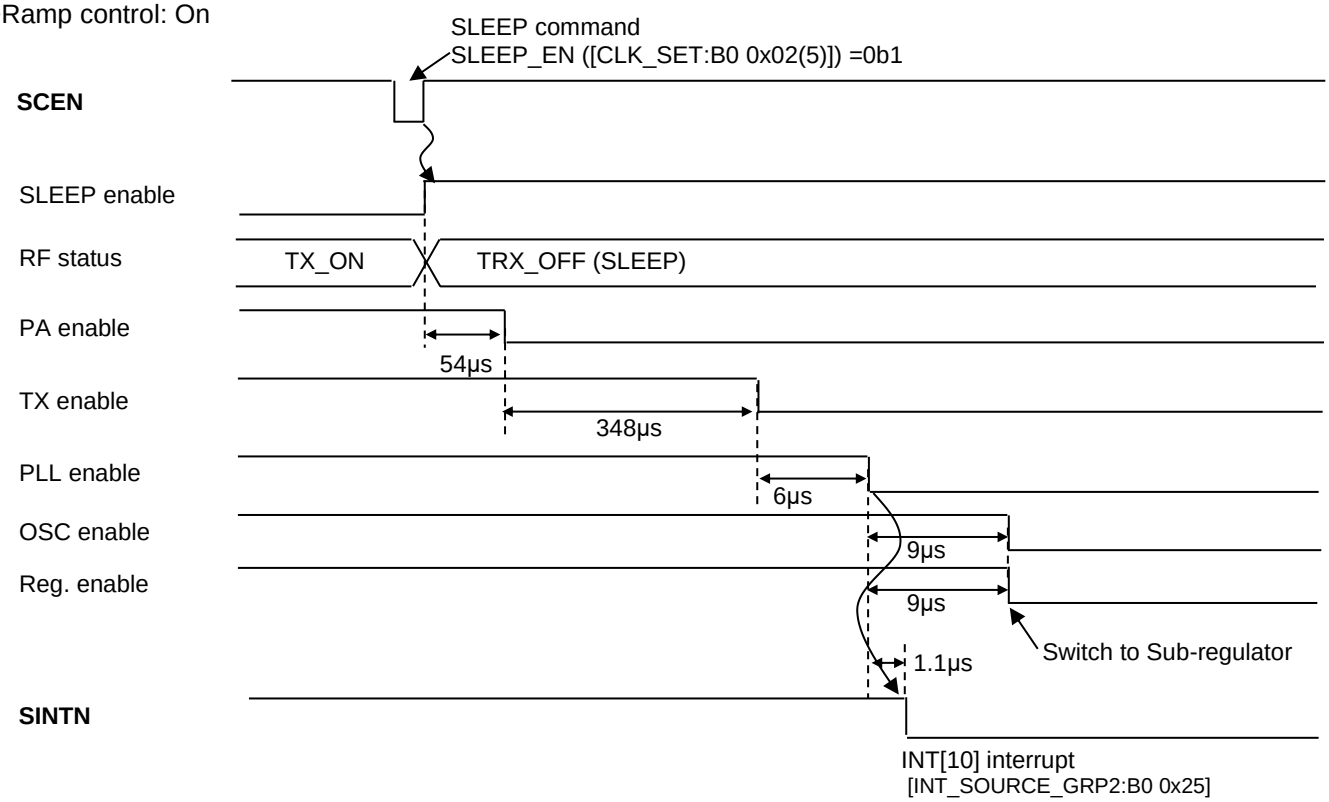
●Transition from RX to TX mode

Condition:
•Ramp control: On



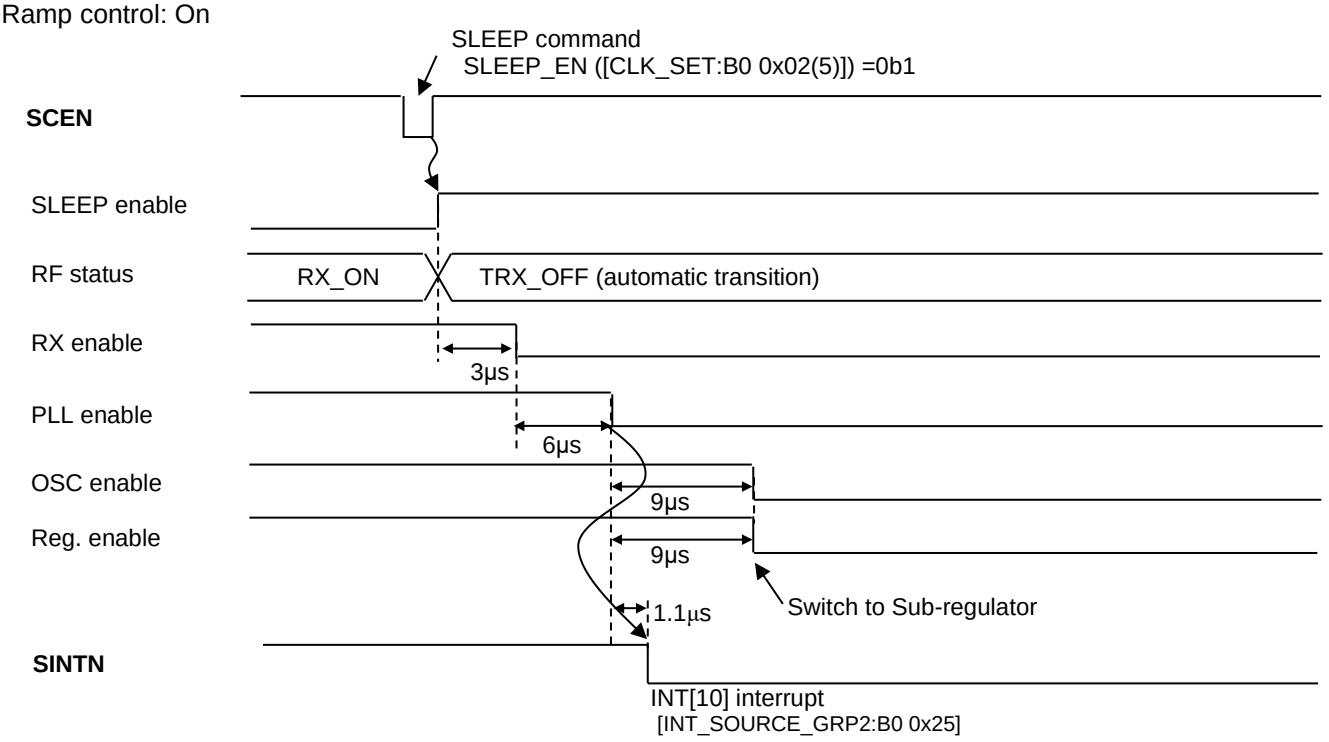
●Transition from TX to SLEEP

Condition:
•Ramp control: On

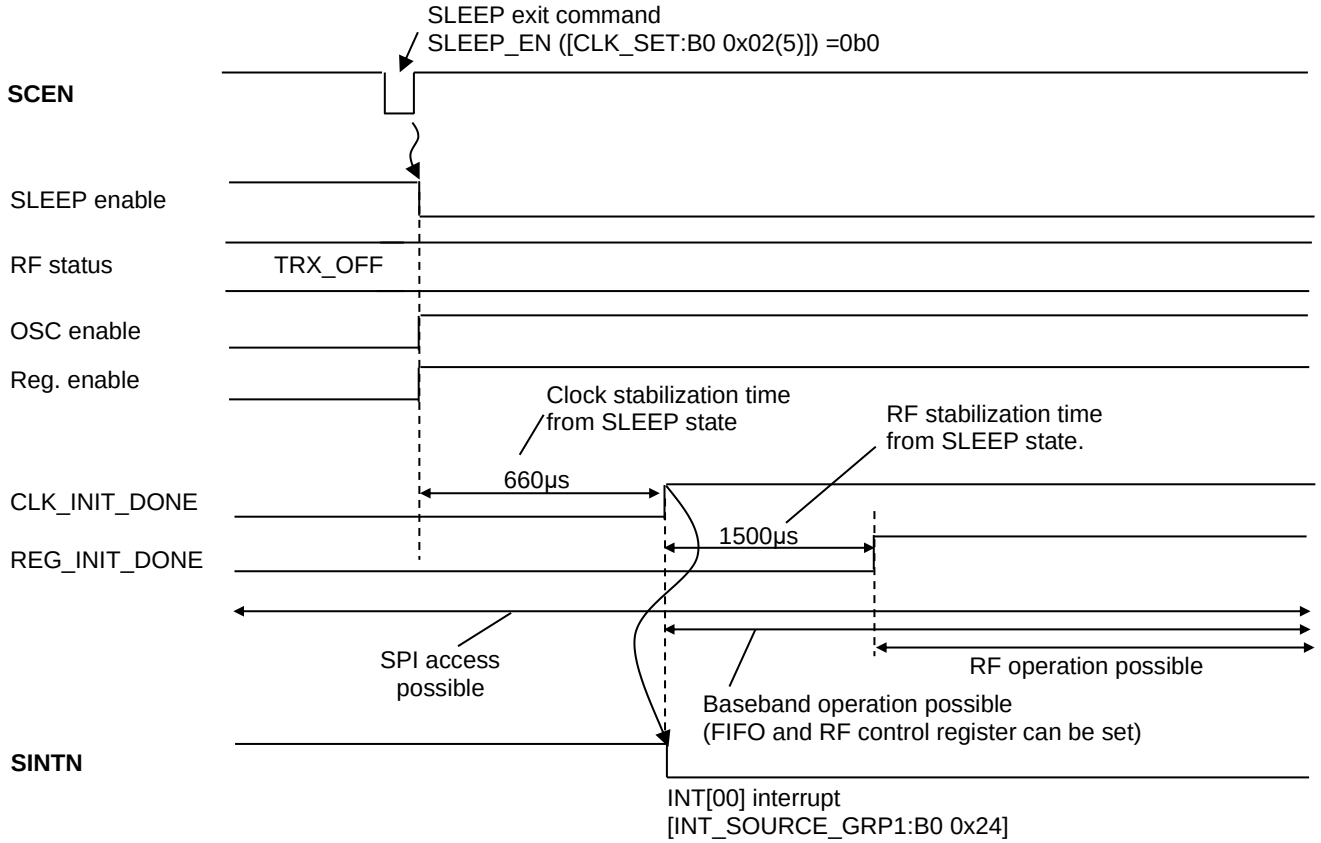


●Transition from RX to SLEEP

Condition:
•Ramp control: On

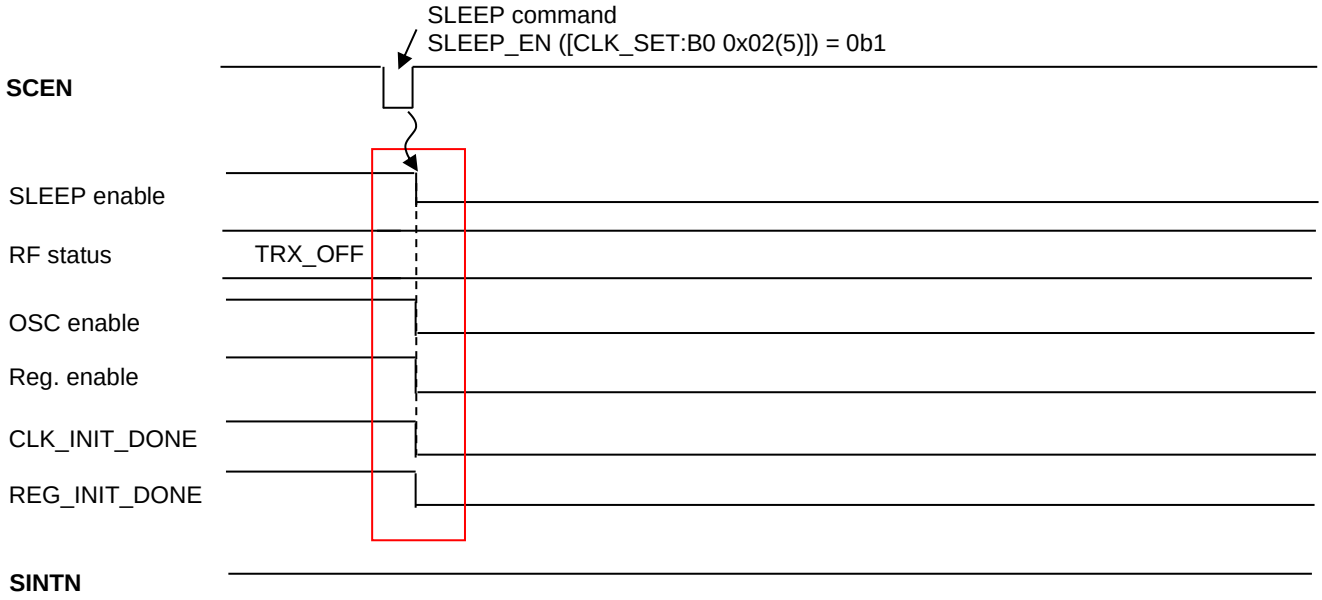


●Transition from SLEEP to IDLE



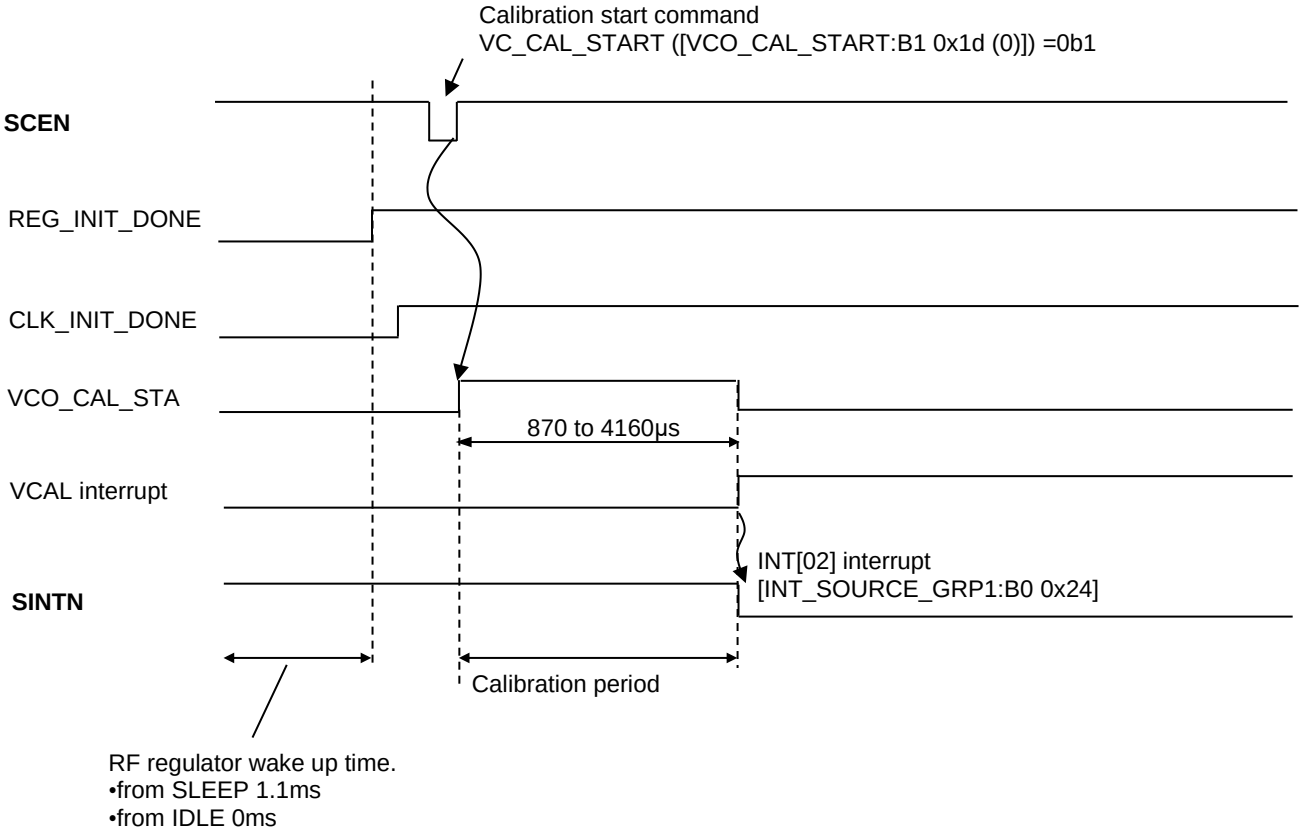
Note: When using TCXO, enabling TCXO (clock) before issuing SLEEP exit command. If enabling TCXO after issuing SLEEP exit command, the start time will delay for a certain time.

●Transition from IDLE to SLEEP



Note: If disabling TCXO during SLEEP, wait more than 4µs after issuing SLEEP command, then disabling TCXO (clock).

●VCO Calibration



■About FCC Support

ML7396A (915MHz band) complies with FCC PART 15. When the outputpowe is -1dBm or less, PART 15.249 is applied, and when the output power is +30dBm or less, PART 15.247 is applied. Spurious emissions should comply with PART 15.209.
PART 15.247 requires the frequency hopping or the wideband digital modulation. For details of the frequency hopping, please refer to the "About frequency hopping" below. For details of the wideband digital modulation, please refer to the " Initial register setting " file.

●About frequency hopping (FHSS: Frequency Hopping Spread Spectrum)

According to the FCC (United States radio act) Part 15.247, the FHSS system which 20dB bandwidth is less than 250 kHz, should have 50 or more hopping channels. If 20dB bandwidth is 250 kHz or more, 25 or more hopping channels should be supported. And the channel occupation time should be limited to 400ms at a maximum.
The following examples show how to control and set registers in order to comply with above regulations.
For details of register settings, please refer to the "Initial registers setting" file.

・ Frequency switch flow during TX
(0) TX completion (TX_ON)
(1) Transition to TRX_OFF or RX_ON state by SET_TRX[3:0] ([RF_STATUS:B0 0x6C(3-0)]).
(2) Switching frequency by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49] and [CH0_FH:B0 0x4A] registers.
(3) Issuing TX_ON command by SET_TRX[3:0].
Repeat (0) to (3).

• Frequency switch flow during RX
(0) RX completion (RX_ON)
(1) Masking PLL unlock interrupt by INT_EN[25] ([INT_EN_GRP4:B0 0x2D(1)]) =0b0.
(2) Switching frequency by [CH0_FL:B0 0x48], [CH0_FM:B0 0x49] and [CH0_FH:B0 0x4A] registers.
(3) Wait 100μs. (PLL lock period)
(4) Clear the PLL unlock interrupt (INT[25] group4), and enable the interrupt by INT_EN[25] =0b1
(5) Receive data
Repeat (0) to (5).
* PLL unlock interrupt may be detected during frequency switch.
It is recommended to masking the PLL unlock interrupt for 100μs during frequency switch as shown in (1) to (4).

The following examples show how to control the frequency hopping system.

•Control example 1. TX equipment transmits a long term preamble, and the RX equipment scans channels to detect a preamble

TX equipment hops the frequency according to the hopping pattern. And the channel occupation time should be less than 400ms to comply with the regulation.
RX equipment does not know the using channel transmitting preamble, and so scans all channels for detecting preamble. The preamble transmitting period should be longer than the channel scan period on the RX equipment. For details of the channel scan flow, please refer to the flow chart shown later.
The one channel scan time can be calculated as "preamble search period (36bits / data rate) + PLL lock period (100μs)".
The following table shows the channel scan period for each data rate. Please set an appropriate preamble length according to the following table. The preamble length can be set by [TX_PR_LEN:B0 0x42] register. (max. 255 bytes)

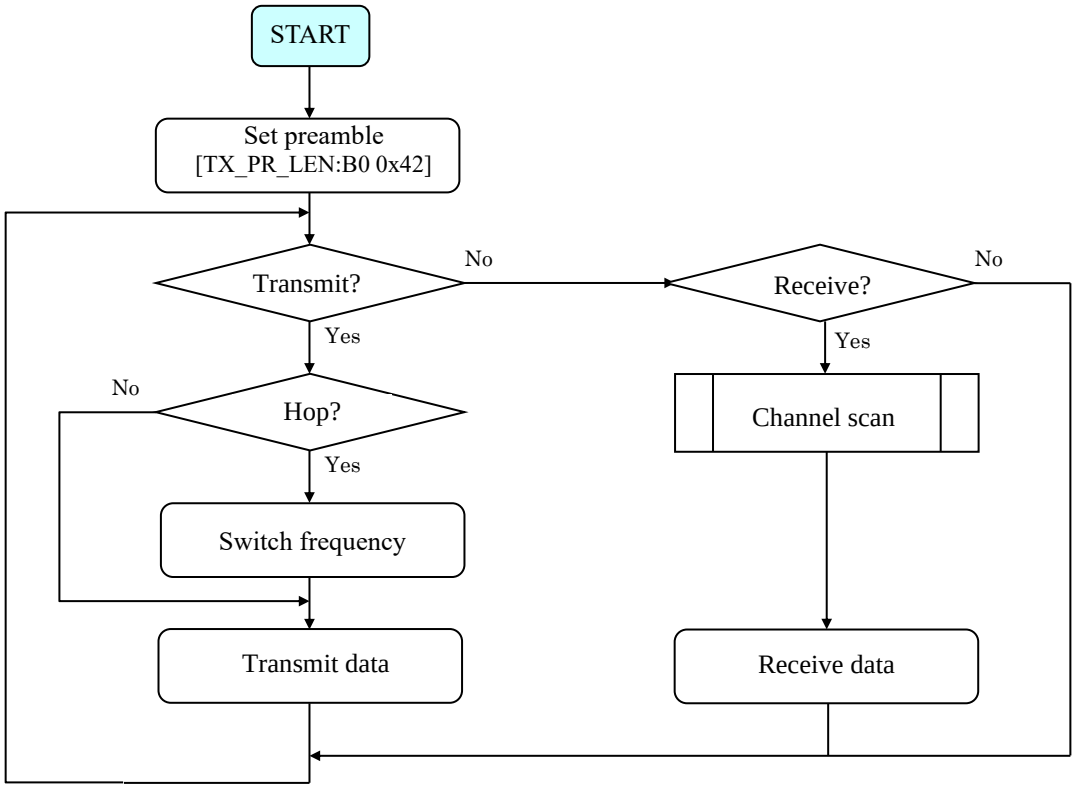
Table. Channel scan period for each data rate

data rate [kbps]	255 byte PB transmitting period [ms]	Required period for one channel scan [ms]	Required period for all channels scan [ms]		Availability	
			25ch	50ch	25ch	50ch
10	204.0	3.70	92.5	185.0	○	○
20	102.0	1.90	47.5	95.0	○	○
40	51.0	1.00	25.0	50.0	○	○
50	40.8	0.82	20.5	41.0	○	×
100	20.4	0.46	11.5	23.0	○	×
150	13.6	0.34	8.5	17.0	○	×
200	10.2	0.28	7.0	14.0	○	×
400	5.1	0.19	4.8	9.5	○	×

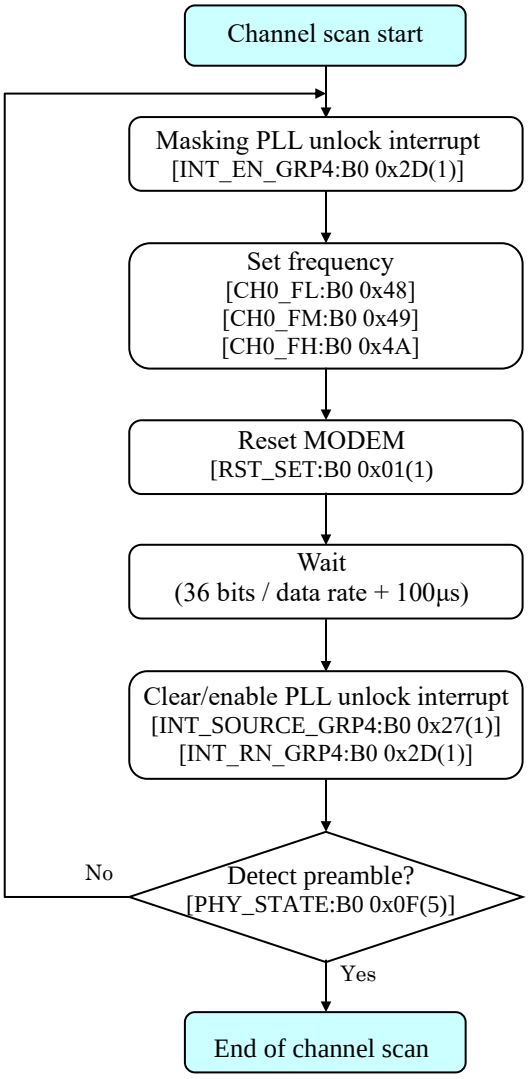
* This table does not take into account the register access time.

* This control method cannot be applied under the "×" condition, since the all channel scanning period exceeds the preamble transmission period.

Control example 1 flowchart.



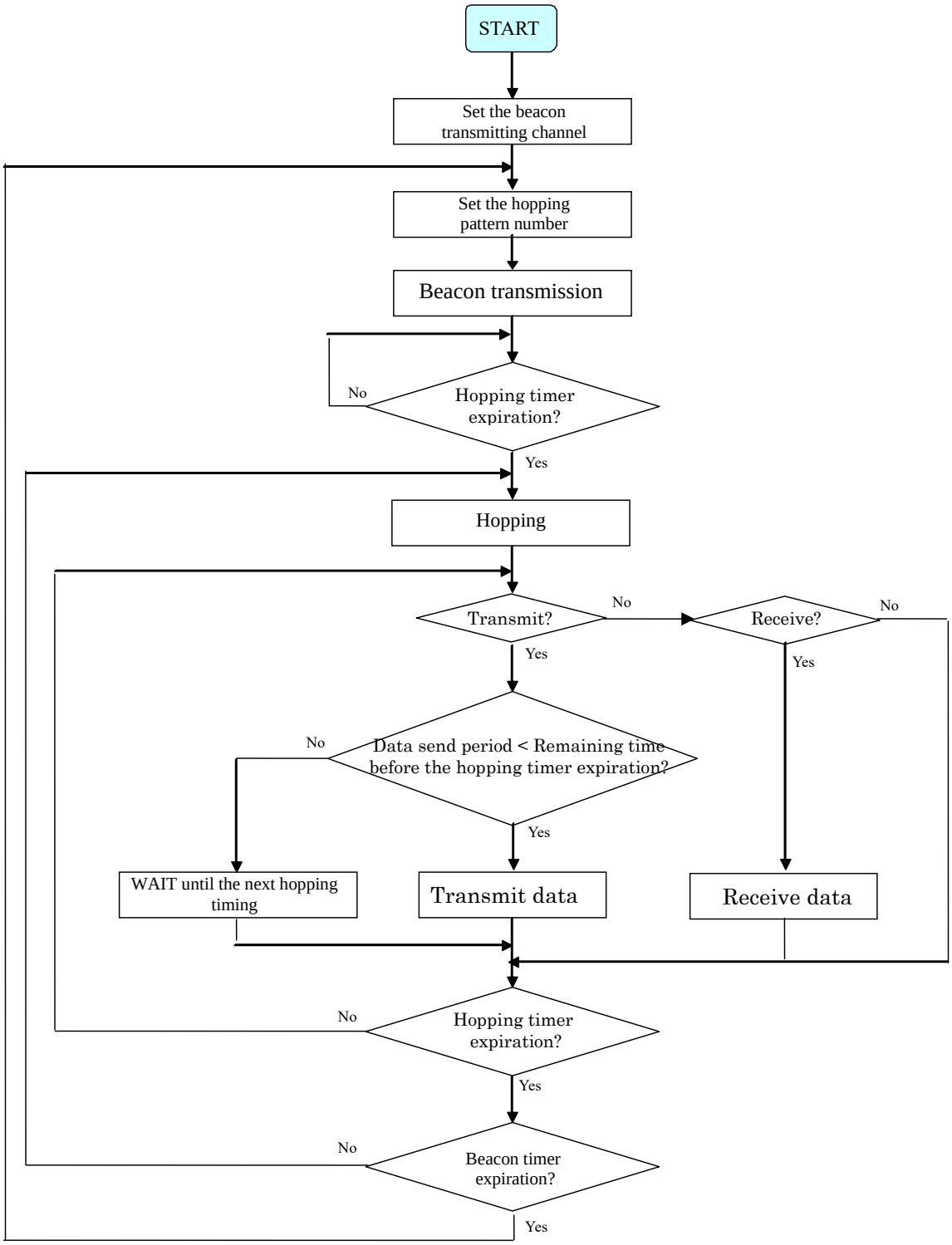
Details of channel scan flow.



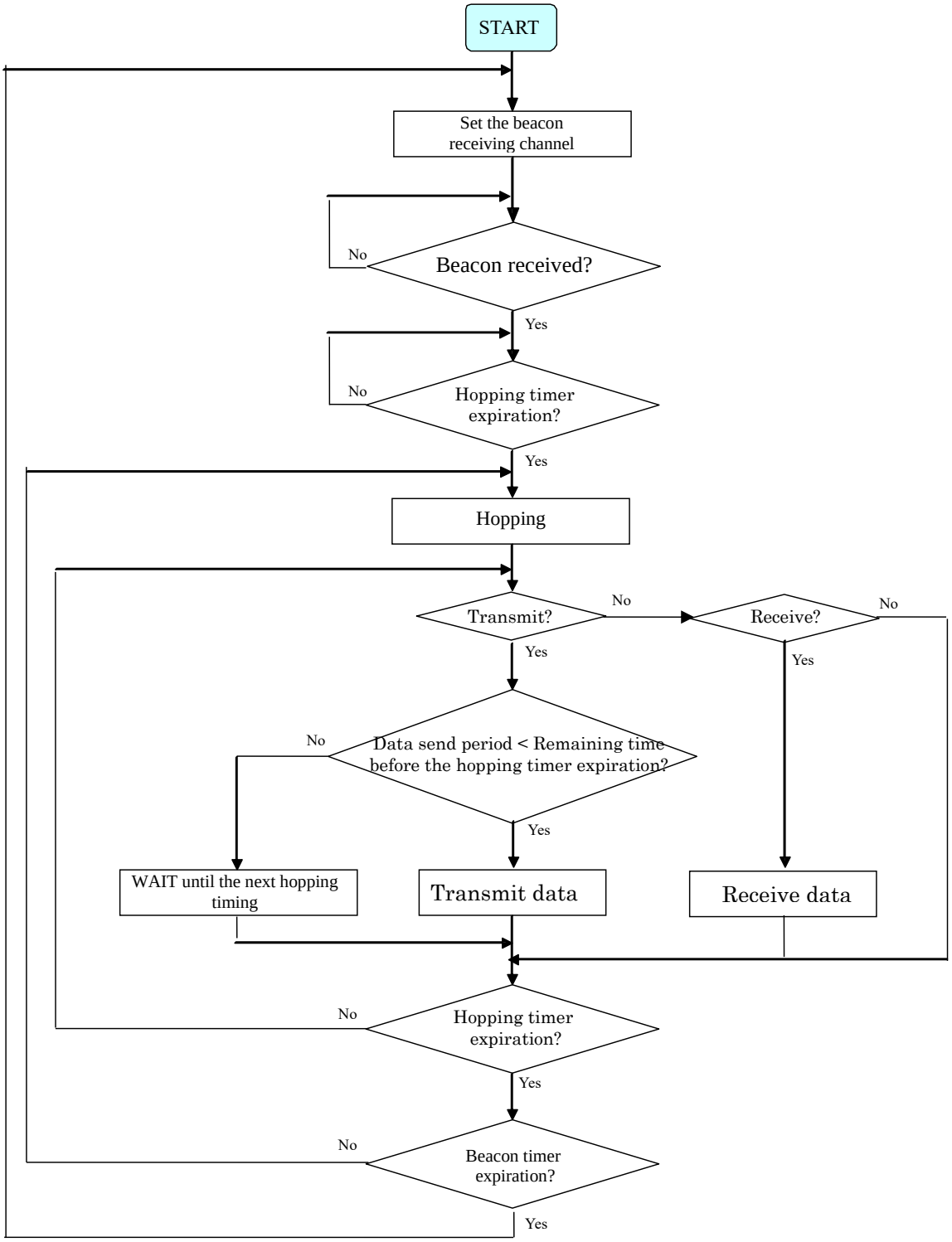
・Control example 2. Use beacon for synchronization and common hopping pattern

In this example, both master and slave nodes use the same synchronized hopping pattern.
The master node periodically transmits a beacon on pre-defined channel. The slave node receives the beacon for synchronizing the hopping pattern.
The slave node waits for a beacon at the pre-defined channel. Once completing synchronization, both nodes hop frequencies according to the common hopping pattern. The hopping interval should be "the beacon interval divided by the number of hopping channels" and required less than 400ms. When transmitting, the transmitting period should be calculated from the data length, making sure to avoid spanning hopping intervals.
When using multiple hopping patterns, adding sequential numbers (pattern number) on each hopping pattern. And the master node attaches the using pattern number into a beacon.
This hopping method is available regardless of the data rate, the diversity search setting, and the number of hopping channels.

[Master node flowchart]



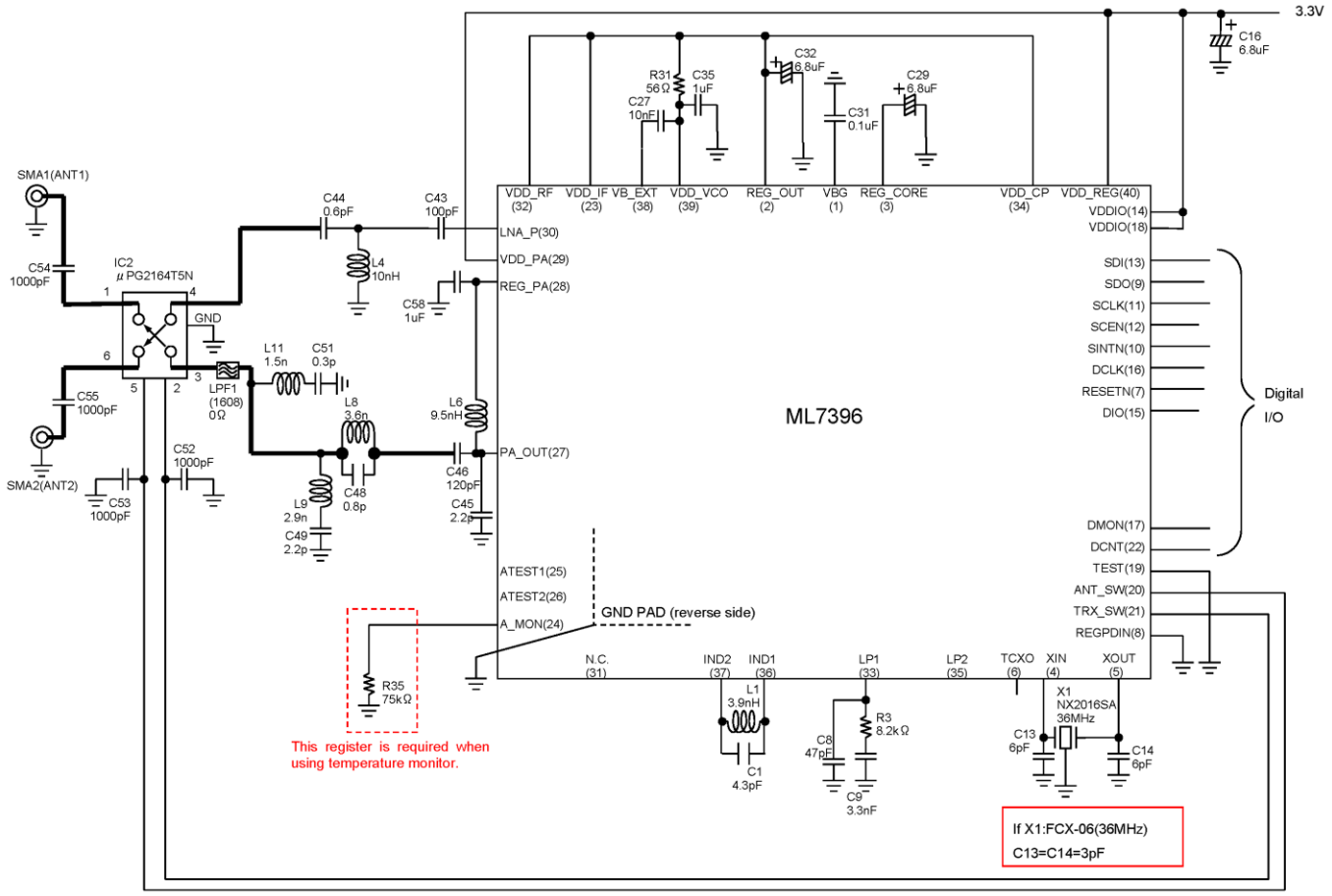
[Slave node flowchart]



■Application Circuit Example

Here is a circuit example for 915MHz/920MHz, 13dBm, and up to 200kbps.
10μF decoupling capacitor should be placed to common 3.3V power pins .
MURATA LQW15series inductors are recommended.

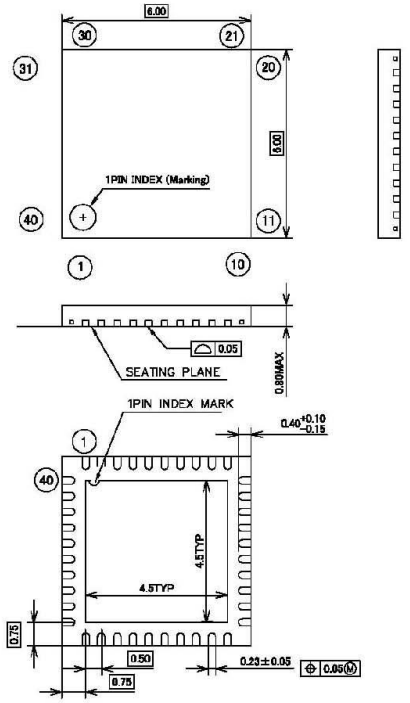
For more details about designing information, please refer to the “ML7396 Family LSIs Hardware Design Manual”.

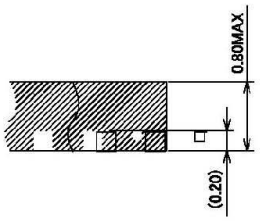


	915MHz	920MHz
L1	4.3nH	3.9nH
C1	3.9pF	4.3pF
LPF1	DEA160915LT-5038A (TDK)	0Ω

■Package Dimensions

P-WQFN40-0606-0.50-63





LAPIS Semiconductor Co.,Ltd.

Package material	EPOXY RESIN
Lead frame material	Cu ALLOY
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 max./0.15 max.
Package weight (g)	0.087 TYP.
Rev. No./Last Revised	4/Oct. 6, 2011

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

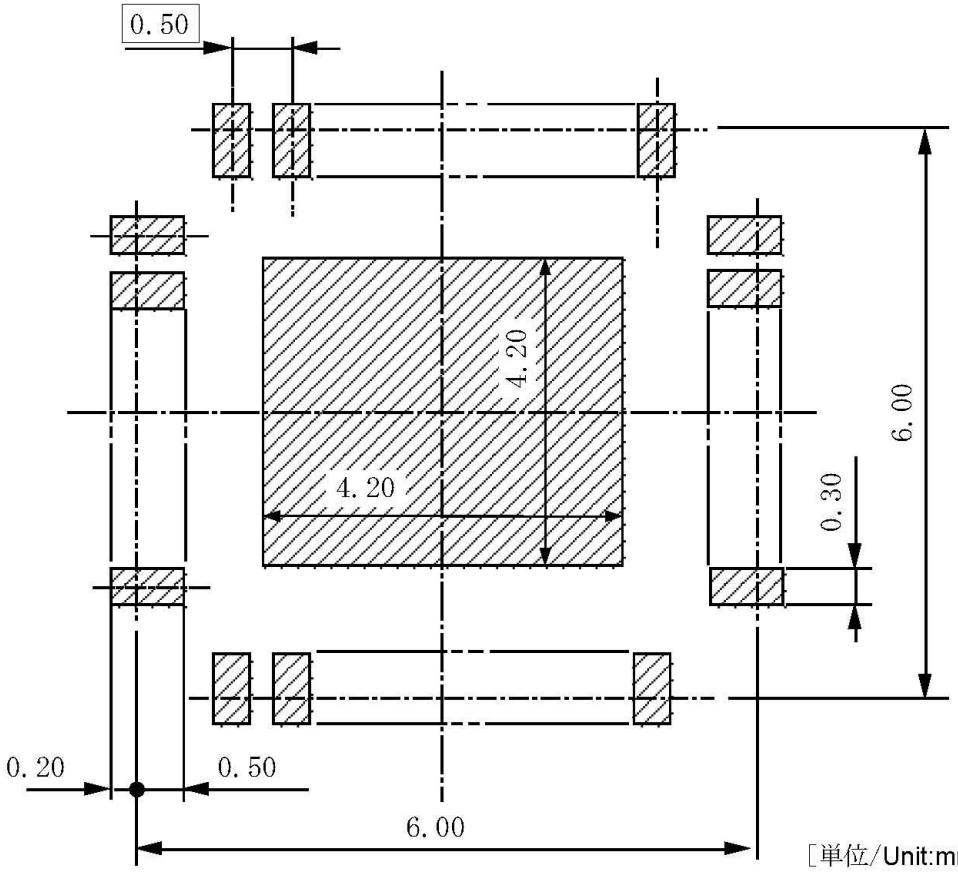
■Footprint Pattern (Recommendation)

P-WQFN40-0606-0.50-63

参考図
for reference

半田付け部端子存在範囲図

Mounting area for package lead soldering to PC boards



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When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.

The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7396A_B_E-01	2013.02.27	–	–	Initial release (Draft version)
FEDL7396A_B_E-02 to -06	–	–	–	These versions are not released.
FEDL7396A_B_E-07	2015.01.15	–	–	Official release (Base on FJDL7396A_B_E-07)
FEDL7396A_B_E_D-08	2016.10.01	1	1	Added ML7396D contents
		2	2	Added current consumption of ML7396D
		11	11	Added current consumption of ML7396D
		14	14	Added RX sensitivity of ML7396D
		28	28	Added description of lower data rate than 50kbps
		99	99	Added ID_CORE of ML7396D
		101	101	Modified description of RX_ON_ADJ2
		107	107	Modified description of RAMP_CNTRL
		126	126	Added ED value calcultaion of ML7396D
FEDL7396A_B_E_D-09	2016.11.29	13	13	Modified spurious emission level
FEDL7396A_B_E_D-10	2019.4.10	2	2	Modified RX current consumption of ML7396E
		7	7	Added description of DMOS pin
		11	11	Modified RX current consumption of ML7396E
		14	14	Modified minimum receiver sensitivity of ML7396E
		99	99	Modified ID_CODE of ML7396E
		124	124	Added note of FEC function
FEDL7396A_B_E_D-11	2023.11.1	1	1	Add application
		1	1	Add Product Name
		229	229	The description of [Note] has been updated.
FEDL7396A_B_E_D-12	2024.1.10	229	229	The description of [Note] has been updated.

Notes

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