Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

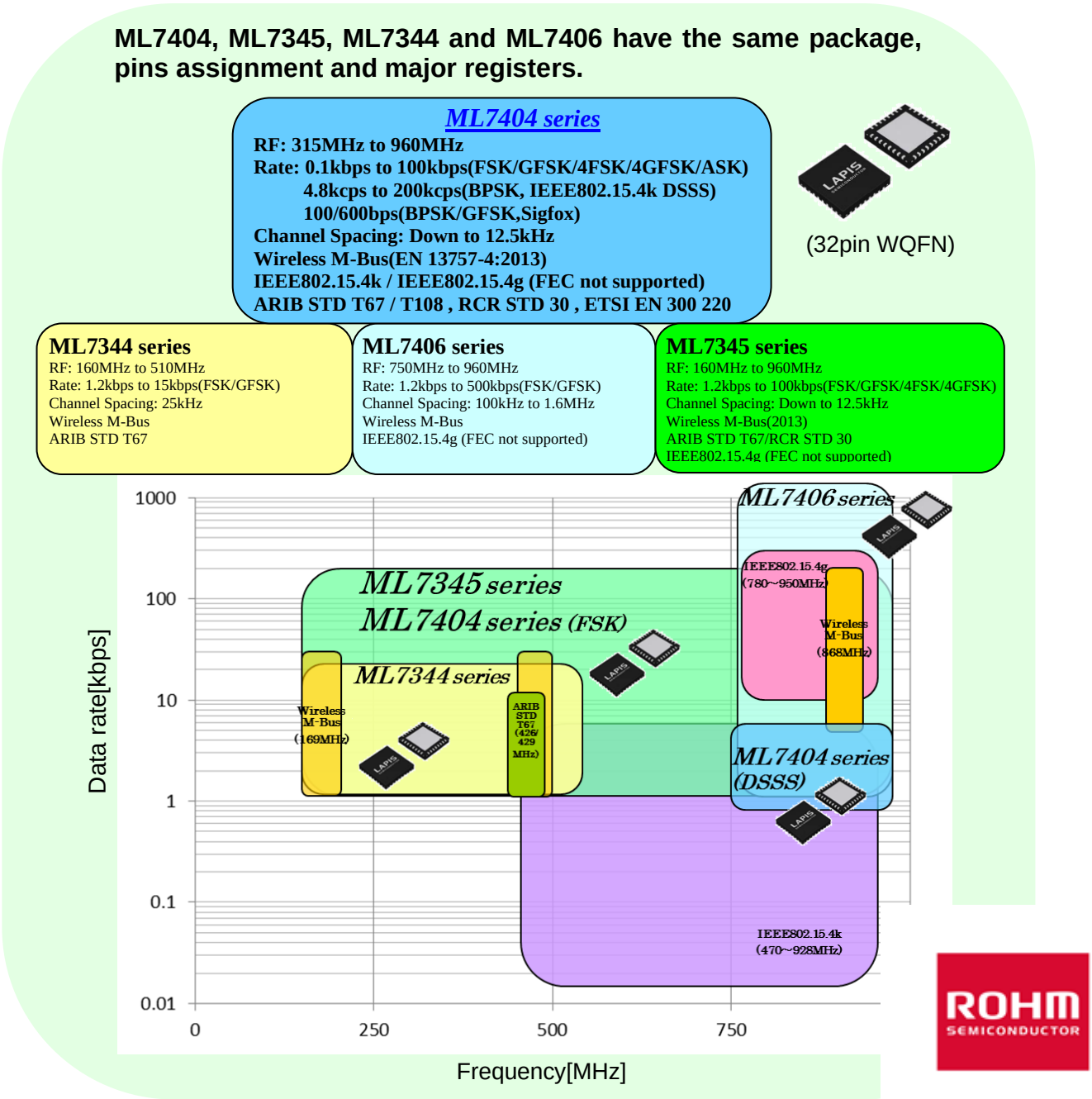
ML7404

Sub-GHz(315MHz to 960MHz) low power transceiver IC for Long range communication

■Overview

The ML7404 is a low power RF transceiver for long range communication in Sub-GHz. The ML7404 includes RF, IF, MODEM, Direct Sequence Spectrum Spreading/Despreading(DSSS), baseband processor, HOST interface. The ML7404 supports RF frequency sets of 315MHz to 960MHz. Built in direct spreading in aaccodance with IEEE802.15.4k standard. And for narrow band wireless communication, it implements programmable channel filters supporting 12.5kHz or wider channel spacing. ML7404 is suitable to F mode (434MHz) , and C/S/T/R mode(868MHz) of Wireless M-Bus in Europe, and to RCR STD-30, ARIB STD-T67, and ARIB STD-T108 in Japan.

ML7404 has the same package, pins assignment and major registers as the ML7344/ML7345/ML7406 family for sharing the board and software between narrow/broadband Sub-GHz applications.



●Product Name ML7404GD

●Application Remote control
Home, Building Security
Sensor Network
Smart Meters
Logistics Tracking
Infrastructure Monitoring
Monitoring system

■Features

- Supported standard
  - ETSI EN 300 220(Europe)
  - EN 13757-4:2013(Wireless M-Bus) S/T/C/R/F Mode
  - RCR STD-30 (III and IV types)
  - ARIB STD-T67
  - ARIB STD-T108
  - Sigfox(Rev 2.E)
- RF frequency: 315MHz to 960MHz supported
- Realized high resolution modulation by using fractional N type PLL direct modulation
- Direct Sequence Spread Spectrum of IEEE802.15.4k (Modulation scheme:BPSK, Chip rate: 4.8kcps to 200kcps)
- Modulation:BPSK, 4GFSK/4GMSK, GFSK/GMSK, FSK/MSK (MSK is FSK at modulation index = 0.5)
- Data transmission rate: 0.1kbps to 100kbps (Modulation scheme:FSK or BPSK for Sigfox)
- Data encoding/decoding by HW: NRZ, Manchester, 3-out-of-6
- Data Whitening by HW
- Programmable channel filters
- Programmable frequency deviation function
- TX/RX data inverse function
- On-chip 36MHz oscillator circuit
- TCXO (36MHz) direct input supported
- Programmable oscillator's load capacitance
- On-chip low power RC oscillator to generate low speed clock
- Low speed clock adjustment function
- Frequency fine tuning function (using fractional N type PLL)
- Synchronous serial peripheral interface (SPI)
- On-chip TX PA (Max. 17dBm)
- TX power tuning function (±0.2dB)
- TX power automatic ramping control (Ramp control time: Max. 57ms)
- External TX PA control function
- RSSI indicator and threshold judgment function
- High speed carrier checking function
- AFC function (IF frequency automatic adjustment by Fractional N type PLL adjustment)
- Antenna diversity function (for FSK mode)
- Automatic Wake-up, auto SLEEP function (external RTC input or internal RC oscillator selectable)
- General purpose timer (2ch)
- Test pattern generator (PN9, CW, 01 pattern, ALL "1", ALL "0" output)
- Packet mode function
  - Wireless M-Bus packet format (Format A/B)
  - General purpose packet format (Format C/D)
  - Max. 255bytes (Format A/B), 2047bytes (Format C/D) packet length
  - TX FIFO (64bytes), RX FIFO (64bytes)
  - RX Preamble pattern detection (Max. 4bytes)
  - Automatic TX preamble length generation (Max. length 16383bytes)
  - SyncWord setting function (Max. 4bytes × 2 type)
  - Program CRC function (CRC32/CRC16/CRC8 selectable, fully programmable polynomial)
  - Wireless M-Bus field checking function (C-field/M-field/A-field can be detected automatically)
    (Note) Proprietary packet format is possible depending on setting

- Supply voltage
  - •FSK mode
    1.8V to 3.6V (TX power 1mW setting)
    2.1V to 3.6V (TX power 10mW setting)
    2.6V to 3.6V (TX power 20mW setting)
  - •BPSK mode
    2.6V to 3.6V (TX power 10mW setting)

- Operational temperature -40°C to 85°C (guaranteed operation)
  -30°C to 75°C (guaranteed RF characteristics)
- Current consumption

Deep sleep mode	0.1μA
Sleep mode 1	0.45μA (registers retained)
Sleep mode 2	1.2μA (Registers and FIFO retained, On-chip RC oscillator, WUT operation)
Idle mode	1.0mA
TX	
20mW	45mA (FSK mode)
10mW	34mA (DSSS mode)
RX	16mA (receiving data in DSSS mode, operating at 18MHz in DSSS cuircuit)

- Package
  32 pins WQFN (5mm × 5mm) P-WQFN32-0505-0.50
  Lead free, RoHS compliance

■Description Convention

1) Numbers description
'0xnn' indicates hexa decimal. '0bnn' indicates binary.

Example: 0x11= 17(decimal), 0b11= 3(decimal)

2) Registers description
[<register name>: B<Bank No> <register address>] register

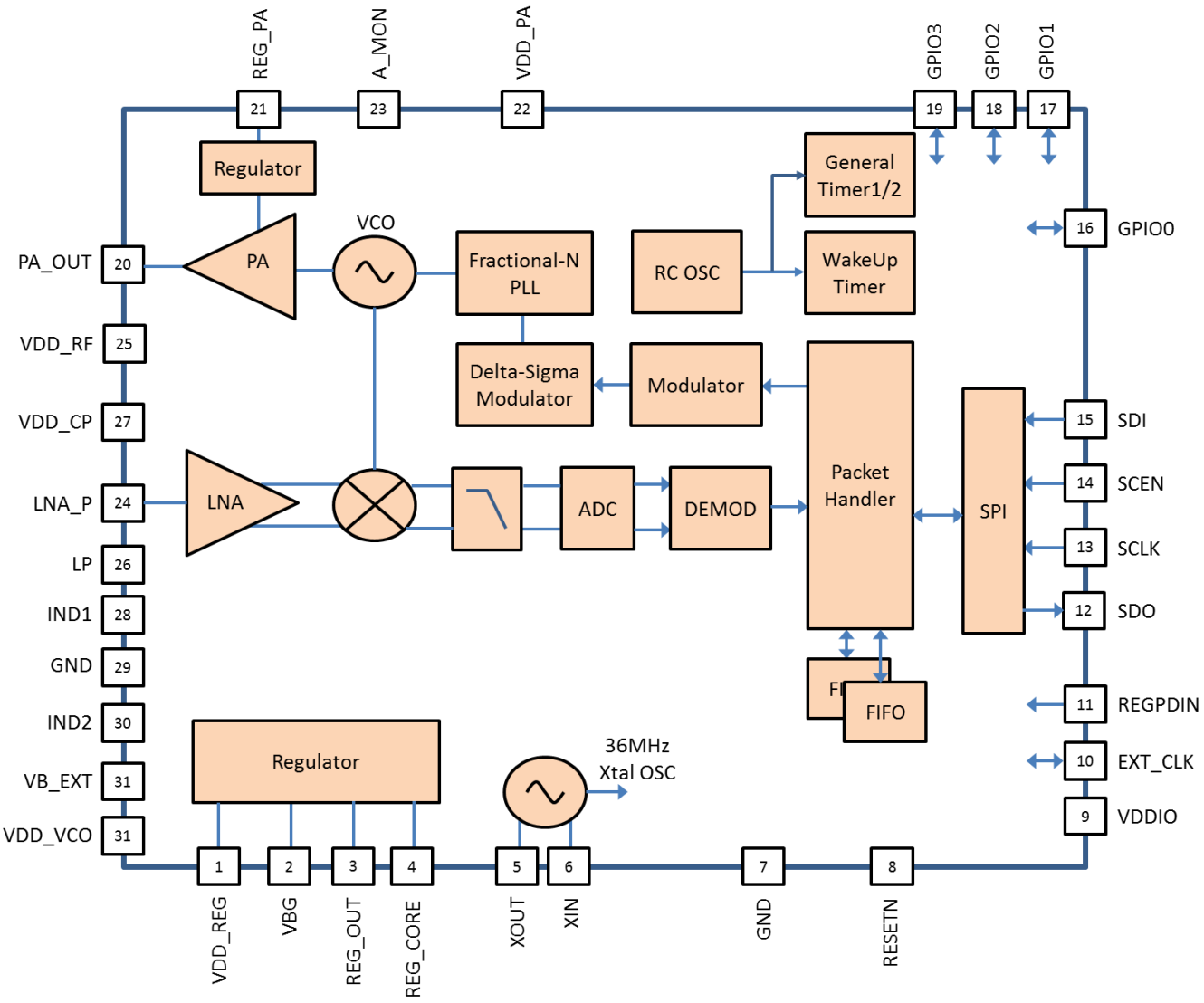
Example: [RF_STATUS: B0 0x0B] register
Register name: RF_STATUS
Bank No: 0
Register address: 0x0B

3) Bir name description
<bit name> ([<register name>: B<Bank No> <register address>(<bit location>)])

Example: **SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])**
Bit name: SET_TRX
Register name: RF_STATUS
Bank No: 0
Register address: 0x0B
Bit location: bit3 to bit0

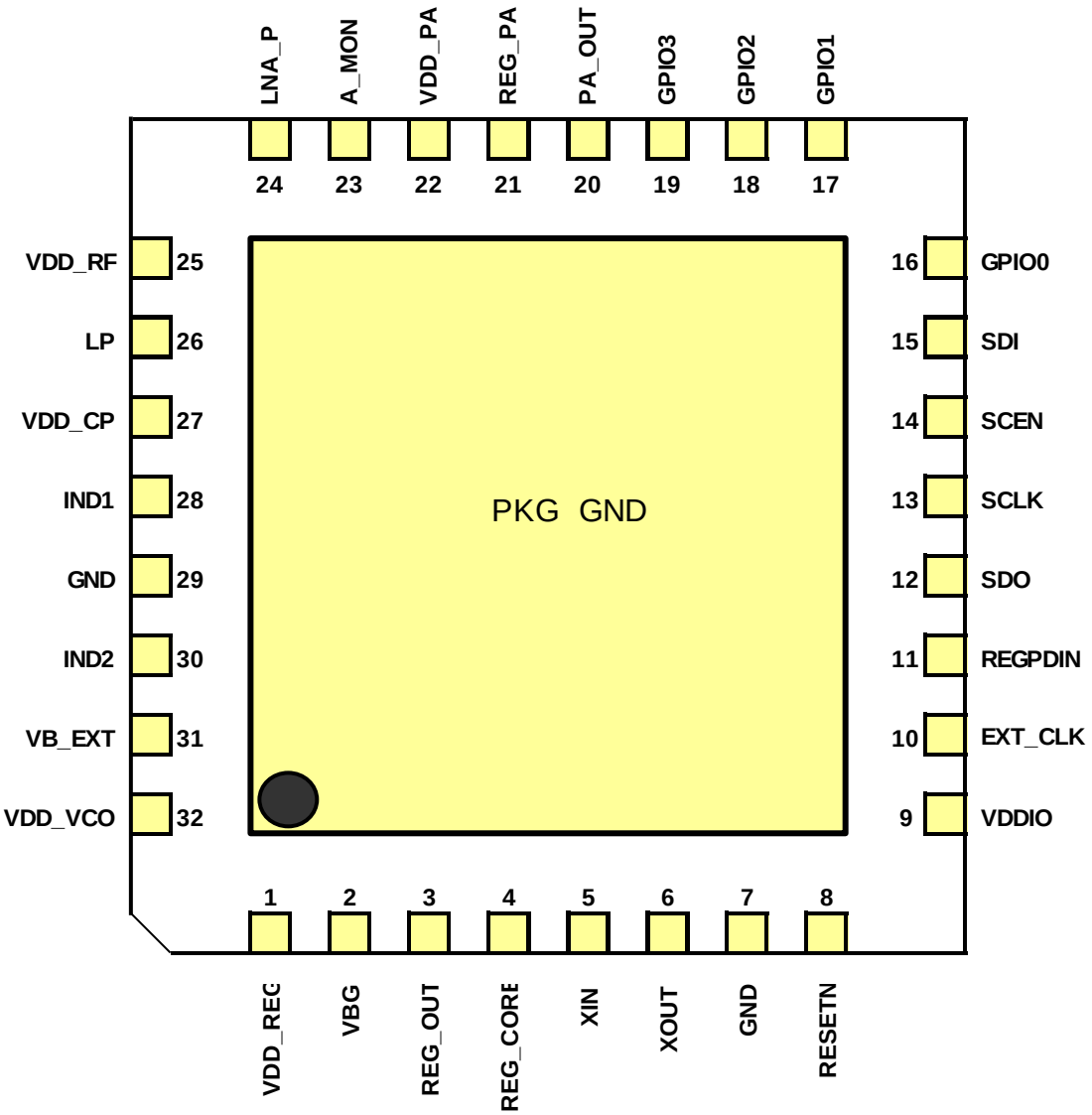
4) In this document
"TX" stands for transmittion.
"RX" stands for reception.

■Block Diagram



■PIN Configuration

32 pins WQFN



NOTE: GND pad in the middle of the LSI is reverse side (name:reversed side GND)

■PIN Definitions

Definiion of Symbols

I/O			Reset state			Active Level		
I	:	Digital input	I	:	Digital Input	H	:	High Level
O	:	Digital output	O	:	Digital Ouput	L	:	Low Level
IS	:	Shmidt Trigger input	Hi-Z	:	High-Impedance	OD	:	Open Drain
IO	:	Digital input/output				P	:	Positive Edge
IA	:	Analog input				N	:	Negative Edge
OA	:	Analog output 1						
OAH	:	Analog output 2						
IOA	:	Analog input/output						
IRF	:	RF input						
ORF	:	RF output						
VDDIO	:	I/O power supply						
VDDRF	:	RF power supply						
GND	:	Ground						

●RF and Analog Pins

Pin	Pin name	Reset state	I/O	Active Level	Function
20	PA_OUT	O	ORF	−	RF antenna output
23	A_MON	Hi-Z	IOA	−	Test pin (*1)
24	LNA_P	I	IA	−	RF antenna input
26	LP	−	IOA	−	Pin for loop filter
28	IND1	−	IOA	−	Pin for VCO tankl inductor
30	IND2	−	IOA	−	Pin for VCO tank inductor
31	VB_EXT	−	IOA	−	Pin for smothing capacitor for internal bias

*1 This pin is used for test of analog circuit in LAPIS semiconductor.

●SPI Interface Pins

Pin	Pin name	Reset state	I/O	Active Level	Function
12	SDO	Hi-Z	O	H or L or OD	SPI data output or DCLK (*1) (Note) Open Drain output is selected in reset state. In case of using SDO as CMOS output, it needs to set SDO_OD([SPI_EXT_PA_CTRL: B0 0x53(7)]) to 0b0 before SPI read access.
13	SCLK	Hi-Z	IS	P or N	SPI clock input
14	SCEN	Hi-Z	IS	L	SPI chip enable L: enable H: disable
15	SDI	Hi-Z	I	H or L	SPI data input or DIO (*1)

*1 Please refer to the “DIO function”.

●Regulator Pins

Pin	Pin name	Reset state	I/O	Active Level	Function
2	VBG	−	OAH	−	Pin for decouppling capacitor
3	REG_OUT	−	OAH	−	Requlator1 ouput (typ. 1.5V)
4	REG_CORE	−	OA	−	Requlator2 ouput (typ. 1.5V)
11	REGPDIN	I	I	H	Power down control pin for regulator Fix to “L” for nomal use. “H” is for deep sleep mode.
21	REG_PA	−	OAH	−	Regulator output for PA block

●Miscellaneous Pins

Pin	Pin name	Reset state	I/O	Active Level	Function
5	XIN N.C.(*1)	I −	IA −	P or N −	36MHz crystal pin1 (Note) In case of TCXO, it must be open.
6	XOUT TCXO(*1)	−	OA	P or N	36MHz crystal pin 2 or TCXO input
8	RESETN	I	IS	L	Reset L: Hardware reset enable (Forcing reset state) H: Normal operation (Note) LSI is initialized when this pin is set to low level. Please set this pin as low level in case of deep sleep mode.
10	EXT_CLK	Hi-Z	IO	-	Digital I/O (*2) Reset state: External PA control signal output.
16	GPIO0	Hi-Z	IO	H or L or OD	Digital GPIO (*3) Reset state: interrupt indication signal output
17	GPIO1	Hi-Z	IO	H or L or OD	Digital GPIO (*4) Reset state: clock output
18	GPIO2	Hi-Z	IO	H or L or OD	Digital GPIO (*5) Reset state: Antenna diversity selection control signal
19	GPIO3	Hi-Z	IO	H or L or OD	Digital GPIO (*6) Reset state: TX – RX selection signal control

*1 In case of using TCXO, set TCXO_EN([CLK_SET2: B0 0x03(6)]) = 0b1. Please make sure only one of the register TCXO_EN, XTAL_EN([CLK_SET2: B0 0x03(4)]) is set to 0b1.
*2 Please refer to [EXTCLK_CTR: B0 0x52] register.
*3 Please refer to [GPIO0_CTRL: B0 0x4E] register.
*4 Please refer to [GPIO1_CTRL: B0 0x4F] register.
*5 Please refer to [GPIO2_CTRL: B0 0x50] register.
*6 Please refer to [GPIO3_CTRL: B0 0x51] register.

●Power Supply/GND Pins

Pin	Pin name	Reset state	I/O	Active Level	Function
1	VDD_REG	−	VDDIO	−	Power supply pin for Regulator (input voltage: 1.8V to 3.3V)
7	GND	−	GND	−	GND pin
9	VDDIO	−	VDDIO	−	Power supply for digital I/O (input voltage: 1.8 to 3.6V)
22	VDD_PA	−	VDDIO	−	Power supply for PA block (input voltage: 18 to 3.6V, depending on TX mode)
25	VDD_RF	−	VDDRF	−	Power supply for RF blocks (REG_OUT is connected, typ. 1.5V)
27	VDD_CP	−	VDDRF	−	Power supply for charge pump (REG_OUT is connected, typ. 1.5V)
29	GND	−	GND	−	GND pin for VCO
32	VDD_VCO	−	VDDRF	−	Power supply for VCO (REG_OUT is connected, typ. 1.5V)

●Unused Pins Treatment

Unused pins treatment are as follows:

Unused pins treatment

Pin name	Pins number	Recommended treatment
N.C.	5	Open
EXT_CLK	10	Open
GPIO0	16	Open
GPIO1	17	Open
GPIO2	18	Open
GPIO3	19	Open
A_MON	23	GND

(Note)

1) If input pins are high-impedance state and leave open, excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.
2) Upon reset, GPIO1 pin is CLK_OUT function. If this function is not used, the clock must to be disabled by setting 0b000 to GPIO1_IO_CFG[2:0] ([GPIO1_CTRL: B0 0x4F (2-0)]). If this pin is left open while outputing clock signal, it may affect RX sensitivity.

■Electrical Characteristics

●Absolute Maximum Rating

Ta = -40˚C to +85˚C and GND = 0V is the typical conditoin if not defined specific condition.

item	symbol	condition	Rating	Unit
I/O Power supply	V_{DDIO}	−	-0.3 to +4.6	V
RF Power supply	V_{DDRF}	−	-0.3 to +2.0	V
RF input power	P_{RFI}	Antenna input in RX	0	dBm
RF output Voltage	V_{RFO}	PA_OUT pin	-0.3 to +4.6	V
Voltage on Analog Pins 1	V_A	−	-0.3 to +2.0	V
Voltage on Analog Pins 2	V_{AH}	−	-1.0 to +4.6	V
Voltage on Digital Pins	V_D	−	-0.3 to +4.6	V
Digital Input Current	I_{DI}	−	-10 to +10	mA
Digital Output Current	I_{DO}	−	-8 to +8	mA
Power Dissipation	Pd	Ta = +25˚C	1.2	W
Storage Temperature	Tstg	−	-55 to +150	˚C

●Recommended Operation Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply (I/O)	VDDIO	VDDIO pin and VDD_REG pin (*1)	1.8 (*3)	3.3	3.6	V
Power Supply (PA)	VDDPA	VDD_PA pin TX power 1mW setting	1.8	3.3	3.6	V
		VDD_PA pin TX Power 10mW setting	2.1	3.3	3.6	V
		VDD_PA pin TX Power 20mW setting	2.6	3.3	3.6	V
Operational Temperature	Ta	−	-40	+25	+85	˚C
Digital Input Rising Time	TIR	Digital Input pins (*1)	−	−	20	ns
Digital Input Falling Time	TIF	Digital Input pins (*1)	−	−	20	ns
Digital Output Load	CDL	All Digital Output pins	−	−	20	pF
Master clock frequency (XIN/XOUT pin)	FMCK1	−	-	36	-	MHz
Master Clock Accuracy (*2)	ACMCK1	FSK mode	-20	−	+20	ppm
	ACMCK2	DSSS mode	-5	−	+5	ppm
X'tal equivalent serial resistance	ESR	−	−	−	80	ohm
TCXO Input Voltage	VTCXO	DC Cutoff TCXO Optionis selected	0.8	−	1.5	Vpp
SPI Clock Input Frequency	FSCLK	SCLK pin	0.032	2	16	MHz
SPI Clock Input Duty Cycle Ratio	DSCLK	SCLK pin	45	50	55	%
RF Frequency	FRF	−	315	−	510	MHz
			685	−	960	MHz

*1 In the pin description, I or Is are specified as the I/O.

*2 Indicating frequency deviation during TX-RX operation. In order to support various standards, please apply the frequency accuracy for each standard to meet the requirements.

Specification	Required accuracy
RCR STD-30 type III	±10 ppm
RCR STD-30 type IV	±4 ppm
ARIB STD T-108	±20 ppm
Wireless M-Bus F mode	±16 ppm
IEEE802.15.4k	±2.5 ppm

*3 In case of TX, the value is specified by minimum value of V_{DDPA}.

(Note) Below typical values are not taking individual LSI variations into consideration.

●Power Consumption

The following values are defined when master clock frequency = 36MHz(Typ.)

Item	Symbol	Condition	Min	Typ (*2)	Max	Unit
Power Consumption (*1)	IDD_DSLP	Deep Sleep mode (Not retaining registers, all function halt)	−	0.1	14	μA
	IDD_SLP1	Sleep mode 1 (*3)	−	0.45	55	μA
	IDD_SLP2	Sleep mode 2 (*3)	−	1.2	56	μA
	IDD_IDLE	Idle state (*4) (*9)	−	1.0	1.2	mA
	IDD_RX	RF RX state (*4) (*9) (ChipRate=200kcps)	−	29	-	mA
		RF RX state (*5) (*9) (ChipRate=200kcps)	−	16	-	mA
		RF RX state (*6) (*9) (ChipRate=100kcps)	−	30	−	mA
		RF RX state (*7) (*9) (ChipRate=100kcps)	−	17	−	mA
		RF RX state (*8) (*9)	−	13.5	-	mA
	IDD_TX10	RF TX state (10mW) (*4) (*9)	−	34	-	mA
	IDD_TX20	RF TX state (20mW) (*8) (*9)	−	45	-	mA
	IDD_XTAL	X'tal osillator cirtcuit only	−	0.3	0.4	mA

*1 Power Consumption is sum of current consumption of all power supply pins.
*2 Typical value is centre value under condition of VDDIO = 3.3V, 25˚C.
*3 The definition of each sleep state is shown in following table.

State	Register	FIFO	RC Osc. (32kHz)	Low clock timer
Sleep mode 1	Retain	Retain RX only	OFF	-
Sleep mode 2	Retain	Retain RX only	ON	ON

*4 The current value in LSI under the condition of DSSS mode (chip rate: 200kcps, RF Frequency: 920MHz, DSSS receiving circuit operation clock: 18MHz, being waiting for data), LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, and using TCXO.
*5 The current value in LSI under the condition of DSSS mode (chip rate: 200kcps, RF Frequency: 920MHz, DSSS receiving circuit operation clock: 18MHz, being receiving data), LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, and using TCXO.
*6 The current value in LSI under the condition of DSSS mode (chip rate: 100kcps, RF Frequency: 920MHz, DSSS receiving circuit operation clock: 9MHz, being waiting for data), LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, and using TCXO.
*7 The current value in LSI under the condition of DSSS mode (chip rate: 100kcps, RF Frequency: 920MHz, DSSS receiving circuit operation clock: 9MHz, being receiving data), LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, and using TCXO.
*8 The value under confition of FSK mode(data rate is 100kbps, RF Frequency is 920MHz), LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, and using TCXO.
*9 When using X'tal osillator, I_{DD_XTAL} is added to power comsumption except for Deep Sleep mode(I_{DD_DSLP}) and Sleep mode(I_{DD_SLP1}/I_{DD_SLP2}).

●DC Characteristics

The following values are defined when master clock frequency = 36MHz(Typ).

Item	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input High	V_{IH1}	Digital Input pins	VDDIO * 0.75	−	VDDIO	V
Voltage Input Low	V_{IL1}	Digital Input pins	0	−	VDDIO * 0.18	V
Schmit Trigger Threshold High Level	V_{T+}	RESETN,SDI, SCLK, SCEN, EXT_CLK, GPIO1, REGPDIN pins	−	1.2	VDDIO * 0.75	V
Schmit Trigger Threshold Low Level	V_{T-}	RESETN,SDI, SCLK, SCEN, EXT_CLK, GPIO1, REGPDIN pins	VDDIO * 0.18	0.8	−	V
Input Leakage Current	I_{IH1}	Digital input pins	-1	−	1	µA
	I_{IL1}	Digital input pins	-1	−	1	µA
Tri-state Output Leakage Current	I_{OZH}	Digital input pins	-1	−	1	µA
	I_{OZL}	Digital input pins	-1	−	1	µA
Voltage Output Level H	V_{OH}	IOH = -4mA	VDDIO * 0.78	−	VDDIO	V
Voltage Output Level L	V_{OL}	IOL = 4mA	0	−	0.3	V
Regulator Output Voltage	REG_{MAIN}	REG_CORE pin applicable to all states except SLEEP state	1.5	1.6	1.65	V
	REG_{SUB}	REG_CORE pin Sleep state	1.2	1.5	1.65	V
Pin Capacitance	C_{IN}	Input pins	−	6	−	pF
	C_{OUT}	Output pins	−	9	−	pF
	C_{RFIO}	RF inout pins	−	9	−	pF
	C_{AI}	Analog input pins	−	9	−	pF

●FSK RF Characteristics

Modulated Data Rate : 0.1kbps to 100kbps
Modulation fomats : 2GFSK/2FSK/4GFSK/4FSK
Channel spacing : Down to 12.5kHz

The measurement point is at antenna end specified in the recommended circuits.

[RF Frequency]

Item	Condition	Min	Typ	Max	Unit
RF frequency	LNA_P, PA_OUT pins 1/2 division mode	315	433	510	MHz
	LNA_P, PA_OUT pins non-division	685	868	960	MHz

(Note)
1) Frequency range can be adjusted from 315MHz to 960MHz by changing external components parameters.
2) If channel frequency is similar frequency range of Integral multiple of the master clock, it may not be able to use this mode. Please refer to the “Channel frequency setting” section for detail.

[TX characteristics]

Value is under condition of the master clock frequency = 36MHz (Typ.).

433MHz Band, Ta = -30 to +75°C

Item	Condition		Min	Typ	Max	Unit
TX power	20mW (13dBm) adjustment		10	13	13.8	dBm
	10mW (10dBm) adjustment		7	10	10.8	dBm
	1mW (0dBm) adjustment		-3	0	0.8	dBm
Programmable frequency deviation [Fdev] (*1)			0.025	-	400	kHz
Occupied bandwidth	99% power bandwidth, Pattern:PN9, Data rate:4800bps, 2.4kHz deviation		-	-	8.5	kHz
Adjacent channel power ratio	Data rate: 4800bps, Pattern: PN9, 2.4kHz deviation, ratio in 25kHzoffset ± 8.5kHz band		-	-	-40	dBc
Spurious emission	10dBm TX Data rate: 4800bps, Pattern: PN9, 2.4kHz deviation, 62.5k to 162.5kHz offset integration value		-	-	-26	dBm
	Harmonics (*2) 10dBm CW TX (Note) With LC trap circuit	2^{nd} 3^{rd} <			-36 -30	dBm

*1 Depends on the master clock frequency.
*2 The value under confition of RF Frequency is 433MHz.

920MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
TX power	20mW (13dBm) Max setting	12	-	-	dBm
Programmable frequency deviation [Fdev] (*1)		0.025	-	400	kHz
Occupied bandwidth	99% power bandwidth, Pattern:PN9, Data rate:100kbps, 50kHz deviation	-	-	400	kHz
Adjacent channel power ratio	Data rate:100kbps, 50kHz deviation, Pattern:PN9 20mW (13dBm) adjustment , +/-1CH, Bandwidth: 200kHz	-	-46	-28	dBm
Spurious emission	Harmonics (2^{nd}/ 3^{rd}) 13dBm CW TX (Note) With LC trap circuit	-	-35	-30	dBm

*1 Depends on the master clock frequency.

685MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
TX power	20mW (13dBm)	-	13	-	dBm
Adjacent channel power ratio	Data rate:100kbps, 50kHz deviation, Pattern:PN9 20mW (13dBm) adjustment , +/-1CH, Bandwidth: 200kHz	-	-46	-	dBm
Spurious emission	Harmonics (2^{nd}/ 3^{rd}) 13dBm CW TX (Note) With LC trap circuit	-	-35	-	dBm

[RX characteristics]

Value is under condition of the master clock frequency = 36MHz (Typ.).

433MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
Sensitivity	2.4kbps mode BER<1%, GFSK, ±2.4kHz deviation	-	-119.5	-112	dBm
	4.8kbps mode BER<1%, GFSK, ±2.4kHz deviation	-	-116.5	-109	dBm
Adjacent channel rejection ratio	12.5kHz spacing, Ta = 25°C, 4.8kbps mode Undesire: PN9	30	33	-	dB
	25kHz spacing, Ta = 25°C, 9.6kbps mode Undesire: PN9	30	33	-	dB
Blocking (*2)	2MHz offset, Ta = 25°C, 4.8kbps mode Undesire: CW	-	69	-	dB
	10MHz offset, Ta = 25°C, 4.8kbps mode Undesire: CW	-	77	-	dB
	-IF frequency *2 [Hz] offset (image frequency), Ta = 25°C After IQ adjustment	30	50	-	dB
Minimum Power detection level (ED value)	RFmin in RSSI characteristics diagram (*1) 4.8kbps, Channel filter band = 10kHz setting	-	-120	-105	dBm
RSSI dynamic range	Dynamic range in RSSI characteristics diagram (*1)	70	80	-	dB
Spurious emission		-	-	-54	dBm

*1 The following diagram shows the RSSI characteristics.
*2 UD ratio by ARIB STD-T67/RCR STD-30 method

920MHz Band, Ta = -30 to +75°C

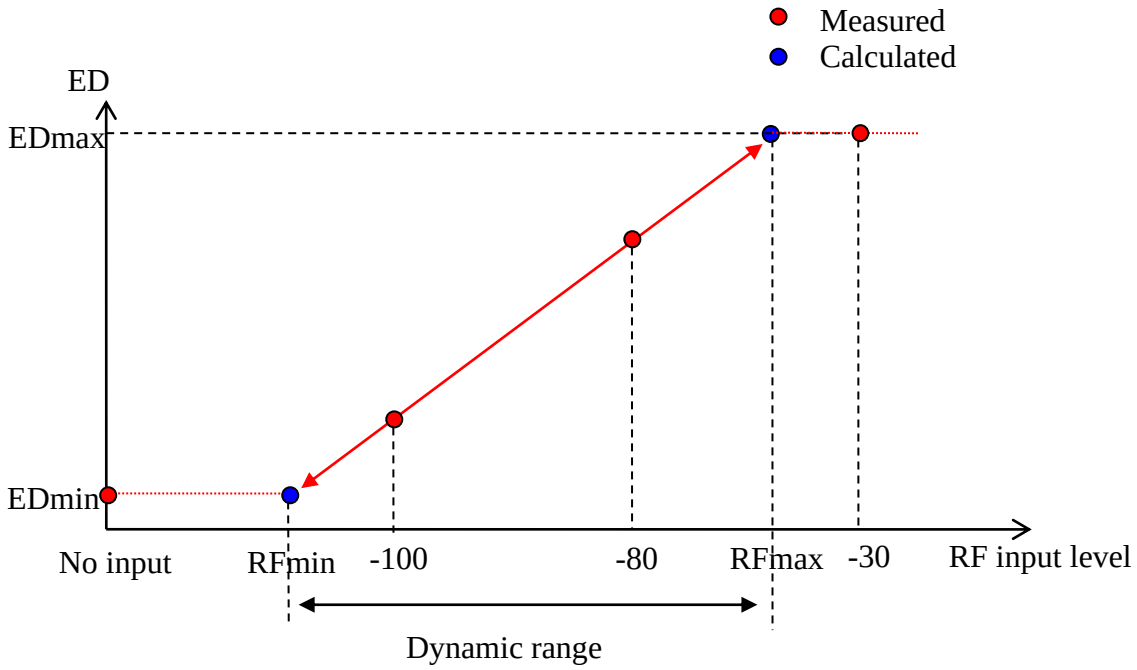
Item	Condition	Min	Typ	Max	Unit
Sensitivity	38.4kbps mode BER<1%, GFSK, ±19.2kHz deviation	-	-109	-100	dBm
	100kbps mode BER<1%, GFSK, ±50kHz deviation		-106	-97	dBm
Adjacent channel rejection ratio (*1)	400kHz spacing, Ta = 25°C, 100kbps mode Undesire: CW	20	37	-	dB
Blocking (*1)	2MHz offset, Ta = 25°C, 100kbps mode Undesire: CW	-	52	-	dB
	10MHz offset, Ta = 25°C, 100kbps mode Undesire: CW	-	62	-	dB
Minimum Power detection level (ED value)	RFmin in RSSI characteristics diagram (*2) 100kbps, Channel filter band = 200kHz setting		-105	-96	dBm
RSSI dynamic range	Dynamic range in RSSI characteristics diagram (*2)	55	65	-	dB
Spurious emission		-	-	-54	dBm

*1 UD ratio by ARIB STD-T67/RCR STD-30 method
*2 The following diagram shows the RSSI characteristics.

685MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
Sensitivity	100kbps mode BER<1%, GFSK, ±50kHz deviation	-	-106	-	dBm
Adjacent channel rejection ratio (*1)	400kHz spacing, Ta = 25°C, 100kbps mode Undesire: CW	-	37	-	dB
Blocking (*1)	2MHz offset, Ta = 25°C, 100kbps mode Undesire: CW	-	52	-	dB
	10MHz offset, Ta = 25°C, 100kbps mode Undesire: CW	-	62	-	dB
Minimum Power detection level (ED value)	RFmin in RSSI characteristics diagram (*2) 100kbps, Channel filter band = 200kHz setting		-105	-	dBm
RSSI dynamic range	Dynamic range in RSSI characteristics diagram (*2)	-	65	-	dB
Spurious emission		-	-	-54	dBm

*1 UD ratio by ARIB STD-T67/RCR STD-30 method
*2 The following diagram shows the RSSI characteristics.


Measured
Calculated
ED
EDmax
EDmin
No input
RFmin
-100
-80
RFmax
-30
RF input level
Dynamic range

●DSSS RF Characteristics

[Spread Spectrum]

Chip Rate	:	4.8 to 200kcps
Spreading Facter(SF)	:	8/16/32/64
Moduration mode	:	BPSK
FEC coding rate	:	1/2

[Sigfox]

Chip Rate	:	100bps
Moduration mode	:	BPSK

The measurement point is at antenna end specified in the recommended circuits.

[RF Frequency]

Item	Condition	Min	Typ	Max	Unit
RF frequency	LNA_P, PA_OUT pins 1/2 division mode	315	433	510	MHz
	LNA_P, PA_OUT pins non-division	685	868	960	MHz

(Note)

1) Frequency range can be adjusted from 315MHz to 960MHz by changing external components parameters.
2) If channel frequency is similar frequency range of Integral multiple of the master clock, it may not be able to use this mode. Please refer to the “Channel frequency setting” section for detail.
3) When using DSSS mode(100/200kcps) in Japan under a recommendation operation condition, RF frequency range is 921-924.6MHz. Please refer to design guide for other chip rate.

[TX characteristics]

Value is under condition of the master clock frequency = 36MHz (Typ.).

920MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
TX power	10mW (10dBm) adjustment	6	10	12	dBm
	1mW (0dBm) adjustment	-4	0	4	dBm
Spreading Facter (SF)		8	-	64	-
Ocupation band width		-	-	400	kHz

(Note)

1. When using DSSS mode(100/200kcps) in Japan under a recommendation operation condition, it is necessary to operate this mode by 5 unit channels. In addition, please refer to design guide for other chip rate.
2. Please be sure to use TCXO when using DSSS mode.

685MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
TX power	10mW (10dBm) adjustment	-	10	-	dBm

(Note)

1. Please be sure to use TCXO when using DSSS mode.

[RX characteristics]

Value is under condition of the master clock frequency = 36MHz (Typ.).

920MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
Sensitivity	Chip rate=200kcps, SF=64 PER<1%, FEC cording rate=1/2	-	-121	-	dBm
	Chip rate=100kcps, SF=64 PER<1%, FEC cording rate=1/2	-	-121	-	dBm
Adjacent channel rejection ratio	Chip rate=200kcps, SF=64, 400kHz spacing, Ta = 25°C	20	37	-	dB
Blocking (*1)	2MHz offset, Ta = 25°C, Chip rate=200kcps	-	52	-	dB
	10MHz offset, Ta = 25°C, Chip rate=200kcps	-	62	-	dB

*1 UD ratio by ARIB STD-T67/RCR STD-30 method

(Note)
1. Please be sure to use TCXO when using DSSS mode.

685MHz Band, Ta = -30 to +75°C

Item	Condition	Min	Typ	Max	Unit
Sensitivity	Chip rate=200kcps, SF=64 PER<1%, FEC cording rate=1/2	-	-121	-	dBm
	Chip rate=100kcps, SF=64 PER<1%, FEC cording rate=1/2	-	-121	-	dBm
Blocking (*1)	2MHz offset, Ta = 25°C, Chip rate=200kcps	-	52	-	dB
	10MHz offset, Ta = 25°C, Chip rate=200kcps	-	62	-	dB

*1 UD ratio by ARIB STD-T67/RCR STD-30 method

(Note)
1. Please be sure to use TCXO when using DSSS mode.

●RC Oscillator Characteristics

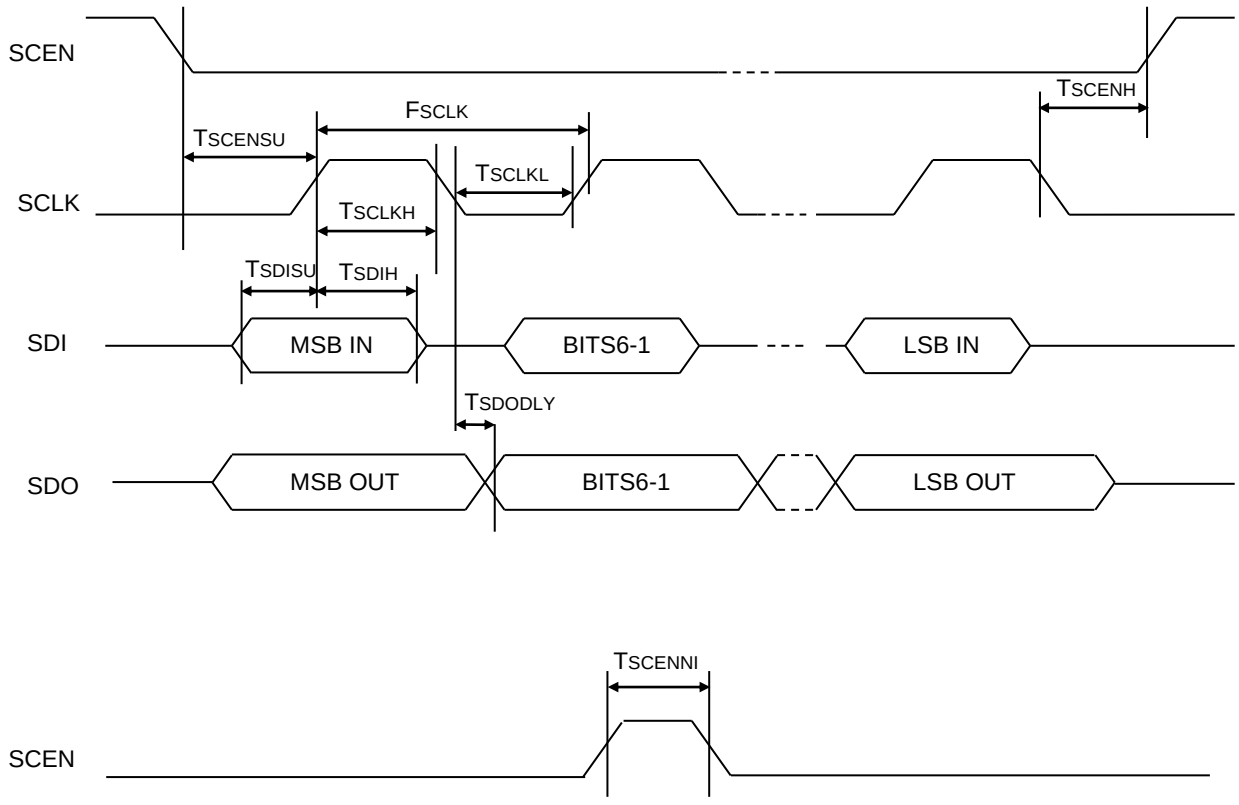
ML7404 has on-chip low speed RC oscillator.
For details, please refer to the “LSI State Transition Control/SLEEP setting” section.

Item	Symbol	Condition	Min	Typ	Max	Unit
RCOSC oscillation frequency	FRCOSC	After triming	27	32	38	kHz
RCOSC stable time	TRCOSC		−	−	100	ms

●SPI Interface Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL = 20pF	0.032	2	16	MHz
SCEN input setup time	TSCENSU		30	−	−	ns
SCEN input hold time	TSCENH		30	−	−	ns
SCLK high pulse width	TSCLKH		31	−	−	ns
SCLK low pulse width	TSCLKL		31	−	−	ns
SDI input setup time	TSDISU		5	−	−	ns
SDI input hold time	TSDIH		15	−	−	ns
SCEN negate period	TSCENNI		200	−	−	ns
SDO output delay time	TSDODLY		0	−	25	ns

(Note)
All measurement condition for the timings are V_{DDIO} * 20% level and V_{DDIO} * 80% level.

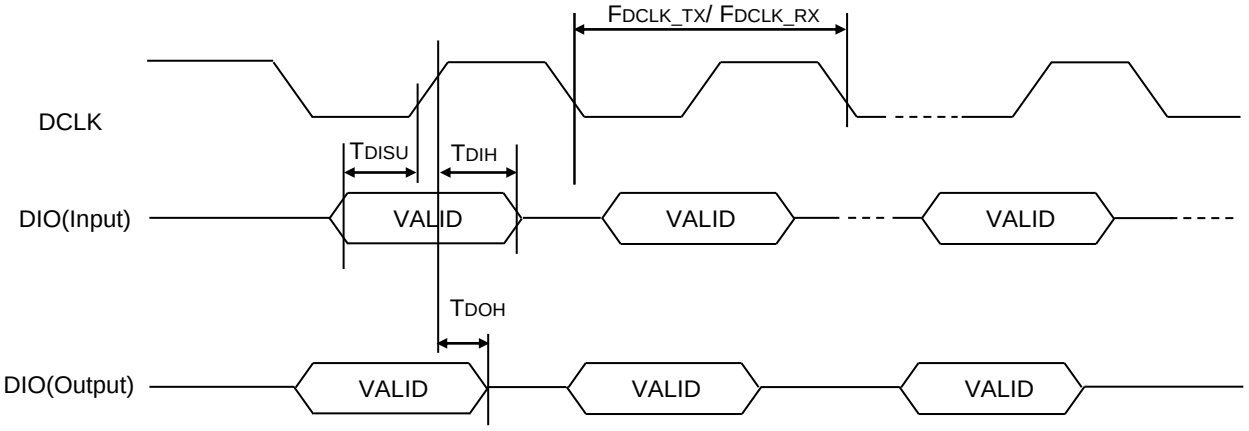


●DIO Interface Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
DIO input setup time	T_{DISU}	Load capacitance CL = 20pF	1	−	−	µs
DIO input hold time	T_{DIH}		0	−	−	ns
DIO output hold time	T_{DOH}		20	−	−	ns
DCLK frequency accuracy (*1) (TX)	F_{DCLK_TX}		-clock frequency deviation	−	+clock frequency deviation	kHz
DCLK frequency accuracy (*2) (RX)	F_{DCLK_RX}		-30	−	+30	%
DCLK output duty ratio (TX)	D_{DCLK_TX}		45	−	55	%
DCLKoutput duty ratio (RX)	D_{DCLK_RX}		30	−	70	%

*1 If there is no decimal point generated in the TX data rate setting caluclation, (see [TX_RATE_H: B1 0x02]), master clock frequency deviation is max.and min.of TX DCLK frequency.
*2 Max.and min.of RX DCLK frequency indicates jitter of recovered clock from RX signal upon synchronization.

(Note)
All timing measurement conditions are V_{DDIO} * 20% and V_{DDIO} * 80%.



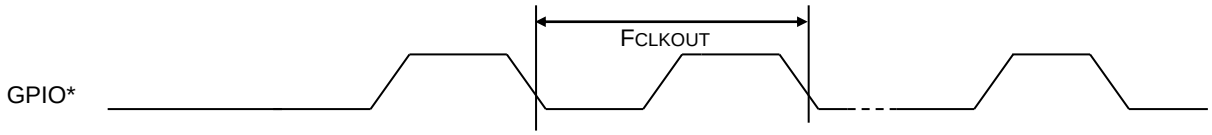
●Clock Output Characteristics

ML7404 has clock output function. Clock output can be controlled by DMON_SET([MON_CTRL: B0 0x4D(3-0)]) and [GPIOn_CTRL: B0 0x4E-0x51] registers (n = 0 to 3). Upon reset, clock is output through GPIO1 pin.

Item	Symbol	Condition		Min	Typ	Max	Unit
Clock output frequency	FCLKOUT	Load capacitance CL = 20pF		0.0088	3	36(*2)	MHz
Clock output duty ratio (*1)	DCLKOUT		12MHz	33	−	67	%
			All conditions except above	47	50	53	%

*1 Duty cycle is High:Low = 1:2 , only when 12MHz is used. Please refer to [CLK_OUT: B1 0x01] register.
*2 Frequency when LOW_RATE_EN([CLK_SET2: 0x03(0)] = 0b0.

(Note)
All timing measurement conditions are V_{DDIO} * 20% and V_{DDIO} * 80%.

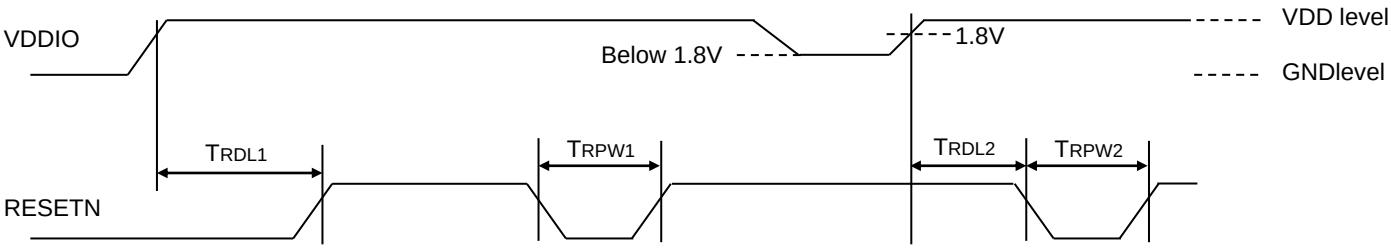


●Reset Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETN release delay time (power on period)	TRDL1	All power pins After Power On	0.5	−	−	ms
RESETN pulse period (start-up from VDDIO = 0V)	TRPW1		0.5	−	−	ns
RESETN pulse period 2(*1) (start-up from VDDIO≠0V)	TRPW2		0.5	−	−	ms
RESETN input delay time	TRDL2	After VDDIO > 1.8V	1	−	−	µs

*1 When starting from VDDIO≠0V, a pulse must be sent to VRESETN after DDIO exceeds 1.8V.

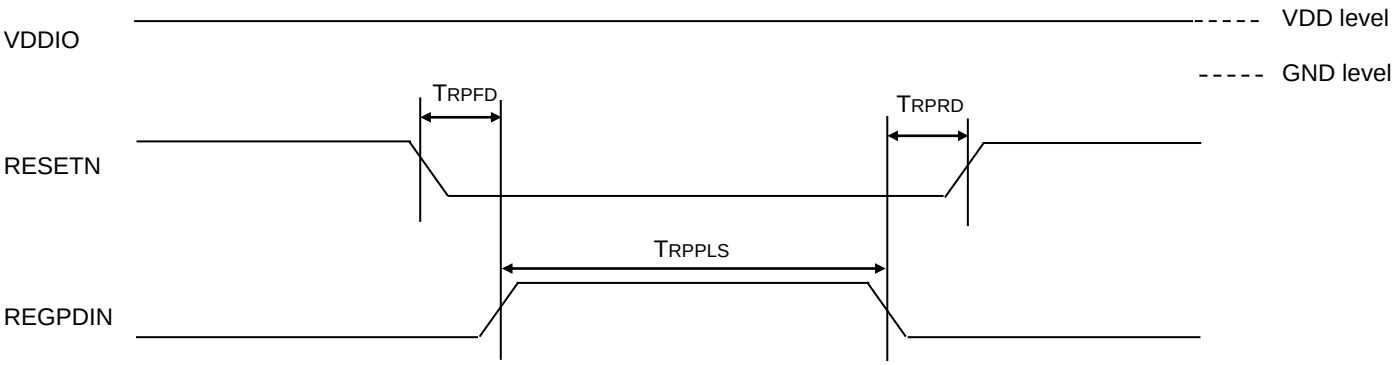
(Note)
All timing measurement conditions are V_{DDIO} * 20% level and V_{DDIO} * 80% level.



●Deep Sleep Mode Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
REGPDIN rising edge delay time	TRPFD	VDDIO = "H"	0	−	−	µs
REGPDIN assert time	TRPPLS	VDDIO = "H"	0.3	−	−	ms
REGPDIN release delay time	TRPRD	VDDIO = "H"	0.5	−	−	ms

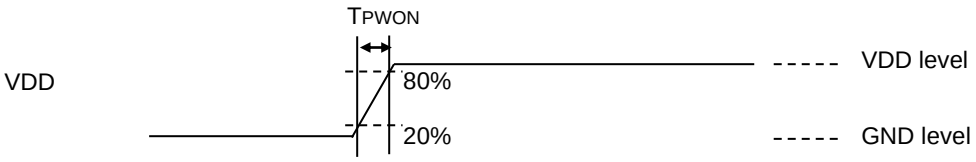
(Note)
All timing measurement conditions are VDDIO * 20% and VDDIO * 80%.



●Power-On Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Power-ontime	TPWON	Power on state (all power pins)	−	−	5	ms

(Note)
All timing measurement conditions are VDDIO * 20% and VDDIO * 80%.



■Functional Description

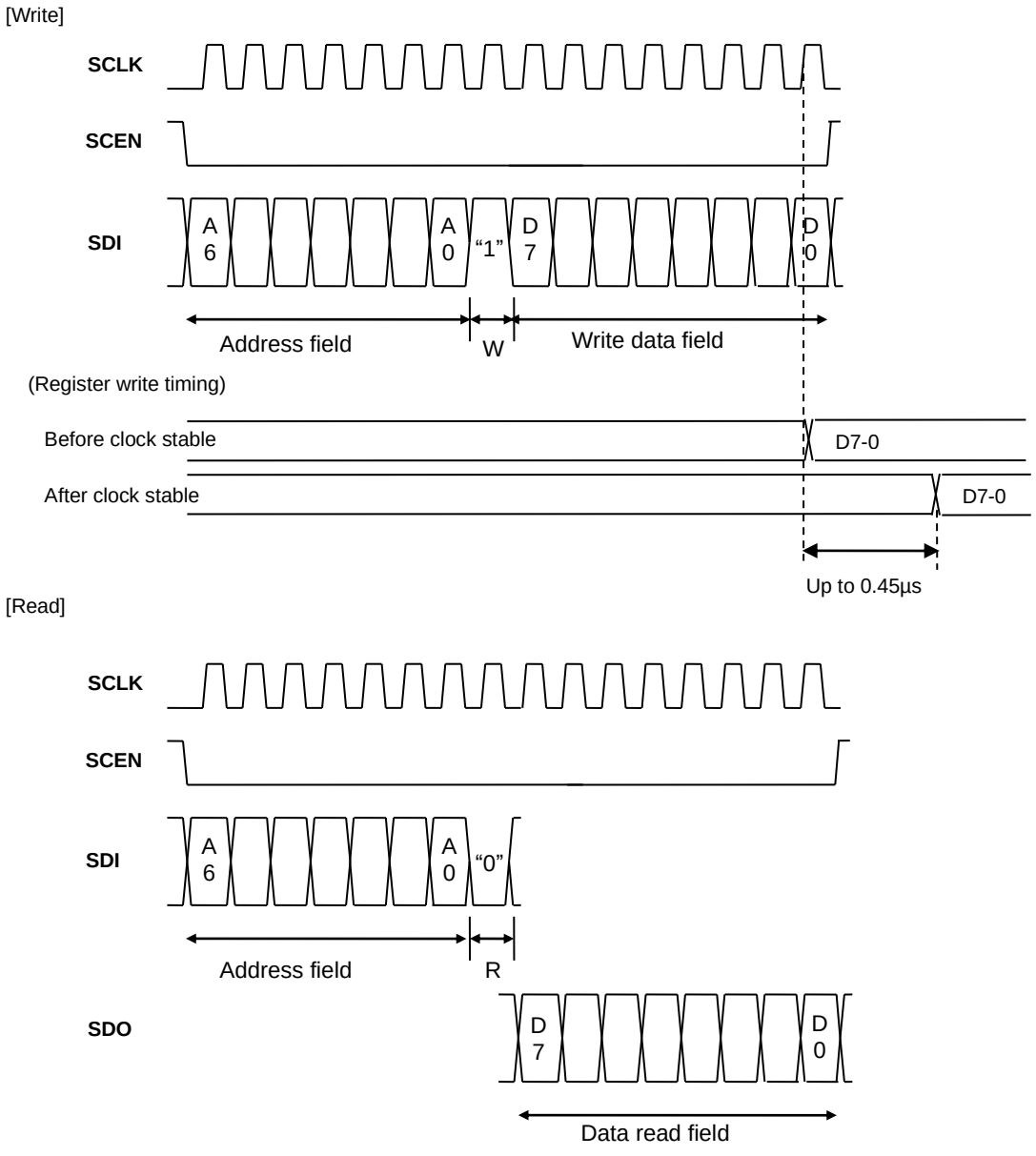
●Host Interface

○Serial Peripheral Interface (SPI)

ML7404 has a SPI which supports slave mode. Host MCU can read/write to the ML7404 registers and on-chip FIFO using MCU clock. Single access mode and burst access mode are also supported.

[Single access mode timing chart]

In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 data. During write operation, if setting SCEN line to “H”, the data will not be stored into register. For more details of SCEN invert perios, please refer to the “SPI interface characteristics”. After the internal clock is stabilized, the data will be written into the register in synchronization with the internal clcok.



[Burst access mode timing chart]

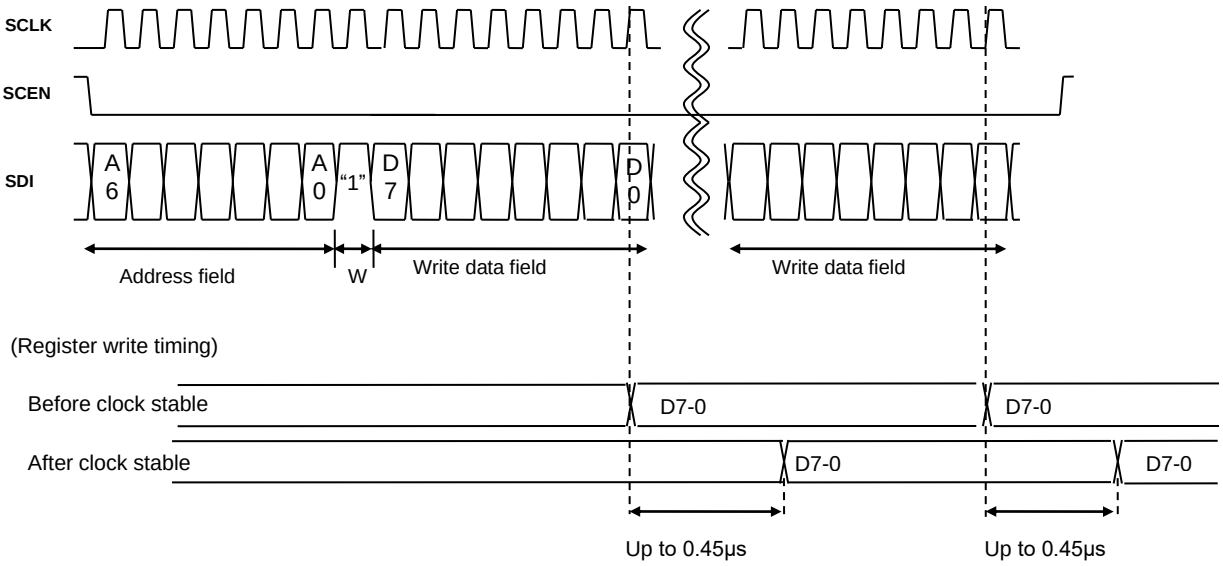
By maintaining SCEN line as “L”, Burst access mode will be active. By setting SCEN line to “H”, exiting from the burst access mode. During burst access mode, address will be automatically incremented.

When SCEN line becomes “H” before Clock for D0 is input, data transaction will be aborted.

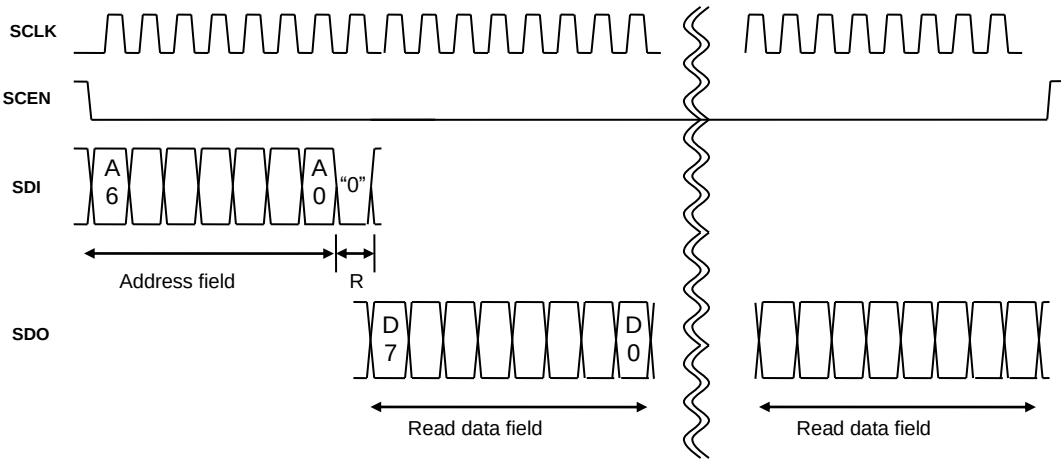
(Note)

If destination is [WR_TX_FIFO: B0 0x7C] or [RD_FIFO: B0 0x7F] register, address will not be incremented. And continuous FIFO access is possible.

[Write]



[Read]



●LSI State Transition Control

○LSI state transition instruction

State can be controlled from MCU by setting registers below.

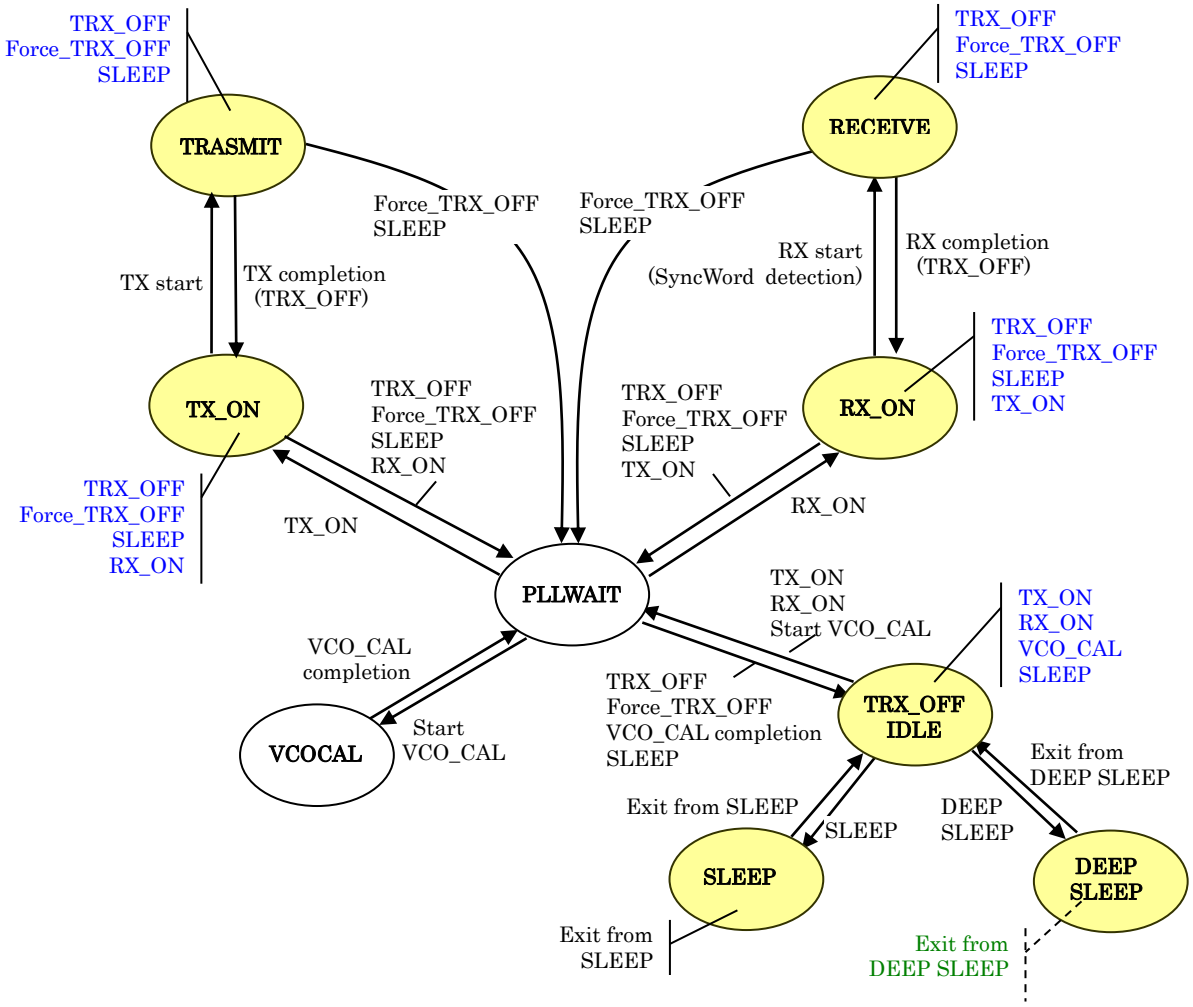
State transition command	Instruction
TX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b1001
RX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b0110
TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b1000
Force_TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0b0011
SLEEP	SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1
VCO_CAL	VCO_CAL_START([VCO_CAL_START: B0 0x6F(0)]) = 0b1

State can be changed without command from MCU. If one of the following condition is met, state is changed automatically according to the following table. In order to enable these functions, the following registers must be programmed.

Function	Control bit name
Automatic TXON after FIFO write completion (AUTO_TX)	AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)])
Automatic TXON during FIFO wrtie (FAST_TX)	FAST_TX_EN([RF_STATUS_CTRL: B0 0x0A(5)])
RF state setting after packet transmission completion	TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)])
RF state setting after packet reception completion	RXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(3-2)])
Automatic RX_ON/TX_ON by Wake-up time	WAKEUP_MODE([SLEEP/WU_SET:B0 0x2D(6)]) WAKEUP_EN([SLEEP/WU_SET:B0 0x2D(4)])
Automatic VCO calibration after exit from SLEEP	AUTO_VCOCAL_EN([VCO_CAL_START: B0 0x6F(4)])
Automatic SLEEP by Timer	WU_DURATION_EN([SLEEP/WU_SET: B0 0x2D(5)])
Automatic SLEEP by high speed carrier checking mode	FAST_DET_MODE_EN([CCA_CTRL:B0 0x39(3)])
Automatic TXON by high speed carrier checking mode	CCADONE_MODE([ED_CTRL:B0 0x41(6)])
Force_TRX_OFF after PLL unlock detection during TX	PLL_LD_EN([PLL_LOCK_DETECT: B1 0x0B(7)])

○State Diagram

Each state transition control is decribed in the follwing state diagram.



[STATE]

DEEP SLEEP	: DEEP SLEEP
SLEEP	: SLEEP
TRX_OFF/IDLE	: IDLE (TX-RX stand-by)
PLL_WAIT	: PLL stand-by
TX_ON	: TX ready (TX data waiting)
TRANSMIT	: TX on-going
RX_ON	: RX stand-by (RX data waiting)
RECEIVE	: RX on-going
VCO_CAL	: VCO calibration

State transition instruction

Pins control

Normal sequence
(state transition)

Command from
Higher layer state

ML7404 Self controlled state transition

LSI state diagram

○SLEEP setting

DEEP_Sleep mode: Powers for all blocks except IO pins are turned off.
Sleep mode: Main regulator and 36MHz oscillation circuits are tured off. But sub-regulator is turned-on.
The following registers can be programmed to control SLEEP state.

Function	Control bit name
Power control	PDN_EN([SLEEP/WU_SET: B0 0x2D(1)])
Wake-up setting	WAKEUP_EN([SLEEP/WU_SET: B0 0x2D(4)])
Wake-up timer clock source setting	WUT_CLK_SOURCE([SLEEP/WU_SET: B0 0x2D(2)])
Internal RC oscillator control	RC32K_EN ([CLK_SET2: B0 0x03(3)])

Setting method and internal state for DEEP_SLEEP and various SLEEP modes are as follows:

SLEEP mode	Setting method	main regulator	Sub regulator	36MHz oscillator	RC oscilator	Low clock timer	TX FIFO
DEEP_SLEEP	RESETN pin = “L” REGPDIN pin = “H”	OFF	OFF	OFF	OFF	OFF	OFF
SLEEP1	[SLEEP/WU_SET: B0 0x2D(5-0)] = 0b00_0111 (*1) [CLK_SET2: B0 0x03(3)] = 0b0	OFF	ON	OFF	OFF	OFF	OFF
SLEEP2	[SLEEP/WU_SET: B0 0x2D(5-0)] = 0b11_0111 (*1) [CLK_SET2: B0 0x03(3)] = 0b1	OFF	ON	OFF	ON	ON	OFF

*1 Please set proper value to [SLEEP/WU_SET: B0 0x2D(3)].

Contents of registers are not kept during DEEP_SLEEP. Contents of registers are kept during SLEEP1 and SLEEP2. However, in SLEEP1 and SLEEP2 mode, contents of TX FIFO are not kept, because power to FIFO is turned off.

○Notes to set RF state

ML7404 is able to change the internal RF state transition autonomously (without commands from MCU) as well as RF state change commands from MCU. (please refer to the "LSI state transition instruction"). If both timing of operation (autonomous state and state change from MCU command) overlapped, unintentional RF state may occur. Timing of autonomous state RF change is described in the following table.
Care must be taken not to overlap the conditions.

Function	RF state change (before→after)	RF state transition timing (not from Host MCU command)	Recommended process
Automatic TX	TRX_OFF/RX_ON →TX_ON	After TX data transfer completion interrut occurs, { value [TX_RATE_H/L: B1 0x02/03)] * 2 / 36}[µs] period.	Write access to [RF_STATUS:B0 0x0B] is possible after RF state transition completion interrupt (INT[3] group1), or move to the state defined by GET_TRX ([RF_STATUS:B0 0x0B(7-4)]).
FAST_TX mode		When FIFO write access exceed trigger level +1, { value [RX_RATE1_H/L:B1 0x04/05] * 5 / 36}[µs] period.	
RF state setting after TX completion	TX_ON→TRX_OFF	After TX completion interrupt (INT[16] group3), { value [TX_RATE_H/L:B1 0x02/03] * 2 / 36} [µs] period	
	TX_ON→RX_ON		
	TX_ON→SLEEP		
RF state setting after RX completion	RX_ON→TRX_OFF	After data RX completion interrupt (INT[8] group2, { value [RX_RATE1_H/L:B1 0x04/05] * 2 / 36}[µs] period	
	RX_ON→TX_ON		
	RX_ON→SLEEP		
Wake-up timer	SLEEP→TX_ON	After wake-up timer completion interrupt (INT[6] group1), 1 clock cycle period defined by WUT_CLK_SET[3:0] ([WUT_CLK_SET:B0 0x2E (3-0)]).	
	SLEEP→RX_ON		
	SLEEP→VCO_CAL →TX_ON	After wake-up timer completion interrupt (INT[6]: group1), before VCO calibration completion interrupt (INT[1] group1).	Write access to [RF_STATUS:B0 0x0B] and BANK2 is possible after VCO calibration completion interrupt (INY[1] group1).
	SLEEP→VCO_CAL →RX_ON		
Continuous operation timer	TX_ON→SLEEP	After continuous operation timer completion, 1 clock cycle period defined by WUT_CLK_SET[3:0] ([WUT_CLK_SET:B0 0x2E (3-0)]).	Write access to [RF_STATUS:B0 0x0B] is possible after RF state transition completion interrupt (INT[3] group1), or move to the state defined by GET_TRX ([RF_STATUS:B0 0x0B(7-4)]).
	RX_ON→SLEEP		
High speed carrier checking	RX_ON→SLEEP	After CCA completion interrupt, duration 6.3[µs].	
PLL unlock detection	TX_ON→TRX_OFF	After PLL unlock detection interrupt (INT[2] group1) occurs, duration 24[µs].(*1)	Write access to [RF_STATUS:B0 0x0B] is possible 24µs(*1) after PLL unlock interrupt (INT[2] group1) detected.

*1 Depends on the ramp-down time setting.

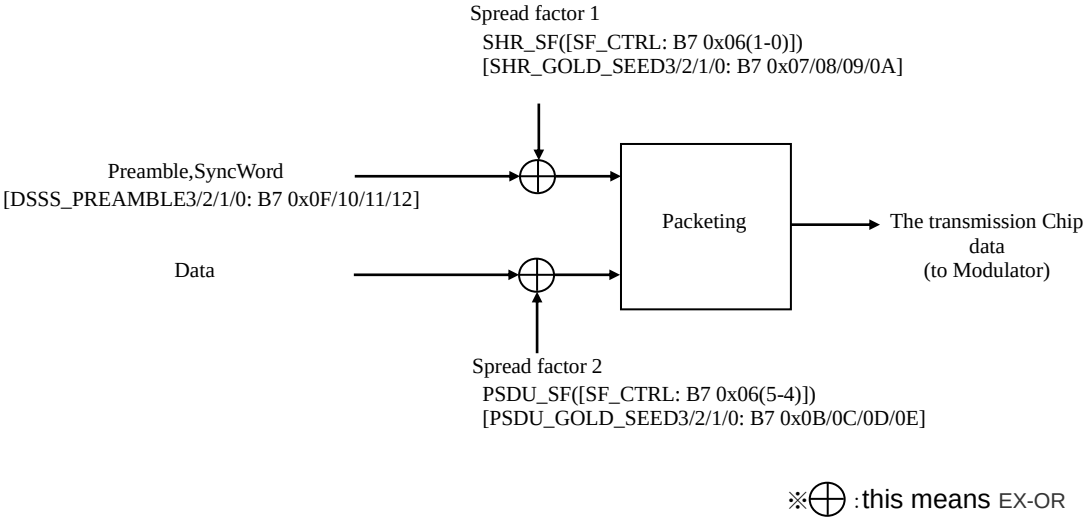
● Spread Spectrum Function

ML7404 supports Direct Sequence Spread Spectrum(DSSS) function in conformity with IEEE802.15.4k. The DSSS function has the characteristic with a noise-resistant, and is superior in interference tolerance, and achieve high-quality data communication. The spreading factor (8/16/32/64) of Spread Spectrum function can be set individually for preamble, SyncWord (SHR) and a data (PSDU). In addition, the spread sequence(generated from a gold sequence) can be set individually for a preamble, SyncWord and a data (PSDU).
The data rate depending on the spreading factor can be culculated by a expression below.

$$\text{Effective Data Rate}[bps] = \frac{ChipRate(\text{Data Rate on Air})[\text{cps}]}{SpreadingFactor}$$

In case of FEC function enabled, it becomes 1/2 of the found effectiveness data rate from an upper expression because an encoding rate is 1/2. In addition, please set a rate on air namely a Chip Rate.on the data rate of “data rate setting function", The configuration of Spread Spectrum function can be set with registers on the table below.

function	Register
DSSS enable setting	DSSS_EN([DSSS_CTRL: B7 0x01(0)])
DSSS preamble setting	DSSS_PR_LEN([DSSS_CTRL: B7 0x01(3)])
DSSS PDSUlength setting	PSDU_SIZE([DSSS_CTRL: B7 0x01(5-4)])
SHRspread factor setting	SHR_SF([SF_CTRL: B7 0x06(1-0)])
PSDU spread factor setting	PSDU_SF([SF_CTRL: B7 0x06(5-4)])
SHR gold sequence setting	[SHR_GOLD_SEED3/2/1/0: B7 0x07/08/09/0A]
PSDU gold sequence setting	[PSDU_GOLD_SEED3/2/1/0: B7 0x0B/0C/0D/0E]
DSSS preamble pattern setting	[DSSS_PREAMBLE3/2/1/0: B7 0x0F/10/11/12]



Spread Spectrum circuit

(Note)

1) ML7404 supports only BPSK modulation if DSSS function is used. Therefore, please set MOD_TYPE([MOD_CTRL: B6 0x01(1-0)]) in 0b01 when you use a spread spectrum function.
2) The chip rate on air can be set in the range of 80 - 200kcps.
3) When the spreading factor (SF)=8 is used, receiving data may fail due to poor frequency estimation accuracy even if the reception level is high. Immediately before using SF=8, be sure to receive data using another SF (16/32/64) and confirm the frequency gap between transmitter and receiver. Packets will be successfully received with SF=8 by correcting the frequency gap.

●Packet Handling Function

○Packet format

ML7404 supports Wireless M-Bus frame FormatA/B/C, and Format D which is non Wireless M-Bus universal format. The following packet handling are supported in FIFO mode or DIO mode

1) Preamble and SyncWord automatic insertion (TX) --- DIO/FIFO mode
2) Preamble and SyncWord automatic detection (RX) --- DIO/FIFO mode
3) Preamble and SyncWord automatic deletion (RX) --- DIO/FIFO mode
4) CRC data insertion (TX) --- FIFO mode
5) CRC check and error notification (RX) --- DIO/FIFO mode

The following table shows control bits relative with the Packet format function.

Function	Control bit name
Packet formatsetting	PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)])
RX extended link layer mode disable	RX_EXTPKT_OFF ([PKT_CTRL1: B0 0x04(3)])
Data area bit order setting	DAT_LF_EN ([PKT_CTRL1: B0 0x04(4)])
Length area bit order setting	LEN_LF_EN ([PKT_CTRL1: B0 0x04(5)])
Extended link layer mode setting	EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])
Length field setting	LENGTH_MODE ([PKT_CTRL2: B0 0x05(0)])

The following table shows packet format list that ML7404 supports.

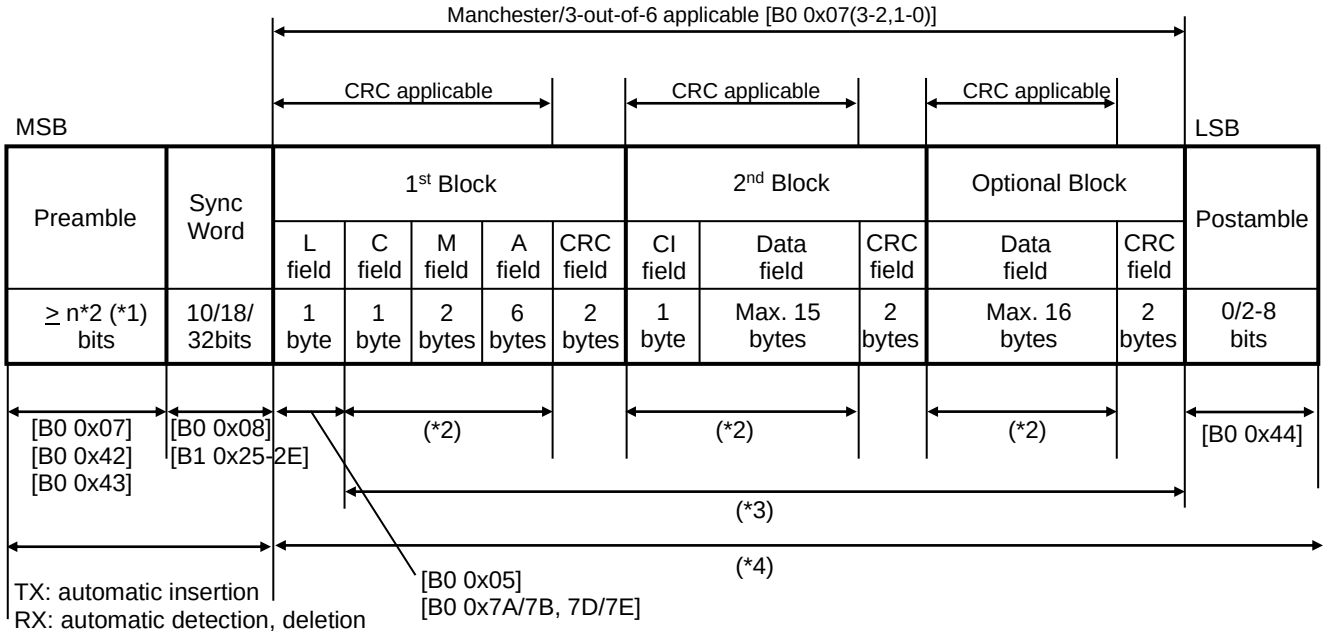
Packet Format	Relationship between the standard	
Format A	Wireless M-Bus Format A	Normal
		Extended Link Layer CI=0x8C
		Extended Link Layer CI=0x8D
		Extended Link Layer CI=0x8E
		Extended Link Layer CI=0x8F
Format B	Wireless M-Bus Format B	Normal
		Extended Link Layer CI=0x8C
		Extended Link Layer CI=0x8D
		Extended Link Layer CI=0x8E
		Extended Link Layer CI=0x8F
Format C	general purpose format1 (with L-field)	
Format D	general purpose format2 (without L-field)	

The detail of each pakect format is as follows.

(1) Format A (Wireless M-Bus)

By setting PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)]) = 0b00, Wireless M-Bus Format A is selected.
Format A consists of 1st Block, 2nd Block and Optional Block(s). Each block has 2bytes of CRC. "L-field" (1st byte of 1st Block) indicates packet length, which includes subsequenct user data bytes from "C-field". However, CRC bytes and postamble are excluded. Depending on "L-field" value, 2nd Block and Optional Block(s) are added.

The following [] indicates register address [bank #, address].



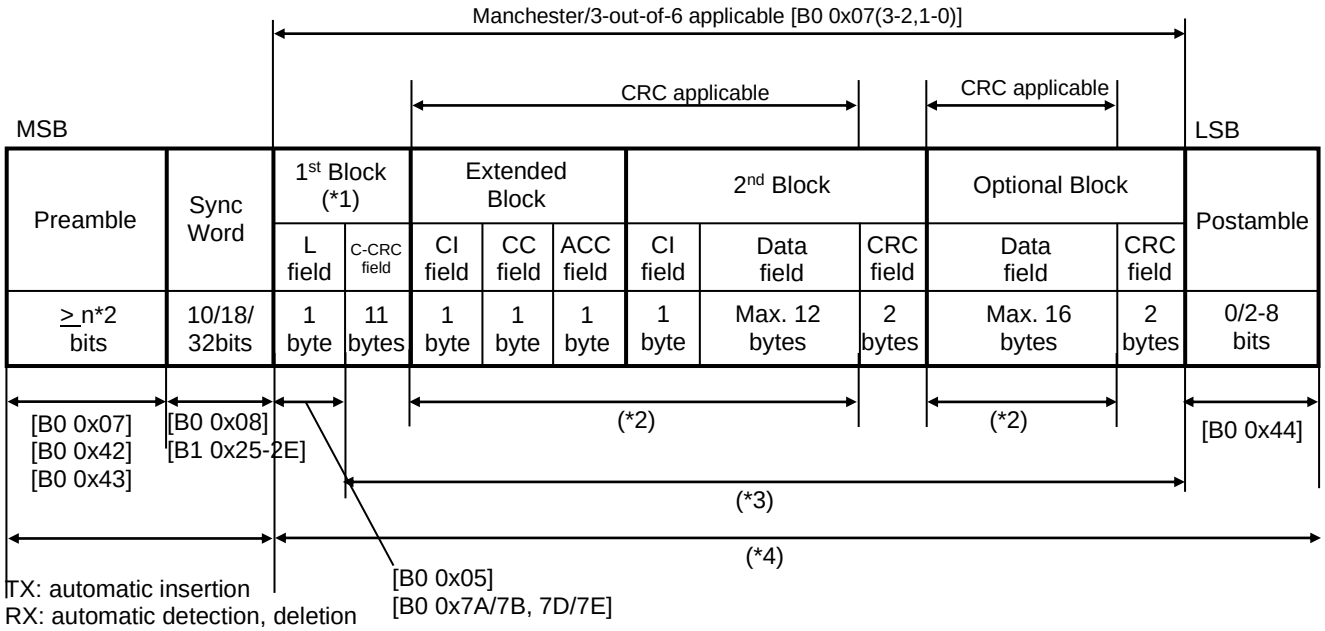
*1 Each mode has different minimum value of n.
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10, indicates DCLK/DIO output area.

Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) is set to 0x8C/0x8D/0x8E/0x8F, Extended Link Layer is applied. The packet format is as follows:

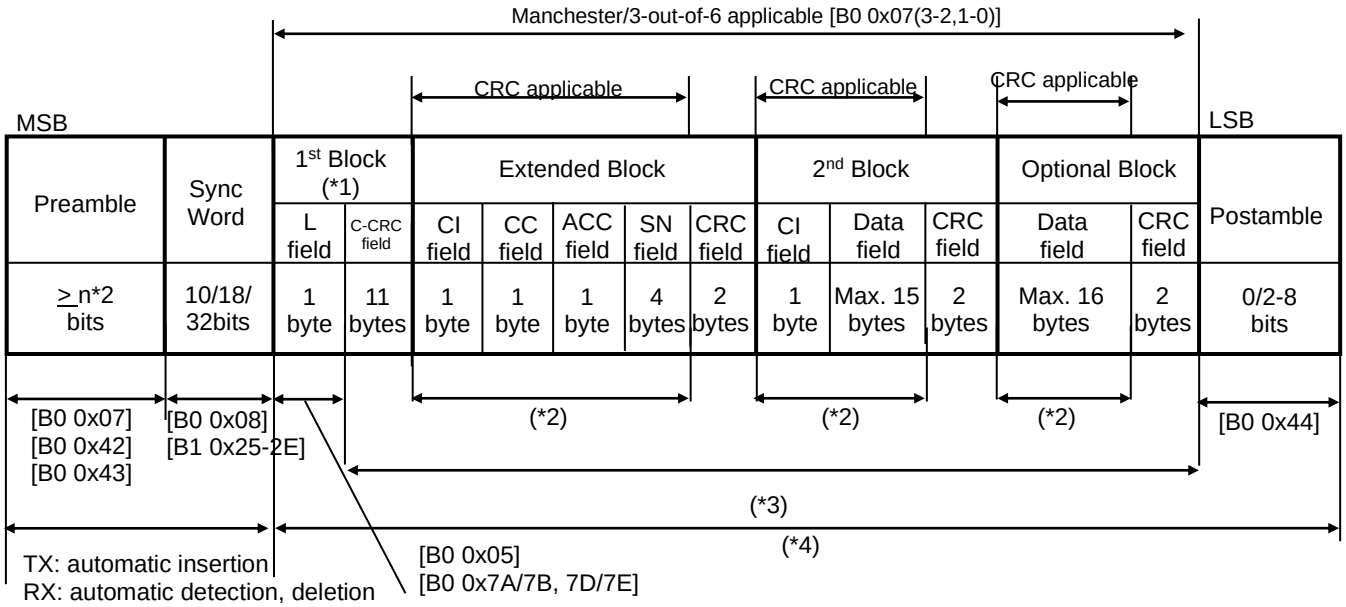
(a) CI-field = 0x8C

If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b01 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if a result of the check is true.



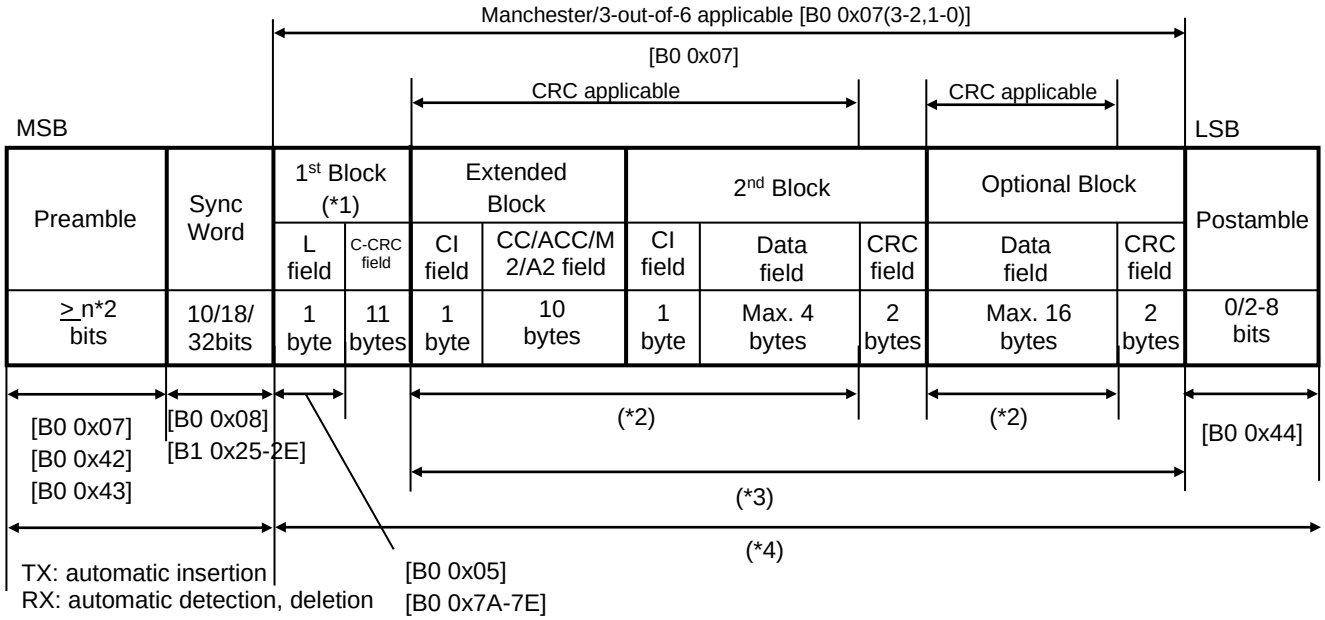
*1 1st Block is equal to Format A without "Extended Block"
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(b) CI-field = 0x8D
If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b10 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if a result of the check is true.



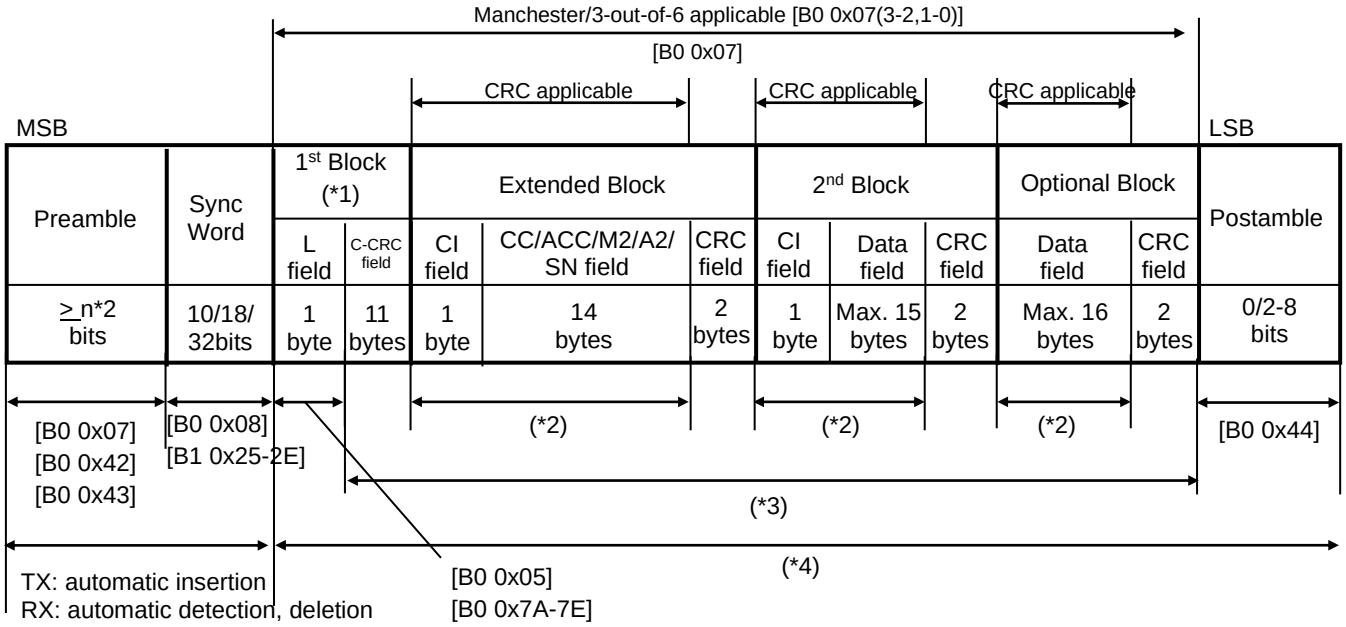
*1 1st Block is equal to Format A without “Extended Block”
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(c) CI-field = 0x8E
If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b01. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if a result of the check is true.



*1 1st Block is equal to Format A without “Extended Block”
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(d) CI-field = 0x8F
If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b10. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if the detection is true.

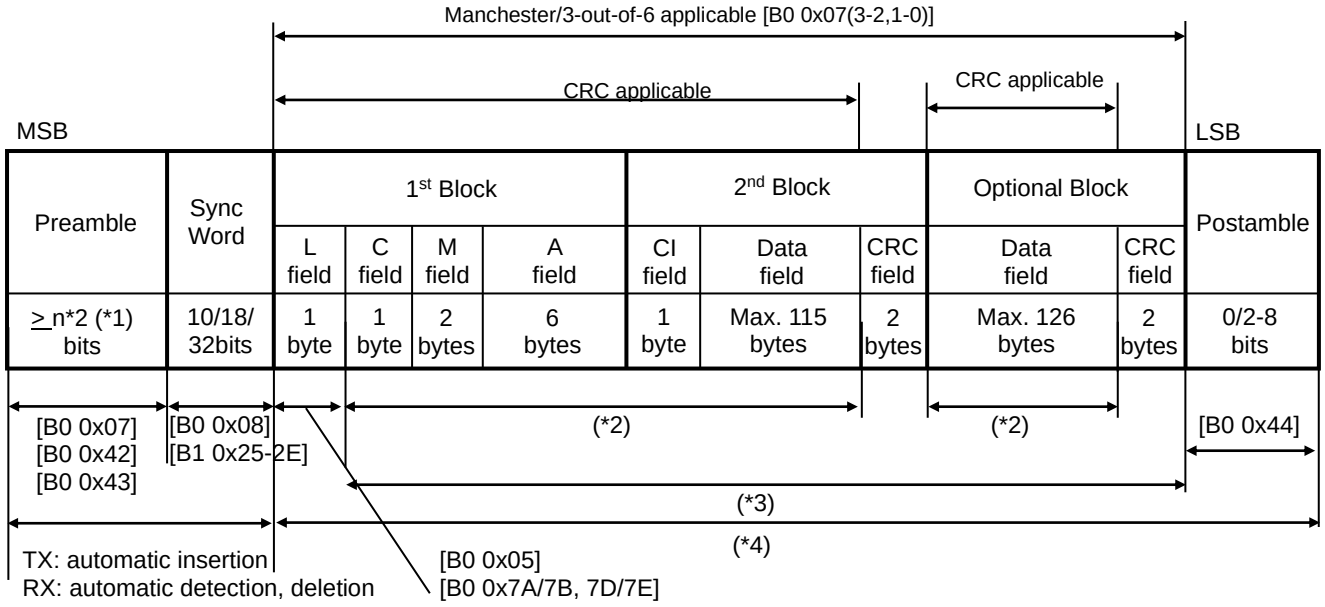


*1 1st Block is equal to Format A without “Extended Block”
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(2) Format B (Wireless M-Bus)

By setting PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b01, Wireless M-Bus Format B is selected.
Format B consists of 1st Block, 2nd Block or Optional Block. Each block after 2nd Block has 2bytes of CRC. "L-field" indicates packet length, which includes subsequent user data bytes from "C-field". However, unlike Format A, CRC bytes are included (Pastamble are exclueded). Depending on "L-field" value, 2nd Block and Optional Block(s) are added.

The following [] indicates register address [bank #, address].



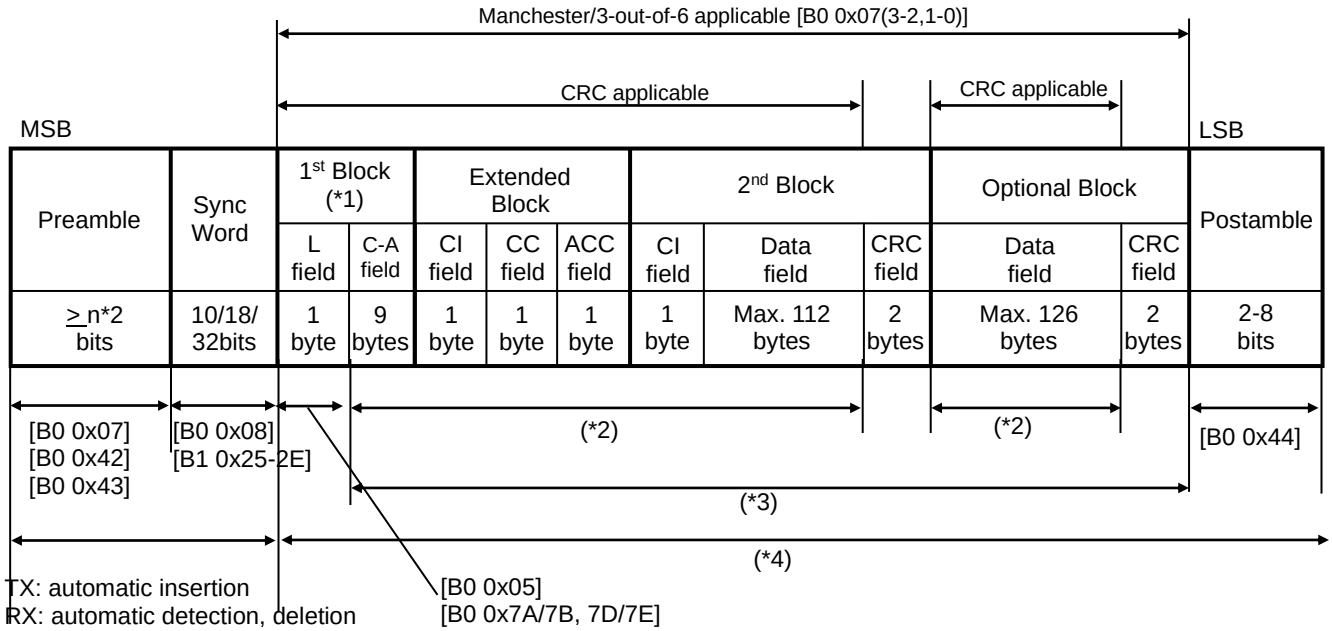
*1 Each mode has different minimum value of n.
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10, indicating DCLK/DIO output area.

Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) is set to 0x8C/0x8D/0x8E/0x8F, Extended Link Layer is applied. The packet format is as follows:

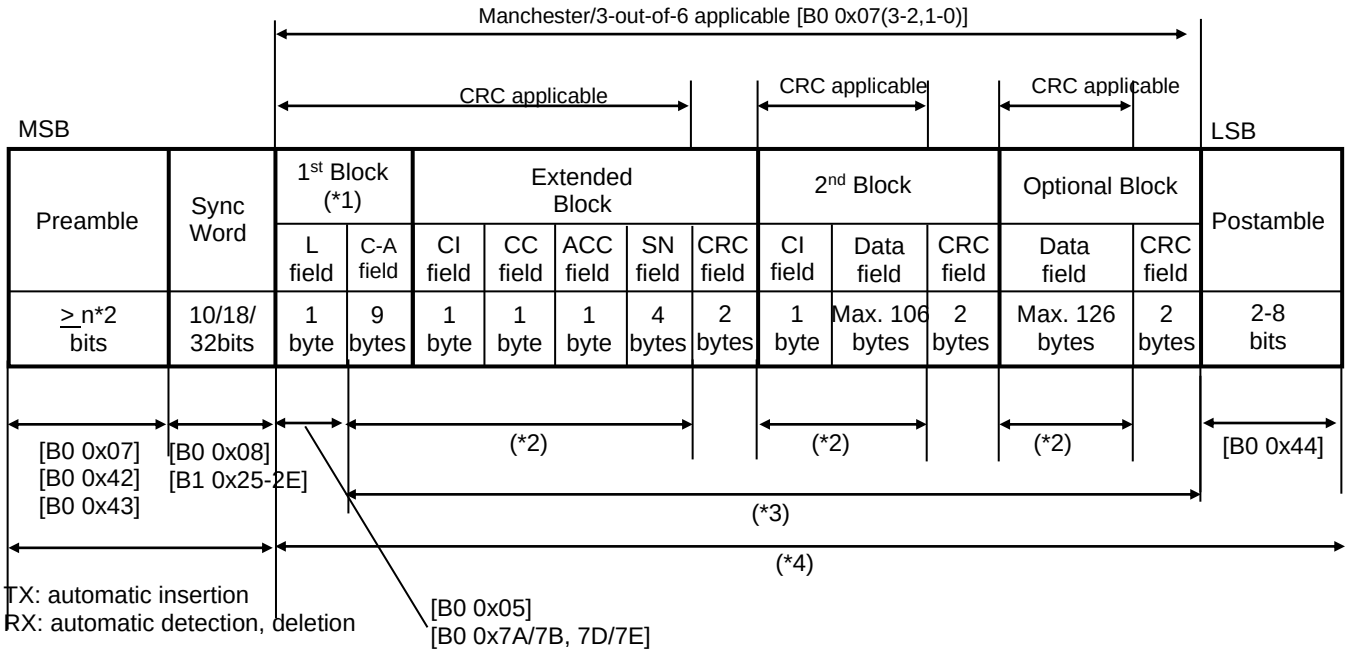
(a) CI-field = 0x8C

If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b01 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if a result of the check is true.



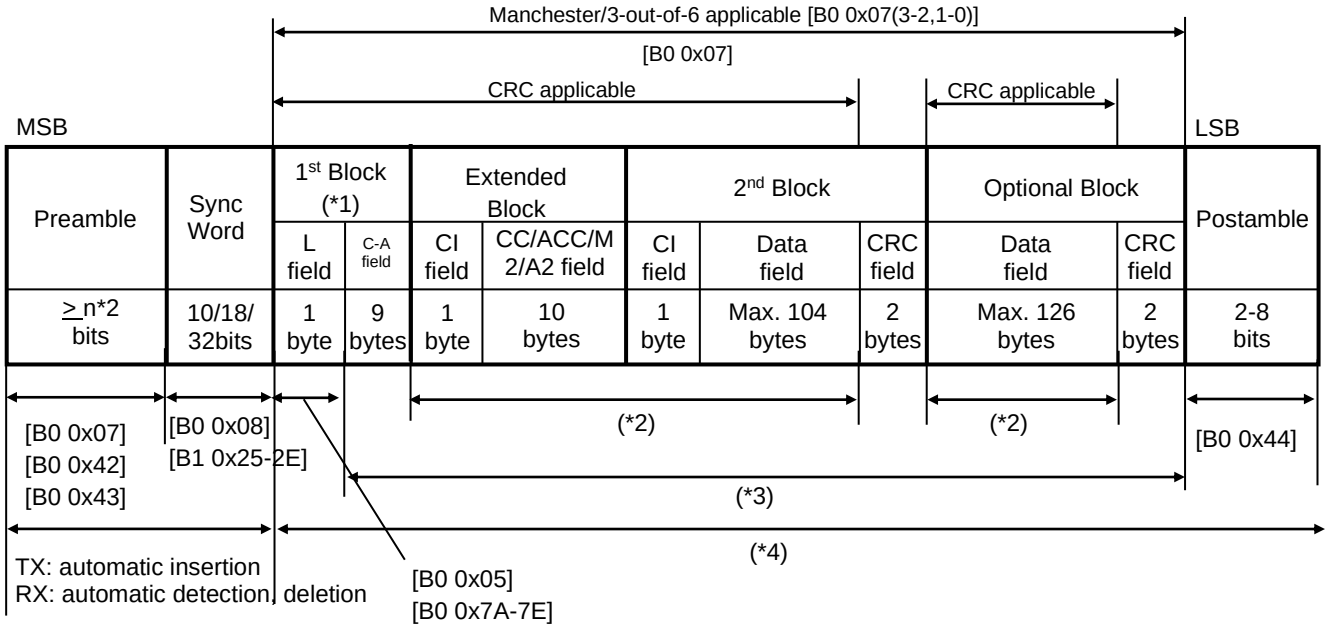
*1 1st Block is equal to Format B without "Extended Block"
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(b) CI-field = 0x8D
If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b10 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if a result of the check is true.



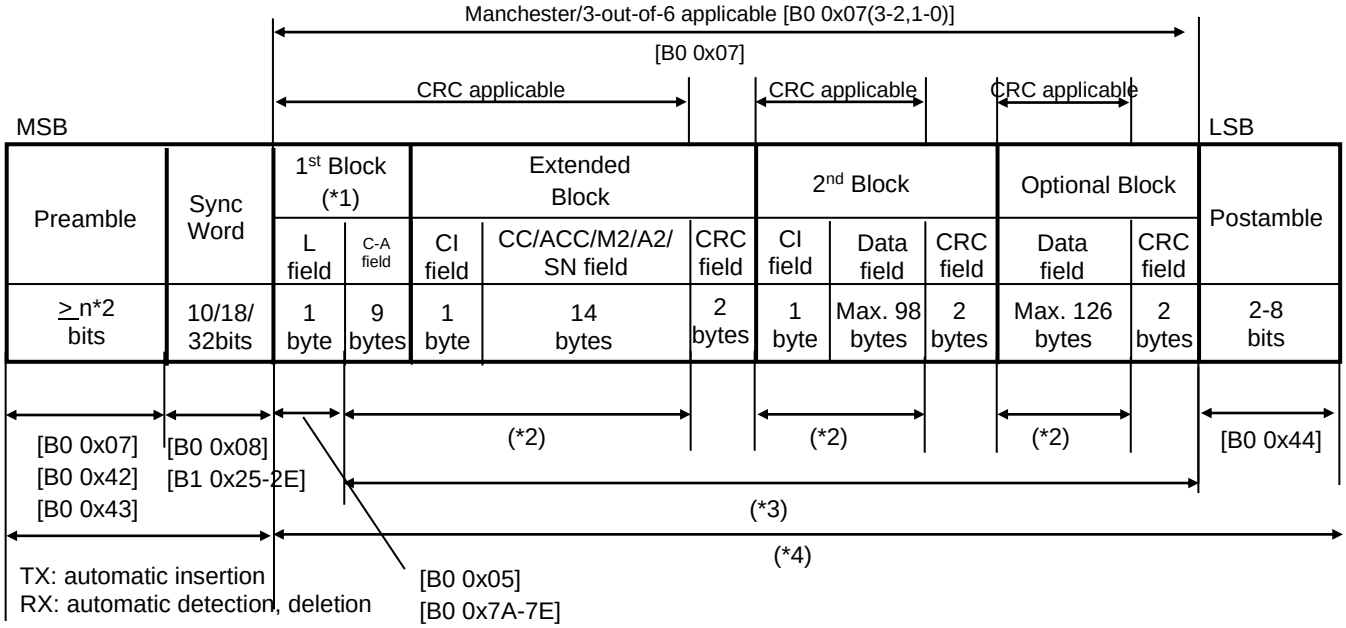
*1 1st Block is equal to Format B without “Extended Block”
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(c) CI-field = 0x8E
If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b01. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process RX sequence if a result of the check is true.



*1 1st Block is equal to Format B without “Extended Block”
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(d) CI-field = 0x8F
If use the extended format in TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b10. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, it is automatically checked whether the RX packet format is the extended packet format. After that, process the RX sequence if the detection is true.

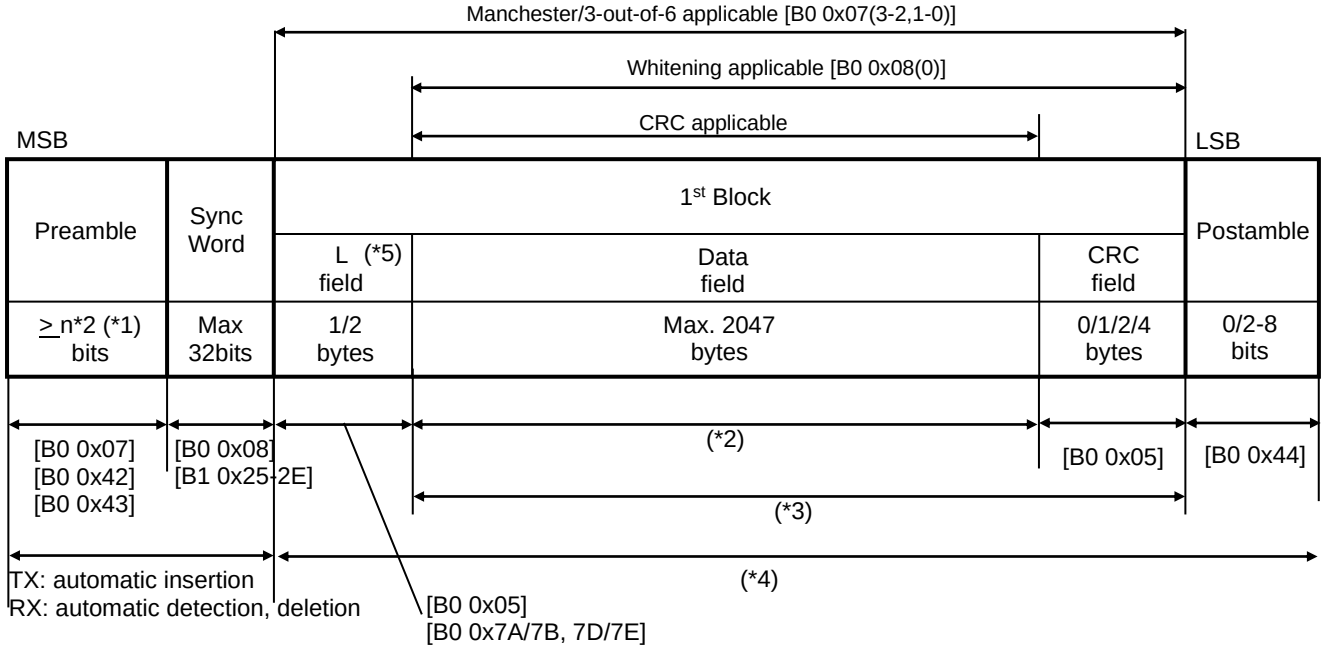


*1 1st Block is equal to Format B without “Extended Block”
*2 Indicates TX FIFO data storage area size.
*3 Indicates RX FIFO data storage area size.
*4 Indicates DCLK/DIO output area at RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(3) Format C (non Wireless M-Bus, general purpose format1)

By setting PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b10, Format C, which is non Wireless M-Bus format, is selected. Format C consists of 1st Block only, which has 2bytes of CRC. "L-field" indicates packet length, which includes subsequent user data bytes, including CRC bytes. The length of "L-field" is defined by LENGTH_MODE([PKT_CTRL2:B0 0x5(0]). Data Whitening function is supported.

The following [] indicates register address [bank #, address].



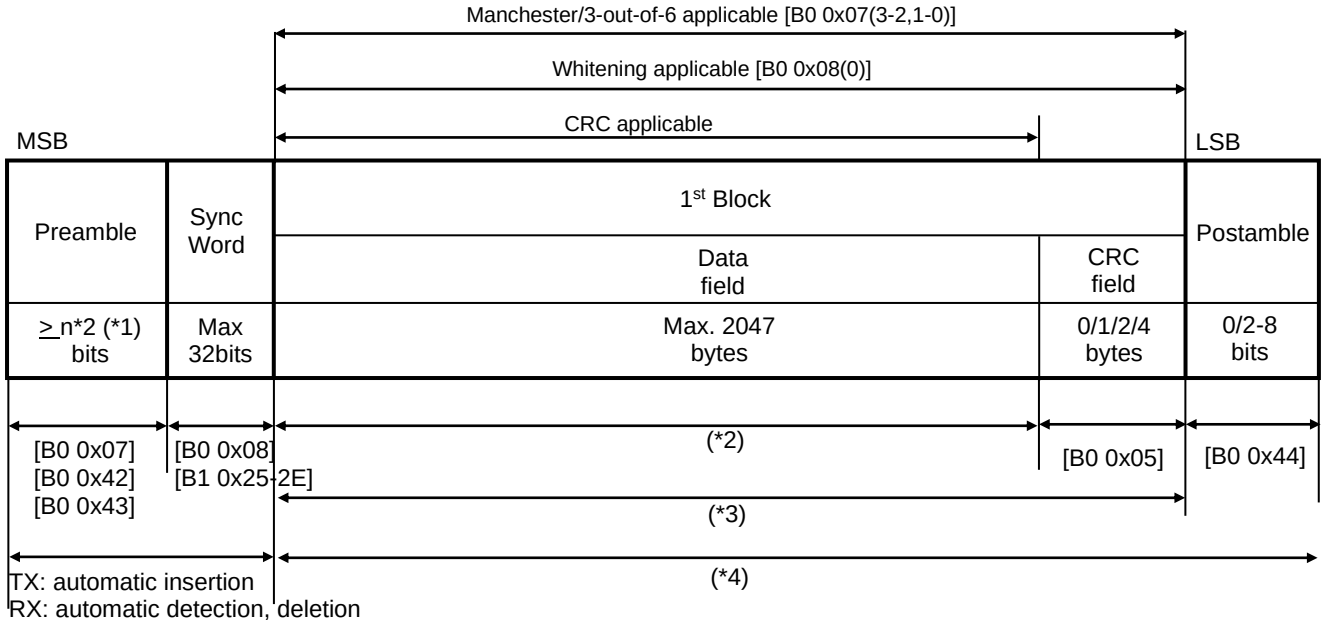
*1 Preamble length (n) is programmable by [TXPR_LEN_H/L: B0 0x42/43] registers.
*2 Indicates TX FIFO data strorage area size.
*3 Indicates RX FIFO data storage area size.
*4 When RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10, indicating DCLK/DIO output area.
*5 ML7404 supports IEEE802.15.4g by setting 2 bytes length mode(LENGTH_MODE ([PKT_CTRL2: B0 0x05(1-0)]) = 0b01). The relationship between L-field and PHR defined by IEEE802.15.4g is as follows.For other setting for IEEE802.15.4g, please refer "Other Functions - IEEE802.15.4g Mode Setting". However, ML7404 does not support Mode Switch function.

L-field		[TX_PKT_LEN: B0 0x7A]					[TX_PKT_LEN: B0 0x7B]
		Bit 7	Bit 6-5	Bit 4	Bit 3	Bit 2-0	Bit 7-0
IEEE802.15.4g PHR	Bits	0	1-2	3	4	5-7	8-15
	Function	Mode Swith	Reserved	FCS Type	Data Whitening	Frame Length(L_{10}-L_0)	

(4) Format D (non Wireless M-Bus, general purpose format2)

When you use Format D, please set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)])=0b11.
Format D is comprised only of 1st Block. The top of 1st Block begins in Data-field, and CRC-field(0/1/2 byte choice possible) is added after Data-field. The Length value shows the total number of bytes from after Data-field to the last CRC data and can be set with [TX_PKT_LENGTH: B0 0x7A/0x7B] or [RX_PKT_LENGTH: B0 0x7D/0x7E].

The following [] indicates register address [bank #, address].



*1 Preamble length (n) is programmable by [TXPR_LEN_H/L: B0 0x42/43] registers.
*2 Indicates TX FIFO data strorage area size.
*3 Indicates RX FIFO data storage area size.
*4 When RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10, indicating DCLK/DIO output area.

○CRC function

ML7404 has CRC32,CRC16 and CRC8 function. CRC is calculated and appended to TX data. CRC is checked for RX data. The following modes are used for automatic CRC function.

- ●FIFO mode: RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b00
- ●DIO mode: RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b11

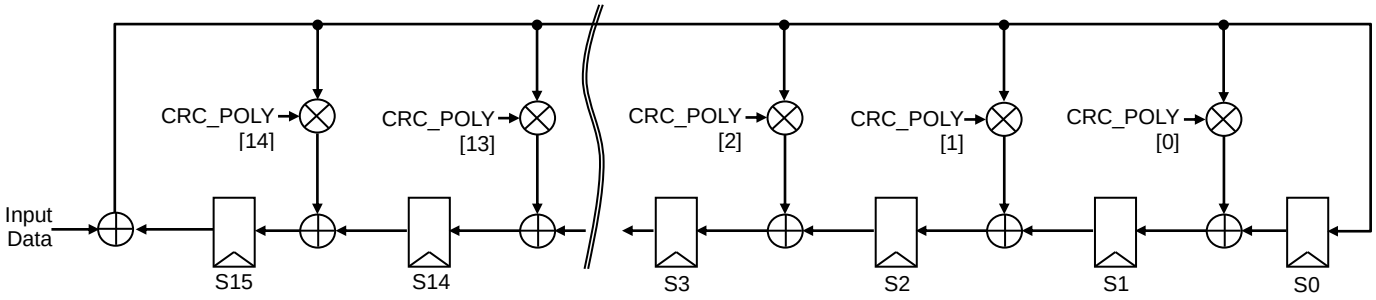
Function	Control bit name / Register
TX CRC setting	TX_CRC_EN([PKT_CTRL2: B0 0x05(2)])
RX CRC setting	RX_CRC_EN([PKT_CTRL2: B0 0x05(3)])
CRC length setting	CRC_LEN([PKT_CTRL2: B0 0x05(5-4)])
CRC complement value OFF setting	CRC_COMP_OFF([PKT_CTRL2: B0 0x05(6)])
CRC polynomial setting	[CRC_POLY3/2/1/0: B1 0x16/17/18/19] registers
CRC error status	[CRC_ERR_H/M/L: B0 0x13/14/15] registers
CRC length setting 2 enable	CRC_LEN2_EN([CRC_ERR_H: B0 0x13(7)])
CRC length setting 2	CRC_LEN2([CRC_ERR_H: B0 0x13(6-5)])

Any CRC polynomials for CRC32/CRC16/CRC8 can be specified. Reset value is as follows:

CRC16 polynomial = $x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$ (reset value)

(Note) CRC result data can be inverted by CRC complement value OFF setting,.

CRC data will be generated by the following circuits. By programming [CRC_POLY3/2/1/0] registers, any CRC polynomials can be supported. Generated CRC will be transfer from the left most bit (S15). If data length is shorter than CRC length (3bytes of CRC32 only), data "0"s will be added for CRC calculation. CRC check result is stored in [CRC_ERR_H/M/L] registers. Unlike Format C, Format A/B can include multiple CRC fields in one packet. For multiple CRCs check results, CRC value closest to L-field will be stored in CRC_ERR[0] ([CRC_ERR_L:B0 0x15(0)]). Subsequent bit will be stored in CRC_ERR from MSB order.



(Note) ⊕ :exclusive OR

CRC16 polynomial circuits

General CRC polynomial can be programmed by below [CRC_POLY3/2/1/0] register setting.
CRC length can be set by CRC_LEN.

CRC polynomial		[CRC_POLY3/2/1/0]			
		(B1 0x16)	(B1 0x17)	(B1 0x18)	(B1 0x19)
CRC8	$x^8 + x^2 + x + 1$	0x00	0x00	0x00	0x03
CRC16	$x^{16} + x^{12} + x^5 + 1$	0x00	0x00	0x08	0x10
	$x^{16} + x^{15} + x^2 + 1$	0x00	0x00	0x40	0x02
	$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$	0x00	0x00	0x1E	0xB2
CRC32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	0x02	0x60	0x8E	0xDB

Furthermore, CRC length for CRC calculation and that for packet attachment (TX) or for checking (RX) can be set separately in ML7404. Set separate CRC lengths in CRC_LEN2_EN, CRC_LEN2 and CRC_LEN.

CRC length for CRC calculation	CRC length for CRC attachment or for checking	CRC_LEN2_EN (B0 0x13)	CRC_LEN2 (B0 0x13)	CRC_LEN (B0 0x05)
CRC8	CRC8	0	-	0b00
CRC16	CRC8	1	0b01	0b00
	CRC16	0	-	0b01
CRC32	CRC8	1	0b10	0b00
	CRC16	1	0b10	0b01
	CRC32	0	-	0b10

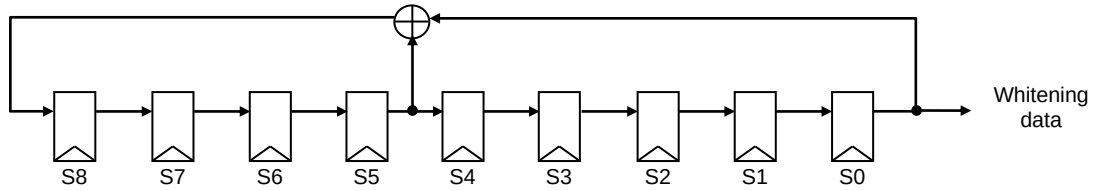
To set different CRC lengths for CRC calculation and for packet attachment (TX) or checking (RX), however, “CRC length for CRC calculation” should be equal to or longer than “CRC length for packet attachment (TX) or for checking (RX).”

○Data Whitening function (non Wireless M-Bus standard)

ML7404 supports Data Whitening function. In packet format A/B, subsequent data followed by C-field can be processed Data Whitening. In packet format C, Data Whitening is applied from data field. Data generated by the following 9bits pseudo random sequence (PN9) will be "XOR" with TX data (encoded data if Manchester or 3-out-of-6 coding is selected) before transmission. Intialization value of the PN9 generation shift register can be defined by [WHT_INIT_H/L: B1 0x64/65] registers. PN9 polynomial can be programmed with [WHT_CFG: B1 0x66] register.

Function	Control bit name
Data Whiteing setting enable	WHT_SET ([DATA_SET2: B0 0x08(0)])
Data Whiteing initiazation value	WHT_INIT[8:0] ([WHT_INIT_H/L: B1 0x64(0)/65(7-0)])
Whitening polynomia	WHT_CFG[7:0] ([WHT_CFG: B1 0x66(7-0)])

In order to make feedback from S1 register, setting 0b1 to WHT_CFG0 ([WHT_CFG: B1 0x66(0)]). Similaly in order to make feedback from S2 register, setting 0b1 to WHT_CFG1 ([WHT_CFG: B1 0x66(1)]). Other bits of [WHT_CFG: B1 0x66] register has same function. Two or more bits can be also set to 0b1. Therefore any type of PN9 polinominal can be programmed.



(Note) ⊕ :exclusive OR

Whitening data generation circuits
(generator polynomial: $x^9 + x^5 + 1$)

General PN9 polynomial can be defined by [WHT_CFG].

PN9 polynomial	WHT_CFG[7:0] [WHT_CFG: B1 0x66]
$x^9 + x^4 + 1$	0x08
$x^9 + x^5 + 1$	0x10

○SyncWord detection function

ML7404 supports automatic SyncWord recognition function. By having two sets of SyncWord pattern storage area, it is possible to detect two different packet format (Format A/B) which are defined by Wireless M-Bus. (For details, please refer to Wireless M-Bus standard) Receiving packet format is indicated by SW_DET_RSLT([STM_STATE:B0 0x77(5)]). In Format C/D, it is possible to search for two SyncWords but detected result is not indicated.

1) TX
SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. SyncWord length for TX is defined by SYNC_WORD_LEN[5:0] ([SYNC_WORD_LEN: B1 0x25(5-0)]). From high bit of each SyncWord pattern will be transmitted.

SYNCWORD_SEL	TX SyncWord pattern
0	SYNC_WORD1[31:0] ([SYNCWORD1_SET3/2/1/0: B1 0x27/28/29/2A])
1	SYNC_WORD2[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E])

Example) SyncWord patten and SyncWord length

If the follwing registers are programmed, from higher bit of SYNC_WORD1[17:0] will be transmitted sequencially.
[SYNC_WORD_LEN: B1 0x25] = 0x12
SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b0

If the following registers are programmed, from higher bit of SYNC_WORD2[23:0] will be transmitted sequencially.
[SYNC_WORD_LEN: B1 0x25] = 0x18
SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b1

2) RX
By setting SYNCWORD_SEL and 2SW_DET_EN ([DATA_SET2: B0 0x08(4,3)]), one SyncWord pattern waiting or two SyncWord patterns waiting can be selected as follows: Packet format automatic detection is valid if 2SW_DET_EN = 0b1 and Format A or Fromat B is selected by PKT_FORMAT[1:0] ([PKT_CTRL1:B0 0x04(1-0)]).

2SW_DET_EN	SYNCWORD_SEL	SyncWord pattern During Sync Detection	SyncWord Detection operation	Automatic packet format detection	Data process after SyncWord
0	0	SYNC_WORD1[31:0]	Waiting for 1 pattern	no	Process according to each Format setting
0	1	SYNC_WORD2[31:0]	Waiting for 1 pattern	no	Process according to each Format setting
1	–	SYNC_WORD1[31:0] SYNC_WORD2[31:0]	Waiting for 2 patterns	yes	[Format A or Format B setting] If matched with SYNC_WORD1, then process as Format A. If matched with SYNC_WORD2, then process as Format B. [Format C/D setting] Process as Format C/D

Length of SyncWord pattern can be defined by SYNC_WORD_LEN[5:0] ([SYNC_WORD_LEN: B1 0x25(5-0)]). In this case, SyncWord pattern defined by the length from low bit of SYNC_WORD1[31:0] or SYNC_WORD2[31:0] will be the pattern for checking.

Example) SyncWord length

If the following registers are set, 18bits of SYNC_WORD1[17:0] or SYNC_WORD2[17:0] will be reference pattern for the SyncWord detection. Higher bits (bit31-18) are not checked.

[SYNC_WORD_LEN: B1 0x25] = 0x12

[SYNC_WORD_EN: B1 0x26] = 0x0F

32bits SyncWord pattern can be controlled by enabling/disabling by each 8bits, when receiving SyncWord. The following table describes enable/disable control and SyncWord pattern.

[SYNC_WORD_EN] (B1 0x26)	SYNCWORD*_SET*				SyncWord detection operation
	[31:24]	[23:16]	[15:8]	[7:0]	
0000					prohibited
0001	D.C.(*1)			ON	Only [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0010	D.C.		ON	D.C.	Only [15:8] are valid. Upon [7:0] detection, SyncWord detection.
0011	D.C.		ON	ON	[15:0] are valid. Upon [7:0] detection, SyncWord detection.
0100	D.C.	ON	D.C.		Only [23:16] are valid. Upon [7:0] detection, SyncWord detection.
0101	D.C.	ON	D.C.	ON	[23:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0110	D.C.	ON	ON	D.C.	[23:8] are valid. Upon [7:0] detection, SyncWord detection.
0111	D.C.	ON	ON	ON	[23:0] are valid. Upon [7:0] detection, SyncWord detection.
1000	ON	D.C.			Only [31:24] are valid. Upon [7:0] detection, SyncWord detection.
1001	ON	D.C.		ON	[31:24] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1010	ON	D.C.	ON	D.C.	[31:24] and [15:8] are valid. Upon [7:0] detection, SyncWord detection.
1011	ON	D.C.	ON	ON	[31:24] and [15:0] are valid. Upon [7:0] detection, SyncWord detection.
1100	ON	ON	D.C.		[31:16] are valid. Upon [7:0] detection, SyncWord detection.
1101	ON	ON	D.C.	ON	[31:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1110	ON	ON	ON	D.C.	[31:8] are valid. Upon [7:0] detection, SyncWord detection.
1111	ON	ON	ON	ON	Whole [31:0] are valid. Upon [7:0] detection, SyncWord detection.

*1 D.C. stands for Don't Care.

*2 Preamble pattern can be added to the SyncWord detection conditions by RXPR_LEN[5:0]([SYNC_CONDITION1: B0 0x45(5-0)]).

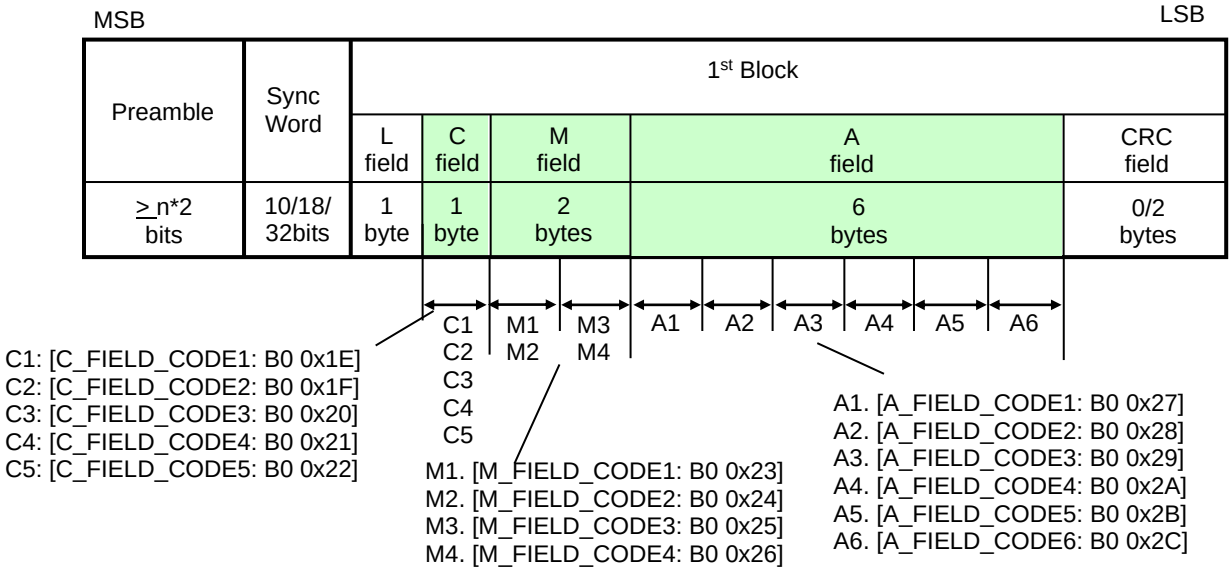
○Field check function

ML7404 has the function of comparing the 9bytes following L-field (Format A/B: start from C-field, Format C: start from Data-field) in a receiving packet. Based on comparison with the expected data, possible to generate interrupts (Field check function). Field check can be possible with the following register setting. When using this function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) = 0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required. Also, when using the spread spectrum function, this function is valid only when FEC is disabled.

Function	Register
RX data process setting when Field check unmatched	[C_CHECK_CTRL: B0 0x1B(7)]
Field check interrupt setting	[C_CHECK_CTRL: B0 0x1B(6)]
C-field detection enable setting	[C_CHECK_CTRL: B0 0x1B(4-0)]
M-field detection enable setting	[M_CHECK_CTRL: B0 0x1C(3-0)]
A-field detection enable setting	[A_CHECK_CTRL: B0 0x1D(5-0)]
C-field code setting	[C_FIELD_CODE1: B0 0x1E] [C_FIELD_CODE2: B0 0x1F] [C_FIELD_CODE3: B0 0x20] [C_FIELD_CODE4: B0 0x21] [C_FIELD_CODE5: B0 0x22]
M-field code setting	[M_FIELD_CODE1: B0 0x23] [M_FIELD_CODE2: B0 0x24] [M_FIELD_CODE3: B0 0x25] [M_FIELD_CODE4: B0 0x26]
A-field code setting	[A_FIELD_CODE1: B0 0x27] [A_FIELD_CODE2: B0 0x28] [A_FIELD_CODE3: B0 0x29] [A_FIELD_CODE4: B0 0x2A] [A_FIELD_CODE5: B0 0x2B] [A_FIELD_CODE6: B0 0x2C]

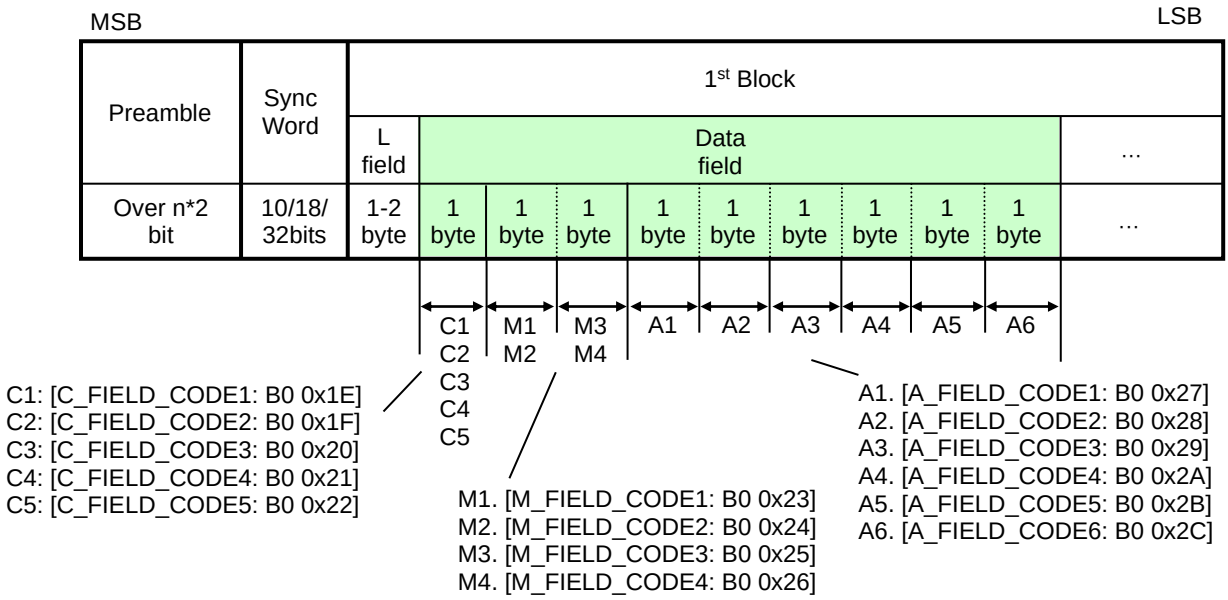
The following describes the relation between each comparison code and incoming RX data.

[Format A/B(Wireless M-Bus)]
Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all specified Field data (C-field/M-field/A-field) are matched, Field checking matching will be notified. However, if C-field data and C_FIELD_CODE5 are matched, even if other Field data (M-field/A-field) are not matched, Field check result will be notified as “match”.



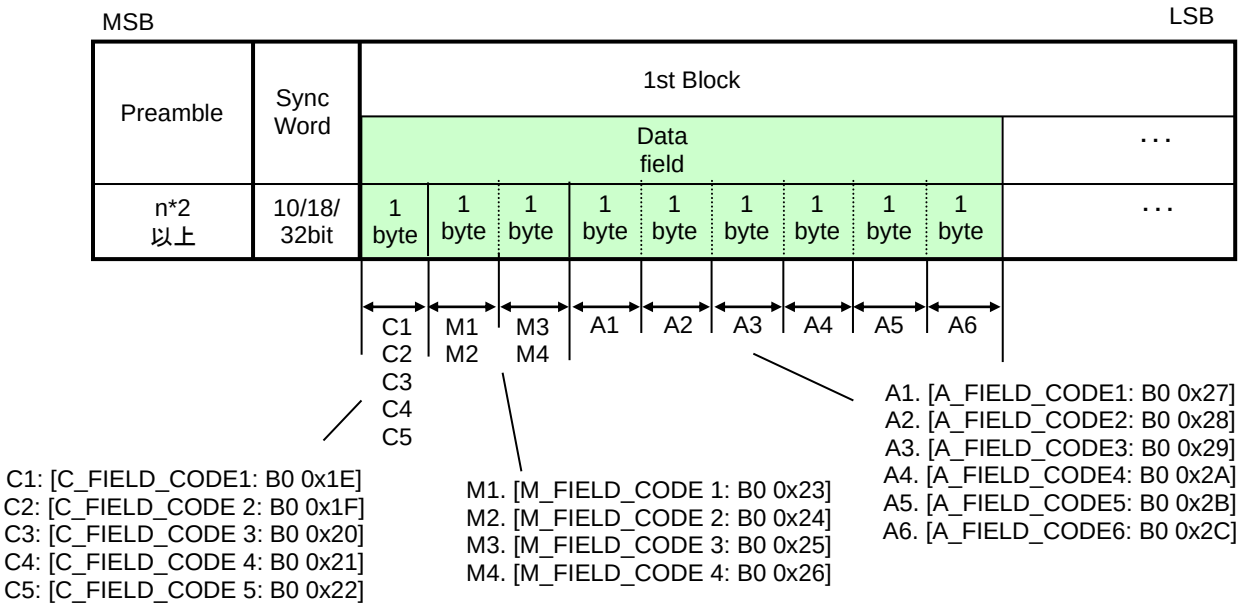
Check Field	Comaprison Code	Conditions for match
C-field	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	If one of the 5 comparison code is matched
M-field 1st byte	M_FIELD_CODE1 or M_FIELD_CODE2	If one of the 2 comparison code is matched.
M-field 2nd byte	M_FIELD_CODE3 or M_FIELD_CODE4	If one of the 2 comparison code is matched.
A-field	A_FIELD_CODE1/2/3/4/5/6	If comparison codes are matched.

[Format C]
Field check can be controlled by setting disabled/enabled for each comarison code (1byte). If all specified Field data (specified table below) are matched, Field checking matching will be notified. However, if 1st byte of Data field and C_FIELD_CODE5 are matched, even if other Field data(from 2nd byte of Data field to 9th byte of Data field) are not matched, Field check result will be notified as "match".



Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	If one of the 5 comparison code is matched
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	If one of the 2 comparison code is matched.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	If one of the 2 comparison code is matched.
Data-field 4th byte	A_FIELD_CODE1	If comparison code is matched.
Data-field 5th byte	A_FIELD_CODE2	If comparison code is matched.
Data-field 6th byte	A_FIELD_CODE3	If comparison code is matched.
Data-field 7th byte	A_FIELD_CODE4	If comparison code is matched.
Data-field 8th byte	A_FIELD_CODE5	If comparison code is matched.
Data-field 9th byte	A_FIELD_CODE6	If comparison code is matched.

[Format D]
Field check can be controlled by setting disabled/enabled for each reference pattern. If all the data of data-field meet the matching conditions specified in the table below, Field checking matching will be notified. However, only if 1st byte of the data-field and C_FIELD_CODE5 are matched even with other field data (from 2nd byte to 9th byte of the data-field) being not matched, Field check result will be notified as "match."



Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	One of the five reference patterns is matched.
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	One of the two reference patterns is matched.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	One of the two reference patterns is matched.
Data-field 4th byte	A_FIELD_CODE1	The reference pattern is matched.
Data-field 5th byte	A_FIELD_CODE2	The reference pattern is matched.
Data-field 6th byte	A_FIELD_CODE3	The reference pattern is matched.
Data-field 7th byte	A_FIELD_CODE4	The reference pattern is matched.
Data-field 8th byte	A_FIELD_CODE5	The reference pattern is matched.
Data-field 9th byte	A_FIELD_CODE6	The reference pattern is matched.

●Packet processing as a result of Field checking
By setting CA_RXD_CLR ([C_CHECK_CTRL: B0 0x1B(7)]) = 0b1, if the result of Field check is unmatch, data packet will be aborted and wait for next packet data.

●Storing number of unmatched packets
Unmatched packets can be counted up to max. 2047 packets and result are stored in [ADDR_CHK_CTR_H: B1 0x62] and[ADDR_CHK_CTR_L: B1 0x63]. This count value can be cleared by STATE_CLR4 ([STATE_CLR: B0 0x16(4)]).

○FIFO control function

ML7404 has on-chip TX_FIFO(64bytes) and RX_FIFO(64bytes). As TX/RX_FIFO do not support multiple packets, packet should be processed one by one. If RX_FIFO keeps RX packet and next RX packet is received, RX_FIFO will be overwritten. It applies to TX_FIFO as well. However TX FIFO access error interrupt (INT[20] group3) will be generated. When receiving, RX data is stored in FIFO (byte by byte) and the host MCU will read RX data through SPI. When transmitting, host MCU write TX data to TX_FIFO through SPI and transmitting through RF.

Writing or reading to FIFO is through SPI with burst access. TX data is written to [WR_TX_FIFO: B0 0x7C] register. RX data is read from [RD_FIFO: B0 0x7F] register. Continuous access increments internal FIFO counter automatically. If FIFO access is suspended during write or read operation, address will be kept until the packet will be process again. Therefore, when resuming FIFO access, next data will be resumed from the suspended address.

FIFO control register are as follows:

Function	Register
TX FIFO Full level setting	[TXFIFO_THRH: B0 0x17]
TX FIFO Empty level setting	[TXFIFO_THRL: B0 0x18]
RX FIFO Full level setting	[RXFIFO_THRH: B0 0x19]
RX FIFO Empty level setting	[RXFIFO_THRL: B0 0x1A]
FIFO readout setting	[FIFO_SET: B0 0x78]
RX FIFO data usafe status indication	[RX_FIFO_LAST: B0 0x79]
TX packet Length setting	[TX_PKT_LEN_H/L: B0 0x7A/7B]
RX packet Length setting	[RX_PKT_LEN_H/L: B0 0x7D/7E]
TX FIFO	[WR_TX_FIFO: B0 0x7C]
FIFO read	[RD_FIFO: B0 0x7F]

TX – RX procedure using FIFO are as follows:

[TX]

i) TX data L-field value is set to [TX_PKT_LEN_H: B0 0x7A], [TX_PKT_LEN_L: B0 0x7B] register. If Length is 1 byte, [TX_PKT_LEN_L] register will be transmitted.
   Length can be set to LENGTH_MODE([PKT_CTRL2: B0 0x05(0)]).
ii) TX data is written to [WR_TX_FIFO:B0 0x7C] register.

(Note)

1. If TX_FIFO write sequence is aborted during transmission, STATE_CLR0 [STATE_CLR:B0 0x16(0)] (TX FIFO pointer clear) must be issued. Otherwise data pointer is kept in the LSI and the next packet is not processed properly.
   For example, TX FIFO access error interrupt (INT[20] group3) is generated. This interrupt can be generated when the next packet data is writren to the TX_FIFO before transmitting previous packet data or TX_FIFO overrun (FIFO is written when no TX_FIFO space) or underrun (attempt to transmit when TX_FIFO is empty)
2. FIFO is overwritten when the following packet data is written in, where the data of one packet is stored.
3. Depending on the packet format, TX data Length value is different.
   Format A: Length includs data area excluding L-field and CRC data.
   Format B: Length includes data area excluding L-field.
   Format C: Length includes data area excluding L-field.
   Format D: Length includes from Data-field to CRC-field.

[RX]
(1) Format A/B/C
i) The value of L-field (Length) is read from [RX_PKT_LEN_H: B0 0x7D] and [RX_PKT_LEN_L: B0 0x7E].
ii) RX data is read from FIFO.
To read RX FIFO, be sure to set FIFO_R_SEL([FIFO_SET: B0 0x78(0)]) to 0b0.
In case of FIFO_R_SEL=0b1, TX FIFO is selected as FIFO readout.
The data usage of RX FIFO is indicated in [RX_FIFO_LAST: B0 0x79].

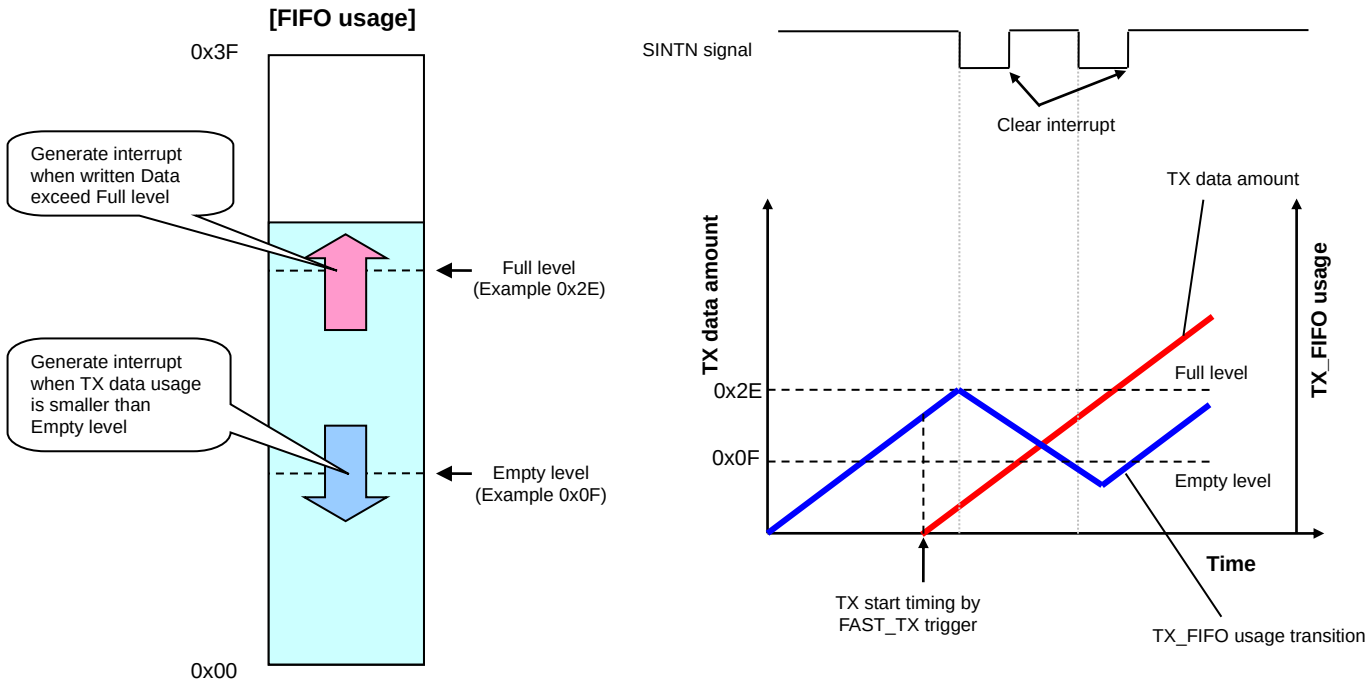
(2) Format D
i) Set the data length (the value of Length) in [RX_PKT_LEN_H: B0 0x7D] and [RX_PKT_LEN_L: B0 0x7E].
ii) RX data is read from FIFO.
To read RX FIFO, be sure to set FIFO_R_SEL([FIFO_SET: B0 0x78(0)]) to 0b0.
In case of FIFO_R_SEL=0b1, TX FIFO is selected as FIFO readout.
The data usage of RX FIFO is indicated in [RX_FIFO_LAST: B0 0x79].

(Note)
1. If reading FIFO data is terminated before reading all data, STATE_CLR1 [STATE_CLR: B0 0x16(1)] (RX FIFO pointer clear) must be issued. Otherwise If RX_FIFO is not cleared, the pointer controlling FIFO data keeps the same status. Next RX data will not be processed in the FIFO properly.
2. If 1 packet data is kept in the RX_FIFO, next RX data will be overwritten. Please read all required receiving data before receiving the next RX data. In addition, when the following packet is received without reading no data, the state can be judged using SyncWord detection interruption.
3. Please control FIFO not to overrun or underrun FIFO. In oder to control FIFO not to overrun or underrun FIFO, there are the following methods.
(1) The data for the amount used is read using [RX_FIFO_LAST:B0 0x79]).
(2) Set up the FIFO Full level([RXFIFO_THRH: B0 0x19]). The amount of data equivalent to a Full level is read from FIFO after FIFO-Full interruption generating.

IF TX/RX pack is larger than FIFO size, FIFO access can be controlled by FIFO-Full trigger or FIFO-Empty trigger.

(1) TX FIFO usage notification function

This function is to notice TX_FIFO usage to the MCU using interrupt (SINTN). If TX_FIFO usage (un-transmitted data in TX_FIFO) exceed the Full level threshold set by [TXFIFO_THRH: B0 0x17] register, interrupt will generate as FIFO-full interrupt (INT[5] group1). If TX_FIFO usage is smaller than Empty level threshold set by [TXFIFO_THRL: B0 0x18] register, FIFO-Empty interrupt will generate as FIFO-Empty interrout (INT[4] grou1). Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin.
For output setting, please refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52] registers for output setting.

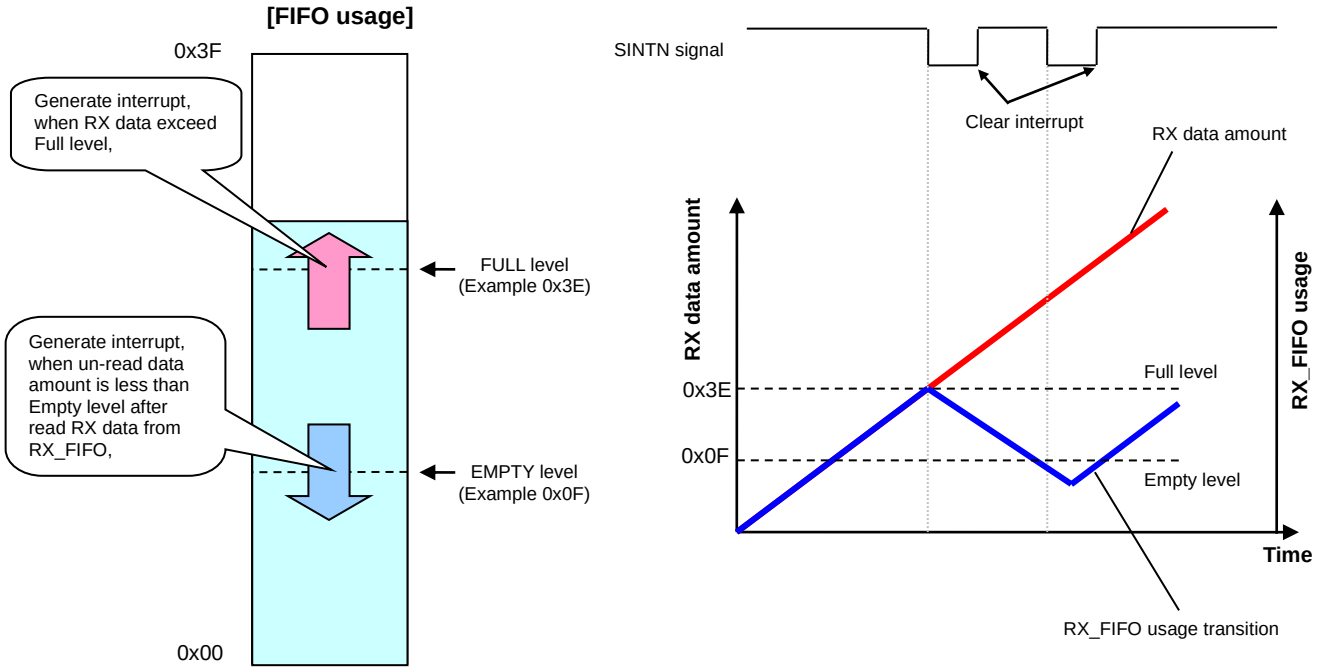


(Note)

1. Should not set [TXFIFO_THRH] and [TXFIFO_THRL] to a same level. Set them as satisfying the condition [TXFIFO_THRH] > [TXFIFO_THRL].
2. The internal state of “Full detected” is cleared when the FIFO usage becomes “Full trigger ([TXFIFO_THRH])” > “FIFO usage”. After that, the FIFO can detect the next Full trigger. Note that the above clear condition may be met during FIFO write, and the Full trigger may be detected again immediately. This depends on the timing of reading TX data (PHY) and writing data to the FIFO via SPI. To avoid such a case, disable the trigger after the Full trigger is detected, and enable again after the FIFO write is completed.
3. The internal state of “Empty detected” is cleared when the FIFO usage becomes “FIFO usage” ≥ ”Empty trigger ([TXFIFO_THRL])”. After that, the FIFO can detect the next Empty trigger. Note that the above clear condition may be met during FIFO write, and the Empty trigger may be detected again immediately. This depends on the timing of reading TX data (PHY) and writing data to the FIFO via SPI. To avoid such a case, disable the trigger after the Empty trigger is detected, and enable again after the FIFO write is completed.

(2) RX FIFO usage notification function

This function is to notify RX_FIFO usage amount by using interrupt (SINTN) to the MCU. If RX_FIFO usage (un-read data in RX_FIFO) exceed Full level threshold defined by [RXFIFO_THRH: B0 0x19] register, interrupt will generate as FIFO-Full interrupt (INT[5] group1). After MCU read RX data from RX_FIFO, un-read amount become smaller than Empty level threshold defined by [RXFIFO_THRL: B0 0x1A] register, interrupt will generated as FIFO-Empty (INT[4] group1). Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK.
For output setting, please refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52] registers.



(Note)

1. Should not set [RXFIFO_THRH] and [RXFIFO_THRL] to a same level. Set them as satisfying the condition [RXFIFO_THRH] > [RXFIFO_THRL].
2. The internal state of “Full detected” is cleared when the FIFO usage becomes “Full trigger ([RXFIFO_THRH])” > “FIFO usage”. After that, the FIFO can detect the next Full trigger. Note that the above clear condition may be met during FIFO read, and the Full trigger may be detected again immediately. This depends on the timing of writing RX data (PHY) and reading data of the FIFO via SPI. To avoid such a case, make the trigger level setting disabled after the Full trigger is detected, and make it enabled again after the FIFO read is completed.
3. The internal state of “Empty detected” is cleared when the FIFO usage becomes ≥ “Empty trigger ([RXFIFO_THRL])”, allowing the next Empty trigger to be detected. Note that the above clear condition may be met during FIFO read, and the Empty trigger may be detected, depending on the timing of writing RX data (PHY) and FIFO read through SPI. To avoid such a case, make the trigger level setting disabled after the Empty trigger is detected, and make it enabled again after the FIFO read is completed.
4. This function is valid during data receiving. FIFO-Empty interrupt does not occur after RX completion.

○DIO function

Using GPIO0-3, EXT_CLK or SDI/SDO pins, TX/RX data can be input/output. Pins can be configured by [GPIO*_CTRL: B0 0x4E/0x4F/0x50/0x51], [EXTCLK_CTRL: B0 0x52] and [SPI/EXT_PA_CTRL: B0 0x53] registers.
Data format for TX/RX are as follows:

TX --- TX data (NRZ or Manchester/3-out-of-6 coding) will be input.
RX --- pre-decoded RX data or decoded RX data will be output. (selectable by [DIO_SET: B0 0x0C] register)

DIO function registers are as follows:

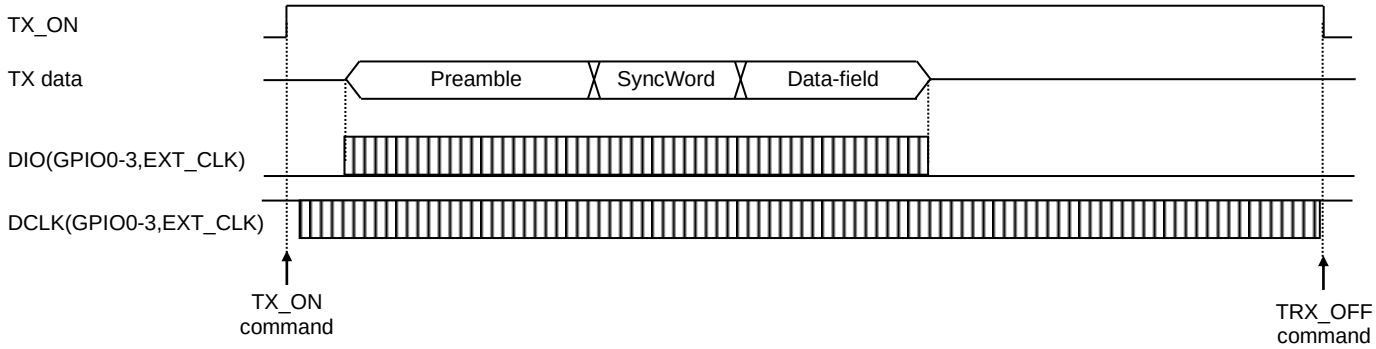
Function	Registers
DIO RX data output start setting	[DIO_SET: B0 0x0C(0)]
DIO RX completion setting	[DIO_SET: B0 0x0C(2)]
TX DIO mode setting	[DIO_SET: B0 0x0C(5-4)]
RX DIO mode setting	[DIO_SET: B0 0x0C(7-6)]

(1) In case of using GPIO*, EXT_CLK pins

If GPIO0-3 or EXT_CLK pins are used as DCLK/DIO, DCLK/DIO should be controlled as follow. (below DIO/DCLK vertical line part indicate output or input period)

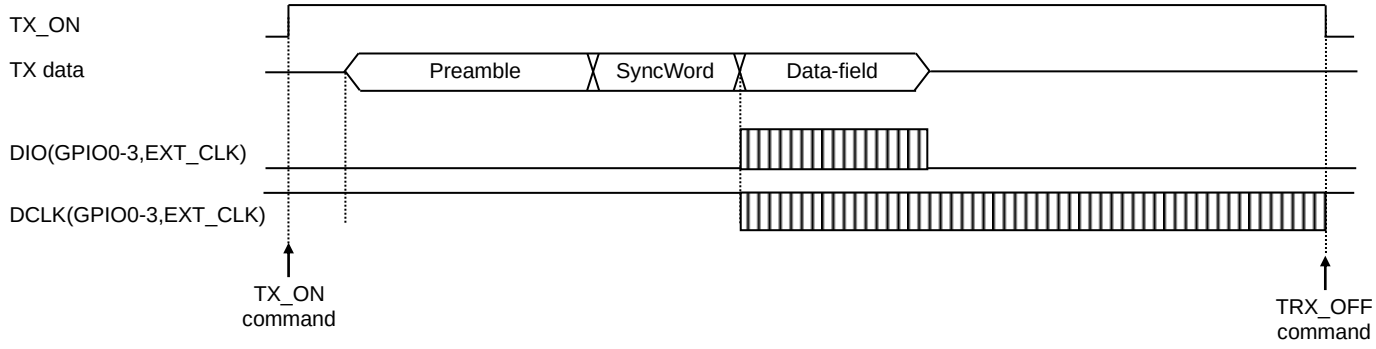
[TX]

i) Continuous input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) = 0b01.
After TX_ON(SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)]) = 0x9), DCLK is output continuously. At falling edge of DCLK, TX data is input from DIO pin. TX data must be encoded data.



(Note)
For details of timing, please refer to the “TX” in the “Timing Chart”.

ii) Data input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) = 0b10.
After TX_ON, DCLK is output during data input period after SyncWord. TX data is input at falling edge of DCLK through DIO input. Encoded TX data must be transferred from the host. Preamble and SyncWordis generated automatically according to the registers setting.



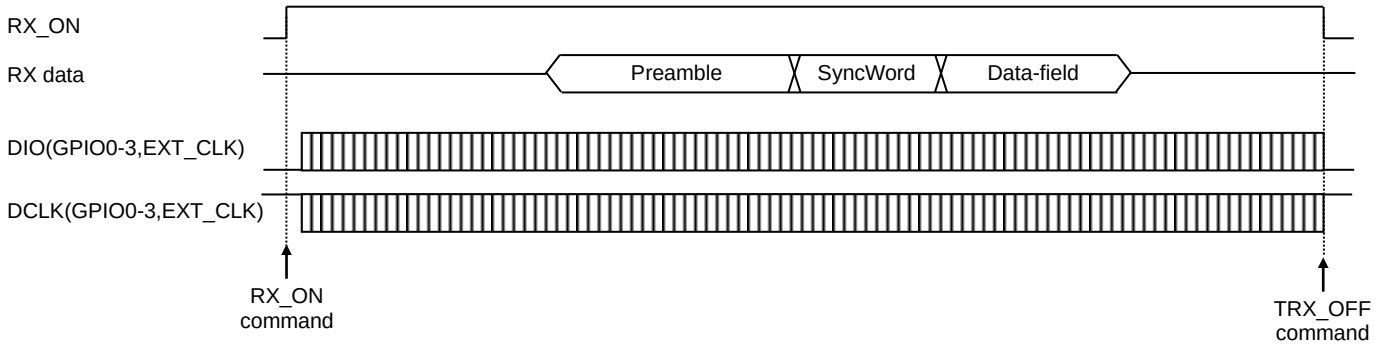
Preamble can be set by PB_PAT([DATA_SET1: B0 0x07(7)] and TXPR_LEN[15:0] ([TXPR_LEN_H/L: B0 0x42/43]). SyncWord can be set by SYNCWORD_SEL([DATA_SET2: B0 0x08(4)), SYNCWORD_LEN[5:0] ([SYNC_WORD_ LEN: 1 0x25(5-0)]), SYNC_WORD_EN* ([SYNC_WORD_EN: B1 0x26(3-0)]), SYNC_WORD1[31:0] ([SYNCWORD1_ SET3/2/1/0: B1 0x27/28/29/2A]), SYNC_WORD2[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E]).

[RX]

i) Continuous output mode (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b01.

After RX_ON(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) = 0x6), DCLK is output continuously. RX data (demodulated data) is output from DIO pin at falling edge of DCLK. RX data is not stored in RX_FIFO.



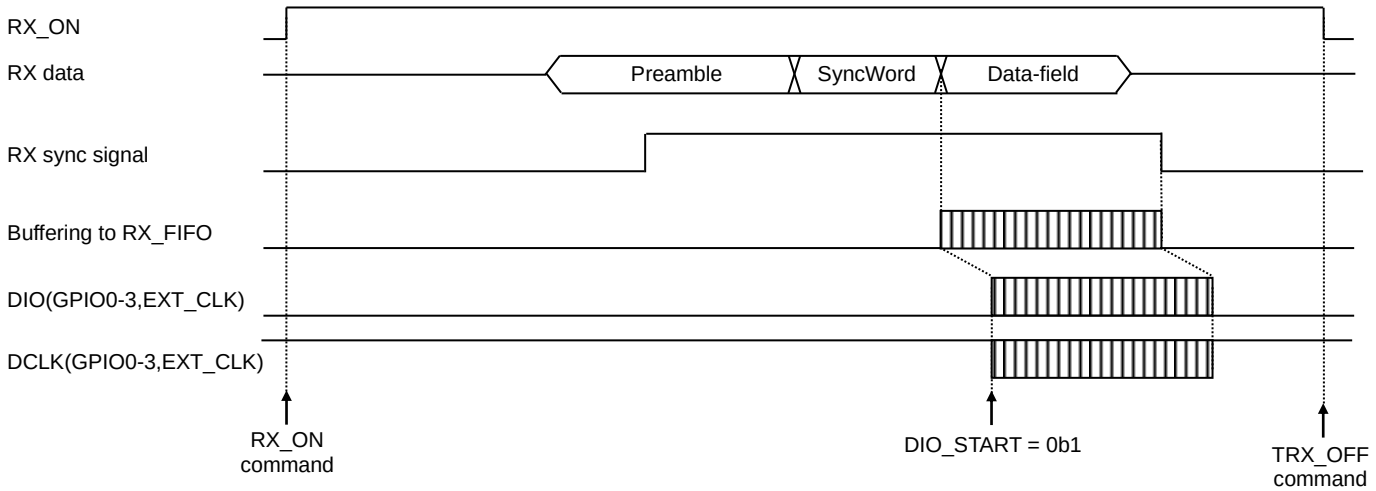
(Note)

For details of timing, please refer to the “RX” in the “Timing Chart”.

ii) Data output mode 1 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

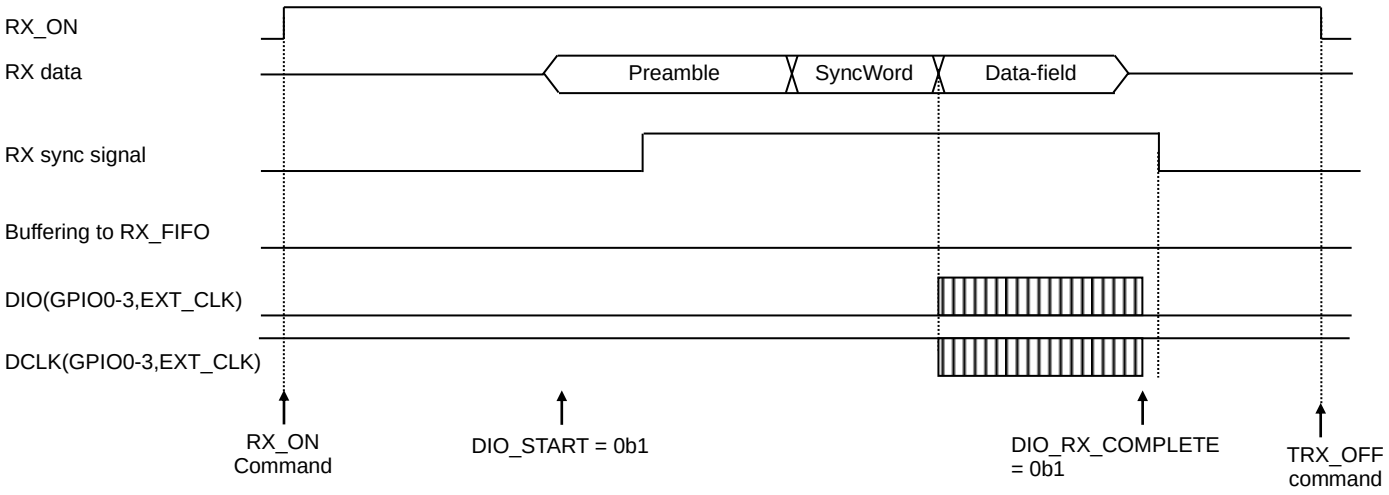
After SyncWord detection, RX data is buffered in RX_FIFO. RX data buffering will continue until RX sync signal (SYNC) becomes “L”. By setting DIO_START ([DIO_SET: B0 0x0C(0)]) = 0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK). However, if DIO_START setting is done after 64byte timing, the top byte will be over written. If all buffered data is output until SYNC becomes “L”, RX completion interrupt (INT[8] group 2) will be generated. After RX completion, ready to receive next packet.



(Note)

1. RX data buffering in RX_FIFO is accessed byte by byte. DIO_START should be issued after 1byte access time upon SyncWord detection.
2. This mode does not process L-field. Field checking function is not supported.

If DIO_START is issued before SyncWord detection, data is not buffered in RX_FIFO and RX data after SyncWord detection will be output at falling edge of DCLK . In order to complete RX before SYNC becomes “L”, DIO RX completion setting (DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)] = 0b1) is necessary. After DIO_RX_COMPLETE setting, ready to receive the next packet.

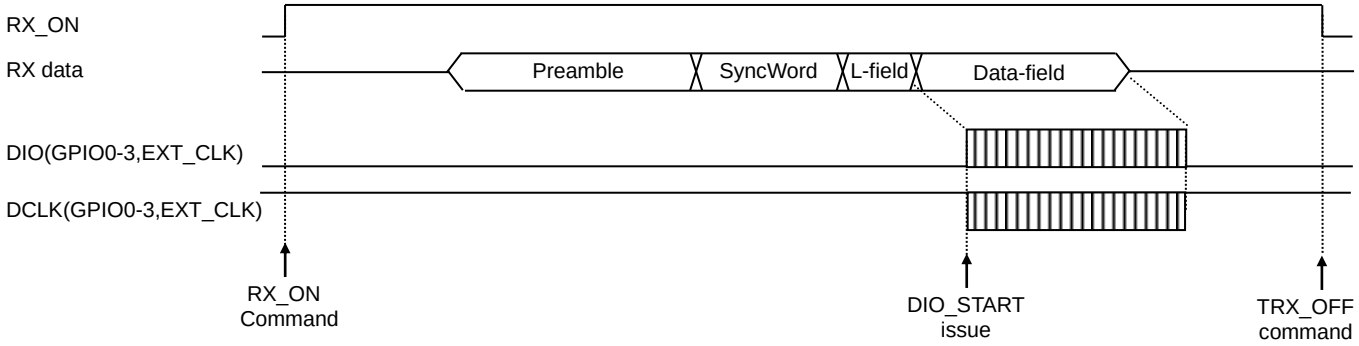


iii) Data output mode 2 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b11.

Only Data-field of RX data is buffered in RX_FIFO. RX data indicated by L-field is stored in RX_FIFO. By DIO_START([DIO_SET: B0 0x0C(0)]) = 0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK).

However, if DIO_START setting is done after 64byte timing, the top byte will be overwritten. If all data indicated by L-field is output, RX completion interrupt (INT[8] group2) will be generated. After RX completion, ready to receive next packet. Length information is stored in [RX_PKT_LEN_H/L: B0 0x7D/7E] registers. This mode support fileld check function.



(Note)

RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after elapsed time from SyncWord detection to L-field length + over 1byte access time.

(2) In case of using SDI/SDO pin (sharing with SPI interface)

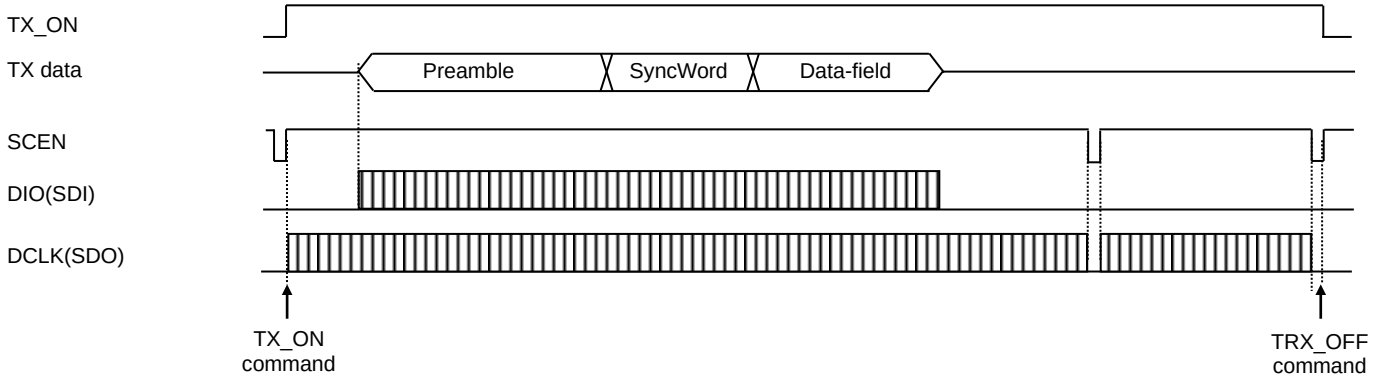
If SDI and SDO pins are used for input/output of transmission data, DCLK/DIO is controlled as follow. (below DIO/DCLK vertical line part indicate output or input.) Both SDO_CFG and SDI_CFG ([SPI/EXT_PA_CTRL:B0 0x53 (5,4)]) should be set 0b1. For operation of LSI about each DIO modes, please refer to the previous chapter "(1)In case of using GPIO*, EXT_CLK pins".

[TX]

i) Continuous input mode (from host)

Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) = 0b01

After TX_ON(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) = 0x9), during SCEN pin is "H", DCLK is output from SDO pin. TX data can be input from SDI pin at falling edge of DCLK. TX data must be encoded data. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) = 0x8), input data from DIO pin are not valid. During DCLK output, if SCEN pin becomes "L", DCLK output will stop. (SPI access has priority)



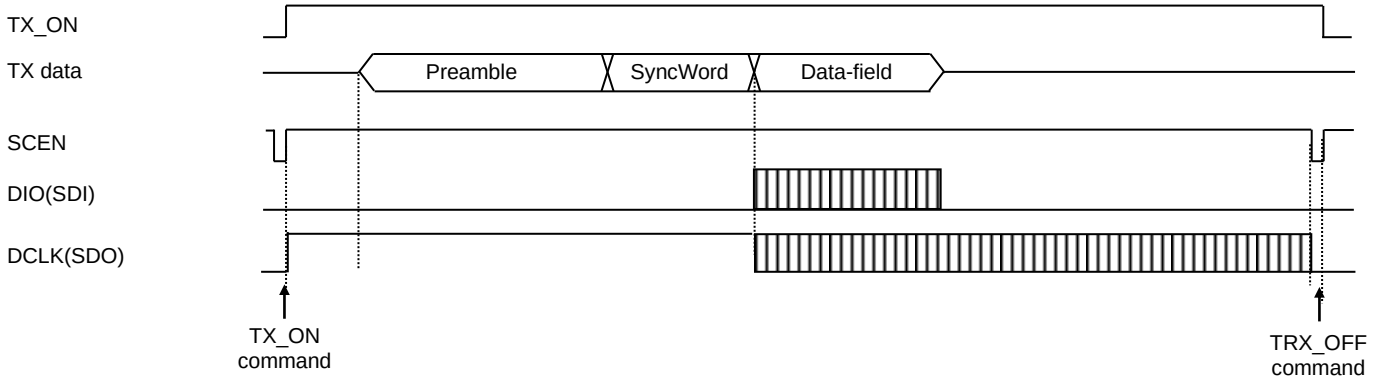
(Note)

Not to access SPI until TX completion. During packet transmission, if SPI access is attempted by the host, TX data error can be expected.

ii) Data input mode (from host)

Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) = 0b10.

After TX_ON, when SCEN is "H", DCLK is output from SDO pin during data input period after SyncWord. At falling edge of DCLK, TX data should be input to SDI from the host. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) = 0x8), TX data/clock input/output are invalid. During DCLK output period, if SCEN becomes "L", DCLK output will stop. (SPI access has a priority)



(Note)

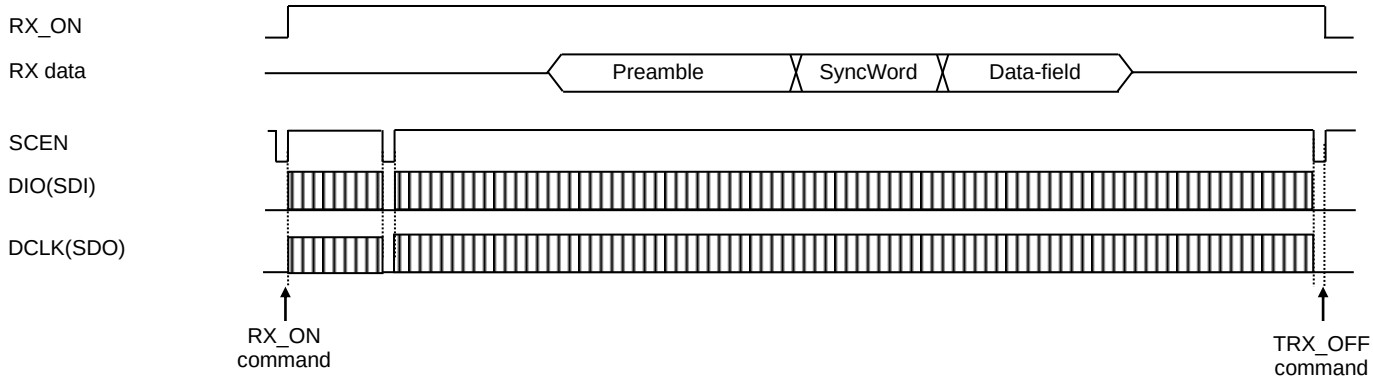
Not to access SPI until TX completion. During packet transmission, if SPI access is attempted by the host, TX data error can be expected.

[RX]

i) Continuous output mode (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b01.

After RX_ON (SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)]) = 0x6) issued, during SCEN is “H” period, DCLK is output from SDO pin, RX data is output from SDI pin at falling edge of DCLK. After TRX_OFF issuing(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) = 0x8), DCLK/DIO output will stop. Even if DCLK/DIO are output, when SCEN becomes “L”, DCLK/DIO will stop. (SPI access has a higher priority)



(Note)

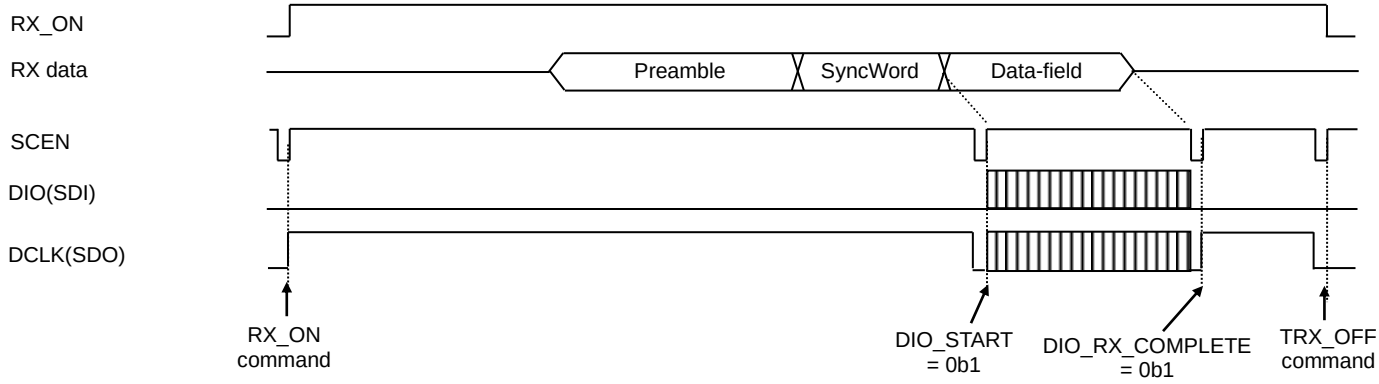
Not to access SPI until RX completion. During packet receiption, if SPI access is attemped by the host, RX data error can be expected. It is recommended

ii) Data ouput mode 1 or data output mode 2 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) = 0b10/11

After RX_ON, RX data upon SyncWord (output mode 1) or RX data upon L-fileld (output mode 2) is buffered in RX_FIFO. During SCEN is “H”, by DIO_START([DIO_SET: B0 0x0C(0)]) = 0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK). Other output condition is same as the case of using GPIO*/ECT_CLK pins. After TRX_OFF isuing, DCLK/DIO output will stop. Even during DCLK/DIO are output period, if SCEN becomes “L”, DCLK/DIO output will stop. (SPI access has a priority)

(In case of data output mode1)



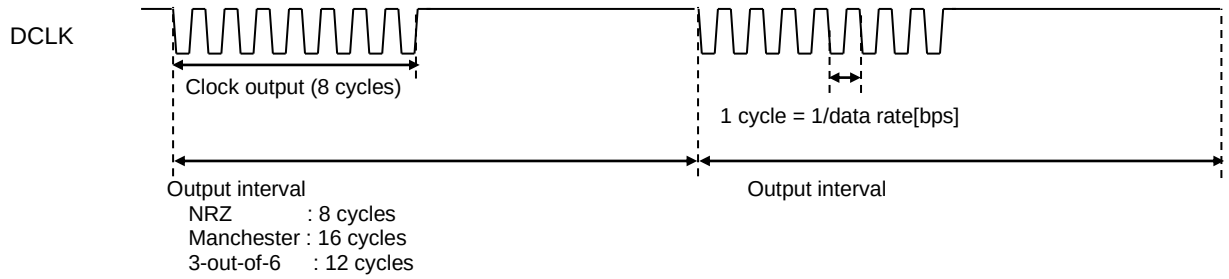
(Note)

Not to access SPI until RX completion. During packet receiption, if SPI access is attemped by the host, RX data error can be expected.

(3) DCLK output

The DCLK output depends on the DIO mode setting.

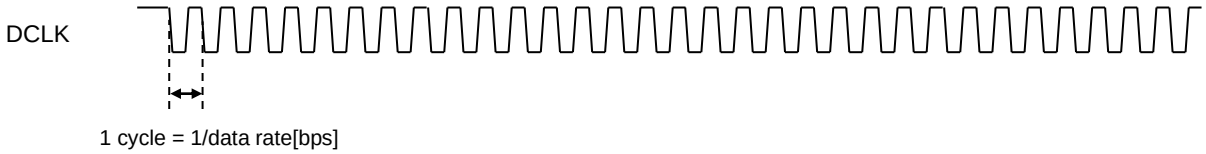
i) Data output mode 2 (RXDIO_CTRL([DIO_SET: 0x0C(7-6)]) = 0b11)
In this mode, decoded data is output. The DCLK output section in an output interval varies depending on the encoding. DCLK output section is as follows.



NRZ : 8 cycles
Manchester : 16 cycles
3-out-of-6 : 12 cycles

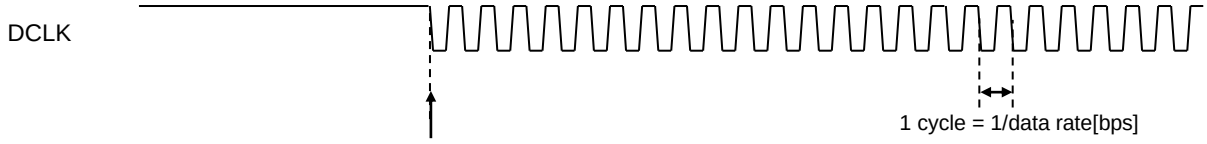
ii) Mode other than i) (RX continuous output mode/data output mode 1, TX continuous input mode/data input mode)
In this mode, undecoded data is input or output. DCLK is output continuously. It does not depend on the encoding.

TX continuous input mode or RX continuous mode



(Note) The nuber of cycle per 1byte
NRZ : 8 cycles
Manchester : 16 cycles
3-out-of-6 : 12 cycles

TX Data input mode / RX Data output mode 1



TX: The timing during transmitting the last 2bits SyncWord
RX: DIO_START issue

(Note) The nuber of cycle per 1byte
NRZ : 8 cycles
Manchester : 16 cycles
3-out-of-6 : 12 cycles

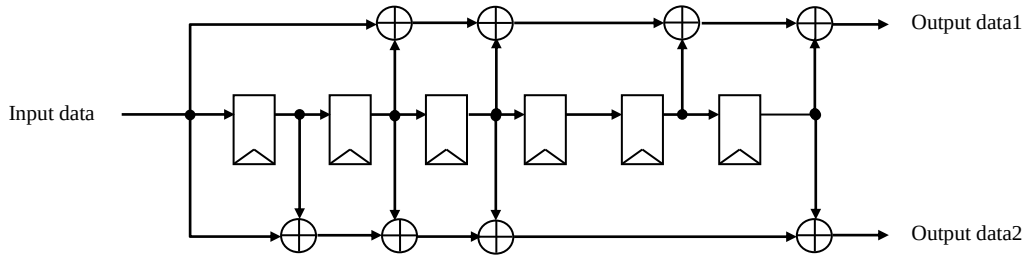
○FEC(Forward Error Correction) function

ML7404 supports FEC function in conformity with IEEE802.15.4k and the Interleaver with Pruned bit reversal interleaving algorithm. The generating polynomial is as follows.

Generating Polynomial: $G_0 = 1 + x^2 + x^3 + x^5 + x^6$

$G_1 = 1 + x + x^2 + x^3 + x^6$

Encoding ate: 1/2



※⊕ : this means EX-OR

FEC Encoder circuits

FEC function registers are as follows:

Function	Register
FEC enable setting	FEC_EN([DSSS_CTRL: B7 0x01(1)])
Interleaver enable setting	INTLV_EN([FEC_ENC_CTRL: B7 0x03(0)])
FEC encoder initilal status select setting	ENC_INIT_SEL([FEC_ENC_CTRL: B7 0x03(1)])
FEC encoder byte transmission order setting	ENC_BYTE_MSB([FEC_ENC_CTRL: B7 0x03(2)])
FEC encoder bit transmission order setting	ENC_BIT_MSB([FEC_ENC_CTRL: B7 0x03(3)])
Interleaver bytetransmission order setting	INTLV_BYTE_MSB([FEC_ENC_CTRL: B7 0x03(4)])
De-interleaverenable setting	DEINTLV_EN([FEC_DEC_CTRL: B7 0x03(0)])
FEC decoder initilaldecode select setting	DEC_INIT_SEL([FEC_DEC_CTRL: B7 0x03(1)])
FEC decoder data transmission order setting	DEC_BYTE_MSB([FEC_DEC_CTRL: B7 0x03(2)])
FEC decoder data input order setting	DEC_BIT_MSB([FEC_DEC_CTRL: B7 0x03(3)])
De-interleaver data output order setting	DEINTLV_BYTE_MSB([FEC_DEC_CTRL: B7 0x03(4)])

(Note)
FEC function supports only in case PSDU is 16 or 24 or 32 byte.

●Timer Function

○Wake-up timer

ML7404 has automatic wake-up function using wake-up timer. The following operations are possible by using wake-up timer.

- Upon timer completion, automatically wake-up from SLEEP state. After wake-up operation can be selected as RX_ON state or TX_ON state by WAKEUP_MODE ([SLEEP/WU_SET: B0 0x2D(6)]).
- By setting WUT_1SHOT_MODE ([SLEEP/WU_SET: B0 0x2D(7)]), continuous wake-up operation (interval operation) or one shot operation can be selected.
- In interval operation, if RX_ON /TX_ON state is caused by wake-up timer, continuous operation timer is in operation..
- After moving to RX_ON state by wake-up timer, when continuous operation timer is completed, move to SLEEP state automatically. However, if SyncWord is detected before timer completion, RX_ON state will be maintained. In this case, ML7404 does not go back to SLEEP state automatically. SLEEPsetting (SLEEP_EN[SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) is necessary to go back to SLEEP state. However if RXDONE_ MODE[1:0]([RF_STATUS_CTRL:B0 0x0A(3-2)]) = 0b11, after RX completion, move to SLEEP state automatically.
  The judgment timing whether continue RX is selected in SyncWord detection, Field check detection or synchronization detection by RCV_CONT_SEL([M_CHECK_CTRL: B0 0x1C(5:4)]) after continuous operation timer completion.
- After moving to TX_ON state by wake-up timer, when continuous operation timer completed, ML7404 does not go back to SLEEPstate automatically. SLEEPsetting (SLEEP_EN[SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) is necessary to go back to SLEEP state.
- After wake-up by combining with high speed carrier checking mode, CCA is automatically performed, if IDLE is detected, able to move to SLEEP state immediately. For details, please refer to the "(3) high speed carrier detection mode".
- By setting WUT_CLK_SOURCE ([SLEEP/WU_SET:B0 0x2D(2)]), clock source for wake-up timer are selectable from EXT_CLK pin or on-chip RC OSC.

Wake-up intervalm, wake-up timer interval and continuous operation timer can be calculated in the following formula.

Wake-up interval [s] = Wake-up timer interval [s] + Continuous operation timer [s]

Wake-uptimer interval [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) *
(Wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) + 1)

Continuous operation timer [s] = Wake-up timer clock cycle *
Division setting([WUT_CLK_SET: B0 0x2E(7-4)]) *
(Continuous operation timer setting ([WU_DURATION: B0 0x31]) – 1)

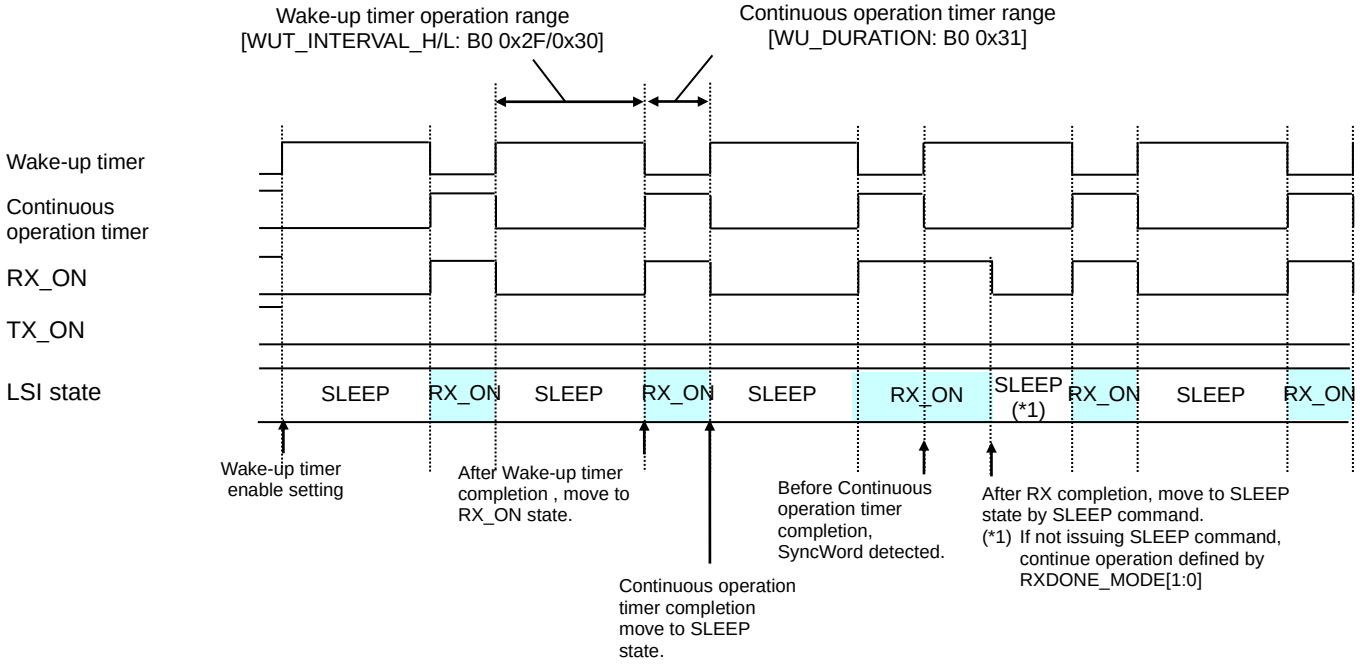
(Note)

1. In case of transition to TX_ON state after wake-up, when the timer expires during transmission, this is judged that transmission is going on, and transmission will be continued. After transmission is completed, RF state transition will be executed according to the setting of TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)]).
2. WUDT_CLK_SET[3:0] ([WUT_CLK_SET: B0 0x2E(7-4)]) and WUT_CLK_SET[3:0] ([WUT_CLK_SET: B0 0x2E (3-0)]) can be set independently. In case of using continuous operation timer, please set the same value as WUDT_CLK_SET as WUT_CLK_SET.
3. Minimum value for wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is 0x02. And minimum value for continuous operation timer setting ([WU_DURATION: B0 0x31]) is 0x01. Be sure to set the timer value of the continuous operation timer in such a manner that the timer expires after notification of the clock stabilization interrupt (INT[0]([INT_SOURCE_GRP1: B0 0x0D(0)])).
4. Be noted that the SyncWord detection is not issued when in DIO mode with RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) = 0b01. Therefore, when continuous operation timer completed, forcibly move to SLEEP state.
5. Though the state of ML7404 autonomously changes to SLEEP due to timer operation, if the timings of the change to SLEEP state and SPI access are the same, SPI access will be disabled. Control the timings of SLEEP transition and SPI access to avoid timing conflict.

(1) Interval operation

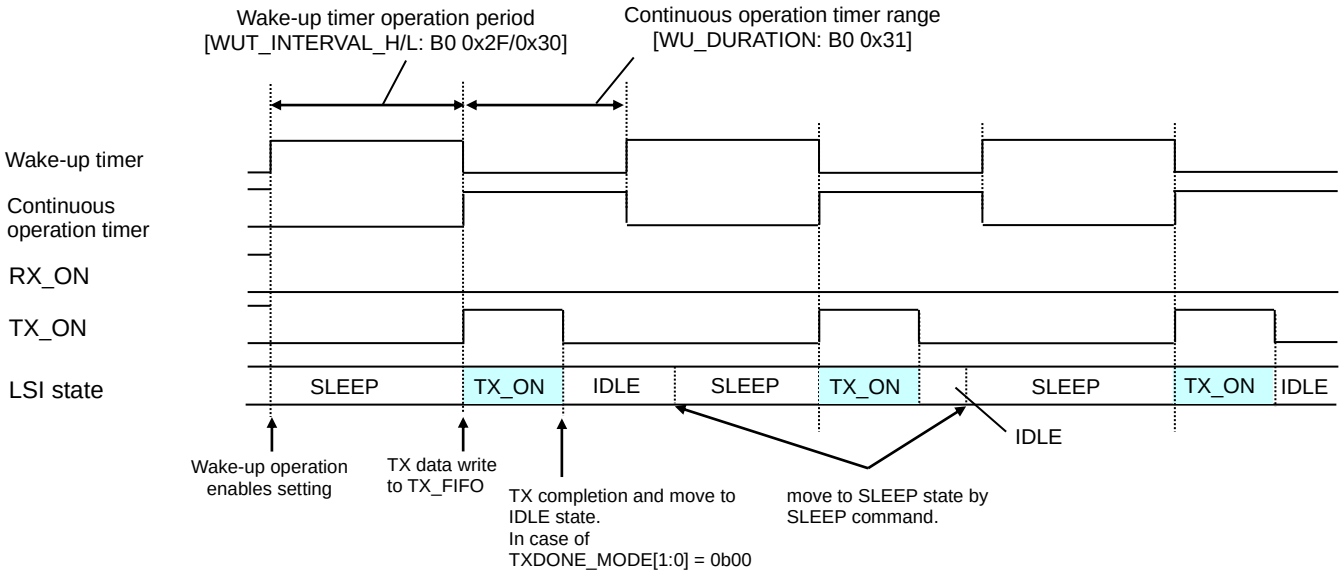
[RX]
After wake-up, RX_ON state. If continuous operation timer completed before SyncWord detection, automatically return to SLEEP state. If SyncWord detected, continue RX_ON. After RX completion, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) .

[SLEEP/WU_SET: B0 0x2D(6-4)] = 0b011



[TX]
After wake-up, TX_ON state. After TX completion, continue operation defined by TXDONE_MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(1-0)]) .
Even if continuous operation timer completed, ML7404 does not return to SLEEP state automatically. So SLEEP setting (SLEEP_EN[SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) is necessary to go back to SLEEP state.

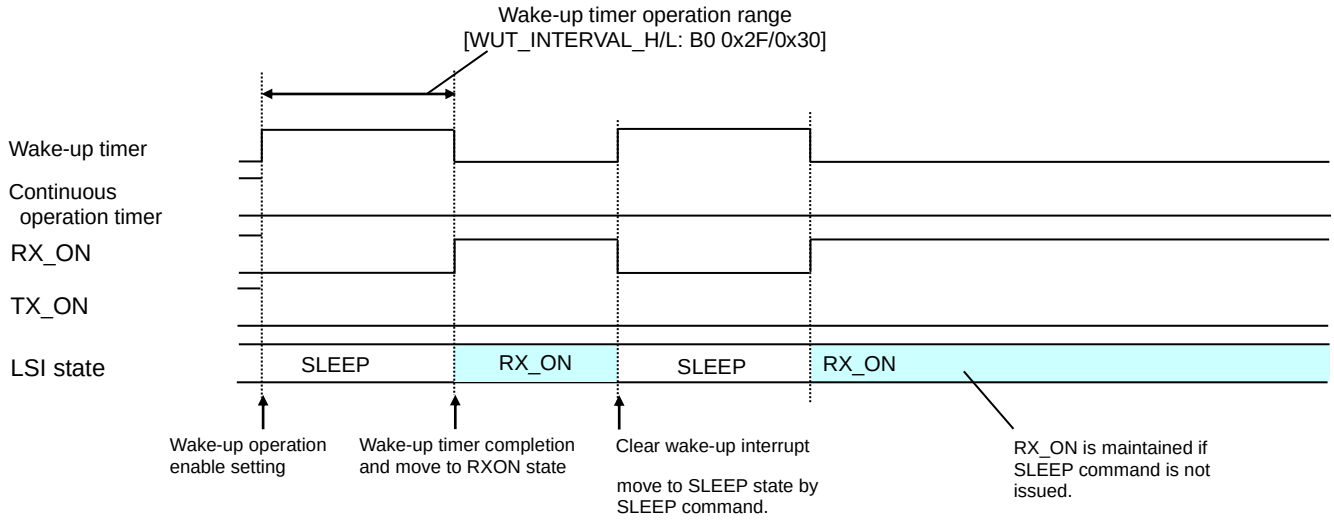
[SLEEP/WU_SET: B0 0x2D(6-4)] = 0b111



(2) 1 shot operation

[RX]
After wake-up timer completion, move to RX_ON state. And continue RX_ON state. Move to SLEEP state by SLEEP command. If wake-up timer interval ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is maintained, after re-issuing SLEEP command, 1 shot operation will be activated again. Also, clear the wake-up interrupt ([INT_SOURCE_GRP1: B0 0x0D(6)]) before moving to SLEEP state. If RX completed during RX_ON, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) . Same manner in TX_ON state.

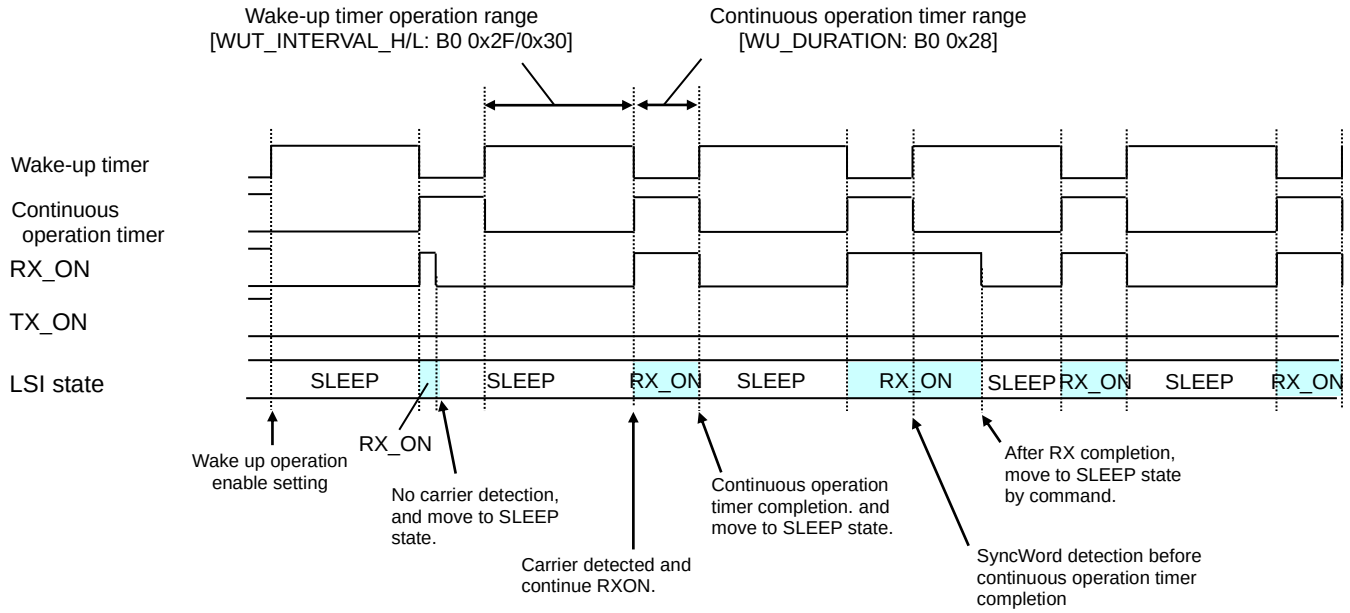
[SLEEP/WU_SET: B0 0x2D(7-4)] = 0b1001



(3) Combination with high speed carrier detection

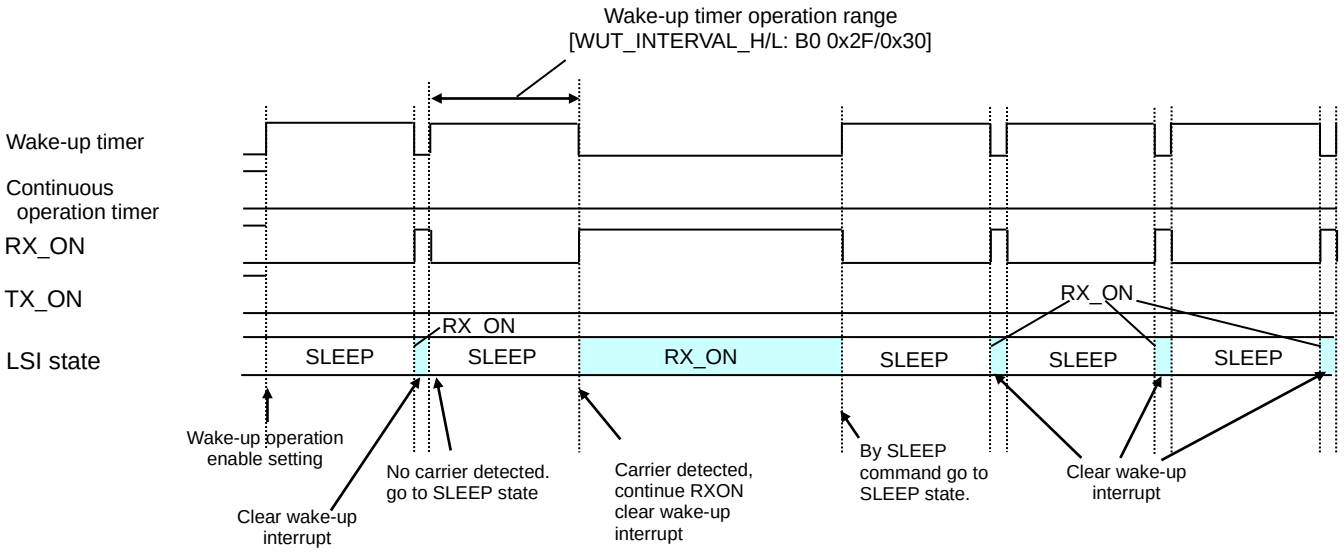
[Interval operation]
After wake-up timer completion, move to RX_ON state. Then perform CCA. If no carrier is detected, automatically move to SLEEP state. If carrier detected, maintaining RX_ON state and perform SuncWord detection. If continuous operation timer completed before SyncWord detection, automatically move to SLEEP state. And If SyncWord detected, continue RX_ON state state.

[SLEEP/WU_SET: B0 0x2D(7-4)] = 0b0011
FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)]) = 0b1



[1 shot operation]
After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier detected, go back to SLEEP state automatically. In case of no carrier detection, if periodic waking up at wake-up timer interval is necessary, clear the wake-up interrupt ([INT_SOURCE_GRP1: B0 0x0D(6)]) before moving to SLEEP state.
If carrier is detected, continue RX state. Able to go back to SLEEP by setting SLEEP parameters.

[SLEEP/WU_SET: B0 0x2D(7-4)] = 0b1001
FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)]) = 0b1



○General purpose timer

ML7404 has general purpose timer. 2 channel of timer are able to function independently. Clock sources, timer setting can be programmed independently. This timer is 1-shot operation. When timer is completed, General purpose timer 1 interrupt (INT[22] group3) or General purpose timer 2 interrupt (INT[23] group3) will be generated.

General timer interval can be programmed as the following formula.

General purpose timer interval[s] = general purpose timer clock cycle *
Division setting ([GT_CLK_SET: B0 0x33]) *
General purpose timer interval setting ([GT1_TIMER: B0 0x34] or [GT2_TIMER: B0 0x35])

By setting GT2/1_CLK_SOURCE ([GT_SET: B0 0x32(5,1)]), clock sources for general purpose timer can be selectable from wake-up timer clock or 2MHz.

●Frequency Setting Function

○Channel frequency setting

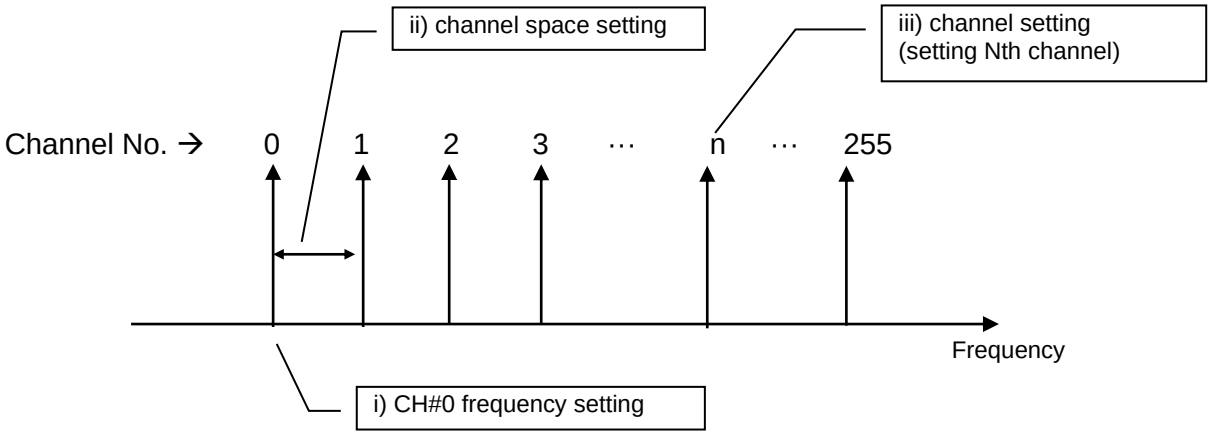
Maximum 256 channels can be selected (CH#0 to CH#255) by the following registers.

Frequency		Register
CH#0 frequency	TX	[TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]
	RX	[RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22]
Channel spacing	-	[CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24]
Channel setting	-	[CH_SET: B0 0x09]
PLL dividing setting	-	[PLL_DIV_SET: B1 0x1A]

[Channel frequency setting]
Using above registers, channel frequency is defined as following formula.

Channel frequency = i) CH#0 frequency + ii) channel space * iii) channel setting

[Channel frequency allocation image]



Set the PLL dividing setting according to the RF frequency (for each frequency band) as shown below.

PLL dividing setting [PLL_DIV_SET: B1 0x1A]	
315 to 510MHz band	900MHz band
0x02 (divided by 2)	0x00 (divided by 1)

(Note)

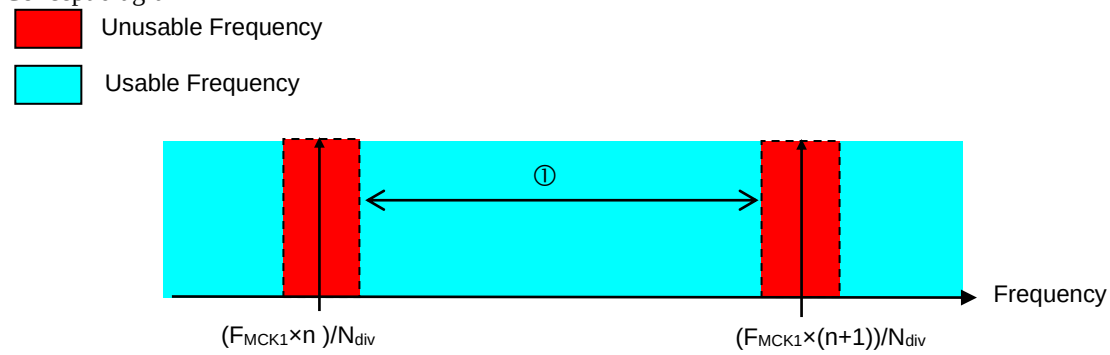
1) The channel frequency must satisfy the following conditions. If cannot do it, change channel #0 frequency or use other channels because PLL may not be locked.

F_{MCK1}: Master clock frequency

N_{div} = 1 or 2 : PLL_MODE ([PLL_DIV_SET: B1 0x1A (1-0)])

(F_{MCK1}*n + 1MHz) / N_{div} ≤ Used channel frequency ≤ (F_{MCK1}*(n+1) - 1MHz) / N_{div} (Note) n = integer

Concept diagram



(Example of calculating range ① shown above)
For 1 division mode (N_{div} = 1), Master clock 36MHz, n = 25

(36MHz×25+1)MHz ≤ Channel frequency to be used ≤ (36MHz×(25+1)-1)

⇒901MHz ≤ Channel frequency to be used ≤ 935MHz

2) "CH#0 frequency [Hz]" and "channel spacing [Hz]" may have error [Hz]. Then the "channel frequency error [Hz]" is defined as following formula.

Channel frequency error [Hz] = CH#0 frequency error [Hz] + channel spacing error [Hz]* channel setting

When changing "channel frequency" by setting "channel setting" without "CH#0 frequency" change, the "channel frequency error" will become larger than by setting both "CH#0 frequency" and "channel setting". If the "channel frequency error" is larger than expectation, please consider to change "CH#0 frequency".

3) If the 26-bit channel frequency (= CH#0 frequency + Channel spacing × Channel setting) setting value (integer and decimal parts, refer to "Channel #0 frequency setting") exceeds the maximum value 0x3FF_FFFF, the expected channel frequency is not achieved. Take this maximum value into account when deciding the channel #0 frequency, channel spacing, and channel setting.

(1) Channel #0 frequency setting

TX frequency can be set by [TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]. RX frequency can be set by [RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22].

For details of N_{div}, please refer to the "Channel frequency setting".

Channel #0 frequency setting value can be caluculated using the following formula.

$$I = \frac{f_{rf}}{f_{ref} / N_{div}} \quad \text{(Integer part)}$$

$$F = \left\{ \frac{f_{rf}}{f_{ref} / N_{div}} - I \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

f_{rf} :Channel #0 frequency

f_{ref} :PLL reference frequency (= master clock frequency: F_{MCK1})

I :Integer part of frequency setting

F :Fractional part of frequency setting

N_{div} :PLL dividing setting (1 or 2)

I (Hex) is set to [TXFREQ_I: B1 0x1B], [RXFREQ_I: B1 0x1F] registers.

F (Hex.) is set to the following registers.

For TX, from MSB, set in order of [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D], [TXFREQ_FL: B1 0x1E] registers.

For RX, from MSB, set in order of [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21], [RXFREQ_FL: B1 0x22] registers.

Frequency error (f_{err}) is calculated as follows :

$$f_{err} = \left\{ I + \frac{F}{2^{20}} \right\} \cdot (f_{ref} / N_{div}) - f_{rf}$$

[Example]

When set TX channel #0 frequency(f_{rf}) to 920MHz (master clock 36MHz, N_{div}=1), the calculations are as follows.

$$I = \frac{920MHz}{(36MHz/1)} \text{ (Integer part) } = 25(0x19)$$

$$F = \left\{ \frac{920MHz}{(36MHz/1)} - 25 \right\} \cdot 2^{20} \text{ (Integer part) } = 582542(0x8E38E)$$

[TXFREQ_I: B1 0x1B] = 0x19
[TXFREQ _FH: B1 0x1C] = 0x08
[TXFREQ _FM: B1 0x1D] = 0xE3
[TXFREQ _FL: B1 0x1E] = 0x8E

Frequency error f_{err} is as follows:

$$f_{err} = \left\{ 25 + \frac{582542}{2^{20}} \right\} \cdot (36MHz/1) - 920MHz = 0Hz$$

(2) Channel space setting

Channel space can be set by [CH_SPACE_H: B1 0x23], [CH_SPACE_L: B1 0x24] registers. Hexadecimal values calculated in the following formula should be set to [CH_SPACE_H: B1 0x23], [CH_SPACE_L: B1 0x24] registers. (MSB->LSB order) Channel space is from the center frequency of given channel to adjacent channel center frequency.

For details of N_{div}, please refer to the "Channel frequency setting".

Channel space setting value can be calculated using the following formula:

$$CH\_SPACE = \left\{ \frac{f_{sp}}{f_{ref} / N_{div}} \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

CH_SPACE : Channel space setting

f_{sp} : Channel space [MHz]

f_{ref} : PLL reference frequency (= master clock frequency : F_{MCK1})

N_{div} : PLL dividing setting (1 or 2)

[Example]
When set channle space to 400kHz (master clock 36MHz, N_{div}=1), the calculation is as follows.

$$CH\_SPACE = \left\{ \frac{0.4MHz}{36MHz/1} \right\} \cdot 2^{20} \quad \text{(Integer part)} \quad = 11650(0x2D82)$$

[CH_SPACE_H: B1 0x23] = 0x2D
[CH_SPACE_L: B1 0x24] = 0x82

○IF frequency setting

IF frequency is set by [IF_FREQ: B0 0x61]. See the following table for each IF frequency setting value.
Setting can be entered individually for normal reception and for CCA.

IF frequency setting IF_FREQ([IF_FREQ: B0 0x61](2-0) IF_FREQ_CCA([IF_FREQ: B0 0x61(6-4)]	IF frequency(*1)
0b000	225kHz
0b001	150kHz
0b010	prohibited
0b011	112.5kHz
0b100	prohibited
0b101	75kHz
0b110	prohibited
0b111	0kHz

*1 Values are for 36MHz master clock. If use another frequency as master clock, the IF frequency varies depending on the amount of frequency change from 36MHz.

●Modulation Function

○FSK Modulation

ML7404 supports GFSK and FSK modulation.
Please set 0b00 in MOD_TYPE([MOD_CTRL: B6 0x01(1-0)])=0b00 in case of FSK modulation

(1) GFSK modulation setting

By setting GFSK_EN([DATA_SET1: B0 0x07(4)]) = 0b1, GFSK mode can be selected. In GFSK modulation, frequency deviation can be set by [GFSK_DEV_H: B1 0x30] and [GFSK_DEV_L: B1 0x31] registers and the filter coefficient of Gaussian filter can be set by [FSK_DEV0_H/GFIL0: B1 0x32] to [FSK_DEV3_H/GFIL6: B1 0x38] registers. 2FSK/4FSK can be selected by FSK_SEL[DATA_SET2: B0 0x08(5)].

For details of N_{div}, please refer to the "Channel frequency setting".

i) GFSK frequency deviation setting
F_DEV value can be calculated as the following formula:

$$F\_DEV = \left\{ \frac{f_{dev}}{f_{ref} / N_{div}} \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

F_DEV : Frequency deviation setting

f_{dev} : Frequency deviation [MHz]

f_{ref} : PLL reference frequency (= master clock frequency: F_{MCK1})

N_{div} : PLL dividing setting (1 or 2)

In 4GFSK mode, frequency deviation applies to maximum frequency deviation.

[Example]
When set frequency deviation to 50kHz (master clock 36MHz, N_{div}=1), the calculation is as follows.

F_DEV = {0.05MHz ÷ (36MHz/1)} ×2^{20} (Integer value) = 1456 (0x05B0)

In this case, please set [GFSK_FDEV_H/L: B1 0x30/31] as follows,
[GFSK_DEV_H: B1 0x30] = 0x05
[GFSK_DEV_L: B1 0x31] = 0xB0

ii) Gaussian filter setting
GFSK mode can be set by GFSK_EN([DATA_SET1: B0 0x07(4)]) = 0b1.
The BT value of the Gaussian filter can be set by the following registers.

Here is the relationship between the BT value and the register setting.

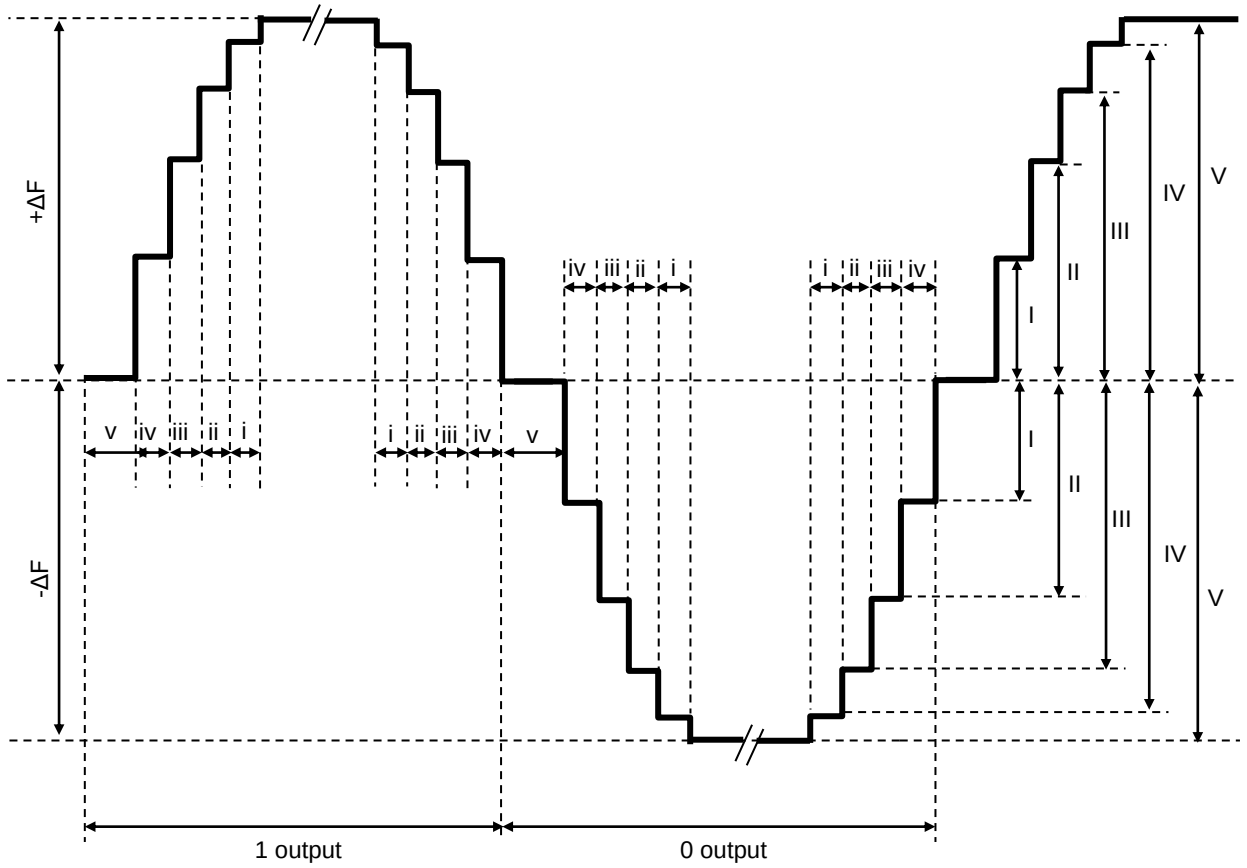
Register	BT value	
	0.5	1.0
[FSK_DEV0_H/GFIL0: B1 0x32]	0x24	0x00
[FSK_DEV0_L/GFIL1: B1 0x33]	0xD6	0x00
[FSK_DEV1_H/GFIL2: B1 0x34]	0x19	0x02
[FSK_DEV1_L/GFIL3: B1 0x35]	0x29	0x0C
[FSK_DEV2_H/GFIL4: B1 0x36]	0x3A	0x31
[FSK_DEV2_L/GFIL5: B1 0x37]	0x48	0x74
[FSK_DEV3_H/GFIL6: B1 0x38]	0x4C	0x9A

(Note)
GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

(2) FSK modulation setting

FSK mode can be set by GFSK_EN([DATA_SET1: B0 0x07(4)]) = 0b0. Also, fine frequency deviation can be set by [FSK_DEV0_H/GFIL0: B1 0x32] to [FSK_DEV4_L: B1 0x3B]. By adjusting [FSK_TIM_ADJ4-0: B1 0x3C-40], FSK timing can be fine tuned. 2FSK/4FSK can be selected by FSK_SEL[DATA_SET2: B0 0x08(5)].

[2FSK]



TX_FSK_POL ([DATA_SET1:B0 0x07(6)]) = 0b0 setting

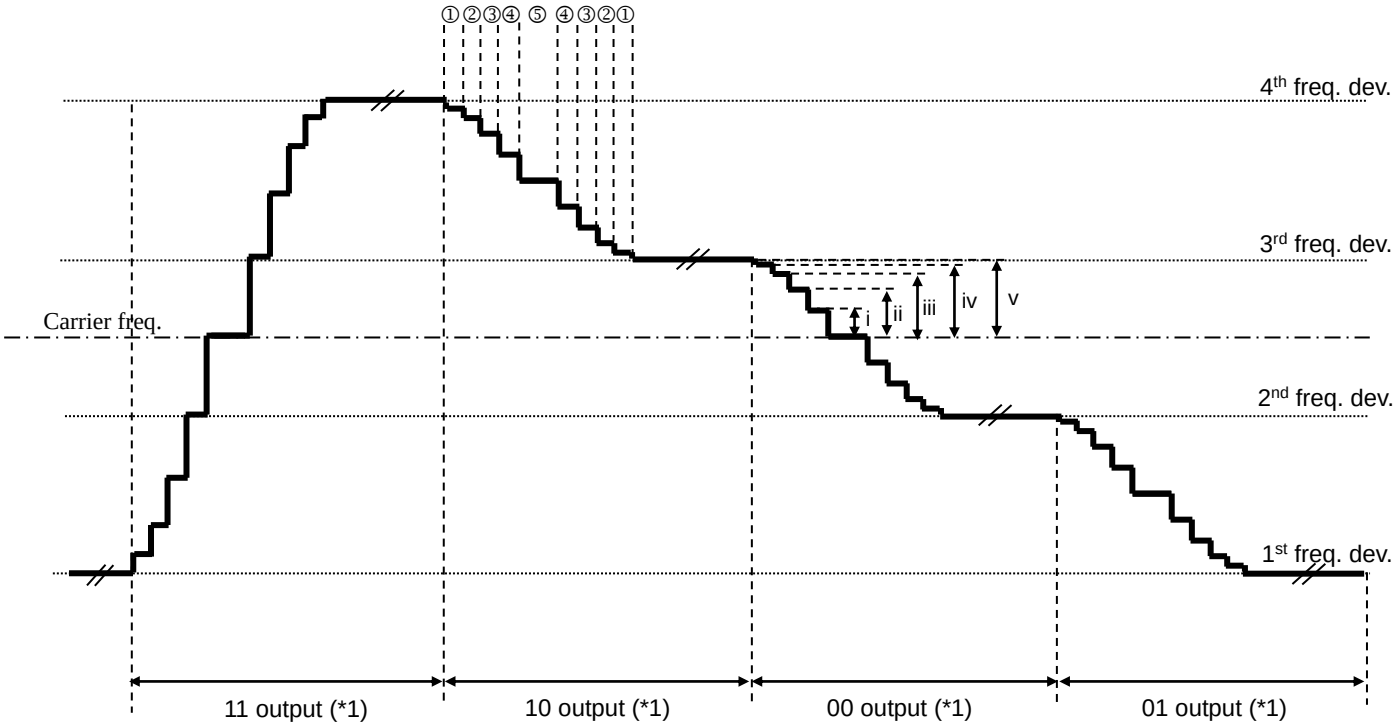
Frequency deviation setting				Timing setting			
symbol	Register name	address	function	symbol	Register name	address	function
I	FSK_FDEV0_H/GFIL0 FSK_FDEV0_L/GFIL1	B1 0x32/33	Frequency deviation Resolution: Approx.34Hz	i	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4MHz/12MHz counter value (*1)
II	FSK_FDEV1_H/GFIL2 FSK_FDEV1_L/GFIL3	B1 0x34/35		ii	FSK_TIM_ADJ3	B1 0x3D	
III	FSK_FDEV2_H/GFIL4 FSK_FDEV2_L/GFIL5	B1 0x36/37		iii	FSK_TIM_ADJ2	B1 0x3E	
IV	FSK_FDEV3_H/GFIL6 FSK_FDEV3_L	B1 0x38/39		iv	FSK_TIM_ADJ1	B1 0x3F	
V	FSK_FDEV4_H FSK_FDEV4_L	B1 0x3A/3B		v	FSK_TIM_ADJ0	B1 0x40	

*1 Modulation timing resolution can be changed by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

(Note)

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

[4FSK]



*1 The mapping of the data (00/01/10/11) for each frequency deviation (1st to 4th) can be changed by [4FSK_DATA_MAP: B1 0x41].

*2 If the frequency is changed by 2 levels such as from 1st to 3rd frequency deviation, the amount of the frequency change is 2 times as much as i to v. If the frequency is changed by 3 levels such as from 1st to 4th frequency deviation, the amount of the frequency change is 3 times as much as i to v.

The table below shows the setting for frequency deviation. Paramete in the expression is name of register.

Frequency deviation setting			
symbol	Register name	address	function
i	FSK_FDEV4 - FSK_FDEV3	B1 0x3A/3B, B1 0x38/39	Frequency deviation Resolution: Approx.34Hz
ii	FSK_FDEV4 - FSK_FDEV2	B1 0x3A/3B, B1 0x36/37	
iii	FSK_FDEV4 - FSK_FDEV1	B1 0x3A/3B, B1 0x34/35	
iv	FSK_FDEV4 - FSK_FDEV0	B1 0x3A/3B, B1 0x32/33	
v	FSK_FDEV4	B1 0x3A/3B	

Timing setting			
symbol	Register name	address	function
①	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4MHz/12MHz counter value (*1)
②	FSK_TIM_ADJ3	B1 0x3D	
③	FSK_TIM_ADJ2	B1 0x3E	
④	FSK_TIM_ADJ1	B1 0x3F	
⑤	FSK_TIM_ADJ0	B1 0x40	

*1 Modulation timing resolution can be changed by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

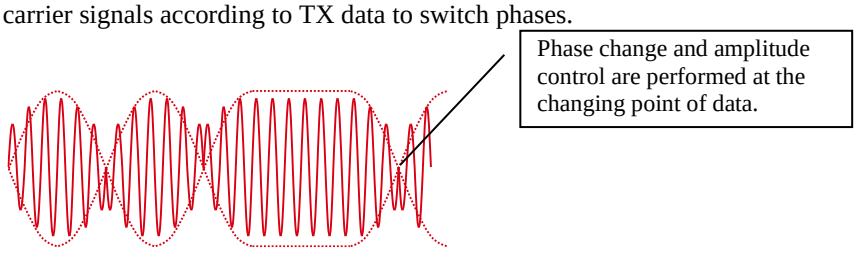
(Note)

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

○BPSK Modulation

ML7404 supports the following two systems for BPSK modulation.

- Phase switch system
  This system switches phases (0°/180°) of carrier signals according to TX data.
- Frequency control system
  This system controls frequencies of carrier signals according to TX data to switch phases.



BPSK modulated waveform (PA output)
Modulation is done by the phase switching and PA control.

The following register setting is required in BPSK mode/PA control setting. Set values described in “Initialization table.”

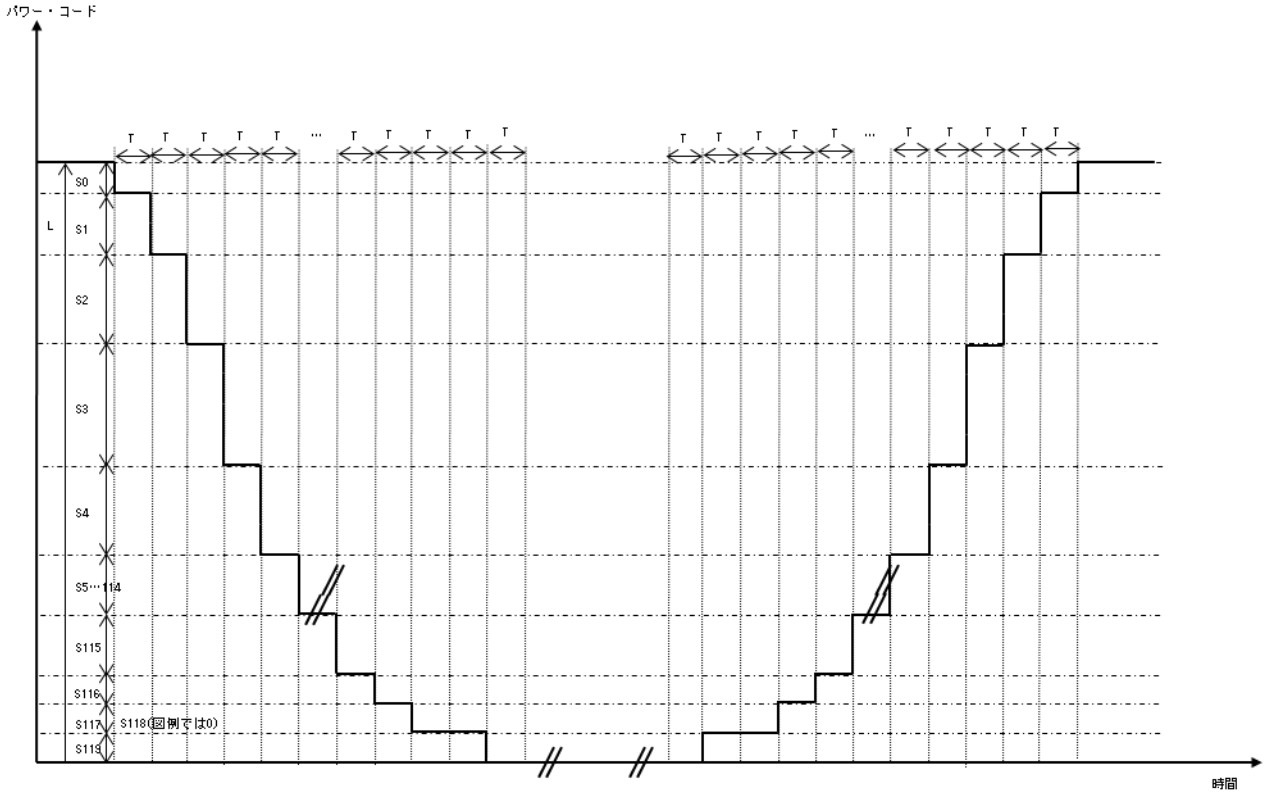
✔: setting required -: setting not required

Bit name	Register name	BPSK scheme	
		Phase switching	Frequency control
MOD_TYPE[1:0]	[MOD_CTRL: B6 0x01(1-0)]	✔(0b01)	✔(0b01)
BPSK_PLL_CTRL	[BPSK_PLL_CTRL: B0 0x7B(0)]	✔(0b0)	✔(0b1)
GFSK_EN	[DATA_SET1: B0 0x07(4)]	✔(0b1)	✔(0b1)
BPSK_P_CLKEL	[BPSK_PLL_CTRL: B6 0x7B(1)]	-	✔
BPSK_P_START[10:0]	[BPSK_P_START_H/L: B6 0x7C(2-0)/7D(7-0)]	-	✔
BPSK_P_HOLD[11:0]	[BPSK_P_HOLD_H/L: B6 0x7E(3-0)/7F(7-0)]	-	✔
BPSK_STEP_EN	[BPSK_STEP_CTRL:B10 0x01(4)]	✔(0b1)	✔(0b1)
BPSK_STEP_SEL	[BPSK_STEP_CTRL:B10 0x01(5)]	✔	✔
BPSK_CLK_SEL	[BPSK_STEP_CTRL:B10 0x01(6)]	✔	✔
BPSK_CLK_SET[8:0]	[BPSK_STEP_CTRL:B10 0x01(0)] [BPSK_STEP_CLK_SET:B10 0x02(7-0)]	✔	✔
STEP0[3:0]-STEP119[3:0]	[BPSK_STEP_SET0:B10 0x04(3-0)] [BPSK_STEP_SET0:B10 0x04(7-4)] … [BPSK_STEP_SET59:B10 0x3F(3-0)] [BPSK_STEP_SET59:B10 0x3F(7-4)]	✔	✔

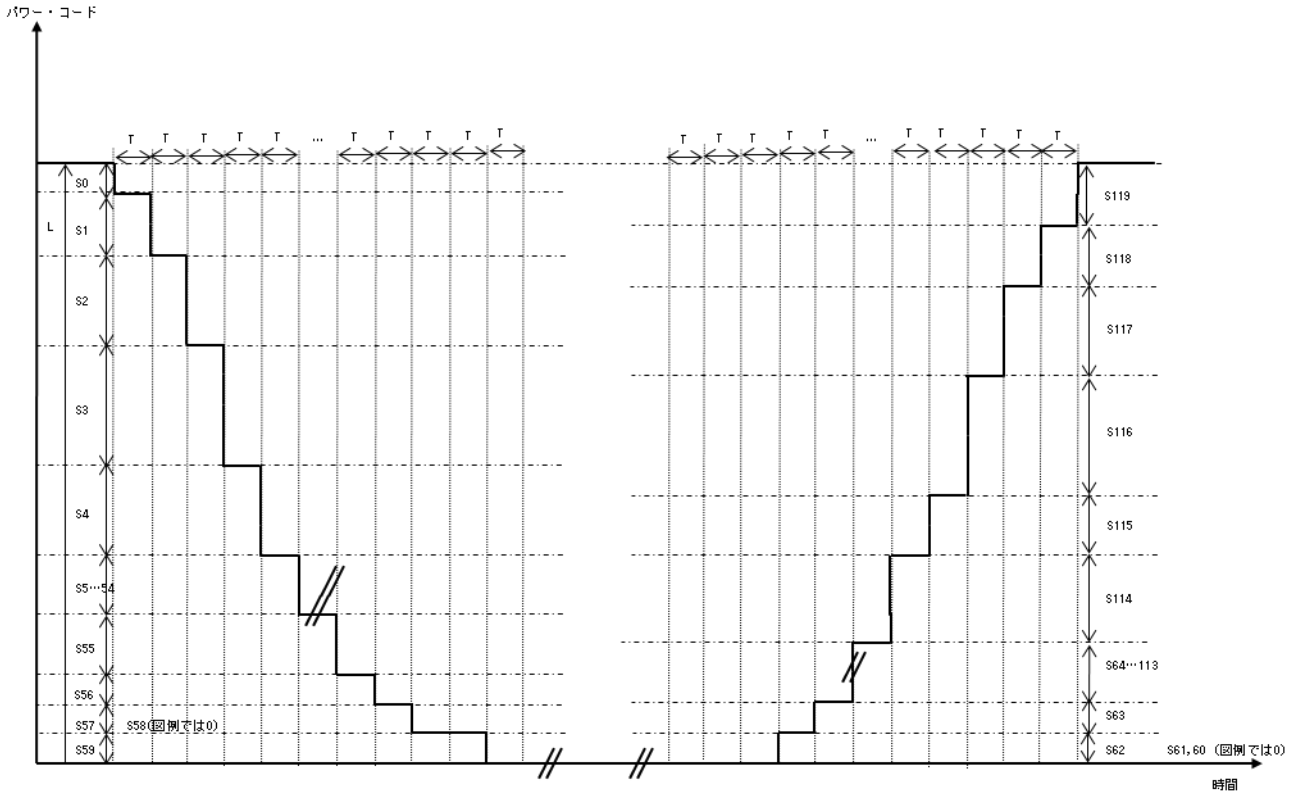
To control high frequency spurious generated when phases or frequencies are switched, transmission output power before and after switch of phases or frequencies is controlled by PA. The following PA control is available for the above two systems.

(i) PA Up-down common setting
(ii) PAUp-down separate setting

(i) PA Up-down common setting (BPSK_STEP_SEL([BPSK_STEP_CTLR: B10 0x01(5)]) = 0b1)



(ii) PAUp-down separate setting (BPSK_STEP_SEL([BPSK_STEP_CTLR: B10 0x01(5)]) = 0b0)



The register for PA control in BPSK is as follows.

Symbol	Bit name	address	function	note
S0	STEP0[3:0]	[B10 0x04(3-0)]	BPSK step control setting0	
S1	STEP1[3:0]	[B10 0x04(7-4)]	BPSK step control setting1	
S2	STEP2[3:0]	[B10 0x05(3-0)]	BPSK step control setting2	
S3	STEP3[3:0]	[B10 0x05(7-4)]	BPSK step control setting3	
S4	STEP4[3:0]	[B10 0x06(3-0)]	BPSK step control setting4	
S5	STEP5[3:0]	[B10 0x06(7-4)]	BPSK step control setting5	
S6	STEP6[3:0]	[B10 0x07(3-0)]	BPSK step control setting6	
S7	STEP7[3:0]	[B10 0x07(7-4)]	BPSK step control setting7	
S8	STEP8[3:0]	[B10 0x08(3-0)]	BPSK step control setting8	
S9	STEP9[3:0]	[B10 0x08(7-4)]	BPSK step control setting9	
S10	STEP10[3:0]	[B10 0x09(3-0)]	BPSK step control setting10	
S11	STEP11[3:0]	[B10 0x09(7-4)]	BPSK step control setting11	
S12	STEP12[3:0]	[B10 0x0A(3-0)]	BPSK step control setting12	
S13	STEP13[3:0]	[B10 0x0A(7-4)]	BPSK step control setting13	
S14	STEP14[3:0]	[B10 0x0B(3-0)]	BPSK step control setting14	
S15	STEP15[3:0]	[B10 0x0B(7-4)]	BPSK step control setting15	
S16	STEP16[3:0]	[B10 0x0C(3-0)]	BPSK step control setting16	
S17	STEP17[3:0]	[B10 0x0C(7-4)]	BPSK step control setting17	
S18	STEP18[3:0]	[B10 0x0D(3-0)]	BPSK step control setting18	
S19	STEP19[3:0]	[B10 0x0D(7-4)]	BPSK step control setting19	
S20	STEP20[3:0]	[B10 0x0E(3-0)]	BPSK step control setting20	
S21	STEP21[3:0]	[B10 0x0E(7-4)]	BPSK step control setting21	
S22	STEP22[3:0]	[B10 0x0F(3-0)]	BPSK step control setting22	
S23	STEP23[3:0]	[B10 0x0F(7-4)]	BPSK step control setting23	
S24	STEP24[3:0]	[B10 0x10(3-0)]	BPSK step control setting24	
S25	STEP25[3:0]	[B10 0x10(7-4)]	BPSK step control setting25	
S26	STEP26[3:0]	[B10 0x11(3-0)]	BPSK step control setting26	
S27	STEP27[3:0]	[B10 0x11(7-4)]	BPSK step control setting27	
S28	STEP28[3:0]	[B10 0x12(3-0)]	BPSK step control setting28	
S29	STEP29[3:0]	[B10 0x12(7-4)]	BPSK step control setting29	
S30	STEP30[3:0]	[B10 0x13(3-0)]	BPSK step control setting30	
S31	STEP31[3:0]	[B10 0x13(7-4)]	BPSK step control setting31	
S32	STEP32[3:0]	[B10 0x14(3-0)]	BPSK step control setting32	
S33	STEP33[3:0]	[B10 0x14(7-4)]	BPSK step control setting33	
S34	STEP34[3:0]	[B10 0x15(3-0)]	BPSK step control setting34	
S35	STEP35[3:0]	[B10 0x15(7-4)]	BPSK step control setting35	
S36	STEP36[3:0]	[B10 0x16(3-0)]	BPSK step control setting36	
S37	STEP37[3:0]	[B10 0x16(7-4)]	BPSK step control setting37	
S38	STEP38[3:0]	[B10 0x17(3-0)]	BPSK step control setting38	
S39	STEP39[3:0]	[B10 0x17(7-4)]	BPSK step control setting39	
S40	STEP40[3:0]	[B10 0x18(3-0)]	BPSK step control setting40	
S41	STEP41[3:0]	[B10 0x18(7-4)]	BPSK step control setting41	
S42	STEP42[3:0]	[B10 0x19(3-0)]	BPSK step control setting42	
S43	STEP43[3:0]	[B10 0x19(7-4)]	BPSK step control setting43	
S44	STEP44[3:0]	[B10 0x1A(3-0)]	BPSK step control setting44	
S45	STEP45[3:0]	[B10 0x1A(7-4)]	BPSK step control setting45	
S46	STEP46[3:0]	[B10 0x1B(3-0)]	BPSK step control setting46	
S47	STEP47[3:0]	[B10 0x1B(7-4)]	BPSK step control setting47	
S48	STEP48[3:0]	[B10 0x1C(3-0)]	BPSK step control setting48	
S49	STEP49[3:0]	[B10 0x1C(7-4)]	BPSK step control setting49	
S50	STEP50[3:0]	[B10 0x1D(3-0)]	BPSK step control setting50	
S51	STEP51[3:0]	[B10 0x1D(7-4)]	BPSK step control setting51	
S52	STEP52[3:0]	[B10 0x1E(3-0)]	BPSK step control setting52	
S53	STEP53[3:0]	[B10 0x1E(7-4)]	BPSK step control setting53	

PA control register (continue)

Symbol	Bit name	address	function	note
S54	STEP54[3:0]	[B10 0x1F(3-0)]	BPSK step control setting54	
S55	STEP55[3:0]	[B10 0x1F(7-4)]	BPSK step control setting55	
S56	STEP56[3:0]	[B10 0x20(3-0)]	BPSK step control setting56	
S57	STEP57[3:0]	[B10 0x20(7-4)]	BPSK step control setting57	
S58	STEP58[3:0]	[B10 0x21(3-0)]	BPSK step control setting58	
S59	STEP59[3:0]	[B10 0x21(7-4)]	BPSK step control setting59	
S60	STEP60[3:0]	[B10 0x22(3-0)]	BPSK step control setting60	
S61	STEP61[3:0]	[B10 0x22(7-4)]	BPSK step control setting61	
S62	STEP62[3:0]	[B10 0x23(3-0)]	BPSK step control setting62	
S63	STEP63[3:0]	[B10 0x23(7-4)]	BPSK step control setting63	
S64	STEP64[3:0]	[B10 0x24(3-0)]	BPSK step control setting64	
S65	STEP65[3:0]	[B10 0x24(7-4)]	BPSK step control setting65	
S66	STEP66[3:0]	[B10 0x25(3-0)]	BPSK step control setting66	
S67	STEP67[3:0]	[B10 0x25(7-4)]	BPSK step control setting67	
S68	STEP68[3:0]	[B10 0x26(3-0)]	BPSK step control setting68	
S69	STEP69[3:0]	[B10 0x26(7-4)]	BPSK step control setting69	
S70	STEP70[3:0]	[B10 0x27(3-0)]	BPSK step control setting70	
S71	STEP71[3:0]	[B10 0x27(7-4)]	BPSK step control setting71	
S72	STEP72[3:0]	[B10 0x28(3-0)]	BPSK step control setting72	
S73	STEP73[3:0]	[B10 0x28(7-4)]	BPSK step control setting73	
S74	STEP74[3:0]	[B10 0x29(3-0)]	BPSK step control setting74	
S75	STEP75[3:0]	[B10 0x29(7-4)]	BPSK step control setting75	
S76	STEP76[3:0]	[B10 0x2A(3-0)]	BPSK step control setting76	
S77	STEP77[3:0]	[B10 0x2A(7-4)]	BPSK step control setting77	
S78	STEP78[3:0]	[B10 0x2B(3-0)]	BPSK step control setting78	
S79	STEP79[3:0]	[B10 0x2B(7-4)]	BPSK step control setting79	
S80	STEP80[3:0]	[B10 0x2C(3-0)]	BPSK step control setting80	
S81	STEP81[3:0]	[B10 0x2C(7-4)]	BPSK step control setting81	
S82	STEP82[3:0]	[B10 0x2D(3-0)]	BPSK step control setting82	
S83	STEP83[3:0]	[B10 0x2D(7-4)]	BPSK step control setting83	
S84	STEP84[3:0]	[B10 0x2E(3-0)]	BPSK step control setting84	
S85	STEP85[3:0]	[B10 0x2E(7-4)]	BPSK step control setting85	
S86	STEP86[3:0]	[B10 0x2F(3-0)]	BPSK step control setting86	
S87	STEP87[3:0]	[B10 0x2F(7-4)]	BPSK step control setting87	
S88	STEP88[3:0]	[B10 0x30(3-0)]	BPSK step control setting88	
S89	STEP89[3:0]	[B10 0x30(7-4)]	BPSK step control setting89	
S90	STEP90[3:0]	[B10 0x31(3-0)]	BPSK step control setting90	
S91	STEP91[3:0]	[B10 0x31(7-4)]	BPSK step control setting91	
S92	STEP92[3:0]	[B10 0x32(3-0)]	BPSK step control setting92	
S93	STEP93[3:0]	[B10 0x32(7-4)]	BPSK step control setting93	
S94	STEP94[3:0]	[B10 0x33(3-0)]	BPSK step control setting94	
S95	STEP95[3:0]	[B10 0x33(7-4)]	BPSK step control setting95	
S96	STEP96[3:0]	[B10 0x34(3-0)]	BPSK step control setting96	
S97	STEP97[3:0]	[B10 0x34(7-4)]	BPSK step control setting97	
S98	STEP98[3:0]	[B10 0x35(3-0)]	BPSK step control setting98	
S99	STEP99[3:0]	[B10 0x35(7-4)]	BPSK step control setting99	
S100	STEP100[3:0]	[B10 0x36(3-0)]	BPSK step control setting100	
S101	STEP101[3:0]	[B10 0x36(7-4)]	BPSK step control setting101	
S102	STEP102[3:0]	[B10 0x37(3-0)]	BPSK step control setting102	
S103	STEP103[3:0]	[B10 0x37(7-4)]	BPSK step control setting103	
S104	STEP104[3:0]	[B10 0x38(3-0)]	BPSK step control setting104	
S105	STEP105[3:0]	[B10 0x38(7-4)]	BPSK step control setting105	
S106	STEP106[3:0]	[B10 0x39(3-0)]	BPSK step control setting106	

PA control register (continue)

Symbol	Bit name	address	function	note
S107	STEP107[3:0]	[B10 0x39(7-4)]	BPSK step control setting107	
S108	STEP108[3:0]	[B10 0x3A(3-0)]	BPSK step control setting108	
S109	STEP109[3:0]	[B10 0x3A(7-4)]	BPSK step control setting109	
S110	STEP110[3:0]	[B10 0x3B(3-0)]	BPSK step control setting110	
S111	STEP111[3:0]	[B10 0x3B(7-4)]	BPSK step control setting111	
S112	STEP112[3:0]	[B10 0x3C(3-0)]	BPSK step control setting112	
S113	STEP113[3:0]	[B10 0x3C(7-4)]	BPSK step control setting113	
S114	STEP114[3:0]	[B10 0x3D(3-0)]	BPSK step control setting114	
S115	STEP115[3:0]	[B10 0x3D(7-4)]	BPSK step control setting115	
S116	STEP116[3:0]	[B10 0x3E(3-0)]	BPSK step control setting116	
S117	STEP117[3:0]	[B10 0x3E(7-4)]	BPSK step control setting117	
S118	STEP118[3:0]	[B10 0x3F(3-0)]	BPSK step control setting118	
S119	STEP119[3:0]	[B10 0x3F(7-4)]	BPSK step control setting119	
T	BPSK_STEP_CLK_SEL	[B10 0x01(5)]	Step control clock select setting 0: master clock frequency / 2 (18MHz) 1: master clock frequency / 4 (9MHz)	Step control clock period = step control clock setting(BPSK_CLK_SEL) * Setting value
	CLK_SET[8:0]	[B0 0x02(0), B0 0x03(7-0)]	Step control clock period setting	
L	PA_REG_ADJ[8:0]	[b0 0x67(0), b0 68(7:0)]	PA regulator output voltage adjustment setting	

●RX Related Function

○AFC function

ML7404 supports AFC function. Frequency deviation (max±20ppm) between remote device and local device can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved. This function can be enabled by setting AFC_EN([AFC/GC_CTRL: B1 0x15(7)]) = 0b1. Note that AFC function to compensate local signals does not work when Spread Spectrum function (DSSS mode) is used.

○Energy detection value (ED value) acquisition function

The ML7404 implements a function to display the received signal strength indicator (RSSI) as the ED value. The ED value can be enabled by setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)]) = 0b1. Calculating for The ED value is automatically started when turned RX_ON state. During RX_ON state, the ED value is constantly updated.
The compensation is adding an offset, multiplying a coefficient and averaging. A number of average times can be specified by ED_AVG([ED_CTRL: B0 0x41(2-0)]). If use diversity function, 2DIV_ED_AVG ([2DIV_MODE: B1 0x48(2-0)]) is available instead of ED_AVG. After the compensation, ED_DONE([ED_CTRL: B0 0x41(4)]) becomes “1” and ED_VALUE ([ED_RSLT: B0 0x3A]) is updated.

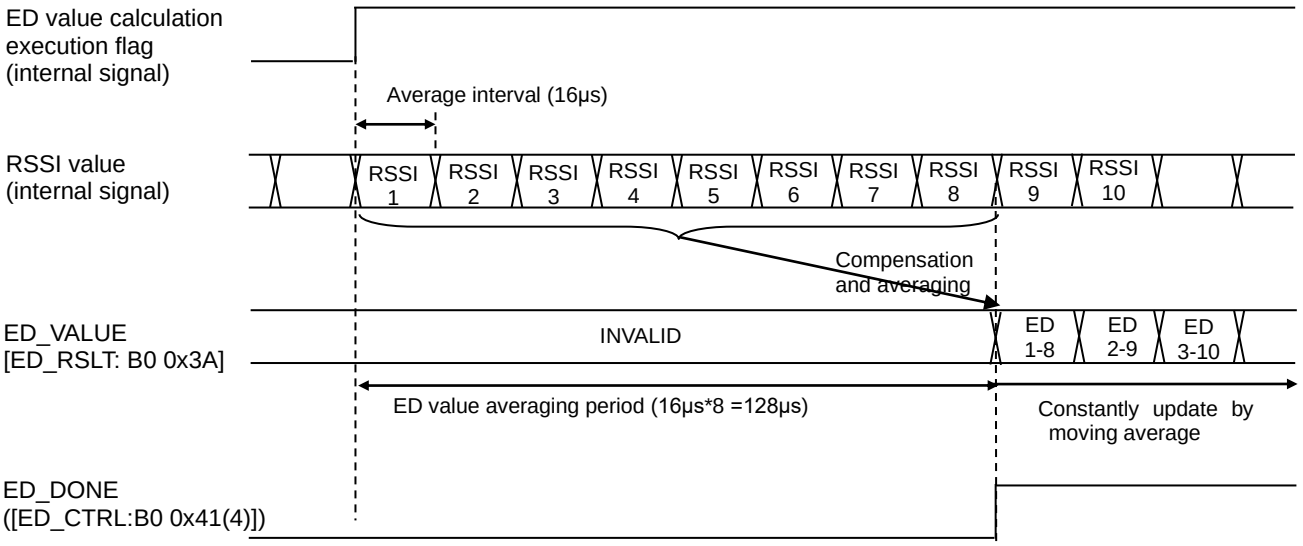
ED_DONE bit will be cleared when one of the following conditions are met.

i) Antenna is switched.
ii) Gain is switched.
iii) Calculating for the ED value is resumed. (After it stopped.)

The ED value’s calculation is required a time as below formula.
ED value calculation time = Average interval (16μs) * number of the average times

The timing example is as follows:

[condition] Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)]) = 0b011 (8 times averaging)



○Setting Channel Filter Bandwidth

The channel filter bandwidth can be set by CHFIL_BW_ADJ([CHFIL_BW: B0 0x54(6-0)]) and CHFIL_WIDE_SET([CHFIL_BW: B0 0x54(7)]) and CHFIL_BW_OPTION([CHFIL_BW_OPTION: B0 0x6B]). The relationship between the setting value and the channel filter bandwidth is expressed by the following formula.

Channel filter bandwidth [Hz] = {Master clock frequency [Hz] * (CHFIL_WIDE_SET+1)}/ (CHFIL_BW_ADJ * 180) * Scale factor setting (CHFIL_BW_OPTION)

See the following table for the channel filter bandwidth for each setting value. Channel filter bandwidths can be set individually for normal reception and for CCA. As for the channel filter bandwidth for CCA, setting values of CHFIL_BW_ADJ_CCA([CHFIL_BW_CCA: B0 0x6A(6-0)]) and CHFIL_WIDE_SET_CCA([CHFIL_BW_CCA: B0 0x6A(7)])) are applied.

(1) CHFIL_WIDE_SET=0b0, CHFIL_BW_OPTION=0b000

CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]	CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]
0	prohibited	16	12.5
1	200	17	11.8
2	100	18	11.1
3	66.7	19	10.5
4	50	20	10
5	40	21	9.5
6	33.3	22	9.1
7	28.6	23	8.7
8	25	24	8.3
9	22.2	25	8
10	20	26	7.7
11	18.2	27	7.4
12	16.7	28	7.1
13	15.4	・・・	・・・
14	14.3	126	1.59
15	13.3	127	1.57

(2) CHFIL_WIDE_SET=0b1, CHFIL_BW_OPTION=0b000

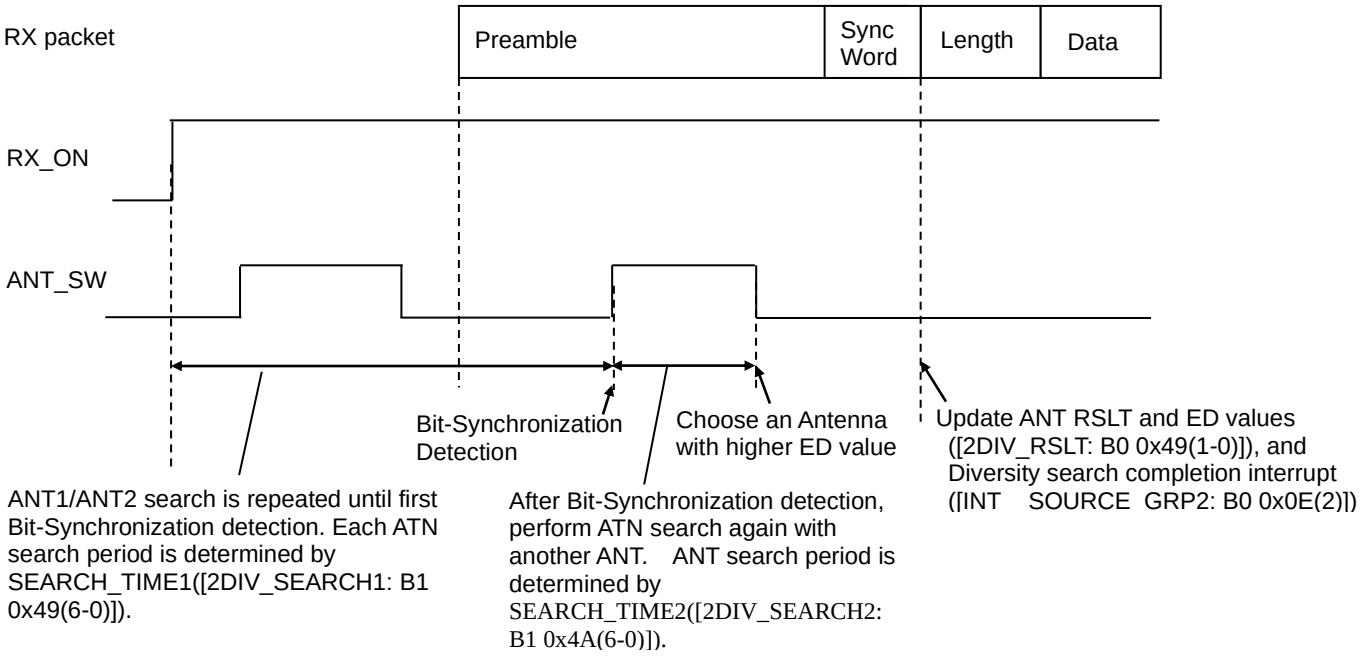
CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]	CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]
0	prohibited	16	25
1	400	17	23.5
2	200	18	22.2
3	133.3	19	21.1
4	100	20	20
5	80	21	19
6	66.7	22	18.2
7	57.1	23	17.4
8	50	24	16.7
9	44.4	25	16
10	40	26	15.4
11	36.4	27	14.8
12	33.3	28	14.3
13	30.8	・・・	・・・
14	28.6	126	3.18
15	26.7	127	3.14

The channel filter bandwidth need to be optimized according to the data rate and the maximum frequency deviation.

○Diversity function

ML7404 supports two antenna diversity function for FSK mode.
While setting 2DIV_EN([2DIV_CTRL: B0 0x48(0)]) = 0b1, as soon as RX_ON is set, diversity mode will start. When diversity mode is started, and upon RX data detection, each ED value will be acquired by switching two antennas. And then antenna with higher ED value will be selected automatically. As diversity uses preamble data for ED value acquisition, longer preamble length is desirable. If preamble is too short, accurate ED values may not be obtained.

The timing example is as below.



ED values acquired by the diversity operation are stored in [ANT1_ED: B0 0x4A] and [ANT2_ED: B0 0x4B] registers and antenna diversity result is indicated at 2DIV_RSLT[1:0] ([2DIV_RSLT: B0 0x49(1-0)]) when SyncWord is detected.
In diversity operation, the number of ED average times is specified by 2DIV_ED_AVG[2:0]([2DIV_MODE: B1 0x48(2:0)]).
Search time for each antenna is defined by [2DIV_SEARCH1:B1 0x49] and [2DIV_SEARCH2:B1 0x4A] registers. And its time resolution can be defined by SEARCH_TIME_SET([2DIV_SEARCH1: B1 0x49(7)]).

If diversity search completion interrupt (INT[10] group2) is cleared, ED values and antenna diversity result are cleared.

(Note)

- When an incorrect diversity completion caused by errornous detection due to thermal noise, ML7404 resume antenna diversity automatically. But when receiving a desired signal during the process of errounous detection, ED value obtained by [ANT1_ED:B0 0x4A] or [ANT2_ED:B0 0x4B] may indicate a low value different from the actual input level.
- If this event occures, the actual ED value of desired signal can be achibed by reading [ED_RSLT:B0 0x3A] registers after SyncWord detection interrupt (INT[13] group2) generation.

(1) Antenna switching function

By using [2DIV_CTRL: B0 0x48], [ANT_CTRL: B0 0x4C], [SPI/EXT_PA_CTRL: B0 0x53] registers, TX-RX signal selection (TRX_SW), antenna switching signal (ANT_SW), external PA control signal(DCNT) can be controlled.

Two types of antenna switch (SPDT / DPDT) can be controlled by [2DIV_CTRL: B0 0x48(3-1)] and [ANT_CTRL: B0 0x4C]). There are the following relationship between ANT_SW pin, TRX_SW pin and [2DIV_CTRL: B0 0x48(2-1)] for each antenna switch.

i) DPDT switch

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) = 0b1 and ANT_CTRL1([2DIV_CTRL: B0 0x48(5)]) = 0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)]) = 0b1, polarity of ANT_SW and TRX_SW are reversed.

TX/RX state	INV_TRX_SW = 0b0 (default setting)		INV_TRX_SW = 0b1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	H	L	L	H	Idle state
TX	L	H	H	L	TX state
RX	H	L	L	H	When Diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x48(0)] = 0b1).
	L/H	H/L	H/L	L/H	If diversity enable is set, during searching, (ANT_SW = H, TRX_SW = L) and (ANT_SW = L, TRX_SW = H) are switched alternatively. After diversity completion, fix to one of the condition.

ii) SPDT switch

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) = 0b0, ANT_CTRL1([2DIV_CTRL: B0 0x48(5)]) = 0b0. ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)]) = 0b1, polarity of TRX_SW is reversed.

TX/RX condition	INV_TRX_SW = 0b0 (default setting)		INV_TRX_SW = 0b1 (polarity reverse)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idel state
TX	L	H	L	L	TX state
RX	L	L	L	H	When diversity disable or initial condition when diversity enable is set ([2DIV_CTRL: B0 0x48(0)] = 0b1).
	H/L	L	H/L	H	If diversity enable is set,during searching (TRX_SW = H) and (TRX_SW = L) is switched alternatively. After diversity completion , fix to one of the condition.

In the above setting, If INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b1 are set, polarity of ANT_SW pin is reversed.

TX/RX state	INV_ANT_SW = 0b0 ANT_CTRL1 = any (default setting)		INV_ANT_SW = 0b1 ANT_CTRL1 = 0b1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	When diversity disable or intial codition when diversity enable is set ([2DIV_CTRL: B0 0x48(0)] = 0b1).
	H/L	L	L/H	L	If diversity enable is set, during searching (ANT_SW = H) and (ANT_SW = L) is switched alternatively. After diversity completion, fix to one of the condition.

(2) Antenna switch forced setting

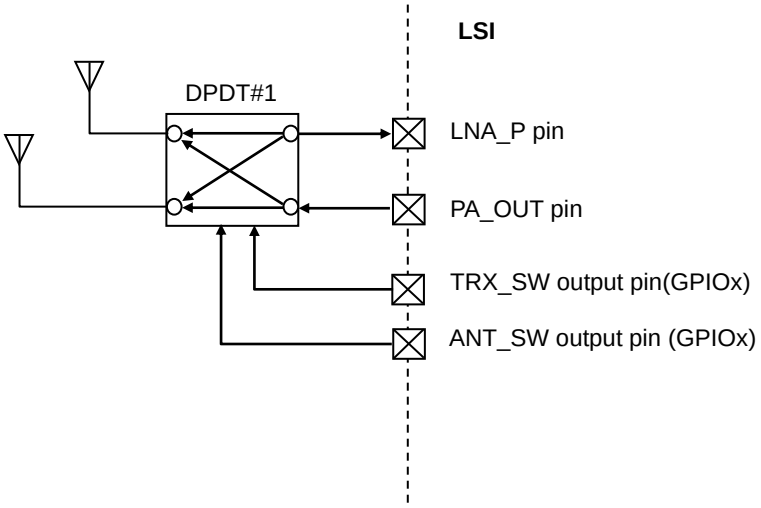
By [ANT_CTRL: B0 0x4C] register, ANT_SW pin output conditions can be set to fix.

TX: By TX_ANT_EN([ANT_CTRL: B0 0x4C(0)]) = 0b1, TX_ANT([ANT_CTRL: B0 0x4C(1)]) condition will be output.
RX: By RX_ANT_EN([ANT_CTRL: B0 0x4C(4)]) = 0b1, RX_ANT([ANT_CTRL: B0 0x4C(5)]) condition will be output.

However, output is defined by [GPIO*_CTRL: B0 0x4E - 0x51] register , [GPIO*_CTRL:B0 0x4E - 0x51] registers setting has higer priority.

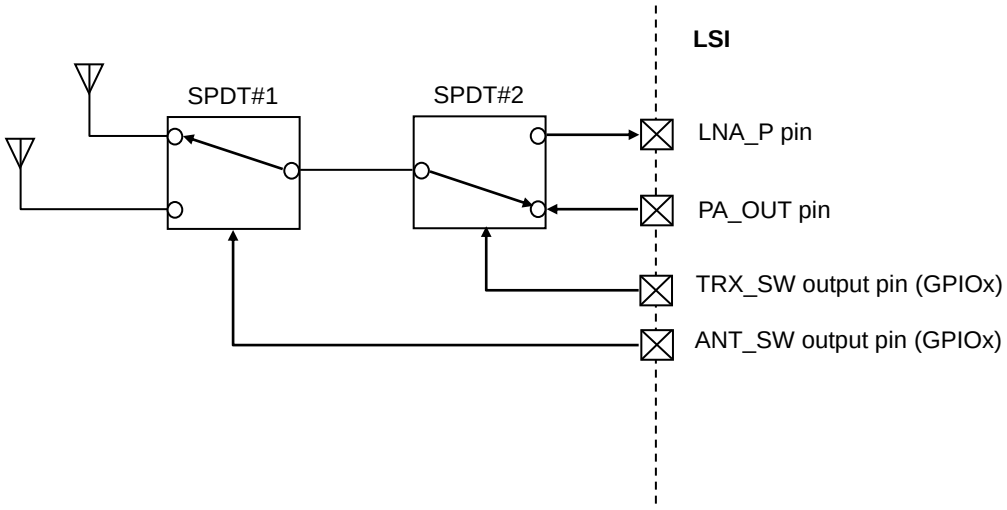
Antenna switching control signals can be also used as below.

Example 1) using one DPDT switch
Please set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) = 0b1.



(Note)
If you assign one more GPIO to external PA control signal, you can use both DPDT SW and external PA together. external circuits around LNA_P pin, PA_OUT pin and antenna switch (DPDT#1) are omitted in this example.

Example 2) using 2 SPDT switches
Please set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) = 0b0.



(Note)
If you assign one more GPIO to external PA control signal, you can use both 2 SPDT SWs and external PA together external circuits around LNA_P pin, PA_OUTpin and antenna switch(SPDT#2) are omitted in this example.

○CCA (Clear Channel Assessment) function

The ML7404 supports CCA. CCA is a function that makes a judgment whether the specified frequency channel is busy or idle. The ML7404 supports Normal mode, Continuous mode and IDLE detection mode as the following table.

[CCA mode setting]

	[CCA_CTRL: B0 0x39]		
	Bit4 (CCA_EN)	Bit5 (CCA_CPU_EN)	Bit6 (CCA_IDLE_EN)
Normal mode	0b1	0b0	0b0
Continuous mode	0b1	0b1	0b0
IDLE detection mode	0b1	0b0	0b1

(1) Normal mode

Normal mode determins IDLE or BUSY. To execute CCA as normal mode, turn state RX_ON after setting CCA_EN(CCA_CTRL: B0 0x39(4)]) = 0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)]) = 0b0 and CCA_IDLE_EN (CCA_CTRL: B0 0x39(6)]) = 0b0.

The result of CCA is determined by comparing the ED value to the threshold value of CCA defined by [CCA_LVL: B0 0x37]. If the ED value displayed in [ED_RSLT: B0 0x3A] exceeds the threshold, it is determined as “BUSY”, and CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) = 0b01 is set. If the ED value is smaller than the threshold for the IDLE detection period defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3C] and [IDLE_WAIT_H: B0 0x3B], it is determined as “IDLE”, and CCA_RSLT[1:0] = 0b00 is set. For details of IDLE_WAIT[9:0], please refer to “IDLE detection for long time period”.

If “BUSY” or “IDLE” state is detected, CCA completion interrupt (INT[18] of group 3) is generated, and CCA_EN bit is cleared to 0b0 automatically.

Upon clearing CCA completion interrupt, CCA_RSLT[1:0] are reset to 0b00. Therefore, CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36], as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case if the averaged ED value exceeds [CCA_LVL: B0 0x37], it is determined as “BUSY” and CCA operation is terminated. If the averaged ED value is smaller than [CCA_LVL: B0 0x37], IDLE judgment is not determined. And CCA_RSLT[1:0] indicates 0b11. CCA operation continues until “BUSY” is determined or the given ED value is out of averaging target and “IDLE” is determined. For detail behavior when the ED value exceeds [CCA_IGNORE_LVL: B0 0x36], refer to “IDLE determination exclusion under strong signal input“.

Time from CCA command issue to CCA completion is in the formula below.

[IDLE detection]
CCA execution time = (ED value average times + IDLE_WAIT setting) × Average interval (16us)

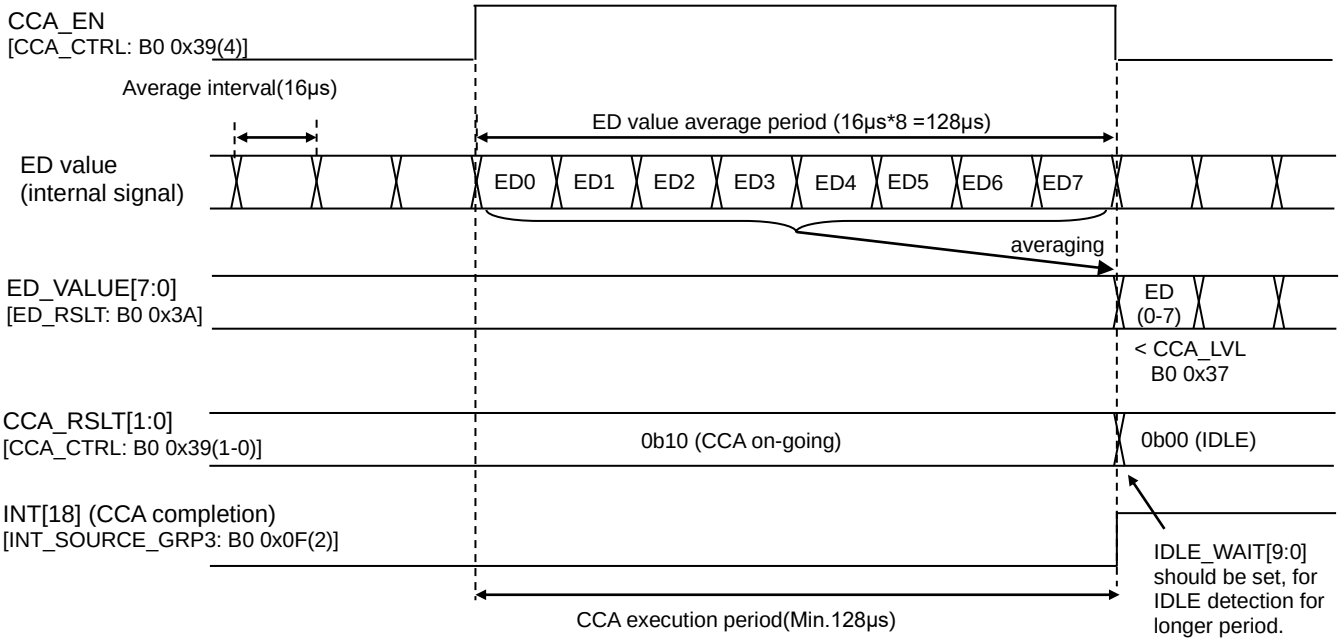
[BUSY detection]
CCA execution time = ED value average times × Average interval (16us)

(Note)
The above equations do not consider IDLE judgment excluded by [CCA_IGNORE_LVL: B0 0x36]. For details of [CCA_IGNORE_LVL: B0 0x36] operation, “IDLE determination exclusion under strong signal input”.

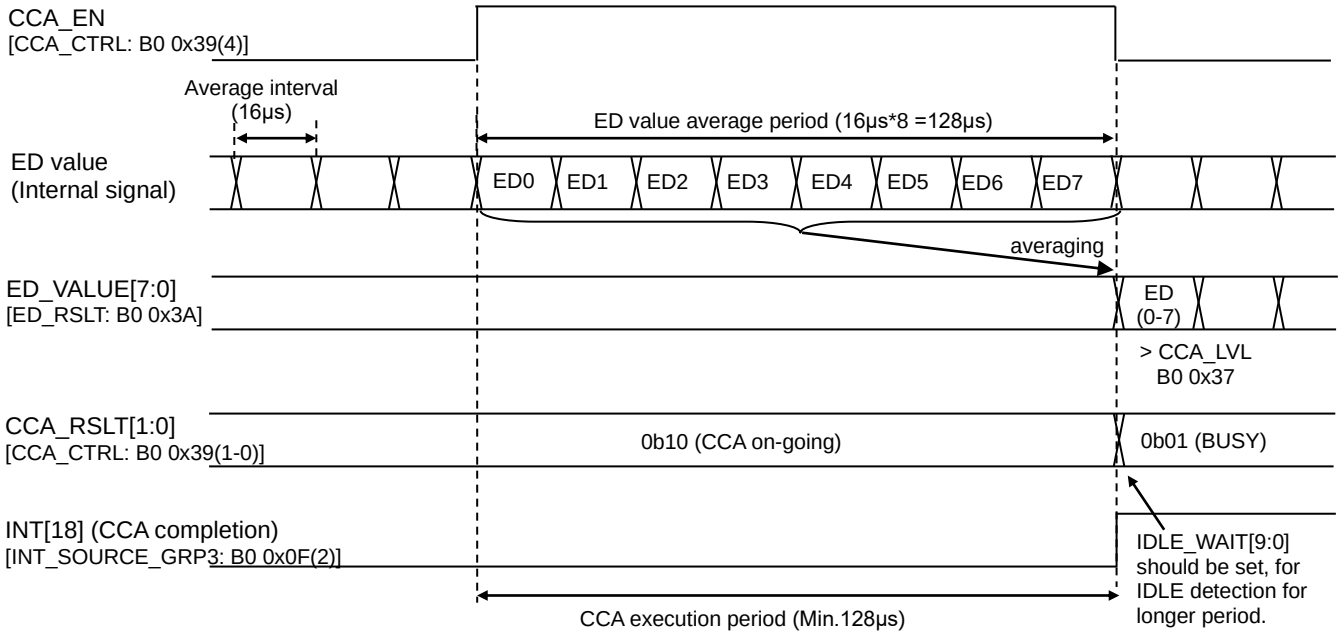
The following is timing chart for normal mode.

[Condition]
ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)]) = 0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)]) = 0b00_0000_0000 (IDLE detection 0µs)

[IDLE detection case]



[BUSY result case]



(2) Continuous mode

Continuous mode continues CCA untill terminated by the host MCU. CCA continuous mode will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)]) = 0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)]) = 0b1 and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)]) = 0b0 are set.

Like normal mode, CCA judgement is determined by average ED value in [ED_RSLT: B0 0x3A] register and CCA threshold defined by [CCA_LVL: B0 0x37] register. If the averaged ED value exceeds the CCA threshold value, it is determined as “BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) = 0b01 is set.

If the averaged ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers, it is determined as “IDLE”. And CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long time period”.

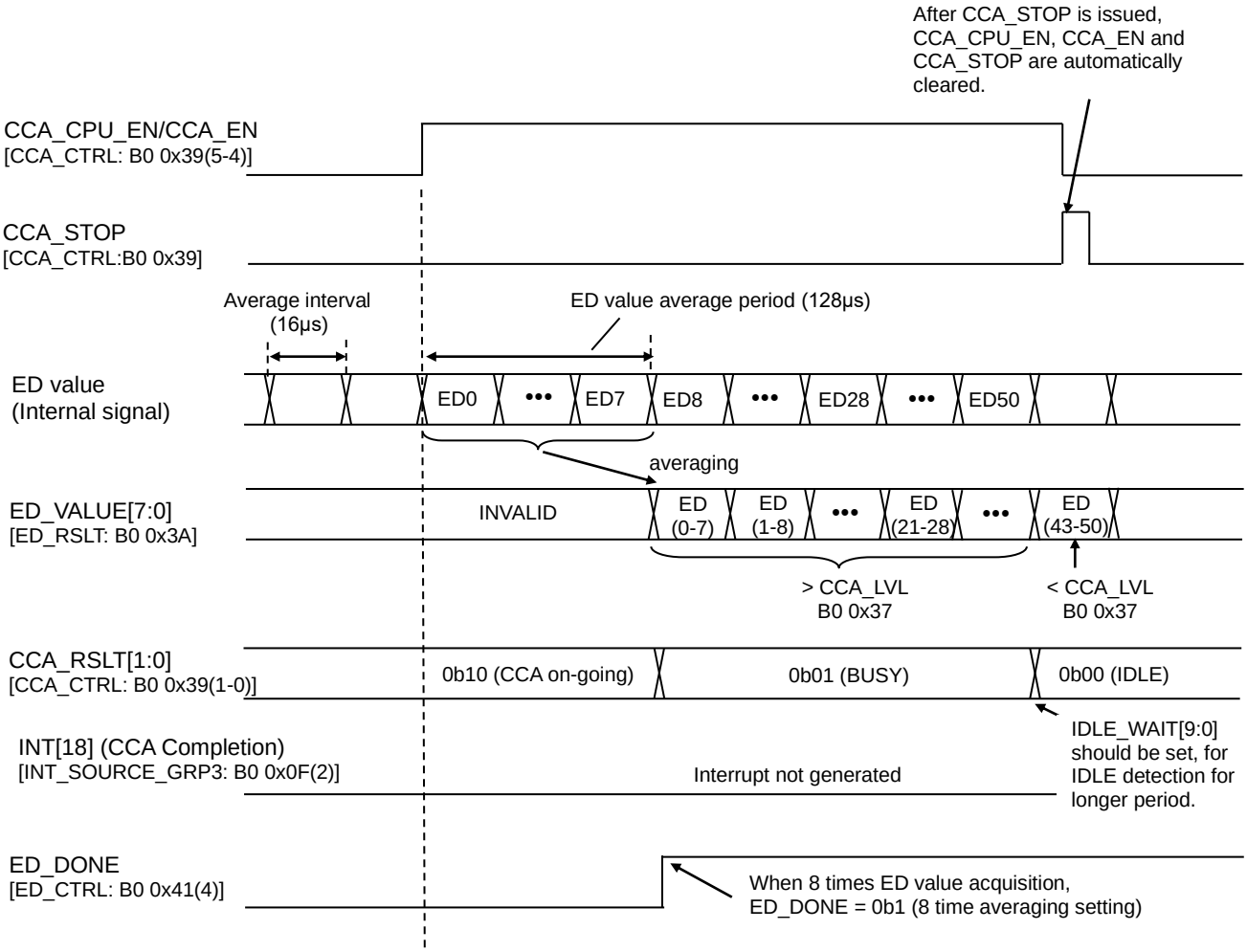
If an ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case if the averaged ED value exceed CCA threshold level, it is determined as “BUSY” and CCA_RSLT[1:0] indicates 0b01. If the averaged ED value is smaller than CCA threshold level, IDLE judgement is not determined. And CCA_RSLT[1:0] indicates 0b11. For details operation of ED value exeeceding [CCA_IGNORE_LVL: B0 0x36] register, please refer to “IDLE determination exclusion under strong signal input”.

Continuous mode does not stop when “BUSY” or “IDLE” is detected. CCA operation continues until 0b1 is set to CCA_STOP([CCA_CTRL: B0 0x39(7)]). Result is updated every time ED value is acquired. CCA completion interrup (INT[18] group3) will not be generated.

The follwing is timing chart for continuous mode.

[Condition]
ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)]) = 0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)]) = 0b00_0000_0000 (IDLE detection period 0µs)

[BUSY to IDLE transition, terminated with CCA_STOP]



(3) IDLE detection mode

IDLE detection mode continues CCA until IDLE detection. IDLE detection CCA will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)]) = 0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)]) = 0b0 and CCA_IDLE_EN (CCA_CTRL: B0 0x39(6)]) = 0b1 are set.

Like normal mode, CCA judgment is determined by average ED value in ED_VALUE([ED_RSLT: B0 0x3A]) and CCA threshold defined by [CCA_LVL: B0 0x37]. If the averaged ED value exceeds the CCA threshold value, it is determined as "BUSY", and CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) = 0b01 is set. If the averaged ED value is smaller than CCA threshold value for the IDLE detection period defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L], [IDLE_WAIT_H]: B0 0x3B,0x3C], it is determined as "IDLE", and CCA_RSLT[1:0] = 0b00 is set. For details operation of IDLE_WAIT[9:0], please refer to "IDLE detection for longer time period".

In IDLE detection mode, only when IDLE is detected, CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is generated. Also, if CCA is performed based on the CCA_EN setting, CCA_EN(CCA_CTRL: B0 0x39(4)]) and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)]) are automatically cleared to 0b0.

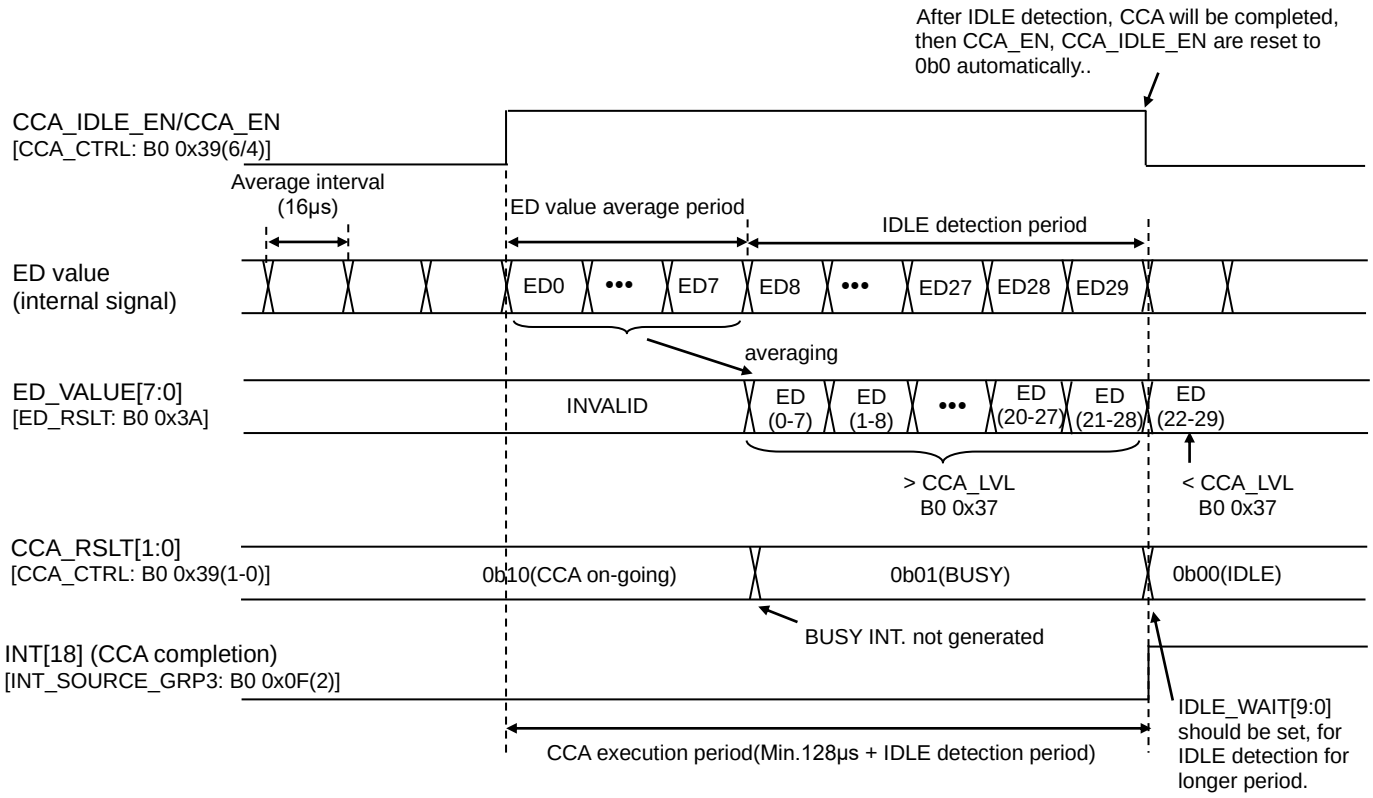
In IDLE detection mode, while BUSY is detected, CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is not generated, and IDLE detection continues. Upon clearing CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]), CCA_RSLT[1:0] are reset to 0b00. Therefore, CCA_RSLT[1:0] should be read before clearing CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]).

If an ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36], as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgment is not performed. In this case, if the averaged ED value is smaller than [CCA_LVL: B0 0x37], IDLE determination is not performed and CCA_RSLT[1:0] indicates 0b11. CCA operation continues until given ED value is out of averaging target and "IDLE" is determined. For detail behavior when the ED value exceeds [CCA_IGNORE_LVL: B0 0x36], refer to " IDLE determination exclusion under strong signal input ".

The follwing is timing chart for IDLE detection.

[Upon BUSY detection, continue CCA and IDLE detection case]

[Condition]
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)]) = 0b011 (ED value 8 times average)
IDLE_WAIT[9:0] ([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)]) = 0b00_0000_0000 (IDLE detection period 0µs)



(4) IDLE determination exclusion under strong signal input

If acquired ED value exceeds [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed as long as a given ED value is included in the averaging target range. If the averaged ED value including this strong ED value indicated in [ED_RSLT: B0 0x39] register exceeds the CCA threshold value defined by [CCA_LVL: B0 0x37] register, it is determined as “carrier detected (BUSY)”, and CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) is set to 0b01. Also, if this average ED value is equal to or smaller than the CCA threshold, it is determined as “CCA evaluation on-going (ED value excluding CCA judgment acquisition”, and CCA_RSLT[1:0] is set to 0b11.

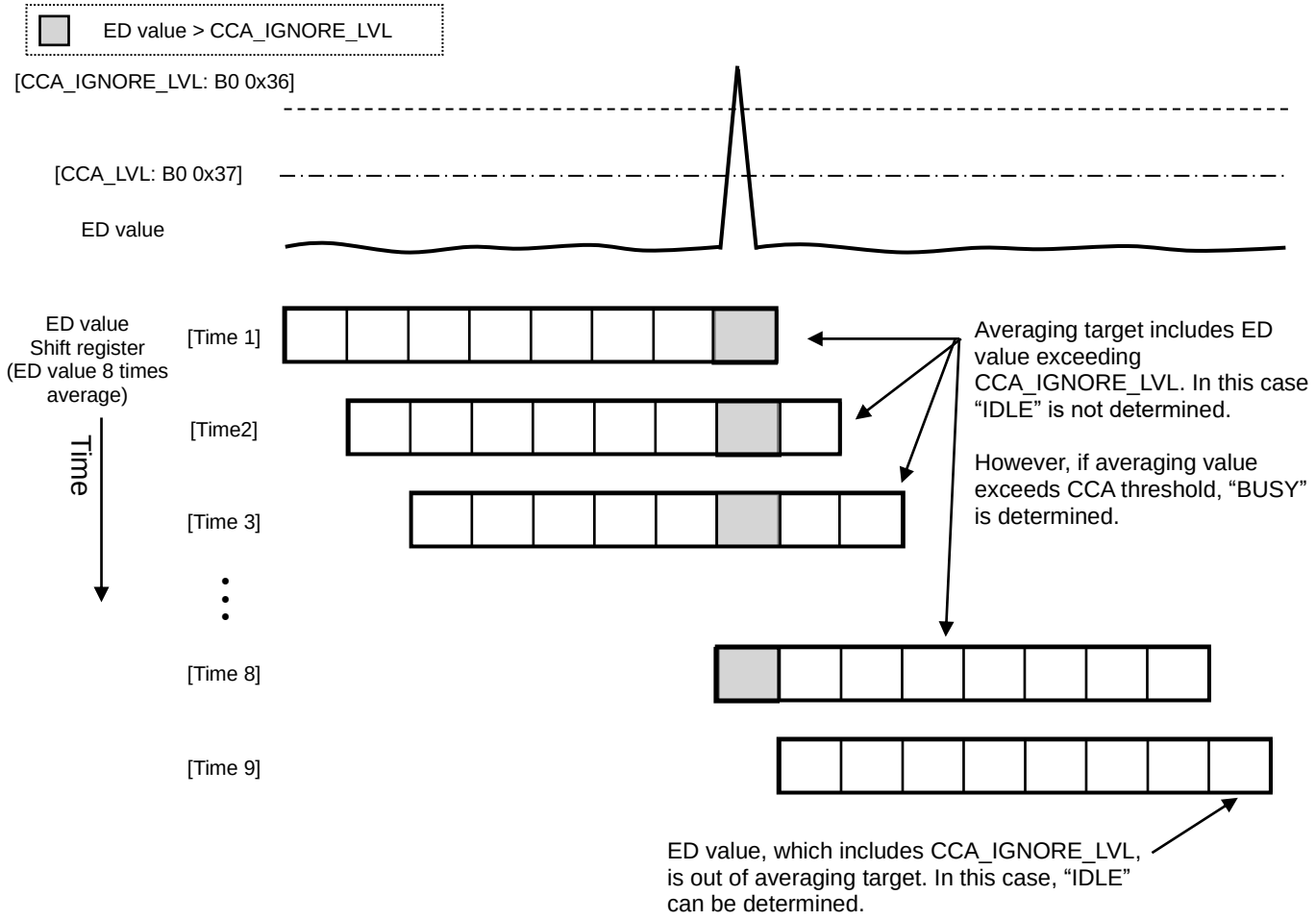
Even if the moving average of the ED value is less than or equal to [CCA_LVL: B0 0x37], IDLE judgment is not made when the ED value to be moving-averaged contains a value larger than [CCA_IGNORE_LVL: B0 0x36]. In this case, CCA_RSLT[1:0] indicates 0b11(on-going), and CCA operation continues until IDLE or BUSY is determined. (IDLE is determined in IDLE detection mode, or CCA_STOP([CCA_CTRL: B0 0x39(7)]) is issued in continuous mode.)

If the moving average of the ED value exceeds [CCA_LVL: B0 0x37], BUSY judgment is made immediately regardless of the comparison result of [CCA_IGNORE_LVL: B0 0x36].

(Note)

CCA completion interrupt is notified of only when CCA result is judged as IDLE or BUSY. Therefore, if data whose ED value exceeds CCA_IGNORE_LVL are input intermittently, neither “IDLE” or “BUSY” can be determined and CCA may continue.

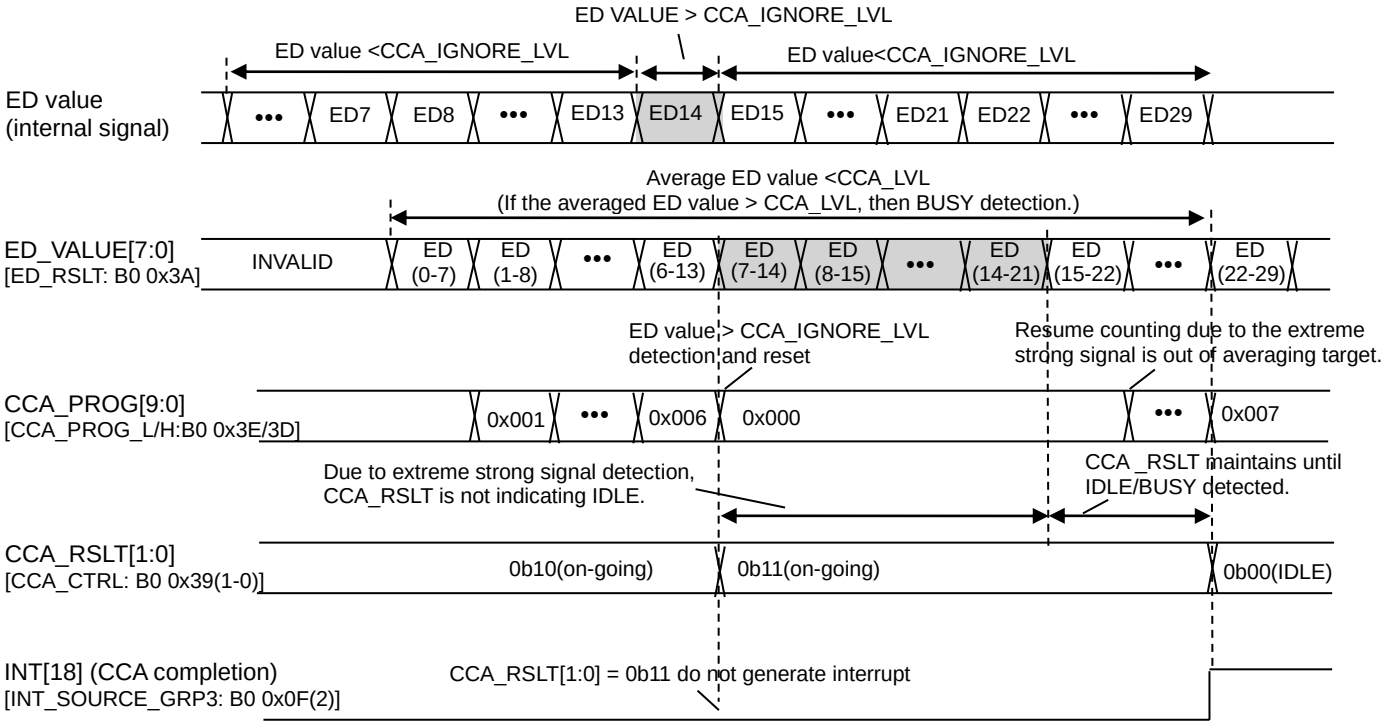
[ED value acquisition under extrem strong signal]



The follwing is timing chart for CCA determination exclusion under strong signal.

[During IDLE_WAIT counting, detected extremly strong signal. After the given signal is out of averaging target, IDLE detection case]

[Condition]
CCA normal mode
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)]) = 0b011 (ED value 8 times average)
IDLE_WAIT[9:0]([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)]) = 0b00_0000_0111(IDLE detection period 112μs)



(5) IDLE detection for longer time period

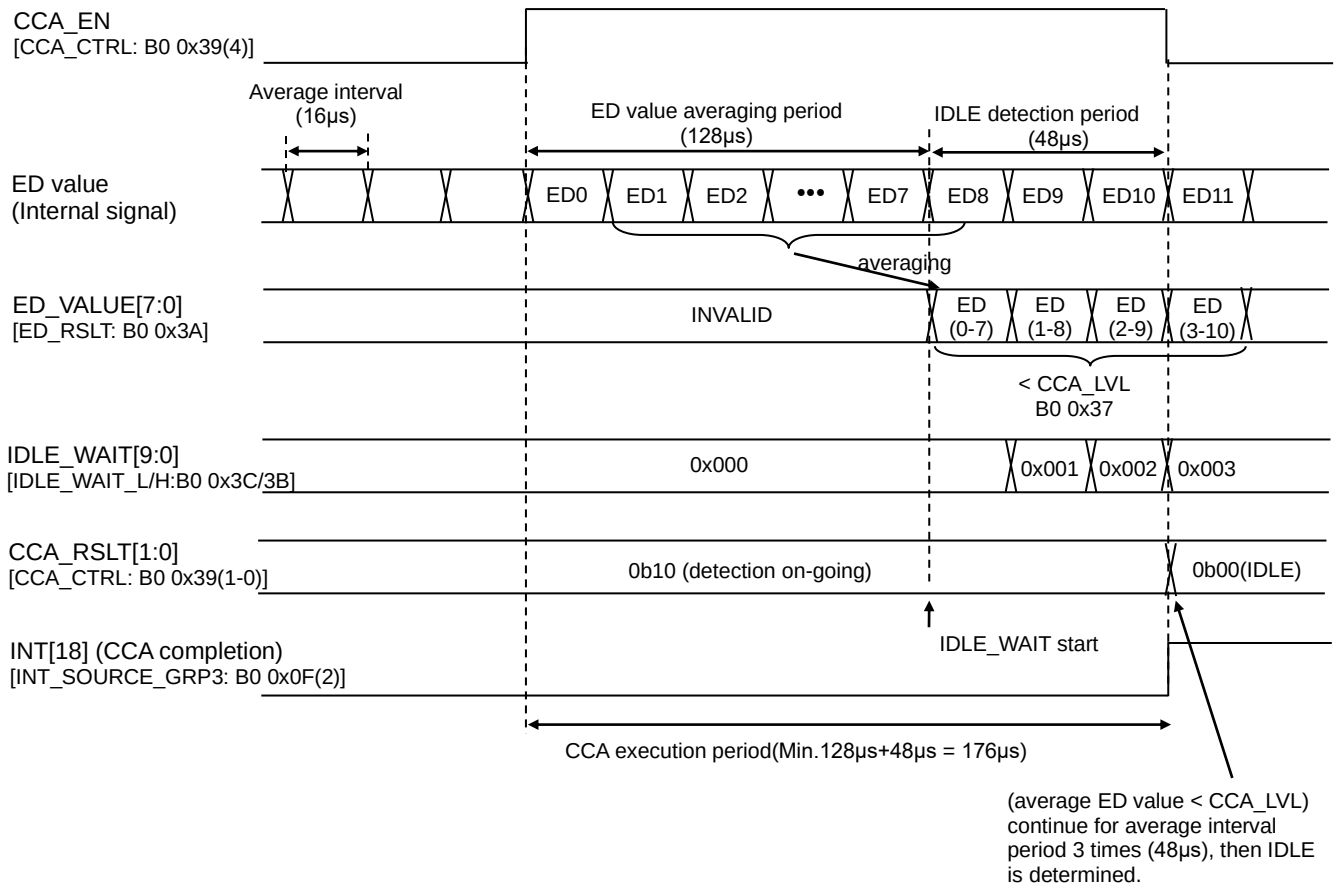
When CCA IDLE detection is performed for longer time period, IDLE_WAIT [9:0] of [IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)] can be used.

By using IDLE_WAIT [9:0], you can detect IDLE whose period is longer than the averaging period (128µs for averaging eight values with 16µs average interval). This function counts how many times moving average of the ED value is less than or equal to [CCA_LVL: B0 0x37] continuously and judge it as IDLE if the count is more than or equal to IDLE_WAIT [9:0]. Even when this function is used, BUSY judgment is made immediately without waiting the IDLE_WAIT [9:0] period if the moving average of the ED value exceeds [CCA_LVL: B0 0x37].

The following timing chart is IDLE detection setting IDLE_WAIT[9:0].

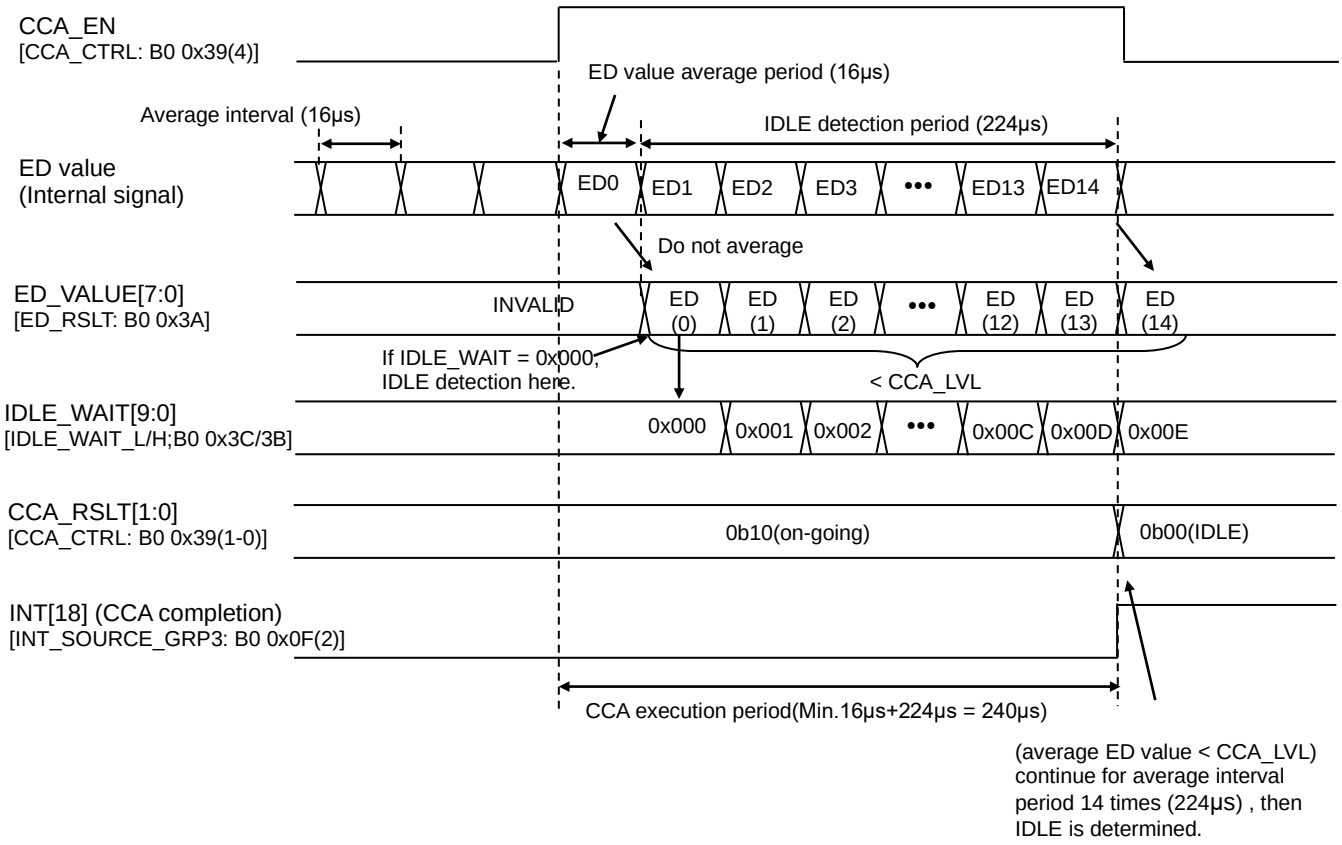
[ED value 8 times average IDLE detection case]

[Condition]
CCA normal mode
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)]) = 0b011 (ED value 8 times average)
IDLE_WAIT[9:0]([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)]) = 0b00_0000_0011 (IDLE detection period 48µs)



[ED value 1time IDLE detection case]

[Condition]
CCA normal mode
ED_AVG[2:0]([ED_CTRL: B0 0x41(2-0)]) = 0b000 (ED value 1 time average)
IDLE_WAIT[9:0]([IDLE_WAIT_L/H: B0 0x3C/3B(1-0)]) = 0b00_0000_1110 (IDLE detection period 224µs)



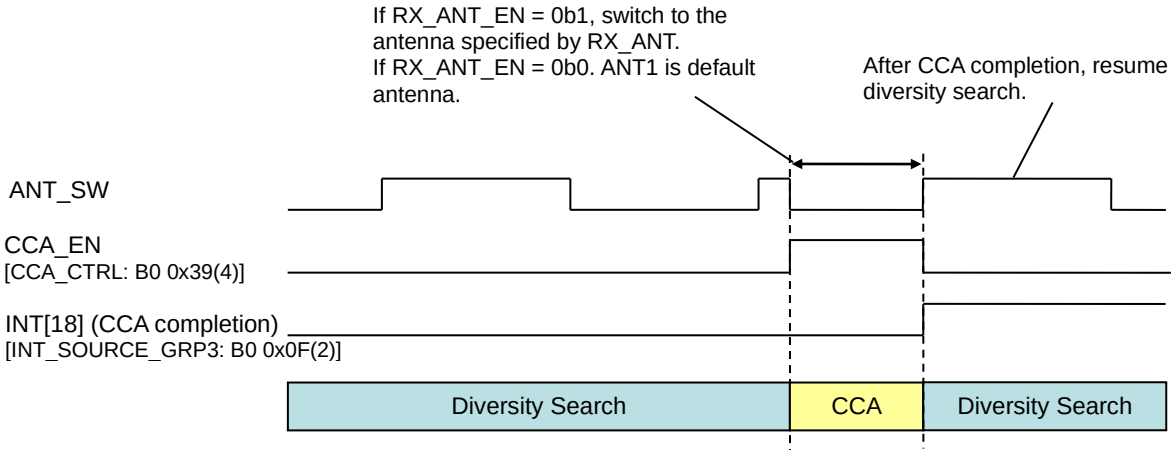
(6) CCA operation during diversity

i) CCA operation during diversity search

During diversity search, if CCA command is issued, diversity search will be terminated and CCA will start.

Upon CCA starting, antenna is fixed to reset value(*1), maintaining until next diversity search. However, if RX_ANT_EN([ANT_CTRL:B0 0x4C(4)]) = 0b1 is set, antenna is specified by RX_ANT([ANT_CTRL: B0 0x4C(5)]). After CCA completion, diversity search will be executed agaim.

*1 Please refer to the “Antenna switching function”. According to the default setting, ANT_SW and TRX_SW signals are set.

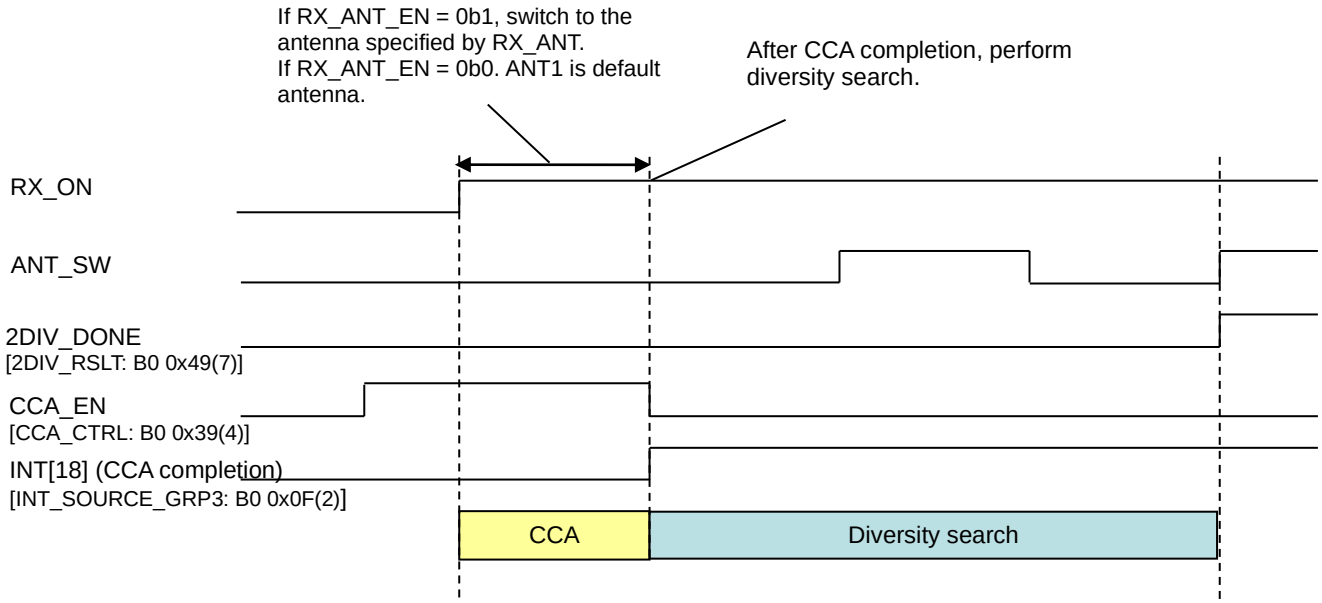


(Note)

During CCA operation, RX operation is performed at the same time, even if CCA completion interrupt is not generated, SyncWord detection interrupt ([INT_SOURCE_GRP2: B0 0x0E(5)]), FIFO-Full interrupt ([INT_SOURCE_GRP1: B0 0x0D(5)]), RX completion interrupt ([INT_SOURCE_GRP3: B0 0x0E(0)]) or CRC error interrupt ([INT_SOURCE_GRP3: B0 0x0E(1)]) can be generated.

For details diversity function, please refer to the “Diversity function”.

ii) During diversity, before RX_ON state, CCA is performed.
If diversity ON setting and CCA operation setting are enabled before RX_ON state, after RX_ON state transition, diversity search will not be perform, but CCA will start. After CCA completion, diversity search will be performed.



(7) CCA threshold setting

Setting of a CCA threshold value ([CCA_LVL: B0 0x37]) should be entered by considering desired input level (ED value) and variations (IC component variations, temperature fluctuation) as well as other losses (in the antenna and matching circuit, etc.). The following formula generally expresses the relationship between input levels and ED values.

[2.4k/4.8kbps]
ED value = 255/80 * (120 + input level [dBm] - variations – other losses)

In order to validate whether CCA threshold is optimised or not, CCA should be executed and confirmimg level changing from IDLE to BUSY, every time input level is changed,

●TX Related function

○Ramp control function

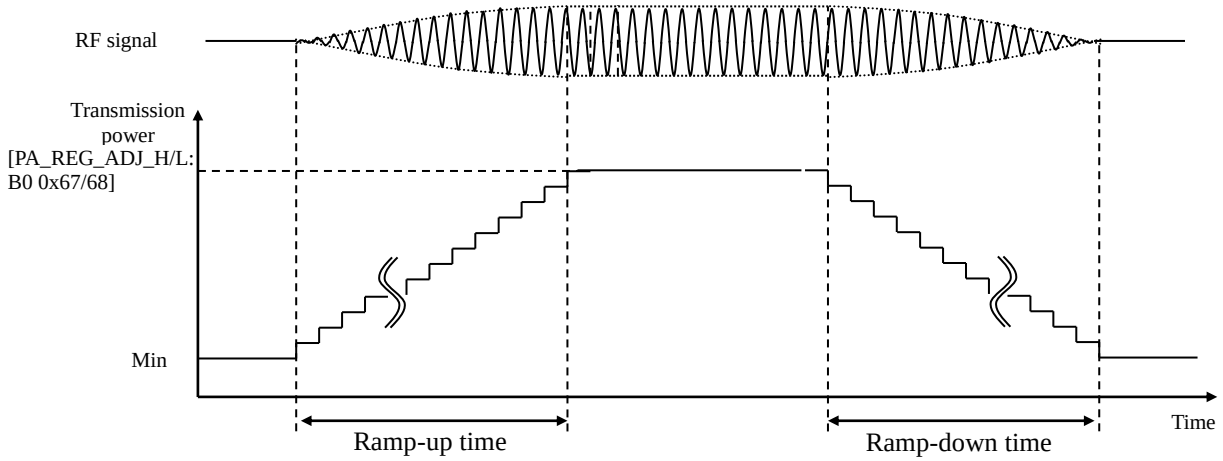
Ramp control function reduces spurious emission at transmission start and transmission stop. Ramp control can be controlled by the following registers.

Setting	Register
Ramp control counter increment setting	RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)])
Ramp control standard clock cycle setting	RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])
Ramp-up time setting	RAMP_CLK_SET_R([RAMP_CTRL2: B3 0x41])
Ramp-down time setting	RAMP_CLK_SET_F([RAMP_CTRL3: B3 0x42])

Ramp-up/down time can be calculated by using the following formulas, respectively.

Ramp-up time [s] = Ramp control standard clock cycle setting (RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])) *
Ramp-up time setting (RAMP_CLK_SET_R([RAMP_CTRL2: B3 0x42]))} *
BPSK/Maximum amplitude setting in FSK ([PA_REG_ADJ_H/L: B0 0x67(0)/0x68]) /
Ramp control counter increment setting (RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)]))

Ramp-down time [s] = Ramp control standard clock cycle setting (RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])) *
Ramp-down time setting (RAMP_CLK_SET_F([RAMP_CTRL3: B3 0x43]))} *
BPSK/Maximum amplitude setting in FSK ([PA_REG_ADJ_H/L: B0 0x67(0)/0x68]) /
Ramp control counter increment setting (RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)]))



The following table shows ramp-up/down times (examples) at reset, for the maximum setting and setting for Sigfox (PA output power +13dBm setting).

Setting register	Reset (Min.)	For Sigfox	Maximum setting
RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)])	0x0	0x0	0x0
RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])	0x0	0x1	0x1
RAMP_TIME_R([RAMP_CTRL1: B3 0x42])	0x01	0x3F	0x7F
RAMP_TIME_F([RAMP_CTRL2: B3 0x43])	0x01	0x3F	0x7F
[PA_REG_ADJ_H/L: B0 0x67/68]	0x0E4	0x0E4	0x0E4
Ramp-up/down time	12.7us	12.8ms	25.7ms

●Other Functions

○Data rate setting function

(1) Data rate change setting

ML7404 supports various TX/RX data rate setting defined by the following registers.
TX: [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03] registers
RX: [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05] and [RX_RATE2: B1 0x06] registers
TX/RX data rate can be defined in the following formula.

[TX]

TX data rate [bps] = round (Master clock frequency[MHz] / 10/ TX_RATE[11:0])

The following table shows the recommended value for each data rate. The following register values are automatically set to [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03] registers by setting TX_DRATE ([DRATE_SET: B0 0x06(3-0)]).

TX data rate [kbps]	[TX_RATE_H][TX_RATE_L] setting value (decimal)	Data rate deviation [%] (*1)
1.2	3000	0.00
2.4	1500	0.00
4.8	750	0.00
9.6	375	0.00
10.0	360	0.00
19.2	188	-0.27
15.0	240	0.00
32.768	110	-0.12
50	72	0.00
100	36	0.00
200	18	0.00

*1 Data rate deviation is assumption that frequency deviation of master clock(36MHz crystal oscillator or TCXO) is 0ppm.

In the TX data rate calculated by the above equation, if the data rate deviation increases, the data rate deviation is adjusted to a smaller value by using [TX_RATE2_H: B1 0x7C] and [TX_RATE2_L: B1 0x7D].

TX_RATE2[13:0] = round [[{1/Data Rate(bps)} -
{1 / (Master clock frequency (Hz) / TX_RATE[11:0]) × 9}] /
{1/ Master clock frequency (Hz)}]

[RX]

RX data rate [bps] = round ({Master clock frequency[MHz] / N} / {RX_RATE1[11:0] ×[RX_RATE2[6:0]})
where, N=1(LOW_RATE_EN=0b0)
N=2(LOW_RATE_EN=0b1)

The following table shows the recommended value for each data rate (LOW_RATE_EN([CLK_SET2: B0 0x03(0)]) = 0b1). The following register values are automatically set to [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05] and [RX_RATE2: B1 0x06] by setting RX_DRATE([DRATE_SET: B0 0x06(7-4)]).

RX data rate [kbps]	[RX_RATE1_H][RX_RATE1_L] setting value (decimal)	[RX_RATE2] setting value (decimal)
1.2	120	125
2.4	60	125
4.8	30	125
9.6	15	125
10.0	15	120
19.2	8	117
15.0	12	100
20	9	100
32.768	5	110
40	5	90
50	3	120
100	2	90
200	9	10

(Note)
When LOW_RATE_EN([CLK_SET2: B0 0x03(0)]) = 0b0 is set, calculate the RX data rate according to the above formula. Note that when LOW_RATE_EN = 0b0 is set, [RX_RATE1_H: B1 0x04][RX_RATE1_L: B1 0x05] and [RX_RATE2: B1 0x06] are not automatically set to optimal values even if the data rate setting register for transmission and reception ([DRATE: B0 0x06]) is set.

(2) Other register setting associate with data rate change

When you change data rate, please change registers according to "Initialization table".

(Note)
Please change data rate setting in TRX_OFF state.

○Interrupt generation function

ML7404 support interrupt generation function. When interrupt occurs, interrupt notification signal (SINTN) become “L” to notify interrupt to the host MCU. Interrupt elements are divided into the 3 groups, [INT_SOURCE_GRP1: B0 0x0D], [INT_SOURCE_GRP2: B0 0x0E] and [INT_SOURCE_GRP3: B0 0x0F]. Each interrupt element can be maskalable using [INT_EN_GRP1: B0 0x10]. [INT_EN_GRP2: B0 0x11] and [INT_EN_GRP3: B0 0x12] registers. Interrupt notification signal (SINTN) can be output from GPIO* or EXT_CLK. For output setting, please refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51] and [EXTCLK_CTRL: B0 0x52] registers.

(Note)
If one of the unmask interrupt event occurs, SINTN maintains Low.

(1) Interrupt events table

Each interrupt event is described below table.

Register	Interrupt name	Description
INT_SOURCE_GRP1	INT[0]	Clock stabilizaion completion interrupt
	INT[1]	VCO calibration completion interrupt/ FUSE access completion interrupt/ IQ adjustment completion interrupt
	INT[2]	PLL unlock interrupt/ Out of VCO adjusting voltage range detected interrupt
	INT[3]	RF state transition completion interrupt
	INT[4]	FIFO-Empty interrupt
	INT[5]	FIFO-Full interrupt
	INT[6]	Wake-up timer completion interrupt
	INT[7]	Clock calibration completion interrupt
INT_SOURCE_GRP2	INT[8]	RX completion interrupt
	INT[9]	CRC error interrupt
	INT[10]	Diversity search completion interrupt
	INT[11]	RX Length error interrupt
	INT[12]	Reserved
	INT[13]	SyncWord detection interrupt
	INT[14]	Field checking interrupt
	INT[15]	Sync error interrupt
INT_SOURCE_GRP3	INT[16]	TX completion interrupt
	INT[17]	TX Data request accept completion interrupt
	INT[18]	CCA completion interrupt
	INT[19]	TX Length error interrupt
	INT[20]	TX FIFO access error interrupt
	INT[21]	Reserved
	INT[22]	General purpose timer 1 interrupt
	INT[23]	General purpose timer 2 interrupt

(2) Interrupt generation timing

In each interrupt generation, timing from reference point to interrupt generation (notification) are described in the following table. Timeout procedure for interrupt notification waiting are also described below.

(Note)

1) The following table assumes 100kbps for numeric values. For any symbol rate, replace the value described as "symbol time" with the symbol period.
2) The following table uses the bellow format for TX/RX data.

10bytes	2bytes	1byte	24bytes	2bytes
Preamble	SyncWord	Length	User data	CRC

3) Even when an interrupt notification is set to OFF, this LSI internally holds the interrupt. When the interrupt notification setting is changed from OFF to ON without clearing the interrupt, it will be notified. When the interrupt occurs, we recommend you clear the interrupt after turning the interrupt notification off.

Interrupt notification			Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	In case of Crystal oscillator circuits	RESETN release (Turn on sequence)	300 to 500µs
			SLEEP release (Returned from SLEEP)	300 to 500µs
		In case of TCXO	TCXO_EN setting (Turn on sequence)	10 to 500µs
			SLEEP release (Returned from SLEEP)	10 to 500µs
INT[1]	VCO calibration completion		VCO calibration start	9ms
INT[2]	PLL unlock detection		-	(TX) during TX after PA_ON (RX) during RX after RX enable
	Out of VCO adjusting voltage range detected		-	(TX) PA_ON rise (RX) RX enable rise
INT[3]	RF state transition completion		TX_ON command	(IDLE) 143µs (RX) 24µs
			RX_ON command	(IDLE) 118µs (TX) 25µs
			TRX_OFF command	(TX) 24µs (RX) 5µs
			Force_TRX_OFF command	(TX) 24µs (RX) 5µs
INT[4]	FIFO-EMPTY		TX_ON command (TX) (*1)	Empty trigger level is set to 0x02. (NRZ encoding) RF wake-up(210µs)+(preamble to 22nd Data byte)×10(bit time) = 3010µs)
			-(RX)	By FIFO read, FIFO usage is under trigger level.
INT[5]	FIFO-FULL		-(TX)	By FIFO write, FIFO usage exceed trigger level.
			SyncWord detection (RX)	Full trigger level is set to 0x05. (NRZ encoding) 500µs(5bytes data×10µs(bit time))
INT[6]	Wake-up timer completion		SLEEP setting	Wake-up timer is completed. For details, please refer to the "Wake-up timer".
INT[7]	Clock calibration completion		Calibration start	Calibration timer is completed. For details, please refer to the "Low speed clock shift detection function".
INT[8]	Data reception completion		SyncWord detection	When the length of L-field is 1byte, and NRZ encoding is used, after 2160µs. (L-field length(8bits)×10(symbol time) = 80µs, data length ((Data to CRC: bit)×10(symbol time) = 2080µs))
INT[9]	CRC error		SyncWord detection	(Format A/B) each RX CRC block calculation completion (Format C) RX completion

Interrupt notification		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[10]	Diversity search completion	-	SyncWord detection during diversity enable setting.
INT[11]	RX Length error	SyncWord detection	80μs(L-field 1byte) 160μs(L-field 2byte)
INT[12]	Reserved	-	-
INT[13]	SyncWord detection	-	SyncWord detection
INT[14]	Field check	-	Match or mismatch detected in Field check
INT[15]	Sync error	-	During RX after SyncWord detection, out-of-sync detected. (When RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b00 or 0b11.)
INT[16]	Data transmission completion	TX_ON command (*1)	RF wake-up+[TX data+3](bit) = 210μs+315bits x 10μs (bit time) = 3360μs
INT[17]	TX Data request accept completion	-	After full length data are written to the TX_FIFO. (RF state is TX_ON, when using FIFO trigger to write additional data in FAST_TX mode)
INT[18]	CCA completion	CCA execution start	(1)Normal mode (ED value average times + IDLE_WAIT setting) × Average period (2) IDLE detection mode ○IDLE detection (ED value average times + IDLE_WAIT setting) × Average period ○BUSY detection ED value average times × Average period Average period is 16μs.
INT[19]	TX Length error	-	When setting Length for [TX_PKT_LEN_H/L: B0 0x7A/0x7B]
INT[20]	TX FIFO access error	-	(1)When data is written with no FIFO free space (2)When adding to FIFO causes overflow (3)When there is no data to transmit during transmission
INT[21]	Reserved	-	-
INT[22]	General purpose timer 1	Timer start	General purpose timer 1 completion General purpose timer clock cycle * Division setting [GT_CLK_SET: B0 0x33] * General purpose timer interval setting [GT1_TIMER: B0 0x34]
INT[23]	General purpose timer 2	Timer start	General purpose timer 2 completion General purpose timer clock cycle * Division setting [GT_CLK_SET: B0 0x33] * General purpose timer interval setting [GT2_TIMER: B0 0x35]

*1 Before issuing TX_ON, writing full-length TX data to the TX_FIFO.

(3) Clearing interrupt conditions

The following table shows the condition of clearing each intereupt. As a procedure to clear the interrup, it is recommended that the interrupt to be cleared after masking the interrupt.

Interrupt notification		Recommended clearing timing for interrupts
INT[0]	CLK stabilization completion	
INT[1]	VCO calibration completion Out of VCO adjusting voltage range detected	
INT[2]	PLL unlock detection	
INT[3]	RF state transition completion	
INT[4]	FIFO-EMPTY	Clear before the next EMPTY trigger generation timing
INT[5]	FIFO-FULL	Clear before the next FULL trigger generation timing
INT[6]	Wake-up timer completion	
INT[7]	Clock calibration completion	
INT[8]	Data reception completion	Clear before the next packet reception
INT[9]	CRC error	Clear before the next packet reception
INT[10]	Diversity search completion	After this interrupt occurred
INT[11]	RX Length error	
INT[12]	Reserved	
INT[13]	SyncWord detection	
INT[14]	Field check	
INT[15]	Sync error	
INT[16/]	Data transmission completion	Clear before the next packet transmission
INT[17]	TX Data request accept completion	Clear before the next packet reception
INT[18]	CCA completion	clear before the next CCA execution (Note) Interrupt clearance clears CCA result as well.
INT[19]	TX Length error	
INT[20]	TX FIFO access error	Clear before the next packet transmission
INT[21]	Reserved	
INT[22]	General purpose timer 1	
INT[23]	General purpose timer 2	

○Low speed clock shift detection function

ML7404 has low speed shift detection function to compensate inaccurate clock generated by RC oscillator (external clock or internal RC oscillation circuits). By detecting frequency shift of the wake up timer, host can set wake-up timer parameters which taking frequency shift into consideration. More accurate timer operation is possible by adjusting wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) or continuous operation timer interval ([WU_DURATION: B0 0x31]).

Setting	Register
Frequency shift detection clock frequency setting	[CLK_CAL_SET: B0 0x70]
Clock calibration time	[CLK_CAL_TIME: B0 0x71]
Clock calibration result value	[CLK_CAL_H: B0 0x72], [CLK_CAL_L: B0 0x73]

This function is to measure low speed wake-up timer cycle by using accurate high speed internal clock and count result will be stored in [CLK_CAL_H/L: B0 0x72/0x73] registers. Above setting and count numbers are as follows:

High speed clock counter = {Wakeup timer clock cycle[SLEEP/WU_SET:B0 0x2D(2)] *
Clcok calibration time setting ([CLK_CAL_TIME:B0 0x71(5-0)]) /
{master clock cycle (36MHz) / clock division setting value ([CLK_CAL_SET: B0 0x70(7-4)])}

Clock calibration time is as follows:

Clock calibration time[s] = Wakeup timer clock cycle * Clock calibration time setting

[Example]
Assuming no division in the internal high speed clock, calibration time is set as 10 cycle. Set 1,000 to Wake-up interval timer:

condition: wake-up timer clock frequency = 32.768kHz
detection clock division setting CLK_CAL_DIV[3:0][CLK_CAL_SET: B0 0x70(7-4)] = 0b0000
clock calibration time setting [CLK_CAL_TIME:B0 0x71] = 0x0A
wake-up timer interval [WUT_INTERVAL_H/L:B0 0x2F,30] = 0x03E8(1000)

Theorical high speed clock count = (1/32.768kHz) ***** 10 / (1/36MHz)
= 10986(0x2AEA)

If getting [CLK_CAL_H/L:B0 0x72,73] = 0x2A03 (10755)
Counter difference = 10755 - 10986 = -231
Frequency shift = 1/[{1/32.768kHz + (-231) / 10 ***** 1/36MHz }] - 32.768kHz = 703.78Hz
Then finding wake-up timer clock frequency accuracy is +2.18% higher. And the compensation vale (C) is calcurared as below:

C = Wake-up timer interval([WUT_INTERVAL_H/L:B0 0x2F,30]) ***** frequecy shift / 32.768
= 1000 ***** 703.78Hz / 32.768kHz
=21

Therefore, setting [WUT_INTERVAL_H/L:B0 0x2F,30] = 1000 +21 = 1021 = 0x03FD to achive more accurate inteval timinig.

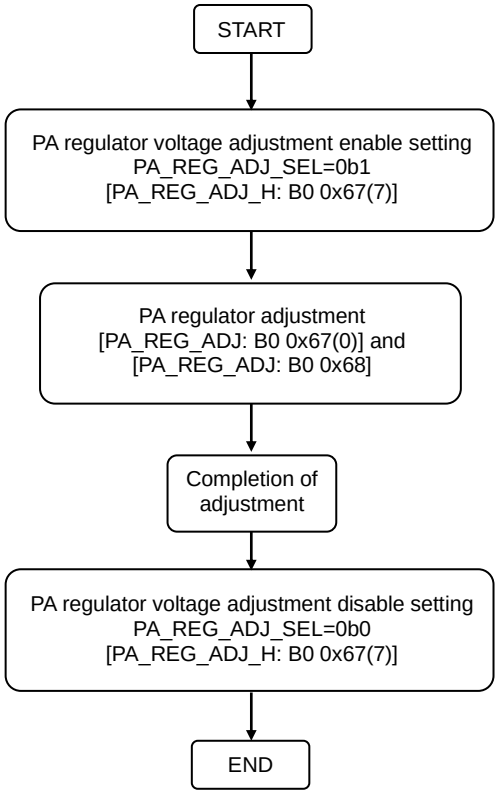
(Note)
1) If calibration time is too short, or if the clock division setting value is large and the high speed clock counter has low time resolution, calibration accuracy will be diminished.
2) In case of [CLK_CAL_TIME: B0 0x71]=0x3F with the master clock set to 36MHz, this exceeds the upper limit of the clock calibration result status ([CLK_CAL_H/L: B0 0x72/73]). Thus, be sure to set a value less than 0x3E.

■LSI Adjustment items and Adjustment Method

●PA Adjustment

ML7404 has a circuit of maximum 50mW output. Output power can be controlled by adjusting PA regulator voltages.
PA regulator voltages are adjustable in PA_REG_ADJ([PA_REG_ADJ_H/L: B0 0x67/68]) total 511 levels).
Be sure to enter the setting in such a manner that the PA regulator voltage is [VDD_PA applied voltage - 0.3V] or less.

【Flow of the output power adjustment】
(1) FSK Mode
PA regulator output voltage setting (PA_REG_ADJ[8:0]([PA_REG_ADJ_H/L: B0 0x67/68])) will be reflected on the output power by setting PA regulator voltage adjustment enable setting (PA_REG_ADJ_SEL([PA_REG_ADJ_H: B0 0x67(7)])) to 0b1.



(2) BPSK Mode
The output power is adjusted by PA_REG_ADJ[8:0]([PA_REG_ADJ_H/L: B0 0x67/68]) like FSK mode. Furthermore, it is necessary to change [BPSK_STEP_SET0: B10 0x04]-[BPSK_STEP_SET59: B10 0x3F] according to adjusted PA_REG_ADJ. Please compute [BPSK_STEP_SET0: B10 0x04]-[BPSK_STEP_SET59: B10 0x3F] based on “ML7404_InitializationTable_vX.XX.xlsm” and write adjustment value in registers.

●I/Q Adjustment

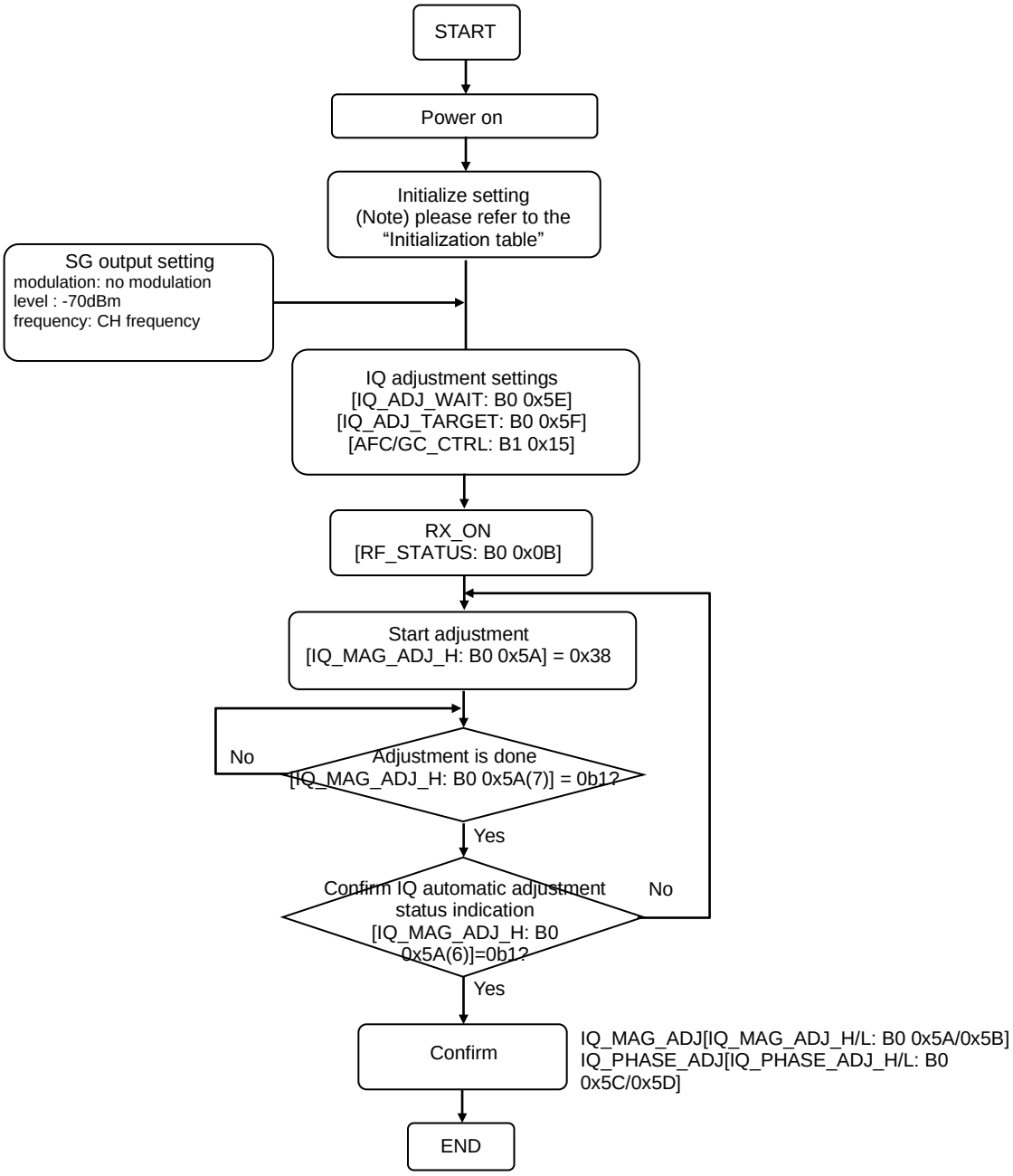
Image rejection ratio can be adjusted by tuning the internal IQ signal balance. The adjustment procedure is as follows:

1. Input the channel frequency signal from SG to the ANT pin.
   Input signal: no modulation wave
   Input frequency: channel frequency
   Input level: -70dBm
2. Set the following registers for I/Q adjustment.

Register name	Setting value
[CHFIL_BW: B0 0x54]	0x14
[DEC_GAIN: B0 0x60]	0x0C
[IQ_ADJ_WAIT: B0 0x5E]	0x00
[IQ_ADJ_TARGET: B0 0x5F]	Make an adjustment according to the conditions used.
[AFC/AGC_CTRL: B1 0x15]	0x00

3. Set IQ_ADJ_START([IQ_MAG_ADJ_H: B0 0x5A(4)]) = 0b1 and LOCAL_SEL([IQ_MAG_ADJ_H: B0 0x5A(5)]) = 0b1(Upper Local setting) after RX_ON, and then start the adjustment.
4. Indicate the adjustment completion by IQ_ADJ_DONE([IQ_MAG_ADJ_H: B0 0x5A(7)]) = 0b1. After that, adjusted values are stored into IQ_MAG_ADJ([IQ_MAG_ADJ_H/L: B0 0x5A/0x5B]) and IQ_PHASE_ADJ([IQ_PHASE_ADJ_H/L: B0 0x5C/0x5D]). The comparison result of the adjusted RSSI value and the RSSI judgment threshold is displayed in IQ_ADJ_RSLT([IQ_MAG_ADJ_H: B0 0x5A(6)]) as a result of IQ automatic adjustment. If IQ_ADJ_RSLT = 0b0 is displayed, that the adjusted RSSI value is larger than the RSSI judgment threshold, retry the IQ adjustment.
   However, even if IQ adjustment is repeated, IQ adjustment value will not necessary turn into below a threshold value.

○I/Q adjustment flow

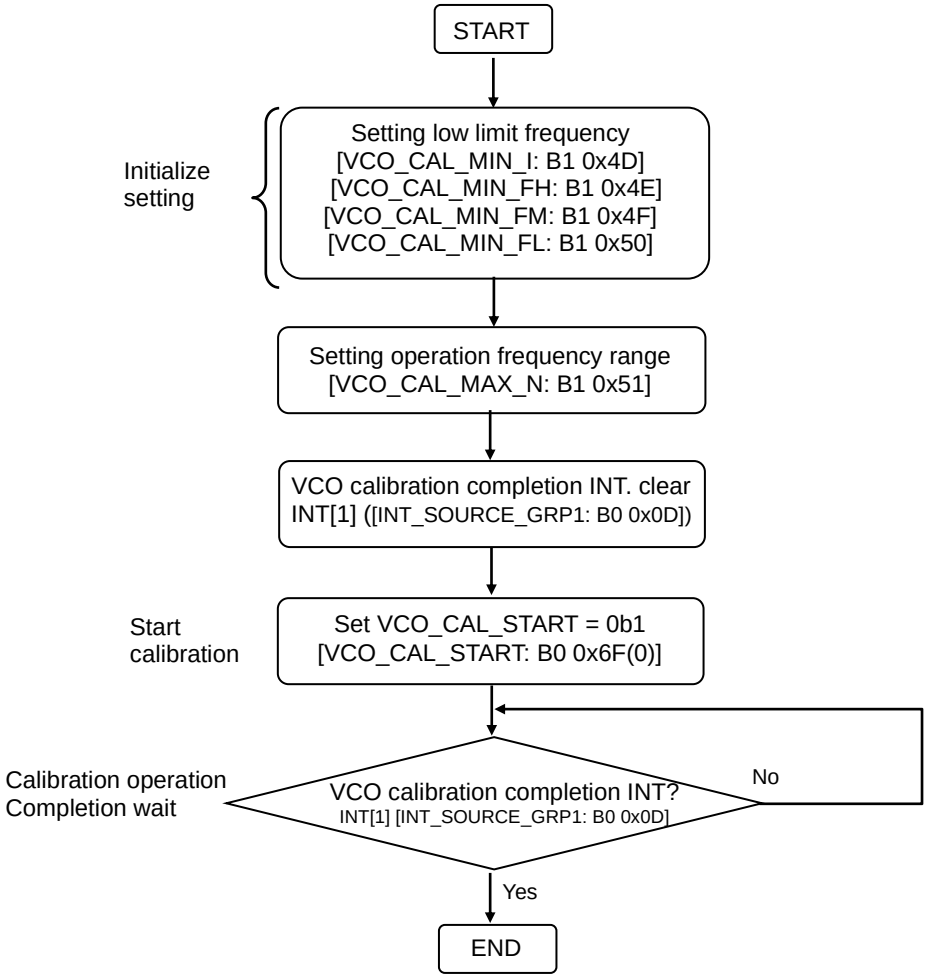


●VCO Adjustment

In order to compensate VCO operation margin, optimized capacitance compensation value should be set in each frequency. This capacitance compensation value can be acquired by VCO calibration.

By performing VCO calibration when power-up or reset, acquired capacitance compensation values for upper limit and lower limit of operation frequency range, based on this value optimised capacitance value is applied during TX/RX operation.

○VCO adjustment flow
The following flow is the procedure for acquiring capacitance compensation value when power-up or reset.



(Note)
VCO calibration should be performed only during IDLE state .

VCO calibration is necessary every 2.6ms to 8.8ms.
After completion, capacitance compensation values are stored in the following registers.

Capacitance compensation value at low limit frequency: [VCAL_MIN: B1 0x52]
Capacitance compensation value at upper limit frequency: [VCAL_MAX: B1 0x53]

In actual operation, based on the 2 compensation values, the most optimized capacitance value for the frequency is calculated and applied. The calculated value is stored in [VCO_CAL: B0 0x6E] register.

By evaluation stage, if below values are stored in the MCU memory and uses these values upon reset or power-up, calibration operation can be omitted.

Registers to be saved in the MCU memory.

[VCO_CAL_MIN_I: B1 0x4D]
[VCO_CAL_MIN_FH: B1 0x4E]
[VCO_CAL_MIN_FM: B1 0x4F]
[VCO_CAL_MIN_FL: B1 0x50]
[VCO_CAL_MAX_N: B1 0x51]
[VCAL_MIN: B1 0x52]
[VCAL_MAX: B1 0x53]

Even after the VCO calibration is performed, VCO adjustment voltage may be out of the optimum function range due to temperature change after the calibration. This LSI has a function which detects whether the VCO adjustment voltage is out of the optimum function range to display it in a register and notify MCU of it using an interrupt. This function is valid by setting VTUNE_COMP_ON([VTUNE_COMP_ON: B2 0x40(5)])=0b1.

VCO adjustment voltage lower limit threshold display: VTUNE_COMP_L[VCO_VTRSLT: B0 0x40(0)]
VCO adjustment voltage upper limit threshold display: VTUNE_COMP_H[VCO_VTRSLT: B0 0x40(1)]
Out of VCO adjustment voltage range detection and interrupt notification setting:
VTUNE_INT_ENB[VCO_VTRSLT: B0 0x40(2)]
PLL lock detection setting: PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)]

VTUNE_COMP_L [VCO_VTRSLT: B0 0x40(0)]	VTUNE_COMP_H [VCO_VTRSLT: B0 0x40(1)]	VCO adjustment voltage state
0	0	Within optimum function range
0	1	Out of optimum function range (over upper limit)
1	0	Out of optimum function (under lower limit)
1	1	Abnormal state

When detecting out of VCO adjustment voltage range, it is notified using the PLL unlock detection interrupt (INT2[INT_SOURCE_GRP1: B0 0x0D(2)]).

(Note)

1) For lower limit frequency, please use frequency at least 400kHz lower than operation frequency.
2) Upper limit frequency should be selected so that operation frequency is in the frequency range.
3) In case of like a channel change, if the setting frequency is outside of calibration frequency range, calibration has to be performed again with proper frequency.
4) When VCO is out of optimum function range, that is, 0b1 is indicated by either VTUNE_COMP_L/VTUNE_COMP_H, an RF operation can cause PLL unlock due to less VCO operation margin. Be sure to perform the calibration again or change the calibration value to ensure enough VCO operation margin.
5) PLL unlock detection interrupt (INT2[INT_SOURCE_GRP1: B0 0x0D(2)]) occurs due to the following two causes. The following tables show the LSI operation after interrupt generation for the PLL lock detection setting PLL_LD_EN([PLL_LOCK_DETECT:B1 0x0B(7)]) and detection timing of each cause.

•PLL When unlock occurs

LSI state	PLL unlock detection period	PLL lock detection setting and LSI operation after interrupt generation	
		PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)] = 0b1	PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)] = 0b0
TX	PA_ON = "H" period	Interrupt occurs, and TX is stopped forcibly	Interrupt occurs, and TX is continued
RX	RX enable = "H" period	Interrupt occurs, and RX is continued	Interrupt occurs, and RX is continued

•When VCO adjustment voltage is out of optimum operation range

LSI state	VCO adjustment voltage judgment timing	PLL lock detection setting and LSI operation after interrupt generation	
		PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)] = 0b1	PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)] = 0b0
TX	PA_ON rise	Interrupt occurs, and TX is stopped forcibly	Interrupt occurs, and TX is continued
RX	RX enable rise	Interrupt occurs, and RX is continued	Interrupt occurs, and RX is continued

○VCO lower limit frequency setting

VCO lower limit frequency can be set as described in the "channel frequency setting". I is set to [VCO_CAL_MIN_I:B1 0x4D] register, F is set to [VCO_CAL_MIN_FH:B1 0x4E], [VCO_CAL_MIN_FM:B1 0x4F], [VCO_CAL_MIN_FL:B1 0x50] registers in MSB – LSB order.

For details of N_{div}, please refer to the "Channel frequency setting".

VCO lower limit frequency setting value can be caluculated using the following formula.

$$I = \frac{f_{rf}}{f_{ref} / N_{div}} \quad \text{(Integer part)}$$

$$F = \left\{ \frac{f_{rf}}{f_{ref} / N_{div}} - I \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

f_{rf} : VCO lower limit frequency (Channel #0 frequency – 400kHz)

f_{ref} :PLL reference frequency (= master clock frequency: F_{MCK1})

I :Integer part of frequency setting

F :Fractional part of frequency setting

N_{div} :PLL dividing setting (1 or 2)

example) If operation low limit frequency(Channel#0 frequency) is 920MHz, setting value should be at least 400kHz lower than that, Then in following example, lower limit frequency is set to 919.6MHz, master clock frequency is 36MHz, N_{div}=1.

I = 919.6MHz/(36MHz/1) (Integer part) = 25(0x19)

F = {919.6MHz/(36MHz/1)-25} * 2^{20} (Integer part) = 570891(0x08B60B)

Setting values for each register is as follows:

[VCO_CAL_MIN_I : B1 0x1B] = 0x19
[VCO_CAL_MIN_FH : B1 0x1C] = 0x08
[VCO_CAL_MIN_FM : B1 0x1D] = 0xB6
[VCO_CAL_MIN_FL : B1 0x1E] = 0x0B

○VCO upper limit frequency setting

VCO upper limit frequency is calculated as following formula, based on low limit frequency value and VCO_CAL_MAX_N[3:0] ([VCO_CAL_MAX_N: B1 0x51(3-0)]). Please choose an upper limit frequency that satisfies the following formula.

When PLL dividing setting is performed by [PLL_DIV_SET: B1 0x1A], replace fref with FMCK1/Ndiv in the following formula. Regarding the value of N_{div}, please refer “Channel frequency setting”.

VCO upper limit frequency = {operation upper limit frequency – (operation lower limit frequency – 400kHz)} x N_{div}

VCO upper limit frequency(VCO_CAL_MAX_N[3:0]) is defined in the table below.

VCO_CAL_MAX_N[3:0]	VCO upper limit frequency[MHz]
0b0000	0
0b0001	1.125
0b0010	2.25
0b0011	4.5
0b0100	9
0b0101	18
0b0110	36
0b0111	72
Other than above	prohibited

●Energy Detection Value (ED Value) Adjustment

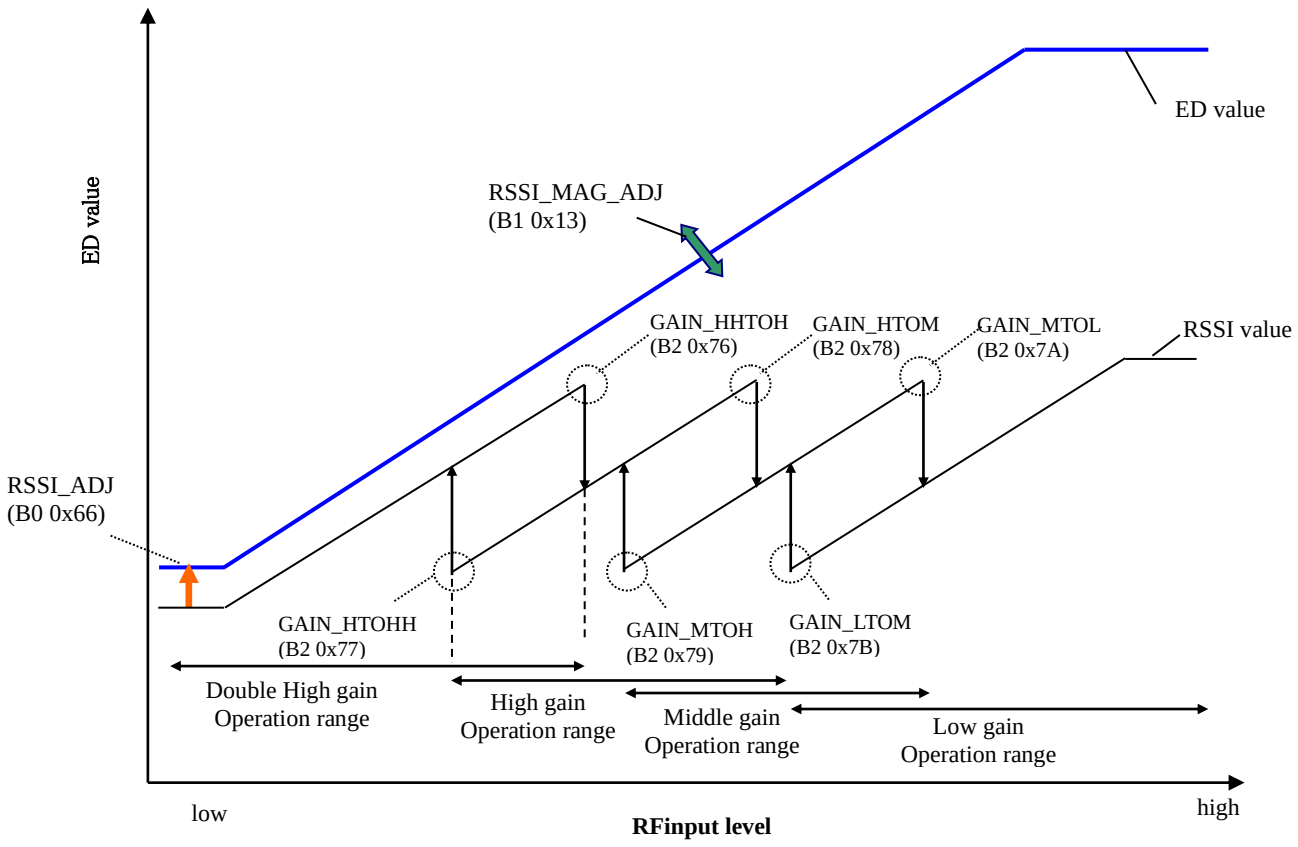
ED values are calculated from RF signals by performing the operation described in this section.
The following adjustment enables correction of variations in IC components.

To cover a wide input range, four gain states should be switched. Thus, ED values (the blue line in the following diagram) are calculated according to RF input levels. To acquire ED values, the following adjustment is available using the registers.

Adjustment item		Register	Remarks
Gain switch point	double high gain --> high gain	[GAIN_HHTOH: B2 0x76]	
	high gain --> double high gain	[GAIN_HTOHH: B2 0x77]	
	high gain --> middle gain	[GAIN_HTOM: B2 0x78]	
	middle gain --> high gain	[GAIN_MTOH: B2 0x79]	
	middle gain --> low gain	[GAIN_MTOL: B2 0x7A]	
	low gain --> middle gain	[GAIN_LTOM: B2 0x7B]	
Linearity	-	[RSSI_ADJ_H: B2 0x7C]	
	-	[RSSI_ADJ_M: B2 0x7D]	
	-	[RSSI_ADJ_L: B2 0x7E]	
RSSI tilt	-	[RSSI_MAG_ADJ: B1 0x13]	
ED value variation (same input level)	-	[RSSI_ADJ: B0 0x66]	

Variations for the same input level are adjusted in [RSSI_ADJ: B0 0x66]. Note that the adjustment corrects the value before the tilt is set by [RSSI_MAG_ADJ: B1 0x13]. If a positive value is set, the ED value cannot be decreased down to 0x00 in a low input signal level. If a negative value is set, the ED value may not be increased up to 0xFF in a high input level.

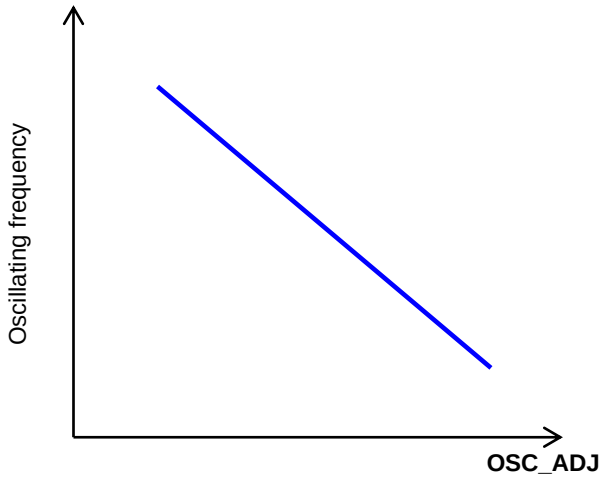
Values of RSSI_ADJ change according to the setting of the channel filter bandwidth and internal gain. Thus, adjustment is required for each setting of the data rate or channel filter bandwidth. Recommended initial values for each data rate are specified in “Initialization table.” As for gain switch points, be sure to set values specified in “Initialization table” and do not change the setting for adjustment, otherwise gains may not be switched properly.



●Oscillation Circuit Adjustment

In case of using a crystal oscillator, crystal oscillator frequency deviation can be tuned by adjusting load capacitance of XIN pin (pin#5) and XOUT pin (pin #6). Load capacitance can be adjusted by [OSC_ADJ1: B0 0x62] and [OSC_ADJ2: B0 0x63]. [OSC_ADJ1: B0 0x62] is coarse and [OSC_ADJ2: B0 0x63] is fine.

The relationship between the adjustment register value and the oscillation frequency is shown in the figure below.



●TRX Frequency Adjustment

An offset of TRX frequency caused by master clock deviation can be adjusted by registers FREQ_ADJ_SIGN([FREQ_ADJ_H: B1 0x42(7)]) and FREQ_ADJ [9:0]([FREQ_ADJ_H/L: B1 0x42(1-0)/0x43]).

For details of N_{div}, please refer to the “Channel frequency setting”.

The value for FREQ_ADJ [9:0] is calculated by the following formula.

$$FREQ\_ADJ = round\left[\left\{\frac{f_{adj}}{f_{ref} / N_{div}}\right\} \cdot 2^{20}\right]$$

Then

$FREQ\_ADJ$: value to adjust an offset of TRX frequency,

f_{adj} : An offset of TRX frequency [MHz],

f_{ref} : reference frequency for PLL (= master clock frequency: F_{MCK1})

N_{div} : PLL dividing setting (1 or 2)

$round[\ ]$: round to closest integer.

[Example]

When adjust +1kHz (= f_{adj}) under condition of master clock is 36MHz and N_{div}=1, the calculations are as follows.

$$FREQ\_ADJ = round\left[\left\{\frac{0.001MHz}{36MHz / 2}\right\} \cdot 2^{20}\right] = 29\ (0x01D)$$

Then set register values to

[FREQ_ADJ_H: B1 0x42] = 0x80

[FREQ_ADJ_L: B1 0x43] = 0x1D

The master clock deviation also can be adjusted by the “Oscillation Circuit Adjustment”.

■Other Functions

●Initilaization Table

ML7404 needs initilaization. For the value to each register, please refer to the “ML7404_Initilaization_Table” and “ML7404_RegisterSettingTool”.

●BER Measurement Setting

The following registers setting are necessary for RX side when BER measurement equipment is connected.

[DIO_SET: B0 0x0C] = 0x40
[MON_CTRL: B0 0x4D] = 0x80
[GPIO0_CTRL: B0 0x4F] to [GPIO3_CTRL: B0 0x52] for setting DCLK/DIO output pins.
[GAIN_HOLD: B1 0x0E] = 0x00

When termiate BER measurement and reurn from RX state, Force TRX_OFF should be issued by SET_TRX[3:0] ([RF_STATUS:B0 0x0b(3-0]) = 0b0011.

(Note)
BER measurement supports only FSK mode. Since use of Spectrum Spread function (DSSS mode) is not supported, check the packet error rate (PER) to evaluate reception features.

●Wireless M-Bus Mode Setting

As for Wireless M-Bus mode (S/T/C/R/F) setting, please refer “ML7404_InitializationTable_vX.XX.xlsm”.

●IEEE802.15.4g Mode setting

The following register settings are needed for supporting IEEE802.15.4g packet formats.

○Register settings common to TX and RX

Parameter	Register		Setting value
	Name	Address	
SyncWord length setting	SYNCWORD_LEN	B1 0x25	0x10
SyncWord #1 setting	SYNCWORD1_SET0	B1 0x27	0x00
	SYNCWORD1_SET1	B1 0x28	0x00
	SYNCWORD1_SET2	B1 0x29	0x90
	SYNCWORD1_SET3	B1 0x2A	0x4E
SyncWord #2 setting	SYNCWORD2_SET0	B1 0x2B	0x00
	SYNCWORD2_SET1	B1 0x2C	0x00
	SYNCWORD2_SET2	B1 0x2D	0x7A
	SYNCWORD2_SET3	B1 0x2E	0x0E
Whitening initializing state setting 1	WHT_INIT_H	B1 0x64	0x00
Whitening initializing state setting 2	WHT_INIT_L	B1 0x65	0xF0
Whitening polynomial generation setting	WHT_CFG	B1 0x66	0x10

○Register settings for TX

(1) In case of CRC16 without whitening

Parameter	Register		Setting value
	Name	Address	
Packet format setting	PKT_CTRL1	B0 0x04	0x16
CRC/Length length setting	PKT_CTRL2	B0 0x05	0x5D
Whitening setting	DATA_SET2	B0 0x08	0x00
PHR setting (bit15-11)	TX_PKT_LEN_H(bit7-3)	B0 0x7A	0b0_0010
CRC polynomial setting	CRC_POLY3	B1 0x16	0x00
	CRC_POLY2	B1 0x17	0x00
	CRC_POLY1	B1 0x18	0x08
	CRC_POLY0	B1 0x19	0x10

(2) In case of CRC16 with Whitening

Parameter	Register		Setting value
	Name	Address	
Packet format setting	PKT_CTRL1	B0 0x04	0x16
CRC/Length length setting	PKT_CTRL2	B0 0x05	0x5D
Whitening setting	DATA_SET2	B0 0x08	0x01
PHR setting (bit15-11)	TX_PKT_LEN_H(bit7-3)	B0 0x7A	0b0_0011
CRC polynomial setting	CRC_POLY3	B1 0x16	0x00
	CRC_POLY2	B1 0x17	0x00
	CRC_POLY1	B1 0x18	0x08
	CRC_POLY0	B1 0x19	0x10

(3) In case of CRC32 without Whitening

Parameter	Register		Setting value
	Name	Address	
Packet format setting	PKT_CTRL1	B0 0x04	0x16
CRC/Length length setting	PKT_CTRL2	B0 0x05	0xAD
Whitening setting	DATA_SET2	B0 0x08	0x00
PHR setting (bit15-11)	TX_PKT_LEN_H(bit7-3)	B0 0x7A	0b0_0000
CRC polynomial setting	CRC_POLY3	B1 0x16	0x02
	CRC_POLY2	B1 0x17	0x60
	CRC_POLY1	B1 0x18	0x8E
	CRC_POLY0	B1 0x19	0xDB

(4) In case of CRC32 with Whitening

Parameter	Register		Setting value
	Name	Address	
Packet format setting	PKT_CTRL1	B0 0x04	0x16
CRC/Length length setting	PKT_CTRL2	B0 0x05	0xAD
Whitening setting	DATA_SET2	B0 0x08	0x01
PHR setting (bit15-11)	TX_PKT_LEN_H(bit7-3)	B0 0x7A	0b0_0001
CRC polynomial setting	CRC_POLY3	B1 0x16	0x02
	CRC_POLY2	B1 0x17	0x60
	CRC_POLY1	B1 0x18	0x8E
	CRC_POLY0	B1 0x19	0xDB

○Register settings for RX

By setting IEEE802_15_4G_EN[PKT_CTRL1: B0 0x04(2)]=0b1, FCS information and whitening information is identified automatically from receved PHR.

Parameter	Register		Setting value
	Name	Address	
Packet format setting	PKT_CTRL1	B0 0x04	0x16
CRC/Length length setting	PKT_CTRL2	B0 0x05	0x5D/0xAD
Whitening setting	DATA_SET2	B0 0x08	0x01/0x00

■Flowchart

Category	Condition 1	Condition 2	Name of flow
Turn on sequence	-	-	(1) Initialization flow
TX/RX common Sequence	-	-	(1) RF state transition wait
TX Sequence	DIO mode	-	TX (1) DIO mode
	FIFO mode	Under 64bytes	TX (2) FIFO mode
		65bytes or more (FAST_TX)	TX (3) FIFO mode
	Automatic TX	-	TX (4) automatic TX
	Sigfox TX	-	TX (5) Sigfox TX
RX Sequence	DIO mode	-	RX (1) DIO mode
	FIFO mode	Under 64bytes	RX (2) FIFO mode
		65bytes or mode	RX (3) FIFO mode
	ACK transmission	-	RX (4) ACK transmission
	Field check	-	RX (5) Field checking
	CCA	Normal mode	RX (6) CCA normal mode
		Continuous execution mode	RX (6) CCA continuous execution mode
		IDLE detection mode	RX (6) CCA IDLE detection mode
	High speed carrier checking	-	RX (7) high speed carrier checking
	ED-SCAN	-	RX (8) ED-SCAN
	Antenna diversity	Execute diversity	RX (9) antenna diversity
SLEEP Sequence	SLEEP	-	(1) SLEEP
	Wake-up timer	-	(2) Wake-up timer
Error Process	Sync error	-	(1) CRC/Sync error
	TX FIFO access error	-	(2) TX FIFO access error
	PLL unlock	-	(3) PLL unlock
Data Rate Change Sequence	-	-	(1) Change Data Rate

●Turn On Sequence

(1) Initializing flow

In initialization status, Interrupt process, registers setting, VCO calibration are necessary.

(1) Interrupt process

Upon reset, INT0([INT_EN_GRP1: B0 0x10(0)], clock stabilization completion interrupt) is only enabled.
After hard reset is released, INT[0] (group1: clock stabilization completion interrupt) and INT[1] (group1: VCO calibration completion / Fuse access completion interrupt) will be detected.

(2) Registers setting

1) In case of Crystal oscillator circuits

Except for FIFO access registers([WR_TX_FIFO: B0 0x7C]、[RD_FIFO: B0 0x7F]), all the registers in BANK0 and BANK1 must be accessed after confirming Clock stabilized completion by reading INT0[INT_SOURCE_GRP1: B0 0x0D(0)]. For the detail of register settings for the initialization, please refer “Initialization table”.

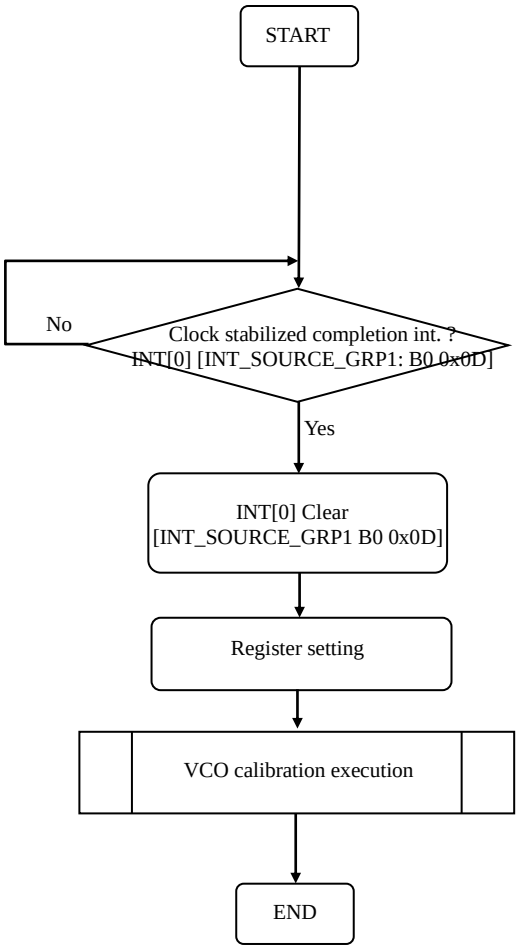
2) In case of TCXO

After TCXO_EN([CLK_SET2: B0 0x03(6)])=0b1 setting, all registers including FIFO access registers ([WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F]), are accessible after INT[0] notification.

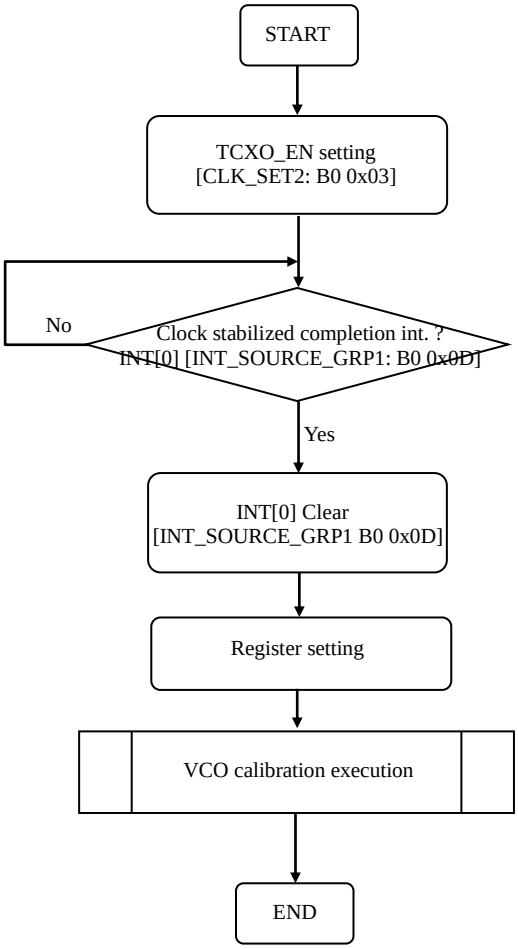
(3) VCO calibration

VCO calibration is executed after setting upper and low limit of the operation frequency.
For details, please refer to the “VCO adjustment”.

[In case of Crystal oscillator circuits]



[In case of TCXO]



(1)Interrupt process

(2)Register setting

(3)VCO calibration
(Note) For details, please refer to the “VCO adjustment”

●TX/RX Common Sequence

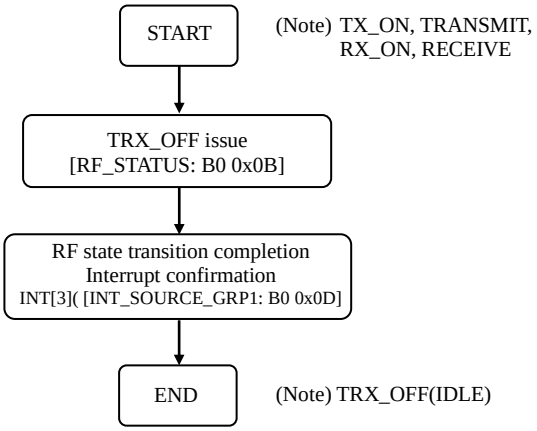
(1) RF state transition wait

If below setting for RF state change is selected, please confirm the completion of RF state transtion by INT[3] (group1: RF state transtion completion interrupt).

○RF state transition by [RF_STATUS: B0 0x0B]
○RF state transition by [RF_STATUS_CTRL: B0 0x0A]
●FAST_TX mode setting
●automatic TX setting
●RF state setting after TX completion
●RF state setting after RX completion
○RF state modification by wake-up timer setting

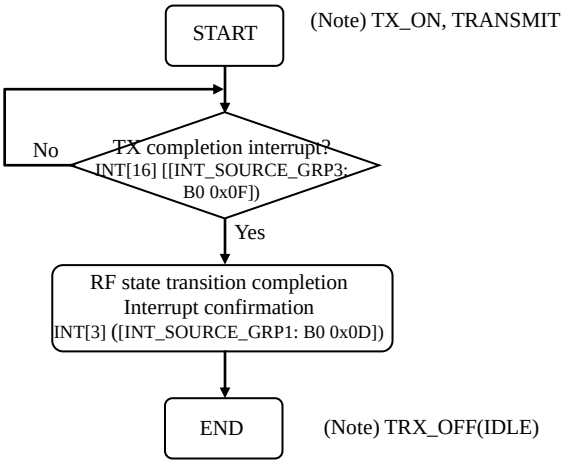
i) TRX_OFF flow
RF state change by [RF_STATUS: B0 0x0B]

SET_TRX[3:0] = 0b1000

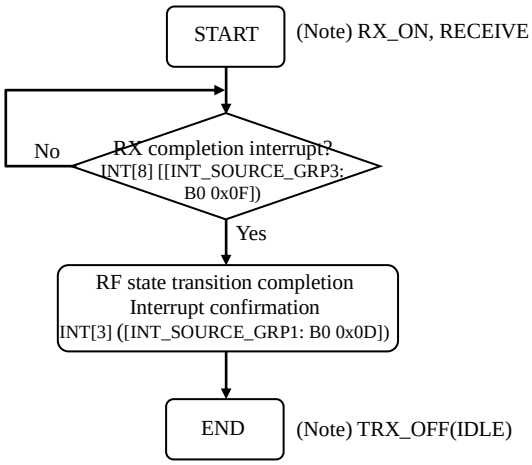


RF state change by [RF_STATUS_CTRL: B0 0x0A]

TXDONE_MODE[1:0] = 0b00

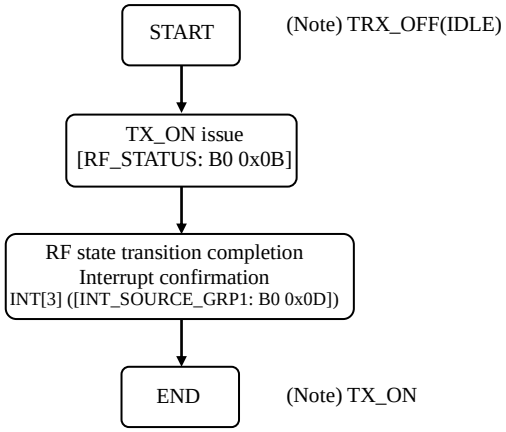


RXDONE_MODE[1:0] = 0b00



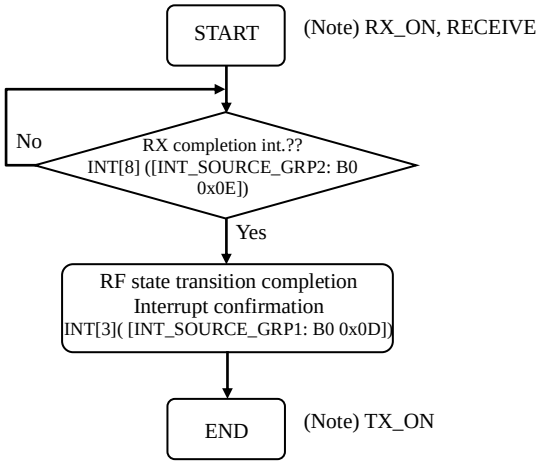
ii) TX_ON flow
RF state transition change by [RF_STATUS: B0 0x0B]

SET_TRX[3:0] = 0b1001

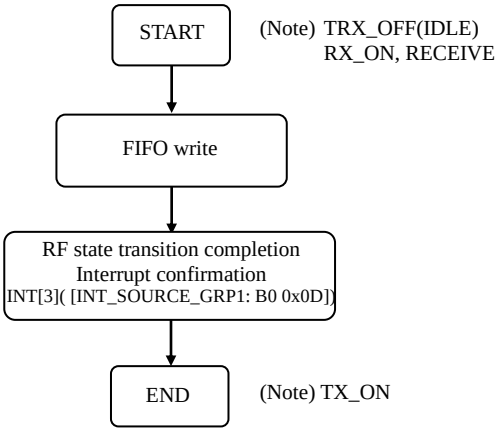


RF state transition by [RF_STATUS_CTRL]register(B0 0x0A)

RXDONE_MODE[1:0] = 0b10



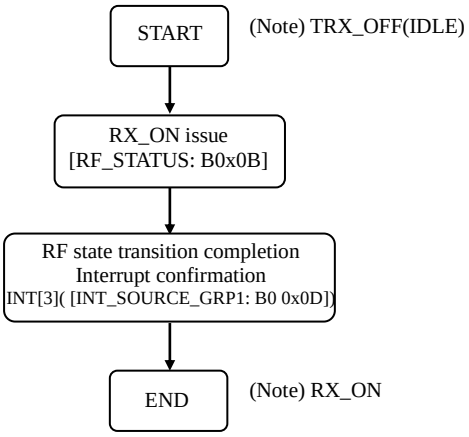
FAST_TX_EN = 0b1 and
AUTO_TX_EN = 0b1



iii) RX_ON flow

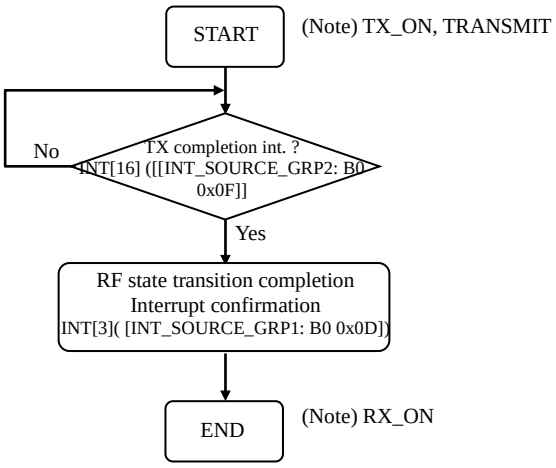
RF state change by [RF_STATUS: B0 0x0B]

SET_TRX[3:0] = 0b0110



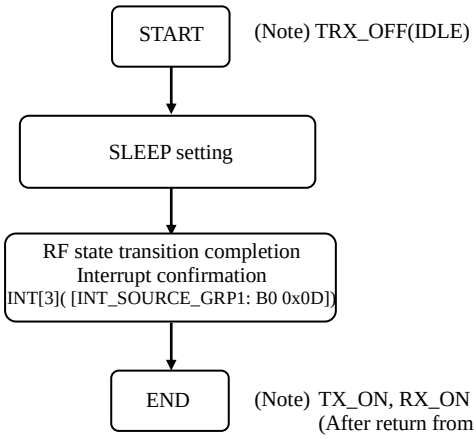
RF state change by [RF_STATUS_CTRL: B0 0x0A]

TXDONE_MODE[1:0] = 0b10



iv) Wake-up flow

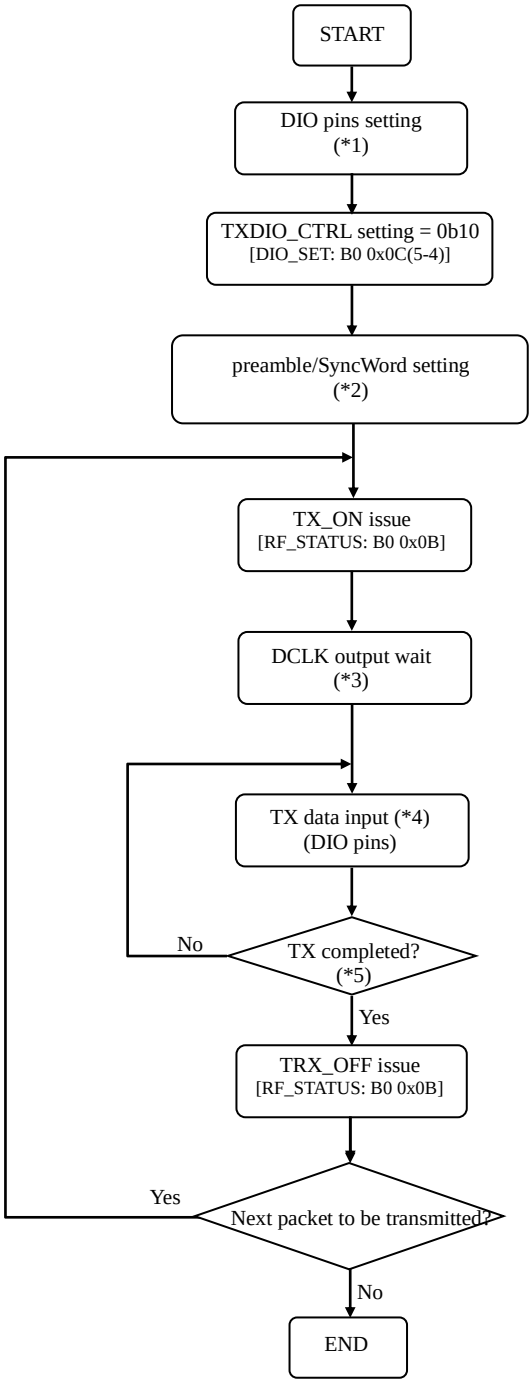
The following flow doses not apply to the case when waiting for INT[13] (group 2: SyncWord detection interrupt.) after wake-up.



● TX Sequence

(1) DIO mode

DIO(TX) mode can be selected by setting TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)]) = 0b01 or 0b10. In DIO mode, when issuing TX_ON by [RF_STATUS:B0 0x0B] register, data input on the pin related DIO will be transimitted to the air. After TX completion, TRX_OFF should be issued by [RF_STATUS:B0 0x0B] register.



*1 DIO/DCLK pins are defined as follows:
[GPIO0_CTRL: B0 0x4E]
[GPIO1_CTRL: B0 0x4F]
[GPIO2_CTRL: B0 0x50]
[GPIO3_CTRL: B0 0x51]
[EXT_CLK_CTRL: B0 0x52]
[SPI/EXT_PA_CTRL: B0 0x53]

*2 Preamble, SyncWord is transmitted based on the following registers.
Preamble [DATA_SET1: B0 0x07]
[TXPR_LEN_H/L: B0 0x42-43]
SyncWord [SYNCWORD1_SET0-3: B1 0x27-2A]
[SYNCWORD2_SET0-3: B1 0x2B-2E]
[SYNC_WORD_LEN: B1 0x25]
[DATA_SET2: B0 0x08]

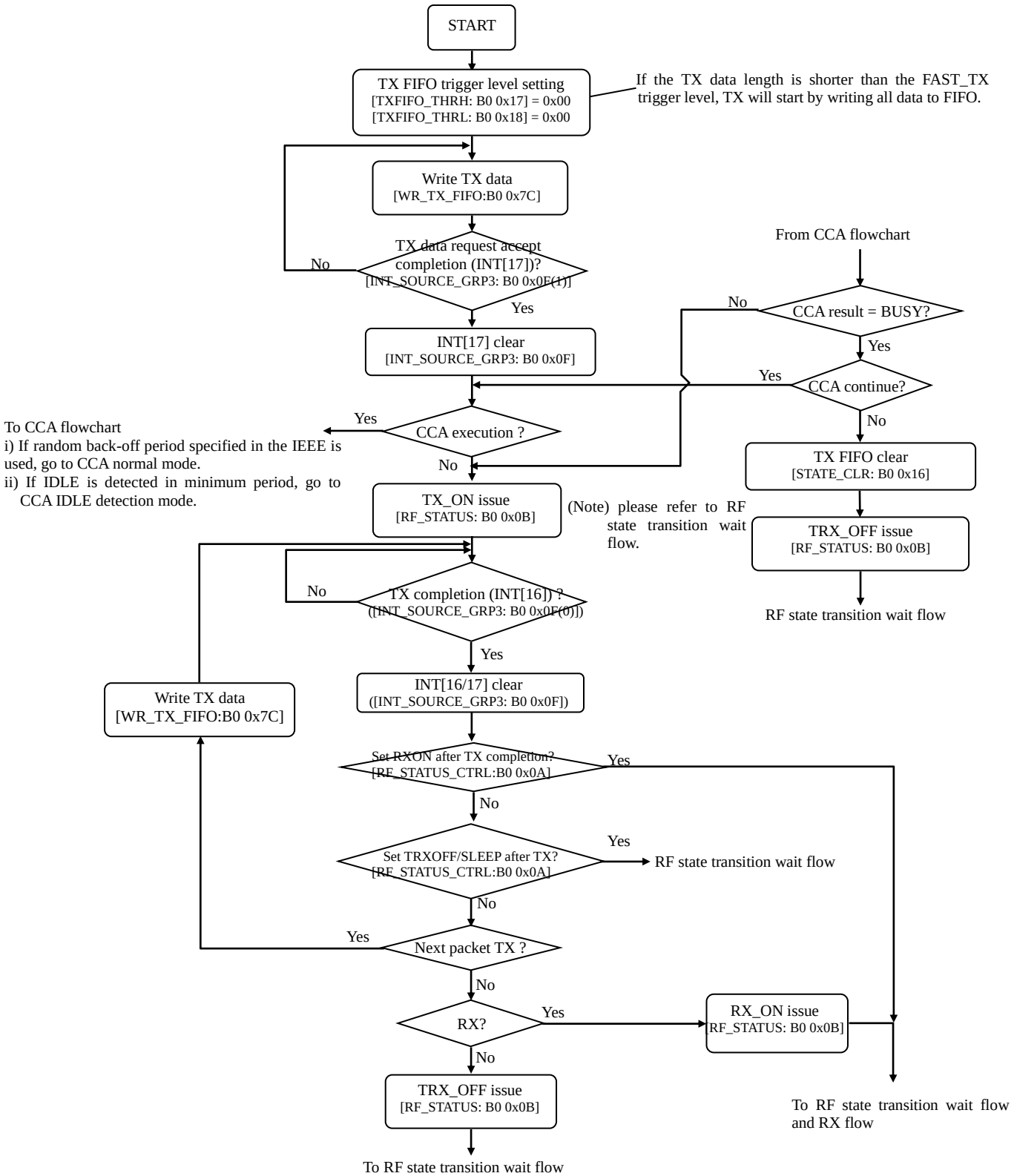
*3 Timing up to DCLK output varies depending on TX preamble, SFC, data rate.

*4 TX data must be input at falling edge of DCLK.

*5 Please refer to RF state transition wait flow.

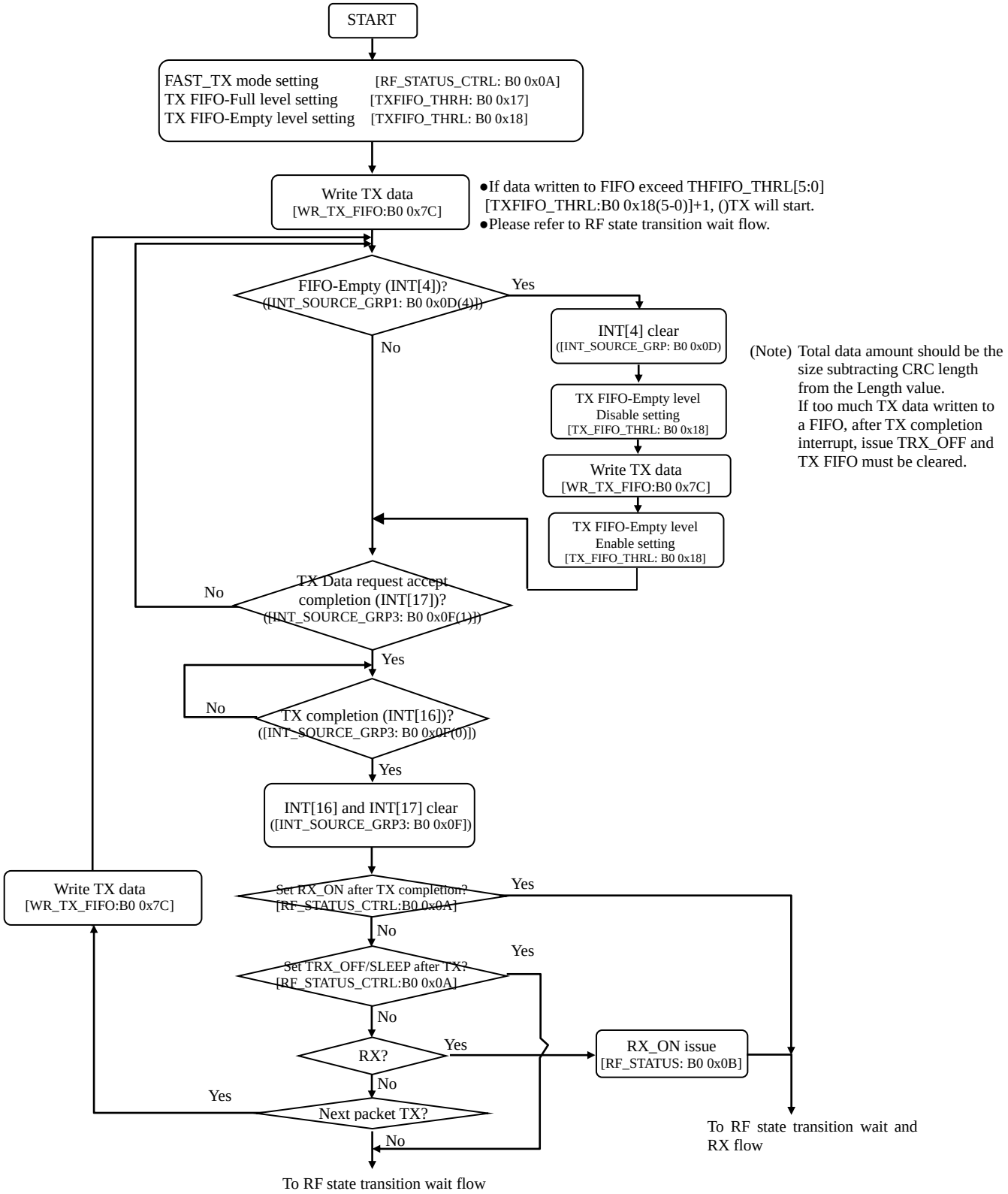
(2) FIFO mode (less than 64bytes)

FIFO mode (packet mode) can be selected by setting TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)]) = 0b00. In FIFO mode, data is written to the TX_FIFO by [WR_TX_FIFO:B0 0x7C] register. After writing full data of a packet, issuing TX_ON by [RF_STATUS:B0 0x0B] resister. Following preamble/SyncWord, TX_FIFO data is transmitted to the air. Upon TX completion interrupt (INT[16] group 3) occurs, interrupt must be cleared. If the next TX packet is sent, the next TX packet data is written to the TX_FIFO. If RX is expected after TX, RX_ON should be issued by [RF_STATUS: B0 0x0B] resister. TX can be terminated by issuing TRX_OFF by [RF_STATUS:B0 0x0B] register.



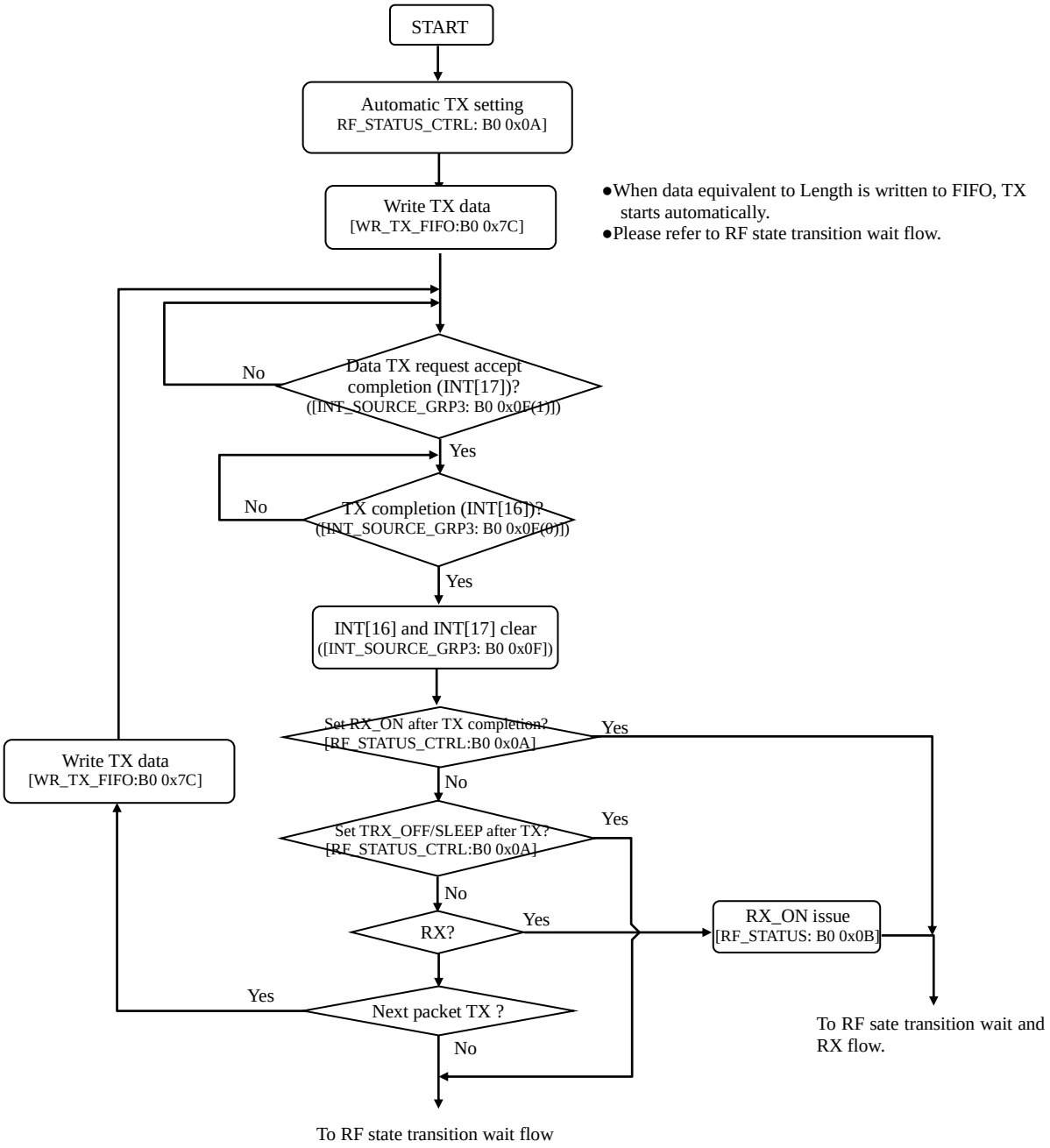
(3) FIFO mode (65bytes or more)

The Host must write TX data to the TX_FIFO while checking INT[5] (group1: FIFO-Full interrupt) and INT[4] (group1: FIFO-Empty interrupt) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operations are identical to the FIFO mode (less than 64bytes). Enabling FAST_TX mode by FAST_TX_EN ([RF_STATUS_CTRL: B0 0x0A(5)] = 0b1, TX will start when data amount written to the FIFO exceeds the bytes+1 in the [TXFIFO_THRL: B0 0x18].



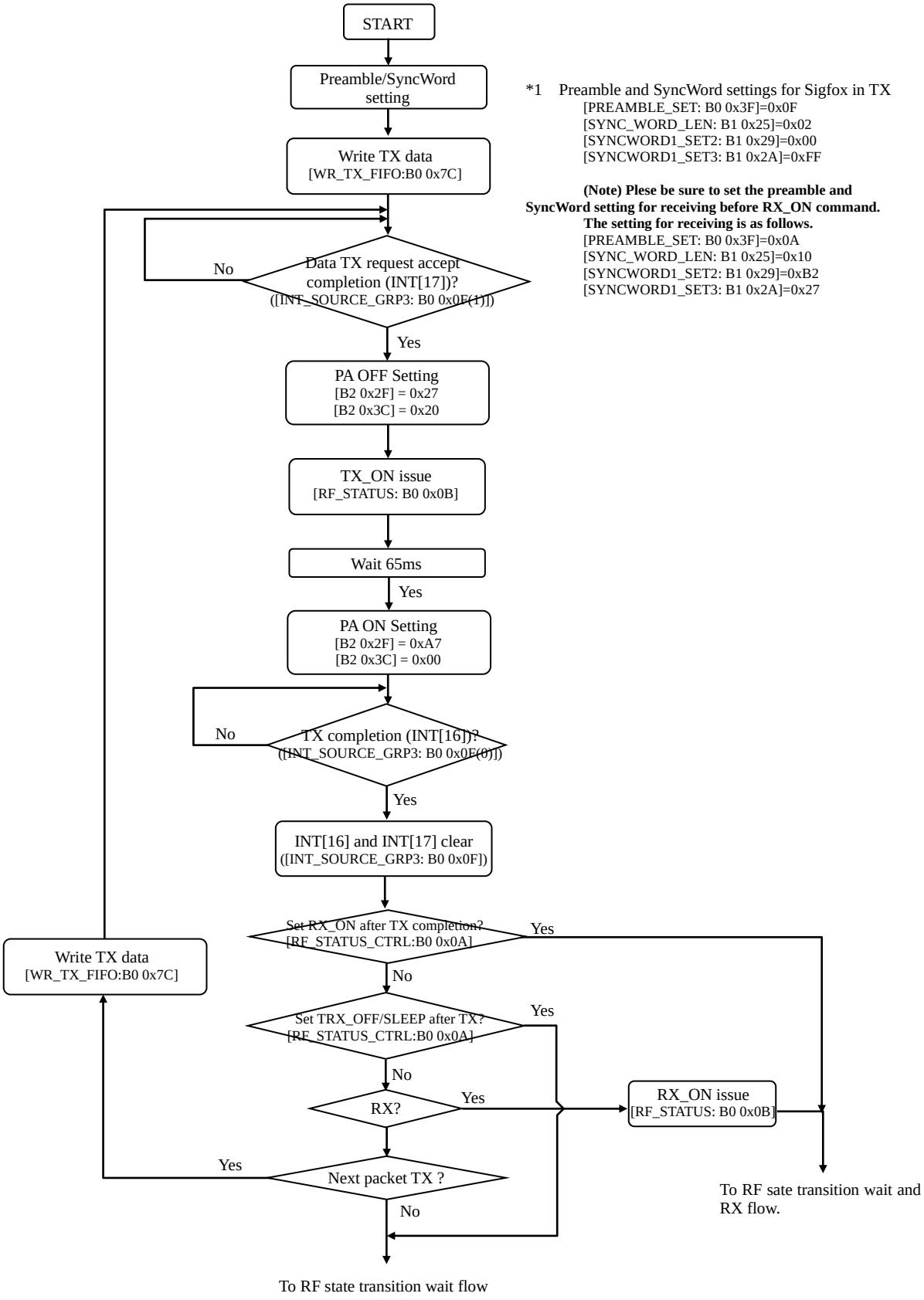
(4) Automatic TX (less than 64bytes)

If AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)] = 0b1, TX starts automatically when FIFO is filled with data equivalent to the Langth. Afer TX completion, RF state transition setting is by TXDONE_MODE ([RF_STATUS_CTRL: B0 0x0A(1:0)]).



(5) Sigfox TX

TX data is written to the TX_FIFO by [WR_TX_FIFO:B0 0x7C] register. After writing PA OFF setting([B2 0x2F]=0x27, [B2 0x3C]=0x20), issuing TX_ON by [RF_STATUS:B0 0x0B] resister. PA ON setting([B2 0x2F]=0xA7, [B2 0x3C]=0x00) is performed after the wait for 65ms from TX_ON command. A subsequent flow is the same as other transmission flow.



*1 Preamble and SyncWord settings for Sigfox in TX
[PREAMBLE_SET: B0 0x3F]=0x0F
[SYNC_WORD_LEN: B1 0x25]=0x02
[SYNCWORD1_SET2: B1 0x29]=0x00
[SYNCWORD1_SET3: B1 0x2A]=0xFF

(Note) Plese be sure to set the preamble and SyncWord setting for receiving before RX_ON command. The setting for receiving is as follows.
[PREAMBLE_SET: B0 0x3F]=0x0A
[SYNC_WORD_LEN: B1 0x25]=0x10
[SYNCWORD1_SET2: B1 0x29]=0xB2
[SYNCWORD1_SET3: B1 0x2A]=0x27

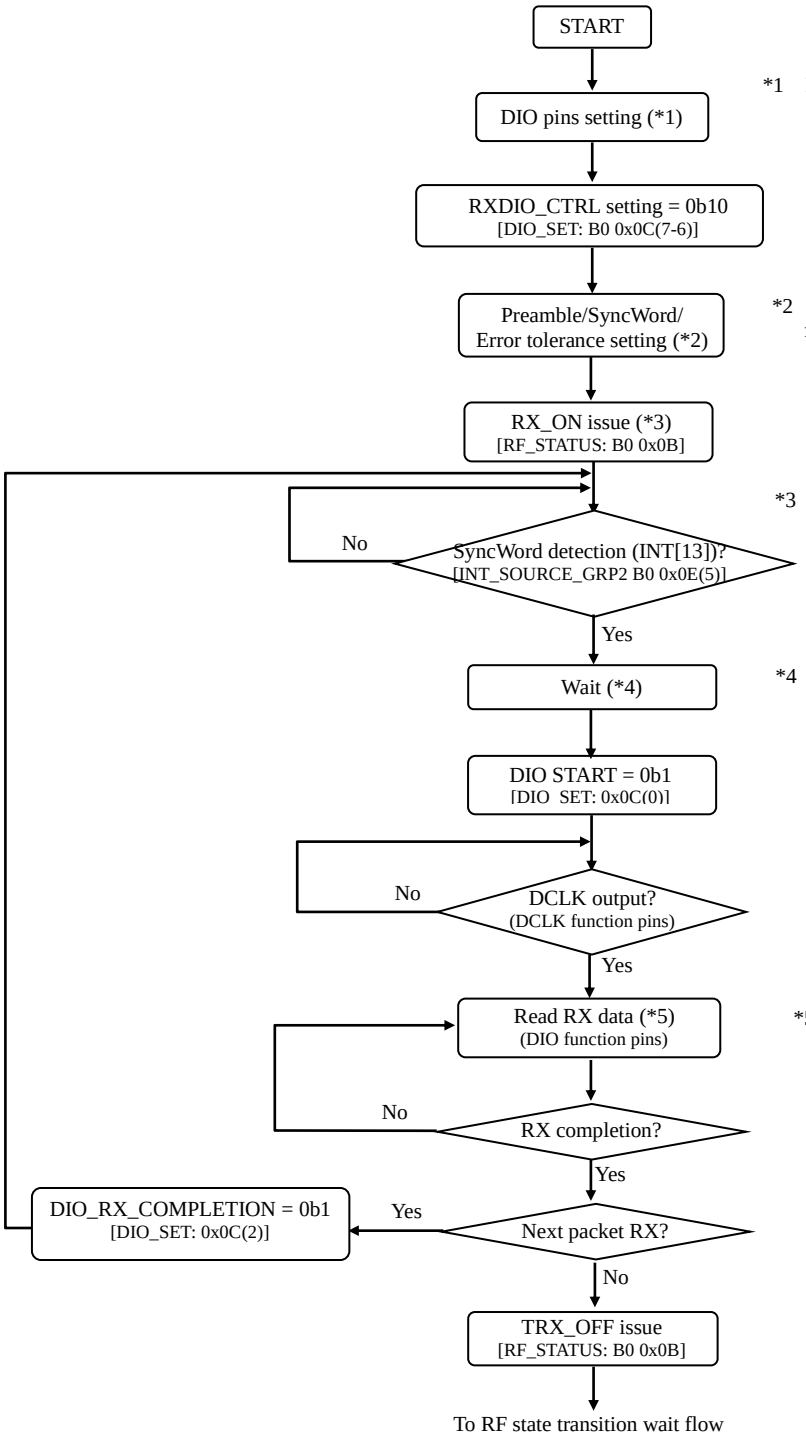
●RX Sequence

(1) DIO mode

DIO mode can be selected by setting RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)]) = 0b10/0b11. Upon setting DIO mode and issuing RX_ON by [RF_STATUS:B0 0x0B] register, SyncWord detection will be started.

○DIO outmupt mode 1 operation

While RXDIO_CTRL[1:0] = 0b10, after SyncWord pattern detection, RX data will be strored into the RX_FIFO. RX data stored in the RX_FIFO is output through DIO pins, if setting DIO_START ([DIO_SET: B0 0x0C(0)]) = 0b1. Upon RX completion, if more data is to be received, by setting DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)]) = 0b1 (DIO RX completion), the next packet will be ready to receive. In case of TRX_OFF, issuing TRX_OFF by [RF_STATUS:B0 0x0B] register.



*1 DIO/DCLK function pins setting
[GPIO0_CTRL: B0 0x4E]
[GPIO1_CTRL: B0 0x4F]
[GPIO2_CTRL: B0 0x50]
[GPIO3_CTRL: B0 0x51]
[EXT_CLK_CTRL: B0 0x52]
[SPI/EXT_PA_CTRL: B0 0x53]

*2 Preamble, SyncWord and Error tolerance are set by following registers.
Preamble [DATA_SET1: B0 0x07]
[SYNC_CONDITION1-3: B0 0x45-47]
SyncWord [SYNCWORD1_SET0-3: B1 0x27-2A]
[SYNCWORD2_SET0-3: B1 0x2B-2E]
[SYNC_WORD_LEN: B1 0x25]
[DATA_SET2: B0 0x08]

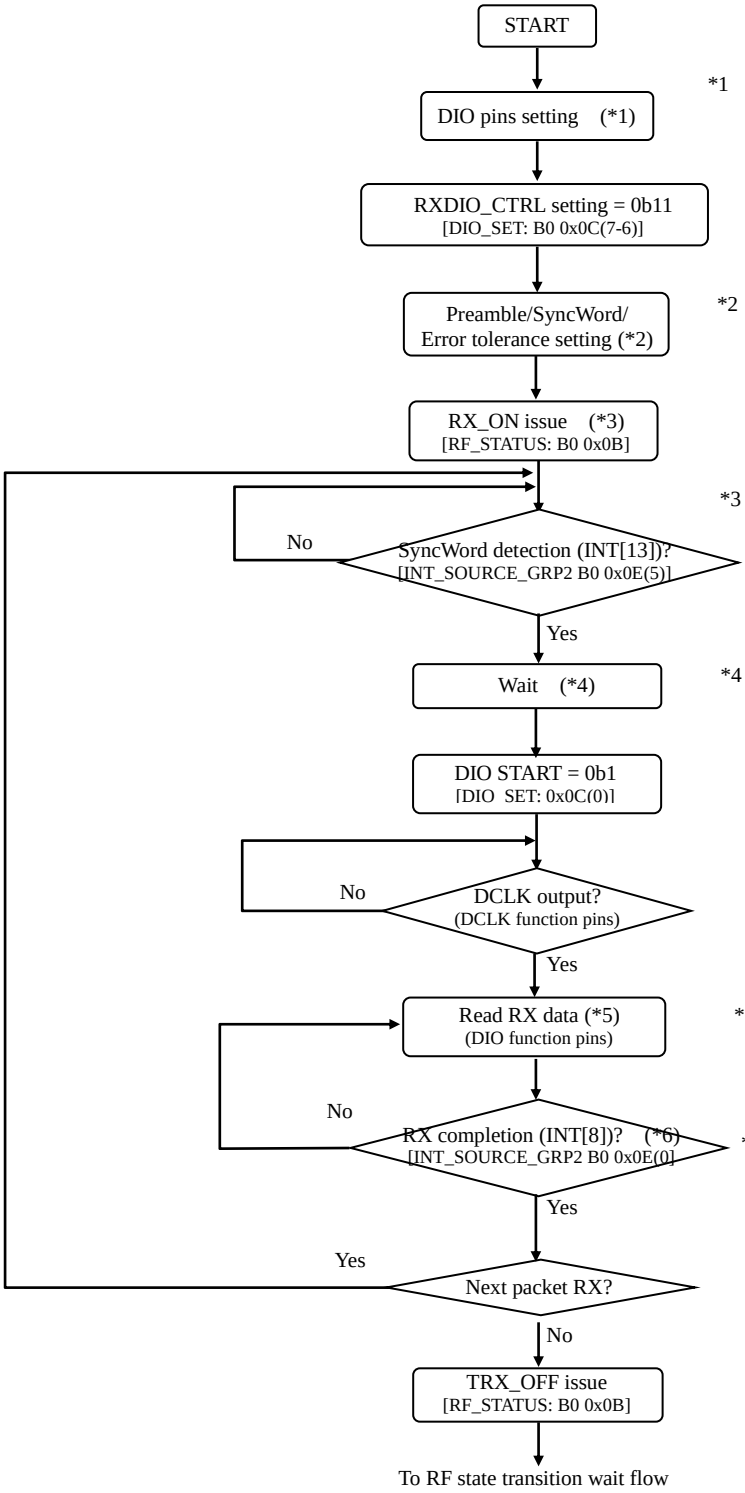
*3 Please refer to RF state transition wait flow.

*4 Wait time should be more than 1byte data receiving period.

*5 RX data must be transferred to the Host at rising edge of DCLK.

○DIO outmupt mode 2 operation

While RXDIO_CTRL[1:0] = 0b11, RX data (after L-field) will be stored into the RX_FIFO. RX data stored in the RX_FIFO is output through DIO pins, if setting DIO_START ([DIO_SET: B0 0x0C(0)]) = 0b1. Upon outputting RX data defined by L-field, RX is completed and generate RF completion interrupt (INT[8] group2). In case of TRX_OFF, issuing TRX_OFF by [RF_STATUS:B0 0x0B] register.



*1 DIO/DCLK function pins setting
[GPIO0_CTRL: B0 0x4E]
[GPIO1_CTRL: B0 0x4F]
[GPIO2_CTRL: B0 0x50]
[GPIO3_CTRL: B0 0x51]
[EXT_CLK_CTRL: B0 0x52]
[SPI/EXT_PA_CTRL: B0 0x53]

*2 Preamble, SyncWord and Error tolerance are set by following registers.
Preamble [DATA_SET1: B0 0x07]
[SYNC_CONDITION1-3: B0 0x45-47]
SyncWord [SYNCWORD1_SET0-3: B1 0x27-2A]
[SYNCWORD2_SET0-3: B1 0x2B-2E]
[SYNC_WORD_LEN: B1 0x25]
[DATA_SET2: B0 0x08]

*3 Please refer to RF state transition wait flow.

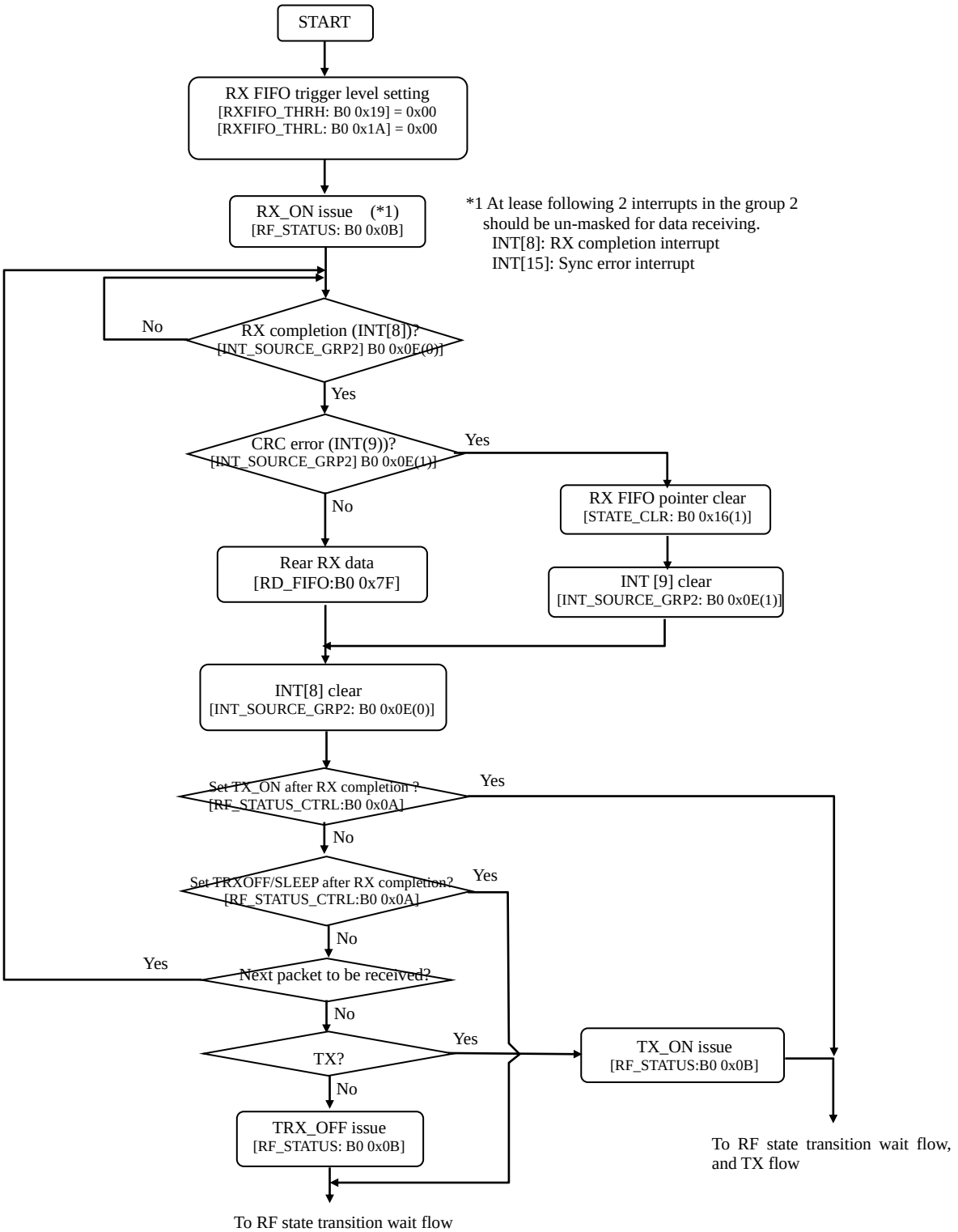
*4 Wait time should be more than Length field+ 1 byte data receiving period.
1byte period is decoded 8bits data. If using Manchester code, 1byte period becomes 160µs (@ 100kbps).

*5 RX data must be transferred to the Host at rising edge of DCLK.

*6 Upon outputting whole RX data. INT[8] will generate.

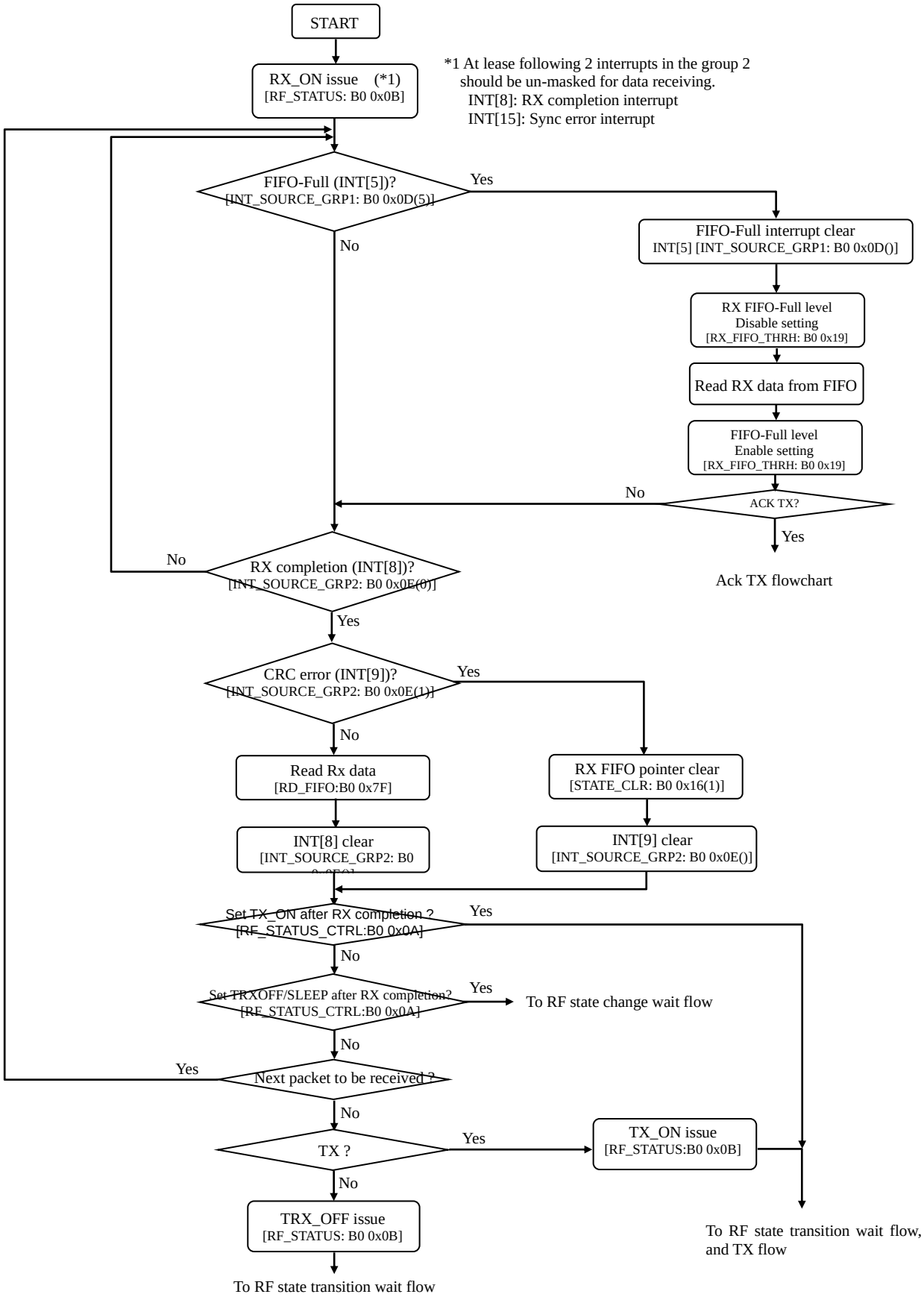
(2) FIFO mode (less than 64bytes)

FIFO mode can be selected by RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)]) = 0b00. After SyncWord detection, RX data will be stored into the RX_FIFO. Upon Data RX completion interrupt (INT[8] group2) occurs, the host will read RX data from [RD_FIFO:B0 0x7F] registers. If CRC errors interrupt (INT[9] group2) is generated, the next packet can be ready to receive without reading all current RX data by setting STATE_CLR1 [STATE_CLR: B0 0x16(1)](RX FIFO pointer clear). If FIFO-Full trigger and FIFO-Empty trigger are not used, please set 0b0 to both RXFIFO_THRH_EN([RXFIFO_THRH: B0 0x19(7)]) and RXFIFO_THRL_EN([RXFIFO_THRH: B0 0x1A(7)]) .



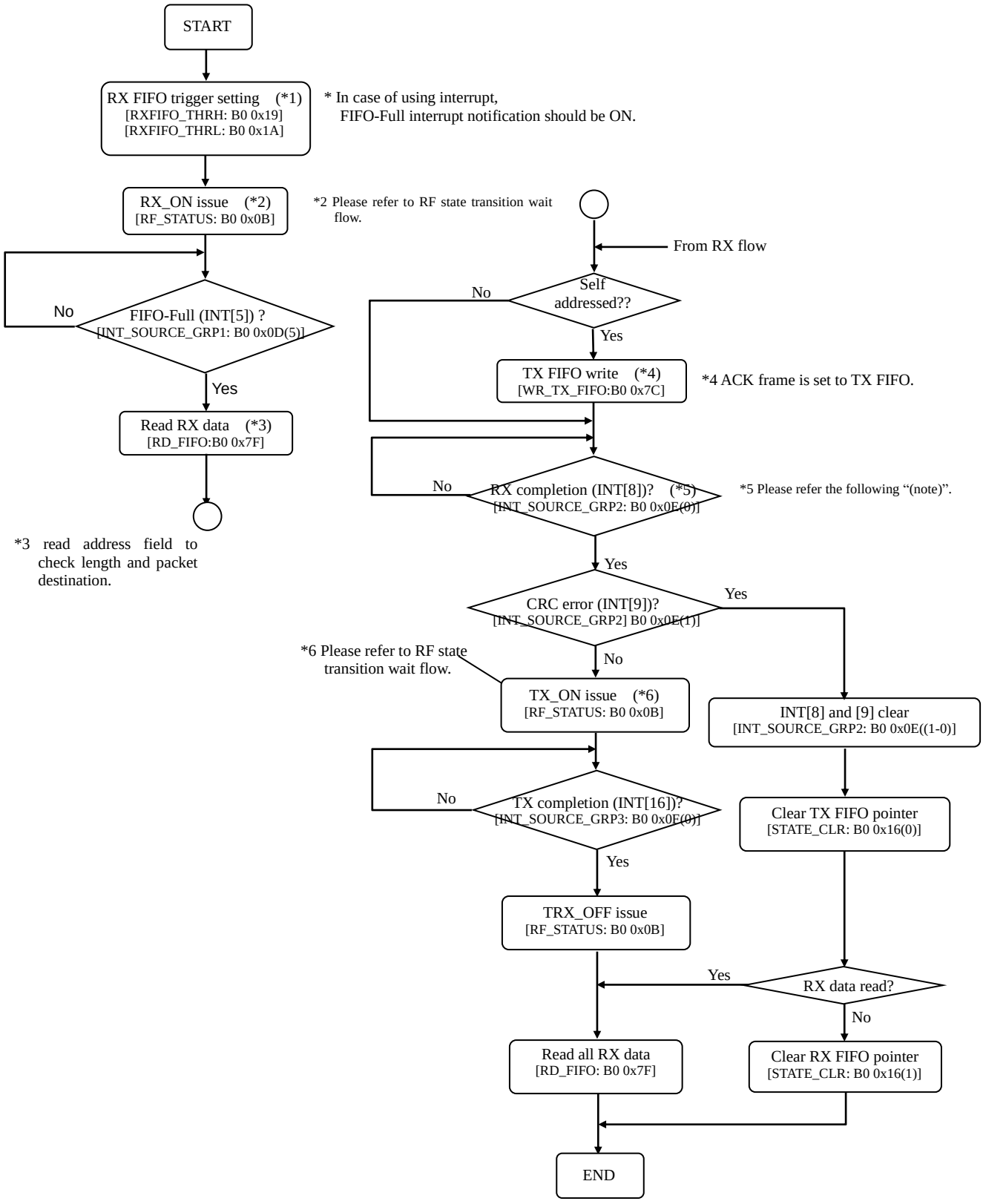
(3) FIFO mode (more than 65bytes)

The Host must read RX data from the RX_FIFO while checking INT[5] (group1: FIFO-Full interrupt) and INT[4] (group1: FIFO-Empty interrupt) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operations are identical to the FIFO mode (less than 64bytes).



(4) ACK transmission

ACK TX flow is as follows. During RX, ACK frame can be set in the TX FIFO.

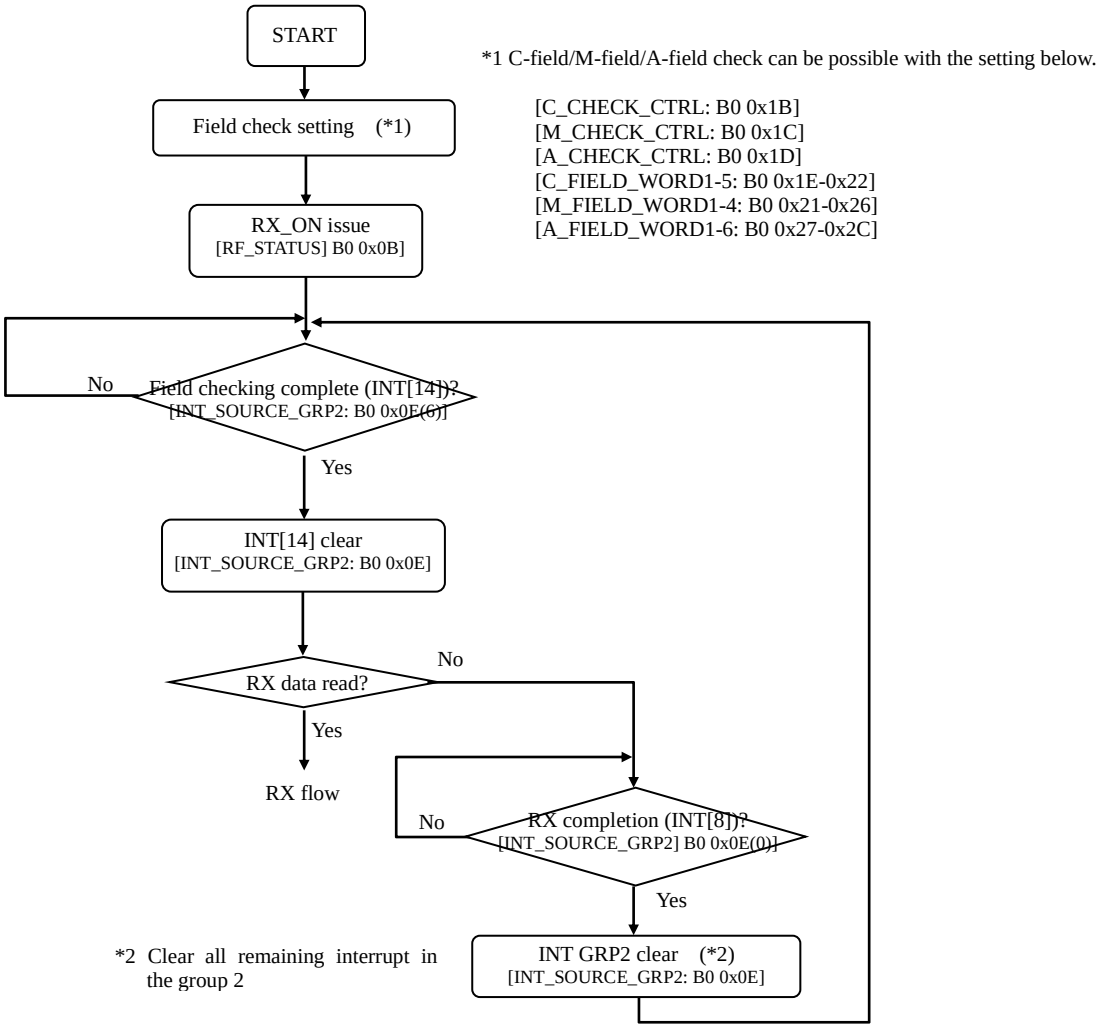


(Note)

- If setting “FAST_TX_EB = 0b1” or “AUTO_TX_EN = 0b1 or “RXDONE_MODE[1:0] = 0b01 (move to TX state)” at the [RF_STATUS:CTRL:B0 0x0A] register, moving to TX_ON state automatically after RX completion in above flowchart.
- Even if CRC error occurs, moving to TX_ON state. Since CRC errors interrupt (INT[9] group2) and RX completion interrupt (INT[8] group2) occur almost same timeing, Therefore in case of CRC error interrupt occurs, Force_TRX_OFF should be issued by [RF_STATUS:B0 0x0B] register withing the transition time from RX state to TX state(1.188ms), and clear TX FIFO pointer by [STATE_CLR:B0 0x16] register. When it is hard to issue Force_TRX_OFF during the trasition time due to MCU performance, “FAST_TX”, “AUTO_TX” and “move to TX state after RX completion” should be disabled. (In “FAST_TX”, trnasmitting conditoin depends on [TXFIFO_THRL:B0 0x18] register.)

(5) Field checking

After enabling Filedcheck functions, issuing RX_ON by [RF_STATU:B0 0x0B] register. According to the setting of CA_INT_CTRL ([C_CHECK_CTRL:B0 0x1B(6)], filed checking result (match or no match) can be notified by the interrupt INT[14](gropup2: Filed checking interrupt). Numbers of unmatched packets can be counted and stored into [ADDR_CHK_CTR_H/L: B1 0x62/0x63]) registers. This counter can be cleared by STATE_CLR4[STATE_CLR: B0 0x16(4)](Address check counter clear).



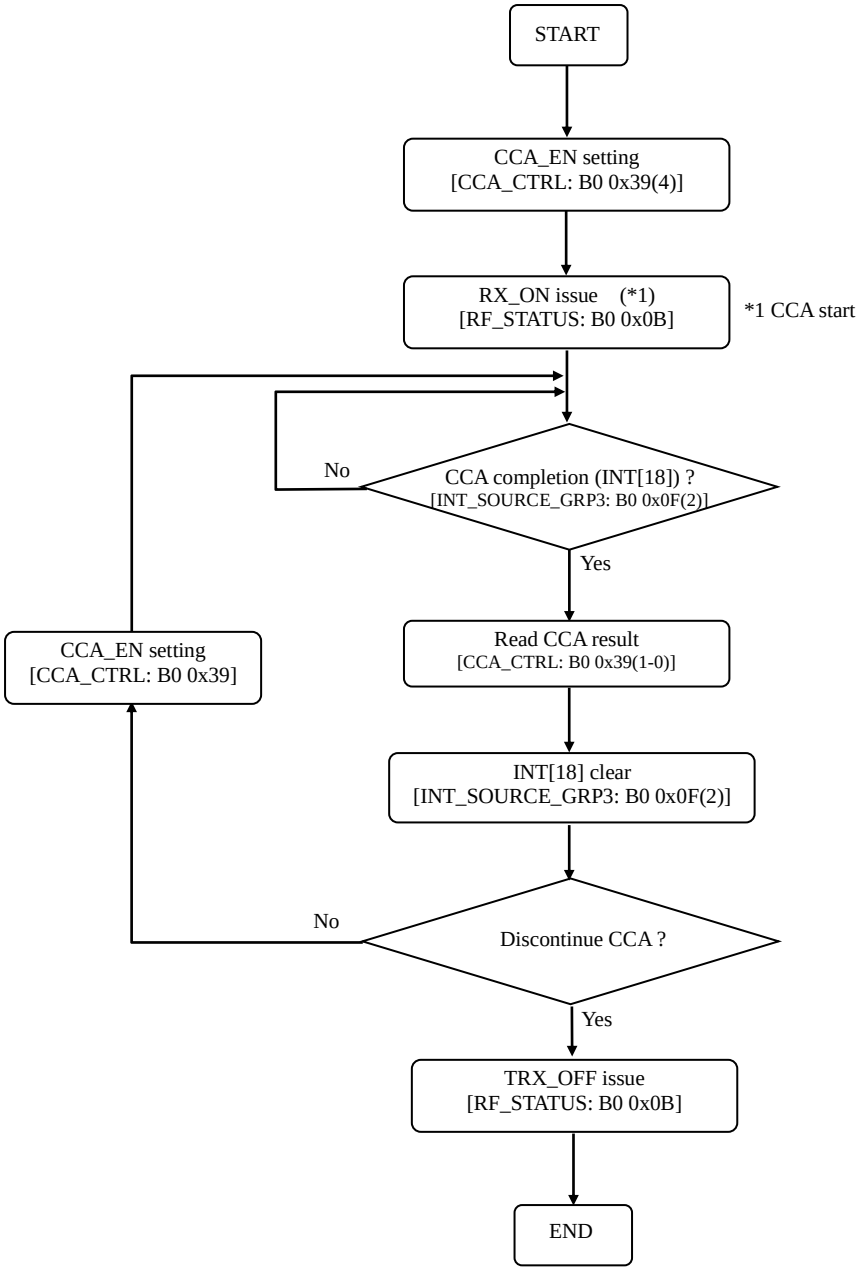
(6) CCA

○Normal mode

After setting CCA_EN([CCA_CTRL: B0 0x39(4)]) = 0b1, issuing RX_ON by [RF_STATU:B0 0x0B] register. Comparing aquired ED average value with CCA threshold value in [CCA_LVL: B0 0x37] register and noitce the result. After CCA execulation,CCA_EN is turned disable and RF maintaind RX_ON.

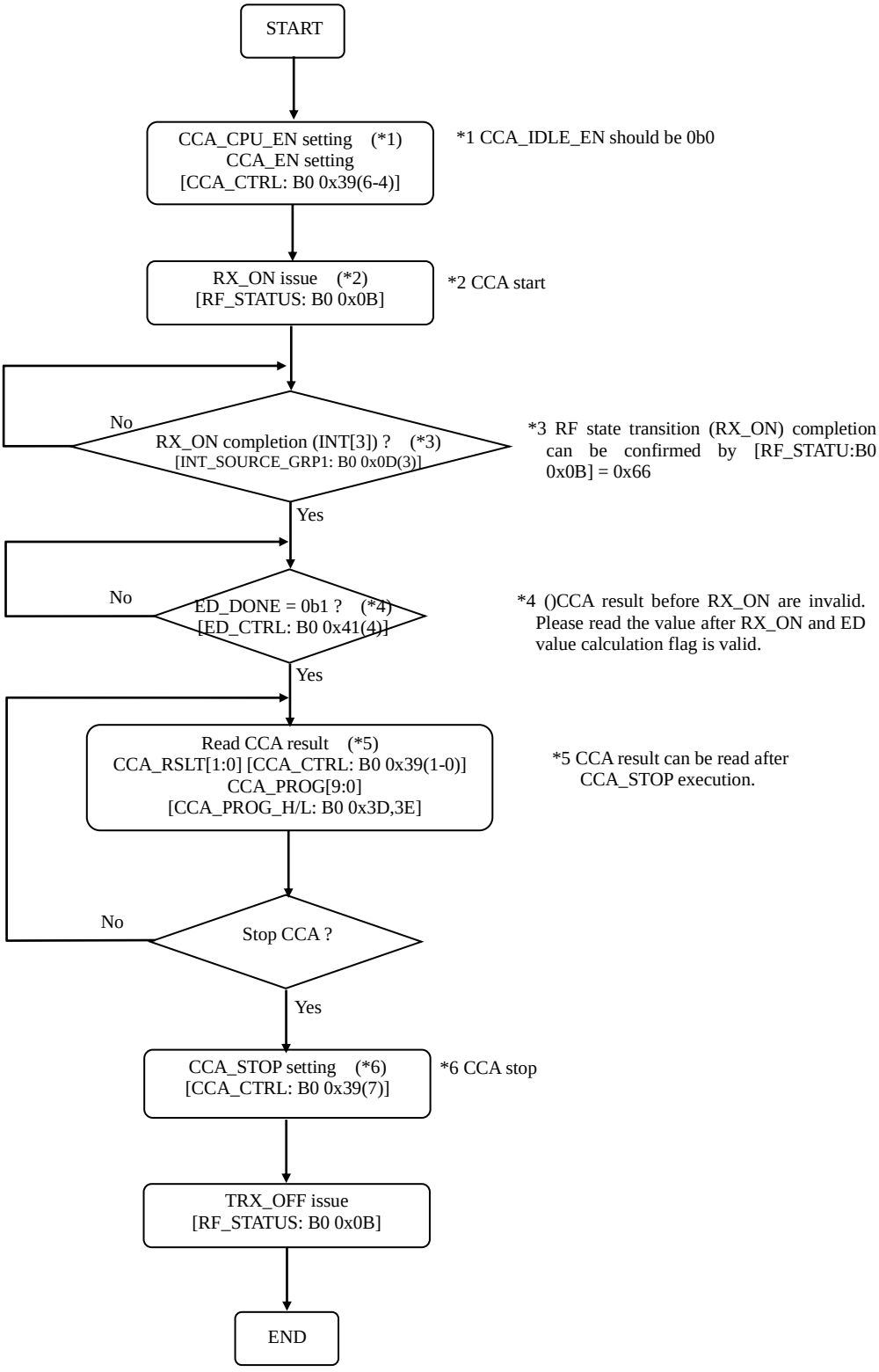
Even if set CCA_EN = 0b1 in the RX_ON state, CCA execulation is possible. CCA execulation is also possible during diversity. In this case, after CCA completion, diversity will be resumed automatically.

CCA can be performed during diversity search as well. In this case, diversity search is automatically restarted after CCA completion.



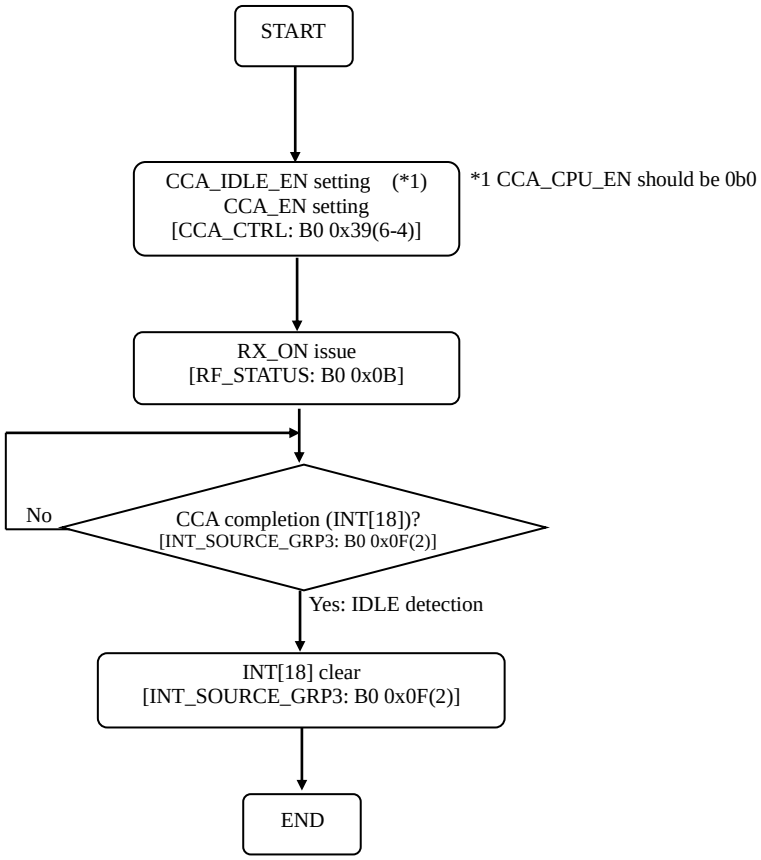
○Continuous mode

Continuous CCA mode is executed by issuing RX_ON by [RF_STATU:B0 0x0B] register after setting CCA_EN([CCA_CTRL: B0 0x39(4)]) = 0b1 and CCA_CPU_EN([CCA_CTRL: B0 0x39(5)]) = 0b1. In this mode, CCA continues until CCA_STOP([CCA_CTRL: B0 0x39(7)]) = 0b1 is set. CCA completion interupt (INT[18]: group3) is not generated. During CCA execution,CCA_RSLT([CCA_CTRL: B0 0x39(1-0)]), [CCA_PROG_L: B0 0x3E], [CCA_PROG_H: B0 0x3D] are constantly updated. The value will be kept by setting CCA_STOP([CCA_CTRL: B0 0x39(7)]) = 0b1.



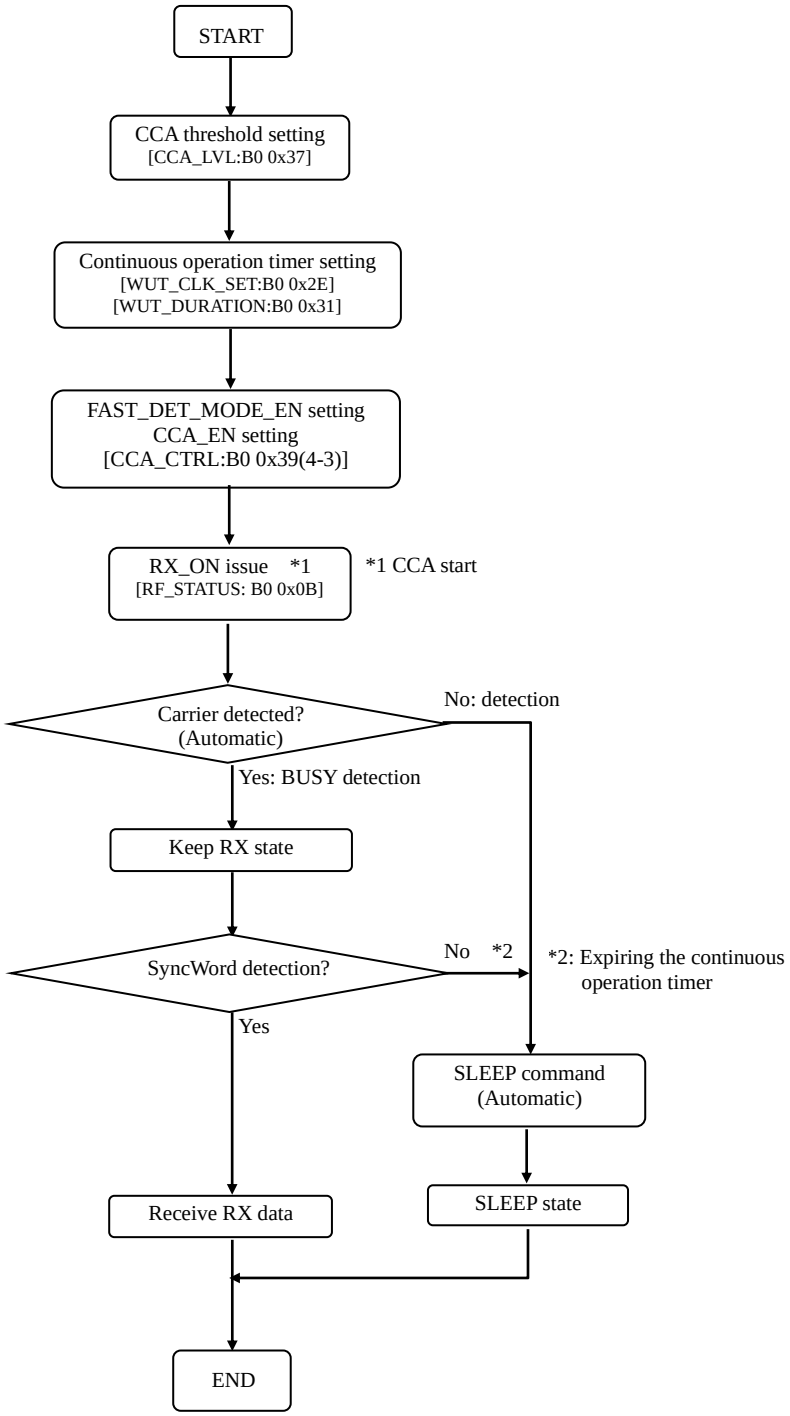
○IDLE detection mode

CCA is continuously executed untill IDLE is detected. CCA (IDLE detection mode) will be executing by issuing RX_ON by [RF_STATU:B0 0x0B] register after setting CCA_EN([CCA_CTRL: B0 0x39(4)]) = 0b1, CCA_IDLE_EN ([CCA_CTRL: B0 0x39(6)]) = 0b1.



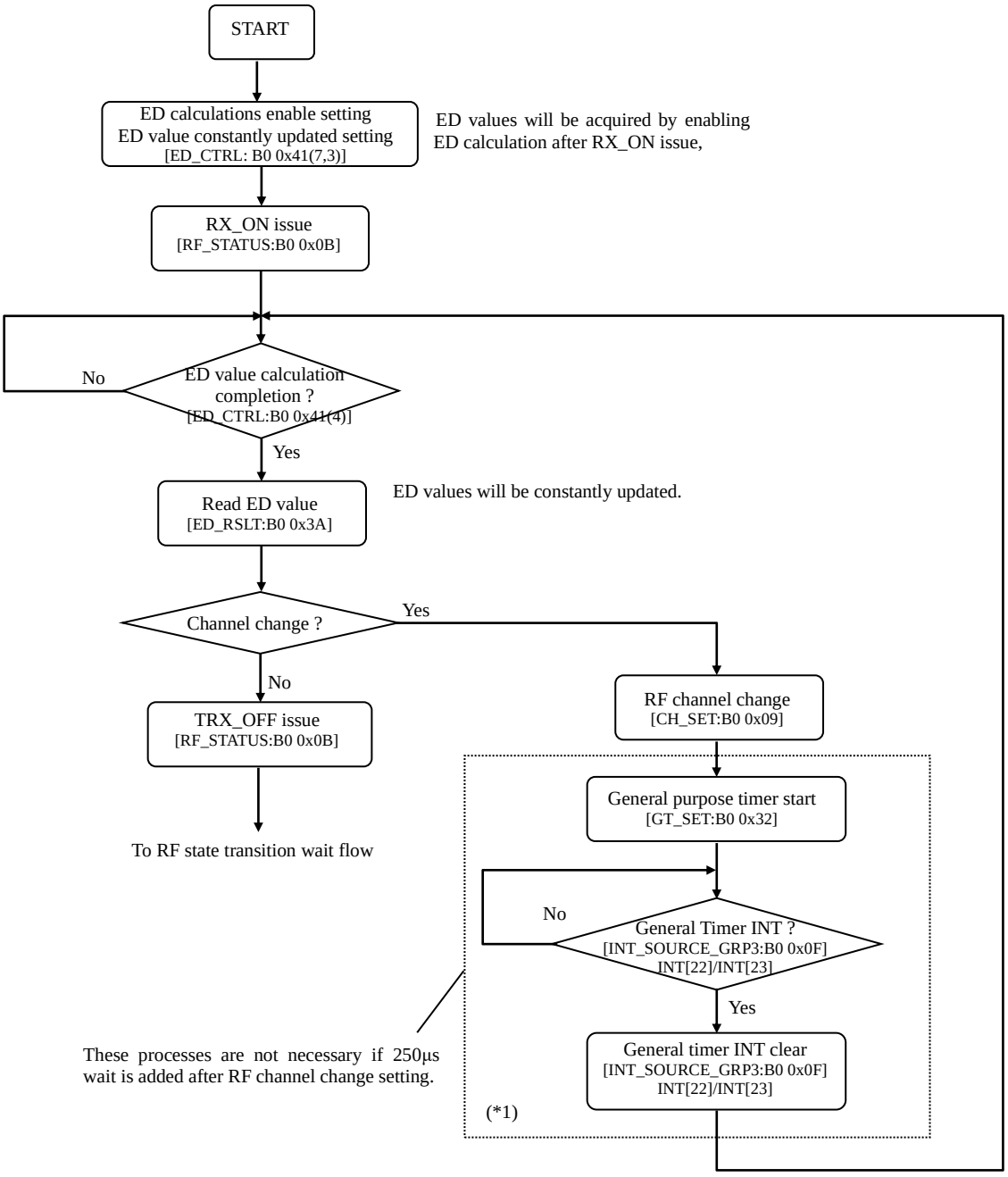
(7) High speed carrier checking mode

This mode is used for deciding whether continuing RX state or stoping RX state during RX state, based on RSSI level and SyncWord detection time. The value set in the [CCA_LVL:B0 0x37] register is used for RSSI level decision, continuous operation timer is used for SyncWord detection time decision. After decision, operation will automaticall switch to – either SLEEP state or RX state.



(8) ED-SCAN

ED value will be automatically acquired by issuing RX_ON by [RF_STATU:B0 0x0B] register after setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)]) = 0b1. ED value is constantly updated when ED_RSLT_SET([ED_CTRL:B0 0x41(3)]) = 0b0.

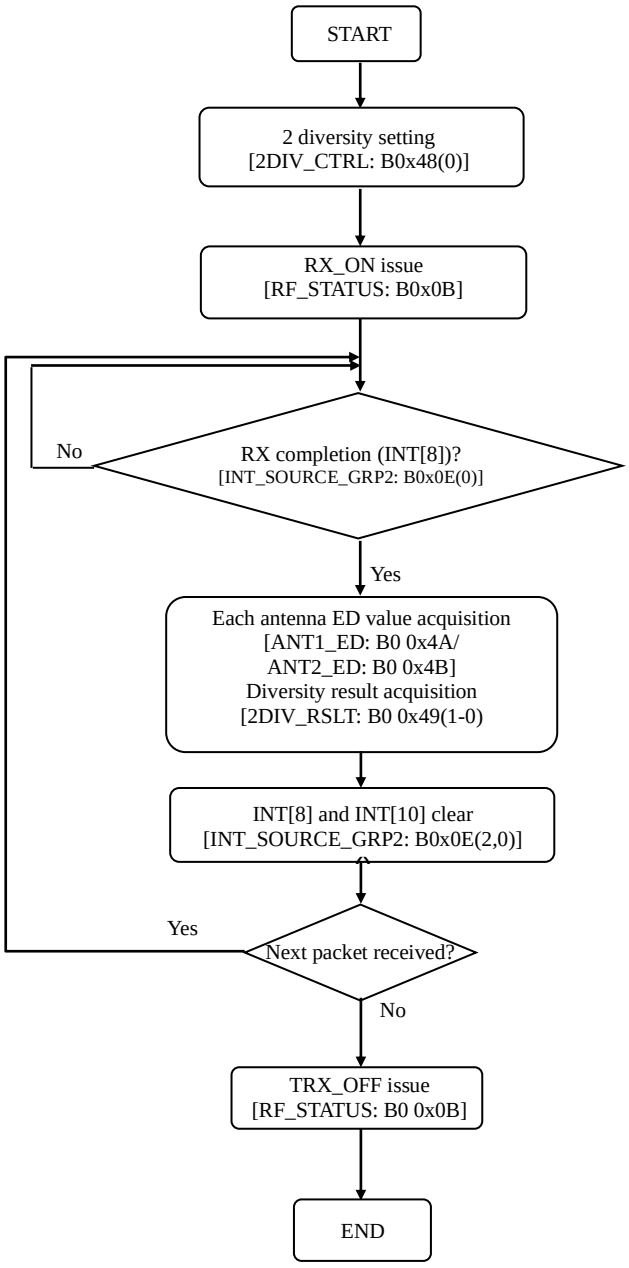


(*1) general purpose timer setting example
If 250µs wait is programmed using general purpose timer 1,
The following registers can be used.
[GT_CLK_SET:B0 0x33] = 0x01(128 division)
[GT_INTERVAL1:B0 0x34] = 0x04(timer setting)
[GT_SET:B0 0x32] = 0x03(2MHz clock, timer start)

(9) Antenna diversity

After setting 2DIV_EN([2DIV_CTRL:B0 0x48(0)]) = 0b1,issuing RX_ON by [RF_STATU:B0 0x0B] register. Antennas are switched to acquire each ED value, the antenna with higher ED value will be automatically selected.

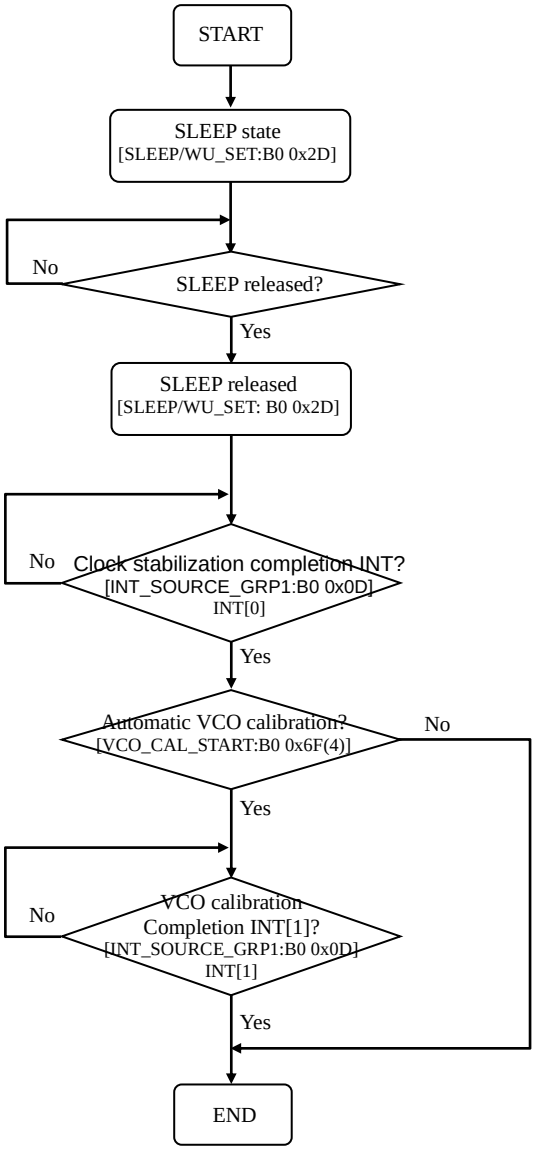
ED values ([ANT1_ED: B0 0x4A/ANT2_ED: B0 0x4B]) from diversity antennas and 2DIV_RSLT ([2DIV_RSLT: B0 0x49(1-0)]) will be updated, upon SyncWord detection. If Diversity detection completion interrupt - INT[10]([INT_SOURCE_GRP2: B0x0E(2)]) is cleared, ED values - ([ANT1_ED: B0 0x4A/ANT2_ED: B0 0x4B]) by diversity and diversity antenna result -2DIV_RSLT([2DIV_RSLT: B0 0x49(1-0)]) will be cleared.



●SLEEP Sequence

(1) SLEEP

SLEEP can be executed by setting SLEEP_EN([SLEEP/WU_SET:B0 0x2D(0)]) = 0b1. SLEEP can be released by setting SLEEP_EN = 0b0. If VCO calibration automatic execution setting AUTO_VCOCAL_EN([VCO_CAL_START:B0 0x6F (4)]) = 0b1, VCO calibration is performed after clock stabilization completion interrupt (INT[0] group1) from SLEEP release automaticaly.



(2) Wake-up timer

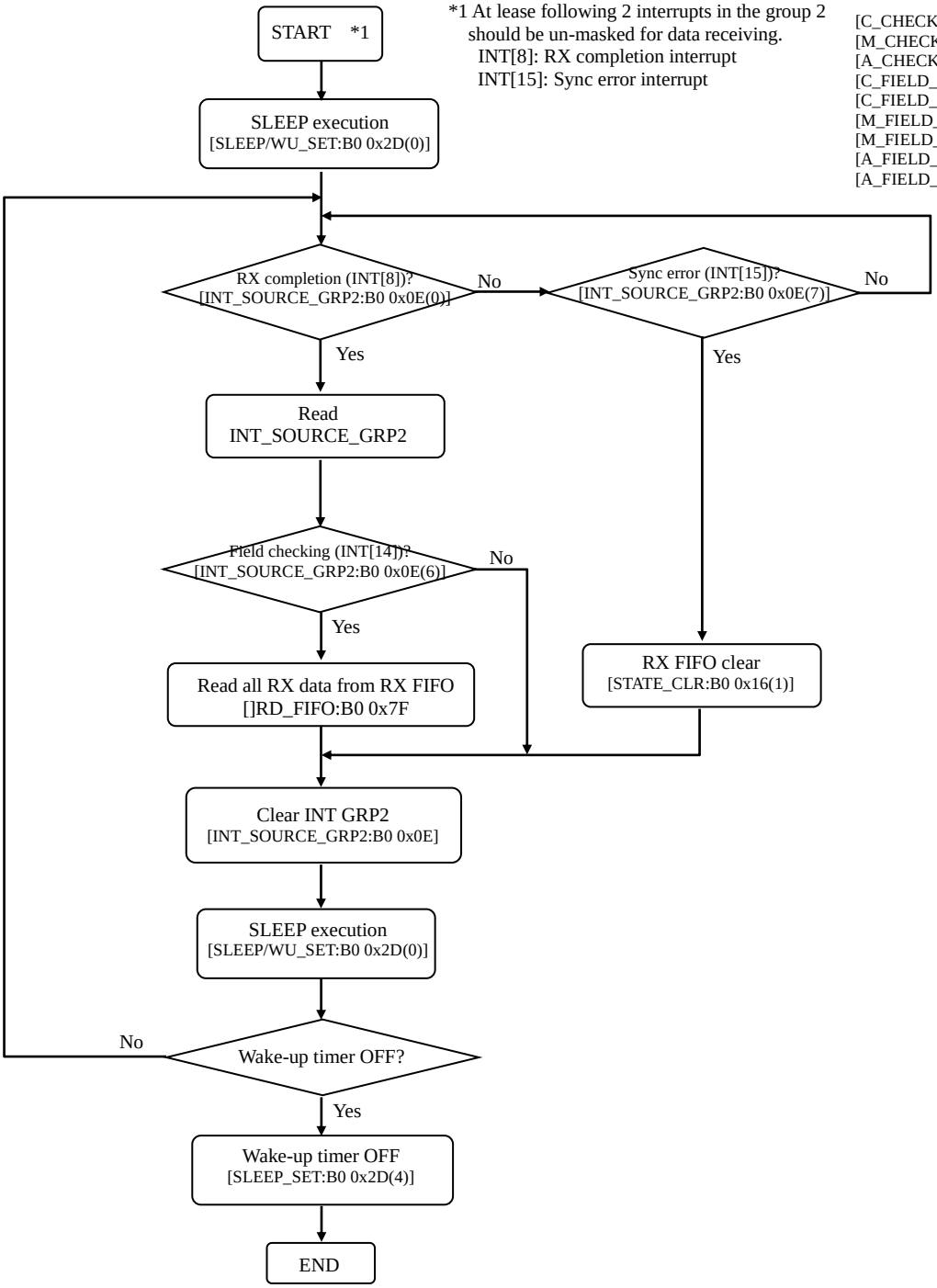
By setting the following registers, automatically wake-up to RX_ON state after SLEEP. After SyncWord detection interrupt (INT[13]: group2), wait receiving RX completion interrupt(INT[8]: group2). After RX completion, determine a Field check interrupt (INT[14]: group2). As the result of the Field check, read RX data for address match, or execute STATE_CLR1([STATE_CLR: B0 0x16(1)])(RX FIFO clear) otherwise. In order to re-enter SLEEP state, execute SLEEP command (SLEEP_EN[SLEEP/WU_SET: B0 0x2D(0)]) after clearing all interrupts in INT group2. If SyncWord cannot be detected, automatically go back to SLEEP state after continuous operation timer-up.

Wake-up timer setting

WAKEUP_EN([SLEEP_SET:B0 0x2D(4)]) = 0b1
RX_DURATION_EN([SLEEP_SET:B0 0x2D(5)]) = 0b1
WAKEUP_MODE([SLEEP_SET:B0 0x2D(6)]) = 0b0
[WUT_CLK_SET:B0 0x2E]
[WUT_INTERVAL_H:B0 0x2F]
[WUT_INTERVAL_L:B0 0x30]
[RX_DURATION:B0 0x31]

Field check function setting

[C_CHECK_CTR:B0 0x1B]
[M_CHECK_CTRL:B0 0x1C]
[A_CHECK_CTRL:B0 0x1D]
[C_FIELD_WORD1:B0 0x1E] to
[C_FIELD_WORD5:B0 0x22]
[M_FIELD_WORD1:B0 0x23] to
[M_FIELD_WORD4:B0 0x26]
[A_FIELD_WORD1:B0 0x27] to
[A_FIELD_WORD6:B0 0x2C]



●Error Process

(1) Sync error

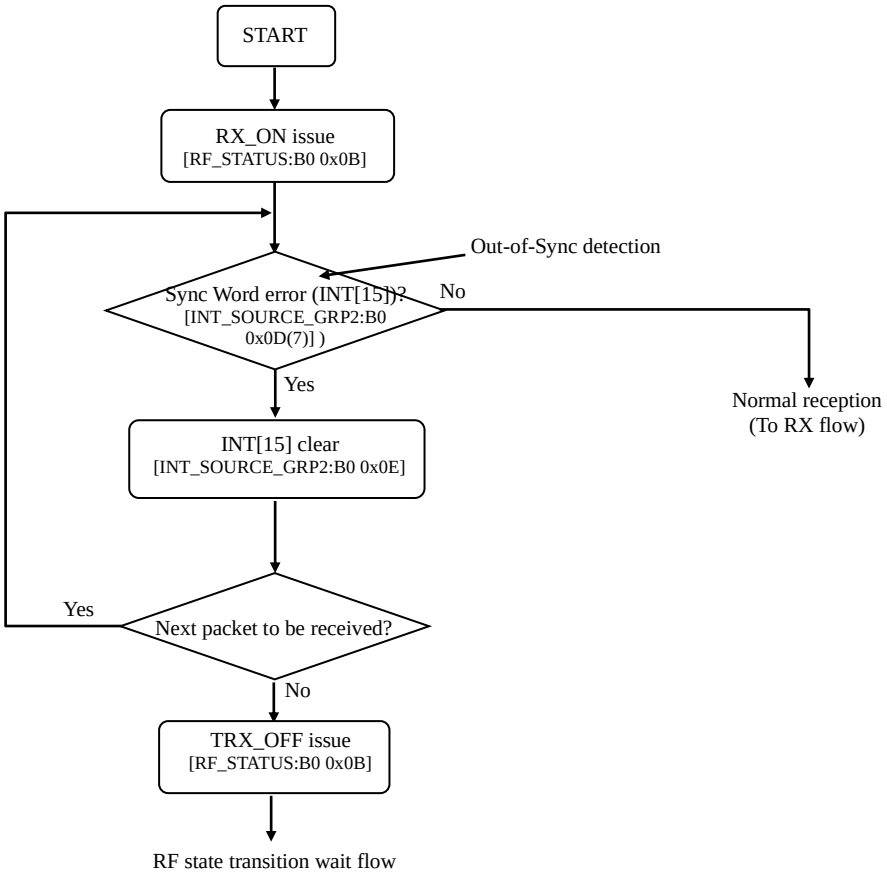
When out-of-sync is detected during data reception after SyncWord detection, Sync error interrupt (INT[15] group2) will be generated, RX completion interrupt (INT[8]: group2) will not be generated. If Sync error interrupt occurs, clear Sync error interrupt.

"data reception" indicates receiving data (L-field, data, CRC). after SyncWord detection.

(Note)

When detecting a Sync error in FIFO mode, ML7404 judges the Sync error generation packet as invalid to stop storage of RX data to FIFO and clear RX FIFO control information (RX data count, FIFO read count, etc.). If FIFO read is performed in this state, invalid FIFO usage will be indicated since there is no RX data. To receive the next packet properly, start receiving packets after clearing RX FIFO ([STATE_CLR:B0 0x16])

When a Sync error occurs, the RF state remains RXON. Then immediately after the notification of Sync error, the RF state changes to SyncWord detection waiting state in preparation for receiving the next packet. To receive the next packet properly, clear RX FIFO ([STATE_CLR:B0 0x16]) and all reception related interrupts ([INT_SOURCE_GRP2:B0 0x0E]).



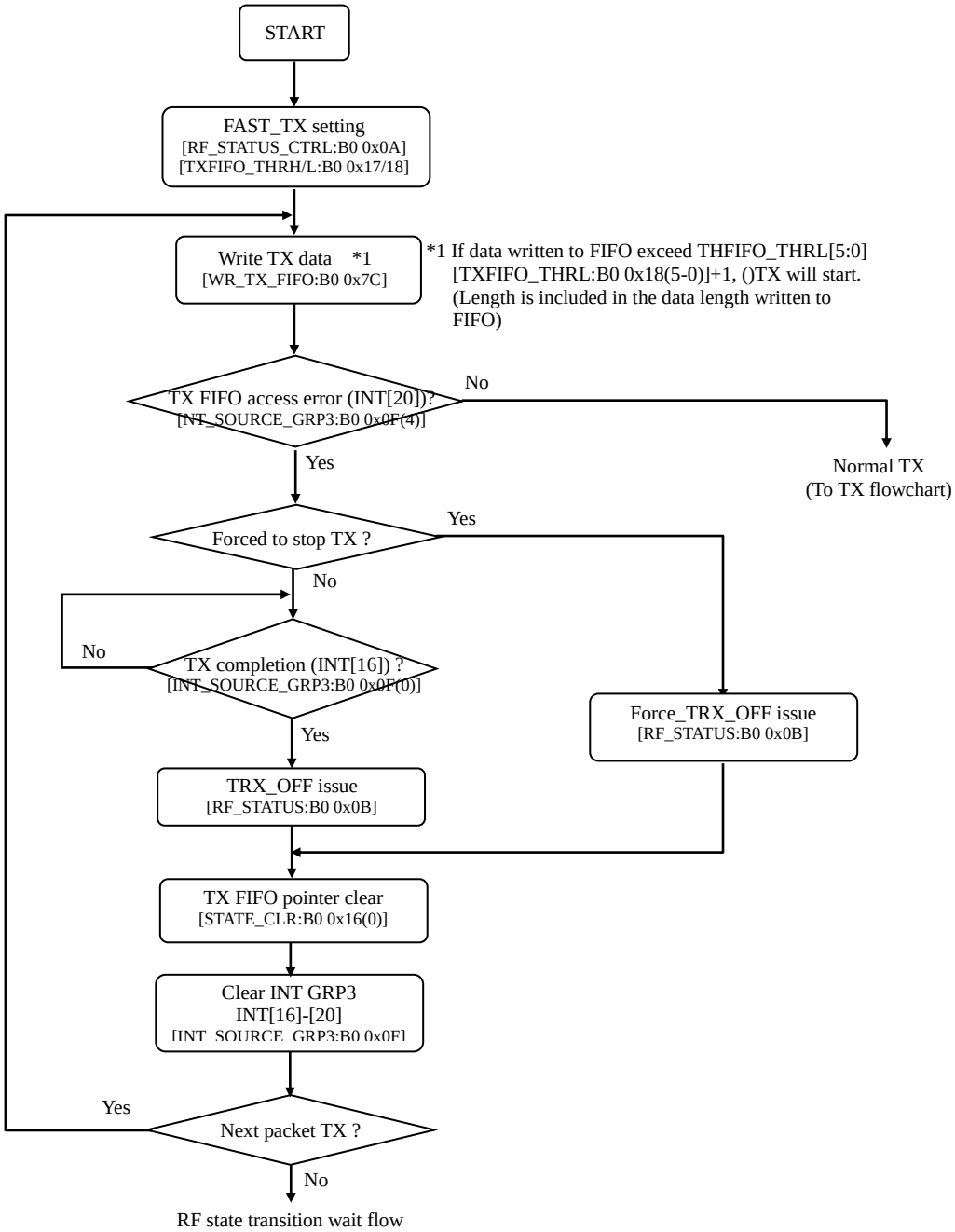
(2) TX FIFO access error

If one of the following conditions is met, TX FIFO access error interrupt (INT[20]: group3) will be generated.

- ●After TX Data request accept completion interrupt (INT[17]: group3] was generated, next packet is written to the TX_FIFO without transmiting the current TX data.
- ●Data write overflow occurs to the TX_FIFO.
- ●No TX data in the TX_FIFO during TX data transimission.

When TX FIFO acccess error interrupt occurs, issuing TRX_OFF after TX completion interrupt(INT[16]: group3) is recognized, or issueing Force_TRX_OFF by [RF_STATUS:B0 0x0B] register without waiting for TX completion interrupt. After that, issuing TX FIFO pointer clear by [STATE_CLR:B0 0x16] register and clear remaining interrupts relative with TX in the [INT_SOURCE_GRP3:B0 0x0F] register.

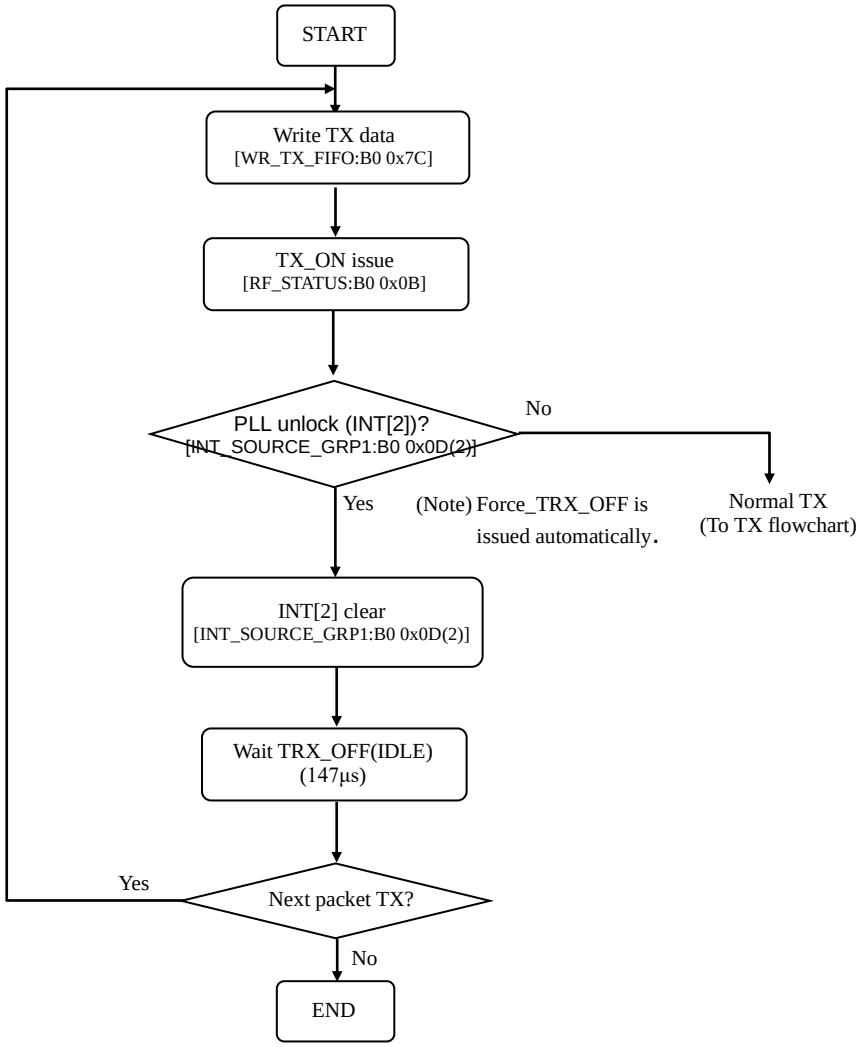
If TX FIFO access error occurs, subquent TX data will be inverted. CRC error should be detected at rexeiver side even if TRX_OFF is issued when TX completion interrupt detected.



(3) PLL unlock detection

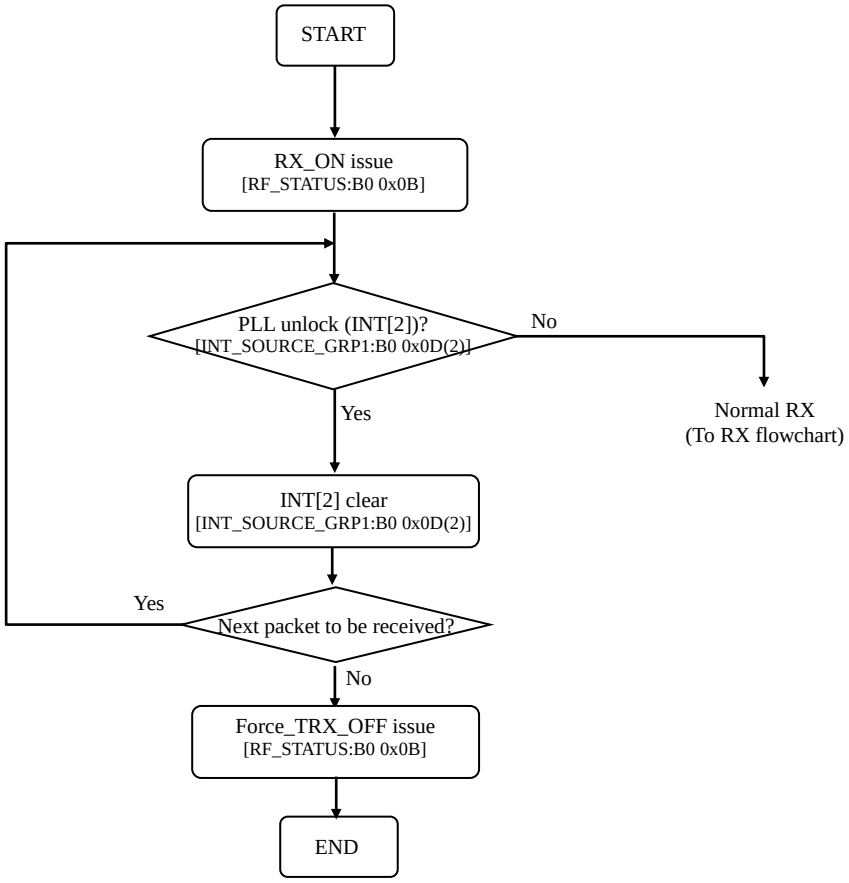
○ TX

If PLL unlock is detected during transmission, transmission is stopped and the ML7404 is forced IDLE state. PLL unlock might be caused by incorrect VCO calibration value. Please confirm VCO calibration or perform VCO calibration again. After PLL unlock interrupt occurs, max. 147μs is necessary to move to IDLE state. Please wait for at least 147μs before next TX, RX or VCO calibration is performed.



○ RX

If PLL unlock is detected during reception, it is continued without forcing IDLE state. Clear the PLL unlock detection interrupt ([INT_SOURCE_GRP1:B0 0x0D] INT[2]).



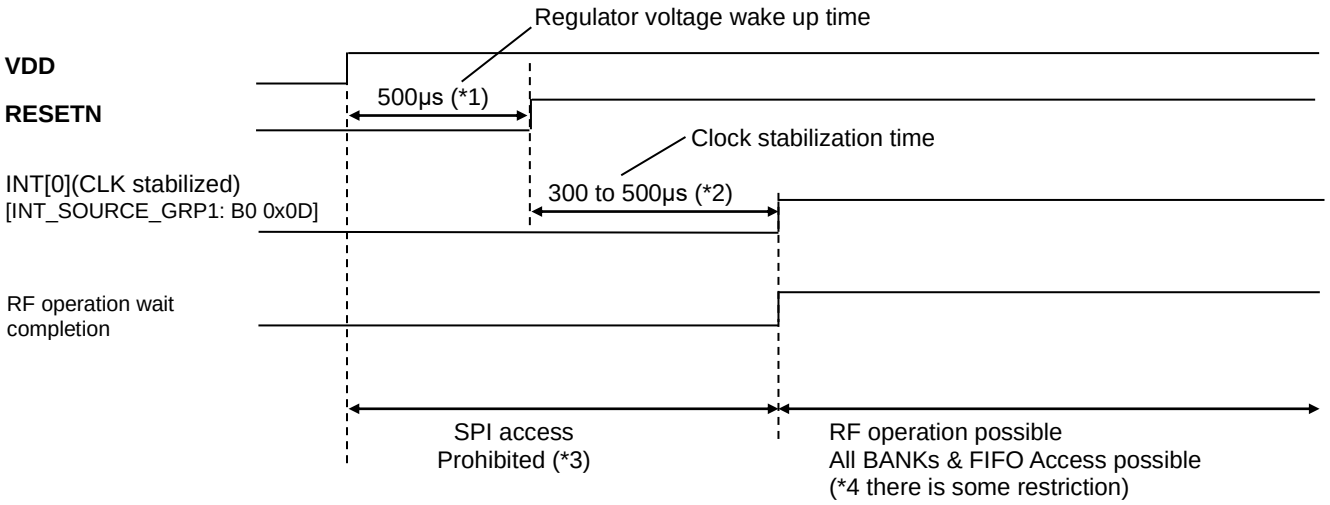
■Timing Chart

The following are operation timing for major functions.

(Note)
Bold characters indicate pins related signals. Non bold characters indicate internal signals.

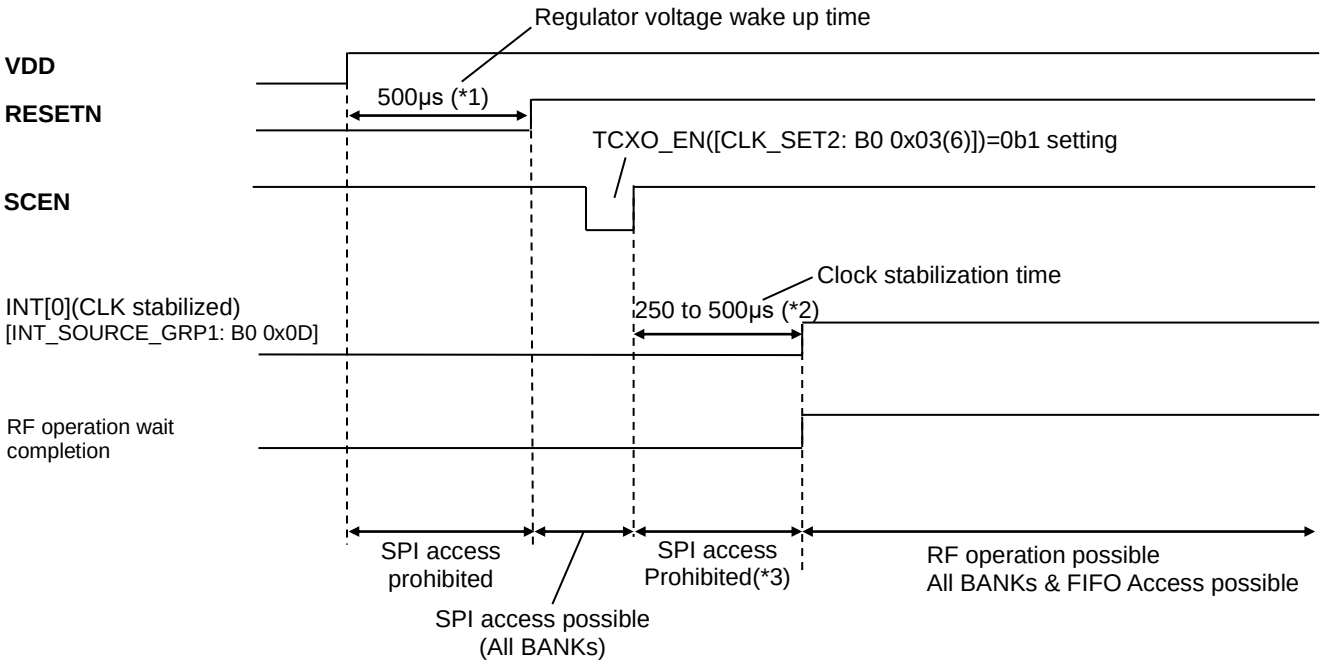
●Start-up

[In case of Crystal oscillator circuits]



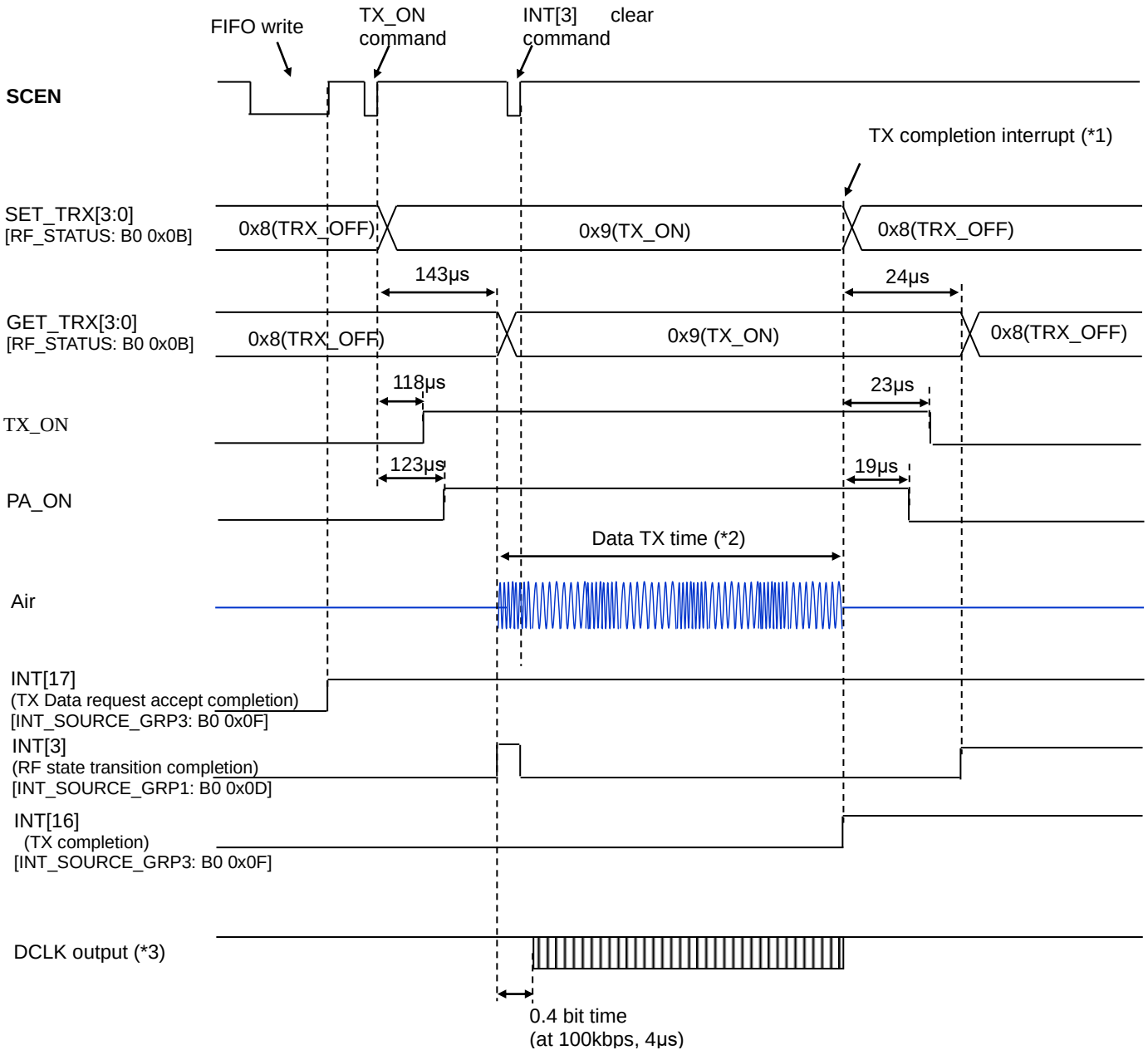
*1 : For wake-up timing of VDD and RESETN, please refer to the “Reset Characteristics”.
*2 : It is possible to adjust to 250/500µs, by setting OSC_W_SEL[1:0]([OSC_W_SEL: B1 0x08(6-5)]).
*3 : SPI access is prohibited after hard reset release(RESETN pin = “H”) to Clock stabilized completion. SPI access must be performed after confirming Clock stabilized completion by reading INT0[INT_SOURCE_GRP1: B0 0x0D(0)].

[In case of TCXO]



*1 : For wake-up timing of VDD and RESETN, please refer to the “Reset Characteristics”.
*2 : It is possible to adjust to 250/500µs, by setting OSC_W_SEL[1:0]([OSC_W_SEL: B1 0x08(6-5)]).
*3 : SPI access must be performed after confirming Clock stabilized completion by reading INT0[INT_SOURCE_GRP1: B0 0x0D(0)]. Please refer to initialization flow of “Flowchart”.

●TX



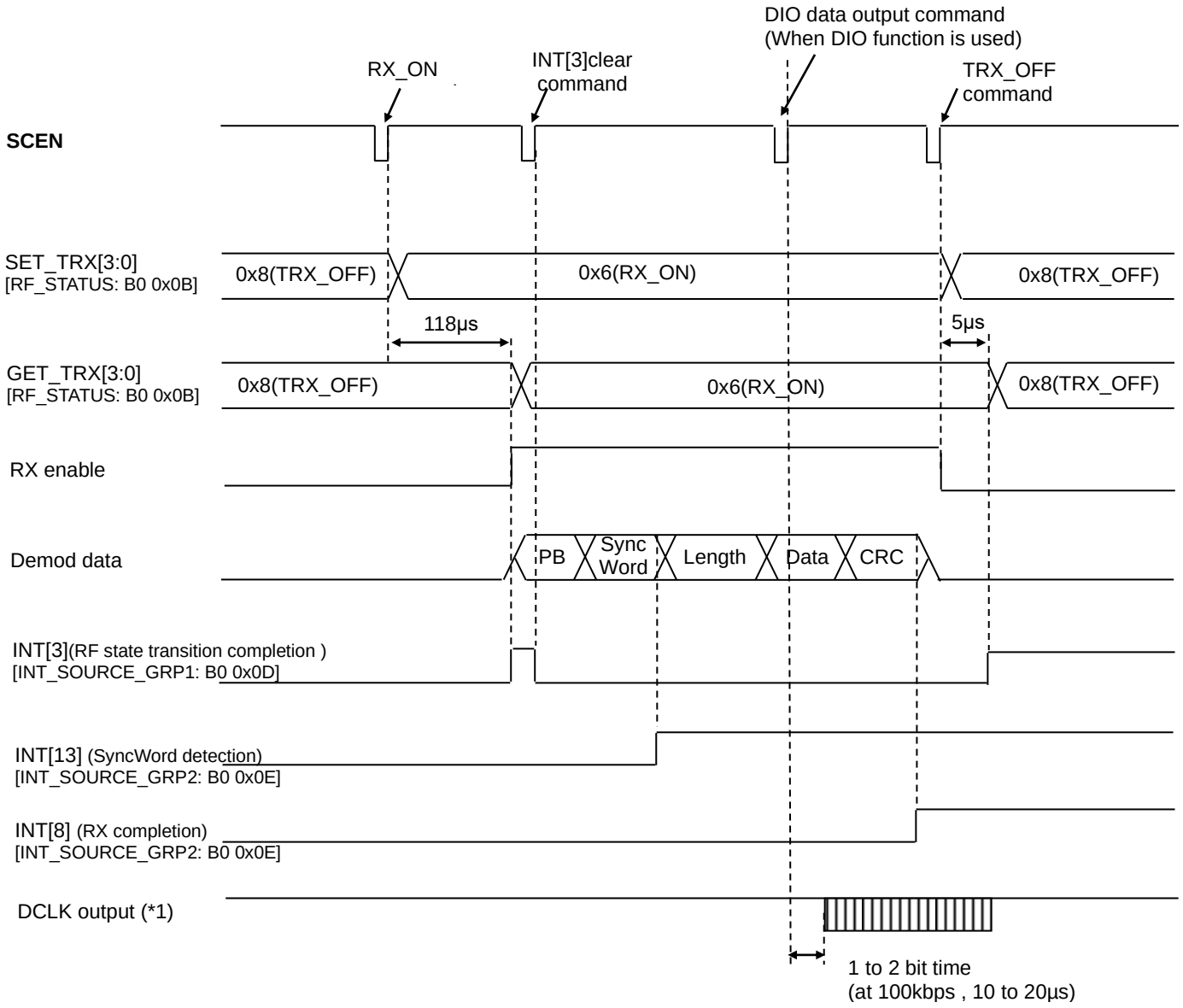
*1 : When TXDONE_MODE[1:0]([RF_STATUS_CTRL: B0 0x0A(1-0)]) = 0b00(default), SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)]) will be set to 0x8(TRX_OFF) automatically, upon detection of TX completion.

*2 : Data TX time calculation is as follows:

Data TX time [sec] = (number of TX bits+3)×1bit TX duration time[sec]
1bit TX duration time [sec] = 1/data rate [bps]

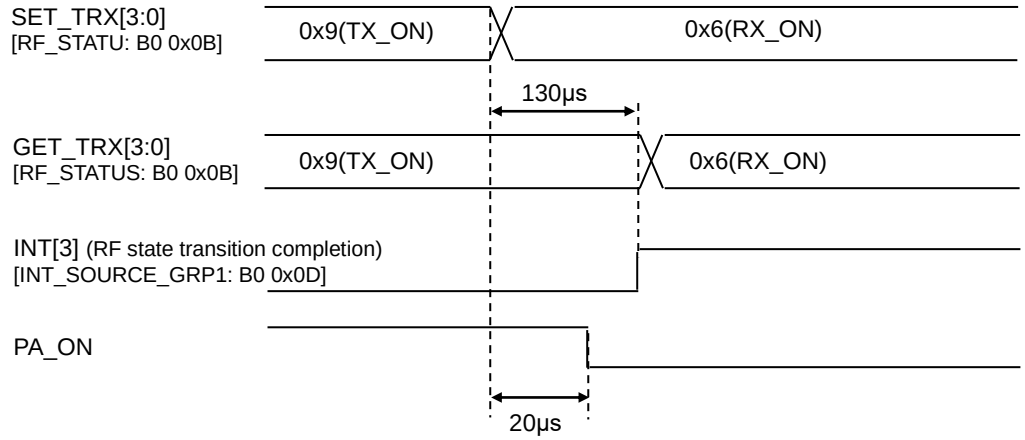
*3 : When setting TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)]) = 0b01.

●RX

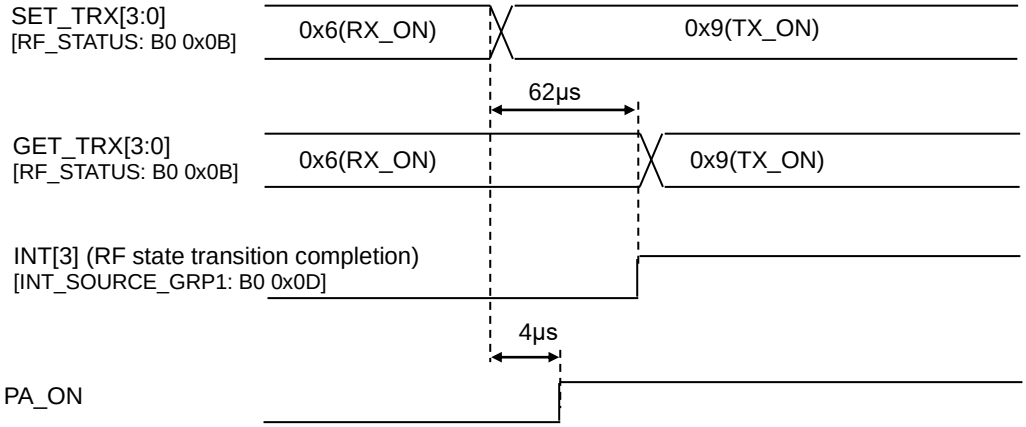


*1 : When setting RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)]) = 0b10 or 0b11.

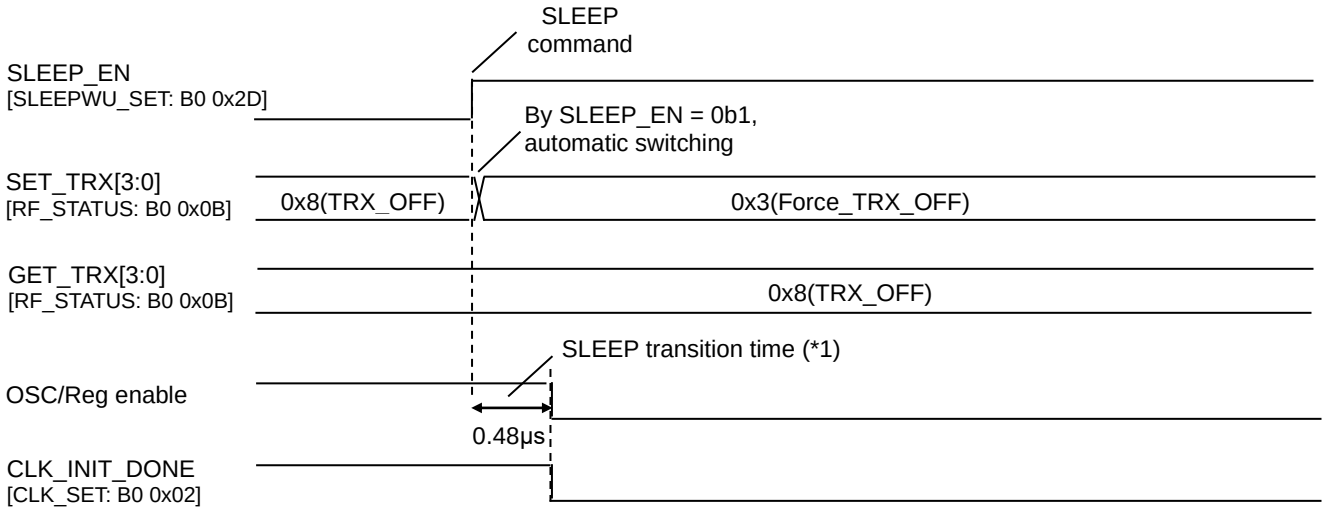
●Transition from TX to RX



●Transition from RX to TX

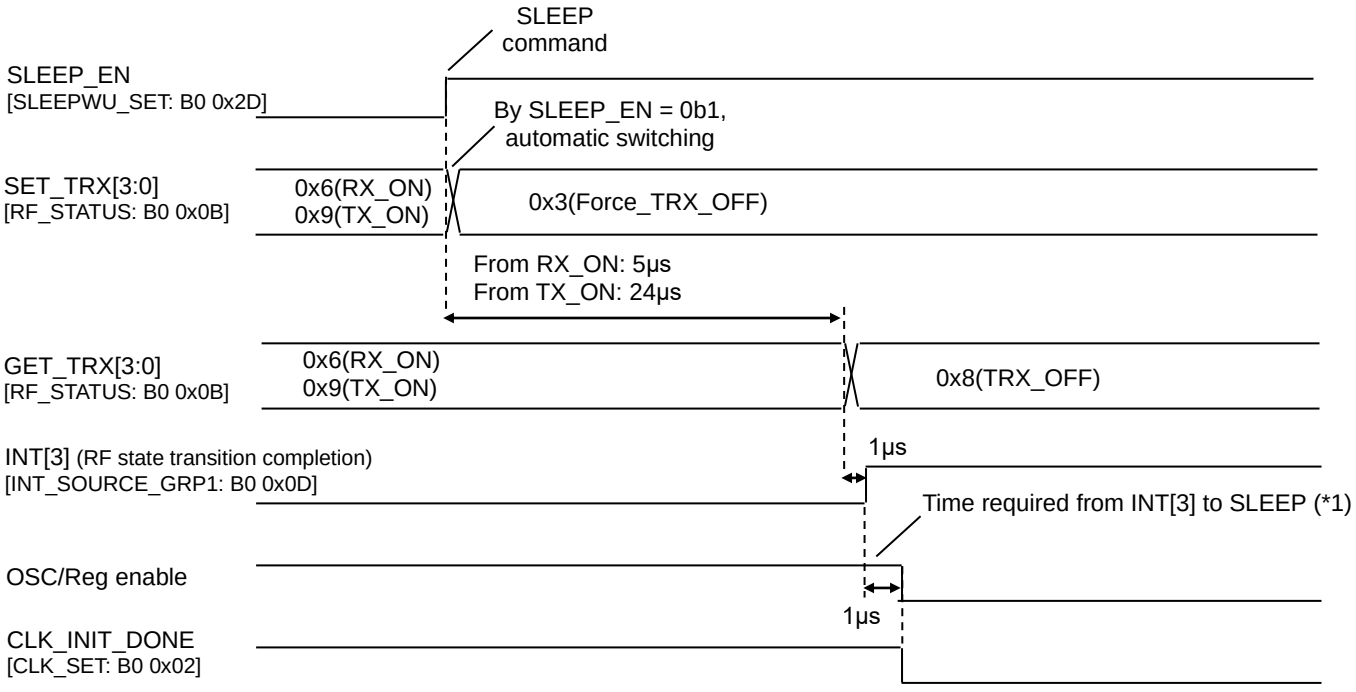


●Transition from IDLE to SLEEP



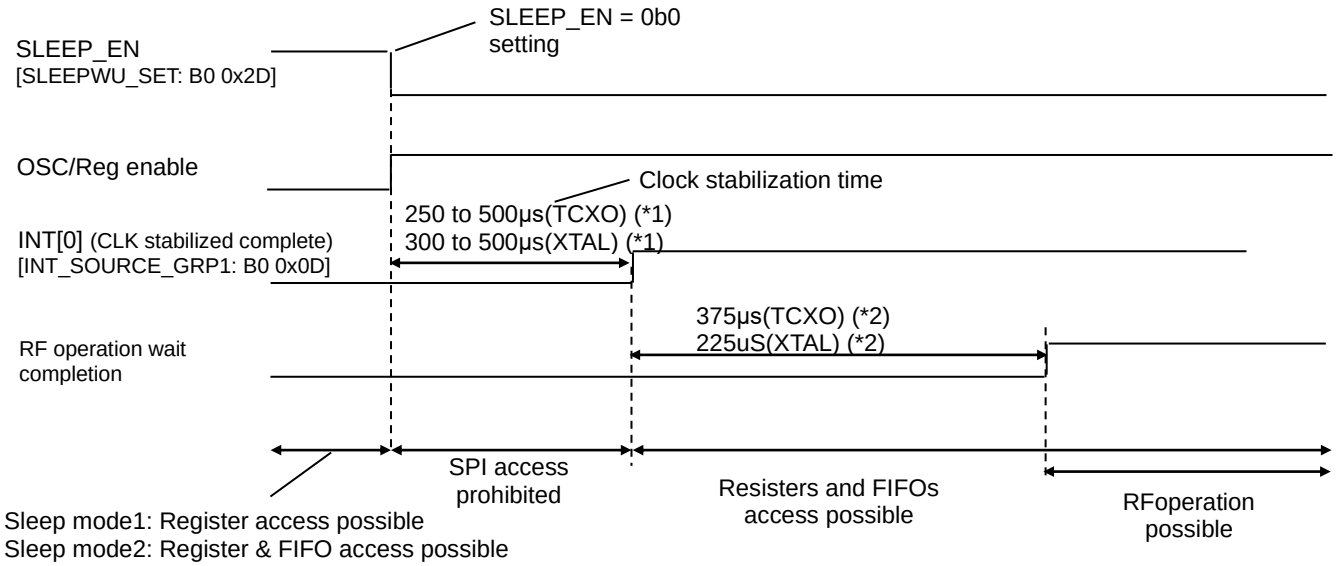
*1 : Clock input should be required for SLEEP transition. If TCXO is stopped during SLEEP state, please wait 1µs after SLEEP command issued (SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) and then stop TCXO.

●Transition from TX/RX state to SLEEP



*1 : If TCXO is used, please stop TCXO input after 2µs from INT[3] notification by setting SLEEP command (SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) .

●Transition from SLEEP to IDLE

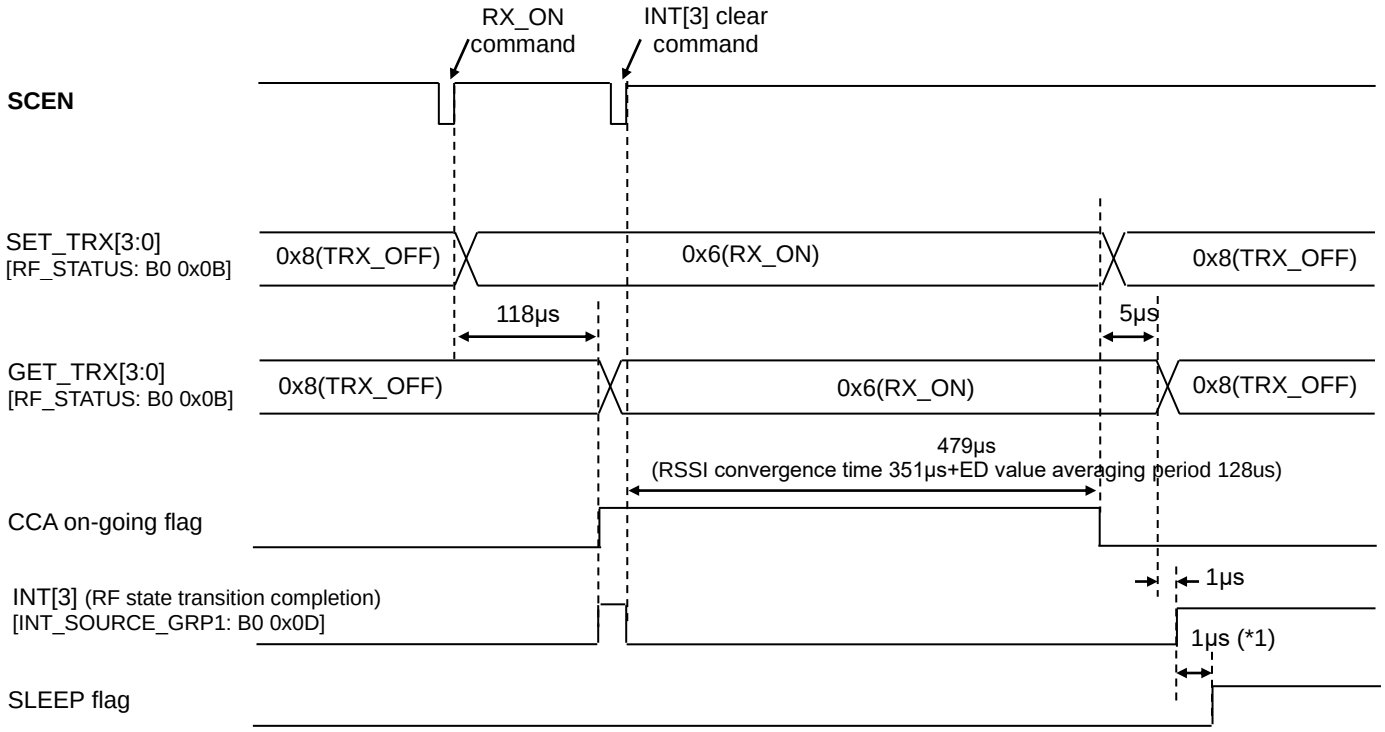


*1: It is possible to adjust to 250/500µs by setting [OSC_W_SEL: B1 0x08(6-5)]. α is oscillation cuircuits start-up time, and max. is 500µs.

*2: [VCO_CAL_START: B0 0x6F] and [SET_TRX: B0 0x0B] registers access is possible, but process is pending until RF operation wait completion signal is asserted.

●High speed carrier checking mode

This timing chart is under the following conditions:
ED value averaging : 8 times
Channel filter bandwidth : 10kHz



*1: Clock input should be required for SLEEP transition. If TCXO is stopped during SLEEP state, please wait 2µs from INT[3] and then stop TCXO.

■Registers

●Registers Map

The ML7404 has four register BANKs whose address range is 0x00-0x7F(128bytes). Grey colours in the table are unused bits or reserved bits . Please use the initial setting value, as reserved bits may be used for functions not open to the customers. It may cause unexpected operation. Reading value of “Reserved” registers are indeterminate. Reading value of “Reserved” bits are indeterminate.

Each BANK can be selected by [BANK_SEL] register (B0 0x00, B1 0x00, B2 0x00, B3 0x00, B6 0x00, B7 0x00, B10 0x00), enabling each bank in bit7-4 (BANK_ACEN) and specified BANK number to bit3-0.

If register’s value is specified in the description, do not change.

BANK0

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01	RST_SET	Reset control
02	CLK_SET1	Clock control 1
03	CLK_SET2	Clock control 2
04	PKT_CTRL1	Packet format setting 1
05	PKT_CTRL2	Packet format setting 2
06	DRATE_SET	Data rate setting
07	DATA_SET1	TX/RX data configuration 1
08	DATA_SET2	TX/RX data configuration 2
09	CH_SET	RF channel setting
0A	RF_STATUS_CTRL	RF status change setting
0B	RF_STATUS	RF status setting
0C	DIO_SET	DIO setting
0D	INT_SOURCE_GRP1	Interrupt indication 1
0E	INT_SOURCE_GRP2	Interrupt indication 2
0F	INT_SOURCE_GRP3	Interrupt indication 3
10	INT_EN_GRP1	Interrupt notification enable 1
11	INT_EN_GRP2	Interrupt notification enable 2
12	INT_EN_GRP3	Interrupt notification enable 3
13	CRC_ERR_H	CRC error status 1
14	CRC_ERR_M	CRC error status 2
15	CRC_ERR_L	CRC error status 3
16	STATE_CLR	State clear control
17	TXFIFO_THRH	TX FIFO-Full threshold
18	TXFIFO_THRL	TX FIFO-Empty threshold, FAST_TX enable threshold
19	RXFIFO_THRH	RX FIFO-Full threshold
1A	RXFIFO_THRL	RX FIFO-Empty threshold
1B	C_CHECK_CTRL	C-field check enable
1C	M_CHECK_CTRL	M-field check enable
1D	A_CHECK_CTRL	A-field check enable
1E	C_FIELD_CODE1	C-field setting code #1
1F	C_FIELD_CODE2	C-field setting code #2
20	C_FIELD_CODE3	C-field setting code #3
21	C_FIELD_CODE4	C-field setting code #4
22	C_FIELD_CODE5	C-field setting code #5
23	M_FIELD_CODE1	M-field 1st byte setting code 1
24	M_FIELD_CODE2	M-field 1st byte setting code 2
25	M_FIELD_CODE3	M-field 2nd byte setting code 1
26	M_FIELD_CODE4	M-field 2nd byte setting code 2
27	A_FIELD_CODE1	A-field 1st byte setting
28	A_FIELD_CODE2	A-field 2nd byte setting
29	A_FIELD_CODE3	A-field 3rd byte setting
2A	A_FIELD_CODE4	A-field 4th byte setting
2B	A_FIELD_CODE5	A-field 5th byte setting
2C	A_FIELD_CODE6	A-field 6th byte setting
2D	SLEEP/WU_SET	SLEEP/Wake-up timer setting
2E	WUT_CLK_SET	Wake-up timer clock division setting
2F	WUT_INTERVAL_H	Wake-up timer interval setting (high byte)
30	WUT_INTERVAL_L	Wake-up timer interval setting (low byte)
31	WU_DURATION	Continue operation timer (after wake-up) setting
32	GT_SET	General purpose timer configuration
33	GT_CLK_SET	General purpose timer clock division setting
34	GT1_TIMER	General purpose timer #1 setting

BANK0 (continued)

Address [HEX]	Register name	Description
35	GT2_TIMER	General purpose timer #2 setting
36	CCA_IGNORE_LVL	ED threshold level setting for excluding CCA judgment
37	CCA_LVL	CCA threshold level setting
38	CCA_ABORT	Timing setting for forced termination of CCA operation
39	CCA_CTRL	CCA control setting and result indication
3A	ED_RSLT	ED value indication
3B	IDLE_WAIT_H	IDLE detection period setting during CCA (high byte)
3C	IDLE_WAIT_L	IDLE detection period setting during CCA (low byte)
3D	CCA_PROG_H	IDLE judgement elapsed time indication during CCA (high byte)
3E	CCA_PROG_L	IDLE judgement elapsed time indication during CCA (low byte)
3F	PREAMBLE_SET	Preamble pattern setting
40	VCO_VTRSLT	VCO adjustment voltage result display
41	ED_CTRL	ED detection control setting
42	TXPR_LEN_H	TX preamble length setting (high byte)
43	TXPR_LEN_L	TX preamble length setting (low byte)
44	POSTAMBLE_SET	Postamble length and pattern setting
45	SYNC_CONDITION1	RX preamble setting and ED threshold check setting
46	SYNC_CONDITION2	ED threshold setting during synchronization detection
47	SYNC_CONDITION3	Bit error tolerance setting in RX preamble and SyncWord detection.
48	2DIV_CTRL	Antena diversity setting
49	2DIV_RSLT	Antenna diversity result indication
4A	ANT1_ED	Acquired ED value by antenna 1
4B	ANT2_ED	Acquired ED value by antenna 2
4C	ANT_CTRL	TX/RX antenna control setting
4D	MON_CTRL	Monitor function setting
4E	GPIO0_CTRL	GPIO0 pin (pin#16) configuration setting
4F	GPIO1_CTRL	GPIO1 pin (pin#17) configuration setting
50	GPIO2_CTRL	GPIO2 pin (pin#18) configuration setting
51	GPIO3_CTRL	GPIO3 pin (pin#19) configuration setting
52	EXTCLK_CTRL	EXT_CLK pin (pin #10) control setting
53	SPI/EXT_PA_CTRL	SPI interface(SDI/SDO)pins/external PAcontrol
54	CHFIL_BW	Channel filter bandwidth setting
55	DC_I_ADJ_H	I phase DC offset adjustment setting(high 6bits)
56	DC_I_ADJ_L	I phase DC offset adjustment setting(low byte)
57	DC_Q_ADJ_H	Q phase DC offset adjustment setting(high 6bits)
58	DC_Q_ADJ_L	Q phase DC offset adjustment setting(low byte)
59	DC_FIL_ADJ	DC offset adjustment filter setting
5A	IQ_MAG_ADJ_H	IF IQ amplitude balance adjustment (high 4bits)
5B	IQ_MAG_ADJ_L	IF IQ amplitude balance adjustment (low byte)
5C	IQ_PHASE_ADJ_H	IF IQ phase balance adjustment (high 3bits)
5D	IQ_PHASE_ADJ_L	IF IQ phase balance adjustment (low byte)
5E	IQ_ADJ_WAIT	IF IQ automatic adjustment RSSI acquisition wait time
5F	IQ_ADJ_TARGET	IF IQ automatic adjustment RSSI judgment threshold
60	DEC_GAIN	Decimation gain setting
61	IF_FREQ	IF frequency selection
62	OSC_ADJ1	Coarse adjustment of load capacitance for oscillation circuits
63	OSC_ADJ2	Fine adjustment of load capacitance for oscillation circuits
64	Reserved	Reserved
65	OSC_ADJ4	Oscillation circuits bias adjustment (start-up)
66	RSSI_ADJ	RSSI value adjustment
67	PA_REG_ADJ_H	PA regulator output voltage adjustment (high bit)
68	PA_REG_ADJ_L	PA regulator output voltage adjustment (low byte)
69	Reserved	Reserved
6A	CHFIL_BW_CCA	Channel filter bandwidth setting when CCA

BANK0 (continued)

Address [HEX]	Register name	Description
6B	CHFIL_BW_OPTION	Channel filter bandwidth option setting
6C	DC_FIL_ADJ2	DC offset adjustment filter setting 2
6D	DEC_GAIN_CCA	Decimation gain setting(CCA)
6E	VCO_CAL	VCO calibration setting or status indication
6F	VCO_CAL_START	VCO calibration execution
70	CLK_CAL_SET	Low speed clock calibration control
71	CLK_CAL_TIME	Low speed clock calibration time setting
72	CLK_CAL_H	Low speed clock calibartion result indication (high byte)
73	CLK_CAL_L	Low speed clock calibartion result indication (low byte)
74	Reserved	Reserved
75	SLEEP_INT_CLR	Interrupt clear setting during SLEEP state
76	RF_TEST_MODE	TX test pattern setting
77	STM_STATE	State machine status/synchronization status indication
78	FIFO_SET	FIFO readout setting
79	RX_FIFO_LAST	RX FIFO data usage status indication
7A	TX_PKT_LEN_H	TX packet length setting (high byte)
7B	TX_PKT_LEN_L	TX packet length setting (low byte)
7C	WR_TX_FIFO	TX FIFO
7D	RX_PKT_LEN_H	RX packet length setting and indication (high byte)
7E	RX_PKT_LEN_L	RX packet length setting and indication (low byte)
7F	RD_FIFO	FIFO read

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK2 registers.

BANK1

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01	CLK_OUT	CLKOUT output frequency setting
02	TX_RATE_H	TX data rate conversion setting (high byte)
03	TX_RATE_L	TX data rate conversion setting (low byte)
04	RX_RATE1_H	RX data rate conversion setting 1 (high byte)
05	RX_RATE1_L	RX data rate conversion setting 1 (low byte)
06	RX_RATE2	RX data rate conversion setting 2
07	Reserved	Reserved
08	OSC_W_SEL	Clock stabilization waiting time setting
09-0A	Reserved	Reserved
0B	PLL_LOCK_DETECT	PLL lock detection setting
0C-0D	Reserved	Reserved
0E	GAIN_HOLD	Gain switching setting
0F	RSSI_STABLE_RES	RSSI Stabilization wat time resolution setting
10	GC_MODE_DIV	Gain control mode setting in diversity
11	Reserved	Reserved
12	RSSI_STABLE_TIME	RSSI stabilization wait time setting
13	RSSI_MAG_ADJ	Scale factor setting for ED value conversion
14	Reserved	Reserved
15	AFC/GC_CTRL	AFC/gain control setting
16	CRC_POLY3	CRC polynomial setting 3
17	CRC_POLY2	CRC polynomial setting 2
18	CRC_POLY1	CRC polynomial setting 1
19	CRC_POLY0	CRC polynomial setting 0
1A	PLL_DIV_SET	PLL frequency division setting
1B	TXFREQ_I	TX frequency setting (I counter)
1C	TXFREQ_FH	TX frequency setting (F counter high 4bits)
1D	TXFREQ_FM	TX frequency setting (F counter middle byte)
1E	TXFREQ_FL	TX frequency setting (F counter low byte)
1F	RXFREQ_I	RX frequency setting (I counter)
20	RXFREQ_FH	RX frequency setting (F counter high 4bits)
21	RXFREQ_FM	RX frequency setting (F counter middle byte)
22	RXFREQ_FL	RX frequency setting (F counter low byte)
23	CH_SPACE_H	Channel space setting (high byte)
24	CH_SPACE_L	Channel space setting (low byte)
25	SYNC_WORD_LEN	SyncWord length setting
26	SYNC_WORD_EN	SyncWord enable setting
27	SYNCWORD1_SET0	SyncWord #1 setting (bit24-31)
28	SYNCWORD1_SET1	SyncWord #1 setting (bit16-23)
29	SYNCWORD1_SET2	SyncWord #1 setting (bit8 to 15)
2A	SYNCWORD1_SET3	SyncWord #1 setting (bit0 to 7)
2B	SYNCWORD2_SET0	SyncWord #2 setting (bit24 to 31)
2C	SYNCWORD2_SET1	SyncWord #2 setting (bit16 to 23)
2D	SYNCWORD2_SET2	SyncWord #2 setting (bit8 to 15)
2E	SYNCWORD2_SET3	SyncWord #2 setting (bit0 to 7)
2F	FSK_CTRL	GFSK/FSK modulation timing resolution setting
30	GFSK_DEV_H	GFSK frequency deviation setting (high 6bits)
31	GFSK_DEV_L	GFSK frequency deviation setting (low byte)
32	FSK_DEV0_H/GFIL0	FSK 1st frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 0
33	FSK_DEV0_L/GFIL1	FSK 1st frequency deviation setting (low byte) / Gaussian filter coefficient setting 1
34	FSK_DEV1_H/GFIL2	FSK 2nd frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 2
35	FSK_DEV1_L/GFIL3	FSK 2nd frequency deviation setting (low byte) / Gaussian filter coefficient setting 3

BANK1 (continued)

Address [HEX]	Register name	Description
36	FSK_DEV2_H/GFIL4	FSK 3rd frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 4
37	FSK_DEV2_L/GFIL5	FSK 3rd frequency deviation setting (low byte) / Gaussian filter coefficient setting 5
38	FSK_DEV3_H/GFIL6	FSK 4th frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 6
39	FSK_DEV3_L	FSK 4th frequency deviation setting (low byte)
3A	FSK_DEV4_H	FSK 5th frequency deviation setting (high 6bits)
3B	FSK_DEV4_L	FSK 5th frequency deviation setting (low byte)
3C	FSK_TIM_ADJ4	FSK 4th frequency deviation hold time setting
3D	FSK_TIM_ADJ3	FSK 3rd frequency deviation hold time setting
3E	FSK_TIM_ADJ2	FSK 2nd frequency deviation hold timesetting
3F	FSK_TIM_ADJ1	FSK 1st frequency deviation hold time setting
40	FSK_TIM_ADJ4	FSK no-deviation frequency (carrier frequency) hold time setting
41	4FSK_DATA_MAP	4FSK data mapping setting
42	FREQ_ADJ_H	TX/RX frequency fine adjustment setting (high byte)
43	FREQ_ADJ_L	TX/RX frequency fine adjustment setting (low byte)
44-47	Reserved	Reserved
48	2DIV_MODE	Average diversity mode setting
49	2DIV_SEARCH1	Antenna diversity search time setting
4A	2DIV_SEARCH2	Antenna diversity search time setting
4B	2DIV_FAST_LVL	ED threshold level setting during Antenna diversity FAST mode
4C	Reserved	Reserved
4D	VCO_CAL_MIN_I	VCO Calibration low limit frequency setting (I counter)
4E	VCO_CAL_MIN_FH	VCO Calibration low limit frequency setting (F counter high 4bits)
4F	VCO_CAL_MIN_FM	VCO Calibration low limit frequency setting (F counter middle byte)
50	VCO_CAL_MIN_FL	VCO Calibration low limit frequency setting (F counter low byte)
51	VCO_CAL_MAX_N	VCO calibration upper limit frequency setting
52	VCAL_MIN	VCO calibration low limit value indication and setting
53	VCAL_MAX	VCO calibration upper limit value indication and setting
54-55	Reserved	Reserved
56	DEMOD_SET0	Demodulator configuration 0
57	DEMOD_SET1	Demodulator configuration 1
58	DEMOD_SET2	Demodulator configuration 2
59	DEMOD_SET3	Demodulator configuration 3
5A-5B	Reserved	Reserved
5C	DEMOD_SET6	Demodulator configuration 6
5D	DEMOD_SET7	Demodulator configuration 7
5E	DEMOD_SET8	Demodulator configuration 8
5F	DEMOD_SET9	Demodulator configuration 9
60	DEMOD_SET10	Demodulator configuration 10
61	DEMOD_SET11	Demodulator configuration 11
62	ADDR_CHK_CTR_H	Address check counter indication (high 3bits)
63	ADDR_CHK_CTR_L	Address check counter indication (low byte)
64	WHT_INIT_H	Whitening initializing state setting (high 1bit)
65	WHT_INIT_L	Whitening initializing state setting (low byte)
66	WHT_CFG	Whitening polynomial setting
67-7A	Reserved	Reserved
7B	TX_RATE2_EN	TX data rate setting 2 enable
7C	TX_RATE2_H	TX data rate setting 2 (high byte)
7D	TX_RATE2_L	TX data rate setting 2 (low byte)
7E	Reserved	Reserved
7F	ID_CODE	ID code indication

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK2 registers.

BANK2

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01-3F	Reserved	Reserved
40	VTUNE_COMP_ON	VCO adjustment voltage comparison result display enable
41-75	Reserved	Reserved
76	GAIN_HHTOH	Threshold level setting for switching “double high gain” to “high gain”
77	GAIN_HTOHH	Threshold level setting for switching “high gain” to “double high gain”
78	GAIN_HTOM	Threshold level setting for switching “high gain” to “middle gain”
79	GAIN_MTOH	Threshold level setting for switching “middle gain” to “high gain”
7A	GAIN_MTOL	Threshold level setting for switching “middle gain” to “low gain”
7B	GAIN_LTOM	Threshold level setting for switching “low gain” to “middle gain”
7C	RSSI_ADJ_H	RSSI offset value setting during high gain operation
7D	RSSI_ADJ_M	RSSI offset value setting during middle gain operation
7E	RSSI_ADJ_L	RSSI offset value setting during low gain operation
7F	Reserved	Reserved

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK1 registers.

BANK3

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01-22	Reserved	Reserved
23	2MODE_DET	2 modes detection setting (MODE-T and MODE-C)
24-40	Reserved	Reserved
41	RAMP_CTRL1	PA ramp control setting 1
42	RAMP_CTRL2	PA ramp control setting 2
43	RAMP_CTRL3	PA ramp control setting 3
44-4F	Reserved	Reserved
50	EXT_WU_CTRL	External wake-up control setting
51	EXT_WU_INTERVAL	External wake-up control setting
52-7F	Reserved	Reserved

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK2 registers.

BANK6

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01	MOD_CTRL	Modulation setting
02-7A	Reserved	Reserved
7B	BPSK_PLL_CTRL	BPSK mode setting
7C	BPSK_P_START_H	Frequency deviation start time setting in BPSK frequency control (high 3 bits)
7D	BPSK_P_START_L	Frequency deviation start time setting in BPSK frequency control (low byte)
7E	BPSK_P_HOLD_H	Frequency deviation hold time setting in BPSK frequency control (high 4bits)
7F	BPSK_P_HOLD_L	Frequency deviation hold time setting in BPSK frequency control (low byte)

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK2 registers.

BANK7

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01	DSSS_CTRL	DSSS control setting
02	DSSS_MODE	DSSS mode setting
03	FEC_ENC_CTRL	FEC encoder setting
04	Reserved	Reserved
05	FEC_DEC_CTRL	FEC decoder setting
06	SF_CTRL	Spreading factor setting
07	SHR_GOLD_SEED3	SHR Gold code seed setting 3
08	SHR_GOLD_SEED2	SHR Gold code seed setting 2
09	SHR_GOLD_SEED1	SHR Gold code seed setting 1
0A	SHR_GOLD_SEED0	SHR Gold code seed setting 0
0B	PSDU_GOLD_SEED3	PSDU Gold code seed setting 3
0C	PSDU_GOLD_SEED2	PSDU Gold code seed setting 2
0D	PSDU_GOLD_SEED1	PSDU Gold code seed setting 1
0E	PSDU_GOLD_SEED0	PSDU Gold code seed setting 0
0F	DSSS_PREAMBLE3	DSSS preamble pattern setting 3
10	DSSS_PREAMBLE2	DSSS preamble pattern setting 2
11	DSSS_PREAMBLE1	DSSS preamble pattern setting 1
12	DSSS_PREAMBLE0	DSSS preamble pattern setting 0
13	SS_DOWN_SIZE	DSSS downsampling setting
14	SS_AFC_RANGE_SYNC	DSSS AFC range setting (during synchronization)
15	SS_AFC_RANGE	DSSS AFC range setting (during receiving data)
16	Reserved	Reserved
17	DSSS_RATE_SYNC_H	DSSS synchronization receive chip rate setting (high byte)
18	DSSS_RATE_SYNC_L	DSSS synchronization receive chip rate setting (low byte)
19	DSSS_RATE_H	DSSS receive chip rate setting (High byte)
1A	DSSS_RATE_L	DSSS receive chip rate setting (low byte)
1B	SS_SYNC_BIT8_GATE_H	Correlation threshold level in DSSS synchronization setting(high byte)
1C	SS_SYNC_BIT8_GATE_L	Correlation threshold level in DSSS synchronization setting(low byte)
1D	SS_SYNC_BIT8_GATE2_H	Correlation threshold level in DSSS synchronization setting 2 (high byte)
1E	SS_SYNC_BIT8_GATE2_L	Correlation threshold level in DSSS synchronization setting 2 (low byte)
1F	SS_SYNC_BIT_GATE_H	Correlation threshold level after DSSS synchronization setting (high byte)
20	SS_SYNC_BIT_GATE_L	Correlation threshold level after DSSS synchronization setting(low byte)
21-30	Reserved	Reserved
31	SS_AFC_OUT	DSSS AFC value indication
32	SS_AFC_FIX_EN	DSSS AFC fixed enable setting
33	SS_AFC_FIX	DSSS AFC fixed setting
34-7F	Reserved	Reserved

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK2 registers.

BANK10

Address [HEX]	Register name	Description
00	BANK_SEL	BANK selection
01	BPSK_STEP_CTRL	BPSK step control setting
02	BPSK_STEP_CLK_SET	BPSK step control clock setting
03	Reserved	Reserved
04	BPSK_SETP_SET0	BPSK step control setting0
05	BPSK_SETP_SET1	BPSK step control setting1
06	BPSK_SETP_SET2	BPSK step control setting2
07	BPSK_SETP_SET3	BPSK step control setting3
08	BPSK_SETP_SET4	BPSK step control setting4
09	BPSK_SETP_SET5	BPSK step control setting5
0A	BPSK_SETP_SET6	BPSK step control setting6
0B	BPSK_SETP_SET7	BPSK step control setting7
0C	BPSK_SETP_SET8	BPSK step control setting8
0D	BPSK_SETP_SET9	BPSK step control setting9
0E	BPSK_SETP_SET10	BPSK step control setting10
0F	BPSK_SETP_SET11	BPSK step control setting11
10	BPSK_SETP_SET12	BPSK step control setting12
11	BPSK_SETP_SET13	BPSK step control setting13
12	BPSK_SETP_SET14	BPSK step control setting14
13	BPSK_SETP_SET15	BPSK step control setting15
14	BPSK_SETP_SET16	BPSK step control setting16
15	BPSK_SETP_SET17	BPSK step control setting17
16	BPSK_SETP_SET18	BPSK step control setting18
17	BPSK_SETP_SET19	BPSK step control setting19
18	BPSK_SETP_SET20	BPSK step control setting20
19	BPSK_SETP_SET21	BPSK step control setting21
1A	BPSK_SETP_SET22	BPSK step control setting22
1B	BPSK_SETP_SET23	BPSK step control setting23
1C	BPSK_SETP_SET24	BPSK step control setting24
1D	BPSK_SETP_SET25	BPSK step control setting25
1E	BPSK_SETP_SET26	BPSK step control setting26
1F	BPSK_SETP_SET27	BPSK step control setting27
20	BPSK_SETP_SET28	BPSK step control setting28
21	BPSK_SETP_SET29	BPSK step control setting29
22	BPSK_SETP_SET30	BPSK step control setting30
23	BPSK_SETP_SET31	BPSK step control setting31
24	BPSK_SETP_SET32	BPSK step control setting32
25	BPSK_SETP_SET33	BPSK step control setting33
26	BPSK_SETP_SET34	BPSK step control setting34
27	BPSK_SETP_SET35	BPSK step control setting35
28	BPSK_SETP_SET36	BPSK step control setting36
29	BPSK_SETP_SET37	BPSK step control setting37
2A	BPSK_SETP_SET38	BPSK step control setting38
2B	BPSK_SETP_SET39	BPSK step control setting39
2C	BPSK_SETP_SET40	BPSK step control setting40
2D	BPSK_SETP_SET41	BPSK step control setting41
2E	BPSK_SETP_SET42	BPSK step control setting42
2F	BPSK_SETP_SET43	BPSK step control setting43
30	BPSK_SETP_SET44	BPSK step control setting44
31	BPSK_SETP_SET45	BPSK step control setting45
32	BPSK_SETP_SET46	BPSK step control setting46
33	BPSK_SETP_SET47	BPSK step control setting47
34	BPSK_SETP_SET48	BPSK step control setting48

BANK10 (continued)

Address [HEX]	Register name	Description
35	BPSK_SETP_SET49	BPSK step control setting49
36	BPSK_SETP_SET50	BPSK step control setting50
37	BPSK_SETP_SET51	BPSK step control setting51
38	BPSK_SETP_SET52	BPSK step control setting52
39	BPSK_SETP_SET53	BPSK step control setting53
3A	BPSK_SETP_SET54	BPSK step control setting54
3B	BPSK_SETP_SET55	BPSK step control setting55
3C	BPSK_SETP_SET56	BPSK step control setting56
3D	BPSK_SETP_SET57	BPSK step control setting57
3E	BPSK_SETP_SET58	BPSK step control setting58
3F	BPSK_SETP_SET59	BPSK step control setting59
40	PADRV_CTRL	PA driver control setting
41	PADRV_ADJ1	PA driver adjustment1
42	PADRV_ADJ2_H	PA driver adjustment2 (high byte)
43	PADRV_ADJ2_L	PA driver adjustment2 (low byte)
44	PADRV_CLK_SET_H	PA driver control clock setting(high byte)
45	PADRV_CLK_SET_L	PA driver control clock setting(low byte)
46	PADRV_UP_ADJ	PA driver control start time setting
47-7F	Reserved	Reserved

(Note)

1. Other registers are closed register and access is limited. Accessible registers are written in the “initialization table”.calibration operation, do not access BANK2 registers.

●Register Bank0

0x00[BANK_SEL]

Function: Register access bank selection
Address:0x00 (BANK0)
Reset value:0x11

Bit	Bit name	Reset value	R/W	Description
7:4	BANK_ACEN[3:0]	0001	R/W	BANK register access enable 0b0001: BANK0 access 0b0010: BANK1 access 0b0100: BANK2 access 0b1000: BANK3 access 0b0011: BANK6 access 0b0101: BANK7 access 0b1001: BANK10 access Other setting: prohibited
3:0	BANK[3:0]	0001	R/W	BANK selection 0b0001: BANK0 access 0b0010: BANK1 access 0b0100: BANK2 access 0b1000: BANK3 access 0b0011: BANK6 access 0b0101: BANK7 access 0b1001: BANK10 access Other setting: prohibited

(Note)

1. During VCOcalibration operation, do not access BANK2 registers.
2. Register acess can be done by CLK_INIT_DONE([CLK_SET1: B0 0x02(7)]) = 0b0.
   But the registers related to RF status has to be accessed after CLK_INIT_DONE = 0b1.

0x01[RST_SET]

Function: Software reset setting
Address:0x01 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	RST3_EN	0	R/W	Reset3 enable setting 0: reset disable 1: reset enable (after reset, automatically written to 0b0)
6	RST2_EN	0	R/W	Reset2 enable setting 0: reset disable 1: reset enable (after reset, automatically written to 0b0)
5	RST1_EN	0	R/W	Reset1 enable setting 0: reset disable 1: reset enable (after reset, automatically written to 0b0)
4	RST0_EN	0	R/W	Reset 0 enable setting 0: reset disable 1: reset enable (after reset, automatically written to 0b0)
3	RST3	0	R/W	PHY function reset bit7(RST3_EN) = 0b1, reset can be executed. 0: no reset 1: reset execution (after reset, automatically written to 0b0)
2	RST2	0	R/W	RF control function reset bit6(RST2_EN) = 0b1, reset can be executed. 0: no reset 1: reset execution (after reset, automatically written 0b0)
1	RST1	0	R/W	MODEM function reset bit5(RST1_EN) = 0b1, reset can be executed. 0: no reset 1: reset execution (after reset, automatically written to 0b0)
0	RST0	0	R/W	CFG (Configuration) function reset bit4(RST0_EN) = 0b1, reset can be executed. 0: no reset 1: reset execution (after reset, automatically written to 0b0) (Note) all registers, except [CLK_SET2: B0 0x03] register bit6-3, are reset to the initial value. (Note) After reset, FIFO data are not guaranteed.

[Description]

1. Please set enable bit (bit7 to bit4) and execution bit (bit3 to bit0) at the same time. After reset, status are not retained and automatically writen to 0b0.
2. 2µs after writing to the execution bit (bit3 to bit0), reset operation will complete. However, if executing reset in SLEEP state (while SLEEP_EN ([SLEEP/WU_SET:B0 0x2D(0)]) = 0b1), reset will be executed at Clock stabilizzation completion interrupt (INT[0] group1) from SLEEP release and each bit turned to 0b0. If chnaging set value before reset execution, last setting is valid.

0x02[CLK_SET1]

Function: Clock setting 1
Address:0x02 (BANK0)
Reset value:0x3F

Bit	Bit name	Reset value	R/W	Description
7	CLK_INIT_DONE	0	R	Clock stabilization completion flag
6	Reserved	0	R	Reserved
5	CLK5_EN	1	R/W	RX function(DSSS) clock control 0: clock stop 1: clock enable
4	CLK4_EN	1	R/W	ADC clock control 0: clock stop 1: clock enable
3	CLK3_EN	1	R/W	RF function (RFstate control) clock control 0: clock stop 1: clock enable
2	CLK2_EN	1	R/W	TX function (MOD) clock control 0: clock stop 1: clock enable
1	CLK1_EN	1	R/W	RX function(DEMOD) clock control 0: clock stop 1: clock enable
0	CLK0_EN	1	R/W	PHY function clock control 0: clock stop 1: clock enable

0x03[CLK_SET2]

Function: Clock setting 2
Address: 0x03 (BANK0)
Reset value: 0x9B

Bit	Bit name	Reset value	R/W	Description
7	MSTR_CLK_EN	1	R/W	Logic block clock enable control 0: disable 1: enable
6	TCXO_EN	0	R/W	TCXO input control (1) (2) (3) 0: disable 1: enable
5	Reserved	0	R	Reserved
4	XTAL_EN	1	R/W	Crystal oscillator circuits control (1) (2) 0: disable 1: enable
3	RC32K_EN	1	R/W	Internal RC oscillator control 0: disable 1: enable
2	Reserved	0	R/W	Reserved
1	REG_PA_ENB	1	R/W	PA regulator control 0: always-on 1: off at RX
0	LOW_RATE_EN	1	R/W	Receiver section clock slowdown setting 0: disable 1: enable (Note) When this is set to 0b1, the current value for RX state described in the “Power Consumption” is achieved.

(Note)

(1) In case of using TCXO, set TCXO_EN = 0b1. Please make sure only one of the register TCXO_EN and XTAL_EN_EN is set to 0b1.
(2) RST0([RST_SET: B0 0x01(0)]) cannot clear this bit. In order to clear it, use the hardware reset (RESETN pin = “L”) or set this bit to 0b0 by SPI access.
(3) In case of using TCXO, this register must be programmed first. If other registers are set before programming this register, values set to other registers are not valid.

0x04[PKT_CTRL1]

Function: Packet configuration 1
Address: 0x04 (BANK0)
Reset value: 0x03

Bit	Bit name	Reset value	R/W	Description
7:6	EXT_PKT_MODE[1:0]	00	R/W	Extended Link Layer mode setting (Wireless M-Bus) 00: No Extended Link Layer 01: 2-byte extension (Extended Link Layer CI = 0x8C) 10: 8-byte extension (Extended Link Layer CI = 0x8D) Other setting: reserved (Note) Please refer to the “Packet format”. (Note) For 10/16-byte extension, set this to 0b00 and set EXT_PKT_MODE2[DATA_SET2: B0 0x08(7-6)].
5	LEN_LF_EN	0	R/W	Length area bit order setting 0: MSB first 1: LSB first
4	DAT_LF_EN	0	R/W	Data area bit order setting 0: MSB first 1: LSB first
3	RX_EXTPKT_OFF	0	R/W	RX Extended Link Layer mode setting (Wireless M-Bus) 0: Automatically detecting “Extended Link Layer” 1: HW does not check “Extended Link Layer” automatically
2	IEEE802_15_4G_EN	0	R/W	IEEE802.15.4g mode setting 0: IEEE802_15.4g mode disable 1: IEEE802_15.4g mode enable (Note) In case of 0b1 (enable), bit12(CRC setting) and bit11(Whitening setting) of L-field for receiving packet are automatically identified and Whitening/CRC process will be performed. LENGTH_MODE([PKT_CTRL2: B0 0x05(0)]) needs to set to 0b1(2 bytes mode). (Note) In case of TX, there is no auto-identification capability. WHT_SET([DATA_SET2: B0 0x08(0)]) and CRC_LEN[1:0]([PKT_CTRL2: B0 0x05(5-4)]) register settings are needed. (Note) For more detail, please refer “IEEE802.15.4g mode setting”.
1:0	PKT_FORMAT[1:0]	11	R/W	Packet configuration 00: Format A (Wireless M-Bus) 01: Format B (Wireless M-Bus) 10: Format C (non Wireless M-Bus, general purpose format1) 11: Format D (non Wireless M-Bus, general purpose format2) (Note) Please refer to the “Packet format”.

0x05[PKT_CTRL2]

Function: Packet configuration 2
Address: 0x05 (BANK0)
Reset value: 0x10

Bit	Bit name	Reset value	R/W	Description
7	CRC_INIT_SEL	0	R/W	CRC initialized state setting 0: ALL0 1: ALL1
6	CRC_COMP_OFF	0	R/W	CRC complement value OFF setting 0: complement value 1: no complement value
5:4	CRC_LEN[1:0]	01	R/W	CRC length setting 00: CRC8 01: CRC16 10: CRC32 Other setting: reserved (Note) 0b00(CRC8) and 0b10(CRC32) are valid for Format C only. (Note) For details, please refer to the “CRC function”.
3	RX_CRC_EN	0	R/W	RX CRC setting 0: disable 1: enable (CRC calculation) (Note) If enable, CRC results are stored in [CRC_ERR_H/M/L: B0 0x13/14/15] registers for RX data.
2	TX_CRC_EN	0	R/W	TX CRC setting 0: disable 1: enable (CRC calculation) (Note) If enable, CRC(s) are automatically appended to the TX data.
1:0	LENGTH_MODE[1:0]	00	R/W	Length field setting 00: 1-byte mode 01: 2-byte mode (Length is extended upper 3bits)

[Description]

1. In transmission (TX), based on the length from [TX_PKT_LEN_H/L:B0 0x7A/7B] registers, total data length will be calculated. Upon transmitting all data, TX complete.
2. In receiving (RX), based on the length from RX data, total data length will be calculated. Upon reception of all data, RX complete.
3. For details. please refer to the “Packet format”.

0x06[DRATE_SET]

Function: Data rate setting
Address: 0x06 (BANK0)
Reset value: 0xCC

<table>
<tr><th>Bit</th><th>Bit name</th><th>Reset value</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:4</td><td>RX_DRATE [3:0]</td><td>0010</td><td>R/W</td><td>RX data rate setting
(Note) When LOW_RATE_EN ([CLK_SET2:B0 0x03(0)]) = 0b1, optimal values are automatically set to the [RX_RATE1_H/L: B1 0x04/05] and [RX_RATE2: B1 0x06] registers by setting this register.
(Note) However, when LOW_RATE_EN = 0b0, optimal values are not set. It is needed to set specified values directly to the [RX_LATE1_H/L:B1 0x04/05] and [RX_LATE2:B1 0x06] registers according to the “Initialization table”.
(Note) When RXDIO_CTRL[1:0]([DIO_SET:B0 0x0C(7-6)]) = 0b10 or 0b11 (enabling DIO mode), less than or equal 9.6kbps cannot be used by setting this register. It is needed to set specified values directly to the [RX_LATE1_H/L:B1 0x04/05] and [RX_LATE2:B1 0x06] registers according to the “Initialization table”.
<table>
<tr><th>Setting value</th><th>Data rate</th></tr>
<tr><td>0000</td><td>1.2kbps</td></tr>
<tr><td>0001</td><td>2.4kbps</td></tr>
<tr><td>0010</td><td>4.8kbps</td></tr>
<tr><td>0011</td><td>9.6kbps</td></tr>
<tr><td>0100</td><td>10kbps</td></tr>
<tr><td>0101</td><td>19.2kbps</td></tr>
<tr><td>0110</td><td>15kbps</td></tr>
<tr><td>0111</td><td>20kbps</td></tr>
<tr><td>1000</td><td>32.768kbps</td></tr>
<tr><td>1001</td><td>40kbps</td></tr>
<tr><td>1010</td><td>50kbps</td></tr>
<tr><td>1011</td><td>100kbps</td></tr>
<tr><td>1100</td><td>200kbps</td></tr>
</table>
</td></tr>
<tr><td>3:0</td><td>TX_DRATE [3:0]</td><td>0010</td><td>R/W</td><td>TX data rate setting
(Note) By setting this field, based on [TX_RATE_H/L: B1 0x02/03], optimal value is selected.
<table>
<tr><th>Setting value</th><th>Data rate</th></tr>
<tr><td>0000</td><td>1.2kbps</td></tr>
<tr><td>0001</td><td>2.4kbps</td></tr>
<tr><td>0010</td><td>4.8kbps</td></tr>
<tr><td>0011</td><td>9.6kbps</td></tr>
<tr><td>0100</td><td>10kbps</td></tr>
<tr><td>0101</td><td>19.2kbps</td></tr>
<tr><td>0110</td><td>15kbps</td></tr>
<tr><td>0111</td><td>20kbps</td></tr>
<tr><td>1000</td><td>32.768kbps</td></tr>
<tr><td>1001</td><td>40kbps</td></tr>
<tr><td>1010</td><td>50kbps</td></tr>
<tr><td>1011</td><td>100kbps</td></tr>
<tr><td>1100</td><td>200kbps</td></tr>
</table>
</td></tr>
</table>

[Description]

1. In order to change data rate, other registers must be programmed. For details, please refer to the “Data rate setting function”.
2. With 4FSK/4GFSK setting, the bit rate is set. The set rate is halved on Air.

0x07[DATA_SET1]

Function: TX/RX data configuration 1
Address: 0x07 (BANK0)
Reset value: 0x15

Bit	Bit name	Reset value	R/W	Description
7	PB_PAT	0	R/W	TX polarity setting 0: Positive polarity 1: Negative polarity (Note) When this is set to 0b1, the polarity of PR_PAT[PREAMBLE_SET: B0 0x3F(3-0)] is reversed.
6	TX_FSK_POL	0	R/W	TX data polarity setting 0: Data“1” = deviated to higher frequency, Data“0” = deviated to lower frequency 1: Data“1” = deviated to lower frequency, Data“0” = deviated to higher frequency
5	RX_FSK_POL	0	R/W	RX data polarity setting 0: Data“1” = deviated to higher frequency, Data“0” = deviated to lower frequency“0” 1: Data“1” = deviated to lower frequency, Data“0” = deviated to higher frequency
4	GFSK_EN	1	R/W	Gaussian filter setting 0: Gaussian filter disable (FSK mode) 1: Gaussian filter enable (Note) For details, please refer to the “Modulation setting”. (Note) In case of using BPSK modulation, set GFSK_EN=0b1.
3:2	RX_DEC_SCHEME [1:0]	01	R/W	RX data encoding mode setting 00: Manchester encoding 01: NRZ 10: 3-out-of-6 encoding 11: Reserved (Note) The Manchester encoding encodes data “0” to “10” and data “1” to “01”.
1:0	TX_DEC_SCHEME [1:0]	01	R/W	TX data encoding mode setting 00: Manchester encoding 01: NRZ 10: 3-out-of-6 encoding 11: Reserved (Note) The Manchester encoding encodes data “0” to “10” and data “1” to “01”.

0x08[DATA_SET2]

Function: TX/RX data configuration 2
Address: 0x08 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:6	EXT_PKT_MODE2[1:0]	00	R/W	Extended Link Layer mode setting 2 (Wireless M-Bus2013) 00: No Extended Link Layer 01: 10-byte extension (Extended Link Layer CI = 0x8E) 10: 16-byte extension (Extended Link Layer CI = 0x8F) Other setting: reserved (Note) Please refer to the “Packet format”. (Note) For 2/8-byte extension, set this to 0b00 and set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)].
5	FSK_SEL	0	R/W	Multi-ary FSK setting 0: 2FSK mode 1: 4FSK mode
4	SYNCWORD_SEL	0	R/W	SyncWord pattern selection setting 0: Sync word pattern 1 1: Sync word pattern 2 (Note) For details, please refer to the “SyncWord detection function”.
3	2SW_DET_EN	0	R/W	Two SyncWords search setting 0: Two SyncWords searching disable 1: Two SyncWords searching enable (Note) For details, please refer to the “SyncWord detection function”.
2	2PB_DET_EN	0	R/W	Two RX preambles search setting 0: Two preamble patterns search disable (distinguish between “01” pattern and “10” pattern) 1: Two preamble patterns search enable (do not distinguish between “01” pattern and “10” pattern)
1	MAN_POL	0	R/W	Manchester polarity setting 0: Do not inverse polarity 1: Inverse polarity
0	WHT_SET	0	R/W	Whitening setting 0: disable Whitening 1: enable Whitening

0x09[CH_SET]

Function: RF channel setting
Address:0x09 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	description
7:0	RF_CH[7:0]	0000_0000	R/W	RF channel setting (setting range: 0 to 255) For details, please refer to the “Channel frequency setting”.

0x0A[RF_STATUS_CTRL]

Function: RF auto status transition control
Address:0x0A (BANK0)
Reset value:0x08

Bit	Bit name	Reset value	R/W	Description
7	INFINITE_TX	0	R/W	Repeatable Transmision mode setting 0: Transimit one pcket 1: Transmit 'preamble + packet' continuously (Note) In order to terminate the transmission, it needs to set 'Force_TRX_OFF' .
6	AUTO_DATA_REQ	0	R/W	Automatic transmission request setting 0: disabled 1: enabled (Note) When TX-ON is executed with AUTO_DATA_REQ is enabled, ML7404 will generate Data transmission request accept completion interrupt and transmit packet automaticaly. The data of packet are latest data in TX_FIFO.
5	FAST_TX_EN	0	R/W	FAST_TX mode setting 0: disabel FAST_TX mode 1: enable FAST_TX mode (Note) If enable. move to the TX state after the data bytes writtrn into the TX FIFO becomes grater than the value specified by TXFIFO_THRL[5:0] ([TXFIFO_THRL: B0 0x18(5-0)]). (Note) When FAST_TX_EN=0b1, FEC coding processing is not performed normally. In addition, coding processing time is about 350 us after FIFO write completion. Please execute TX_ON by TX_ON command after coding processing.
4	AUTO_TX_EN	0	R/W	Automatic TX mode setting 0: disable automatic TX mode 1: enable automatic TX mode (Note) If enable, TX data specified by the Length are written to the TX FIFO, move to the TX state. (Note) When FAST_TX_EN=0b1, FEC coding processing is not performed normally. In addition, coding processing time is about 350 us after FIFO write completion. Please execute TX_ON by TX_ON command after coding processing.
3:2	RXDONE_MODE[1:0]	10	R/W	RF state setting after packet reception completion. 00: move to IDLE state(TRX_OFF) 01: move to TX state 10: continue RX state 11: move to SLEEP state
1:0	TXDONE_MODE[1:0]	00	R/W	RF state setting after packet transmission completion. 00: move to IDLE state(TRX_OFF) 01: continue TX state 10: move to RX state 11: move to SLEEP state

(Note)

1. For details, please refer to the "LSI State Transition Control".

0x0B[RF_STATUS]

Function: RF state setting and status indication
Address:0x0B (BANK0)
Reset value:0x88

Bit	Bit name	Reset value	R/W	Description
7:4	GET_TRX[3:0]	1000	R	RF staus indication 0110: RX_ON (RX state) 1000: TRX_OFF (RF OFF state) 1001: TX_ON (TX state)
3:0	SET_TRX[3:0]	1000	R/W	RF state setting 0011: Force_TRX_OFF (force RF OFFsetting) 0110: RX_ON (RX setting) (*1) 1000: TRX_OFF (RF OFFsetting) (*3) 1001: TX_ON (TX setting) (*2) *1 During TX operation, setting RX_ON is possible. In this case, after TX completion, move to RX_ON state automatically. *2 During RX operation, setting TX_ON is possible. In this case, after RX completion, move to TX_ON state automatically. *3 If TRX_OFF is selected during TX or RX operation, after TX or RX operation completed, RF is turned off. If Force_TRX_OFF is selected during TX or RX operation, RF is turned off immediately.

[Description]

1. For details, please refer to the “LSI State Transition Control”

0x0C[DIO_SET]

Function: DIO mode configuration
Address:0x0C (BANK0)
Reset Value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	RXDIO_CTRL[1:0]	00	R/W	RX DIO mode setting 00: disable DIO mode (FIFO mode) 01: continuous output mode DIO (demodulated data) and DCLK are constantly output 10: data output mode 1 DIO (undecoded data) and DCLK is output after SyncWord detection. 11: data output mode 2 DIO (decoded data) and DCLK is output after L-field detection. (Note) When measuring BER, set to 0b01. (Note) If 0b10, as FIFO is used for storing undecoded RX data, FIFO cannot be used. By setting bit0(DIO_START) = 0b1, DIO and DCLK are output. Data after SyncWord is stored into FIFO. (Note) If 0b11, as FIFO is used for storing decoded RX data. By setting bit0(DIO_START) = 0b1, DIO and DCLK are output. Upon completion of data (specified by the Length) transfering , DIO and DCLK output are stop. Data after Length field is stored into FIFO.
5:4	TXDIO_CTRL[1:0]	00	R/W	TX DIO mode setting 00: disable DIO mode (FIFO mode) 01: DCLK is constantly output 10: DCLK is output after SyncWord. (Note) When setting 0b01/10, FIFOcannot be used. Encoded data must be sent to ML7404 at the falling edge of DCLK.
3	Reserved	0	R	Reserved
2	DIO_RX_COMPLETE	0	R/W	DIO RX completion setting 0: RX not finished 1: RX completion (Note) after RX completion, reset to 0b0 automatically.
1	Reserved	0	R	Reserved
0	DIO_START	0	R/W	DIO RX data output start setting 0: no OUTPUT (NOT stop output) 1: start OUTPUT (Note) Upon out of synchronization, reset to 0.

(Note)

1. For details, please refer to the “DIO function”.

0x0D[INT_SOURCE_GRP1]

Function: Interrupt status for INT0 to INT7
Address: 0x0D (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7	INT[7]	0	R/W	Clock calibration completion interrupt 0: no interrupt 1: interrupt
6	INT[6]	0	R/W	Wake-up timer completion interrupt 0: no interrupt 1: interrupt (Note) If this interrupt is cleared during SLEEP state, interrupt by wake-up timer completion will not generate. Refer to (Note) 3.
5	INT[5]	0	R/W	FIFO-Full interrupt 0: no interrupt 1: interrupt (Note) Interrupt will be generated when FIFO usage exceeds the threshold defined by TXFIFO_THRH[5:0]([TXFIFO_THRH: B0 0x17(5-0)]) in TX or remaining FIFO exceeds the threshold defined by RXFIFO_THRL[5:0] ([RXFIFO_THRH: B0 0x19(5-0)]) in RX.
4	INT[4]	0	R/W	FIFO-Empty interrupt 0: no interrupt 1: interrupt (Note) Interrupt will be generated when FIFO usage falls below the threshold defined by TXFIFO_THRL[5:0] ([TXFIFO_THRL: B0 0x18(5-0)]) in TX or remaining FIFO falls below the threshold defined by RXFIFO_THRL[5:0] ([RXFIFO_THRL: B0 0x1A(5-0)] in RX.
3	INT[3]	0	R/W	RF state transition completion interrupt 0: no interrupt 1: interrupt
2	INT[2]	0	R/W	PLL unlock interrupt 0: no interrupt 1: interrupt (Note) When VTUNE_INT_ENB [PLL_VTRSLT: B0 0x40(2)] = 0b0, this interrupt is generated at PLL unlock or out of VCO adjustment voltage range detection.
1	INT[1]	0	R/W	VCO calibration completion interrupt or Fuse access completion interrupt or IQ automatic adjustment completion interrupt 0: no interrupt 1: interrupt (Note) After RESETN pin release, (RESETN = “H”) or by setting PDN_EN([SLEEP/WU_SET: B0 0x2D(2)]) = 0b1 to return from SLEEP state, Fuse access completion interrupt occurs. VCO calibration should be done after clearing INT[1].
0	INT[0]	0	R/W	Clock stabilization completion interrupt 0: no interrupt 1: interrupt

(Note)

1. Regardless of [INT_EN_GRP1: B0 0x10] register setting, this register value reflect internal status. For writing, only 0b0 is valid, writing 0b1 is ignored.
2. If one of unmasked interrupt event occur, interrupt pin keeps output “Low”.
3. During SLEEP state, interrupts are not cleared immediately by this register. In this case, interrupts are cleared at the clock stabilization completion timing after return from the SLEEP state. To immediately clear interrupts during SLEEP state, please use SLEEP_INT_CLR.

0x0E[INT_SOURCE_GRP2]

Function: Interrupt status for INT8 to INT15 (RX)
Address:0x0E (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	INT[15]	0	R/W	Sync error interrupt 0: no interrupt 1: interrupt (Note) Upon SyncWord detection, while receiving packet (length specified by L-filed), if RX out-of-sync detected, interrupt will generate.
6	INT[14]	0	R/W	Field checking interrupt 0: no interrupt 1: interrupt
5	INT[13]	0	R/W	SyncWord detection interrupt 0: no interrupt 1: interrupt
4	INT[12]	0	R/W	Reserved
3	INT[11]	0	R/W	RX Length error interrupt 0: no interrupt 1: interrupt
2	INT[10]	0	R/W	Diversity search completion interrupt 0: no interrupt 1: interrupt (Note) After diversity completion, interrupt will generate at SyncWord detection timing.
1	INT[9]	0	R/W	CRC error interrupt 0: no interrupt 1: interrupt (Note) Upon detection of CRC error, interrupt will generate. As Format A/B have multiple CRC-fields, error CRC block is indicated by [CRC_ERR_H/M/L: B0 0x13/14/15] registers. Format C has only one CRC field. Therefore MCU can detect CRC error with this interruption,
0	INT[8]	0	R/W	RX completion interrupt 0: no interupt 1: interrupt (Note) interrupt will generate, when RX data specified by the L-field, received.

[Description]

(1) If the following L-field data is received, RX Length error interruption will generate.

Packet format [PKT_CTRL1:B0 0x04]	Extension format [PKT_CTRL1: B0 0x04]	Length Indicating RX Length error
Format A	No extension	Under 8bytes
	2bytes extension	Under 12bytes
	8bytes extension	Under 16 byte
Format B	No extension	Under 10bytes, 128 to 129 bytes
	2bytes extension	
	8bytes extension	Under 17byte, 19 to 20bytes, 128 to 129bytes
Format C	-	0byte(CRC8) 1byte(CRC16) 2bytes(CRC32)

(Note)

1. Regardless of setting [INT_EN_GRP2: B0 0x11], this register value reflect internal status. For writing, only 0b0 is valid, writing 0b1 is ignored.
2. If one of unmasked interrerupt event occurs, inturrupt pin keeps output “Low” .
3. During SLEEP state, interupts are not cleared immediately by this register. In this case, interrupts are cleared at the clock stabilizzation completion timing after return from the SLEEP state.
   If need to clear interrupts during SLEEP state, please use [SLEEP_INT_CLR:B0 0x75] register.
4. INT[12] (INT_SOURCE_GRP2: B0 0x0E (4)) may be set to 1 at the time of FIFO read-out under reception. Therefore, please ignore INT[12]. In addition, when INT_EN[12](INT_EN_GRP2: B0 0x11 (4))=0b1 and INT[12]=0b1, a interrupt is generated. Please be sure to set INT_EN[12] to 0b0.

0x0F[INT_SOURCE_GRP3]

Function: Inrerrupt status for INT16 to INT23 (TX)
Address:0x0F (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	INT[23]	0	R/W	General purpose timer 2 interrupt 0: no interrupt 1: interrupt
6	INT[22]	0	R/W	General purpose timer 1 interrupt 0: no interrupt 1: interrupt
5	INT[21]	0	R/W	Reserved
4	INT[20]	0	R/W	TX FIFO access error interrupt 0: no interrupt 1: interrupt (Note) During TX using FIFO mode, if the FIFO overrun / underrun occur, or if the next packet data is written to the FIFO before transmitting, interrupt will generate.
3	INT[19]	0	R/W	TX lenghth error interrupt (1) 0: no interrupt 1: interrupt
2	INT[18]	0	R/W	CCA completion interrupt 0: no interrupt 1: interrupt
1	INT[17]	0	R/W	TX Data request accept completion interrupt 0: no interrupt 1: interrupt (Note) Interrupt will generate. when TX data, whose lenghth specified by [TX_PKT_LEN_H/L: B0 0x7A/7B] registers, written to the FIFO,
0	INT[16]	0	R/W	TX completion interrupt 0: no interrupt 1: interrupt (Note) Interrupt will generate.when TX data, whose length specified by the [TX_PKT_LEN_H/L: B0 0x7A/7B] registers, transmitted,

[Description]

1. If the following L-field data is written to the [TX_PKT_LEN_H/L: B0 0x7A/7B] registers, TX Length error interrupt will generate.

Packet format [PKT_CTRL1: B0 0x04]	Extension format [PKT_CTRL1: B0 0x04]	Length indicating TX Length error
Format A	No extension	Under 8bytes
	2bytes extension	Under 12bytes
	8bytes extension	Under 16bytes
Format B	No extension	Under 10bytes, 128 to 129bytes
	2bytes extension	
	8bytes extension	Under 17bytes, 19 to 20bytes, 128 to 129bytes
Format C	-	0byte (CRC8) 1byte (CRC16) 2bytes (CRC32)

(Note)

1. Regardless of setting [INT_EN_GRP3: B0 0x12], this register value reflect internal status. For writing, only 0b0 is valid, writing 0b1 is ignored.
2. If one of unmasked interrerupt event occurs, inturrupt pin keeps output “Low”.
3. During SLEEP state, interupts are not cleared immediately by this register. In this case, interrupts are cleared at the clock stabilizzation completion timing after return from the SLEEP state.
   If need to clear interrupts during SLEEP state, please use [SLEEP_INT_CLR:B0 0x75] register.

0x10[INT_EN_GRP1]

Function: Interupt mask for INT0 to INT7
Address:0x10 (BANK0)
Reset value:0x01

Bit	Bit name	Reset value	R/W	Description
7:0	INT_EN[7:0]	0x01	R/W	Enabling from interrupt 0 event to interrupt 7 event. 0: masking interrupt 1: generate interrupt

[Description]

1. Please refer to the “Interrupt events table”.
2. For event details, please refer to [INT_SOURCE_GRP1: B0 0x0D] register.

0x11[INT_EN_GRP2]

Function: Interupt mask for INT8 to INT15
Address:0x11 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:5	INT_EN[15:13]	0x00	R/W	Enabling from interrupt 13 event to interrupt 15 event. 0: masking interrupt 1: generate interrupt
4	Reserved	0	R/W	
3:0	INT_EN[11:8]	0x00	R/W	Enabling from interrupt 8 event to interrupt 11 event. 0: masking interrupt 1: generate interrupt

[Description]

1. Please refer to the “Interrupt events table”.
2. For event details, please refer to [INT_SOURCE_GRP2: B0 0x0E] register.

(Note)

1. INT[12] (INT_SOURCE_GRP2: B0 0x0E (4)) may be set to 1 at the time of FIFO read-out under reception. Therefore, please ignore INT[12]. In addition, when INT_EN[12](INT_EN_GRP2: B0 0x11 (4))=0b1 and INT[12]=0b1, a interrupt is generated. Please be sure to set INT_EN[12] to 0b0.

0x12[INT_EN_GRP3]

Function: Interuptmask for INT16 to INT23
Address:0x12 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	INT_EN[23:22]	00	R/W	Enabling from interrupt 22 event to interrupt 23 event. 0: masking interrupt 1: generate interrupt
5	Reserved	0	R/W	
4:0	INT_EN[20:16]	0_0000	R/W	Enabling from interrupt 16 event to interrupt 20 event. 0: masking interrupt 1: generate interrupt

[Description]

1. Please refer to the “Interrupt events table”.
2. For event details, please refer to [INT_SOURCE_GRP3: B0 0x0F] register.

0x13[CRC_ERR_H]

Function: CRC error status (high byte)
Address:0x13 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7	CRC_LEN2_EN	0	R/W	CRC length setting 2 enable 0: enable 1: disable
6:5	CRC_LEN2[1:0]	00	R/W	CRC length setting 2 00: CRC8 01: CRC16 10: CRC32 11: Reserved (Note) Enabled in case of CRC_LEN2_EN=0b1, and CRC is calculated according to this setting. Note that the CRC length for packet attachment or packet CRC checking is determined by CRC_LEN([PKT_CTRL2: B0 0x05(5-4)]).
4	CRC_INT_SET	0	R/W	CRC check interrupt selection setting 0: Generate interrupt at CRC error 1: Generate interrupt at CRC OK
3:1	Reserved	000	R	Reserved
0	CRC_ERR[16]	0	R	17th CRC error status (Note) For Format A (Wireless M-Bus). 0: CRC OK or no CRC calculation 1: CRC error

[Description]

1. For details, please refer to the “CRC function”.

0x14[CRC_ERR_M]

Function: CRC error status (middle byte)
Address:0x14 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	CRC_ERR[15]	0	R	16th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
6	CRC_ERR[14]	0	R	15th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
5	CRC_ERR[13]	0	R	14th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
4	CRC_ERR[12]	0	R	13th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
3	CRC_ERR[11]	0	R	12th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
2	CRC_ERR[10]	0	R	11th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
1	CRC_ERR[9]	0	R	10th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
0	CRC_ERR[8]	0	R	9th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)

[Description]

1. For details, please refer to the “CRC function”.

0x15[CRC_ERR_L]

function: CRC error status (low byte)
Address:0x15 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	CRC_ERR[7]	0	R	8th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
6	CRC_ERR[6]	0	R	7th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
5	CRC_ERR[5]	0	R	6th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
4	CRC_ERR[4]	0	R	5th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
3	CRC_ERR[3]	0	R	4th CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A (Wireless M-Bus)
2	CRC_ERR[2]	0	R	3rd CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A or B (Wireless M-Bus)
1	CRC_ERR[1]	0	R	2nd CRC error status 0: CRC OK or no CRC calculation 1: CRC error (Note) For Format A or B (Wireless M-Bus)
0	CRC_ERR[0]	0	R	1st CRCerror status 0: CRC OK or no CRCcalculation 1: CRC error (Note) For Format A or B (Wireless M-Bus) and Format C

[Description]

1. For details, please refer to the “CRC function”.

0x16[STATE_CLR]

Function: State clear control
Address:0x16 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	STATE_CLR_EN	0	R/W	State clear enable 0: disabel State clear 1: enable State clear State clear to bit0-6 can be enabled depending on this bit. This bit will be cleared at State clear.
6:5	Reseverd	00	R	Reserved
4	STATE_CLR4	0	R/W	Address check counter clear 1: Clear addres check counter. (Note) [ADDR_CHK_CTR_H/L:B1 0x62,63] registers wull be cleard (Note) bit7(STATE_CLR_EN) = 0b1 is required. After clear operation and then automatically return to 0b0.
3	STATE_CLR3	0	R/W	Diversity State clear 1: Clear diversity state. (Note) bit7(STATE_CLR_EN) = 0b1 is required. After clear operation and then automatical return to 0b0.
2	STATE_CLR2	0	R/W	PHY State clear 1: Clear PHY state. (Note) bit7(STATE_CLR_EN) = 0b1 is required. After clear operation and then automatically return to 0b0.
1	STATE_CLR1	0	R/W	RX FIFO pointer clear 1: Clear write pointer/read pointer of FIFO. (Note) bit7(STATE_CLR_EN) = 0b1 is required. After clear operation and then automatically return to 0b0.
0	STATE_CLR0	0	R/W	TX FIFO pointer clear 1: Clear write pointer/read pointer of FIFO. (Note) bit7(STATE_CLR_EN) = 0b1 is required. After clear operation and then automatically return to 0b0.

[Description]

1. Please set enable bit (bit7) and execution bit (bit4 to bit0) at the same time. After completing a clearing operation, automatically 0b0 will be written to each bit.
2. After writing to the execution bits, (bit3 to bit0), clearing will be completed within (master clock period × [RX_RATE_H/L: B1 0x04/05] × 2[sec]) μs.

0x17[TXFIFO_THRH]

Function: TX FIFO-Full level setting
Address:0x17 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	TXFIFO_THRH_EN	0	R/W	TX FIFO Full level enable 0: disable 1: enable
6	Reserved	0	R	Reserved
5:0	TXFIFO_THRH[5:0]	00_0000	R/W	TX FIFO Full level setting (Note) Valid, if bit7(TXFIFO_THRH_EN) = 0b1

[Description]

1. For details, please refer to the “TX FIFO usage notification function”
2. When TX FIFO data size exceeds the threshold , INT[5] (group 1) interrupt will generate.

0x18[TXFIFO_THRL]

Function: TX FIFO-Empty level setting and TX trigger level setting in FAST_TX mode
Address:0x18 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	TXFIFO_THRL_EN	0	R/W	TX FIFO Empty level enable 0: disable 1: enable
6	Reserved	0	R	Reserved
5:0	TXFIFO_THRL[5:0]	00_0000	R/W	TX FIFO Empty level setting and TX trigger level setting in FAST_TX mode (Note) valid if bit7(TXFIFO_THRH_EN) = 0b1. (Note) TXFIFO_THRL[5:0] should be set larger than or equal 1. (Note) If using FAST_TX mode, please set 0b1 to the FAST_TX_EN ([RF_STATUS_CTRL: B0 0x0A(5)]). Empty level should be set less than or equal [FIFO write size(byte) – 3(byte)].

[Description]

1. For details, please refer to the “TX FIFO usage notification function”.
2. When TX FIFO data size becomes below the threshold , INT[4] (gropu 1) interrupt will generate.

0x19[RX FIFO_THRH]

Function: RX FIFO-Full level enable and level setting
Address:0x19 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	RXFIFO_THRH_EN	0	R/W	RX FIFO Full level enable 0: disable 1: enable
6	Reserved	0	R	Reserved
5:0	RXFIFO_THRH[5:0]	00_0000	R/W	RX FIFO Full level settting (Note) Valid if bit7(RXFIFO_THRH_EN) = 0b1.

[Description]

1. For details, please refer to the “RX FIFO usage notification function”.
2. When RX FIFO data size excceds the threshold , INT[5] (group1) interrupt will generate.

0x1A[RX FIFO_THRL]

Function: RX FIFO-Empty level enable and level setting (high byte)
Address:0x1A (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	RXFIFO_THRL_EN	0	R/W	RX FIFO Emptylevel enable 0: disable 1: enable
6	Reserved	0	R	Reserved
5:0	RXFIFO_THRL[5:0]	00_0000	R/W	RX FIFO Emptylevel setting (Note) Valid if bit7(RXFIFO_THRL_EN) = 0b1. (Note) Empty level should be set larger or equal 2.

[Description]

1. For details, please refer to the “RX FIFO usage notification function”.
2. When RX FIFO data size becomes below the threshold , INT[4] (group1) interrupt will generate.

0x1B[C_CHECK_CTRL]

Function: Control field detection setting
Address:0x1B (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	CA_RXD_CLR	0	R/W	Data processing if Field mismatch. 0: RX data continue 1: RX data abort (Note) if 0b1 is set, immediately abort RX data and wait for the next RX packet.
6	CA_INT_CTRL	0	R/W	Field check interrupt setting 0: generate interrupt if Field match. 1: generate interrupt if Field mismatch. (Note) selecte interupt will becomen INT[14] (group2).
5	Reserved	0	R	Reserved
4	C_FIELD_CODE5_EN	0	R/W	Control field pattern 5 check enable 0: disable 1: enable (Note) The pattern 5 has specific function. If received Control field data matches with the patterm 5, immediately generate interrupt and following M-filed and A-field check do not proceed. Field mismach interrupt will not generate.
3	C_FIELD_CODE4_EN	0	R/W	Control field code #4 check enable 0: disable 1: enable
2	C_FIELD_CODE3_EN	0	R/W	Control field code #3 check enable 0: disable 1: enable
1	C_FIELD_CODE2_EN	0	R/W	Control field code #2 check enable 0: disable 1: enable
0	C_FIELD_CODE1_EN	0	R/W	Control field code #1 check enable 0: disable 1: enable

[Description]

1. For details, please refer to the “Field check function”.
2. When using field check function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) = 0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

0x1C[M_CHECK_CTRL]

Function: Manufacture ID field detection setting
Address:0x1C (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:4	RCV_CONT_SEL[1:0]	00	R/W	Continued reception condition setting at continuous operation timer completion 00: Continue reception when SyncWord detection interrupt is generated 01: Continue reception when Field check interrupt is generated 10: Continue reception when RX sync is established 11: Reserved
3	M_FIELD_CODE4_EN	0	R/W	Manufacture ID field code #4 check enable 0: disable 1: enable
2	M_FIELD_CODE3_EN	0	R/W	Manufacture ID field code #3 check enable 0: disable 1: enable
1	M_FIELD_CODE2_EN	0	R/W	Manufacture ID field code #2 check enable 0: disable 1: enable
0	M_FIELD_CODE1_EN	0	R/W	Manufacture ID field code #1 check enable 0: disable 1: enable

[Description]

1. For details, please refer to the “Field check function”.
2. Field check function is enabled only in the FIFO mode which judges L-field (RXDIO_CTRL[DIO_SET: B0 0x0C(7-6)] = 0b00) and in the data output mode 2 of the DIO mode (RXDIO_CTRL[DIO_SET: B0 0x0C(7-6)] = 0b11).

0x1D[A_CHECK_CTRL]

Function: Address field detection setting
Address:0x1D (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	A_FIELD_CODE6_EN	0	R/W	Address field code #6 check enable 0: disable 1: enable
4	A_FIELD_CODE5_EN	0	R/W	Address field code #5 check enable 0: disable 1: enable
3	A_FIELD_CODE4_EN	0	R/W	Address field code #4 check enable 0: disable 1: enable
2	A_FIELD_CODE3_EN	0	R/W	Address field code #3 check enable 0: disable 1: enable
1	A_FIELD_CODE2_EN	0	R/W	Address field code #2 check enable 0: disable 1: enable
0	A_FIELD_CODE1_EN	0	R/W	Address field code #1 check enable 0: disable 1: enable

[Description]

1. For details, please refer to the “Field check function”.
2. When using field check function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) = 0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

0x1E[C_FIELD_CODE1]

Function: Control field setting (code #1)
Address:0x1E (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	C_FIELD_CODE1[7:0]	0000_0000	R/W	C-field setting code #1

[Description]

1. For details, please refer to the “Field check function”.

0x1F[C_FIELD_CODE2]

Function: Control field setting (code #2)
Address:0x1F (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	C_FIELD_CODE2[7:0]	0000_0000	R/W	C-field setting code #2

[Description]

1. For details, please refer to the “Field check function”.

0x20[C_FIELD_CODE3]

Function: Control field setting (code #3)
Address:0x20 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	C_FIELD_CODE3[7:0]	0000_0000	R/W	C-field setting code #3

[Description]

1. For details, please refer to the “Field check function”.

0x21[C_FIELD_CODE4]

Function: Control field setting (code #4)
Address:0x21 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	C_FIELD_CODE4[7:0]	0000_0000	R/W	C-field setting code #4

[Description]

1. For details, please refer to the “Field check function”.

0x22[C_FIELD_CODE5]

Function: Control field setting (code #5)
Address:0x22 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	C_FIELD_CODE5[7:0]	0000_0000	R/W	C-field setting code #5

[Description]

1. For details, please refer to the “Field check function”.

0x23[M_FIELD_CODE1]

Function: Manufacture ID 1st byte setting (code#1)
Address:0x23 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	M_FIELD_CODE1[7:0]	0000_0000	R/W	M-field 1st byte setting code #1

[Description]

1. For details, please refer to the “Field check function”.

0x24[M_FIELD_CODE2]

Function: Manufacture ID 1st byte setting (code#2)
Address:0x24 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	M_FIELD_CODE2[7:0]	0000_0000	R/W	M-field 1st byte setting code #2

[Description]

1. For details, please refer to the “Field check function”.

0x25[M_FIELD_CODE3]

Function: Manufacture ID 2nd byte setting (code#1)
Address:0x25 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	M_FIELD_CODE3[7:0]	0000_0000	R/W	M-field 2nd byte setting code #1

[Description]

1. For details, please refer to the “Field check function”.

0x26[M_FIELD_CODE4]

Function: Manufacture ID 2nd byte setting (code#2)
Address:0x26 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	M_FIELD_CODE4[7:0]	0000_0000	R/W	M-field 2nd byte setting code #2

[Description]

1. For details, please refer to the “Field check function”.

0x27[A_FIELD_CODE1]

Function: Address field 1st byte setting
Adress:0x27 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	A_FIELD_CODE1[7:0]	0000_0000	R/W	A-field setting (1st byte)

[Description]

1. For details, please refer to the “Field check function”.

0x28[A_FIELD_CODE2]

Function: Address field 2nd byte setting
Adress:0x28 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	A_FIELD_CODE2[7:0]	0000_0000	R/W	A-fieldsetting (2nd byte)

[Description]

1. For details, please refer to the “Field check function”.

0x29[A_FIELD_CODE3]

Function: Address field 3rd byte setting
Adress:0x29 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	A_FIELD_CODE3[7:0]	0000_0000	R/W	A-field setting (3rd byte)

[Description]

1. For details, please refer to the “Field check function”.

0x2A[A_FIELD_CODE4]

Function: Address field 4th byte setting
Adress:0x2A (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	A_FIELD_CODE4[7:0]	0000_0000	R/W	A-field setting (4th byte)

[Description]

1. For details, please refer to the “Field check function”.

0x2B[A_FIELD_CODE5]

Function: Address field 5th byte setting
Adress:0x27B (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	A_FIELD_CODE5[7:0]	0000_0000	R/W	A-field setting (5th byte)

[Description]

1. For details, please refer to the “Field check function”.

0x2C[A_FIELD_CODE6]

Function: Address field 6th byte setting
Adress:0x2C (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	A_FIELD_CODE6[7:0]	0000_0000	R/W	A-field setting (6th byte)

[Description]

1. For details, please refer to the “Field check function”.

0x2D[SLEEP/WU_SET]

Function: SLEEP execution and Wake-up operation setting
Address:0x2D (BANK0)
Reset value: 0x06

Bit	Bit name	Reset value	R/W	Description
7	WUT_1SHOT_MODE	0	R/W	Wake-up timer operation mode setting 0: continue interval operation 1: after 1 shot operation, stop Wake-up timer.
6	WAKEUP_MODE	0	R/W	After Wake-up operation setting 0: Move to RX_ON 1: Move to TX_ON (Note) When continue operation timer is time-out, move to the SLEEP state. (Note) If TX FIFO is written in the SLEEP state, TX Data request accept completion interrupt (INT[17] group 3) will generate after return from the SLEEP state. (Note) When this is set to 0b1, TX Data should be transmitted before time out of continue operation timer.
5	WU_DURATION_EN	0	R/W	Continue operation timer enable setting after Wake-up. 0: After Wake-up, do not start continue operation timer 1: After Wake-up, start continue operation timer. (Note) When this is set to 0b1, and WAKEUP_MODE = 0b0, if SyncWord or specified fields if specified are not detected until continue operation time-out, automatically move to the SLEEP state.
4	WAKEUP_EN	0	R/W	Wake-up enable setting 0: disable Wake-up 1: enable Wake-up (Note) When 0b1 is set, after wake-up timer is time-out, automatically recover from the SLEEP state. Move to the state specified by bit6 (WAKEUP_MODE).
3	RCOSC_MODE	0	R/W	RC oscillation circuits operation mode setting 0: continuous operation 1: operation when in the SLEEP state. (Note) Please refer to the “SLEEP setting”. (Note) If 0b1 is set when continuous operation timer is used, continuous operation timer does not work. Please set 0b0.
2	WUT_CLK_SOURCE	1	R/W	Wake-up timer clock source setting 0: External clock source (EXT_CLK Pin #10) 1: On-chip RC oscillation circuit (Note) Please refer to the “SLEEP setting”.
1	PDN_EN	1	R/W	Power control enable at SLEEP 0: All logic power-on 1: Partial logic only power-on (power-off at TX FIFO) (Note) Please refer to the “SLEEP setting”.
0	SLEEP_EN	0	R/W	SLEEP mode control 0: Recover from the SLEEP state (normal operation) 1: Move to SLEEP (Note) Please refer to the “SLEEP setting”.

[Description]

1. For details, please refer to the “Wake-up timer”.

0x2E[WUT_CLK_SET]

Function: Wake-up timer clock division setting
Address:0x2E (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:4	WUDT_CLK_SET[3:0]	0000	R/W	Continuous operation timer clock setting 0000: no division (This setting is prohibitted when XTAL_EN([CLK_SET2: B0 0x02(4)]) = 0b1) 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 1000: divided by 16384 1001: divided by 2 1010: divided by 4 1011: divided by 8 1100: divided by 16 1101: divided by 32 1110: divided by 64 Other setting: divided by 16384 (Note) the source clock is specified by WUT_CLK_SOURCE ([SLEEP/WU_SET: B0 0x2D(2)]). (Note) In case of using continuous operation timer, please set the same value as WUDT_CLK_SET as WUT_CLK_SET.
3:0	WUT_CLK_SET[3:0]	0000	R/W	Wake-up timer clock setting 0000: no division 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 1000: divided by 16384 1001: divided by 2 1010: divided by 4 1011: divided by 8 1100: divided by 16 1101: divided by 32 1110: divided by 64 Other setting: divided by 16384 (Note) the source clock is specified by WUT_CLK_SOURCE ([SLEEP/WU_SET: B0 0x2D(2)]).

[Description]

1. For details, please refer to the “Wake-up timer”.

0x2F[WUT_INTERVAL_H]

Function: Wake-up timer interval setting (high byte)
Address:0x2F (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	WUT_INTERVAL[15:8]	0000_0000	R/W	Wake-up timer interval setting (high byte) (Note) combined toghether with [WUT_INTERVAL_H:B0 0x30] register. Timer interval can be programmed as follows: Wake-up timer interval = Wake-up timer clock cycle ([SLEEP/WU_SET:B0 0x2D(2)])* Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) * Wake-up timer interval setting [WUT_INTERVAL_H/L:B0 0x2F/30] (Note) WUT_INTERVAL[15:0] should be set larger than or equal 2.

[Description]

1. For details, please refer to the “Wake-up timer”.

0x30[WUT_INTERVAL_L]

Function: Wake-up timer interval setting (low byte)
Address:0x30 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	WUT_INTERVAL[7:0]	0000_0000	R/W	Wake-up timer interval setting (low byte) For details, please refer to [TIMER_INTERVAL_H: B0 0x2F] register

[Description]

1. For details, please refer to the “Wake-up timer”.

0x31[WU_DURATION]

function: Continuous operation timer (after Wake-up) setting
Address:0x31 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	WU_DURATION[7:0]	0000_0000	R/W	Continuousoperation timer (after wake-up) setting Operation timer period = Wake-up timer clock cycle ([SLEEP/WU_SET:B0 0x2D(2)]) * Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) * Continuous operation timer setting (WU_DURATI: B0 0x31] (Note) WU_DURATION[7:0] should be set larger than or equal 1.

[Description]

1. For details, please refer to the “Wake-up timer”.

0x32[GT_SET]

Function: General purpose timer configuration
Address:0x32 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	GT2_CLK_SOURCE	0	R/W	General purpose timer #2 clock sources setting 0: wake-up timer clock 1: 2MHz clock
4	GT2_START	0	R/W	General purpose timer #2 execution setting 0: pause timer counting 1: start or resume timer counting (Note) After time-out, reset to 0b0 automatically. (Note) As for restart of timer counting with GT2_CLK_SOURCE=0b0 after timer expiration, restart timer counting after more than two cycles of the wake-up timer clock are complete.
3:2	Reserved	00	R	Reserved
1	GT1_CLK_SOURCE	00	R/W	General purpose timer #1 clock sources setting 0: wake-up timer clock 1: 2MHz clock
0	GT1_START	0	R/W	General purpose timer #1 execution setting 0: pause timer counting 1: start or resume timer counting (Note) After time-out, reset to 0b0 automatically. (Note) As for restart of timer counting with GT1_CLK_SOURCE=0b0 after timer expiration, restart timer counting after more than two cycles of the wake-up timer clock are complete.

[Description]

1. For details, please refer to the “General purpose timer”.

0x33[GT_CLK_SET]

Function: General purpose timer clock division setting
Address:0x33 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:4	GT2_CLK_SET[3:0]	0000	R/W	General purpose timer clock #2 division setting 0000: no division 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 1000: divided by 16384 1001: divided by 32768 Other setting: divided by 65536 (Note): The source clock is specified by GT2_CLK_SOURCE ([GT_SET:B0 0x32(5).
3:0	GT1_CLK_SET[3:0]	0000	R/W	General purpose timer clock #1 division setting 0000: no division 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 1000: divided by 16384 1001: divided by 32768 Other setting: divided by 65536 (Note): The source clock is specified by GT1_CLK_SOURCE ([GT_SET:B0 0x32(1).

[Description]

1. For details, please refer to the “General purpose timer”.

0x34[GT1_TIMER]

Function: General purpose timer #1 setting
Address:0x34 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	GT1_TIMER[7:0]	0000_0000	R/W	General purpose timer #1 period setting General purpose timer #1period = General purpose timer clock cycle ([GT_SET:B0 0x32(1)]) * Division setting ([GT_CLK_SET:B0 0x33(3-0)]) * General purpose timer 1 period setting (GT1_TIMER[7:0])

[Description]

1. For details, please refer to the “General purpose timer”.

0x35[GT2_TIMER]

Function: General purpose timer #2 setting
Address:0x35 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	GT2_TIMER[7:0]	0000_0000	R/W	General purpose timer #2 period setting General purpose timer #2 period = GT2 clock cycle ([GY_SET:B0 0x32(5)]) * Division setting ([GT_CLK_SET:B0 0x33(7-4)]) * GT2 timer period setting (GT2_TIMER[7:0])

[Description]

1. For details, please refer to the “General purpose timer”.

0x36[CCA_IGNORE_LVL]

Function: ED threshold level setting for excluding CCA judgement
Address:0x36 (BANK0)
Reset value:0xFE

Bit	Bit name	Reset value	R/W	Description
7:0	CCA_IGNORE_LVL[7:0]	1111_1110	R/W	ED threshold level setting for excluding CCA running average judgement (Note) An ED value exceeding this threshold, is not used for averaging defined by ED_AVG([ED_CTRL: B0 0x41(2-0)]). CCA result will not be judged until acquiring ED values reached averaging number. CCA_RSLT ([CCA_CTRL: B0 0x39(1-0)]) indicates 0b11 (evaluation on-going).

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x37[CCA_LVL]

Function: CCA threshold setting
Address:0x37 (BANK0)
Reset value:0x5C

Bit	Bit name	Reset value	R/W	Description
7:0	CCA _LVL[7:0]	0101_1100	R/W	CCA thresold level setting (setting range:0 to 255) (Note) If ED value exceed this threshold, CCA_RSLT ([CCA_CTRL: B0 0x39(1-0)]) indicates 0b01 (carrier detected)

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x38[CCA_ABORT]

Function: Timing setting for forced termination of CCA operation
Address:0x38 (BANK0)
Reset value: 0xFF

Bit	Bit name	Reset value	R/W	Description
7:0	CCA _ABORT[7:0]	1111_1111	R/W	CCA forced termination timing setting (range:0 to 255) (Note) If set 0b0000_0000, this function becomes invalid. (Note) 1bit resolution is 128µs (Note) Time out function for avoiding incompletion of CCA operation by carrier detection. If CCA operated period becomes the value defined by this register value x RSSI average interval (16µs), IDLE detection is terminated, packets are discarded, and RF state becomes TRX_OFF.

[Description]

1. For details operation of CCA, please refer to “CCA(Clear Channel Assessment) function”.

0x39[CCA_CTRL]

Function: CCA control setting and result indication
Address:0x39 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	CCA_STOP	0	R/W	CCA continuous mode termination setting (terminate by set 0b1) (Note) If CCA_CPU_EN is executed, CCA will continuously perform until this bit is set to 0b1.
6	CCA_IDLE_EN	0	R/W	CCA IDLE detection mode enable setting 0: disable 1: enable
5	CCA_CPU_EN	0	R/W	CCA continuous mode enable setting 0: disable 1: enablee (Note) CCA will continue untill terminated by CCA_STOP bit.
4	CCA_EN	0	R/W	CCA execution setting 0: not perform CCA 1: perform CCA (Note) After completion of CCA, reset to 0b0 automatically.
3	FAST_DET_MODE_EN	0	R/W	High speed carrier checking mode setting 0: during RX_ON, do not perform CCA. 1: during RX_ON, perform CCA. (Note) As a result of CCA, if no carrier found, automatically move to SLEEP state. Timer function can be combined together as well. For details, please refer to the “Wake-up timer”.
2	CCA_ABORT_EN	0	R/W	CCA forced termination setting 0: do not terminate CCA 1: terminate CCA (Note) valid if bit6(CCA_IDLE_EN) = 0b1.
1:0	CCA_RSLT[1:0]	00	R/W	CCA result 00: no carrier 01: carrier detected 10: CCA evaluation on-going (evaluating IDLE) 11: CCA evaluation on-going (ED value excluding CCA judgement acquisition.) Please refer to [CCA_IGNORE_LVL:B0 0x36]) register. (Note) These bits are not cleared automatically. Every time CCA detects carrier, these bits need to be cleared. These bits are cleared by clearing CCA completion interrupt([INT_SOURCE_GRP3: B0 0x0F(2)]). CCA completion is indicated by INT[18] (group 3).

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.
2. Please do not set 0b1 to both bit6(CCA_IDLE_EN) and bit5(CCA_CPU_EN) at the same time.

0x3A[ED_RSLT]

Function: ED value indication
Address:0x3A (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	ED_VALUE[7:0]	0000_0000	R	ED value indication (Note) If ED_RSLT_SET([ED_CTRL: B0 0x41(3)]) = 0b0, ED value is updated constantly during RX_ON. If ED_RSLT_SET = 0b1, ED value is acquired at SyncWord detection timing. The value is updated at reading RX_FIFO.

[Description]

1. For details of ED value acquisition operation, please refer to the “Energy detection value (ED value) acquisition function”

0x3B[IDLE_WAIT_H]

Function: IDLE detection period setting during CCA (high 2bits)
Address:0x3B (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R	
1:0	IDLE_WAIT[9:8]	00	R/W	IDLE judgement max. wait time setting (high 2bits) (Note) In CCA IDLE judgement, it is used for detecting long IDLE (no carrier) period. (Note)Combined toghether with [IDLE_WAIT_L:B0 0x3C] register. IDLE detection period is programmed as follows. IDLE detection period = ED value averaging period (default 8 times = 128µs) + (IDLE_WAIT[9:0] * 16µs)

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3C[IDLE_WAIT_L]

Function: IDLE detection period setting during CCA (low byte)
Address:0x3C (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	IDLE_WAIT[7:0]	0000_0000	R/W	IDLE judgement max. wait time setting (low byte) For details, please refer to [IDLE_WAIT_H:B0 0x3B] register

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3D[CCA_PROG_H]

Function: IDLE judgement elapsed time indication during CCA (high 2bits)
Address:0x3D (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R	Reserved
1:0	CCA_PROG[9:8]	00	R	IDLE judgement elapsed time indication during CCA (upper byte) (Note) combined toghether with [CCA_PROG_L:B0 0x3E] register. IDLE judgement elapsed time is calculated as follows. IDLE judgement elapsed time = ED value averaging period (default 8 times = 128µs) + (IDLE_WAIT[9:0] * 16µs)

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3E[CCA_PROG_L]

Function: IDLE judgement elapsed time indication during CCA (low byte)
Address:0x3E (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	CCA_PROG[7:0]	0000_0000	R	IDLE judgement elapsed time indication during CCA (low byte) For details, please refer to [CCA:PROG_H:B0 0x3D] register.

[Description]

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3F[PREAMBLE_SET]

Function: Preamble pattern setting
Address:0x3F (BANK0)
Reset value: 0x05

Bit	Bit name	Reset value	R/W	Description
7:6	CCA_INT_SEL[1:0]	00	R/W	CCA interrupt select setting 00: 01: 10: Other than above: Reserved
5:4	Reserved	00	R	Reserved
3:0	PR_PAT[3:0]	0101	R/W	Preamble pattern setting (Note) Sent in sequence from MSB side.

0x40[VCO_VTRSLT]

Function: VCO adjustment voltage result display
Address: 0x40 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2	VTUNE_INT_ENB	0	R/W	Out of VCO adjustment voltage range detection and interrupt notification setting 0: Notify by PLL unlock detection interrupt (INT2[INT_SOURCE_GRP1: B0 0x0D(2)]) 1: Do not generate interrupt (Note) When this is set to 0b1, PLL unlock interrupt is generated at PLL unlock or out of VCO adjustment voltage range detection.
1	VTUNE_COMP_H	0	R	VCO adjustment voltage upper limit threshold display 0: Adjustment voltage is lower than the upper limit 1: Adjustment voltage is equal to or higher than the upper limit
0	VTUNE_COMP_L	0	R	VCO adjustment voltage lower limit threshold display 0: Adjustment voltage is equal to or higher than the lower limit 1: Adjustment voltage is lower than the lower limit

0x41[ED_CTRL]

Function: ED detection control setting
Address: 0x41 (BANK0)
Initial value: 0xA0

Bit	Bit name	Reset value	R/W	Description
7	ED_CALC_EN	1	R/W	ED value calculation enable setting 0: disable ED value calculation 1: enable ED value calculation
6	CCADONE_MODE	0	R/W	RF state setting at high speed carrier checking 0: Move to SLEEP at carrier not detected Continue reception at carrier detected 1: Move to TX_ON at carrier not detected Move to SLEEP at carrier detected (Note) This function is valid when FAST_DET_MODE_EN[CCA_CTRL: B0 0x39(4)] = 0b1.
5	CCA_ED_SEL	1	R/W	ED value calculation signal selection setting at high speed carrier checking 0: Calculate ED value based on channel filter bandpass signal 1: Channel filter 2 (two times as wide as channel filter band) bandpass signal (Note) When this is set to 0b1, the channel filter calculates the ED value with two times as large as filter band set in CHFIL_BW_ADJ[CHFIL_BW: B0 0x54(6-0)].
4	ED_DONE	0	R/W	ED value calculation completion flag 0: calculation on-going (not completed) 1: ED value calculation completion
3	ED_RSLT_SET	0	R	ED indication setting Select ED value displayed in [ED_RSLT:B0 0x3A] register. 0: ED value constantly updated 1: ED value acquired at SyncWord detection timing (Note) If this is set to 0b1, the ED value is updated at reading RX data FIFO. Please read [ED_RSLT:B0 0x3A] after reading FIFO.
2:0	ED_AVG[2:0]	000	R/W	ED value calculation average times setting 000: 1 time average 001: 2 times average 010: 4 times average 011: 8 times average 100: 16 times average 101: 32 times average Other than above: 16 times average (Note) ED_AVG[2:0] must be set when ED value calculation is stopped (TRX_OFF state or TX_ON state or bit7(ED_CALC_EN) = 0b0).

[Description]

1. For details of ED value acquisition operation, please refer to the “Energy detection value(ED value) acquisition function”.

0x42[TXPR_LEN_H]

Function: TX preamble length setting (high byte)
Address:0x42 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TXPR_LEN[15:8]	0000_0000	R/W	TX preamble length setting (high byte) (setting range: 0x0001 to 0xFFFF) TX preamble length = (specified value x2) bits (Note) combined toghether with [TXPR_LEN_L: B0 0x43] register. (Note) Do not set value less than 0x0010 to TXPR_LEN[15:0] in a system that requires preamble. ML7404 requires more than or equal 0x0010 preamble for synchronization. (Note) If diversity is used, this parameter may have to change according to the data rate. Please refer to the “Initialization table”

0x43[TXPR_LEN_L]

Function: TX preamble length setting (low byte)
Address:0x43 (BANK0)
Reset value:0x08

Bit	Bit name	Reset value	R/W	Description
7:0	TXPR_LEN[7:0]	0000_1000	R/W	TX preamble length setting (low byte) For details, please refer to [TXPR_LEN_H:B0 0x42] register.

0x44[POSTAMBLE_SET]

Function: Postamble length and pattern setting
Address:0x44 (BANK0)
Reset value:0x12

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:4	POSTAMBLE_LEN[2:0]	001	R/W	Postamble length setting Postamble length = (specified value × 2) bits.
3	Reserved	0	R	Reserved
2:1	POSTAMBLE_PAT[1:0]	01	R/W	Postamble pattern setting 00: “01” pattern repetition 01: “10” pattern repetition 10: repetition of the last CRC pattern and its inversion 11: “11” pattern repetition
0	POSTAMBLE_EN	0	R/W	Postamble enable setting 0: no postamble addition 1: postamble addition

0x45[SYNC_CONDITION1]

Function: RX preamble setting and ED threshold check setting
Address:0x45 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	SYNC_ED_EN	0	R/W	ED threshold check enable setting during synchronization 0: disable ED threshold check during synchronization 1: enable ED threshold check during synchronization (Note) ED threshold value is set to the [SYNC_CONDITION2: B0 0x46] register.
6	Reserved	0	R	Reserved
5:0	RXPR_LEN[5:0]	00_0000	R/W	RX preamble checking length setting (setting range: 0 to 32, unit: bit) (Note) if lager than 0b10_0000, interpret as 0b10_0000. (Note) when 1 or more value is set to this register, for syncword detection, syncword detection is performed with the pattern added to syncword pattern for the number of preambles set. If the false detection probability is high only with the syncword length, this function can reduce the probability by adding a preamble. (Note) ML7404 requires AFC convergence time(Max 24 bits). If the preamble comparison length set in RXPR_LEN[5:0] overlaps the AFC convergence time, syncword can not be detected. Therefore, please set this register to a value equal to or less than the number of bytes obtained by subtracting the AFC convergence time from the transmission preamble.

0x46[SYNC_CONDITION2]

Function: ED threshold setting during synchronization detection
Address:0x46 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_ED_TH[7:0]	0000_0000	R/W	ED thereshold value setting during synchronization (Note) If SYNC_ED_EN ([SYNC_CONDITION1: B0 0x45(7)]) = 0b1, ED thereshold value become valid. (Note) If acquired ED value does not exceed this threshold, synchronization is not detected.

0x47[SYNC_CONDITION3]

Function: Bit error tolerance setting in RX preamble and SyncWord detection.
Address:0x47 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:4	SW_RCV[3:0]	0000	R/W	Error tolerance value (bits) in the SyncWord (setting range: 0 to 15)
3:0	PB_RCV[3:0]	0000	R/W	Error tolerance value (bits) in the preamble (setting range: 0 to 15)

0x48[2DIV_CTRL]

Function: Antenna diversity setting
Address:0x48 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	ANT_CTRL1	0	R/W	ANT control bit1
4	ANT_CTRL0	0	R/W	ANT control bit0
3	INV_ANT_SW	0	R/W	ANT_SW polarity setting
2	INV_TRX_SW	0	R/W	TRX_SW polarity setting
1	2PORT_SW	0	R/W	Antenna switch setting 0: SPDT switch is used 1: DPDT switch is used
0	2DIV_EN	0	R/W	Antenna diversity setting 0: no antenna diversity 1: antenna diversity

[Description]

1. For details, please refer to the “Diversity function”.

0x49[2DIV_RSLT]

Function: Antenna diversity result indication
Address:0x49 (BANK0)
Reset value:0x01

Bit	Bit name	Reset value	R/W	Description
7	2DIV_DONE	0	R	Antenna diversity search completion status 0: diversity search on-going (not completed) 1: diversity search completion
6:2	Reserved	0_0000	R	Reserved
1:0	2DIV_RSLT[1:0]	01	R	Antenna diversity result 01: Antenna 1 10: Antenna 2

[Description]

1. For details, please refer to the “Diversity function”.
2. This register is updated at SyncWord detection timing in each packet.

0x4A[ANT1_ED]

Function: Acquired ED value by antenna 1
Address:0x4A (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	ANT1_ED[7:0]	0000_0000	R	Acquired ED value by antenna 1 (Note) Set 2DIV_EN([2DIV_CTRL: B0 0x48(0)]) = 0b1. This register is updated at SyncWord detection timing in each packet. However, if diversity completion interrupt- ([INT_SOURCE_GRP2: B0 0x0D(2)]) is cleared, this register will be cleared.

0x4B[ANT2_ED]

Function: Acquired ED value by antenna 2
Address:0x4B (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	ANT2_ED[7:0]	0000_0000	R	Acquired ED value by antenna 2 (Note) Set 2DIV_EN([2DIV_CTRL: B0 0x48(0)]) = 0b1. This register is updated at SyncWord detection timing in each packet. However, if diversity completion interrupt- ([INT_SOURCE_GRP2: B0 0x0D(2)]) is cleared, this register will be cleared.

0x4C[ANT_CTRL]

Function: TX/RX antenna control setting
Address:0x4C (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	RX_ANT	0	R/W	Antenna setting for RX 0: antenna 1 1: antenna 2 (Note) Valid if bit4(RX_ANT_EN) = 0b01. This bit defines antenna during RX_ON.
4	RX_ANT_EN	0	R/W	Antenna settinge enable for RX 0: disable 1: enable
3:2	Reserved	00	R	Reserved
1	TX_ANT	0	R/W	Antenna setting for TX 0: antenna 1 1: antenna 2 (Note) Valid If bit0(TX_ANT_EN) = 0b01. This bit defines antenna during TX_ON.
0	TX_ANT_EN	0	R/W	Antenna settinge enable for TX 0: disable 1: enable

[Description]

1. For details, please refer to the “Diversity function”.

0x4D[MON_CTRL]

Function: Monitor function setting
Address:0x4D (BANK0)
Reset value:0x01

Bit	Bit name	Reset value	R/W	Description
7	BER_MODE	0	R/W	BER measurement mode setting 0: normal operation mode 1: BER measurement mode (Note) By setting BER measurement mode, demodulated data/clock are output from DIO/DCLK. For details, please refer to the "BER Measurement Setting"
6	FIFOMODE_MON	0	R/W	FIFO mode monitor setting 0: FIFO mode and DIO/DCLKare not output. 1: FIFOmode and DIO/DCLKare output. (Note) Demodulated data/clock are output from DIO/DCLK.
5:4	DMON_SET2[1:0]	00	R/W	Digital monitor output signal selection setting 00: L output Others: reserved
3:0	DMON_SET	0001	R/W	Digital monitor output signal selection setting 0000: "L" output 0001: CLK_OUT output 0010: PLL lock detection signal output (if PLL is locked, digital monitor signal outputs "H") 0011: Synchronization detection signal output (if synchronization is completed, digital monitor signal outputs "H") Other setting: reserved

0x4E[GPIO0_CTRL]

Function: GPIO0 pin (pin #16) cpnfiguration setting
Address:0x4E (BANK0)
Reset value:0x07

Bit	Bit name	Reset value	R/W	Description
7	GPIO0_INV	0	R/W	GPIO0 output signal polarity setting
6	GPIO0_OD	0	R/W	GPIO0 output OpenDrain setting 0: CMOS output 1: OpenDrain output
5	GPIO0_FORCEOUT	0	R/W	GPIO0 forced output value setting 0: "L" output 1: "H" output (Note) the setting of bit7(GPIO0_INV) does not affect on this output value.
4	GPIO0_FORCEOUTEN	0	R/W	GPIO0 forced output enable setting 0: disable 1: enable (output the value according to bit5(GPIO0_FORCEOUT) setting.)
3:0	GPIO0_IO_CFG[3:0]	0111	R/W	GPIO0 input-output signal setting 0000: [output] "L" level 0001: [output] antenna switch control signal 1 (TX-RX switch signal: TRW_SW) 0010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 0011: [output] external PA control signal 0100: [input/output] data (DIO) 0101: [output] data clock (DCLK) 0110: [output] digital monitor signal please refer to DEMON_SET[3:0] ([MON_CTRL:B0 0x4D(3-0)]). 0111: [output] interrupt notification signal (SINTN) 1001: [output] digital monitor signal 2

0x4F[GPIO1_CTRL]

Function: GPIO1 pin (pin #17) configuration setting
Address:0x4F (BANK0)
Reset value:0x06

Bit	Bit name	Reset value	R/W	Description
7	GPIO1_INV	0	R/W	GPIO1 output signal polarity setting
6	GPIO1_OD	0	R/W	GPIO1 output OpenDrainsetting 0: CMOS output 1: OpenDrain output
5	GPIO1_FORCEOUT	0	R/W	GPIO1 output forced setting 0: “L” output 1: “H” output (Note) the setting of bit7(GPIO1_INV) does not affect on this output value.
4	GPIO1_FORCEOUTEN	0	R/W	GPIO1 forced output enable setting 0: disable 1: enable (output the value according to bit5(GPIO1_FORCEOUT) setting.)
3:0	GPIO1_IO_CFG [3:0]	110	R/W	GPIO1 input-output signal selection setting 0000: [output] “L” level 0001: [output] antenna switch control signal 1 (TX-RX switch signal: TRW_SW) 0010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 0011: [output] external PA control signal 0100: [input/output] data (DIO) 0101: [output] data clock (DCLK) 0110: [output] digital monitor signal please refer to DEMON_SET[3:0] ([MON_CTRL:B0 0x4D(3-0)]) 0111: [output] Interrupt notification signal (SINTN) 1000: [input] SLEEP state release signal 1001: [output] digital monitor signal 2

0x50[GPIO2_CTRL]

Function: GPIO2 pin (pin #18) configuration setting
Address:0x50 (BANK0)
Reset value:0x02

Bit	Bit name	Reset value	R/W	Description
7	GPIO2_INV	0	R/W	GPIO2 output signal polarity setting
6	GPIO2_OD	0	R/W	GPIO2 output OpenDrain setting 0: CMOS output 1: OpenDrain output
5	GPIO2_FORCEOUT	0	R/W	GPIO2 forced output value setting 0: “L” output 1: “H” output (Note) the setting of bit7(GPIO2_INV) does not affect on this output value.
4	GPIO2_FORCEOUTEN	0	R/W	GPIO2 forced output enable setting 0: disable 1: enable (output the value according to bit5(GPIO2_FORCEOUT) setting.)
3:0	GPIO2_IO_CFG [3:0]	0010	R/W	GPIO2 input-output signal selection setting 0000: [output] “L” level 0001: [output] antenna switch control signal 1 (TX-RX switch signal: TRW_SW) 0010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 0011: [output] external PA control signal 0100: [input/output] data (DIO) 0101: [output] data clock (DCLK) 0110: [output] digital monitor signal please refer DEMON_SET[3:0] ([MON_CTRL:B0 0x4D(3:0)]) 0111: [output] Interrupt notification signal (SINTN) 1001: [output] digital monitor signal 2

0x51[GPIO3_CTRL]

Function: GPIO3 pin (pin#19) configuration setting
Address:0x51 (BANK0)
Reset value:0x01

Bit	Bit name	Reset value	R/W	Description
7	GPIO3_INV	0	R/W	GPIO3 output signal polarity setting
6	GPIO3_OD	0	R/W	GPIO3 output OpenDrain setting 0: CMOS output 1: OpenDrain output
5	GPIO3_FORCEOUT	0	R/W	GPIO3 output forced setting 0: “L” output 1: “H” output (Note) the setting of bit7(GPIO3_INV) does not affect on this output value.
4	GPIO3_FORCEOUTEN	0	R/W	GPIO3 forced output enable setting 0: disable 1: enable (output the value accoding to bit5(GPIO3_FORCEOUT) setting.)
3:0	GPIO3_IO_CFG [3:0]	0001	R/W	GPIO3 input-output signal selection setting 0000: [output] “L” level 0001: [output] antenna switch control signal 1 (TX-RX switch signal:TRW_SW) 0010: [output] antenna switch control signal 2 (antenna switch signal:ANT_SW) 0011: [output] external PA control signal 0100: [input/output] data (DIO) 0101: [output] data clock (DCLK) 0110: [output] digital monitor signal please refer to DEMON_SET[3:0] ([MON_CTRL:B0 0x4D(3:0)]) 0111: [output] Interrupt notification signal (SINTN) 1001: [output] digital monitor signal 2

0x52[EXTCLK_CTRL]

Function: EXT_CLK pin (pin #10) control setting
Address:0x52 (BANK0)
Reset value:0x03

Bit	Bit name	Reset value	R/W	Description
7	EXTCLK_INV	0	R/W	EXT_CLK output signal polarity setting
6	EXTCLK _OD	0	R/W	EXT_CLK output OpenDrain setting 0: CMOS output 1: OpenDrain output
5	EXTCLK _FORCEOUT	0	R/W	EXT_CLK output forced setting 0: “L” output 1: “H” output (Note) the setting of bit7(EXTCLK_INV) does not affect on this output value.
4	EXTCLK _FORCEOUTEN	0	R/W	EXT_CLK forced output enable setting 0: disable 1: enable (output the value according to bit5(EXTCLK_FORCEOUT) setting.)
3:0	EXTCLK _IO_CFG [3:0]	0011	R/W	EXT_CLK input/outputsignal selection setting 0000: [input] external clock (32 kHz) 0001: [output] antenna switch control signal 1 (TX/RXswitch signal: TRX_SW) 0010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 0011: [output] external PA control signal 0100: [input/output] data (DIO) 0101: [output] During RX: RX clock output During TX: TX clock output 0110: [output] Digital monitor signal 0111: [output] interrupt notificationsignal (SINTN) output 1001: [output] digital monitor signal 2

0x53[SPI/EXT_PA_CTRL]

Function: SPI interface(SDI/SDO)pins/external PAcontrol
Address:0x53 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	SDO_OD	0	R/W	SDO output Open Drain setting 0: CMOS output 1: Open Drain output
6	Reserved	0	R	Reserved
5	SDO_CFG	0	R/W	SDO pin (pin #12) input/output signal setting 0: [output] SDO (SPI interface) 1: [output] SDO (when SCEN pin (pin #14) = “L”) SCEN pin = when “H”, DCLK output For details, please refer to the “DIO function”
4	SDI_CFG	0	R/W	SDI pin (pin #15) input/ouput signal setting 0: [input] SDI(SPI interface) 1: [input] SDI (when SCEN pin (pin #14) = “L” [input/output] DIO (when SCEN pin = “H”) For details, please refer to the “DIO function”
3:2	Reserved	00	R	Reserved
1	EXT_PA_CNT	0	R/W	External PA control signal control timing setting 0: TX_ON signal output. 1: PA_ON signal output. For details of each signal timing, please refer to “TX” in the “Timing Chart”
0	EXT_PA_EN	0	R/W	External PA control timing enable setting 0: disable (“L” output) 1: enable (valid bit1(EXT_PA_CNT) setting)

0x54[CHFIL_BW]

Function: Channel filter bandwidth setting
Address: 0x54 (BANK0)
Reset value: 0x01

Bit	Bit name	Reset value	R/W	Description
7	CHFIL_WIDE_SET	0	R/W	Channel Filter Wideband setting 0: Channel filter band width are set with CHFIL_BW_ADJ always 1: Channel filter band width are double width set with CHFIL_BW_ADJ always
6:0	CHFIL_BW_ADJ[6:0]	000_0001	R/W	Channel filter bandwidth setting (Setting range: 1 to 127) Channel filter bandwidth [Hz] = {Master clock frequency * (CHFIL_WIDE_SET+1)}/ (Setting value * 180} (Note) The initial value is 200kHz. (Note) For details, see the “Setting Channel Filter Bandwidth.” (Note) 0b000_0000 is prohibited

0x55[DC_I_ADJ_H]

Function: I phase DC offset adjustment setting (high 6bits)
Address: 0x55 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7	DC_ADJ_SET	0	R/W	DC offset correction setting 0: Automatic adjustment 1: Manual adjustment
6	DC_ADJ_HOLD	0	R/W	DC offset adjustment hold setting 0: always updated 1: fix DC offset value after synchronized.
5:0	DC_I_ADJ[13:8]	00_0000	R/W	I phase DC offset adjustment setting (Note) This adjustment value is valid when bit7 is set to 0b1. (Note) A negative setting value is specified in the two's complement format. (Note) Combined with 8 bits of [DC_I_ADJ_L:B0 0x56] register.

0x56[DC_I_ADJ_L]

Function: I phase DC offset adjustment setting (low byte)
Address: 0x56 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	DC_I_ADJ[7:0]	0000_0000	R/W	I phase DC offset adjustment setting (Note) For details, please refer to [DC_I_ADJ_H:B0 0x55] register.

0x57[DC_Q_ADJ_H]

Function: Q phase DC offset adjustment setting (high 6bits)
Address: 0x57 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	DC_Q_ADJ[13:8]	00_0000	R/W	Q phase DC offset adjustment setting (Note) This adjustment value is valid when DC_ADJ_SET[DC_I_ADJ_H: B0 0x55(7)] is set to 0b1. (Note) A negative setting value is specified in the two's complement format. (Note) Combined with 8 bits of [DC_I_ADJ_L:B0 0x58] register.

0x58[DC_Q_ADJ_L]

Function: Q phase DC offset adjustment setting (low byte)
Address: 0x58 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	DC_Q_ADJ[7:0]	0000_0000	R/W	Q phase DC offset adjustment setting (Note) For details, please refer to [DC_Q_ADJ_H:B0 0x57] register.

0x59[DC_FIL_ADJ]

Function: DC offset adjustment filter setting
Address: 0x59 (BANK0)
Reset value: 0xD5

Bit	Bit name	Reset value	R/W	Description
7:6	DC_FIL_ADJ2[1:0]	11	R/W	DC offset adjustment filter setting 2 00: disable 01: 1/16 10: 1/32 11: 1/64
5	DC_FIL_MODE	0	R/W	DC offset adjustment filter mode setting 0: Start with the initial state 1: Start with DC offset value at receiving last packet
4	DC_FIL_ON	1	R/W	DC offset adjustment filter enable setting 0: disable 1: enable
3	Reserved	0	R	Reserved
2:0	DC_FIL_SEL[2:0]	101	R/W	DC offset adjustment filter setting 000: 1/4 001: 1/8 010: 1/16 011: 1/32 100: 1/64 101: 1/128 110: 1/256 111: disable(DC offset adjustment filter) (Note) Set the adjustment filter constant to be used when DC_ADJ_SET[DC_I_ADJ_H: B0 0x55(7)] is set to 0b0 (automatic adjustment).

0x5A[IQ_MAG_ADJ_H]

Function: IF IQ amplitude balance adjustment (high 4bits)
Address: 0x5A (BANK0)
Reset value: 0x08

Bit	Bit name	Reset value	R/W	Description
7	IQ_ADJ_DONE	0	R	IQ automatic adjustment completion display 0: Not completed 1: Completed
6	IQ_ADJ_RSLT	0	R	IQ automatic adjustment status display 0: RSSI value after IQ automatic adjustment is larger than RSSI threshold set in [IQ_ADJ_TARGET: B0 0x5F] 1: RSSI value after IQ automatic adjustment is smaller than RSSI threshold set in [IQ_ADJ_TARGET: B0 0x5F]
5	LOCAL_SEL	0	R/W	RX local frequency setting 0: Lower-Local setting (for Normal receiving mode) 1: Upper-Local setting (for IQ adjustment) (Note) Set 0b0 when Normal receiving mode
4	IQ_ADJ_START	0	R/W	IQ automatic adjustment execution 0: Execution completion 1: Execution start (Note) The result after automatic adjustment is stored in IQ_MAG_ADJ[11:0], IQ_PHASE_ADJ_SIGN [IQ_PHASE_ADJ_H: B0 0x5C(4)] and IQ_PHASE_ADJ [IQ_PHASE_ADJ_H/L: B0 0x5C(3-0)/0x5D(7-0)].
3:0	IQ_MAG_ADJ[11:8]	1000	R/W	IQ signal amplitude adjustment setting (high 4bits) (Note) Combined with 8bits of the [IQ_MAG_ADJ_L:B0 0x5B] register, this is calculated using a total of 12bits. bit11: 1 bit10: 1/2 bit9 : 1/4 bit8 : 1/8 bit7 : 1/16 bit6 : 1/32 bit5 : 1/64 bit4 : 1/128 bit3 : 1/256 bit2 : 1/512 bit1 : 1/1024 bit0 : 1/2048

[Description]

1. Image rejection can be adjusted by IQ_MAG_ADJ[11:0]. For details, please refer to the “I/Q Adjustment”.

0x5B[IQ_MAG_ADJ_L]

Function: IF IQ amplitude balance adjustment (low byte)
Address: 0x5B (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	IQ_MAG_ADJ[7:0]	0000_0000	R/W	IQ signal amplitude adjustment setting (low byte) (Note) Combined with 4bits of [IQ_MAG_ADJ_H:B0 0x5A] register, this is calculated using a total of 12bits.

[Description]

1. Image rejection can be adjusted by IQ_MAG_ADJ[11:0]. For details, please refer to the “I/Q Adjustment”.

0x5C[IQ_PHASE_ADJ_H]

Function: IF IQ phase balance adjustment (high 3bits)
Address: 0x5C (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4	IQ_PHASE_ADJ_SIGN	0	R/W	IQ signal phase adjustment sign bit 0: Plus 1: Minus
3	Reserved	0	R	Reserved
2:0	IQ_PHASE_ADJ[10:8]	000	R/W	IQ signal phase adjustment setting (high 3bits) (Note) Combined with 8bits of the [IQ_PHASE_ADJ_L:B0 0x5D] register, this is calculated using a total of 11bits. bit10: 1/2 bit9 : 1/4 bit8 : 1/8 bit7 : 1/16 bit6 : 1/32 bit5 : 1/64 bit4 : 1/128 bit3 : 1/256 bit2 : 1/512 bit1 : 1/1024 bit0 : 1/2048

[Description]

1. Image rejection can be adjusted by IQ_PHASE_ADJ [10:0] and IQ_PHASE_ADJ_SIGN. For details, please refer to the "I/Q Adjustment".

0x5D[IQ_PHASE_ADJ_L]

Function: IF IQ phase balance adjustment (low byte)
Address: 0x5D (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	IQ_PHASE_ADJ[7:0]	0000_0000	R/W	IQ signal phase adjustment setting (low byte) (Note) Combined with 3bits of [IQ_PHASE_ADJ_H:B0 0x5C] register, this is calculated using a total of 11bits.

[Description]

1. Image rejection can be adjusted by IQ_PHASE_ADJ [10:0] and IQ_PHASE_ADJ_SIGN. For details, please refer to the "I/Q Adjustment".

0x5E[IQ_ADJ_WAIT]

Function: IF IQ automatic adjustment RSSI acquisition wait time
Address: 0x5E (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4	IQ_ADJ_MODE	0	R/W	IQ automatic adjustment mode setting 0: Best adjustment mode 1: Simple adjustment mode (Note) When this is set to 0b1, IQ automatic adjustment is terminated when a detected RSSI is equal to or less than threshold set in [IQ_ADJ_TARGET: B0 0x5F] during automatic adjustment.
3:2	Reserved	00	R	Reserved
1:0	IQ_ADJ_WAIT[1:0]	00	R/W	IQ automatic adjustment RSSI acquisition wait time setting 00: 1ms 01: 750µs 10: 500µs 11: 250µs

[Description]

1. For details, please refer to the “I/Q Adjustment”.

0x5F[IQ_ADJ_TARGET]

Function: IF IQ automatic adjustment RSSI judgment threshold
Address: 0x5F (BANK0)
Reset value: 0x38

Bit	Bit name	Reset value	R/W	Description
7:0	IQ_ADJ_TARGET[7:0]	0011_1000	R/W	IQ automatic adjustment RSSI judgment threshold (Note) The comparison result between the final RSSI value after IQ automatic adjustment and this setting value is displayed in IQ_ADJ_RSLT[IQ_MAG_ADJ_H: B0 0x5A(6)].

[Description]

1. For details, please refer to the “I/Q Adjustment”.

0x60[DEC_GAIN]

Function: Decimation gain setting
Address: 0x60 (BANK0)
Reset value: 0x18

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4:0	DEC_GAIN[4:0]	1_1000	R/W	Decimation gain setting Gain = 1/2^(setting value - 21)

0x61[IF_FREQ]

Function: IF frequency selection
Address: 0x61 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:4	IF_FREQ_CCA[2:0]	000	R/W	IF frequency selection when CCA 000: 225kHz 001: 150kHz 010: prohibited 011: 112.5kHz 100: prohibited 101: 75kHz 110: prohibited 111: 0kHz
3	Reserved	0	R	Reserved
2:0	IF_FREQ[2:0]	000	R/W	IF frequency selection 000: 225kHz 001: 150kHz 010: prohibited 011: 112.5kHz 100: prohibited 101: 75kHz 110: prohibited 111: 0kHz

[Description]
1. For details, please refer to the “IF frequency setting”.

0x62[OSC_ADJ1]

Function: Coarse adjustment of load capacitance for oscillation circuits
Address: 0x62 (BANK0)
Reset value: 0x88

Bit	Bit name	Reset value	R/W	Description
7:4	OSC_ADJ_COARSE_XO [3:0]	1000	R/W	XO load capacitance coarse adjustment
3:0	OSC_ADJ_COARSE_XI [3:0]	1000	R/W	XI load capacitance coarse adjustment

[Description]
1. For details, please refer to the “Oscillation Circuits Adjustment”.

0x63[OSC_ADJ2]

Function: Fine adjustment of load capacitance for oscillation circuits
Address:0x63 (BANK0)
Reset value:0x80

Bit	Bit name	Reset value	R/W	Description
7:0	OSC_ADJ_FINE[7:0]	1000_0000	R/W	Fine adjustment of load capacitance - approximately 0.02pF/step (adjustment range 0x00 to 0x77)

[Description]
1. For details, please refer to the “Oscillation Circuits Adjustment”.

0x64[Reserved]

Function: Reserved
Address:0x64 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x65[OSC_ADJ4]

Function: Oscillation circuit bias adjustment (start-up)
Address: 0x65 (BANK0)
Reset value: 0x0F

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	OSC_START_SET	0	R/W	OSC start mode setting 0: High-speed starting mode Start with [OSC_ADJ1: B0 0x62] = 0x00, [OSC_ADJ1: B0 0x63] = 0x00 setting 1: Normal starting mode Start with the value set in [OSC_ADJ1: B0 0x62], [OSC_ADJ1: B0 0x63] (note) After OSC output(clock) becomes stable In High-speed starting mode it is changes the mode set by [OSC_ADJ1: B0 0x62]、[OSC_ADJ1: B0 0x63] automatically.
4:0	Reserved	0_1111	R/W	Reserved

0x66[RSSI_ADJ]

Function: RSSI value adjustment
Address:0x66 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	RSSI_ADD	0	R/W	Adjustment direction setting 0: decrease (set -) 1: increase (set +)
6	Reserved	0	R	Reserved
5:0	RSSI_ADJ[5:0]	00_0000	R/W	RSSI adjustment value setting

[Description]

1. For details, please refer to the “Energy Detection Value (ED Value) Adjustment”.

0x67[PA_REG_ADJ_H]

Function: PA regulator output voltage adjustment (high bit)
Address:0x67 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	PA_REG_ADJ_SEL	0	R	PA regulator output voltage adjustment enable setting 0: disable 1: enable (Note) 0b1 should be set only for adjustment. PA regulator output voltages are adjustable in PA_REG_ADJ[8:0] when 0b1 is set.
6:1	Reserved	00_0000	R	Reserved
0	PA_REG_ADJ[8]	0	R/W	PA regulator output voltage adjustment setting (Note) Combined with 8 bits of the [PA_REG_ADJ_L: B0 0x68] register, this is calculated using a total of 9 bits.

[Description]

1. For details, please refer to the “PA Adjustment”.

The following table shows the rough standard of PA_REG_ADJ, PA regulator output voltage, and PA output power.

PA_REG_ADJ[8:0]	PA regulator output voltage [V]
0x000	0.00
…	…
0x082	0.84
…	…
0x0E6	1.48
…	…
0x140	2.06
…	…
0x1FF	3.29

0x68[PA_REG_ADJ_L]

Function: PA regulator output voltage adjustment (low byte)
Address:0x68 (BANK0)
Reset value:0xE4

Bit	Bit name	Reset value	R/W	Description
7:0	PA_REG_ADJ[7:0]	1110_0100	R/W	PA regulator output voltage adjustment setting (Note) Combined with 1 bit of the [PA_REG_ADJ_H:B0 0x67] register, this is calculated using a total of 9 bits.

[Description]

1. For details, please refer to the “PA Adjustment”.

0x69[Reserved]

Function: Reserved
Address:0x69 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x6A[CHFIL_BW_CCA]

Function: Channel filter bandwidth setting when CCA
Address: 0x6A (BANK0)
Reset value: 0x01

Bit	Bit name	Reset value	R/W	Description
7	CHFIL_WIDE_SET_CCA	0	R/W	Channel Filter Wideband setting when CCA 0: Channel filter band width are set with CHFIL_BW_ADJ always 1: Channel filter band width are double width set with CHFIL_BW_ADJ always
6:0	CHFIL_BW_ADJ_CCA [6:0]	000_0001	R/W	Channel filter bandwidth setting when CCA (Setting range: 1 to 127) Channel filter bandwidth [Hz] = {Master clock frequency * (CHFIL_WIDE_SET+1)}/ (Setting value * 180} (Note) The initial value is 200kHz. (Note) For details, see the “Setting Channel Filter Bandwidth.” (Note) 0b000_0000 is prohibited

0x6B[CHFIL_BW_OPTION]

Function: Channel filter bandwidth option setting
Address:0x6B (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	CHFIL_BW_OPTION	000	R/W	Channel filter bandwidth option setting 000: same 001: 0.56 times 010: 0.67 times 011: 0.77 times 100: 0.83 times 101: 0.91 times (Note) This changes the scale factor of the channel filter bandwidth set in [CHFIL_BW: B0 0x54] and [CHFIL_BW_CCA: B0 0x6A].

0x6C[DC_FIL_ADJ2]

Function: DC offset adjustment filter setting 2
Address:0x6C (BANK0)
Reset value:0x03

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	DC_FIL_SEL2[2:0]	011	R/W	DC offset adjustment filter setting 000: 1/4 001: 1/8 010: 1/16 011: 1/32 100: 1/64 (Note) Set the filter time constant to be used when DC_ADJ_SET[DC_I_ADJ_H: B0 0x55(7)] is set to 0b0 (automatic adjustment).

0x6D[DEC_GAIN_CCA]

Function: Decimation gain setting when CCA
Address: 0x6D (BANK0)
Reset value: 0x18

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4:0	DEC_GAIN_CCA[4:0]	1_1000	R/W	Decimation gain setting when CCA Gain = 1/2^(setting value - 21)

0x6E[VCO_CAL]

Function: VCO calibration setting or status indication
Address:0x6E (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	CAL_WR_EN	0	R/W	VCO calibration mode setting 0: automatic setting mode 1: forced writing mode
6:0	VCO_CAL[6:0]	000_0000	R/W	Current VCO calibration value setting (Note) In automatic setting mode, current calibration value is indicated. (Note) In forced writing mode, the value set to VCO_CAL[6:0] will be applied as the calibration value. (If CAL_WR_EN = 0b0, the set value is ignored.) (Note) after completion of clock stabilization, the value will be 0b100_0000.

[Description]

1. For details, please refer to the “VCO Adjustment”.

0x6F[VCO_CAL_START]

Function: VCO calibration execution
Address:0x6F (BANK0)
Reset value:0x00

Bit	Bit name	Reset valu	R/W	Description
7:5	Reserved	000	R	Reserved
4	AUTO_VCOCAL_EN	0	R/W	Automatic VCO calibration execution enable 0: disable automatic VCO calibration 1: execute automatic calibration when recovering from the SLEEP state.
3:1	Reserved	000	R	Reserved
0	VCO_CAL_START	0	R/W	Execute VCO calibration 0: execution completed 1: execution started (Note) After the execution completed, this bit will return to 0 automatically.

[Description]

1. For details, please refer to the “VCO Adjustment”.

0x70[CLK_CAL_SET]

Function: Low speed clock calibration control
Address:0x70 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:4	CLK_CAL_DIV[3:0]	0000	R/W	Clock division control for low speed clock calibration 0000: no division 0001: no division Other setting: division setting
3:1	Reserved	000	R	Reserved
0	CLK_CAL_START	0	R/W	Execute low speed clock calibration 0: execution completion 1: execution start (Note) After the execution completed, this bit will return to 0 automatically.

[Description]

1. For details, please refer to the “Low speed clock shift detection function”.

0x71[CLK_CAL_TIME]

Function: Low speed clock calibration time setting
Address:0x71 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	CLK_CAL_TIME [5:0]	00_0000	R/W	Low speed Clock calibration time setting Calibration time = Wake-up timer clock cycle ([SLEEP/WU_SET:B0 0x2D(2)]) * [set value] (Note) In case of CLK_CAL_TIME=0x3F with the master clock set to 36MHz, this exceeds the upper limit of the clock calibration result status ([CLK_CAL_H/L: B0 0x72/73]). Thus, be sure to set a value less than 0x3E.

[Description]

1. For details, please refer to the “Low speed clock shift detection function”.

0x72[CLK_CAL_H]

Function: Low speed clock calibartion result indication (high byte)
Address:0x72 (BANK0)
Reset value:0xFF

Bit	Bit name	Reset value	R/W	Description
7:0	CLK_CAL [15:8]	1111_1111	R	Low speed clock calibartion result (high byte)

[Description]

1. For details, please refer to the “Low speed clock calibartion Auxiliary function”.

0x73[CLK_CAL_L]

Function: Low speed clock calibartion result indication (low byte)
Address:0x73 (BANK0)
Reset value:0xFF

Bit	Bit name	Reset value	R/W	Description
7:0	CLK_CAL [7:0]	1111_1111	R	Low speed clock calibartion result (low byte)

[Description]

1. For details, please refer to the “Low speed clock calibartion Auxiliary function”.

0x74[Reserevd]

Function: Reserved
Address:0x74 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

0x75[SLEEP_INT_CLR]

Function: Interrupt clear setting during SLEEP state
Address: 0x75 (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R	Reserved
1	AUTO_SLEEP_INT_CLR	0	R/W	Interrupt clear setting during automatic SLEEP 0: not clear interrupt 1: clear interrupt (Note) The interrupt is automatically cleared at wake-up during wake-up timer operation.
0	SLEEP_INT_CLR	0	R/W	Interrupt clear setting during SLEEP 0: not clear interrupt 1: clear interrupt (Note) During SLEEP state, interrupt cannot be cleared by [INT_SOURCE_GRP*: B0 0x0D/0E/0F] registers. By setting this bit to 0b1, interrupt can be cleared. This register can be written only during SLEEP state. After return from SLEEP state, this bit becomes 0b0. (Note) This is applicable to all interrupts [INT_SOURCE_GRP*: B0 0x0D/0E/0F].

0x76[RF_TEST_MODE]

Function: TX test pattern setting
Address:0x76 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	TEST5	0	R/W	CW output
4	TEST4	0	R/W	“01” pattern output
3	TEST3	0	R/W	All “0” output
2	TEST2	0	R/W	All “1” output
1	TEST1	0	R/W	PN9 output
0	TEST_EN	0	R/W	Test mode enable 0: disable test mode 1: enable test mode

[Description]

1. During normal operation, all bits have to be 0b0.
2. More than one bits are enabled at the same time, lowest bit is valid.
3. Data rate is value in the TX_DRATE[3:0] ([DRATA_SET: B0 0x06(3-0)]).
4. During PN9 output setting, any PN9 polynomial can be specified by [WHT_CFG: B1 0x66].
   Most of the commercial Bit error metter use PN9’s polynomial as x^9+x^4+1, which is equivalent to [WHT_CFG: B1 0x66] = 0x08.
5. During TEST_EN=0b1, do not change modulation setting(FSK_SEL([DATA_SET2: B0 0x08(5)])) and frequency deviation setting([FSK_CTRL: B1 0x2F] – [FSK_TIM_ADJ0: B1 0x40]). If you change these register, please set after TEST_EN=0b0.
6. If you use this test mode in FSK mode, please set test mode to enable(TEST_EN=0b1) after TX_ON. Alternatively, if you execute MODEM reset ([RST_SET: B0 0x01]=0x22), you can set test mode to enable before TX_ON.
   When FSK mode
   (1) Set test mode
   (2) Execute TX_ON (SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)])=0b1001)
   (3) Execute MODEM reset([RST_SET: B0 0x01]=0x22)

0x77[STM_STATE]

Function: State machine status/synchronization status indication
Address:0x77 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	MODE_DET_RSLT	0	R	Receiving mode indication 0: Receive mode T 1: Receive mode C (Note) Indication is valid when 2MODE_DET_EN([2MODE_DET:B3 0x23(0)]) =0b1. (Note) Indication becomes valid after Sync Word detection and is updated at every SyncWord detection
6	SYNC_STATE	0	R	RX synchronization detection status 0: not synchronized 1: synchronization detected
5	SW_DET_RSLT	0	R	SyncWord detection indication 0: detect SyncWord #1 (Format A) 1: detect SyncWord #2 (Foomat B) (Note) Indication is valid whne Packet format A or B is selected, i.e., (PKT_FORMAT[PKT_CTRL1: B0 0x04(1-0]=0b00 or 0b01) (Note) Indication becomes valid after Sync Word detection and is updated at every SyncWord detection timing. (Note) This indication is invalid if mode T packet is received in case of 2MODE_DET_EN([2MODE_DET: B3 0x23(0)])=0b1.
4:0	PHY_STATE[4:0]	0_0000	R	State machine status 0_0000: IDLE state 0_0001: Preamble transmission state 0_0010: SyncWord transmission state 0_0011: L-field transmission state 0_0100: Data area TX state 0_0101: Postamble transmission state 0_0110: TX delay waiting state 0_0111: DIO TX state 1_0010: SyncWord detection state 1_0011: L-field receiving state 1_0100: Data area receiving state 1_0111: DIO RX state

0x78[FIFO_SET]

Function: FIFO readout setting
Address:0x78 (BANK0)
Reset value:0x02

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R/W	Reserved
3	CLKINIT_TRX_SET	0	R/W	RF status setting after clock stabilization 0: move to RX state after clock stabilization 1: move to TX state after clock stabilization
2	CLKINIT_TRX_EN	0	R/W	RF status setting enable after clock stabilization 0: disabled 1: enabled
1	FAST_CCA_LC	1	R/W	Low power consumption mode setting in High-speed carrier checking 0: disabled 1: enabled (Note) Demodulation is stoped during High-speed carrier checking
0	FIFO_R_SEL	0	R/W	FIFO readout setting 0: read RX FIFO 1: read TX FIFO (Note) [RD_FIFO:B0 0x7F] register is used for reading both RX FIFO and TX FIFO. If 0b1 is set in order to read TX FIFO, please readout data length specified by [TX_PKT_LEN_H/L: B0 0x7A/7B] registers or set STATE_CLR1 ([STATE_CLR:B0 0x16(1)]) = 0b1 (RX FIFO pointer clear). If FIFO read is aborted without RX FIFO pointer clear and then change to read RX FIFO, reading starts from the interrupting pointer. Therefore RX FIFO could not be read correctly

0x79[RX_FIFO_LAST]

Function: RX FIFO data usage status indication
Address:0x79 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	RX_FIFO_LAST[5:0]	00_0000	R	RX FIFO data usage status (range: 0 to 63) For details, please refer to the “FIFO control function”

0x7A[TX_PKT_LEN_H]

Function: TX packet length setting (high byte)
Address:0x7A (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TX_PKT_LEN[15:8]	0000_0000	R/W	TX packet length setting (high byte) (Note) setting TX data Length. FormatA: Length excluded L-field and CRC-field FormatB/C: Length excluded L-field FormatD: Length is from Data-field to CRC-field (Note) combined toghether with [TX_PKT_LEN_L: B0 0x7B] register. high byte value is valid when LENGTH_MODE([PKT_CTRL: B0 0x05 (0)]) = 0b1 For details, please refer to the “FIFO control function”

0x7B[TX_PKT_LEN_L]

Function: TX packet length setting (low byte)
Address:0x7B (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TX_PKT_LEN[7:0]	0000_0000	R/W	TX packet length setting (low byte) For details, please refer to [PKT_LEN_H: B0 0x7A] register.

0x7C[WR_TX_FIFO]

Function: TX FIFO
Address:0x7C (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TX_FIFO[7:0]	0000_0000	W	TX FIFO (Note) TX data strored in the TX FIFO is one packet, regardless of packet length. If one packet is stored - (after generation of TX data request acceptance completion interrupt (INT[17] and before generation of TX completion interrupt, INT16) - and if the next writing access is atempted, the TX FIFO will be over-wrtten. And TX FIFO access error interrupt, INT[20] (group3) will be generated. In case of TX FIFO access error occurs, set STATE_CLR0([STATE_CLR: B0 0x16(0)]) = 0b1. (TX FIFO pointer clear) For details, plese refer to the “FIFO control function”.

0x7D[RX_PKT_LEN_H]

Function: RX packet length setting and indication (high byte)
Address:0x7D (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	RX_PKT_LEN[15:8]	0000	R	RX packet Length value setting and indication (high byte) (Note) combined toghether with [RX_PKT_LEN_L: B0 0x7E] register. (Note) FormatA/B/C: indicating packet length excluding L-field. FormatD: Because of the packet format that L-field does not exist, FIFO control is done by treating this register as the RX packet length value

0x7E[RX_PKT_LEN_L]

Function: RX packet length setting indication (low byte)
Address:0x7E (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	RX_PKT_LEN[7:0]	0000_0000	R	RX packet Length value setting and indication (low byte) For details, please refer to [RX_PKT_LEN_H: B0 0x7D] register.

0x7F[RD_FIFO]

Function: FIFO read
Address: 0x7F (BANK0)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	RD_FIFO[7:0]	0000_0000	R	FIFO read (Note) Read FIFO specified by FIFO_R_SEL([FIFO_SET: B0 0x78(0)]). (Note) When RX operation, RX data can be stored up to one packet length, regardless of packet length. If one packet data is stored and the next packet is received, the FIFO will be over-written. (Note) If FIFO read is aborted, set STATE_CLR1 ([STATE_CLR:B0 0x16(1)]) = 0b1 (RX FIFO pointer clear). (Note) For details, please refer to the “FIFO control function”. (Note) If FIFO is read during sleep, set STATE_CLR1([STATE_CLR: B0 0x16(1)]) = 0b1 to clear the RX FIFO pointer.

●Register Bank1

0x00[BANK_SEL]

[Description]
Refer to [BANK_SEL:B0 0x00]

0x01[CLK_OUT]

Function: CLKOUT output frequency setting
Address:0x01 (BANK1)
Reset value:0x05

Bit	Bit name	Reset value	R/W	Description
7:0	CLK_DIV[7:0]	0000_0101	R/W	Output clock frequency setting The following formula is used. 0000_0000: 36MHz 0000_0001: 18MHz 0000_0010: 12MHz (Duty ratio ⋯High:Low = 1:2) 0000_0011: 9MHz 0000_0100: 6MHz 0000_0101: 4.5MHz 0000_0110: 3.6MHz 0000_0111: 1.0MHz 0000_1000: 0.6MHz 0000_1001: 246.5MHz Other setting: The following formula is used to define output frequency. Output frequency = 36 / (16 * [set value] + 2) [MHz] For example, If value is 0x0A, Output frequency = 36 / (16 * 10 + 2) = 222kHz

0x02[TX_RATE_H]

Function: TX data rate conversion setting (high byte)
Address:0x02 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TX_RATE[15:8]	0000_0000	R/W	TX data rate conversion setting (high byte) (Note) combined toghether with [TX_RATE_L: B1 0x03] register. When a given data rate is set, the following formula is used. Setting value = round (master clock frequency / 10 / [a given data rate]) For details, please refer to the “Data rate setting function”

0x03[TX_RATE_L]

Function: TX data rate conversion setting (low byte)
Adress:0x03 (BANK1)
Reset value:0x12

Bit	Bit name	Reset value	R/W	Description
7:0	TX_RATE[7:0]	0001_0010	R/W	TX data rate conversion setting (low byte) For details, please refer to [TX_RATE_H:B1 0x02] register .

0x04[RX_RATE1_H]

Function: RX data rate concversion setting 1 (high byte)
Address:0x04 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	RX_RATE1[15:8]	0000_0000	R/W	RX data rate conversion setting (high byte) (Note) combined toghether with [RX_RATE1_L: B1 0x05] register. When a given data rate is set, the following formula is used. Setting value = round ({master clock frequency / N} / {[a given data rate] × [RX_RATE2:B1 0x06]register}) where, N=1(LOW_RATE_EN([CLK_SET2: B0 0x03(0)]) =0b0) N=2(LOW_RATE_EN([CLK_SET2: B0 0x03(0)]) =0b1) For details, please refer to the “Data rate setting function”

0x05[RX_RATE1_L]

Function: RX data rate cnvesrion setting 1 (low byte)
Address:0x05 (BANK1)
Reset value:0x09

Bit	Bit name	Reset value	R/W	Description
7:0	RX_RATE1[7:0]	0000_1001	R/W	RX data rate conversion setting 1 (low byte) For details, please refer to “[RX_RATE1_H]” register.

0x06[RX_RATE2]

Function: RX data rate conversion setting 2
Address: 0x06 (BANK1)
Reset value: 0x0A

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	RX_RATE2[6:0]	000_1010	R/W	RX data rate conversion setting 2 (setting range: 30 to 127) (Note) Combined with the RX_RATE1 register. For details, please refer to [RATE_SET1_H/L] register. (Note) Do not set this to a value between 0x1D and 0x01. Note that 0x00 is set as 128.

0x07[Reserved]

Function: Reserved
Address:0x07(BANK1)
Reset value:0x5E

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0101_1110	R/W	Reserved

0x08[OSC_W_SEL]

Function: Clock stabilization waiting time setting
Address:0x08 (BANK1)
Reset value:0x20

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:5	OSC_W_SEL[1:0]	01	R/W	Clock stabilization waiting time setting 00: 500µs 01: 250µs 10: prohibited 11: prohibited (Note) When start-up or return from SLEEP state, the waiting time for clock stabilization is set by this register. For details, please refer to “Start-up time” in the “Timing Chart”.
4:0	Reserved	0_0000	R/W	Reserved

0x09-0x0A[Reserved]

Function: Reserved
Address:0x09-0x0A(BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x0B[PLL_LOCK_DETECT]

Function: PLL lock detection setting
Address:0x0B (BANK1)
Reset value:0x81

Bit	Bit name	Reset value	R/W	Description
7	PLL_LD_EN	1	R/W	State control after PLL unlock detection when TX operation 0: Keep TX state 1: Stop TX state forcibly by Force_TRX_OFF (Note) after PLL unlock detection, generates INT2 (group 1) and then move to selected state. (Note) during RX operation, after PLL unlock detection, generates INT2 and keep RX state.
6:0	TIM_PLL_LD[6:0]	000_0001	R/W	PLL lock detection time adjustment Detection time = ([set value] * 8µs +1µs (default: 9µs) (Note) If PLL lock detection signal = "H" period excceds the detection time, determined as PLL lock. If detecting PLL lock detection signal = "L", determined as PLL unlock immediately.

(Note)

1. When move to IDLE state due to PLL unlock detection, please clear PLL unlock interrupt (INT[2] group1) before transmitting or receive next data. And [RF_STATE:B0 0x0B] registers write access must be after 5µs.
2. For details about PLL unlock detection condition and timing, please refer to the "VCO Adjustment".

0x0C-0x0D[Reserved]

Function: Reserved
Address:0x0C-0x0D(BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x0E[GAIN_HOLD]

Function: Gain switching setting
Address:0x0E (BANK1)
Reset value:0x80

Bit	Bit name	Reset value	R/W	Description
7	GAIN_SYNC_HOLD	1	R/W	Gain switching setting 0: constantly updating 1: Upon synchronization established, gain will be fixed. (Note) During BER measurement, set 0b0.
6:0	Reserved	000_0000	R	Reserved

0x0F[RSSI_STABLE_RES]

Function: RSSI Stabilization wat time resolution setting
Address:0x0F-0x10(BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:1	Reserved	000_0000	R	Reserved
0	RSSI_STABLE_RES	0	R/W	RSSI Stabilization wait time resolution setting 0: 1 times 1: ½ times (Note) Combined with [RSSI_STABLE: B1 0x12], RSSI stabilization wait time is set.

0x10[GC_MODE_DIV]

Function: Gain control mode setting in diversity
Address:0x10(BANK1)
Reset value:0x0F

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3:0	GC_MODE_DIV [3:0]	1111	R/W	Gain control mode setting when diversity mode 0001: High-High gain fix 0010: High gain fix 0011: High gain ↔ High-High gain transition enable 0100: Middle gain fix 0110: Middle gain ↔ High gain transition enable 0111: Middle gain ↔ High gain ↔ High-High gain transition enable 1000: Low gain fix 1100: Low gain ↔ Middle gain transition enable 1110: Low gain ↔ Middle gain ↔ High gain transition enable 1111: Low gain ↔ Middle gain ↔ High gain ↔ High-High gain transition enable Other than above: High gain fix

0x11[Reserved]

Function: Reserved
Address:0x11(BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x12[RSSI_STABLE_TIME]

Function: RSSI stabilization wait time setting
Address: 0x12 (BANK1)
Reset value: 0x23

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:4	RSSI_STABLE2[2:0]	010	R/W	RSSI stabilization wait time setting after gain switching at high speed carrier checking (Note) This period is RSSI stabilization time after gain switching. During this period, RSSI value is not used for ED value calculation. Wait time[s] = 1/{Master clock frequency / CHFIL_BW_ADJ[CHFIL_BW: B0 0x54(6-0)] setting value / 8} × Wait time samples × [RSSI_STABLE_RES: B1 0x12] The relationship between the setting value and the wait time samples is as follows: 000: 50 samples 001: 100 samples 010: 125 samples 011: 150 samples 100: 175 samples 101: 200 samples 110: 225 samples 111: 250 samples
3	Reserved	0	R	Reserved
2:0	RSSI_STABLE[2:0]	011	R/W	RSSI stabilization wait time setting (Note) This period is RSSI stabilization time after gain switching. During this period, RSSI value is not used for ED value calculation. Wait time[s] = 1/{Master clock frequency / CHFIL_BW_ADJ[CHFIL_BW: B0 0x54(6-0)] setting value / 8} × Wait time samples × [RSSI_STABLE_RES: B1 0x12] The relationship between the setting value and the wait time samples is as follows: 000: 50 samples 001: 100 samples 010: 125 samples 011: 150 samples 100: 175 samples 101: 200 samples 110: 225 samples 111: 250 samples

(Note)

1. Do not set 0x00 to this register. Please use the value specified in the “Initialization table”.

0x13[RSSI_MAG_ADJ]

Function: Scale factor setting for ED value conversion
Address: 0x13 (BANK1)
Reset value: 0x0C

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4	RSSI_MAG_D4	0	R/W	RSSI scaling factor 2 times setting 0: Do not apply 1: Apply
3	RSSI_MAG_D3	1	R/W	RSSI scaling factor 1 time setting 0: Do not apply 1: Apply
2	RSSI_MAG_D2	1	R/W	RSSI scaling factor 1/2 times setting 0: Do not apply 1: Apply
1	RSSI_MAG_D1	0	R/W	RSSI scaling factor 1/4 times setting 0: Do not apply 1: Apply
0	RSSI_MAG_D0	0	R/W	RSSI scaling factor 1/8 times setting 0: Do not apply 1: Apply

(Note)

1. For details, please refer to the “Energy Detection Value (ED Value) Adjustment”.
2. Please use the value specified in the “Initialization table”.
3. For this register, the setting value is calculated by adding up the scaling factors that are set to 0b1 (for example, when 0b1 is written to bit3 and bit1, the total scaling factor is the sum of 1 and 1/4, that is 1.25). Even if a calculated value is larger than 0xFF, it is limited to 0xFF.

0x14[Reserved]

Function: Reserved
Address:0x14 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x15[AFC/GC_CTRL]

Function: AFC /gain control setting
Address: 0x15 (BANK1)
Reset value: 0x0F

Bit	Bit name	Reset value	R/W	Description
7	AFC_EN	0	R/W	AFC enable setting 0: disable AFC 1: enable AFC
6:4	Reserved	000	R	Reserved
3:0	GC_MODE [3:0]	1111	R/W	Gain control mode setting 0001: High-High gain fix 0010: High gain fix 0011: High gain ↔ High-High gain transition enable 0100: Middle gain fix 0110: Middle gain ↔ High gain transition enable 0111: Middle gain ↔ High gain ↔ High-High gain transition enable 1000: Low gain fix 1100: Low gain ↔ Middle gain transition enable 1110: Low gain ↔ Middle gain ↔ High gain transition enable 1111: Low gain ↔ Middle gain ↔ High gain ↔ High-High gain transition enable Other than above: High gain fix

(Note)
1. Please use the value specified in the “Initialization table”.

0x16[CRC_POLY3]

Function: CRC polynomial setting 3
Address:0x16 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	CRC_POLY [30:24]	000_0000	R/W	CRC polynomial setting 3

[Description]
1. For details, please refer to the “CRC function”.

0x17[CRC_POLY2]

Function: CRC polynomial setting 2
Address:0x17 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	CRC_POLY [23:16]	0000_0000	R/W	CRC polynomial setting 2

[Description]
1. For details, please refer to the “CRC function”.

0x18[CRC_POLY1]

Function: CRC polynomial setting 1
Address:0x18 (BANK1)
Reset alue:0x1E

Bit	Bit name	Reset name	R/W	Description
7:0	CRC_POLY [15:8]	0001_1110	R/W	CRC polynomial setting 1

[Description]

1. For details, please refer to the “CRC function”.

0x19[CRC_POLY0]

Function: CRC polynomial setting 0
Address:0x19 (BANK1)
Reset value:0xB2

Bit	Bit name	Reset name	R/W	Description
7:0	CRC_POLY [7:0]	1011_0010	R/W	CRC polynomial setting 0

[Description]

1. For details, please refer to the “CRC function”.

0x1A[PLL_DIV_SET]

Function: PLL frequency division setting
Address: 0x1A (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R/W	Reserved
1:0	PLL_MODE	00	R/W	PLL mode setting 00: No division 10: Divide by 2 Other than above: reserved (Note) When this is set to 0b10, set 2 times as large as the desired frequency for the settings related to the PLL frequency. For the registers related to the PLL frequency, refer to the “Frequency Setting Function”.

0x1B[TXFREQ_I]

Function: TX frequency setting (I counter)
Address:0x1B (BANK1)
Reset value:0x19

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R/W	Reserved
5:0	TXFREQ_I [5:0]	01_1001	R/W	TX frequency setting - I counter (Note) Reset value is 920.7MHz

[Description]

1. For details, please refer to the “Channel #0 frequency setting”.

0x1C[TXFREQ_FH]

Function: TX frequency setting (F counter high 4bit)
Address:0x1C (BANK1)
Reset value:0x09

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R/W	Reserved
3:0	TXFREQ_F[19:16]	1001	R/W	TX frequency setting (F counter high 4bits) (Note) Reset value is 920.7MHz

[Description]
For details, please refer to the “Channel #0 frequency setting”.

0x1D[TXFREQ_FM]

Function: TX frequency setting (F counter middle byte)
Address:0x1D (BANK1)
Reset value:0x33

Bit	Bit name	Reset value	R/W	Description
7:0	TXFREQ_F[15:8]	0011_0011	R/W	TX frequency setting (F counter middle byte) (Note) Reset value is 920.7MHz

[Description]
1. For details, please refer to the “Channel #0 frequency setting”.

0x1E[TXFREQ_FL]

Function: TX frequency setting (F counter low byte)
Address:0x1E (BANK1)
Reset value:0x33

Bit	Bit name	Reset value	R/W	Description
7:0	TXFREQ_F[7:0]	0011_0011	R/W	TX frequency setting (F counter low byte) (Note) Reset value is 920.7MHz

[Description]
1. For details, please refer to the “Channel #0 frequency setting”.

0x1F[RXFREQ_I]

Function: RX frequency setting (I counter)
Address:0x1F (BANK1)
Reset value:0x19

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R/W	Reserved
5:0	RXFREQ_I[5:0]	01_1001	R/W	RX frequency counter setting (I counter) (Note) Reset value is 920.7MHz

[Description]
1. For details, please refer to the “Channel #0 frequency setting”.

0x20[RXFREQ_FH]

Function: RX frequency setting (F counter high 4bit)
Address:0x20 (BANK1)
Reset value:0x09

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R/W	Reserved
3:0	RXFREQ_F[19:16]	1001	R/W	RX frequency setting F counter (high 4bit) (Note) Reset value is 920.7MHz

[Description]

1. For details, please refer to the “Channel #0 frequency setting”.

0x21[RXFREQ_FM]

Function: RX frequency setting (F counter middle byte)
Address:0x21 (BANK1)
Reset value:0x33

Bit	Bit name	Reset value	R/W	Description
7:0	RXFREQ_F[15:8]	0011_0011	R/W	RX frequency setting F counter (middle byte) (Note) Reset value is 920.7MHz

[Description]

1. For details, please refer to the “Channel #0 frequency setting”.

0x22[RXFREQ_FL]

Function: RX frequency setting (F counter low byte)
Address:0x22 (BANK1)
Reset value:0x33

Bit	Bit name	Reset value	R/W	Description
7:0	RXFREQ_F[7:0]	0011_0011	R/W	RX frequency setting F counter (low byte) (Note) Reset value is 920.7MHz

[Description]

1. For details, please refer to the “Channel #0 frequency setting”.

0x23[CH_SPACE_H]

Function: Channel space setting (high byte)
Address:0x23 (BANK1)
Reset value:0x2D

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	CH_SPACE[15:8]	010_1101	R/W	Channel space setting (high byte) (Note) Reset value is 400 kHz

[Description]

1. For details, please refer to the “Channel space setting”.

0x24[CH_SPACE_L]

Function: Channel space setting (low byte)
Address:0x24 (BANK1)
Reset value:0x83

Bit	Bit name	Reset value	R/W	Description
7:0	CH_SPACE[7:0]	1000_0011	R/W	Channel space setting (low byte) (Note) Reset value is 400 kHz

[Description]

1. For details, please refer to the “Channel space setting”.

0x25[SYNC_WORD_LEN]

Function: SyncWord length setting
Address:0x25 (BANK1)
Reset value:0x08

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	SYNC_WORD_LEN[5:0]	00_1000	R/W	SyncWord length setting (setting range:2 to 32, unit:bit) (Note) If setting is larget than 0b10_0000, operate as 0b10_0000. (Note) If setting is smaller than 0b00_0011, the behavior varies according to operating mode(TX/RX) as follows. (RX) operate as 0b00_0100. (TX) follow setting value.

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x26[SYNC_WORD_EN]

Function: SyncWord enable setting
Address:0x26 (BANK1)
Reset value:0x0F

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3	SYNC_WORD_EN3	1	R/W	SYNC_WORD[31:24] checking enable 0: disable 1: enable
2	SYNC_WORD_EN2	1	R/W	SYNC_WORD[23:16] checking enable 0: disable 1: enable
1	SYNC_WORD_EN1	1	R/W	SYNC_WORD[15:8] checking enable 0: disable 1: enable
0	SYNC_WORD_EN0	1	R/W	SYNC_WORD[7:0] checking enable 0: disable 1: enable

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x27[SYNCWORD1_SET0]

Function: SyncWord #1 setting (bit24 to 31)
Address:0x27 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD1[31:24]	0000_0000	R/W	SyncWord pattern #1 setting (bit24 to 31)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x28[SYNCWORD1_SET1]

Function: SyncWord #1 setting (bit16 to 23)
Address:0x28 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD1[23:16]	0000_0000	R/W	SyncWord pattern #1 setting (bit16 to 23)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x29[SYNCWORD1_SET2]

Function: SyncWord #1 setting (bit8 to 15)
Address:0x29 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD1[15:8]	0000_0000	R/W	SyncWord pattern #1 setting (bit8 to 15)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x2A[SYNCWORD1_SET3]

Function: SyncWord #1 setting (bit0 to 7)
Address:0x2A (BANK1)
Reset value:0x38

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD1[7:0]	0011_1000	R/W	SyncWord pattern #1 setting (bit0 to 7)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x2B[SYNCWORD2_SET0]

Function: SyncWord #2 setting (bit24 to 31)
Address:0x2B (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD2[31:24]	0000_0000	R/W	SyncWord pattern #2 setting (bit24 to 31)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x2C[SYNCWORD2_SET1]

Function: SyncWord #2 setting (bit16 to 23)
Address:0x2C (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD2[23:16]	0000_0000	R/W	SyncWord pattern #2 setting (bit16 to 23)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x2D[SYNCWORD2_SET2]

Function: SyncWord #2 setting (bit8 to 15)
Address:0x2D (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD2[15:8]	0000_0000	R/W	SyncWord pattern #2 setting (bit8 to 15)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x2E[SYNCWORD2_SET3]

Function: SyncWord #2 setting (bit0 to 7)
Address:0x2E (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SYNC_WORD2[7:0]	0000_0000	R/W	SyncWord pattern #2 setting (bit0 to 7)

[Description]

1. For details, please refer to the “SyncWord detection function”.

0x2F[FSK_CTRL]

Function: GFSK/FSK modulation timing resolution setting
Address:0x2F (BANK1)
Reset value:0x02

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R/W	Reserved
5:4	BT_SEL	00	W	BT select setting 00: FSK Frequency Deviation setting([FSK_DEV0_H/GFIL0: B1 0x32]～[FSK_DEV0_H/GFIL6: B1 0x38]) is valid 01: BT=0.3 10: BT=0.4 Others: Reserved
3:1	GFSK_CLKX	001	R/W	GFSK clock setting 000: work with the clock 001: work with double clock 010: wok with clock of 4 times 100: wok with clock of 8 times Other setting: reserved (Note) For some data rates, values that can be set are limited. Refer to "Initialization table" for setting values.
0	FSK_CLK_SET	0	R/W	GFSK/FSK modulation timing resolution setting 0: 4MHz resolution 1: 12MHz resolution (Note) please set 0b0 for ML7404

[Description]

1. For details, please refer to the "Modulation setting".

0x30[GFSK_DEV_H]

Function: GFSK frequency deviation setting (high 6bits)
Address:0x30 (BANK1)
Reset value:0x05

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	GFSK_DEV[13:8]	00_0101	R/W	GFSK frequency deviation setting (high 6bits) / BPSK (frequency control) frequency deviation setting (high 6bits) (Note) combined toghether with [GFSK_DEV_L: B1 0x31] register. (Note) Reset value is 50kHz.

[Description]

1. For details, please refer to the "Modulation setting".

0x31[GFSK_DEV_L]

Function: GFSK frequency deviation setting (low byte)
Address: 0x31 (BANK1)
Reset value:0xB0

Bit	Bit name	Reset value	R/W	Description
7:0	GFSK_DEV[7:0]	1011_0000	R/W	GFSK frequency deviation setting (low byte) / BPSK (frequency control) frequency deviation setting (low byte) (Note) Combined toghether with [GFSK_DEV_H: B1 0x30] register. (Note) Reset value is 50kHz.

[Description]

1. For details, please refer to "Modulation setting".

0x32[FSK_DEV0_H/GFIL0]

Function: FSK 1st frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 0
Address: 0x32 (BANK1)
Reset value:0x22

Bit	Bit name	Reset value	R/W	Description
7:6	GFIL0[7:6]	00	R/W	Gaussian filter coefficient setting 0 (Note) Gaussian filter coefficient bit range is bit7-0.
5:0	FSK_DEV0[13:8]/ GFIL0[5:0]	10_0010	R/W	FSK 1st frequency deviation setting (high 6bits)/ Gaussian filter coefficient setting 0 (Note) 1st frequency deviation in FSK is cilculated with all 14 bit including 8bit of [FSK_DEV0_L/GFIL1:B1 0x33]

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET0: B10 0x04] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x33[FSK_DEV0_L/GFIL1]

Function: FSK 1st frequency deviation setting (low byte) / Gaussian filter coefficient setting 1
Address: 0x33 (BANK1)
Reset value:0x22

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_DEV0[7:0]/ GFIL1[7:0]	0010_0010	R/W	FSK 1st frequency deviation setting (low byte)/ Gaussian filter coefficient setting 1 (Note) 1st frequency deviation in FSK is cilculated with all 14 bit including 6bit of [FSK_DEV0_H/GFIL0:B1 0x32]

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET1: B10 0x05] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x34[FSK_DEV1_H/GFIL2]

Function: FSK 2nd frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 2
Address: 0x34 (BANK1)
Reset value:0x22

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	FSK_DEV1[13:8]/ GFIL2[5:0]	01_0010	R/W	FSK 2nd frequency deviation setting (high 6bits)/ Gaussian filter coefficient setting 2 (Note) 2nd frequency deviation in FSK is cilculated with all 14 bit including 8bit of [FSK_DEV1_L/GFIL3:B1 0x35] Register

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET2: B10 0x06] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x35[FSK_DEV1_L/GFIL3]

Function: FSK 2nd frequency deviation setting (low byte) / Gaussian filter coefficient setting 3
Address: 0x35 (BANK1)
Reset value:0x33

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_DEV1[7:0]/ GFIL3[5:0]	0011_0011	R/W	FSK 2nd frequency deviation setting (low byte)/ Gaussian filter coefficient setting 3 (Note) 2nd frequency deviation in FSK is cilculated with all 14 bit including 6bit of [FSK_DEV1_H/GFIL2:B1 0x34] Register

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET3: B10 0x07] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x36[FSK_DEV2_H/GFIL4]

Function: FSK 3rd frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 4
Address: 0x36 (BANK1)
Reset value:0x22

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	FSK_DEV2[13:8]/ GFIL4[5:0]	10_0010	R/W	FSK 3rd frequency deviation setting (high 6bits)/ Gaussian filter coefficient setting 4 (Note) 3rd frequency deviation in FSK is cilculated with all 14 bit including 8bit of [FSK_DEV2_L/GFIL5:B1 0x37] Registe

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET4: B10 0x08] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x37[FSK_DEV2_L/GFIL5]

Function: FSK 3rd frequency deviation setting (low byte) / Gaussian filter coefficient setting 5
Address: 0x37 (BANK1)
Reset value:0x43

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_DEV2[7:0]/ GFIL5[7:0]	0100_0011	R/W	FSK 3rd frequency deviation setting (low byte)/ Gaussian filter coefficient setting 5 (Note) 3rd frequency deviation in FSK is cilculated with all 14 bit including 6bit of [FSK_DEV2_H/GFIL4:B1 0x36] Register

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET5: B10 0x09] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x38[FSK_DEV3_H/GFIL6]

Function: FSK 4th frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 6
Address: 0x38 (BANK1)
Reset value:0x43

Bit	Bit name	Reset value	R/W	Description
7:6	GFIL6[7:6]	01	R/W	Gaussian filter coefficient setting 6 (Note) Gaussian filter coefficient bit range is bit7-0.
5:0	FSK_DEV3[13:8]/ GFIL6[5:0]	00_0011	R/W	FSK 4th frequency deviation setting (high 6bits) / Gaussian filter coefficient setting 6 (Note) 4th frequency deviation in FSK is cilculated with all 14 bit including 8bit of [FSK_DEV3_L:B1 0x39] Register

[Description]

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.
3. [BPSK_STEP_SET6: B10 0x0A] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x39[FSK_DEV3_L]

Function: FSK 4th frequency deviation setting (low byte)
Address: 0x39 (BANK1)
Reset value:0x54

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_DEV3[7:0]	0101_0100	R/W	FSK 4th frequency deviation setting (low byte) (Note) 4th frequency deviation in FSK is cilculated with all 14 bit including 6bit of [FSK_DEV3_H/GFIL6:B1 0x38] Register.

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET7: B10 0x0B] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x3A[FSK_DEV4_H]

Function: FSK 5th frequency deviation setting (high 6bits)
Address: 0x3A (BANK1)
Reset value:0x45

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	01	R/W	Reserved
5:0	FSK_DEV4[13:8]	00_0101	R/W	FSK 5th frequency deviation setting (high 6bits) (Note) 5th frequency deviation in FSK is cilculated with all 14 bit including 8bit of [FSK_DEV4_L:B1 0x3B] Register.

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET8: B10 0x0C] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x3B[FSK_DEV4_L]

Function: FSK 5th frequency deviation setting (low byte)
Address: 0x3B (BANK1)
Reset value:0x65

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_DEV4[7:0]	0110_0101	R/W	FSK 5th frequency deviation setting (low byte) (Note) 5th frequency deviation in FSK is cilculated with all 14 bit including 6bit of [FSK_DEV4_H:B1 0x3A] Register.

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET9: B10 0x0D] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x3C[FSK_TIM_ ADJ4]

Function: FSK 4th frequency deviation hold time setting
Address: 0x3C (BANK1)
Reset value:0x76

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_TIM_ADJ4 [7:0]	0111_0110	R/W	FSK 4th frequency deviation hold time

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET10: B10 0x0E] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x3D[FSK_TIM_ ADJ3]

Function: FSK 3rd frequency deviation hold time setting
Address: 0x3D (BANK1)
Reset value:0x87

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_TIM_ADJ3[7:0]	1000_0111	R/W	FSK 3rd frequency deviation hold time

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET11: B10 0x0F] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x3E[FSK_TIM_ ADJ2]

Function: FSK 2nd frequency deviation hold time setting
Address: 0x3E (BANK1)
Reset value:0x88

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_TIM_ADJ2[7:0]	1000_1000	R/W	FSK 2nd frequency deviation hold time

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET12: B10 0x10] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x3F[FSK_TIM_ ADJ1]

Function: FSK 1st frequency deviation hold time setting
Address: 0x3F (BANK1)
Reset value:0x88

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_TIM_ADJ1[7:0]	1000_1000	R/W	FSK 1st frequency deviation hold time

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET13: B10 0x11] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x40[FSK_TIM_ ADJ0]

Function: FSK no-deviation frequency (carrier frequency) hold time setting
Address: 0x40 (BANK1)
Reset value:0x77

Bit	Bit name	Reset value	R/W	Description
7:0	FSK_TIM_ADJ0[7:0]	0111_0111	R/W	FSK no-diviation frequency hold time

[Description]

1. For details, please refer to the “Modulation setting”.
2. [BPSK_STEP_SET14: B10 0x12] and this function are sharing this register. However, each register have different function. Therefore, please set a suitable value as each register according to a use(Gaussian filter coefficient, FSK or BPSK step control).

0x41[4FSK_DATA_MAP]

Function: 4FSK data mapping setting
Address: 0x41 (BANK1)
Reset value: 0xE1

Bit	Bit name	Reset value	R/W	Description
7:6	FSK4_FREQ3[1:0]	11	R/W	Data setting for 4th frequency deviation (Note) Setting for the positive maximum frequency deviation.
5:4	FSK4_FREQ2[1:0]	10	R/W	Data setting for 3rd frequency deviation
3:2	FSK4_FREQ1[1:0]	00	R/W	Data setting for 2nd frequency deviation
1:0	FSK4_FREQ0[1:0]	01	R/W	Data setting for 1st frequency deviation (Note) Setting for the negative maximum frequency deviation.

[Description]

1. For details, please refer to the “Modulation setting”.
2. The default value is Wireless M-Bus data mapping.

0x42[FREQ_ADJ_H]

Function: TX/RX frequency fine adjustment setting (high byte)
Address: 0x42 (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7	FREQ_ADJ_SIGN	0	R/W	TX/RX frequency fine adjustment sign setting 0: Minus 1: Plus
6:2	Reserved	0_0000	R	Reserved
1:0	FREQ_ADJ[9:8]	00	R/W	TX/RX frequency fine adjustment setting (high 2bits) (Note) Combined with 8bits of the [FREQ_ADJ_L:B1 0x43] register, this is calculated using a total of 10bits.

[Description]

1. For details, please refer to the “TX/RX frequency adjustment”.

0x43[FREQ_ADJ_L]

Function: TX/RX frequency adjustment setting (low byte)
Address: 0x43 (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	FREQ_ADJ[7:0]	0000_0000	R/W	TX/RX frequency fine adjustment setting (low byte) (Note) Combined with 7bits of the [FREQ_ADJ_H:B1 0x42] register, this is calculated using a total of 15bits.

[Description]

1. For details, please refer to the “TX/RX frequency adjustment”.

0x44-0x47[Reserved]

Function: Reserved
Address: 0x41-0x47 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

0x48[2DIV_MODE]

Function: Average diversity mode setting
Address: 0x48 (BANK1)
Reset value:0x01

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R/W	Reserved
4	SEARCH_MODE	0	R/W	Antenna diversity mode setting 0: disable Antenna diversity FAST mode 1: enable Antenna diversity FAST mode (Note) In FAST mode, if ED value, which is gotten from ANT search for SEARCH_TIME1([2DIV_SEARCH1: B1 0x49(6-0)]), exceeds [2DIV_FAST_LVL: B1 0x4B], then the subsequent search will be canceled and ANT will be fixed.
3	Reserved	0	R	Reserved
2:0	2DIV_ED_AVG [2:0]	001	R/W	Average number of ED calculation during Antenna diversity 000: average 1 time 001: average 2 times 010: average 4 times 011: average 8 times 100: average 16 times 101: average 32 times Other than above: 16 times

[Description]

1. For details, please refer to the “Diversity function”.

0x49[2DIV_SEARCH1]

Function: Antenna diversity search time setting
Address: 0x49 (BANK1)
Reset value:0x8E

Bit	Bit name	Reset value	R/W	Description
7	SEARCH_TIME_SET	1	R/W	Antenna diversity search time resolution setting 0 : 16µs 1 : 256µs (Note) Define search time resolution for both SEARCH_TIME1[6:0] and SEARCH_TIME2[6:0].
6:0	SEARCH_TIME1[6:0]	000_1110	R/W	Antenna diversity search time setting 1 Search time = (setting value + 1) x (Search time resolution) (Note) Define search time for ANT1 or ANT2 until first Bit-Synchronization detection.

[Description]

1. For details, please refer to the “Diversity function”.

0x4A[2DIV_SEARCH2]

Function: Antenna diversity search time setting
Address: 0x4A (BANK1)
Reset value:0x0E

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	SEARCH_TIME2[6:0]	000_1110	R/W	Antenna diversity search time setting 2 Search time = setting value x Search time resolution (Note) After Bit-Synchronization detection, define search time for another ANT different from the one used in the last search.

[Description]

1. For details, please refer to the “Diversity function”.

0x4B[2DIV_FAST_LVL]

Function: ED threshold level setting during Antenna diversity FAST mode
Address: 0x4B (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	2DIV_FAST_LVL[7:0]	0000_0000	R/W	Antenna diversity FAST mode ED threshold level

0x4C[Reserved]

Function: Reserved
Address: 0x4C (BANK1)
Reset value:0x06

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0110	R/W	Reserved

0x4D[VCO_CAL_MIN_I]

Function: VCO calibration low limit frequency setting (I counter)
Address: 0x4D (BANK1)
Reset value:0x19

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	VCO_CAL_MIN_I[5:0]	01_1001	R/W	VCO calibration low limit frequency setting - I counter

[Description]

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”.
2. For frequency setting method, please refer to the “VCO lower limit frequency setting”.

(Note)

1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x4E[VCO_CAL_MIN_FH]

Function: VCO calibration low limit frequency setting (F counter high 4bits)
Address: 0x4E (BANK1)
Reset value:0x09

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3:0	VCO_CAL_MIN_F[19:16]	1001	R/W	VCO calibration low limit frequency setting - F counter high 4bits

[Description]

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”.
2. For frequency setting method, please refer to the “VCO lower limit frequency setting”.

(Note)

1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x4F[VCO_CAL_MIN_FM]

Function: VCO calibration low limit frequency setting (F counter middle byte)
Address: 0x4F (BANK1)
Reset value:0x05

Bit	Bit name	Reset value	R/W	Description
7:0	VCO_CAL_MIN_F[15:8]	0000_0101	R/W	VCO calibration low limit frequency setting - F counter middle byte

[Description]

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”.
2. For frequency setting method, please refer to the “VCO lower limit frequency setting”.

(Note)

1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x50[VCO_CAL_MIN_FL]

Function: VCO calibration low limit frequency setting (F counter low byte)
Address: 0x50 (BANK1)
Reset value:0xB0

Bit	Bit name	Reset value	R/W	Description
7:0	VCO_CAL_MIN_F[7:0]	1011_0000	R/W	VCO calibration low limit frequency setting - F counter low byte)

[Description]

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”.
2. For frequency setting method, please refer to the “VCO lower limit frequency setting”.

(Note)

1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x51[VCO_CAL_MAX_N]

Function: VCO calibration upper limit frequency setting
Address: 0x51 (BANK1)
Reset value:0x05

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3:0	VCO_CAL_MAX_N[3:0]	0101	R/W	VCO calibration upper frequency limit range setting (ΔF from low limit frequency) 0000: 0MHz 0001: 1.125MHz 0010: 2.25 MHz 0011: 4.5 MHz 0100: 9 MHz 0101: 18 MHz 0110: 36 MHz 0111: 72 MHz Other setting: prohibited

[Description]

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”.
2. For frequency setting method, please refer to the “VCO upper limit frequency setting”.

(Note)

1. For upper limit frequency, please set the frequency range that includes the frequency used.

0x52[VCAL_MIN]

Function: VCO calibration low limit value indication and setting
Address: 0x52 (BANK1)
Reset value:0x40

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	VCAL_MIN[6:0]	100_0000	R/W	VCO calibration low limit value (Note) after calibration by [VCO_CAL_START: B0 0x6F], value will be saved automatically.

[Description]

1. For details usage of VCO calibration, please refer to the “VCO adjustment”.

0x53[VCAL_MAX]

Function: VCO calibration upper limit value indication and setting
Address: 0x53 (BANK1)
Reset value:0x40

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	VCAL_MAX[6:0]	100_0000	R/W	VCO calibration upper limit value (Note) after calibration by [VCO_CAL_START: B0 0x6F], value will be saved automatically.

[Description]

1. For details usage of VCO calibration, please refer to the “VCO adjustment”.

0x54-0x55[Reserved]

Function: Reserved
Address: 0x54-0x55 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x56[DEMOD_SET0]

Function: Demodulator configuration 0
Address: 0x56 (BANK1)
Reset value: 0x50

Bit	Bit name	Reset value	R/W	Description
7	CHFIL_WIDE_SYNC	0	R/W	Channel Filter Wideband setting before sychronization 0: Channel filter band width are set with CHFIL_BW_ADJ([CHFIL_BW: B0 0x54(6-0)]) always 1: Channel filter band width are double width set with CHFIL_BW_ADJ before synchronization. After synchronized channel filter band width is set with CHFIL_BW_ADJ
6	IQ_INV	1	R/W	IQ invert function 0: Do not invert 1: Invert
5	Reserved	0	R	Reserved
4	STR_LIM_ON	1	R/W	Symbol timing recovery limiter setting 0: Turn off the limiter 1: Turn on the limiter
3	STR_HOLD_ON	0	R/W	Symbol timing recovery setting 0: Constantly track symbol timing 1: Keep symbol timing after SFD detection
2	AFC_LIM_OFF	0	R/W	AFC limiter setting 0: Turn on the AFC limiter 1: Turn off the AFC limiter
1	AFC_HOLD_ON	0	R/W	AFC mode setting 0: Constantly perform AFC 1: Turn off AFC after SFD detection
0	AFC_OFF_EN	0	R/W	AFC OFF enable setting 0: enable (perform AFC) 1: disable (not perform AFC)

0x57[DEMOD_SET1]

Function: Demodulator configuration 1
Address: 0x57 (BANK1)
Reset value: 0x04

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:4	DEM_FIL2[1:0]	00	R/W	Demodulator filter setting 2 00: No averaging 01: 2 times average 10: 4 times average 11: 8 times average
3	Reserved	0	R	Reserved
2:0	DEM_FIL[2:0]	0100	R/W	Demodulator filter bandwidth setting 000: Master clock frequency/8×(1/120) 001: Master clock frequency/8×(1/100) 010: Master clock frequency/8×(7/600) 011: Master clock frequency/8×(1/75) 100: Master clock frequency/8×(3/200) 101: Master clock frequency/8×(1/60) 110: Master clock frequency/8×(1/30) 111: Master clock frequency/8×(1/30)

(Note)
1. Please use the value specified in the “Initialization table”.

0x58[DEMOD_SET2]

Function: Demodulator configuration 2
Address: 0x58 (BANK1)
Reset value: 0x01

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	DEM_GAIN[2:0]	001	R/W	Demodulator gain setting Gain = (Setting value+1)/2

(Note)
1. Please use the value specified in the “Initialization table”.

0x59[DEMOD_SET3]

Function: Demodulator configuration 3
Address: 0x59 (BANK1)
Reset value: 0x10

Bit	Bit name	Reset value	R/W	Description
7:0	DEM_4FSK_TH[7:0]	0001_0000	R/W	4FSK threshold level setting

(Note)
1. Please use the value specified in the “Initialization table”.

0x5A-0x5B[Reserved]

Function: Reserved
Address: 0x5A-0x5B (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

0x5C[DEMOD_SET6]

Function: Demodulator configulation 6
Address: 0x5C (BANK1)
Reset value:0x18

Bit	Bit name	Reset value	R/W	Description
7:0	RXDEV_RANGE[7:0]	0001_1000	R/W	RX frequency deviation range setting setting value = RX frequency deviation range[Hz] * 512 / {Master clock frequency[Hz] / 8 / CHFIL_BW_ADJ([CHFIL_BW: B0 0x54(6-0)])}

(Note)
1. The value specified in “Initialization table” is recommended.

0x5D[DEMOD_SET7]

Function: Demodulator configulation 7
Address: 0x5D (BANK1)
Reset value:0x0B

Bit	Bit name	Reset value	R/W	Description
7:0	AFC_LIM[7:0]	0000_1011	R/W	AFC tacking range setting setting value = RX frequency deviation range[Hz] * 1024 / {Master clock frequency[Hz] / 8 / CHFIL_BW_ADJ([CHFIL_BW: B0 0x54(6-0)])} * Demodulator gain (DEM_GAIN([DEMOD_SET: B1 0x58(2-0)])) (Note) This setting is valid when AFC_LIM_OFF(DEMOD_SET0: B1 0x56(2)) = 0b0.

(Note)
1. The value specified in “Initialization table” is recommended.

0x5E[DEMOD_SET8]

Function: Demodulator configuration 8
Address: 0x5E (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	PLL_AFC_SHIFT[2:0]	000	R/W	PLL-AFC magnification adjustment 1

(Note)
1. Please use the value specified in the “Initialization table”.

0x5F[DEMOD_SET9]

Function: Demodulator configulation 9
Address: 0x5F (BANK1)
Reset value:0x07

Bit	Bit name	Reset value	R/W	Description
7:0	PLL_AFC_CO[7:0]	0000_0111	R/W	PLL-AFC magnification adjustment 2

(Note)
1. Please use the value specified in the “Initialization table”.

0x60[DEMOD_SET10]

Function: Demodulator configulation 10
Address: 0x60 (BANK1)
Reset value:0x0C

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4:0	STR_PB_LEN[4:0]	0_1100	R/W	Demodulator preamble detection threshold value setting

(Note)
1. Please use the value specified in the “Initialization table”.

0x61[DEMOD_SET11]

Function: Demodulator configulation 11
Address: 0x61 (BANK1)
Reset value:0x08

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4:0	STR_PB_LEN_DIV[4:0]	0_1000	R/W	Demodulator preamble detection threshold value setting (during diversity)

(Note)
1. Please use the value specified in the “Initialization table”.

0x62[ADDR_CHK_CTR_H]

Function: Address check counter indication (high 3bits)
Address: 0x62 (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	ADDR_CHK_CTR[10:8]	000	R	Indicating the number of packets mismatch during Field checking (high 3bits) (Note) Combined with 8bits of the [ADDR_CHK_CTR_L:B1 0x63] register. (Note) Max. count is 2047. Count value can be cleared by STATE_CLR4([STATE_CLR: B0 0x16(4)]).

[Description]
1. For details, please refer to the “Field checking function”.

0x63[ADDR_CHK_CTR_L]

Function: Address check counter indication (low byte)
Address: 0x63 (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	ADDR_CHK_CTR[7:0]	0000_0000	R	Indicating the number of packets mismatch during Field checking (low byte) For details, please refer to “[ADDR_CHK_CTR_H:B1 0x62]” register.

[Description]
1. For details, please refer to the “Field checking function”.

0x64[WHT_INIT_H]

Function: Whiteing initialized state setting (high 1bit)
Address: 0x64 (BANK1)
Reset value:0x01

Bit	Bit name	Reset value	R/W	Description
7:1	Reserved	000_0000	R	Reserved
0	WHT_INIT[8]	1	R/W	Whiteing initialized state setting (high 1bit)

[Description]

1. For details, please refer to the “Data Whitening function”.

0x65[WHT_INIT_L]

Function: Whiteing initialized state setting (low byte)
Address: 0x65 (BANK1)
Reset value:0xFF

Bit	Bit name	Reset value	R/W	Description
7:0	WHT_INIT[7:0]	1111_1111	R/W	Whiteing initialized state setting (low byte)

[Description]

1. For details, please refer to the “Data Whitening function”.

0x66[WHT_CFG]

Function: Whiteing polynomial setting
Address: 0x66 (BANK1)
Reset value:0x08

Bit	Bit name	Reset value	R/W	Description
7:0	WHT_CFG[7:0]	0000_1000	R/W	Whiteing polynomial setting

[Description]

1. For details, please refer to the “Data Whitening function”.

0x67-0x7A[Reserved]

Function: Reserved
Address: 0x67-0x7A (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x7B[TX_RATE2_EN]

Function: TX data rate setting 2 enable
Address: 0x7B (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:1	Reserved	000_0000	R	Reserved
0	TX_RATE2_EN	0	R/W	TX data rate conversion setting 2 enable 0: disable 1: enable (Note) When this is set to 0b1, TX data rate conversion setting of [TX_RATE2_H/L: B1 0x7C/7D] is enabled.

0x7C[TX_RATE2_H]

Function: TX data rate conversion setting 2 (high byte)
Address: 0x7C (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TX_RATE2[15:8]	0000_0000	R/W	TX data rate conversion setting 2 (high byte) (Note) Combined with 8bits of the [TX_RATE2_L: B1 0x7D] register, this is calculated using a total of 14bits. (Note) Valid only for TX_RATE2_EN([TX_RATE2_EN: B1 0x7B(0)]) = 0b1. For data rate setting by [TX_RATE_H/L: B1 0x02/03], set a value calculated by the following formula to adjust data rate deviation, if it is larger. Setting value = round [[{1 / Data rate (bps)} – {1 / (Master clock frequency(Hz) / TX_RATE[13:0]) × 9}] / {1 / Master clock frequency (Hz)}] (Note) For details, please refer to the “Data rate setting function”.

0x7D[TX_RATE2_L]

Function: TX data rate conversion setting 2 (low byte)
Address: 0x7D (BANK1)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	TX_RATE2[7:0]	0000_0000	R/W	TX data rate conversion setting 2 (low byte) (Note) For details, please refer to [TX_RATE2_H: B1 0x7C] register.

0x7E[Reserved]

Function: Reserved
Address: 0x7E (BANK1)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x7F[ID_CODE]

Function: ID code indication
Address: 0x7F (BANK1)
Reset value:0x65

Bit	Bit name	Reset value	R/W	Description
7:0	ID[7:0]	0110_0101	R/W	ID code

●Register Bank2

0x00[BANK_SEL]

[Description]
Refer to [BANK_SEL:B0 0x00]

0x01-0x3F[Reserved]

Function: Reserved
Address: 0x01-0x3F (BANK2)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x40[VTUNE_COMP_ON]

Function: VCO adjustment voltage comparison result display enable
Address:0x40(BANK2)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Drescription
7:6	Reserved	00	R/W	Reserved
5	VTUNE_COMP_ON	0	R/W	VCO adjustment voltage comparison result display enable 0: disable 1: enable
4:0	Reserved	0_0000	R/W	Reserved

[Description]

1. For details of VCO adjustment voltage comparison result, please refer to the “VCO Adjustment”.

0x41-0x75[Reserved]

Function: Reserved
Address: 0x41-0x75 (BANK2)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x76[GAIN_HHTOH]

Function: Threshold level setting for switching “double high gain” to “high gain”
Address:0x76(BANK2)
Reset value:0x8E

Bit	Bit name	Reset value	R/W	Drescription
7:0	GCTRIM_HHTOH[7:0]	1000_1110	R/W	Gain switching threshold (double high gain to high gain)

[Description]

2. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.
2. This register value and [GAIN_HTOHH] value have to be [GAIN_HHTOH] > [GAIN_HTOHH].

0x77[GAIN_HTOHH]

Function: Threshold level setting for switching “high gain” to “double high gain”
Address:0x77(BANK2)
Reset value:0x32

Bit	Bit name	Reset value	R/W	Drescription
7:0	GCTRIM_HTOHH[7:0]	0011_0010	R/W	Gain switching threshold (high gain to double high gain)

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.
2. This register value and [GAIN_HHTOH] value have to be [GAIN_HHTOH] > [GAIN_HTOHH].

0x78[GAIN_HTOM]

Function: Threshold level setting for switching “high gain” to “middle gain”
Address:0x78(BANK2)
Reset value:0x8E

Bit	Bit name	Reset value	R/W	Drescription
7:0	GCTRIM_HTOM[7:0]	1000_1110	R/W	Gain switching threshold (high gain to middle gain)

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.
2. This register value and [GAIN_MTOH] value have to be [GAIN_HTOM] > [GAIN_MTOH].

0x79[GAIN_MTOH]

Function: Threshold level setting for switching “middle gain” to “high gain”
Address:0x79(BANK2)
Reset value:0x32

Bit	Bit name	Reset value	R/W	Drescription
7:0	GCTRIM_MTOH[7:0]	0011_0010	R/W	Gain switching threshold (middle gain to high gain)

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.
2. This register value and [GAIN_HTOM] value have to be [GAIN_HTOM] > [GAIN_MTOH].

0x7A[GAIN_MTOL]

Function: Threshold level setting for switching “middle gain” to “low gain”
Address:0x7A (BANK2)
Reset value:0x8E

Bit	Bit name	Reset value	R/W	Drescription
7:0	GCTRIM_MTOL[7:0]	1000_1110	R/W	Gain switching threshold (middle gain to low gain)

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.
2. This register value and [GAIN_LTOM] value have to be [GAIN_MTOL] > [GAIN_LTOM].

0x7B[GAIN_LTOM]

Function: Threshold level setting for switching “low gain” to “middle gain”
Address:0x7B (BANK2)
Reset value:0x32

Bit	Bit name	Reset value	R/W	Drescription
7:0	GCTRIM_LTOM[7:0]	0011_0010	R/W	Gain switching threshold (low gain to middle gain)

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.
2. This register value and [GAIN_MTOL] value have to be [GAIN_MTOL] > [GAIN_LTOM].

0x7C[RSSI_ADJ_H]

Function: RSSI offset value setting during high gain operation
Address:0x7C (BANK2)
Reset value:0x22

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R/W	Reserved
6:0	RSSI_ADJ H[6:0]	010_0010	R/W	RSSI offset value during high gain operation

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.

0x7D[RSSI_ADJ_M]

Function: RSSI offset value setting during middle gain operation
Address:0x7D (BANK2)
Reset value:0x47

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R/W	Reserved
6:0	RSSI_ADJ M[6:0]	100_0111	R/W	RSSI offset value during middle gain operation

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.

0x7E[RSSI_ADJ_L]

Function: RSSI offset value setting during low gain operation
Address:0x7E (BANK2)
Reset value:0x6E

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R/W	Reserved
6:0	RSSI_ADJ L[6:0]	110_1110	R/W	RSSI offset value during low gain operation

[Description]

1. For details operation of RSSI adjustment using this register, please refer to the “Energy Detection Value(ED value) Adjustment”.

(Note)

1. Please use the value specified in the “Initialization table”.

0x7F[Reserved]

Function:Reserved
Address: 0x7F (BANK2)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

●Register Bank3

0x00[BANK_SEL]

[Description]
Refer to [BANK_SEL:B0 0x00]

0x01-0x22[Reserved]

Function:Reserved
Address:0x01-0x22 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x23[2MODE_DET]

Function: 2 modes detection setting (MODE-T and MODE-C)
Address:0x23 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	description
7:1	Reserved	0000_000	R	Reserved
0	2MODE_DET_EN	0	R/W	Receiving mode setting 0: receiving Mode-C only 1: receiveing both Mode-T and Mode –C (Note) mode chang is inhibited in the RX_ON state. Please change in the TRX_OFF state.

0x24-0x40[Reserved]

Function:Reserved
Address:0x24-0x40 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x41[RAMP_CTRL1]

Function: PA ramp control setting 1
Address:0x41 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	description
7:3	Reserved	0_0000	R	Reserved
2	RAMP_CLK_STEP	0	R/W	Ramp control standard clock cycle setting 0: Master clock cycle * 2 (18MHz) 1: Master clock cycle * 32 (18MHz / divided by 16)
1:0	RAMP_INC [1:0]	00	R/W	Ramp control counter increment setting 00: 1 01: 2 10: 4 11: 8 (Note) In 9-bit counter (0 to 511), ramp-up/down time is controlled by changing the increment or decrement count according to the setting count.

[Description]

1. Refer to “Ramp control function” for details.
2. Set values specified by “Initialization table,” and do not change the setting for adjustment.

0x42[RAMP_CTRL2]

Function: PA ramp control setting 2
Address:0x42 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	description
7	Reserved	0	R	Reserved
6:0	RAMP_CLK_SET_R [6:0]	000_0001	R/W	Ramp-up time setting Ramp-up time = Ramp control standard clock cycle (RAMP_CLK_STEP[RAMP_CTRL1: B3 0x41(2)]) * setting value * [PA_REG_ADJ_H/L: B0 0x67/68] / Ramp control increment setting (RAMP_INC[RAMP_CTRL1: B3 0x41(1-0)])

[Description]

1. Refer to “Ramp control function” for details.
2. Set values specified by “Initialization table,” and do not change the setting for adjustment.

0x43[RAMP_CTRL3]

Function: PA ramp control setting 3
Address:0x43 (BANK3)
Reset value:0x01

Bit	Bit name	Reset value	R/W	description
7	Reserved	0	R	Reserved
6:0	RAMP_CLK_SET_F[6:0]	000_0001	R/W	Ramp-down time setting Ramp-down time = Ramp control standard clock cycle (RAMP_CLK_STEP[RAMP_CTRL1: B3 0x41(2)]) * setting value * [PA_REG_ADJ_H/L: B0 0x67/68] / Ramp control increment setting (RAMP_INC[RAMP_CTRL1: B3 0x41(1-0)])

[Description]

1. Refer to “Ramp control function” for details.
2. Set values specified by “Initialization table,” and do not change the setting for adjustment.

0x44-0x4F[Reserved]

Function:Reserved
Address:0x44-0x4F (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x50[EXT_WU_CTRL]

Function: External wake-up control setting
Address:0x50 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	description
7:2	Reserved	00_0000	R	Reserved
1	INT_CLR_WU_EN	0	R/W	Interrupt clear setting at wake-up 0: disable 1: enable
0	EXT_WU_EN	0	R/W	External wake-up enable 0: disable 1: enable (Note) In case of 0b1 setting, rising edge in signals input from GPIO1 pin is detected to change (wake-up) the state from SLEEP to IDLE. Wake-up operation is performed once for the setting value of [EXT_WU_INTERVAL: B3 0x51].

0x51[EXT_WU_INTERVAL]

Function: External wake-up control setting
Address:0x51 (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	description
7:0	EXT_WU_INTERVAL [7:0]	0000_0000	R/W	External wake-up interval setting (Note) In case of EXT_WU_EN([EXT_WU_CTRL: B3 0x50(0)])=0b1, wake-up is performed once for the setting value.

0x52-0x7F[Reserved]

Function:Reserved
Address:0x52-0x7F (BANK3)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

●Register BANK6

0x00[BANK_SEL]

[Description]
Refer to [BANK_SEL:B0 0x00]

0x01[MOD_CTRL]

Function : Modulation setting
Address : 0x01 (BANK6)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R	Reserved
1:0	MOD_TYPE[1:0]	01	R/W	Modulation Method setting 00: FSK 01: BPSK Others: reserved

[Description]
1. For details, please refer to the “Modulation setting”.

0x02-0x7A[Reserved]

Function : Reserved
Address : 0x02-0x7A (BANK6)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

0x7B[BPSK_PLL_CTRL]

Function : BPSK mode setting
Address : 0x7B (BANK6)
Reset value : 0x02

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R	Reserved
1	BPSK_P_CLKSEL	1	R/W	Frequency deviation time calculation clock selection in BPSK PLL control 0: 450kHz 1: 4MHz
0	BPSK_PLL_CTRL	0	R/W	BPSK mode selection setting 0: selector system 1: frequency control system

0x7C[BPSK_P_START_H]

Function : Frequency deviation start time setting in BPSK frequency control (high 3 bits)
Address : 0x7C (BANK6)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	BPSK_P_START[10:8]	000	R/W	Frequency deviation start time in BPSK frequency control (high 3 bits)

0x7D[BPSK_P_START_L]

Function : Frequency deviation start time setting in BPSK frequency control (low byte)
Address : 0x7D (BANK6)
Reset value : 0x05

Bit	Bit name	Reset value	R/W	Description
7:0	BPSK_P_START[7:0]	0000_0101	R/W	Frequency deviation start time in BPSK frequency control (low byte)

0x7E[BPSK_P_HOLD_H]

Function : Frequency deviation hold time setting in BPSK frequency control (high 4 bits)
Address : 0x7E (BANK6)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3:0	BPSK_P_HOLD[11:8]	0000	R/W	Frequency deviation hold time in BPSK frequency control (high 4 bits)

0x7F[BPSK_P_HOLD_L]

Function : Frequency deviation hold time setting in BPSK frequency control (low byte)
Address : 0x7F (BANK6)
Reset value : 0x02

Bit	Bit name	Reset value	R/W	Description
7:0	BPSK_P_HOLD[7:0]	0000_0010	R/W	Frequency deviation hold time in BPSK frequency control (low byte)

●Register BANK7

0x00[BANK_SEL]

[Description]
Refer to [BANK_SEL:B0 0x00]

0x01[DSSS_CTRL]

Function : DSSS control setting
Address : 0x01 (BANK7)
Reset value : 0x07

Bit	Bit name	Reset value	R/W	Description
7	SF_OFF	0	R/W	Spread OFF setting 0: spread ON 1: spread OFF
6	Reserved	0	R	Reserved
5:4	PSDU_SIZE[1:0]	00	R/W	PSDU size setting in DSSS 00: 16byte 01: 24byte 10: 32byte 11: arbitrary PSDU length (Note) In case of 0b11 setting, set the packet length according to the packet format set in PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]). FEC function properly works only when one of 16/24/32 bytes is set. Thus, in case of 0b11 setting, be sure to set FEC function to disable. FEC function disable setting is as follows. FEC_EN([DSSS_CTRL: B7 0x01(2)])=0b0 INTLV_EN([FEC_ENC_CTRL: B7 0x03(0)])=0b0 DEINTLV_EN([FEC_DEC_CTRL: B7 0x05(0)])=0b0
3	Reserved	0	R	Reserved
2	DIFF_ENC_EN	1	R/W	Differential coding enable setting 0: disable 1: enable
1	FEC_EN	1	R/W	FEC enable control 0: disable 1: enable (Note) When FEC_EN=0b1, FEC coding processing is not performed normally if AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)]) or FAST_TX_EN([RF_STATUS_CTRL: B0 0x0A(5)]) are set to be 0b1. In addition, coding processing time is about 350 us after FIFO write completion. Please execute TX_ON by TX_ON command after coding processing.
0	DSSS_EN	1	R/W	DSSS enable control 0: disable 1: enable

[Description]
1. For details, please refer to the “Spread Spectrum Function”.

0x02[DSSS_MODE]

Function : DSSS mode setting
Address : 0x02 (BANK7)
Reset value : 0x65

Bit	Bit name	Reset value	R/W	Description
7:6	FEC_CLK_SEL	01	R/W	Decoder operation clock setting in FEC decoding 00: 4MHz 01: 2MHz 10: 1MHz 11: 0.5MHz
5:4	Reserved	10	R/W	Reserved
3:2	DSSS_LC_RCV[1:0]	01	R/W	DSSS demodulating circuit clock setting (during receiving data) (The operation clock frequency of the demodulating circuit is switched.) 00: master clock frequency 01: master clock frequency * 1/2 10: master clock frequency * 1/4 Others: master clock frequency
1:0	DSSS_LC_SYNC[1:0]	01	R/W	DSSS demodulating circuit clock setting (during synchronization) (The operation clock frequency of the demodulating circuit is switched.) 00: master clock frequency 01: master clock frequency * 1/2 10: master clock frequency * 1/4 Others: master clock frequency

0x03[FEC_ENC_CTRL]

Function : FEC encoder setting
Address : 0x03 (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:5	Reserved	000	R	Reserved
4	INTLV_BYTE_MSB	00	R/W	Interleave byte transmission order control 0: MSB first 1: LSB first
3	ENC_BIT_MSB	0	R/W	FEC encoder bit transmission order control 0: LSB first 1: MSB first
2	ENC_BYTE_MSB	0	R/W	FEC encoder byte transmission order control 0: LSB first 1: MSB first
1	ENC_INIT_SEL	0	R/W	FEC encoder initilal configuration select control 0: Initial configuration follows ALL 0 1: Initial configuration follows the last PSDUvalue of transimittion (Note) In case of 0b0 the last data(1 byte) of input data is changed to 8'h00
0	INTLV_EN	1	R/W	Interleave enable control 0: disable 1: enable (Note) Set 0b0 in case of PSDU_SIZE([DSSS_CTRL: B7 0x01(5-4)])=0b11.

[Description]

1. For details, please refer to the "Spread Spectrum Function".

0x04[Reserved]

Function : Reserved
Address : 0x04 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

0x05[FEC_DEC_CTRL]

Function : FEC decoder setting
Address : 0x05 (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5	FEC_CRC_AREA_SEL	0	R/W	CRC calculation range when FEC reception 0: Data-field (this is usual range) 1: 1st byte of Data-field to (Length value - 1 - CRC length) (Note) Final data (1 byte) is transposed to 8'h00 when ENC_INIT_SEL=0b0. Therefore, a CRC calculation range can be changed into the range except final data when FEC_CRC_AREA_SEL=0b1.
4	DEINTLV_BYTE_MSB	0	R/W	Deinterleave data output order control 0: MSB first 1: LSB first
3	DEC_BIT_MSB	0	R/W	FEC decoder deta input order control 0: LSB first 1:MSB first
2	DEC_BYTE_MSB	0	R/W	FEC decoder data output order control 0: LSB first 1: MSB first
1	DEC_INIT_SEL	0	R/W	FEC decoder decoding select control 0: decode with consideration of termination 1: decode without consideration of termination
0	DEINTLV_EN	1	R/W	Deinterleave enable control 0: disable 1: enable (Note) Set 0b0 in case of PSDU_SIZE([DSSS_CTRL: B7 0x01(5-4)])=0b11

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x06[SF_CTRL]

Function : Spreading factor setting
Address : 0x06 (BANK7)
Reset value : 0x22

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:4	PSDU_SF[1:0]	10	R/W	PSDU spreading factor setting 00: 16 01: 32 10: 64 11: 8
3:2	Reserved	00	R	Reserved
1:0	SHR_SF[1:0]	10	R/W	SHR spreading factor setting 00: 16 01: 32 10: 64 11: 8

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

[Note]

1. When the spread factor (SF)=8 is used, receiving data may fail due to poor frequency estimation accuracy even if the reception level is high. Immediately before using SF=8, be sure to receive data using another SF (16/32/64) and confirm the frequency gap between transmitter and receiver. Packets will be successfully received with SF=8 by correcting the frequency gap.

0x07[SHR_GOLD_SEED3]

Function : SHR Gold code seed setting 3
Address : 0x07 (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:1	Reserved	000_0000	R	Reserved
0	SHR_GOLD_SEED[24]	1	R/W	SHR Gold code seed setting 3

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x08[SHR_GOLD_SEED2]

Function : SHR Gold code seed setting 2
Address : 0x08 (BANK7)
Reset value : 0x6E

Bit	Bit name	Reset value	R/W	Description
7:0	SHR_GOLD_SEED [23:16]	0110_1110	R/W	SHR Gold code seed setting 2

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x09[SHR_GOLD_SEED1]

Function : SHR Gold code seed setting 1
Address : 0x09 (BANK7)
Reset value : 0xCD

Bit	Bit name	Reset value	R/W	Description
7:0	SHR_GOLD_SEED [15:8]	1100_1101	R/W	SHR Gold code seed setting 1

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x0A[SHR_GOLD_SEED0]

Function : SHR Gold code seed setting 0
Address : 0x0A (BANK7)
Reset value : 0x5F

Bit	Bit name	Reset value	R/W	Description
7:0	SHR_GOLD_SEED [7:0]	0101_1111	R/W	SHR Gold code seed setting 0

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x0B[PSDU_GOLD_SEED3]

Function : PSDU Gold code seed setting 3
Address : 0x0B (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:1	Reserved	000_0000	R	Reserved
0	PSDU_GOLD_SEED[24]	1	R/W	PSDU Gold code seed setting 3

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x0C[PSDU_GOLD_SEED2]

Function : PSDU Gold code seed setting 2
Address : 0x0C (BANK7)
Reset value : 0x6E

Bit	Bit name	Reset value	R/W	Description
7:0	PSDU_GOLD_SEED [23:16]	0110_1110	R/W	PSDU Gold code seed setting 2

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x0D[PSDU_GOLD_SEED1]

Function : PSDU Gold code seed setting 1
Address : 0x0D (BANK7)
Reset value : 0xCD

Bit	Bit name	Reset value	R/W	Description
7:0	PSDU_GOLD_SEED [15:8]	1100_1101	R/W	PSDU Gold code seed setting 1

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x0E[PSDU_GOLD_SEED0]

Function : PSDU Gold code seed setting setting 0
Address : 0x0E (BANK7)
Reset value : 0x5F

Bit	Bit name	Reset value	R/W	Description
7:0	PSDU_GOLD_SEED [7:0]	0101_1111	R/W	PSDU Gold code seed setting 0

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x0F[DSSS_PREAMBLE3]

Function : DSSS preamble pattern setting 3
Address : 0x0F (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	DSSS_PREAMBLE [31:24]	0000_0000	R/W	DSSS preamble pattern setting 3

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x10[DSSS_PREAMBLE2]

Function : DSSS preamble pattern setting 2
Address : 0x10 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	DSSS_PREAMBLE [23:16]	0000_0000	R/W	DSSS preamble pattern setting 2

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x11[DSSS_PREAMBLE1]

Function : DSSS preamble pattern setting 1
Address : 0x11 (BANK7)
Reset value : 0x3F

Bit	Bit name	Reset value	R/W	Description
7:0	DSSS_PREAMBLE [15:8]	0011_1111	R/W	DSSS preamble pattern setting 1

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x12[DSSS_PREAMBLE0]

Function : DSSS preamble pattern setting 0
Address : 0x12 (BANK7)
Reset value : 0x59

Bit	Bit name	Reset value	R/W	Description
7:0	DSSS_PREAMBLE [7:0]	0101_1001	R/W	DSSS preamble pattern setting 0

[Description]

1. For details, please refer to the “Spread Spectrum Function”.

0x13[SS_DOWN_SIZE]

Function : DSSS downsampling setting
Address : 0x13 (BANK7)
Reset value : 0x24

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	SS_DOWN_SIZE[6:0]	010_0100	R/W	DSSS downsampling setting Downsampling setting value = {Master clock frequency [Hz] / [CHFIL_BW: B0 0x54] / 5} / Chip rate [cps]

0x14[SS_AFC_RANGE_SYNC]

Function : DSSS AFC range setting (during synchronization)
Address : 0x14 (BANK7)
Reset value : 0x05

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	SS_AFC_RANGE_SYNC [6:0]	000_0101	R/W	DSSS AFC range setting (during synchronization)

0x15[SS_AFC_RANGE]

Function : DSSS AFC range setting (during receiving data)
Address : 0x15 (BANK7)
Reset value : 0x05

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6:0	SS_AFC_RANGE[6:0]	000_0101	R/W	DSSS AFC range setting (during receiving data)

0x16[Reserved]

Function : Reserved
Address : 0x16 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x17[DSSS_RATE_SYNC_H]

Function : DSSS receive chip rate setting (high byte) during synchronization
Address : 0x17 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3:0	DSSS_RATE_SYNC [11:8]	0000	R/W	DSSS chip rate setting (high byte) during synchronization Setting value = round(DSSS demodulating circuit operation clock frequency/Chip rate) (Note) DSSS demodulating circuit operation clock frequency is determined by DSSS_LC_SYNC([DSSS_MODE: B7 0x02(1-0)]).

0x18[DSSS_RATE_SYNC_L]

Function : DSSS receive chip rate setting (low byte) during synchronization
Address : 0x18 (BANK7)
Reset value : 0x59

Bit	Bit name	Reset value	R/W	Description
7:0	DSSS_RATE_SYNC[7:0]	0101_1001	R/W	DSSS chip rate setting (low byte) during synchronization (Note) Refer to [DSSS_RATE_H: B7 0x1A] register for details.

0x19[DSSS_RATE_H]

Function : DSSS receive chip rate setting (High byte) during receiving data
Address : 0x19 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0000	R	Reserved
3:0	DSSS_RATE[11:8]	0000	R/W	DSSS receive chip rate setting (high byte) during receiving data Setting value = round(DSSS demodulating circuit operation clock frequency/Chip rate) (Note) DSSS demodulating circuit operation clock frequency is determined by DSSS_LC_RCV([DSSS_MODE: B7 0x02(3-2)]).

0x1A[DSSS_RATE_L]

Function : DSSS receive chip rate setting (low byte) during receiving data
Address : 0x1A (BANK7)
Reset value : 0x59

Bit	Bit name	Reset value	R/W	Description
7:0	DSSS_RATE[7:0]	0101_1001	R/W	DSSS receive chip rate setting(low byte) during receiving data (Note) For details, please refer to [DSSS_RATE_H: B7 0x19] Register

0x1B[SS_SYNC_BIT8_GATE_H]

Function : Correlation threshold level in DSSS synchronization setting(high 3bits)
Address : 0x1B (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0_0000	R	Reserved
3:0	SS_SYNC_BIT8_GATE [10:8]	001	R/W	Correlation threshold level in DSSS synchronization setting(hig 3bits)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x1C[SS_SYNC_BIT8_GATE_L]

Function : Correlation threshold level in DSSS synchronization setting(low byte)
Address : 0x1C (BANK7)
Reset value : 0x13

Bit	Bit name	Reset value	R/W	Description
7:0	SS_SYNC_BIT8_GATE [7:0]	0001_0011	R/W	Correlation threshold level in DSSS synchronization setting(low byte)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x1D[SS_SYNC_BIT8_GATE2_H]

Function : Correlation threshold level in DSSS synchronization setting 2 (high 3bits)
Address : 0x1D (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:3	Reserved	0_0000	R	Reserved
2:0	SS_SYNC_BIT8_GATE2[10:8]	001	R/W	Correlation threshold level in DSSS synchronization setting 2 (high 3bits)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x1E[SS_SYNC_BIT8_GATE2_L]

Function : Correlation threshold level in DSSS synchronization setting 2 (low byte)
Address : 0x1E (BANK7)
Reset value : 0x23

Bit	Bit name	Reset value	R/W	Description
7:0	SS_SYNC_BIT8_GATE2[7:0]	0010_0011	R/W	Correlation threshold level in DSSS synchronization setting 2 (low byte)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x1F[SS_SYNC_BIT_GATE_H]

Function : Correlation threshold level after DSSS synchronization setting (high byte)
Address : 0x1F (BANK7)
Reset value : 0x01

Bit	Bit name	Reset value	R/W	Description
7:4	Reserved	0_0000	R	Reserved
3:0	SS_SYNC_BIT_GATE[10:8]	001	R/W	Correlation threshold level after DSSS synchronization setting (high byte)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x20[SS_SYNC_BIT_GATE_L]

Function : Correlation threshold level after DSSS synchronization setting (low byte)
Address : 0x20 (BANK7)
Reset value : 0x06

Bit	Bit name	Reset value	R/W	Description
7:0	SS_SYNC_BIT_GATE[7:0]	0000_0110	R/W	Correlation threshold level after DSSS synchronization setting (low byte)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x21-0x30[Reserved]

Function : Reserved
Address : 0x21-0x30 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R/W	Reserved

0x31[SS_AFC_OUT]

Function : DSSS AFC value indication
Address : 0x31 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SS_AFC_FIX[7:0]	0000_0000	R	DSSS AFC value indication (Note) This indicates the AFC value at SW detection.

0x32[SS_AFC_FIX_EN]

Function : DSSS AFC fixed enable setting
Address : 0x32 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:1	Reserved	000_0000	R	Reserved
0	SS_AFC_FIX_EN	0	R/W	DSSS AFC fixed enable 0: disable 1: enable

0x33[SS_AFC_FIX]

Function : DSSS AFC fixed setting
Address : 0x33 (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	SS_AFC_FIX[7:0]	0000_0000	R/W	DSSS AFC fixed setting

0x34-0x7F[Reserved]

Function : Reserved
Address : 0x34-0x7F (BANK7)
Reset value : 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

●Register BANK10

0x00[BANK_SEL]

[Description]
Refer to [BANK_SEL:B0 0x00]

0x01[BPSK_STEP_CTRL]

Function: BPSK step control setting
Address:0x01 (BANK10)
Reset value:0x30

Bit	Bit name	Reset value	R/W	Description
7	Reserved	0	R	Reserved
6	BPSK_CLK_SEL	0	R/W	Step control clock select setting 0: master clock frequency / 2 (18MHz) 1: master clock frequency / 4 (9MHz)
5	BPSK_STEP_SEL	1	R/W	Step control function select setting 0: Up-down separate setting 1: Up-down common setting
4	BPSK_STEP_EN	1	R/W	Step control enable 0: disable 1: enable
3:1	Reserved	000	R	Reserved
0	BPSK_CLK_SET[8]	0	R/W	Step control clock period setting (high 1 bit) Step control clock period = step control clock setting(BPSK_CLK_SEL) * Setting value

0x02[BPSK_STEP_CLK_SET]

Function: BPSK step control clock setting
Address:0x02 (BANK10)
Reset value:0x3F

Bit	Bit name	Reset value	R/W	Description
7:0	BPSK_SET_SET[7:0]	0000_0000	R/W	Step control clock period setting (low byte)

0x03[Reserved]

Function：Reserved
Address：0x03 (BANK10)
Reset value：0x00

Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

0x04[BPSK_STEP_SET0]

Function: BPSK step control setting 0
Address: 0x04 (BANK10)
Reset value: 0x20

Bit	Bit name	Reset value	R/W	Description
7:4	STEP1[3:0]	0010	R/W	BPSK step control1
3:0	STEP0[3:0]	0000	R/W	BPSK step control0

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV0_H/GFIL0: B1 0x32] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x05[BPSK_STEP_SET1]

Function: BPSK step control setting 1
Address: 0x05 (BANK10)
Reset value: 0x22

Bit	Bit name	Reset value	R/W	Description
7:4	STEP3[3:0]	0010	R/W	BPSK step control3
3:0	STEP2[3:0]	0010	R/W	BPSK step control2

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV0_L/GFIL1: B1 0x33] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x06[BPSK_STEP_SET2]

Function: BPSK step control setting 2
Address: 0x06 (BANK10)
Reset value: 0x22

Bit	Bit name	Reset value	R/W	Description
7:4	STEP5[3:0]	0010	R/W	BPSK step control5
3:0	STEP4[3:0]	0010	R/W	BPSK step control4

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV1_H/GFIL2: B1 0x34] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x07[BPSK_STEP_SET3]

Function: BPSK step control setting 3
Address: 0x07 (BANK10)
Reset value: 0x33

Bit	Bit name	Reset value	R/W	Description
7:4	STEP7[3:0]	0011	R/W	BPSK step control7
3:0	STEP6[3:0]	0011	R/W	BPSK step control6

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV1_L/GFIL3: B1 0x35] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x08[BPSK_STEP_SET4]

Function: BPSK step control setting 4
Address: 0x08 (BANK10)
Reset value: 0x22

Bit	Bit name	Reset value	R/W	Description
7:4	STEP9[3:0]	0010	R/W	BPSK step control9
3:0	STEP8[3:0]	0010	R/W	BPSK step control8

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV2_H/GFIL4: B1 0x36] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x09[BPSK_STEP_SET5]

Function: BPSK step control setting 5
Address: 0x09 (BANK10)
Reset value: 0x43

Bit	Bit name	Reset value	R/W	Description
7:4	STEP11[3:0]	0100	R/W	BPSK step control11
3:0	STEP10[3:0]	0011	R/W	BPSK step control10

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV2_L/GFIL5: B1 0x37] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x0A[BPSK_STEP_SET6]

Function: BPSK step control setting 6
Address: 0x0A (BANK10)
Reset value: 0x54

Bit	Bit name	Reset value	R/W	Description
7:4	STEP13[3:0]	0101	R/W	BPSK step control13
3:0	STEP12[3:0]	0100	R/W	BPSK step control12

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV3_H/GFIL6: B1 0x38] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x0B[BPSK_STEP_SET7]

Function: BPSK step control setting 7
Address: 0x0B (BANK10)
Reset value: 0x45

Bit	Bit name	Reset value	R/W	Description
7:4	STEP15[3:0]	0100	R/W	BPSK step control15
3:0	STEP14[3:0]	0101	R/W	BPSK step control14

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV3_L: B1 0x39] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x0C[BPSK_STEP_SET8]

Function: BPSK step control setting 8
Address: 0x0C (BANK10)
Reset value: 0x65

Bit	Bit name	Reset value	R/W	Description
7:4	STEP17[3:0]	0110	R/W	BPSK step control17
3:0	STEP16[3:0]	0101	R/W	BPSK step control16

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV4_H: B1 0x3A] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x0D[BPSK_STEP_SET9]

Function: BPSK step control setting 9
Address: 0x0D (BANK10)
Reset value: 0x76

Bit	Bit name	Reset value	R/W	Description
7:4	STEP19[3:0]	0111	R/W	BPSK step control19
3:0	STEP18[3:0]	0110	R/W	BPSK step control18

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_DEV4_L: B1 0x3B] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x0E[BPSK_STEP_SET10]

Function: BPSK step control setting 10
Address: 0x0E (BANK10)
Reset value: 0x87

Bit	Bit name	Reset value	R/W	Description
7:4	STEP21[3:0]	1000	R/W	BPSK step control21
3:0	STEP20[3:0]	0111	R/W	BPSK step control20

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_TIM_ADJ4: B1 0x3C] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x0F[BPSK_STEP_SET11]

Function: BPSK step control setting 11
Address: 0x0F (BANK10)
Reset value: 0x88

Bit	Bit name	Reset value	R/W	Description
7:4	STEP23[3:0]	1000	R/W	BPSK step control23
3:0	STEP22[3:0]	1000	R/W	BPSK step control22

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_TIM_ADJ3: B1 0x3D] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x10[BPSK_STEP_SET12]

Function: BPSK step control setting 12
Address: 0x10 (BANK10)
Reset value: 0x88

Bit	Bit name	Reset value	R/W	Description
7:4	STEP25[3:0]	1000	R/W	BPSK step control25
3:0	STEP24[3:0]	1000	R/W	BPSK step control24

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_TIM_ADJ2: B1 0x3E] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x11[BPSK_STEP_SET13]

Function: BPSK step control setting 13
Address: 0x11 (BANK10)
Reset value: 0x77

Bit	Bit name	Reset value	R/W	Description
7:4	STEP27[3:0]	0111	R/W	BPSK step control27
3:0	STEP26[3:0]	0111	R/W	BPSK step control26

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_TIM_ADJ1: B1 0x3F] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x12[BPSK_STEP_SET14]

Function: BPSK step control setting 14
Address: 0x12 (BANK10)
Reset value: 0x76

Bit	Bit name	Reset value	R/W	Description
7:4	STEP29[3:0]	0111	R/W	BPSK step control29
3:0	STEP28[3:0]	0110	R/W	BPSK step control28

[Description]
1. For details, please refer to the “BPSK Modulation”.
2. [FSK_TIM_ADJ0: B1 0x40] and this function are sharing a register. However, each register is a different function. Please set up a suitable value according to a use (Gaussian filter coefficient, FSK or BPSK step control).

0x13[BPSK_STEP_SET15]

Function: BPSK step control setting 15
Address: 0x13 (BANK10)
Reset value: 0x76

Bit	Bit name	Reset value	R/W	Description
7:4	STEP31[3:0]	0111	R/W	BPSK step control31
3:0	STEP30[3:0]	0110	R/W	BPSK step control30

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x14[BPSK_STEP_SET16]

Function: BPSK step control setting 16
Address: 0x14 (BANK10)
Reset value: 0x67

Bit	Bit name	Reset value	R/W	Description
7:4	STEP33[3:0]	0110	R/W	BPSK step control33
3:0	STEP32[3:0]	0111	R/W	BPSK step control32

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x15[BPSK_STEP_SET17]

Function: BPSK step control setting 17
Address: 0x15 (BANK10)
Reset value: 0xA8

Bit	Bit name	Reset value	R/W	Description
7:4	STEP35[3:0]	1010	R/W	BPSK step control35
3:0	STEP34[3:0]	1000	R/W	BPSK step control34

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x16[BPSK_STEP_SET18]

Function: BPSK step control setting 18
Address: 0x16 (BANK10)
Reset value: 0x8A

Bit	Bit name	Reset value	R/W	Description
7:4	STEP37[3:0]	1000	R/W	BPSK step control37
3:0	STEP36[3:0]	1010	R/W	BPSK step control36

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x17[BPSK_STEP_SET19]

Function: BPSK step control setting 19
Address: 0x17 (BANK10)
Reset value: 0x58

Bit	Bit name	Reset value	R/W	Description
7:4	STEP39[3:0]	0101	R/W	BPSK step control39
3:0	STEP38[3:0]	1000	R/W	BPSK step control38

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x18[BPSK_STEP_SET20]

Function: BPSK step control setting 20
Address: 0x18 (BANK10)
Reset value: 0x03

Bit	Bit name	Reset value	R/W	Description
7:4	STEP41[3:0]	0000	R/W	BPSK step control41
3:0	STEP40[3:0]	0011	R/W	BPSK step control40

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x19[BPSK_STEP_SET21]

Function: BPSK step control setting 21
Address: 0x19 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP43[3:0]	0000	R/W	BPSK step control43
3:0	STEP42[3:0]	0000	R/W	BPSK step control42

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x1A[BPSK_STEP_SET22]

Function: BPSK step control setting 22
Address: 0x1A (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP45[3:0]	0000	R/W	BPSK step control45
3:0	STEP44[3:0]	0000	R/W	BPSK step control44

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x1B[BPSK_STEP_SET23]

Function: BPSK step control setting 23
Address: 0x1B (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP47[3:0]	0000	R/W	BPSK step control47
3:0	STEP46[3:0]	0000	R/W	BPSK step control46

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x1C[BPSK_STEP_SET24]

Function: BPSK step control setting 24
Address: 0x1C (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP49[3:0]	0000	R/W	BPSK step control49
3:0	STEP48[3:0]	0000	R/W	BPSK step control48

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x1D[BPSK_STEP_SET25]

Function: BPSK step control setting 25
Address: 0x1D (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP51[3:0]	0000	R/W	BPSK step control51
3:0	STEP50[3:0]	0000	R/W	BPSK step control50

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x1E[BPSK_STEP_SET26]

Function: BPSK step control setting 26
Address: 0x1E (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP53[3:0]	0000	R/W	BPSK step control53
3:0	STEP52[3:0]	0000	R/W	BPSK step control52

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x1F[BPSK_STEP_SET27]

Function: BPSK step control setting 27
Address: 0x1F (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP55[3:0]	0000	R/W	BPSK step control55
3:0	STEP54[3:0]	0000	R/W	BPSK step control54

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x20[BPSK_STEP_SET28]

Function: BPSK step control setting 28
Address: 0x20 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP57[3:0]	0000	R/W	BPSK step control57
3:0	STEP56[3:0]	0000	R/W	BPSK step control56

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x21[BPSK_STEP_SET29]

Function: BPSK step control setting 29
Address: 0x21 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP59[3:0]	0000	R/W	BPSK step control59
3:0	STEP58[3:0]	0000	R/W	BPSK step control58

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x22[BPSK_STEP_SET30]

Function: BPSK step control setting 30
Address: 0x22 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP61[3:0]	0000	R/W	BPSK step control61
3:0	STEP60[3:0]	0000	R/W	BPSK step control60

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x23[BPSK_STEP_SET31]

Function: BPSK step control setting 31
Address: 0x23 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP63[3:0]	0000	R/W	BPSK step control63
3:0	STEP62[3:0]	0000	R/W	BPSK step control62

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x24[BPSK_STEP_SET32]

Function: BPSK step control setting 32
Address: 0x24 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP65[3:0]	0000	R/W	BPSK step control65
3:0	STEP64[3:0]	0000	R/W	BPSK step control64

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x25[BPSK_STEP_SET33]

Function: BPSK step control setting 33
Address: 0x25 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP67[3:0]	0000	R/W	BPSK step control67
3:0	STEP66[3:0]	0000	R/W	BPSK step control66

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x26[BPSK_STEP_SET34]

Function: BPSK step control setting 34
Address: 0x26 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP69[3:0]	0000	R/W	BPSK step control69
3:0	STEP68[3:0]	0000	R/W	BPSK step control68

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x27[BPSK_STEP_SET35]

Function: BPSK step control setting 35
Address: 0x27 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP71[3:0]	0000	R/W	BPSK step control71
3:0	STEP70[3:0]	0000	R/W	BPSK step control70

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x28[BPSK_STEP_SET36]

Function: BPSK step control setting 36
Address: 0x28 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP73[3:0]	0000	R/W	BPSK step control73
3:0	STEP72[3:0]	0000	R/W	BPSK step control72

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x29[BPSK_STEP_SET37]

Function: BPSK step control setting 37
Address: 0x29 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP75[3:0]	0000	R/W	BPSK step control75
3:0	STEP74[3:0]	0000	R/W	BPSK step control74

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x2A[BPSK_STEP_SET38]

Function: BPSK step control setting 38
Address: 0x2A (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP77[3:0]	0000	R/W	BPSK step control77
3:0	STEP76[3:0]	0000	R/W	BPSK step control76

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x2B[BPSK_STEP_SET39]

Function: BPSK step control setting 39
Address: 0x2B (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP79[3:0]	0000	R/W	BPSK step control79
3:0	STEP78[3:0]	0000	R/W	BPSK step control78

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x2C[BPSK_STEP_SET40]

Function: BPSK step control setting 40
Address: 0x2C (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP81[3:0]	0000	R/W	BPSK step control81
3:0	STEP80[3:0]	0000	R/W	BPSK step control80

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x2D[BPSK_STEP_SET41]

Function: BPSK step control setting 41
Address: 0x2D (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP83[3:0]	0000	R/W	BPSK step control83
3:0	STEP82[3:0]	0000	R/W	BPSK step control82

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x2E[BPSK_STEP_SET42]

Function: BPSK step control setting 42
Address: 0x2E (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP85[3:0]	0000	R/W	BPSK step control85
3:0	STEP84[3:0]	0000	R/W	BPSK step control84

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x2F[BPSK_STEP_SET43]

Function: BPSK step control setting 43
Address: 0x2F (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP87[3:0]	0000	R/W	BPSK step control87
3:0	STEP86[3:0]	0000	R/W	BPSK step control86

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x30[BPSK_STEP_SET44]

Function: BPSK step control setting 44
Address: 0x30 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP89[3:0]	0000	R/W	BPSK step control89
3:0	STEP88[3:0]	0000	R/W	BPSK step control88

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x31[BPSK_STEP_SET45]

Function: BPSK step control setting 45
Address: 0x31 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP91[3:0]	0000	R/W	BPSK step control91
3:0	STEP90[3:0]	0000	R/W	BPSK step control90

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x32[BPSK_STEP_SET46]

Function: BPSK step control setting 46
Address: 0x32 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP93[3:0]	0000	R/W	BPSK step control93
3:0	STEP92[3:0]	0000	R/W	BPSK step control92

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x33[BPSK_STEP_SET47]

Function: BPSK step control setting 47
Address: 0x33 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP95[3:0]	0000	R/W	BPSK step control95
3:0	STEP94[3:0]	0000	R/W	BPSK step control94

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x34[BPSK_STEP_SET48]

Function: BPSK step control setting 48
Address: 0x34 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP97[3:0]	0000	R/W	BPSK step control97
3:0	STEP96[3:0]	0000	R/W	BPSK step control96

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x35[BPSK_STEP_SET49]

Function: BPSK step control setting 49
Address: 0x35 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP99[3:0]	0000	R/W	BPSK step control99
3:0	STEP98[3:0]	0000	R/W	BPSK step control98

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x36[BPSK_STEP_SET50]

Function: BPSK step control setting 50
Address: 0x36 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP101[3:0]	0000	R/W	BPSK step control101
3:0	STEP100[3:0]	0000	R/W	BPSK step control100

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x37[BPSK_STEP_SET51]

Function: BPSK step control setting 51
Address: 0x37 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP103[3:0]	0000	R/W	BPSK step control103
3:0	STEP102[3:0]	0000	R/W	BPSK step control102

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x38[BPSK_STEP_SET52]

Function: BPSK step control setting 52
Address: 0x38 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP105[3:0]	0000	R/W	BPSK step control105
3:0	STEP104[3:0]	0000	R/W	BPSK step control104

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x39[BPSK_STEP_SET53]

Function: BPSK step control setting 53
Address: 0x39 (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP107[3:0]	0000	R/W	BPSK step control107
3:0	STEP106[3:0]	0000	R/W	BPSK step control106

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x3A[BPSK_STEP_SET54]

Function: BPSK step control setting 54
Address: 0x3A (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP109[3:0]	0000	R/W	BPSK step control109
3:0	STEP108[3:0]	0000	R/W	BPSK step control108

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x3B[BPSK_STEP_SET55]

Function: BPSK step control setting 55
Address: 0x3B (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP111[3:0]	0000	R/W	BPSK step control111
3:0	STEP110[3:0]	0000	R/W	BPSK step control110

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x3C[BPSK_STEP_SET56]

Function: BPSK step control setting 56
Address: 0x3C (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP113[3:0]	0000	R/W	BPSK step control113
3:0	STEP112[3:0]	0000	R/W	BPSK step control112

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x3D[BPSK_STEP_SET57]

Function: BPSK step control setting 57
Address: 0x3D (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP115[3:0]	0000	R/W	BPSK step control115
3:0	STEP114[3:0]	0000	R/W	BPSK step control114

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x3E[BPSK_STEP_SET58]

Function: BPSK step control setting 58
Address: 0x3E (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP117[3:0]	0000	R/W	BPSK step control117
3:0	STEP116[3:0]	0000	R/W	BPSK step control116

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x3F[BPSK_STEP_SET59]

Function: BPSK step control setting 59
Address: 0x3F (BANK10)
Reset value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:4	STEP119[3:0]	0000	R/W	BPSK step control119
3:0	STEP118[3:0]	0000	R/W	BPSK step control118

[Description]
1. For details, please refer to the “BPSK Modulation”.

0x40[PADRV_CTRL]

Function: PA driver control setting
Address: 0x40 (BANK10)
Reset value: 0x53

Bit	Bit name	Reset value	R/W	Description
7:4	PADRV_DLY[3:0]	0101	R/W	PA driver control delay setting Delay time = master clock period / 2 * setting value (Note) Setting value should be set larger than or equal 2.
3:2	Reserved	00	R	Reserved
1	PADRV_CTRL_SEL	1	R/W	PA driver function select setting 0: Control relevant to PA regulator voltage 1: linear control
0	PADRV_CTRL_EN	1	R/W	PA driver control enable 0: disable 1: enable

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x41[PADRV_ADJ1]

Function: PA driver adjustment 1
Address: 0x41 (BANK10)
Initial value: 0x00

Bit	Bit name	Reset value	R/W	Description
7:0	PADRV_ADJ1[7:0]	0000_0000	R/W	PA driver adjustment 1 (Note) This function is valid when PADRV_CTRL_SEL([PADRV_CTRL: B10 0x40(1)])=0b0 (Note) This register sets up the offset value over PA regulator voltage control .

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x42[PADRV_ADJ2_H]

Function: PA driver adjustment 2(high byte)
Address:0x42 (BANK10)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:2	Reserved	00_0000	R	Reserved
1	PADRV_INC	0	R/W	PA driver control enable 0: 1 step 1: 2 step
0	PADRV_ADJ2[8]	0	R/W	PA driver adjustment 2(high 1 bit) (Note) This function is valid when PADRV_CTRL_SEL([PADRV_CTRL: B10 0x40(1)])=0b1 (Note) When PA regulator voltage setting is equal to this register , linear control starts.

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x43[PADRV_ADJ2_L]

Function: PA driver adjustment 2(low byte)
Address:0x43 (BANK10)
Reset value:0x2C

Bit	Bit name	Reset value	R/W	Description
7:0	PADRV_ADJ2[7:0]	0010_1100	R/W	PA driver adjustment 2(low byte)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x44[PADRV_CLK_SET_H]

Function: PA driver control clock setting (high byte)
Address:0x44 (BANK10)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7	PADRV_CLK_STEP	0	R/W	PA driver linear control clock frequency select setting 0: master clock frequency / 2 (18MHz) 1: master clock frequency / 32 (1.125MHz)
6:1	Reserved	00_0000	R	Reserved
0	PADRV_CLK_SET[8]	0	R/W	PA driver control clock period setting(high 1bit) PA driver control clock period = PA driver linear control clock frequency select setting(PADRV_CLK_STEP) * setting value

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x45[PADRV_CLK_SET_L]

Function: PA driver control clock setting (low byte)
Address:0x45 (BANK10)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:0	PADRV_CLK_SET[7:0]	0000_0000	R/W	PA driver control clock period setting(low byte)

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

0x46[PADRV_UP_ADJ]

Function: PA driver control start time setting
Address:0x46 (BANK10)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R	Reserved
5:0	PADRV_UP_ADJ[5:0]	00_0001	R/W	PA driver control start time setting

[Note]
1. Please use the value specified in the “Initialization table” and don’t change it.

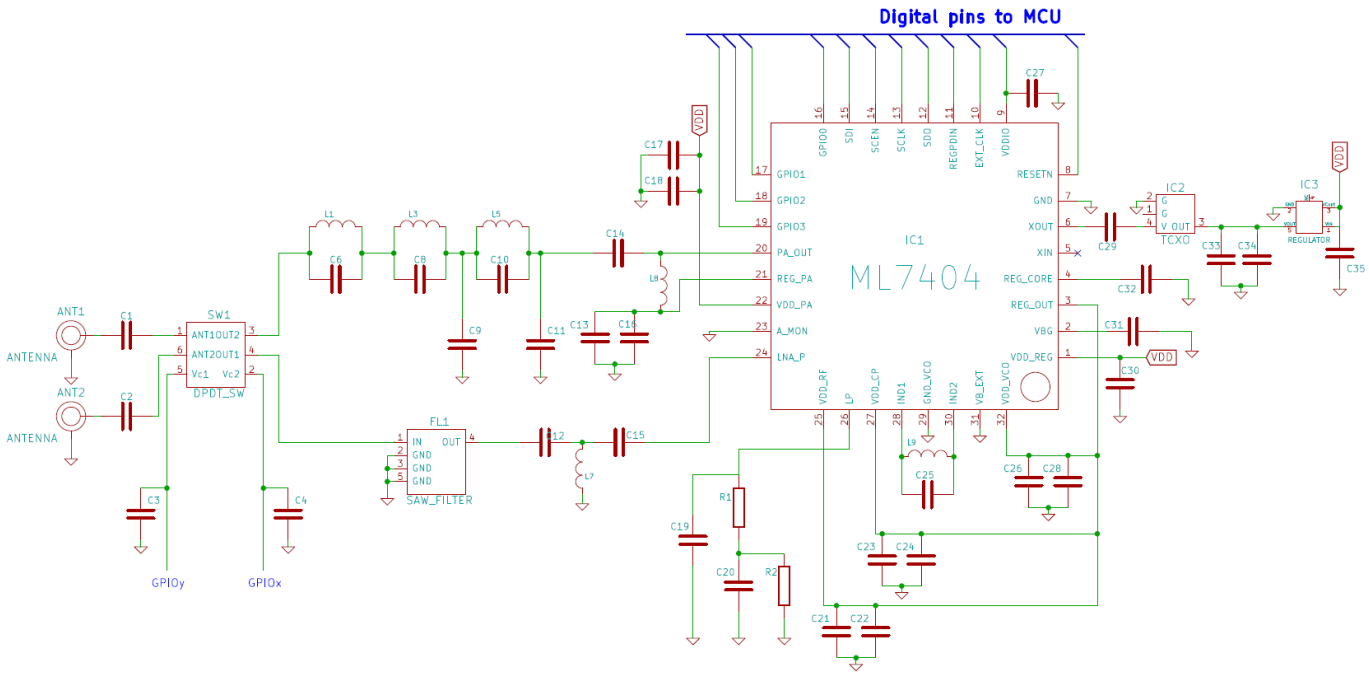
0x47-0x7F[Reserved]

Function : Reserved
Address : 0x47-0x7F (BANK10)
Reset value : 0x00

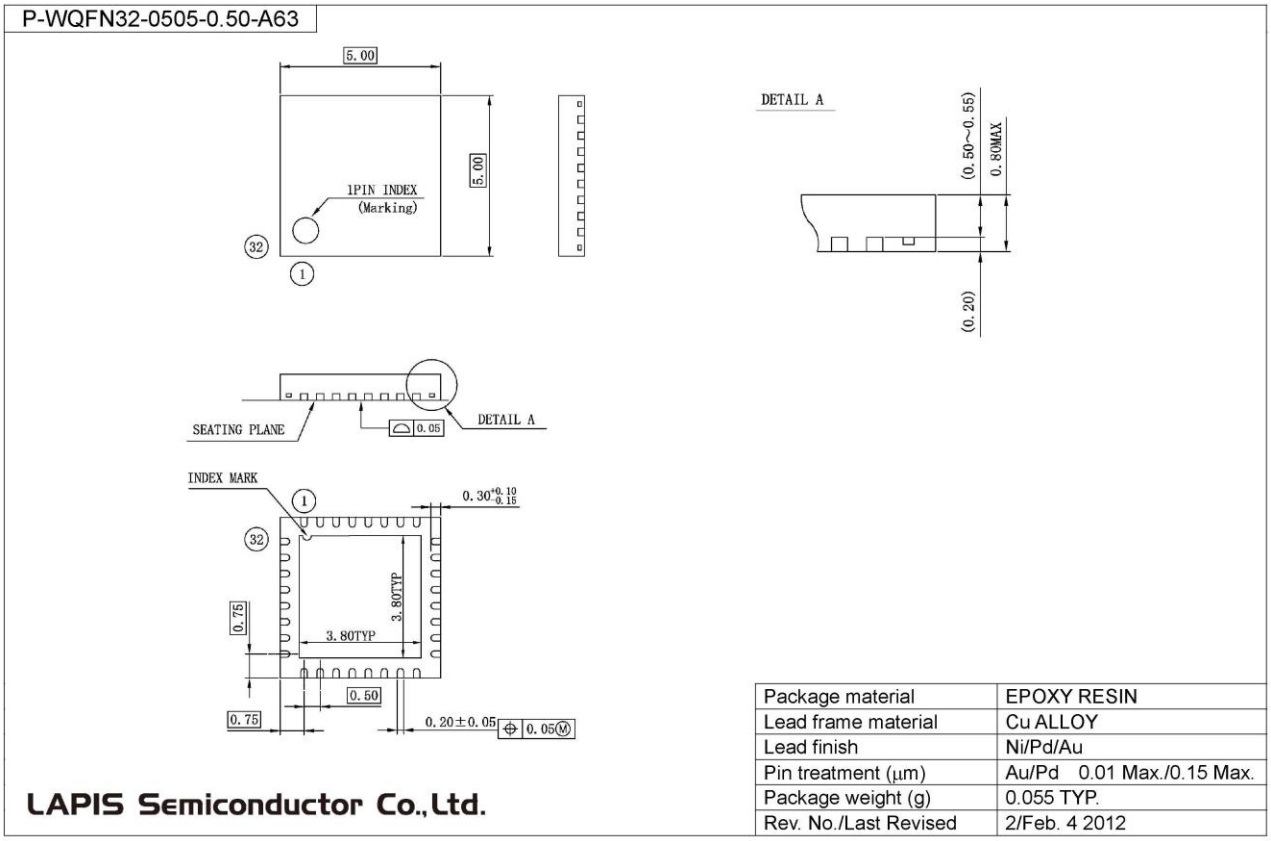
Bit	Bit name	Reset value	R/W	Description
7:0	Reserved	0000_0000	R	Reserved

■Application circuit

The below diagram does not show decoupling capacitors for LSI power pins.
10uF decoupling capacitor should be placed to common 3.3V power pins .
MURATA LQW15series inductors are recommended.



■Package Dimensions



Package material	EPOXY RESIN
Lead frame material	Cu ALLOY
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 Max./0.15 Max.
Package weight (g)	0.055 TYP.
Rev. No./Last Revised	2/Feb. 4 2012

Remarks for surface mount type package

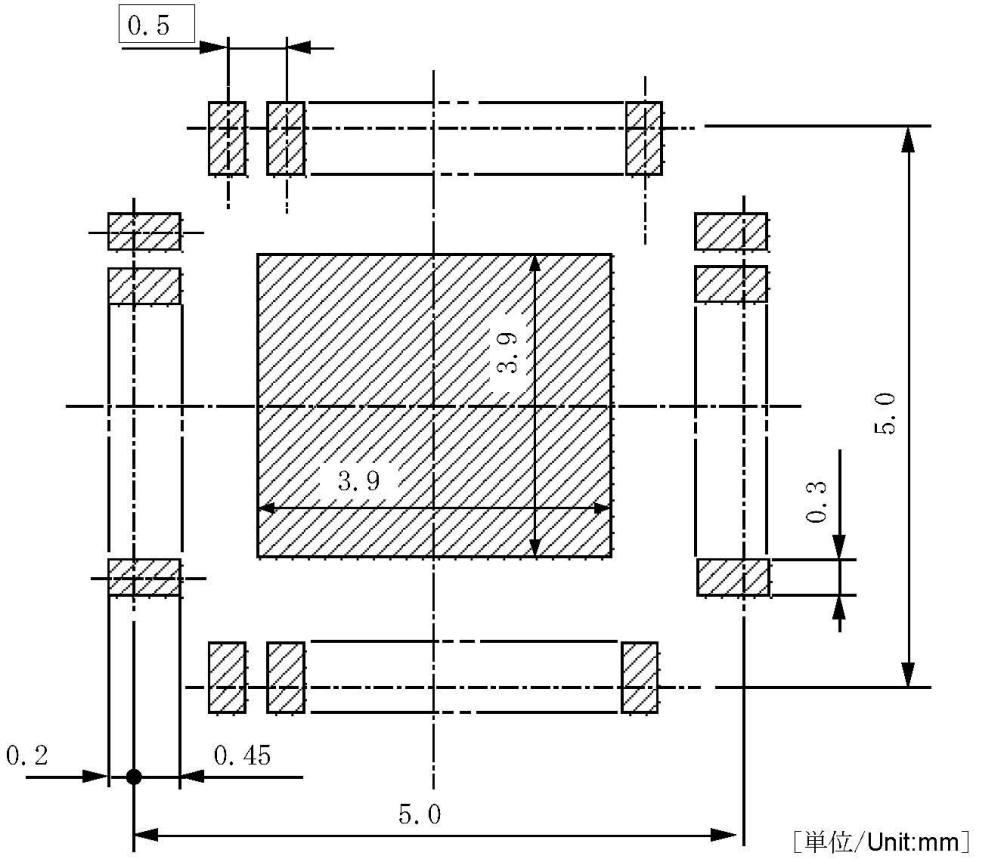
Surface mount type package is very sensitive affected by heating from reflow process, humidity during storaging Therefore, in case of reflow mouting process, please contact sales office about product name, package name, number of pin, package code and required reflow process condition (reflow method, temperature, number of reflow process), storage condition.

■Footprint Pattern (Recommendation)

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts, reliability, wiring, and elimination of slder bridges.

The optimum design for the foot pattern varies with the materials of the substrate, the sort and thichness of used soldering paste, and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering PC boards.

P-WQFN32-0505-0.50-A63



■Revision History

Document No.	Release date	page		Revision description
		Before revision	After revision	
FEDL7404-03	May 28, 2018	-	-	initial release (This document starts with the 3rd edition in order to match the version number of this document to FJDL7404)
FEDL7404-04	Oct 5, 2018	2	2	[Features] Added supporting modulation scheme to anntena diversity function.
		82	82	[Functional Description-RX Related Funcition-Diversity funcition] Added supporting modulation scheme.
		209	209	DC_FIL_SEL([DC_FIL_SET: B0 0x59(2-0)]) Added bit description(0b110/111)
FEDL7404-05	Apr 1st, 2019	8	8	[Pin Definitions]-[Reulator Pins] delete description(*1)
		23	23	[Electrical Characteristics]-[Reset Characteristics] delete “RESETN rising edge delay time”
		56	56	[Function Description]-[PacketHandling Function]-[FIFO control function] added note(4)
		110	110	[LSI Adjustment items and Adjustment Method]-[VCO Adjustment] added description(VTUNE_COMP_ON)
		201	202	[SYNC_CONDITION1: B0 0x45] added register description
		-	259	[VTUNE_COMP_ON: B2 0x40] added register description
FEDL7404-06	Nov 1, 2023	2	2	Add Product Name,application
		305	305	The description of [Note] has been updated.
FEDL7404-07	Jan 10, 2024	305	305	The description of [Note] has been updated.

(Note) Corrections in spelling , improvements in the description are not included in the Revision history.

Notes

1) When using LAPIS Technology Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings[*1], recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

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