Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ROHM GROUP
LAPIS TECHNOLOGY

FEDL7425-02
Issue Date: March. 19, 2024

ML7425

Sub-GHz RF low-power transceiver IC

■Overview

The ML7425 is a low-power sub-GHz radio transceiver LSI which integrates RF, IF, MODEM, and HOST interface into a single chip. RF frequency supports 145 to 1,020MHz range. In addition, a programable channel-selection filter can support a reception band of 1.7kHz to 1,200kHz. The ML7425 can be used for N-mode (169MHz), F-mode (434MHz), and S/T/C/R mode (868MHz) in the European telemetry standard (Wireless M-Bus), Japanese low-power security system radio stations and specified low-power radio stations (RCR STD-30, STD-T67, STD-T108), and worldwide Sigfox standards. The ML7425 includes IEEE802.15.4g and Wireless M-Bus packet handling functions.

■Features

- Compliant with wireless regulations of each country
  - Japanese: RCR STD-30, ARIB STD-T67, ARIB STD-T108
  - Europe: ETSI EN 300 220, ETSI EN 54-25
  - North America: FCC CFR47 Part 15, FCC CFR47 Part 90, 24, 101

- Support standards
  - IEEE802.15.4g/15.4aa
  - Wi-SUN
  - Wireless M-BUS
  - Sigfox Revision 2.E

- RF Frequency
  - 145MHz to 170MHz
  - 210MHz to 250MHz
  - 280MHz to 340MHz
  - 415MHz to 510MHz
  - 835MHz to 1,020MHz

- Realizes high-precision modulation by direct modulation method of fractional-N PLL
- Support modulation scheme: 2(G)FSK/4(G)FSK, ASK, OOK, BPSK (Tx only)
- Suppot data rate : 0.1k to 1,200kbps (2FSK: 0.1k to 600kbps/4FSK: 0.2k to 1,200kbps)
- Equipped with encoding function of NRZ, Manchester, and 3 out of 6
- Equipped with data whitening function
- Equipped with a programmable channel filter function
- Equipped with a programmable frequency deviation function
- Built-in polarity reversal function for Tx/Rx data
- Equipped with TCXO direct input function (24 to 26MHz/48MHz to 52MHz)
- On-chip crystal oscillation circuit (24 to 26MHz/48MHz to 52MHz)
- Equipped with a load capacitance adjustment function for oscillation circuit pin
- Equipped with frequency fine adjustment function (Fine-tunable with fractional-N PLL)
- Built-in synchronous serial peripheral interface(SPI)
- Built-in Tx PA with power control function
- Equipped with Tx power fine adjustment function
- Equipped with automatic ramp control of Tx power
- Equipped with external Tx PA control function

ROHM SEMICONDUCTOR

- Equipped with received signal strength indicator (RSSI) notification function and threshold judgment function
- Equipped with high speed carrier checking function
- Equipped with FEC Function
- Equipped with AFC Function
- Equipped with antenna diversity function
- Equipped with general purpose timer (2ch)
- Equipped with Test Pattern Generator (PN9, CW, 01-pattern, ALL "1", and ALL "0" are supported)
- Packet mode function
    - Supports IEEE802.15.4g Packet Format (Format C)
    - Supports Wireless M-Bus Packet Format (Format A/B)
    - Supports General-purpose Packet Format (Format C/D)
    - Supports packet length up to 255 bytes (Format A/B) and 2,047 bytes (Format C/D)
    - Built-in Tx FIFO (64 bytes) and Rx FIFO (64 bytes)
    - Detection preamble pattern setting function (Max.4 bytes)
    - Tx preamble length setting function (Max. 255 bytes)
    - SyncWord setting function (Max. 4 bytes x 2 patterns)
    - CRC Function (CRC32/CRC16/CRC8 selectable)
    - Address check function (Max. 13 bytes x 2 patterns)
        Wireless M-Bus: C-field/M-field/A-field
        ∗Proprietary packet format is possible depending on setting
    - Supports IEEE802.15.4g ModeSwitch Packet Format

- Supply voltage
    2.6V to 3.6V (when using DCDC)
    1.8V to 3.6V (when not using DCDC)

- Operational temperature -40°C to 105°C (average operational temperature 70°C)

- Consumption current

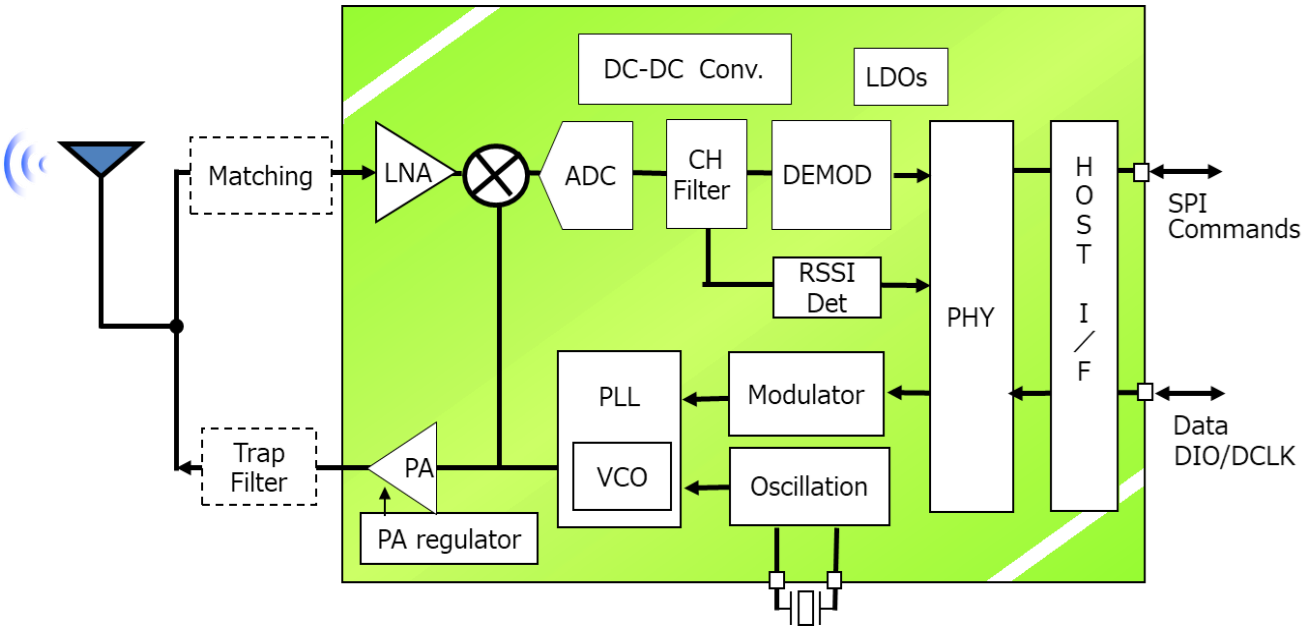
Deep sleep mode		0.1 μA
Sleep mode		0.45 μA (registers retained)
At transmission	13dBm	27mA(Typ.) @3.3V, When using DCDC
At reception		11mA(Typ.) @3.3V, When using DCDC

- Package
    32-pin WQFN (5mm x 5mm) 0.5mm
    Lead-free, RoHS compliance

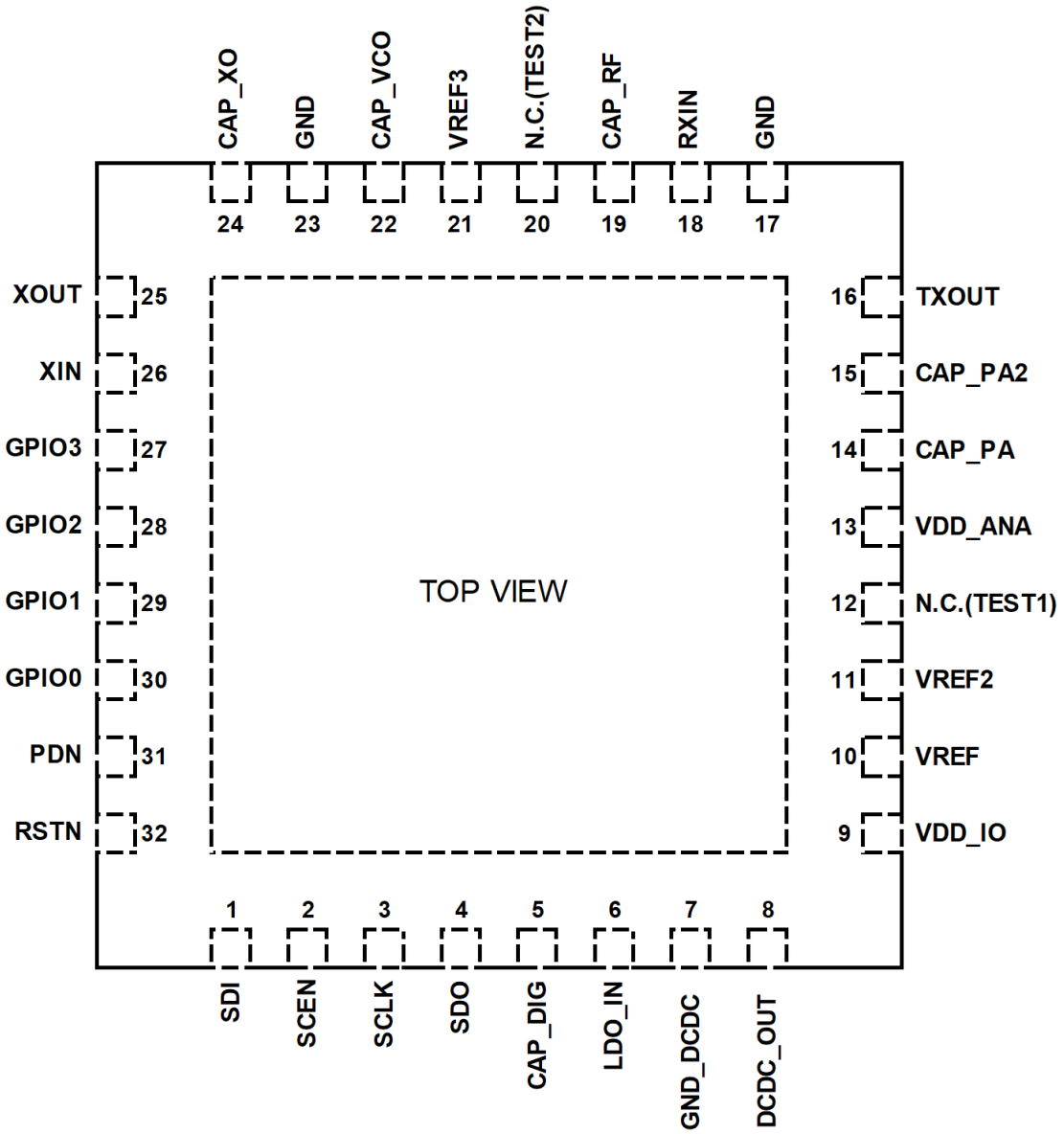
- Product Name ML7425GD

- Application
    Remote control
    Home, Building security
    Sensor networks
    Smart Meter
    Logistics Tracking
    Infrastructure Monitoring
    Monitoring system

■Block Diagram



■Pin Layout



32-pin WQFN (5mm x 5mm) 0.5mm pitch

■Pin Description

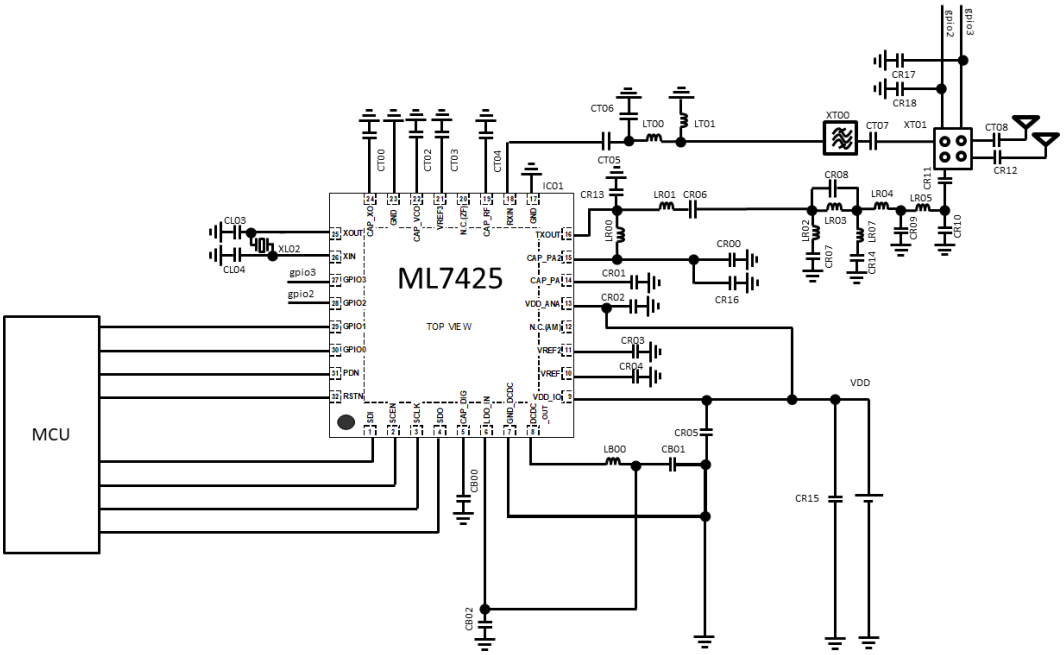
Pin status			Attribute definition		
I	:	CMOS input	IS	:	Schmitt Trigger input pin
O	:	CMOS output	O	:	Digital output pin
OD	:	Open drain output	IOS	:	Digital input/output pin (Schmitt input)
Hi-Z	:	High impedance	IOA	:	Analog input/output pin
			IRF	:	RF input pin
			ORF	:	RF output pin
			VDD	:	Power supply pin
			GND	:	Ground

Pin No.	Pin Name	Attribute	Description
1	SDI	IS	SPI data input pin
2	SCEN	IS	SPI enable pin (H: disable, L: SPI enable)
3	SCLK	IS	SPI clock input pin
4	SDO	O	SPI data output pin
5	CAP_DIG	IOA	Pin for an internal LDO decoupling capacitor (Digital)
6	LDO_IN	VDD	Power supply pin (Regulator)
7	GND_DCDC	GND	Ground
8	DCDC_OUT	IOA	Switching regulator output pin (N.C. when DCDC is not used)
9	VDD_IO	VDD	Power supply pin (IO)
10	VREF	IOA	Pin for a decoupling capacitor 1
11	VREF2	IOA	Pin for a decoupling capacitor 2
12	N.C.(TEST1)	N.C.	Pin to open
13	VDD_ANA	VDD	Power supply pin (Analog)
14	CAP_PA	IOA	Pin for a decoupling capacitor (PA)
15	CAP_PA2	IOA	Pin for an internal LDO decoupling capacitor (PA)
16	TXOUT	ORF	RF signal output pin
17	GND	GND	Ground
18	RXIN	IRF	RF signal input pin
19	CAP_RF	IOA	Pin for an internal LDO decoupling capacitor (RF)
20	N.C.(TEST2)	N.C.	Pin to open
21	VREF3	IOA	Pin for a decoupling capacitor 3
22	CAP_VCO	IOA	Pin for an internal LDO decoupling capacitor (VCO)
23	GND	GND	Ground
24	CAP_XO	IOA	Pin for an internal LDO decoupling capacitor (XO)
25	XOUT	IOA	Pin for connecting a crystal (TCXO input pin when TCXO is used)
26	XIN	IOA	Pin for connecting a crystal (N.C when TCXO is used)
27	GPIO3	IOS	Digital input/output pin (N.C. when GPIO3 is not used)
28	GPIO2	IOS	Digital input/output pin (N.C. when GPIO2 is not used)
29	GPIO1	IOS	Digital input/output pin (N.C. when GPIO1 is not used)
30	GPIO0	IOS	Digital input/output pin (N.C. when GPIO0 is not used)
31	PDN	IS	Power-down setting pin (H: Power-down mode, L: Normal mode)
32	RSTN	IS	Reset pin (H: Normal mode, L: Reset mode)

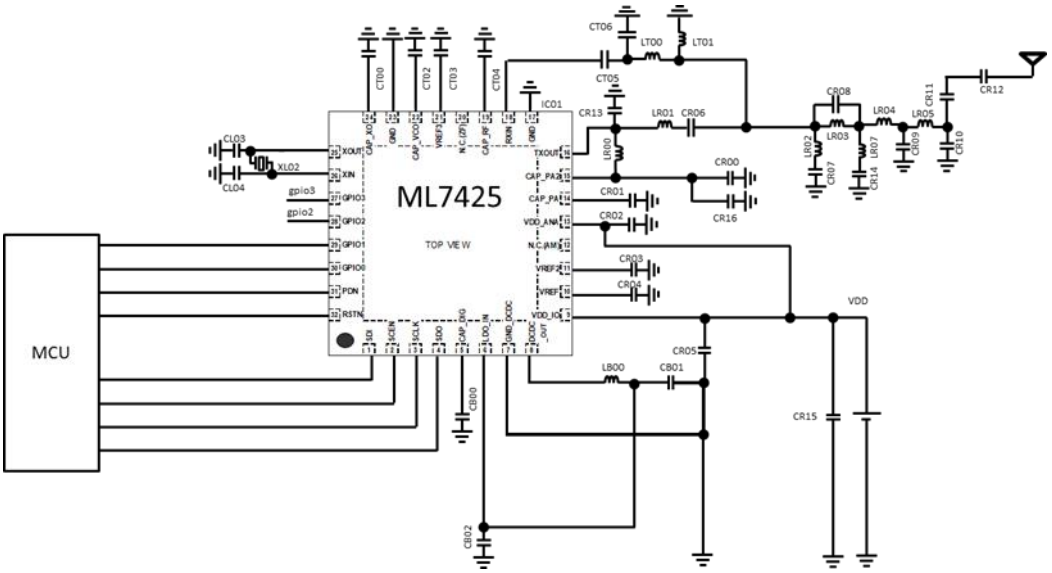
(Note)
Input pins (SDI, SCEN, SCLK, PDN, RSTN) must be logically Low or High.
Input/output pins (GPIO0 to 3) should be controlled by the host microcomputer.
The output pin (SDO) becomes an open-drain output pin after the reset is released. And this pin can be selected as a CMOS output or an open drain output. Please switch it according to the application.

Pin No.	Pin Name	Pin status				Attribute	Description
		[At deep sleep] PDN=H RSTN=L/H	【At reset】 PDN=L RSTN=L	[After reset release] PDN=L RSTN=H	[Normal mode] PDN=L RSTN=H		
1	SDI	I	I	I	I	IS	SPI data input pin
2	SCEN	I	I	I	I	IS	SPI enable pin (H: disable, L: enable)
3	SCLK	I	I	I	I	IS	SPI clock input pin
4	SDO	Hi-Z	Hi-Z	OD	OD or O	O	SPI data output pin
27	GPIO3	Hi-Z	Hi-Z	O	I or O	IOS	Digital input/output pin
28	GPIO2	Hi-Z	Hi-Z	O	I or O	IOS	Digital input/output pin
29	GPIO1	Hi-Z	Hi-Z	O	I or O	IOS	Digital input/output pin
30	GPIO0	Hi-Z	Hi-Z	O	I or O	IOS	Digital input/output pin
31	PDN	I	I	I	I	IS	Power-down setting pin (H: Power-down mode, L: Normal mode)
32	RSTN	I	I	I	I	IS	Reset pin (H: Normal mode, L: Reset mode)

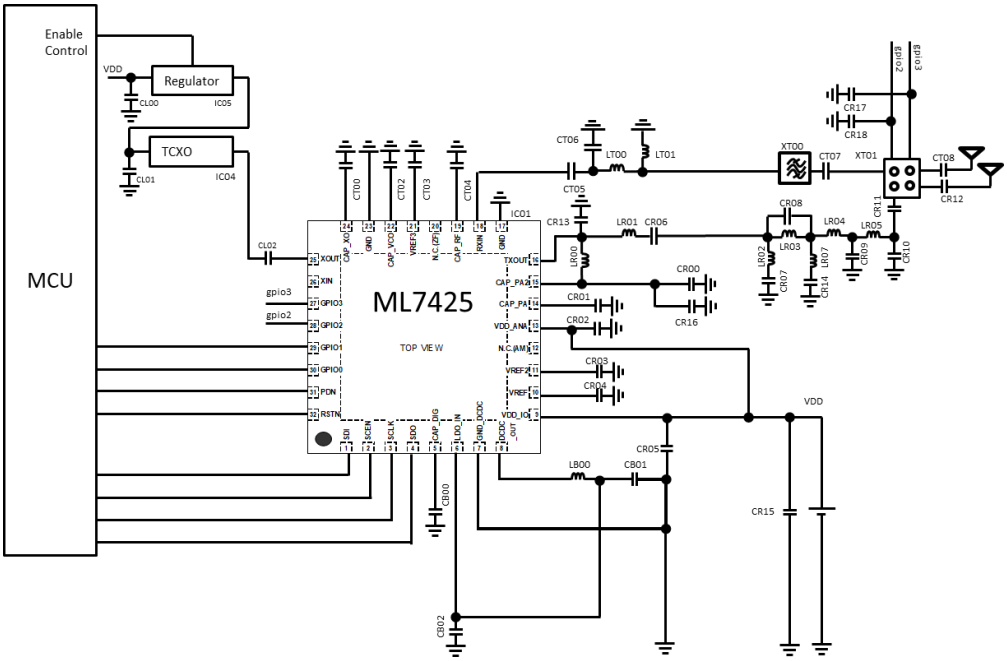
■Reference Schematic



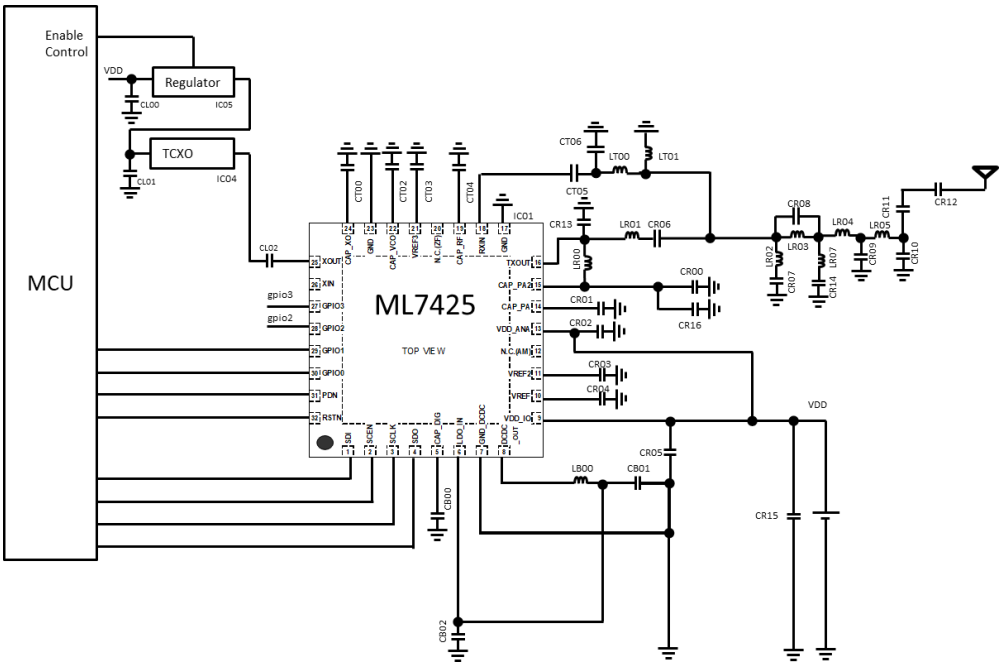
Separate Transmission and Reception Configuration (Using Crystal Oscillator and Antenna switch)



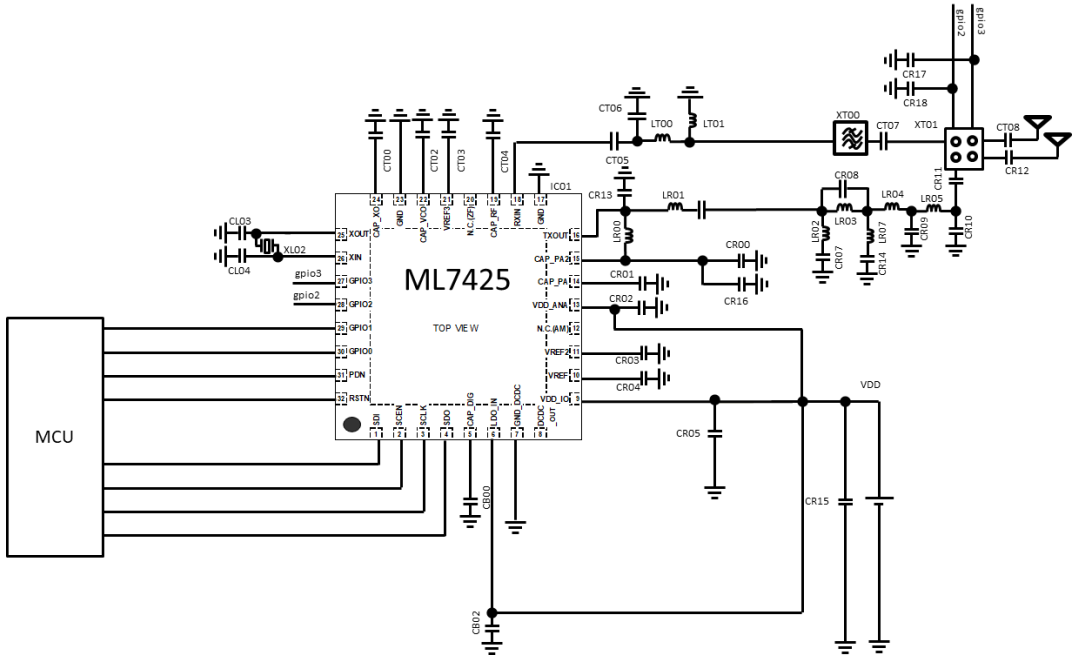
Common Transmission and Reception Configuration (Using Crystal Oscillator, Not Using Antenna switch)



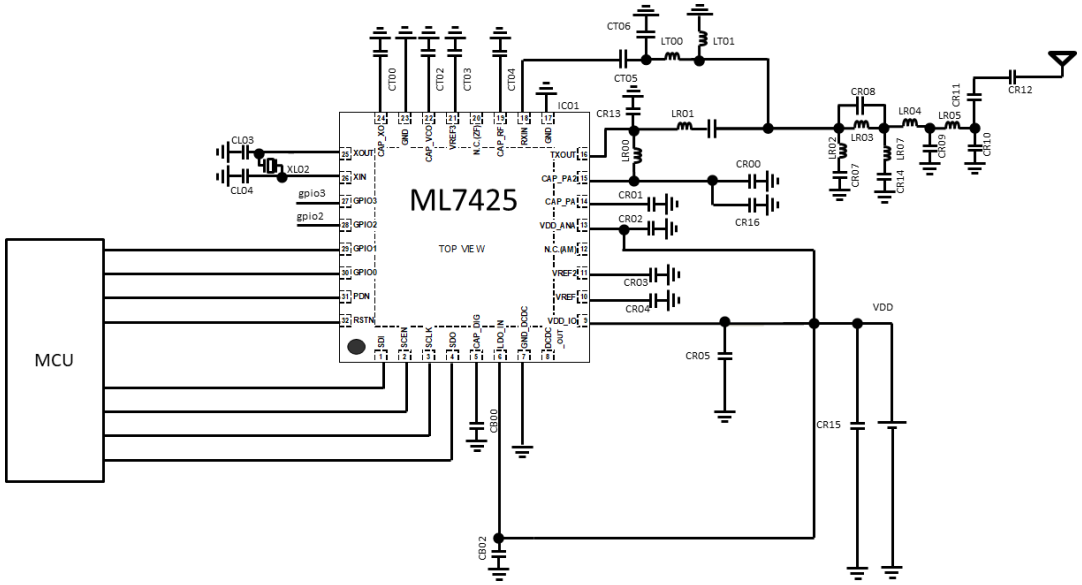
Separate Transmission and Reception Configuration (Using TCXO and Antenna switch)



Common Transmission and Reception Configuration (Using TCXO, Not Using Antenna switch)



Separate Transmission and Reception Configuration (Using Crystal Oscillator, Not using DCDC and Antenna switch)



Common Transmission and Reception Configuration (Using Crystal Oscillator, Not using DCDC, Not Using Antenna switch)

■Electrical Characteristics

●Absolute Maximum Ratings

Item	Pin name	Condition	Rating	Unit
Supply voltage	VDD_IO、VDD_ANA	-	-0.3 to +4.6	V
Ground voltage	GND	-	-0.3 to +0.3	V
Digital input voltage	PDN, SDI, SCEN, SCLK, GPIO0 to 3	-	-0.3 to +4.6	V
Digital output voltage	GPIO0 to 3、SDO	-	-0.3 to +4.6	V
High-level output current	GPIO0 to 3、SDO	-	-8.0 (*1)	mA
Low-level output current	GPIO0 to 3、SDO	-	8.0 (*1)	mA
Voltage to Analog pins 1	DCDC_OUT, LDO_IN, CAP_PA, CAP_PA2, VREF	-	-0.3 to +4.6	V
Voltage to Analog pins 2	CAP_VCO, CAP_RF, CAP_DIG, CAP_XO, XIN, XOUT, VREF2, VREF3	-	-0.3 to +2.0	V
RF input voltage	RXIN	-	-0.3 to +2.0	V
RF output voltage	TXOUT	-	-0.3 to +4.6	V
RF input level	-	Antenna end of board (50Ω)	0	dBm
Power dissipation	-	Ta= +25°C	3.45	W
Storage temperature	-	-	-55～+150	°C

*1 The current flowing out of the LSI is specified as a minus sign.
Example: -1mA indicates that up to 1mA of current flows out of the LSI pin.

●Reference Operating Conditions

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Voltage (I/O, ANA)	VDDIO/ VDD_ANA	VDD_IO, VDD_ANA pin	When not using DCDC	1.8	3.3	3.6	V
			When using DCDC	2.6	3.3	3.6	V
Operating temperature	Ta	-		-40	+25	+105	°C
Digital input Rising time	TIR	(*1)		-	-	20	ns
Digital input Falingl time	TIF	(*1)		-	-	20	ns
Digital output load	CDL	(*2)		-	-	20	pF
Reference clock frequency	FREF	XIN/XOUT pin		24	24	26	MHz
				48	48	52	MHz
Reference clock accuracy	ACREF	-		(*3)	(*3)	(*3)	ppm
X'tal equivalent series resistance	ESR	-		-	-	50	ohm
TCXO input voltage	VTCXO	DC Cutoff *When TCXO option is selected		0.8	-	1.5	Vpp
SPI clock input frequency	FSCLK	SCLK pin		0.032	2	16	MHz
SPI clock input duty ratio	DSCLK	SCLK pin		45	50	55	%
RF frequency	FRF	-		145	-	170	MHz
				210	-	250	MHz
				280	-	340	MHz
				415	-	510	MHz
				835	-	1020	MHz

*1 GPIO0, GPIO1, GPIO2, GPIO3, PDN, RSTN, SDI, SCEN, SCLK pin

*2 GPIO0, GPIO1, GPIO2, GPIO3, SDO pin

*3 The allowable frequency accuracy for transmission and reception are shown below.
In order to comply with various standards, please use the frequency accuracy according to the standards as shown in the table below.

Standard	Required frequency accuracy
ARIB STD-T108	±20 ppm
RCR STD-30 type III (Japanese)	±10 ppm
RCR STD-30 type IV (Japanese)	±4 ppm
Wireless M-Bus F mode	±16 ppm

●Power Consumption

FREF =48 MHz, DCDC:ON

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Deep sleep current	I_{DD_DSLP}	Deep sleep state (Not retaining Registers, all function halt)		-	0.1	50 (*1)	μA
Sleep current	I_{DD_SLP}	Sleep state (retaining registers, retaining RXFIFO)		-	0.45	120 (*2)	μA
Idle current	I_{DD_IDL1}	DCDC=ON		-	1.2	3	mA
	I_{DD_IDL2}	DCDC=OFF		-	1.8	6	mA
Rx current	I_{DD920_RX1}	920MHz band, 2-FSK, 100kbps	DCDC=ON	-	11	25	mA
	I_{DD920_RX2}		DCDC=OFF		18	32	mA
Tx current	I_{DD920_TX1}	920MHz band, 2-FSK, 100kbps, 13 dBm output	DCDC=ON	-	27	48	mA
	I_{DD920_TX2}		DCDC=OFF	-	48	60	mA

(*1) For reference, maximum 0.8uA at 25℃
(*2) For reference, maximum 2.0uA at 25℃

●DC Characteristics

FREF =48MHz

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage Input High	VIH	RSTN, PDN, SDI, SCLK, SCEN, GPIO0/1/2/3 pin	V_{DDIO} x 0.75	-	V_{DDIO}	V
Voltage Input Low	VIL	RSTN, PDN, SDI, SCLK, SCEN, GPIO0/1/2/3 pin	0	-	V_{DDIO} x 0.18	V
Schmitt Trigger Threshold High Level	VT+	RSTN, PDN, SDI, SCLK, SCEN, GPIO0/1/2/3 pin	-	1.2	V_{DDIO} x 0.75	V
Schmitt Trigger Threshold Low Level	VT-	RSTN, PDN, SDI, SCLK, SCEN, GPIO0/1/2/3 pin	V_{DDIO} x 0.18	0.8	-	V
Input leakage current	IIH	RSTN, PDN, SDI, SCLK, SCEN, GPIO0/1/2/3 pin	-1	-	1	µA
	IIL	RSTN, PDN, SDI, SCLK, SCEN, GPIO0/1/2/3 pin	-1	-	1	µA
Tri-state Output leakage current	IOZH	SDO, GPIO0/1/2/3 pin	-1	-	1	µA
	IOZL	SDO, GPIO0/1/2/3 pin	-1	-	1	µA
Voltage Output High	VOH	SDO, GPIO0/1/2/3 pin IOH=-2mA	V_{DDIO} x 0.8	-	V_{DDIO}	V
Voltage Output Low	VOL	SDO, GPIO0/1/2/3 pin IOL=2mA	0	-	0.25	V
Pin capacitance	CIN	Input pins	-	6	-	pF
	COUT	Output pins	-	9	-	pF
	CRFIO	RF input pins	-	9	-	pF
	CAI	Analog input pins	-	9	-	pF

●RF Characteristics

Condition:

- Reference Schematic: Separate transmission and reception configuration (Using TCXO)
- Measurement point: Evaluation board antenna end (excluding loss of antenna switch and SAW filters)
- Modulation scheme: 2-FSK
- Frequency: 920MHz band

【Transmission Characteristics】

FREF =48 MHz, DCDC:ON

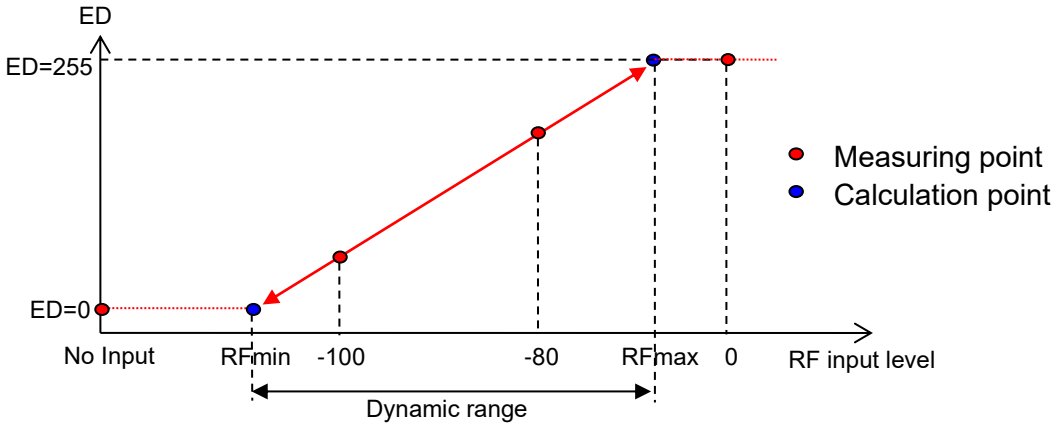
Item	Condition		Min.	Typ.	Max.	Unit
Tx output power	20mW (13dBm)		9	13	15	dBm
Occupied bandwidth (99%)	99% power bandwidth, Pattern: PN9 Data rate: 100 kbps Freq. deviation ±50kHz, BT=0.5		150	-	250	kHz
Adjacent channel leakage power ratio [ACPR]	Data rate: 100kbps, Pattern: PN9 13dBm output, Freq. deviation: ±50kHz, BT=0.5 Leakage power ratio in 300kHz offset ± 100kHz bandwidth		-	-	-28	dBc
Spurious emission level	At 13 dBm output Pattern: PN9 Data rate:100kbps Freq. deviation: ±50kHz, BT=0.5	710MHz or below	-	-	-36	dBm/100kHz
		710-900MHz	-	-	-55	dBm/1MHz
		900-915MHz	-	-	-55	dBm/100kHz
		915-930MHz	-	-	-36	dBm/100kHz
		930-1000MHz	-	-	-55	dBm/100kHz
		1000-1215MHz	-	-	-45	dBm/1MHz
		1215MHz or more	-	-	-30	dBm/1MHz
	Harmonic spurious level (2nd harmonic/3rd harmonic) At 13 dBm CW transmission ※When LC filter circuit is mounted		-	-	-30	dBm

【Receiver Characteristics】

FREF =48 MHz, DCDC:ON

Item	Condition		Min.	Typ.	Max.	Unit
Min. receiver sensitivity	100kbps mode Center frequency: 920.7MHz BER<0.1% GFSK, Freq. deviation: ± 50kHz, BT=0.5		-	-106	-97	dBm
Adjacent channel selectivity (*1)	Ta=25°C, 100kbps mode Center frequency: 920.7MHz Desired signal: GFSK, Freq. deviation: ± 50kHz, BT=0.5	Interference signal: CW +400kHz offset	25	40	-	dB
		Interference signal: CW -400KHz offset	22	37	-	dB
Blocking (*1)	Ta=25°C, 100kbps mode Center-frequency: 920.7MHz Desired signal: GFSK, Freq. deviation: ± 50kHz, BT=0.5	Interference signal: CW 2MHz offset	36	55	-	dB
		Interference signal: CW 10MHz offset	41	65	-	dB
Min. energy detection level (ED value)	RFmin in ED characteristics diagram (*2) 100kbps mode Center frequency: 920.7MHz Channel filter band =200kHz setting		-	-106	-100	dBm
Energy detection range	Dynamic range in ED characteristics diagram (*2) 100kbps mode Center frequency: 920.7MHz Channel filter band =200kHz setting		55	65	-	dB
Spurious emission level			-	-	-57	dBm

*1. The Measuring condition for interference-related characteristics is as follows:
Set the desired signal as [the level with BER = 0.1% (= reference sensitivity) + 3 dB], change the interference signal level to find the level at which becomes BER = 0.1%, and stipulate as U/D [dB] = (interference signal level) - (desired signal input level).
*2. ED characteristic diagram is shown below.



ED Characteristic Diagram

[Note]
The characteristics may be degraded when using channels near the multiplication of the reference clock or the multiplication of the reference clock divided by 2 or 4.

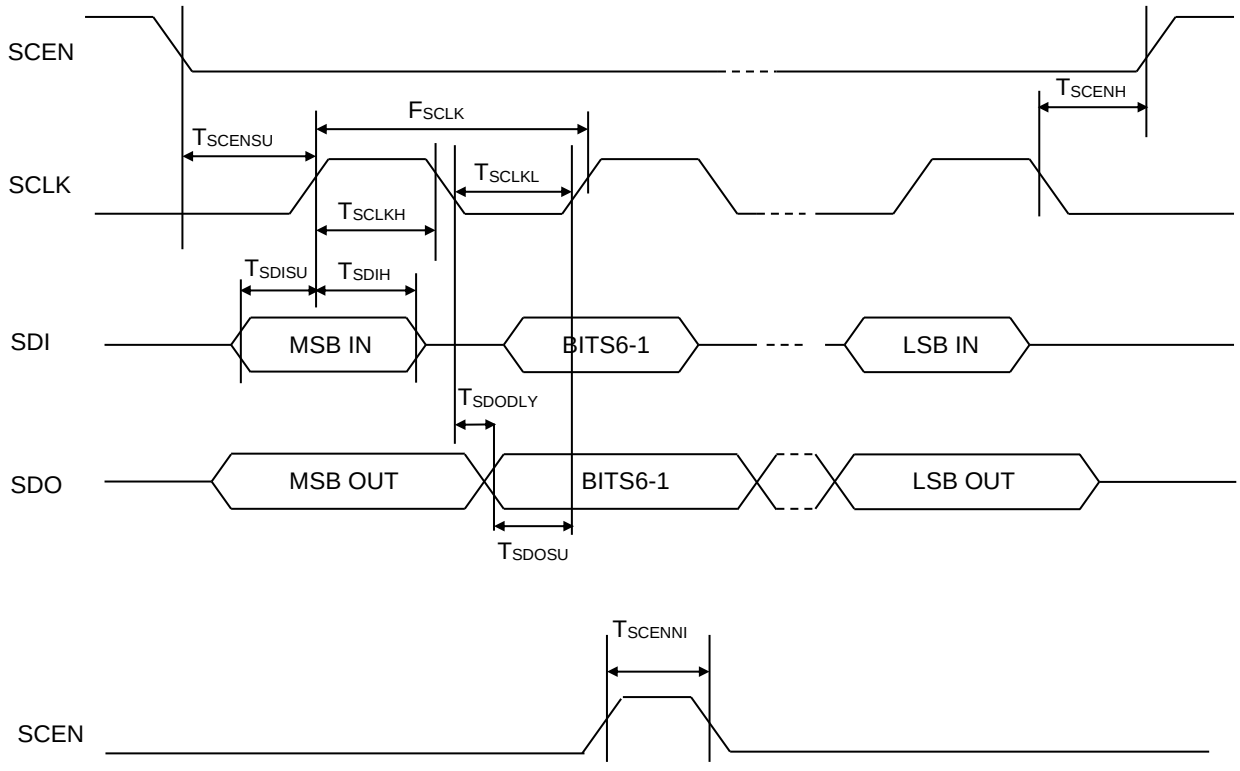
- Reference

●SPI Interface Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK clock frequency	F_{SCLK}	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	T_{SCENSU}		30	-	-	ns
SCEN input hold time	T_{SCENH}		30	-	-	ns
SCLK high pulse width	T_{SCLKH}		31	-	-	ns
SCLK low pulse width	T_{SCLKL}		31	-	-	ns
SDI input setup time	T_{SDISU}		5	-	-	ns
SDI input hold time	T_{SDIH}		15	-	-	ns
SCEN negate period	T_{SCENNI}		200	-	-	ns
SDO output delay time	T_{SDODLY}		-	-	25	ns
SDO output setup time	T_{SDOSU}		6	—	—	ns

[Note]

All timing measurement points are at VDDIO* 20% and VDDIO*80%.
Please refer the required setup time of host MCU for SDO output.

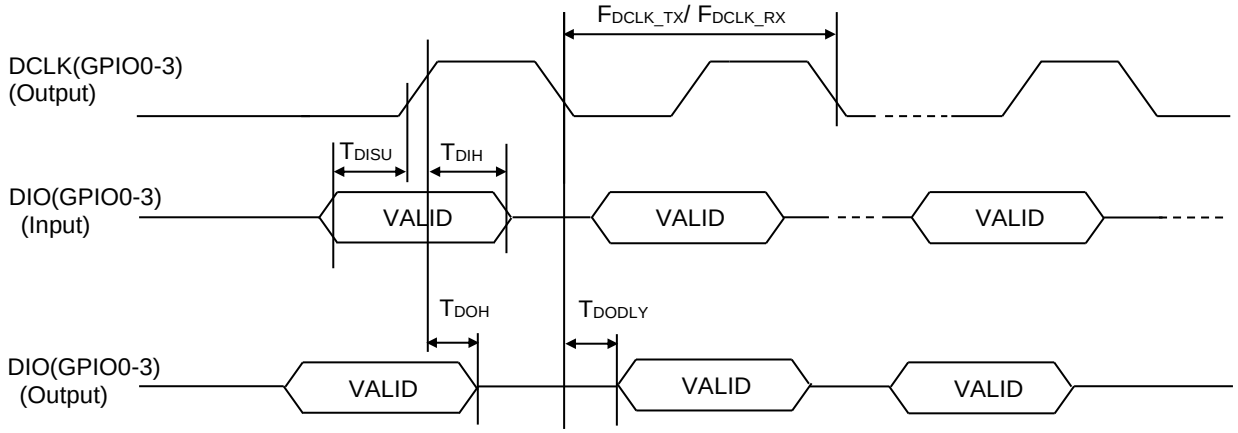


●DIO Interface Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DIO input setup time	T_{DISU}	Load capacitance CL=20pF	DataRate*1/4	-	-	μs
DIO input hold time	T_{DIH}		0	-		ns
DIO output delay time	T_{DODLY}		-	-	DataRate*1/10	μs
DIO output hold time	T_{DOH}		20	-	-	ns
DCLK frequency accuracy (*1) (TX)	F_{DCLK_TX}		- Clock freq. deviation	-	+ Clock freq. deviation	kHz
DCLK frequency accuracy (*2) (RX)	F_{DCLK_RX}		-30	-	+30	%
DCLK output duty ratio (TX)	D_{DCLK_TX}		45	-	55	%
DCLK output duty ratio (RX)	D_{DCLK_RX}		30	-	70	%

*1 When no decimal point occurs in calculating the Tx data rate value, Max. and Min. values of Tx DCLK frequency are the reference clock frequency deviations.
*2 Min. and max. of Rx DCLK frequency indicates the amount of jitter in the regenerated clock generated from the received signal (when synchronization is established).

[Note]
All timing measurement points are at VDDIO* 20% and VDDIO*80%.



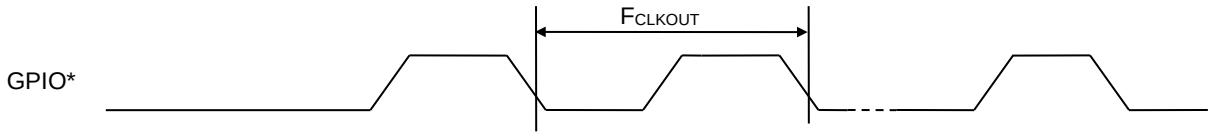
●Clock Output Characteristics

ML7406 has clock output function. The clock is output through GPIO1 pin as initialized setting.

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20 pF		FREF/8164 (0.0059) (*2)	FREF/740 (0.0649) (*2)	FREF/2 (24) (*2)	MHz
Clock output duty ratio (*1)	D_{CLKOUT}	Load capacitance CL=20 pF	FREF/2 (24)	25	-	75	%
			FREF/6 (8) (*2)	33	-	67	%
			Except above	47	50	53	%

*1 When set to FREF/2, the duty ratio is High:Low = 1:3. When set to FREF/6, the duty ratio is High:Low = 1:2 .
*2 The values in parentheses are the values at FREF =48MHz.

[Note]
All timing measurement points are at VDDIO* 20% and VDDIO*80%.



●Reset Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RSTN release delay time (power on period)	T_{RDL1}	All power pins After Power On	1	-	-	ms
RSTN pulse period (when booting from VDD_IO/VDD_ANA = 0V)	T_{RPW1}		0.5	-	-	ms
RSTN pulse-time 2 (*1) (when booting from VDD_IO/VDD_ANA ≠ 0V)	T_{RPW2}		1	-	-	ms
RSTN input delay time	T_{RDL2}	After VDD_IO/VDD_ANA>1.8	1	-	-	µs
RSTN input delay time after Power on (start from VDD_IO/VDD_ANA = 0V)	T_{RDL3}	From the rising edge of T_{RDL1} to the falling edge of TRPW1	100	-	-	µs

(*1) When starting from VDD_IO/VDD_ANA ≠ 0V, input Low pulse to RSTN pin after VDD_IO/VDD_ANA exceeds 1.8V.

[Note]

All timing measurement points are at VDDIO* 20% and VDDIO*80%.

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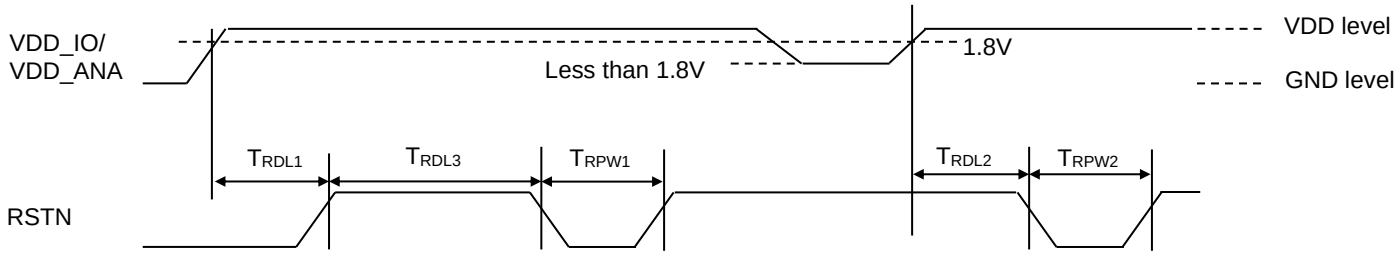
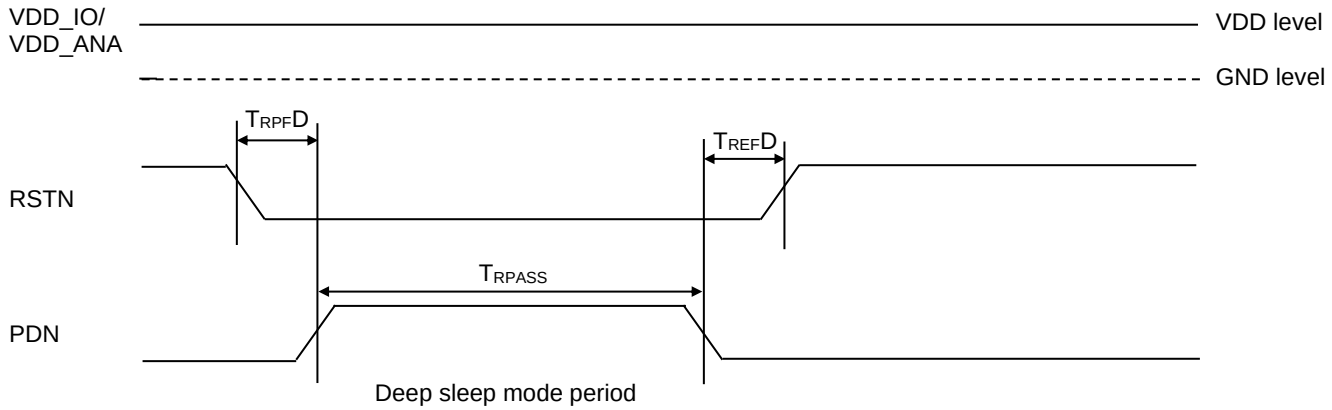


●Deep Sleep Mode Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PDN rising edge delay time	T_{RPFD}	VDD_IO/VDD_ANA ="H"	10	-	-	ms
PDN assert time (Deep sleep mode period)	T_{RPASS}	VDD_IO/VDD_ANA ="H"	1.2	-	-	ms
RSTN release delay time	T_{REFD}	VDD_IO/VDD_ANA ="H"	1	-	-	ms

[Note]

All timing measurement points are at VDDIO* 20% and VDDIO*80%.

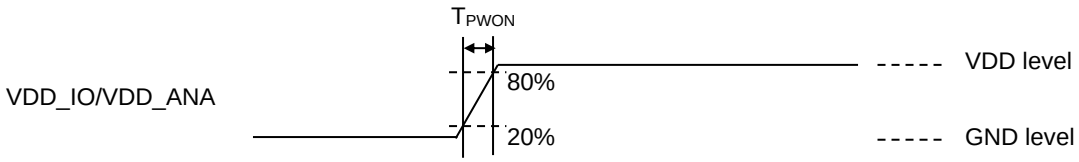


●Power-on Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power up time	T_{PWON}	Power on state (VDD_IO/VDD_ANA pin)	0.1	-	5	ms

[Note]

All timing measurement points are at VDDIO* 20% and VDDIO*80%.



■Revision History

Document No.	Issue Date	Page		Change Contents
		Previous Edition	Current Edition	
FEDL7425-01	2023/12/11	−	−	Initial release
FEDL7425-02	2024/03/19	1	1	Unify the names of radio stations and radio regulations
		7−8	7−9	Updating the reference circuit diagram and adding the common configuration circuit diagram
		12	13	Updating the maximum value of the power supply current characteristic
		22	23	Changed wording of Notes

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