Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML7436N

Sub-GHz/2.4GHz Narrowband/Wideband RF Tranceiver with Built-in MCU

■1. Overview

ML7436N is a LSI for Sub-GHz/2.4GHz narrowband/wideband radio communication, which integrates Microcontroller and RF Transceiver in a single chip.

●Product Name ML7436N-480ATB

●Application Remote control
Home, Building Security
Sensor Network
Smart Meters

Features:

- ◆ RF
  - Supported Standard
    - ✧ ARIB STD-T66, T67, T108
    - ✧ ETSI EN 300 220(Europe)
  - RF Frequency
    - ✧ 389 - 550MHz band
    - ✧ 778 - 1100MHz band
    - ✧ 2.4Ghzband
  - Realize high resolution modulation by using fractional N type PLL direct modulation
  - Modulation： 4GFSK/4GMSK, GFSK/GMSK, 4FSK/FSK/MSK
    (MSK is FSK at modulation index =0.5)
  - Data transmission rate:1.2kbps to 300 kbps
  - Data encoding/decoding by HW: NRZ, Manchester, 3-out-of-6
  - Data Whitening by HW
  - Programmable chnnel filters
  - Programmable frequency diviation function
  - TX/RX data inverse function
  - TCXO direct input supported
  - Programmable osillator's load capacitance

- Low speed clock adjustment function
- Frequency fine tuning function (using fractional N type PLL)
- On-chip TX PA
- TX POWER 20mW /10mW/1mW selectable function
- TX power tuning function(±0.2dB)
- TX power automatic ramping control
- External TX PA control function
- RSSI indicator and threshold judgment function
- High speed carrier checking function
- FEC function
- AFC function (IF frequency automatic adjustment by fractional N type PLL)
- Antenna diversity function
- Automatic Wake-up, auto SLEEP function
- General purpose timer(2ch)
- Test pattern generator(PN9, CW, 01 pattern、ALL"1"、ALL"0" output)
- Packet mode function
    - ✧ IEEE802.15.4g packet format (Format C)
    - ✧ Wireless M-Bus packet format(Format A/B)
    - ✧ General purpose packet format (Format C/D)
    - ✧ Max. 255byes (Format A/B), 2047bytes (Format C/D) packet length
    - ✧ TX FIFO(256bytes) , RX FIFO(256bytes)
    - ✧ RX preamble pattern detection(Max. 4bytes)
    - ✧ Automatic TX preamble length generator(Max 16383bytes)
    - ✧ SyncWord setting function(Max4bytes x2type)
    - ✧ Programable CRC function(CRC32/CRC16/CRC8 selectable, fully programmable polynomial)
    - ✧ Address checking function (Max 13Bytes x3)
      Wireless M-Bus field (C-field/M-field/A-field)
      IEEE802.15.4g (PANID/SHORT address/ 64bits address)

◆ MCU

- ARM®Cortex®-M3 RISC processor(maximum speed: 81MHz)
    - ✧ Memory Protection Unit(MPU)
    - ✧ SysTick Timer
    - ✧ Nested Vectored Interrupt Contoller (NVIC)
    - ✧ Embedded Trace Macro (ETM)

- 1MB Flash ROM
  - ✧ 512Kbytes ×2BANK
  - ✧ 32Kbytes within 1MByte can be used as data area
  - ✧ 1K erase cycles for program area/ 100K erase cycles for data aera, 10years data retention
  - ✧ Write Protection/Read Protection (Flash Control)

- 256KBytes RAM(Multi banks, controllable data retention function for each banks during low power mode, minimus 1kBytes retention)
- ECC function for 32KBytes of 256Kbytes
- True Random Number Generator (TRNG)
- Cryptograph Accellarator (CRYPTO)
  - ✧ AES(128/192/256bits, ECB/CBC/CFB/OFB/CTR/CCM/GCM/GMAC mode operation)
  - ✧ SHA-1/SHA-224/SHA-256
- Secure Key Storage
- Universal Asynchronous Receiver Transceiver (UART) (Max 3ch)
- Synchronous Serial Interface (SPI) (Max3ch)(1ch(SPI2) is for MCU/RF communication)
- Digital Interface for RFcontrol(DIO) (Max1ch)
- Watchdog Timer(WDT)
- General Purpose IO(GPIO)
- 32bit Timer ※4ch(Timer)
- Real Time Clock(RTC)
- 32bit Flexible Timer(auto-reload/Compare/PWM/Capture mode)(FTM) 6ch
- I2C
  Standard-Mode(100kHz)/ Fast-Mode(400kHz)/ Fast-Mode+(1MHz)/High Speed-Mode(3.4MHz)
- DMA Contoller (8ch)
- Serial Wire Debug Port(SWD)
- XTAL oscillator ※32.768KHz
- PLL 32.768KHz(Xtal oscilator) * 2475 or 64.86kHz(RF clockout)*1249
- Analog-to-Digital Converter (ADC) 10bits SAR, 120ksps, 1ch (extensible 3ch depending on package)
- Power-on Reset (POR)
- RC oscillator

◆ Supply Voltage 2.6V to 3.6V

◆ Operation Temperature -40°C to 85°C(Operation Guarantee)

- Current cosumption

TX	20mW	28.8mA(CPU=1.26MHz)
	1mW	12.8mA(CPU=1.26MHz)
RX		11.6mA (RF DCDC operation)

- Package

  48pin TQFP

  Lead-free package conforming to RoHS

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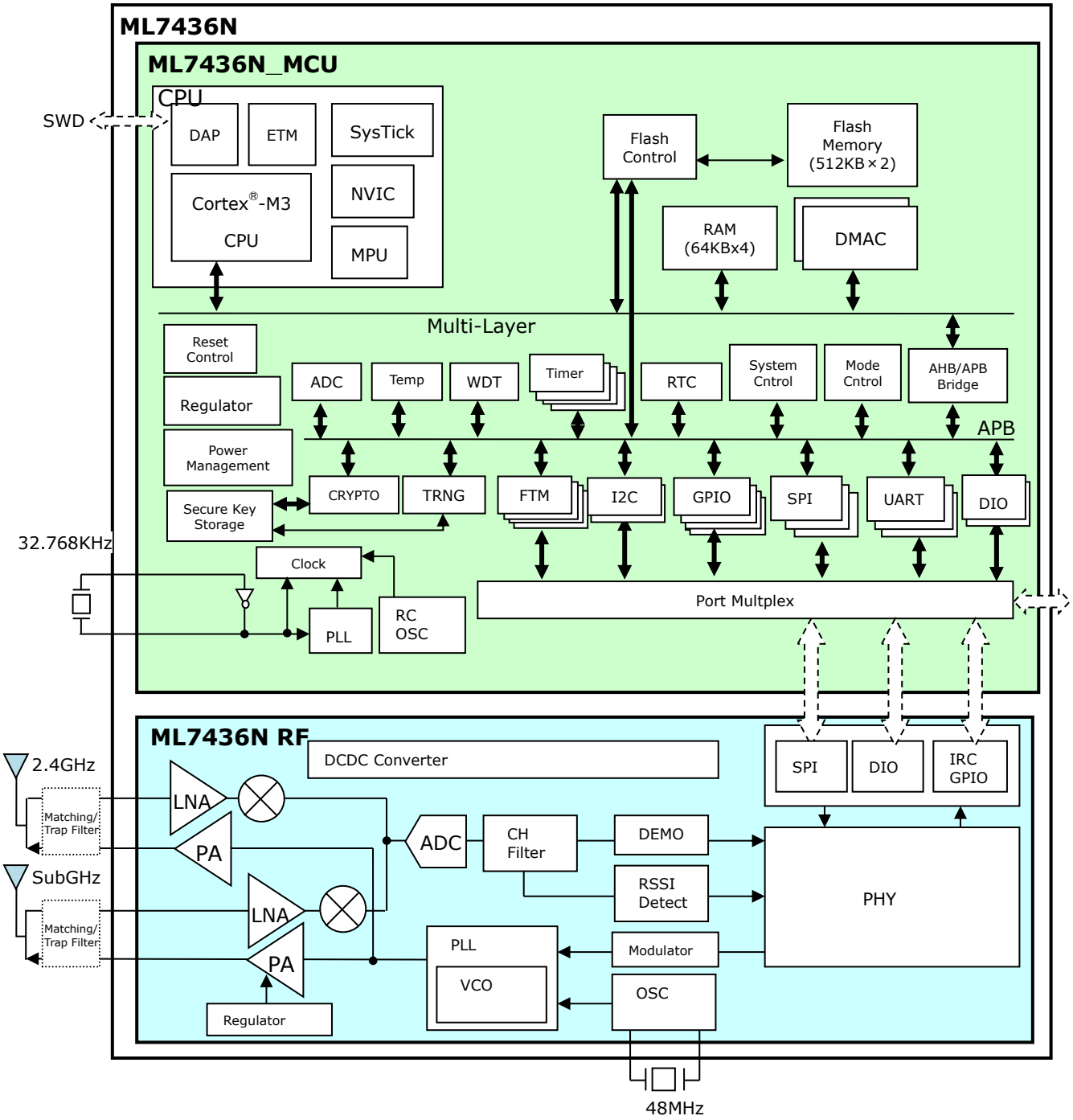
■2. Block Diagram



■3. Pin Layout

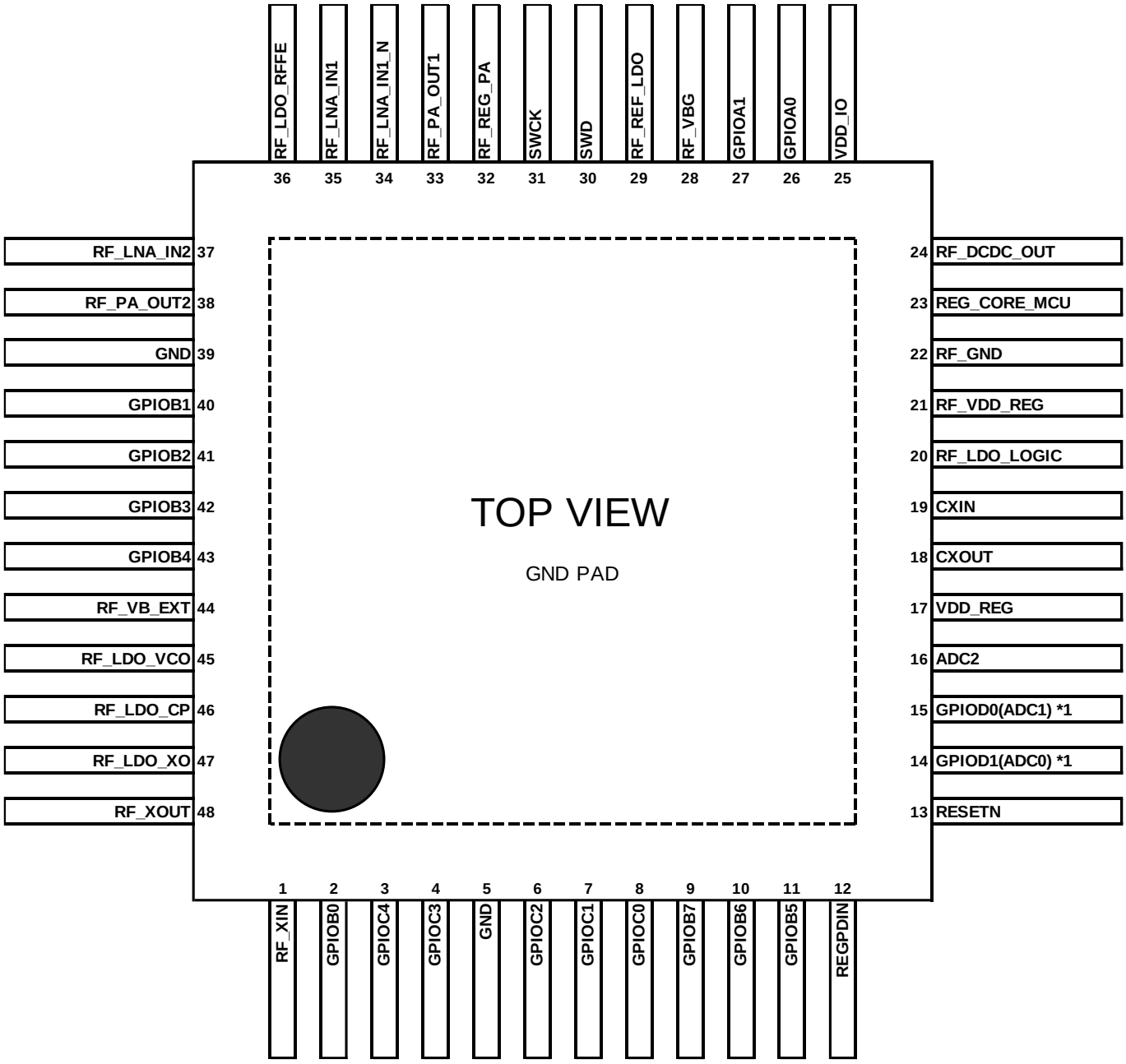


Table 3-1. Pin Table

No.	Port Name	1st Function	2nd Function	3rd Function	4th Function	5th Function	6th Function	7th Function
1	RF_XIN	RF_XIN	-	-	-	-	-	-
2	GPIOB0	GPIOB0	RF_GPIO2	-	FTMA	-	-	CLKOUT
3	GPIOC4	GPIOC4	UART0 RXD	SPI1 MISO	SPI01 MISO	I2C0 SCL	-	RF_SDO

Back Plane GND

4	GPIOC3	GPIOC3	UART0 TXD	SPI1 MOSI	SPI01 MOSI	I2C0 SDA	RF_GPIO4	RF_SDI
5	GND	-	-	-	-	-	-	-
6	GPIOC2	GPIOC2	UART1 RXD	SPI1 SCK	SPI01 SCK	I2C1 SCL	RF_GPIO5	RF_SCK
7	GPIOC1	GPIOC1	UART1 TXD	SPI1 SSN	FTMF	I2C1 SDA	I2C0 SDA	RF_SCEN
8	GPIOC0	GPIOC0	UART2 RXD	SPI0 SSN	FTME	I2C0 SCL	-	RF_SDO
9	GPIOB7	GPIOB7	UART2 TXD	SPI0 MISO	FTMD	I2C0 SDA	I2C1 SDA	RF_SDI
10	GPIOB6	GPIOB6	UART0 RXD	SPI0 MOSI	FTMC	I2C1 SCL	-	RF_SCK
11	GPIOB5	GPIOB5	UART0 TXD	SPI0 SCK	FTMB	I2C1 SDA	-	RF_SCEN
12	REGPDIN	REGPDIN	-	-	-	-	-	-
13	RESETN	RESETN	-	-	-	-	-	-
14	GPIOD1/ADC0 (*1)	GPIOD1	UART0 CTS	-	FTMF	I2C1 SCL	-	-
15	GPIOD0/ADC1 (*1)	GPIOD0	UART0 RTS	-	FTME	I2C1 SDA	-	-
16	ADC2	-	-	-	-	-	-	-
17	VDD_REG	-	-	-	-	-	-	-
18	CXOUT	CXOUT	-	-	-	-	-	-
19	CXIN	CXIN	-	-	-	-	-	-
20	RF_LDO_LOGIC	RF_LDO_LOGIC	-	-	-	-	-	-
21	RF_VDD_REG	RF_VDD_REG	-	-	-	-	-	-
22	RF_GND	RF_GND	-	-	-	-	-	-
23	REG_CORE_MCU	REG_CORE_MCU	-	-	-	-	-	-
24	RF_DCDC_OUT	RF_DCDC_OUT	-	-	-	-	-	-
25	VDD_IO (RF/MCU)	VDD_IO (RF/MCU)	-	-	-	-	-	-
26	GPIOA0	GPIOA0	RF_GPIO1	SPI2 MISO	FTMC	I2C0 SDA	ETM TRACEDATA0	-

27	GPIOA1	GPIOA1	RF_GPIO0	SPI2 SSN	FTMD	I2C0 SCL	ETM TRACECLK	-
28	RF_VBG	RF_VBG	-	-	-	-	-	-
29	RF_REF_LDO	RF_REF_LDO	-	-	-	-	-	-
30	SWD	SWD	GPIOA2	SPI2 MOSI	FTMB	I2C1 SCL	-	-
31	SWCK	SWCK	GPIOA3	SPI2 SCK	FTMA	I2C1 SDA	-	-
32	RF_REG_PA	RF_REG_PA	-	-	-	-	-	-
33	RF_PA_OUT1	RF_PA_OUT1	-	-	-	-	-	-
34	RF_LNA_IN1_N	RF_LNA_IN1_N	-	-	-	-	-	-
34	RF_LNA_IN1	RF_LNA_IN1	-	-	-	-	-	-
36	RF_LDO_RFFE	RF_LDO_RFFE	-	-	-	-	-	-
37	RF_LNA_IN2	RF_LNA_IN2	-	-	-	-	-	-
38	RF_PA_OUT2	RF_PA_OUT2	-	-	-	-	-	-
39	GND	-	-	-	-	-	-	-
40	GPIOB1	GPIOB1	UART2 TXD	SPI0 SSN	FTMD	I2C0 SCL	-	RF_RESET
41	GPIOB2	GPIOB2	UART2 RXD	SPI0 MISO	FTMC	I2C0 SDA	I2C1 SDA	RF_REGPDIN
42	GPIOB3	GPIOB3	UART1 TXD	SPI0 MOSI	FTMB	I2C1 SCL	I2C0 SCL	RF_GPIO2
43	GPIOB4	GPIOB4	UART1 RXD	SPI0 SCK	FTMA	I2C1 SDA	-	RF_GPIO3
44	RF_VB_EXT	RF_DSM_VREF	-	-	-	-	-	-
45	RF_LDO_VCO	RF_VB_EXT	-	-	-	-	-	-
46	RF_LDO_CP	RF_LDO_VCO	-	-	-	-	-	-
47	RF_LDO_XO	RF_LDO_CP	-	-	-	-	-	-
48	RF_XOUT	RF_XOUT	-	-	-	-	-	-

(*1) Those pins are configured as package option (ADC0/1 or GPIOD1/0). On GPIOD1/0 configured product, 1st-7th function can be used. On ADC0/1 configured products, they are analog input only.

■4. Pin Description

Input/Output definition

I	:Digital input
O	:Digital output
Is	:Schmitt trigger input
O_D	:Open drain
O_A	:Analog output
O_{AH}	:Analog output2
I_A	:Analog input
IO_A	:Analog inout
I_{RF}	:RF input
O_{RF}	:RF output
I_{OSL}	:32.768KHz osillator input
O_{OSL}	:32.768KHz osillator output

Input/Output attribute definition

I	:Input
O	:Output
oZ	:High-impedance output

4-1. Power/Ground

Pin	IO	Active Level	Attribute/Value At reset	Description
VDDIO	Power	-	-	Power supply for digital IO (2.6 to 3.6V)(MCU/RF common)
RF_GND	Ground	-	-	Ground for RF.
GND	Ground	-	-	Common Ground

4-2. Regulator Interface

Pin	IO	Active Level	Attribute/Value At reset	Description
REGPDIN	I	H	I / -	Regulator power down control(Fixed to Low in normal operation)
VDD_REG	-	-	-	Power supply for Regulator (Typ: 3.3V)(MCU)
REG_CORE_MCU	-	-	-	Regulator output(Typ: 1.2V)(MCU)
RF_VBG	-	-	-	C connect pin(RF)
RF_DCDC_OUT	-	-	-	Switching regulator output (RF)
RF_VDD_REG	-	-	-	Switching regulator input(RF)
RF_REG_PA	-	-	-	PA regulator output (RF)
RF_REF_LDO	-	-	-	Linear regulator reference voltage output(RF)
RF_LDO_RFFE	-	-	-	RFFR circuit Linear regulator output(RF)
RF_LDO_CPO	-	-	-	CP circuit Linear regulator output(RF)
RF_LDO_VCO	-	-	-	VCO circuit Linear regulator output(RF)
RF_LDO_XO	-	-	-	Oscillator circuit Linear regulator output(RF)
RF_LDO_LOGIC	-	-	-	Logic circuit Linear regulator output(RF)

4-3. RF Interface

Pin	IO	Active Level	Attribute/Value At reset	Description
RF_PA_OUT1	O_{RF}	-	-	RF Antenna output pin (160M - 920MHz)
RF_LNA_IN1	I_A	-	I / -	RF Antenna input pin (160M - 920MHz)
RF_LNA_IN1_N	I_A	-	I / -	RF Antenna input pin (160M - 920MHz)
RF_PA_OUT2	O_{RF}	-	-	RF Antenna output pin (2.4GHz)
RF_LNA_IN2	I_A	-	I / -	RF Antennainput pin (2.4GHz)
RF_VB_EXT	I_{OA}	-	-	Internal bias smoothing capacitor connection pin

4-4. MCU Interface

Pin	IO	Active Level	Attribute/Value At reset	Description
GPIOA0	I/O	-	oZ / -	1st : General Purpose IO(GPIOA0)
	O	-	-	2nd : RF General Purpose IO(RF_GPIO1)(Clock out)
	I/O	-	-	3rd : SPI2 MISO
	I/O	-	-	4th : Flexible TimerC I/O (FTMC_IO)
	I/O_D	-	-	5th : I2C0 serial data (I2C0 SDA)
	O	-	-	6th : ETM TRACEDATA0
GPIOA1	I/O	-	oZ / -	1st : General Purpose IO(GPIOA1)
	O	-	-	2nd : General Purpose IO (RF_GPIO0)(SINTN)
	I/O	L	-	3rd : SPI2 SSN
	I/O	-	-	4th : Flexible TimerD I/O (FTMD_IO)
	I/O_D	-	-	5th : I2C0 serial clock(I2C0 SCL)
	O	-	-	6th : ETM TRACECLK
SWD	I/O	-	I / -	1st : Serial wire debug port data(SWD)
	I/O	-	-	2nd : General Purpose IO(GPIOA2)
	I/O			3rd : SPI2 MOSI
	I/O			4th : Flexible TimerB I/O (FTMB_IO)
	I/O_D	-	-	5th : I2C1 serial clock(I2C1 SCL)
SWCK	I/O	-	I / -	1st : Serial wire debug port clock(SWCK)
	I/O	-	-	2nd : General Purpose IO(GPIOA3)

	I/O	-	-	3rd : SPI2 SCK
	I/O			4th : Flexible TimerA I/O (FTMA_IO)
	I/OD	-	-	5th : I2C1 serial data(I2C1 SDA)
GPIOB0	I/O	-	I / -	1st : General Purpose IO (GPIOB0) Use this pin for MCU mode detection during power on reset sequence. L level at power on: normal mode H Level at power on: ISP mode
GPIOB1	I/O	-	oZ / -	1st : General Purpose IO (GPIOB1)
	O	L	-	2nd : UART2 transmit data(UART2_TXD)
	I/O	L	-	3rd : SPI0 SSN
	I/O	-	-	4th : Flexible TimerD I/O（FTMD_IO）
	I/OD	-	-	5th : I2C0 serial clock(I2C0 SCL)

Pin	IO	Active Level	Attribute/Value At reset	Description
GPIOB2	I/O	-	oZ / -	1st : General Purpose IO (GPIOB2)
	I	-	-	2nd : UART2 receive data(UART1_TXD)
	I/O	-	-	3rd : SPI0 MISO
	I/O	-	-	4th : Flexible TimerC I/O（FTMC_IO）
	I/OD	-	-	5th : I2C0 serial data(I2C0 SDA)
	I/OD	-	-	6th : I2C1 serial data(I2C1 SDA)
GPIOB3	I/O	-	oZ / -	1st : General Purpose IO (GPIOB3)
	O	-	-	2nd : UART1 transmit data(UART1_TXD)
	I/O	-	-	3rd : SPI0 MOSI
	I/O	-	-	4th : Flexible TimerB I/O（FTMB_IO）
	I/OD	-	-	5th : I2C1 serial clock(I2C1 SCL)
	I/OD	-	-	6th : I2C0 serial clock(I2C0 SCL)
GPIOB4	I/O	-	oZ / -	1st : General Purpose IO (GPIOB4)
	I	-	-	2nd : UART1 receive data(UART1_RXD)
	I/O	-	-	3rd : SPI0 SCK
	I/O	-	-	4th : Flexible TimerA I/O（FTMA_IO）
	I/OD	-	-	5th : I2C1 serial data(I2C1 SDA)
GPIOB5	I/O	-	oZ / -	1st : General Purpose IO (GPIOB5)
	O	-	-	2nd : UART0 transmit data(UART0_TXD)

	I/O	-	-	3rd : SPI0 SCK
	I/O	-	-	4th : Flexible TimerB I/O（FTMB_IO）
	I/OD	-	-	5th : I2C1 serial data(I2C1 SDA)
GPIOB6	I/O	-	oZ / -	1st : General Purpose IO (GPIOB6)
	I	-	-	2nd : UART0 receive data(UART0_RXD)
	I/O	-	-	3rd : SPI0 MOSI
	I/O	-	-	4th : Flexible TimerC I/O（FTMC_IO）
	I/OD	-	-	5th : I2C1seridal clock(I2C1 SCL)
GPIOB7	I/O	-	oZ / -	1st : General Purpose IO (GPIOB7)
	O	-	-	2nd : UART2 transmit data (UART2_TXD)
	I/O	-	-	3rd : SPI0 MISO
	I/O	-	-	4th : Flexible TimerD I/O（FTMD_IO）
	I/OD	-	-	5th : I2C0 serial data(I2C0 SDA)
	I/OD	-	-	6th : I2C1 serial data(SDA)

Pin	IO	Active Level	Attribute/Value At reset	Description
GPIOC0	I/O	-	oZ / -	1st : General Purpose IO(GPIOC0)
	I	-	-	2nd : UART2 receive data(UART2_RXD)
	I/O	L	-	3rd : SPI0 slave select(SPI0_SSN)
	I/O	-	-	4th : Flexible TimerE I/O（FTME_IO）
	I/OD	-	-	5th : I2C0 serial clock(I2C0_SCL)
GPIOC1	I/O	-	oZ / -	1st : General Purpose IO(GPIOC1)
	O	-	-	2nd : UART1 transmit data(UART1_TXD)
	I/O	L	-	3rd : SPI1 slave select(SPI1_SSN)
	I/O	-	-	4th : Flexible TimerF I/O（FTMF_IO）
	I/OD	-	-	5th : I2C1 serial data(I2C1_SDA)
	I/OD	-	-	6th : I2C0 serial data(I2C0_SDA)
GPIOC2	I/O	-	oZ / -	1st : General Purpose IO(GPIOC2)
	I	-	-	2nd : UART1 receive data（UART1_RXD）
	I/O	-	-	3rd : SPI1 serial clock(SPI1_SCK)
	I/O	-	-	4th : SPI0/SPI1 shared serial clock(SPI01_SCK)
	I/OD	-	-	5th : I2C1 serial clock(I2C1_SCL)
GPIOC3	I/O	-	oZ / -	1st : General Purpose IO(GPIOC3)
	O	-	-	2nd : UART0 transmit data（UART1_TXD）

	I/O	-	-	3rd：SPI1 Master Out/Slave In(SPI1_MOSI)
	I/O	-	-	4th：SPI0/SPI1 shared Master Out/Slave In(SPI01_MOSI)
	I/OD	-	-	5th：I2C1 serial data(I2C1_SDA)
GPIOC4	I/O	-	oZ / -	1st：General Purpose IO(GPIOC4)
	O	L	-	2nd：UART0 receive data(UART0_RXD)
	I/O	-	-	3rd：SPI1 Master In/Slave Out（SPI1_MISO）
	I/O	-	-	4th ：SPI0/SPI1 shared Master In/Slave Out（SPI01_MISO）
	I/OD	-	-	5th：I2C0 serial clock (I2C0_SCL)

Pin	IO	Active Level	Attribute/Value At reset	Description
GPIOD0	I/O	-	oZ / -	1st：General Purpose IO(GPIOD0)
	O	L	-	2nd：UART0 request to send(UART0_RTS)
	I/O	-	-	4th：Flexible TimerE I/O（FTME_IO）
	I/OD	-	-	5th：I2C1 Serial data(I2C0_SDA)
GPIOD1	I/O	-	oZ / -	1st：General Purpose IO(GPIOD1)
	I	L	-	2nd：UAR01 Clear to send(UART0_CTS)
	I/O	-	-	4th：Flexible TimerF I/O（FTMF_IO）
	I/OD	-	-	5th：I2C1 serial clock(I2C0_SCL)

4-5. Others

Pin	IO	Active Level	Attribute/Value At reset	Description
RESETN	IS	L	I / -	RESET
RF_XIN	IA	P or N	I / -	48MHz Xtal Oscillator(IN)(RF)
RF_XOUT	OA	P or N	-	48MHz Xtal Oscillator(OUT)(RF)
CXIN	Ios	P or N	I	32.768kHz Xtal Oscillator(IN)(MCU)
CXOUT	Oos	P or N	O	32.768kHz Xtal Oscillator(OUT)(MCU)
ADC2	IA	-	I / -	ADC input

4-6. Handling of Unused pins

See below for handling of unused pins.

Pin name	Recommended treatment
SWCK/SWD	Connect pull-down or pull-up register (*2)
GPIOB0	Connect pull-down register or Tie Low(*1)
GPIO*(except GPIB0)	open
ADC2	open
XIN	open (To be used when the TCXO is connected)

(*1)

Connect Ground or small pull-down register in order to stable Low level during power-on sequence.

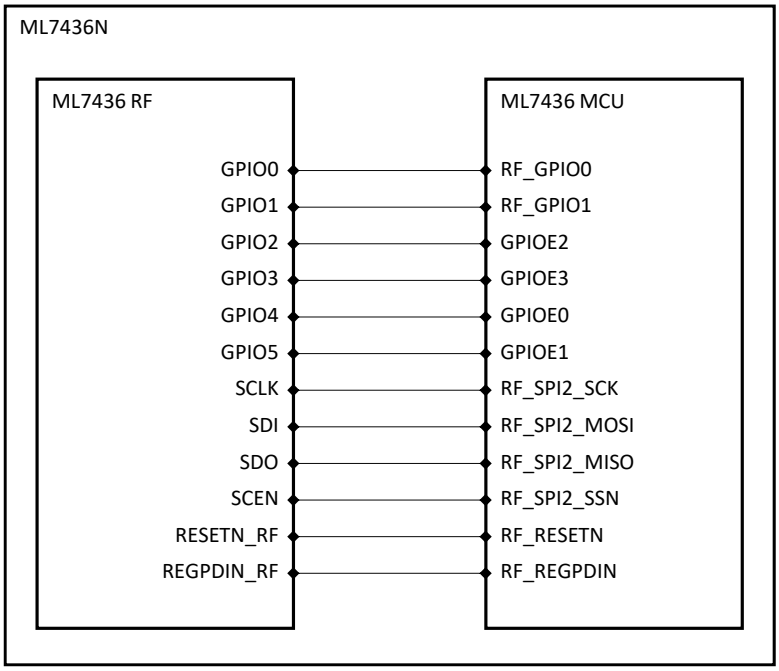
(*2)

Connect pull-up or pull-down register.

4-7. Internal pins

ML7436N is configured by RF and MCU. This chapter explains the internal pins.

The following figure shows each chips connection.



4-7-1. MCU

Pin	IO	Active Level	Attribute/Value At reset	Description
RF_GPIO0	I	-	oZ / -	1st : External interrupt input pin (EXTINT function)
	I/O	-	-	4th : General purpose IO (GPIOF0)
RF_GPIO1	I	-	oZ / -	1st : External interrupt input pin (EXTINT function)
	I/O	-	-	4th : General purpose IO (GPIOF1)
GPIOE2	I	-	oZ / -	1st : External interrupt input pin (EXTINT function)
	I/O	-	-	4th : General purpose IO (GPIOF2)
GPIOE3	I	-	oZ / -	1st : External interrupt input pin (EXTINT function)
	I/O	-	-	4th : General purpose IO (GPIOF3)
GPIOE0	I	-	oZ / -	1st : External interrupt input pin (EXTINT function)
	I/O	-	-	2ns : DIO0 DATA
	I/O	-	-	4th : General purpose IO (GPIOF4)
GPIOE1	I	-	oZ / -	1st : External interrupt input pin (EXTINT function)
	I	-	-	2nd : DIO0 CLK
	I/O	-	-	4th : General purpose IO (GPIOF5)
RF_SPI2_SCK	I/O	-	O/L	1st : SPI2 SCK
RF_SPI2_MOSI	I/O	-	O/L	1st : SPI2 MOSI
	I/O	-	-	2nd : DIO0 DATA
RF_SPI2_MISO	I/O	-	oZ / -	1st : SPI2 MISO
	I	-	-	2nd : DIO0 CLK
RF_SPI2_SSN	I/O	-	O/H	1st : SPI2 SSN
RF_RESETN	O	-	O/L	RF chip reset control pin
RF_REGPDIN	O	-	O/L	RF chip regulator power down control pin

4-7-2. RF

Pin	IO	Active Level	During the RF resetting	The initial value after RF resetting	Description

GPIO0	I/O	H or L or OD	oZ/-	O/L	Digital input/output pin Initial function: Interrupt notification signal output
GPIO1	I/O	H or L or OD	oZ/-	O/Clock	Digital input/output pin Initial function: Clock out
GPIO2	I/O	H or L or OD	oZ/-	O/Clock	Digital input/output pin Initial function: Antenna switching control signal output
GPIO3	I/O	H or L or OD	oZ/-	O/L	Digital input/output pin Initial function: TX/RX switching signal output
GPIO4	I/O	H or L or OD	oZ/-	O/L	Digital input/output pin Initial function: Data (DIO DATA)
GPIO5	I/O	H or L or OD	oZ/-	O/H	Digital input/output pin Initial function: Data (DIO DCLK)
SCLK	Is	-	oZ/-	I	SPI clock input pin
SDI	Is	-	oZ/-	I	SPI data input pin / DIO DATA pin
SDO	O	-	oZ/-	I	SPI data output pin / DCLK output pin * OpenDrain output is the initial setting. Set SDO_OD([SPI/EXT_PA_CTRL:B0 0x53(7)])=0b0 when SDO pin is used as output pin before SPI reading operation.
SCEN	Is	L	oZ/-	I	SPI chip enable pin L: Enable H: Disable
RESETN_RF	Is	L	I	I	Reset pin L: Operation stop H: Executable *LSI is reset when RESETN_RF is set to "L" Set "L" when RF set DEEPSLEEP
REGPDIN_RF	Is	H	I	I	Regulator power down control pin *Set "L" at normal operation. Set "H" when RF set DEEPSLEEP

4-7-3. Handling of Unused pins (Internal pins)

Handling of unused pins

Pin name	Recommended treatment
RF GPIO0	MCU RF_GPIO0=oZ(default)
RF GPIO1	MCU RF_GPIO1=oZ(default)
RF GPIO2	MCU GPIOE2=oZ(default)
RF GPIO3	MCU GPIOE3=oZ(default)
RF GPIO4	MCU GPIOE0=oZ(default)
RF GPIO5	MCU GPIOE1=oZ(default)

<Note>

*1. GPIO1 pin's initial state is clock output (CLK_OUT function). When the clock output function is unnecessary, set [GPIO1_CTRL: B0 0x4F] bit2-0=0b000. The setting stops clock output.
RF GPIO1 pin's state is clock output and MCU is set to open, it causes RF receive sensitivity deterioration.

■5. Electrical Characteristics

5-1. Absolute Maximum Ratings

Under Ta=-40 to +85°C, GND=0V, if any special condition is not described.

Item	Symbol	Conditions	Rating	Unit
Power supply I/O (*1)	VDDIO	−	-0.3 to +4.6	V
RF input voltage	PRFI	Antenna input at RX	0	dBm
RF output voltage	VRFO	−	-0.3 to +4.6	V
Digital input voltage	VDIN	−	-0.3 to 5.8	V
Analog input voltage(*2)	VAIN	−	-0.3 to 1.8	V
Digital output voltage	VDO	−	-0.3 to 4.6	V
Analog output	VAO	−	-0.3 to 1.8	V
Analog output voltage2	VAO2	−	-0.3 to 4.6	V
Digital input current	IDI	−	-10 to +10	mA
Analog input current (*2)	IAI	−	-2 to +2	mA
Digital output current	IDO	−	-8 to +8	mA
Analog output current(*3)	IAO	−	-2 to +2	mA
Analog output current2	IAO2	−	-2 to +2	mA
Power dissipation	PD	Ta=+25°C	1	W
Storage Temperature	Tstg	−	-55 to +150	°C

(*1) VDDIO_MCU、VDD_REG_MCU

(*2) RF_XIN、CXIN

(*3) RF_XOUT、CXOUT

5-2. Recommended operation conditions

Item	Symbol	Conditions	MIN	TYP	MAX	UNIT
Power supply voltage(I/O) VDDIO and VDD_REG_MCU	VDDIO		2.6	3.3	3.6	V
Operating temperature	Ta	-	-40	+25	+85	°C
Digital input rise time	tIR1	Digital input (*1)	-	-	20	ns
Digital input fall time	tIF1	Digital input (*1)	-	-	20	ns
Digital output load	CDL	All digital output pin	—	—	20	pF
Slow Clock 32.768kHz Xtal Frequency	FXCK1	CXIN,CXOUT	-20ppm (*2)	32.768	+20ppm (*2)	kHz
IOSC Clock Internal high-speed RC	FICK1		-10%	16	+10%	MHz
IOSC Clock Internal low-speed RC	FICK2		-10%	32	+10%	kHz
RF Master Frequency	FMCK1	RF_XIN/RF_XOUT	30	48	52	MHz
RF Master clock Acculancy	ACMCK1		(*4)	(*4)	(*4)	ppm
RF Xtal Equivalent series resistance	Esr		—	—	80	ohm
RF channel Frequency	FRF	-	389	—	80	MHz
			778	—	1100	MHz
			2402.0	—	2483.5	MHz

(*1) Pins described as I or Is in the Input/output column in "Pin Description".

(*2) These values are provided under the condition of 25 °C. Under the condition of -40 to 85 °C, the maximum value is +150 ppm, and the minimum value -150 ppm.

(*3) In case of TX operation, this value is specified by minimum value of VDDIO.

(*4) Indicating frequency deviation during TX-RX operation. In order to support various standards, apply the frequency accuracy for each standard to meet the requirements as described below.

Specification	Required Accuracy
ARIB STD-T108	±20 ppm
RCR STD-30 type III (Japan)	±10 ppm
RCR STD-30 type IV (Japan)	±4 ppm
Wireless M-Bus F mode	±16 ppm

[Notices]

The electrical characteristics are measured under the recommended operating conditions above, unless otherwise specially noted.

The timings are measured at the 20 % and 80 % levels of VDDIO, unless otherwise specially noted.

5-3. Common Characteristics

Item	Symbol	Conditions/Pins	MIN	TYP(*2)	MAX(*11)	Unit
Supply Current(*1)	IDD_IDLE	MCU : Active (*10) RF : RF Sleep state 1	—	1.3	9.9	mA
	IDD_RX	MCU : Active(*10) RF : RX Operation (*5)(*6)	-	11.6	32.3	mA
		MCU : Active(*10) RF : RX Operation (*5)(*7)	-	17.9	33.9	mA
	IDD_TX1	MCU : Active(*10) RF : TX Operation(1mW) (*5) (*6)	-	12.8	39.5	mA
	IDD_TX20	MCU : Active(*10) RF : TX Operation(20mW) (*5) (*6)	-	28.8	67.5	mA
		MCU : Active(*10) RF : TX Operation(20mW) (*5) (*6)	-	44.3	67.5	mA
		MCU : Active(*10) RF : TX Operation(20mW) (*5) (*7)	-	39.3	69.5	mA
High level input voltage (*12)	VIH1	Digital input	VDDIOx0.75	—	5.5	V
High level input voltage (*13)	VIH2	Digital input	VDDIOx0.75	—	VDDIO	V
Low level input voltage	VIL1	Digital input	0	—	VDDIOx0.18	V
Schmitt trigger high level decision threshold value	VT+	Digital pin with schmit trigger	—	—	VDDIOx0.75	V

Schmitt trigger low level decision threshold value	VT-	Digital pin with schmit trigger	VDDIOx0.18	—	—	V
Input leakage Current	IIH1	Digital input	-1	—	1	μA
	IIH2	XIN, CXIN	-0.3	—	0.3	μA
	IIL1	Digital input	-1	—	1	μA
	IIL2	XIN, CXIN	-0.3	—	0.3	μA
Tri-state Output leakage Current	IOZH1	Digital I/O	-1	—	1	μA
	IOZL1	Digital I/O	-1	—	1	μA
High level output voltage	VOH	3.0V≦VDDIO≦3.6V	VDDIOx0.75	—	VDDIO	V
		PIN2,PIN1=0,0 IOH=-3.5mA				
		PIN2,PIN1=0,1 IOH=-7.0mA(*19)				
		PIN2,PIN1=1,1 IOH=-14.0mA(*4) IOH=-9.0mA(*16) (*20)				
		2.6V≦VDDIO<3.0V				
		PIN2,PIN1=0,0 IOH=-1.25mA				
		PIN2,PIN1=0,1 IOH=-2.5mA(*19)				
		PIN2,PIN1=1,1 IOH=-5.0mA(*20)				
Low level output voltage	VOL	3.0V≦VDDIO≦3.6V	0	—	0.55	V
		PIN2,PIN1=0,0 IOL=3.5mA				
		PIN2,PIN1=0,1 IOL=7.0mA(*19)				
		PIN2,PIN1=1,1 IOL=14.0mA(*20)				

		2.6V≦VDDIO<3.0V PIN2,PIN1=0,0 IOH=1.25mA	0	—	0.45	
		2.6V≦VDDIO<3.0V PIN2,PIN1=0,1 IOH=2.5mA(*19)				
		2.6V≦VDDIO<3.0V PIN2,PIN1=1,1 IOH=5.0mA(*20)				
Pin capacitance	CIN	Input (*14)	—	6	—	pF
	CIO	Inout(*15)	—	9	—	pF
	CAI	Analog input	—	20	—	pF

(*1) The power supply current is the total current of all power supply pins.

(*2) The "Typ." value is the center value under the condition of VDDIO = 3.3 V and 25 °C.

(*3) Under the condition 25°C for both Typ and Max.

(*4) Applied to GPIOA0,GPIOA1. Default drive strength is under the conditionPIN2,PIN1=0,0 and can beconfigured by IO set registers.

(*5) Data rate is 100kbps.

(*6) With DCDC. Then, minimum supply voltage is 2.6v.

(*7) Without DCDC.

(*8) With DCDC and Changing PA Voltage Supply.

(*9) 32.768kHz Xtal osillator, RTC operation, SRAM(1KB[BANK4]) retension.

(*10) MCU=81.1MHz、FCLK_DIV=64 division, All peripheral clocks are disabled (All existing bits of SYSCON_PCLK_DIS, SYSCON_EPCLK_DIS, SYSCON_SPCLK_DIS are "1".)

(*11) For supply current characteristics, Worst value under the conditoin VDD=3.3v.

(*12) All GPIOs except GPIOB0,GPIOD0 and GPIOD1.

(*13) All digital ports except (*12).

(*14) REGPDIN, RESETN

(*15) All digital ports except (*14).

(*16) Applied to all GPIOs except (*4). Default setting is under the condition PIN2,PIN1=0,0 and can beconfigured by IO set registers.

(*19) PIN2,PIN1=0,1 Simultaneous switching pins are under 5 pins.

(*20) PIN2,PIN1=1,1 Simultaneous switching pins are under 1 pins.

5-4. RF Characteristics

Modulated Data Rate	:	1.2kbps to 300kbps
Modulation fomats	:	2/4-level GFSK/FSK
Rx Bandwidth	:	Up to 600kHz

The measurement point is at antenna end specified in the recommended circuits.

5-4-1 [TX characteristics]

Value is under condition of the master clock frequency = 48MHz (Typ.).

5.4.1.1 ○400MHz Band

Item	Condition		Min	Typ	Max	Unit
TX power	20mW (13dBm) (*2) After power adjustment		10	13	13.8	dBm
	10mW (10dBm) (*2) After power adjustment		7	10	10.8	dBm
	1mW (0dBm) (*2) After power adjustment		-3	0	0.8	dBm
Programmable frequency deviation [Fdev] (*1)	-		0.025	-	400	kHz
Occupied bandwidth	99% power bandwidth, PN9 4.8kbps mode (*2) Modulation frequency deviation = ±2.4kHz		-	-	8.5	kHz
Adjacent channel leakage power [ACPR]	PN9, 4.8kbps mode, Modulation frequency deviation = ±2.4kHz Leakage power in 12.5kHz offset ± 8.5kHz bandwidth		-	-	-40	dBc
Spurious emission	10dBm TX Data rate: 4.8kbps (*2), PN9, 2.4kHz deviation, 62.5k to 162.5kHz offset integration value		-	-	-26	dBm
	Harmonics (*2) 10dBm CW TX (Note) With LC trap circuit	2^{nd} 3^{rd} <	-	-	-36 -30	dBm

*1 Depends on the master clock frequency.

*2 For 426MHz.

5.4.1.2 ○868M/920MHz Band

Item	Condition		Min	Typ	Max	Unit
TX power	20mW (13dBm)		9	13	15	dBm
	10mW (10dBm)		6	10	12	dBm
	1mW (0dBm)		-6.5	0	7.5	dBm
Programmable frequency deviation [Fdev] (*1)	-		0.025	-	400	kHz
Occupied bandwidth	99% power bandwidth, PN9 100kbps mode Modulation frequency deviation = ±50kHz		-	-	200	kHz
Adjacent channel leakage power [ACP]	PN9, 100kbps mode, TX power = 13dBm, Modulation frequency deviation = ±50kHz Leakage power in 300kHz offset ± 100kHz bandwidth		-	-	-20	dBm
Spurious emission	20mW (13dBm) adjustment, Data rate:100kbps, 50kHz deviation, Pattern:PN9, (*2)	710MHz ≥	-	-	-36	dBm/100kHz
		710-900MHz	-	-	-55	dBm/1MHz
		900-915MHz	-	-	-55	dBm/100kHz
		915-930MHz	-	-	-36	dBm/100kHz
		930-1000MHz	-	-	-55	dBm/100kHz
		1000-1215MHz	-	-	-45	dBm/1MHz
		1215MHz <	-	-	-30	dBm/1MHz
	Harmonics (2^{nd}/ 3^{rd}) 13dBm CW TX (Note) With LC trap circuit		-	-35	-30	dBm

*1 Depends on the master clock frequency.

*2 For 920MHz band.

5.4.1.3 ○2.4GHz Band

Item	Condition	Min	Typ	Max	Unit
TX power	1mW (0dBm)	-4	0	4	dBm
Programmable frequency deviation [Fdev] (*1)		0.025	-	400	kHz
Occupied bandwidth	99% power bandwidth, PN9 100kbps mode Modulation frequency deviation = ±50kHz setting	-	180	-	kHz
Spurious emission	Harmonics (2^{nd}/ 3^{rd}) 0dBm CW TX (Note) With LC trap circuit	-	-29	-26	dBm

*1 Depends on the master clock frequency.

5.4.2[RX characteristics]

5.4.2.1 ○400MHz Band

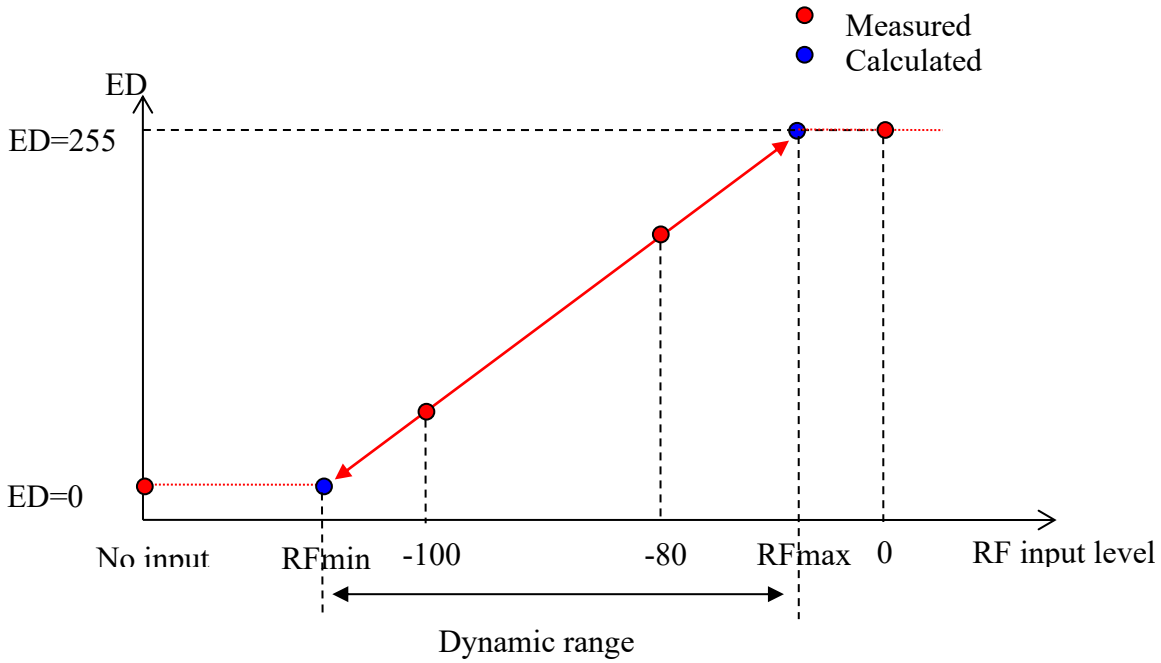
Item	Condition		Min	Typ	Max	Unit
Sensitivity	4.8kbps mode Center frequency 426MHz BER<1%, GFSK, 2.4kHz deviation	FREF =48MHz	-	-120.5	-112.0	dBm
	9.6kbps mode Center frequency 426MHz BER<1%, GFSK, 4.8kHz deviation	FREF =48MHz	-	-116.5	-109	dBm
Adjacent channel rejection ratio (*1)	12.5kHz spacing, Ta = 25°C, 4.8kbps mode Center frequency 426MHz Undesire: PN9	FREF =48MHz	30	33	-	dB
	25kHz spacing, Ta = 25°C, 9.6kbps mode Center frequency 426MHz Undesire: PN9	FREF =48MHz	30	33	-	dB
Blocking (*1)	2MHz offset, Ta = 25°C, 4.8kbps mode Center frequency 426MHz	FREF =48MHz	-	73	-	dB
	10MHz offset, Ta = 25°C, 4.8kbps mode Center frequency 426MHz	FREF =48MHz	-	82	-	dB
	-IF frequency*2[Hz] offset (image frequency) , Ta=25℃, after IQ adjustment	FREF =48MHz	30	50	-	dB
Minimum power detection level (ED value)	RFmin in RSSI characteristics diagram (*2) 4.8kbps, Center frequency 426MHz Channel filter band = 10kHz setting	FREF =48MHz	-	-115	-105	dBm

Item	Condition		Min	Typ	Max	Unit
ED dynamic range	Dynamic range in ED characteristics diagram (*2)	FREF =48MHz	60	65	-	dB
Spurious emission		FREF =48MHz	-	-	-54	dBm

*1 Adjacent channel rejection ratio and Blocking measurement condition is as follows.
Desired signal level is set to receiver sensitivity level (BER=1%)+3dB.
By sweeping undesired signal level, search the undesired signal level at BER=1%.
U/D[dB]= (undesired signal level) - (sensitivity level(BER=1%))

*2 The following diagram shows the RSSI characteristics.

(Note)
If channel frequency is the neighborhood to multiply of the reference clock frequency or the neighborhood to 2 dividing of the reference clock frequency or the neighborhood to 4 dividing of the reference clock frequency, they may cause a deterioration of RX characteristics.



RSSI characteristics

5.4.2.2 ○868M/920MHz Band

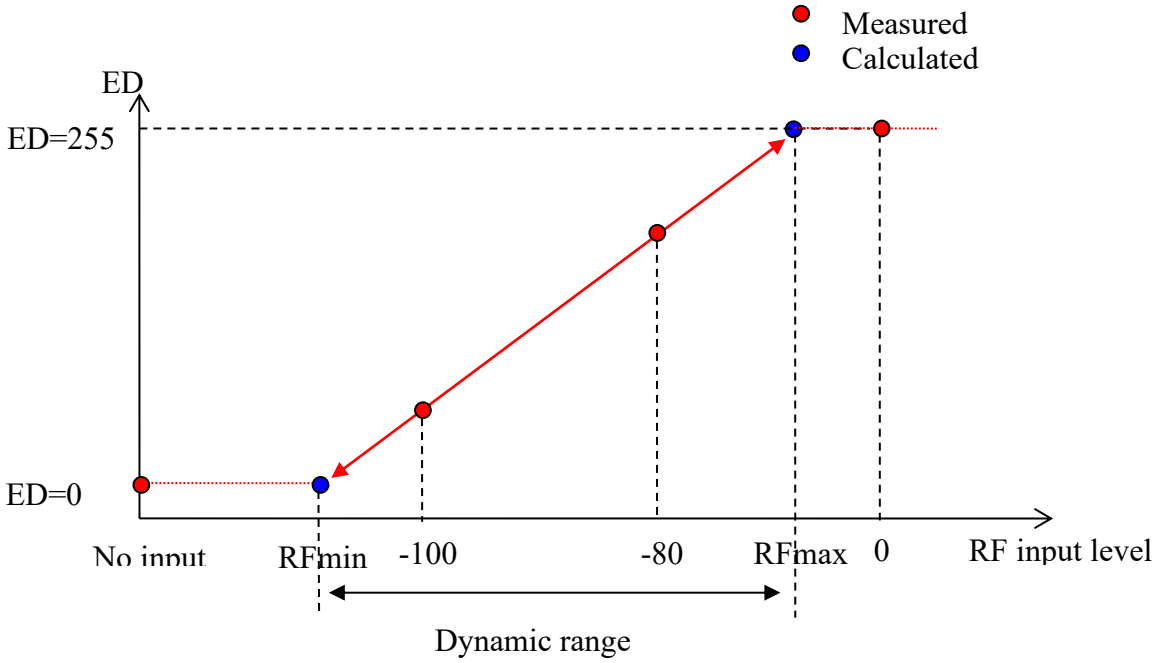
Item	Condition			Min	Typ	Max	Unit
Sensitivity	100kbps mode Center frequency 920.7MHz BER<0.1%, GFSK, 50kHz deviation		FREF =48MHz	-	-105	-98	dBm
Adjacent channel rejection ratio (*1)	Ta = 25°C, 100kbps mode Center frequency 920.7MHz Undesire: CW	+400kHz	FREF =48MHz	25	40	-	dB
		-400kHz	FREF =48MHz	22	37	-	dB
Blocking (*1)	2MHz offset, Ta = 25°C, 100kbps mode Center frequency 920.7MHz		FREF =48MHz	36.5	55	-	dB
	10MHz offset, Ta = 25°C, 100kbps mode Center frequency 920.7MHz		FREF =48MHz	41.5	65	-	dB
Minimum power detection level (ED value)	RFmin in RSSI characteristics diagram (*2) 100kbps, Center frequency 920.7MHz Channel filter band = 200kHz setting		FREF =48MHz	-	-106	-100	dBm
ED dynamic range	Dynamic range in ED characteristics diagram (*2) 100kbps, Center frequency 920.7MHz		FREF =48MHz	60	65	-	dB
Spurious emission			FREF =48MHz	-	-	-57	dBm

*1 Adjacent channel rejection ratio and Blocking measurement condition is as follows.
Desired signal level is set to receiver sensitivity level (BER=0.1%)+3dB.
By sweeping undesired signal level, search the undesired signal level at BER=0.1%.
U/D[dB]= (undesired signal level) - (desired singnal level)

*2 The following diagram shows the ED characteristics.

(Note)

If channel frequency is the neighborhood to multiply of the reference clock frequency or the neighborhood to 2 dividing of the reference clock frequency or the neighborhood to 4 dividing of the reference clock frequency, they may cause a deterioration of RX characteristics.



ED characteristics

5.4.2.3 ○2.4GHz Band

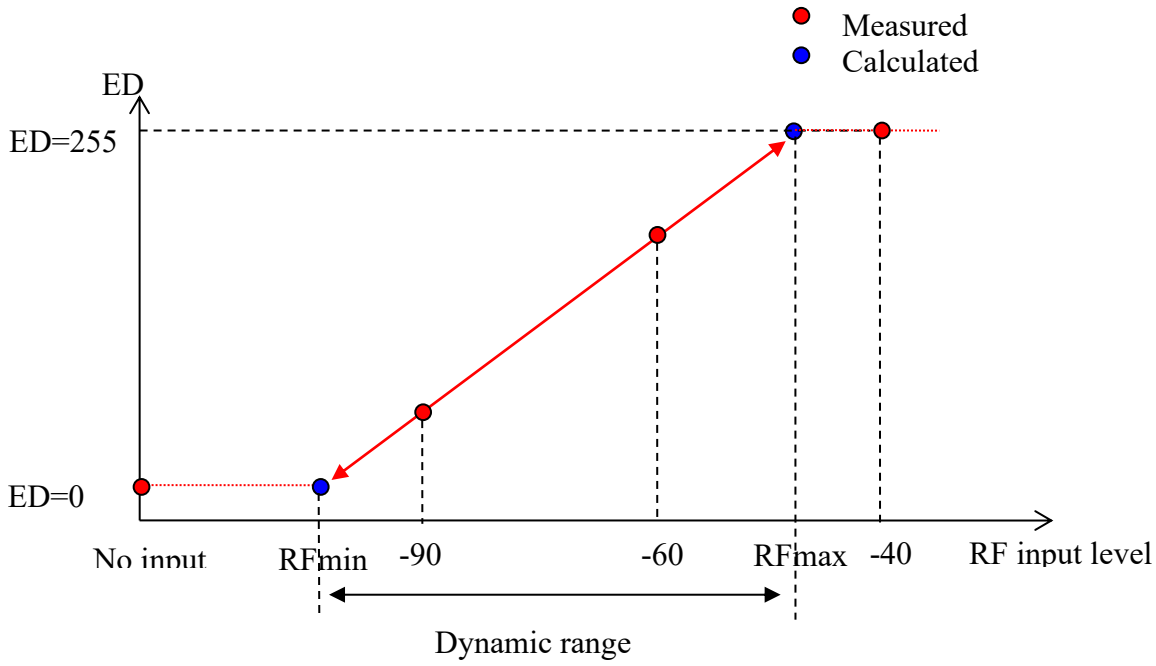
Item	Condition			Min	Typ	Max	Unit
Sensitivity	100kbps mode Center frequency 2.45GHz BER<0.1%, GFSK, 50kHz deviation		FREF =48MHz	-	-97	-89	dBm
Adjacent channel rejection ratio (*1)	Ta = 25°C, 100kbps mode Center frequency 2.45GHz Undesired : CW	+400kHz	FREF =48MHz	25	36	-	dB
		-400kHz	FREF =48MHz	10	31	-	dB
Blocking (*1)	2MHz offset, Ta = 25°C, 100kbps mode Center frequency 2.45GHz		FREF =48MHz	38	55	-	dB
	10MHz offset, Ta = 25°C, 100kbps mode Center frequency 2.45GHz		FREF =48MHz	58	65	-	dB
Minimum power detection level (ED value)	RFmin in RSSI characteristics diagram(*2) 100kbps mode, Center frequency 2.45GHz Channel filter bandwidth = 200kHz setting		FREF =48MHz	-	-105	-90	dBm
ED dynamic range	Dynamic range in ED characteristics diagram(*2), 100kbps mode Center frequency 2.45GHz		FREF =48MHz	50	60	-	dB
Spurious emission			FREF =48MHz	-	-72	-36	dBm

*1 Adjacent channel rejection ratio and Blocking measurement condition is as follows.
Desired signal level is set to receiver sensitivity level (BER=0.1%)+3dB.
By sweeping undesired signal level, search the undesired signal level at BER=0.1%.
U/D[dB]= (undesired signal level) - (desired singnal level)

*2 The following diagram shows the ED characteristics.

(Note)

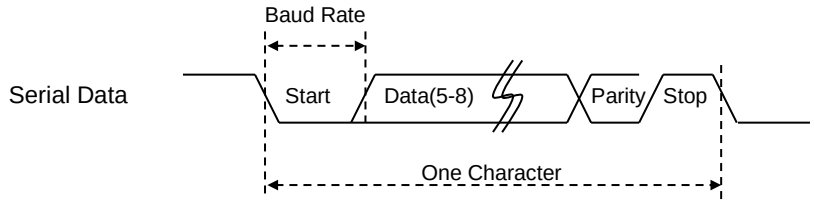
If channel frequency is the neighborhood to multiply of the reference clock frequency or the neighborhood to 2 dividing of the reference clock frequency or the neighborhood to 4 dividing of the reference clock frequency, they may cause a deterioration of RX characteristics.



ED characteristics

5-5. UART interface characteristics

Item	Symbol	Conditions	Min	Typ	Max	Unit
Baud Rate	F_{BAUD}	Load capacitance CL=20pF	F_{UART}/(16*(2^16-1))	-	F_{UART}/16	bps



* F_{UART} is frequency of UART clock. It is derived clock which divides main clock by 1-64.

5-6. SPI Interface Charactaristics

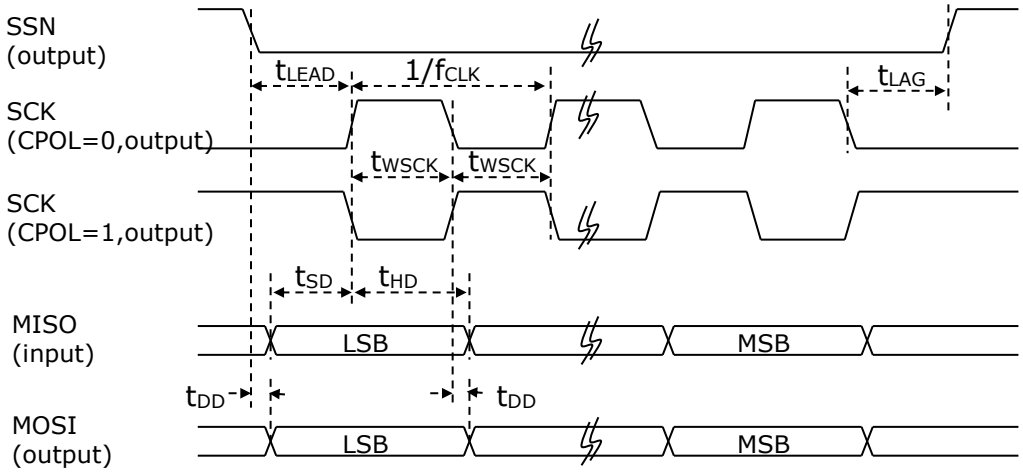
5-6-1. Master

Item	Symbol	Condition	Min	Typ	Max	Unit
Serial clock cycle time	f_{CLK}	CL=20pF	-	-	13.52	MHz
Serial clock High/Low time	t_{WSCK}		30	-	-	ns
Data delay time(output)	t_{DD}		-	-	10	ns
Data setup time(input)	t_{SD}		20	-	-	ns
Data hold time(input)	t_{HD}		System clock x 1 frequency	-	-	ns
SSN-SCK lead time	t_{LEAD}		$0.5t_{SCK}$ -5	-	$1.5t_{SCK}$ +10	ns
SCK-SSN lag time	t_{LAG}		$0.5t_{SCK}$ -5	-	$1.5t_{SCK}$ +10	ns
SSN H minimum width	t_{WSSH}		$1t_{SCK}$ -5	-	$511t_{SCK}$+ 5	ns

* $t_{SCK} = (1000/f_{CLK})$ [ns]

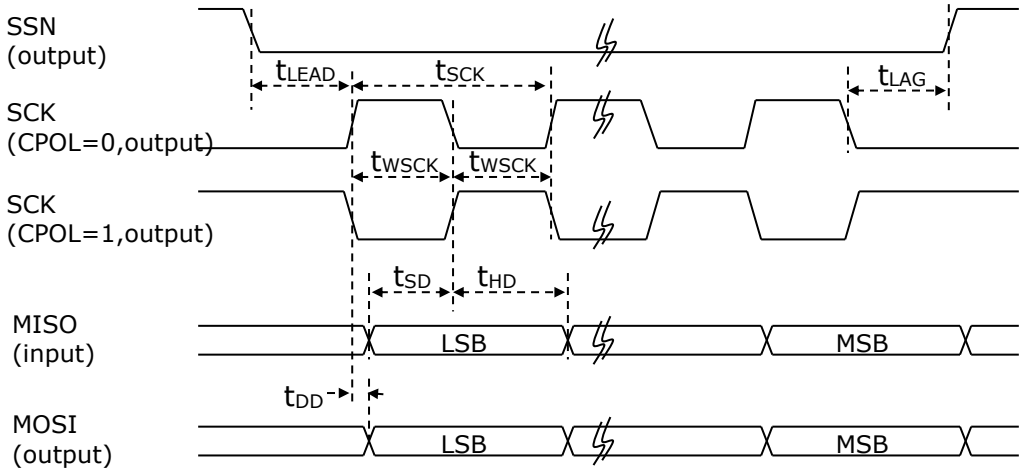
Characteristics when SDLY=1

◎ SPI Master mode timing (CPHA=0)



CPHA=0

◎ SPI Master mode timing (CPHA=1)



CPHA=1

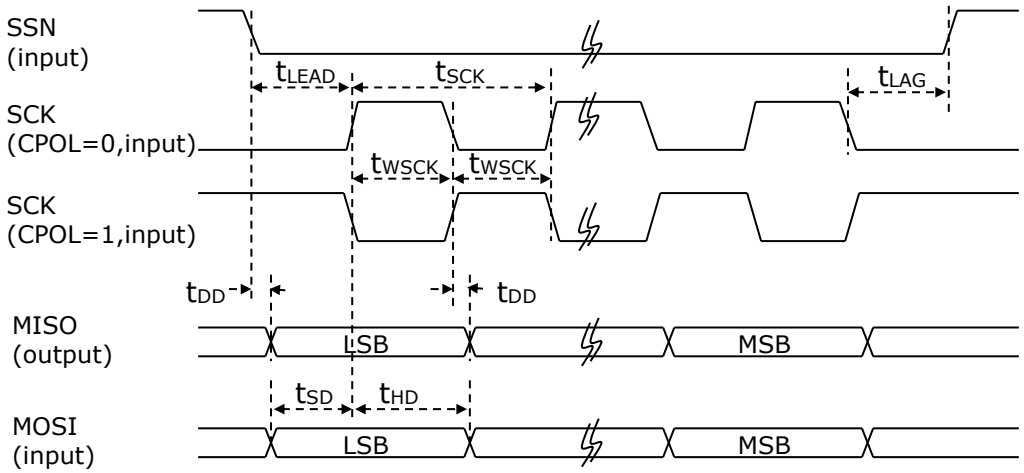
* CPHA and CPOL registers set the data output timing and clock polarity.

5-6-2. Slave

Item	Symbol	Conditions	Min	Typ	Max	Unit
Serial clock cycle time	f_{CLK}	CL=20pF	-	-	12	MHz
Serial clock High/Low time	t_{WSCK}		40	-	-	ns
Data delay time (output)	t_{DD}		-	-	41.5	ns
Data setup time (input)	t_{SD}		10	-	-	ns
Data hold time (input)	t_{HD}		10	-	-	ns
SSN-SCK lead time	t_{LEAD}		40	-	-	ns
SCK-SSN lag time	t_{LAG}		40	-	-	ns

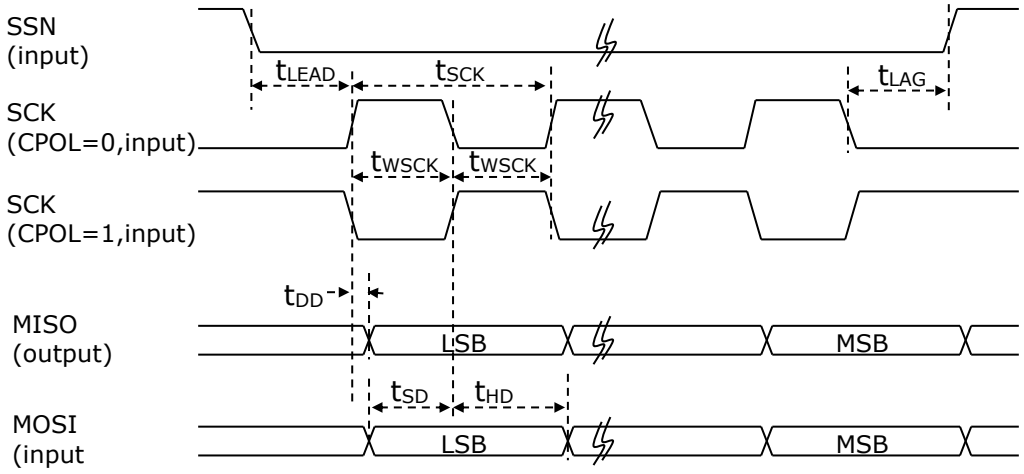
※t_{SCK} = (1000/f_{CLK}) [ns]

◎ SPI slave mode timing (CPHA=0)



CPHA=0

◎ SPI slave mode timing (CPHA=1)



CPHA=1

* CPHA and CPOL registers set the data output timing and clock polarity.

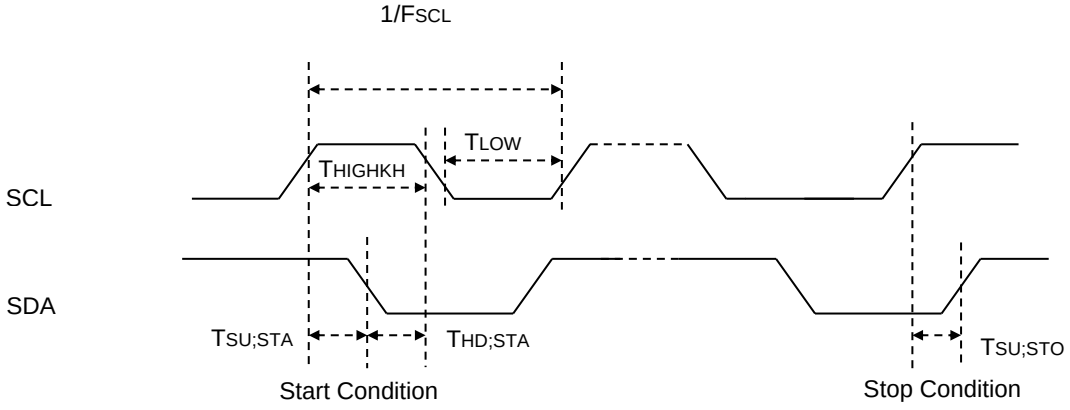
5-7. I2C Interface characteristics

			Standard-Mode		Fast-Mode		Fast-Mode+ Plus		
Item	Symbol	Conditions	MIN	MAX	MIN	MAX	MIN	MAX	Unit
SCL clock frequency	Fscl	Capacitive Load C_L= 10pF	0	100	0	400	0	1000	kHz
SCL H pulse width	T_{HIGH}		4.0	-	0.6	-	0.26	-	μs
SCL L pulse width	T_{LOW}		4.7	-	1.3	-	0.5	-	μs
Start condition hold time	$T_{HD;STA}$		4.0	-	0.6	-	0.26	—	μs
Stop condition setup time	$T_{SU;STA}$		4.7	-	0.6	-	0.26	-	μs
SDA output hold time	$T_{SU;STO}$		4.7	-	0.6	-	0.26	—	μs
SCL output delay time	$T_{HD;DAT}$		0	-	0	-	0	-	μs
SDA input setup time	$T_{SU;DAT}$		250	-	100		50	—	ns

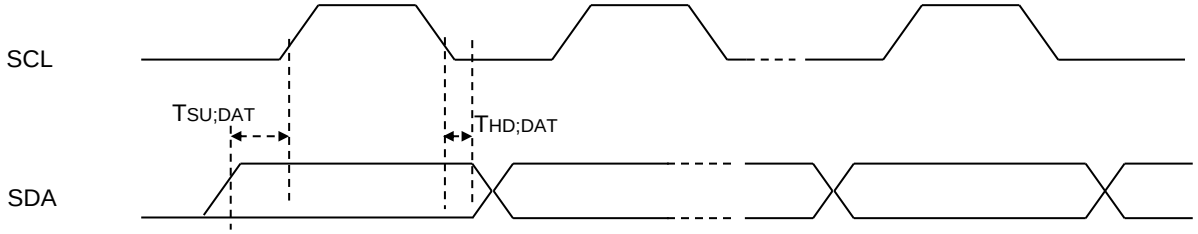
			High Speed-Mode		
Item	Symbol	Conditions	MIN	MAX	Unit
SCL clock frequency	Fscl	Capacitive Load C_L= 10pF	0	3.4	MHz
SCL H pulse width	T_{HIGH}		60	-	ns
SCL L pulse width	T_{LOW}		160	-	ns
Start condition hold time	$T_{HD;STA}$		160		ns
Stop condition setup time	$T_{SU;STO}$		160		ns
SDA output hold time	$T_{HD;DAT}$		0	70	ns
SDA setup time	$T_{SU;DAT}$		10	-	ns

* SCL clock frequency on High Speed-Mode (Master) is restricted by I2C clock source selected by MODE_CNT_CLKGEN3 register and registers in I2C block(I2Cn_HS_SCL_HCNT, I2Cn_HS_LCNT, IC2n_HS_SPKLEN).

◎ Stop condition(SDA fall at SCL=1), Start condition(SDA rise at SCL=1)



◎ Data Transmission, Reception



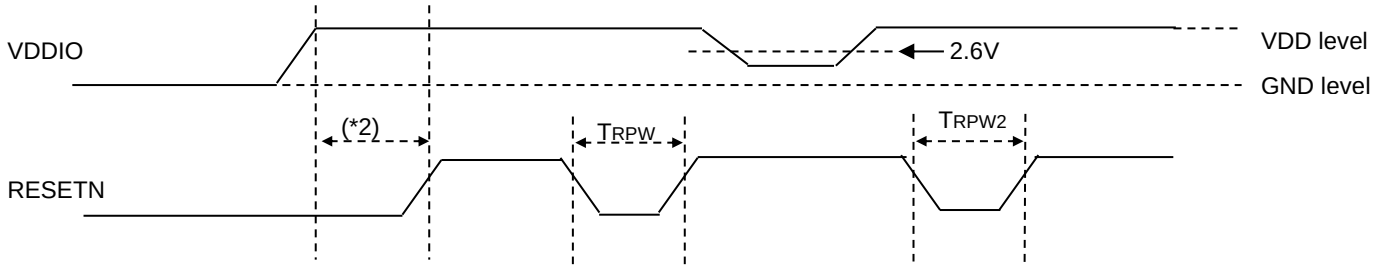
5-8. A/D Conversion Characteristics

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Number of bits	N_{SAR}	Number of bits SAR register	—	10	—	bits
Resolution	RES	VIN=0 to V_{DDIO}	2.6	—	3.6	mV/LSB
Input voltage range	VIN		0	—	VDDIO	V
Differential non-linearity	D_{NL}	-10bit accurate -Input impedance≤1kOhm Input voltage ≧0.1V	-2.5	—	2.5	LSB
Integral non-linearity	I_{NL}		-2.5	—	2.5	LSB
Conversion time	T_L		10	—	20	us

[Note] The ADC output is based on power/GND (tracked).
Connect a sufficient bypass capacitor between each power and GND to suppress the power fluctuation.

5-9. Reset Characteristics

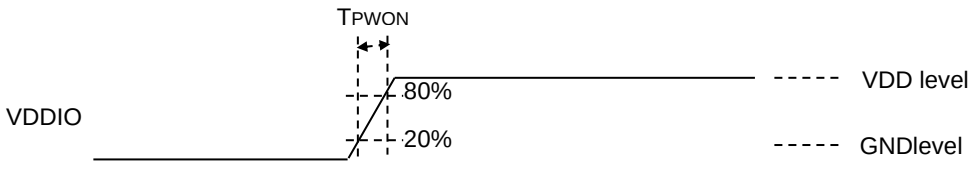
Item	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETN activation time (pulse width) (When starting from VDDIO=0V)	T_{RPW}	–	200	–	–	ns
RESETN pulse time 2 (*1)(When starting from VDDIO≠0V)	T_{RPW2}	VDD>2.6V	1	–	–	ms



(*1) When starting from VDDIO≠0V, input a pulse by external component (such as Reset IC) to the RESETN signal after VDDIO exceeds 2.6V.

5-10. Power-On Characteristics

Items	Symbol	Conditions	MIN	TYP	MAX	Unit
Power-on time difference	T_{PWON}	At power on (All power supply pins)	–	–	5	ms



5-11. Flash ROM characteristics

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Erase cycles endurance	C_{EP}	data retention 10years	10,000	-	-	cycles
		data retention 5years	50,000	-	-	cycles
		data retention 1years	100,000	-	-	cycles
Program time	t_{PR}	32bit program	54	60	66	usec
Erase time	t_{ER}	1KB sector erase	3.3	3.7	4.1	msec

■6. Functional Description

6-1. CPU (Cortex®-M3)

A RISC processor manufactured by ARM®.
It is a 32-bit processor for small size and low power consumption applications and has a 3-stage pipeline configuration. ARMv7-M architecture[1] is implemented.

The configuration is as follows:

- Little-Endian[2]
- A 24-bit system timer (SysTick timer) is included
- NVIC (Nested Vectored Interrupt Controller) is included (maximum interrupt level of 8)
- Multiplier: High-speed (1-cycle) hardware multiplier is provided
- SLEEP supported
- WFI (Wait for Interrupts)/WFE (Wait for Events) supported
- Relocatable vector table
- Privileged/unprivileged mode supported
- Equipped with MPU (Memory Protection Unit)
- Equipped with Serial Wire debug port as debugger interface
- Equipped with ETM (Embedded Trace Macro) (I-ETM/D-ETM)

[1] For details, please refer to "ARMv7-M Architecture Reference Manual" issued by ARM®.
[2] This LSI is fixed to Little-Endian. Little-Endian is unchangeable.

6-2. Flash ROM

It has built-in Flash ROM with 512 KBytes x two banks.
Flash ROM controllers are included. The boot from the Flash ROM is possible.

- Configuration consisting of 512 KBytes x two banks
- Sector size 1 KByte, block size 8 KBytes
- While software is running on one of the banks, program can run in parallel against the other bank.
- Rewriting from the debugger through the debug port (SWD) is possible.
- It is possible to perform 1-word rewrite, sector erase (in 1 KByte), block erase (in 8 KBytes), or chip erase.
- When starting-up, entire Flash ROM area is assigned to the remapping area beginning with address 0x00000000. In addition, arbitrary 1 KByte can be assigned to the remapping area beginning with address 0x00000000 by remapping function.
- Consists of the boot program area storing startup program, such as ISP, the protect set area storing protection settings, the security set area, the user program area, and the data area.
- Offers write protection/read protection features.

6-3. SRAM

256 KB SRAM is included.
Availability of ECC function can be selected against 32 KB out of 256 KB.
When ECC function is enabled, it performs 1-bit error correction and 2-bit error detection. If an error is corrected/detected, an error interrupt is generated.
Most significant 1 KByte in the SRAM space can be used as the secure area enabling secure key storage and data transfer.

6-4. Multilayer Bus

The hierarchical multilayer bus structure provides parallel transfer between CPU/DMAC and each slave. RAMs are located in different layers for each bank, and efficiency can be improved by assigning CPU work area and transfer source/destination of DMAC to different banks.

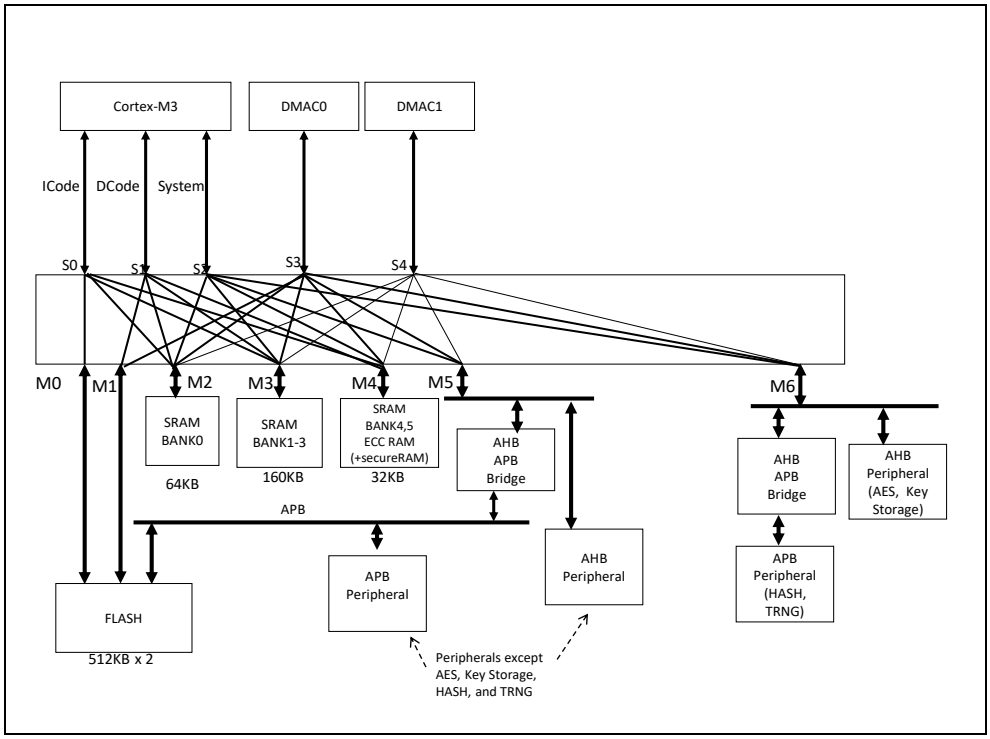


Figure 6-1 Multilayer Bus

6-5. Debug Port

The Serial Wire debug port is included.

ETM (Embedded Trace Macro) interface is included.

6-6. Clock

Crystal oscillator (32.768 kHz for RTC/48 MHz for RF), PLL, high-speed RC oscillator, and low-speed RC oscillator are included as the clock source.

With PLL

81 MHz obtained by multiplying crystal oscillator 32.768 kHz by 2475

or

81 MHz as the result of multiplying 64.864 kHz generated in RF chip by 1249

is generated.

When 64.86 kHz generated in RF chip is used as source clock for PLL, an external crystal oscillator is not required.

6-7. Reset

The chip or individual blocks are reset by power-on reset through the built-in power-on reset generation circuit, hardware reset through the external terminal, WDT reset, software reset, peripheral reset, LOCKUP reset.

6-7-1. Hardware Reset through External Terminal

Occurs through L input to the RESETN terminal.
This occurs as soon as L input is detected.

6-7-2. WDT Reset

Occurs with completion of watchdog timer (WDT).
Time period before the reset becomes valid can be controlled with WDT_TORR.

6-7-3. Software Reset

This refers to SYSRESETREQ reset of Cortex-M3.
This is generated by setting SYSRESETREQ bit of Application Interrupt and Reset Control Register (AIRCR) within Cortex-M3 from the CPU or debugger.
This occurs immediately after the set of SYSRESETREQ bit and is released after the time period between

0.8us and 1.6us.

6-7-4. Peripheral Reset

This resets only the target peripheral through setting the bit assigned to each peripheral of the peripheral reset register (SYSCON_PRST_CON、SYSCON_EPRST_CON、SYSCON_SPRST_CON).
It occurs over the period of eight cycles immediately after register setting. (12.3 ns*8 = approximately 100 ns when 81 MHz)

6-7-5. LOCKUP Reset

This occurs when the CPU becomes lock up state with RESET_LU of SYSCON_CPU_CON configured to 1.

6-8. Power Management

Operation of the CPU (Cortex-M3) in SLEEP and SLEEPDEEP can be set for each peripheral.
It supports the partial shout-down function performing power shut-off for each power supply domain within the chip.
It also supports the retention function retaining the state of storage element at power shut-off.

The power supply area is divided into PD0 area (Always On area) and PD1/PD2/PD3 areas that enable power shut-down. Operation of each area can be set through registers.

6-9. System Control

Performs clock source selection, stopping clock for each peripheral, supply control, control in low power consumption state, chip ID display, and remapping control.

6-10. Peripheral

6-10-1. UART

Includes three 16550-compatible UART ports (UART0/UART1/UART2).
Supports automatic flow control (UART0 only).
Maximum Baud Rate of 460,800 bps.

6-10-2. SPI

Includes three master/slave selectable SPI ports[3]. (SPI0/SPI1/SPI2)
SPI0 and SPI1 can be commonly or exclusively used for clock and/or data input/output.

6-10-3. WDT

Programmable 16-bit watchdog timer.
Clock for timer counter can be selected.

6-10-4. I2C

Supports Standard Mode, Fast Mode, Fast Mode+, High Speed Mode.

6-10-5. GPIO

Includes up to 19 general-purpose ports.

[3] One (SPI2) of these ports is used for communication with the built-in RF chip.

6-10-6. EXTINT

A general-purpose external interrupt controller that can set signals between arbitrary general-purpose ports or MCP chips as interrupt signals.
Enables setting of H level detection/L level detection/rising edge detection/falling edge detection.
Includes the input debounce function.

6-10-7. Timer

Includes four channels of 32-bit standard timers.

6-10-8. Flexible Timer

Includes six channels of 32-bit multifunction timers providing PWM output, capture, and compare output functions.

6-10-9. RTC

Includes a real time clock with the perpetual calendar function capable of read/write by seconds.
It can operate through the crystal oscillator (32.768 kHz) or built-in low-speed RC[4].
Includes time correction and time designation interrupt functions.

6-10-10. DIO

Includes the digital interface for communication with built-in RF.

[4] Accuracy of RTC depends on that of clock source.

6-10-11. DMAC

Includes two direct memory access controllers. Among peripherals, SPI0/1/SPI2, CRYPTO (AES/HASH), UART0/1/2, and I2C0/1 support DMA transfer[5].

DMAC features include:

- Eight channels on DMAC0 and two channels on DMAC1.
- Each channel includes an 8-stage FIFO for source transfer and destination transfer.
- Supports inter-memory and peripheral-to-memory transfer.
- Includes the hardware handshake interface that accepts transfer requests from each peripheral supporting DMA transfer.
- Supports up to 2048-byte block transfer.
- Supports the channel priority setting.
- Multilayer bus enables allocation to the individual bus for each DMAC
- Supports increment/decrement of the transfer address and transfer to a single address.
- Supports multiple block transfer using a linked list.

[5] Use DMAC1 to transfer an encryption key when the secure key storage function is enabled.

6-10-12. TRNG

Includes the true random number generation circuit consisting of the ring oscillator and linear feedback shift register.

6-10-13. CRYPTO

Includes the following encryption operation engine:

AES engine
  128/192/256-bit
  ECB/CBC/CFB/OFB/CTR/CCM/GCM/GMAC modes
SHA-1/SHA-224/SHA-256

When the key storage is enabled, the encryption key can be protected against read from the CPU.

6-10-14. Secure Key Storage

Includes RAM area (1 KB), which is unreadable from the CPU and stores encryption keys used in CRYPTO.
Availability of the secure storage function can be set[6].
When the secure key storage function is disabled, it becomes the RAM area readable from the CPU.
When the secure key storage function is enabled, it transfers data between CRYPTO, key storage, and SRAM via DMAC1.

[6] For how to enable the secure key storage function, contact us as needed.

6-10-15. ADC

This function controls the 10-bit successive approximation type A/D converter.
ADC features include:

- Programmable scan of up to three channels (CH0 to CH2) (scan time/order configurable).
- Scan result notification (The scan completion is notified by an interrupt.)
- Averaging of A/D conversion data (The average value of A/D conversion results is displayed.)
- Calculation of CH0 to CH2 input voltage (It is assumed that the reference voltage output from the regulator at CH3 is monitored.)

  *CH0,1 are supported for only PKG option.

6-10-16. CLK_Timer

This function uses the high-speed clock to count a certain time period of the low-speed clock and stores the count result in a register.
Based on the count result, it can determine the frequency error between the result and an ideal clock.

6-11. RF

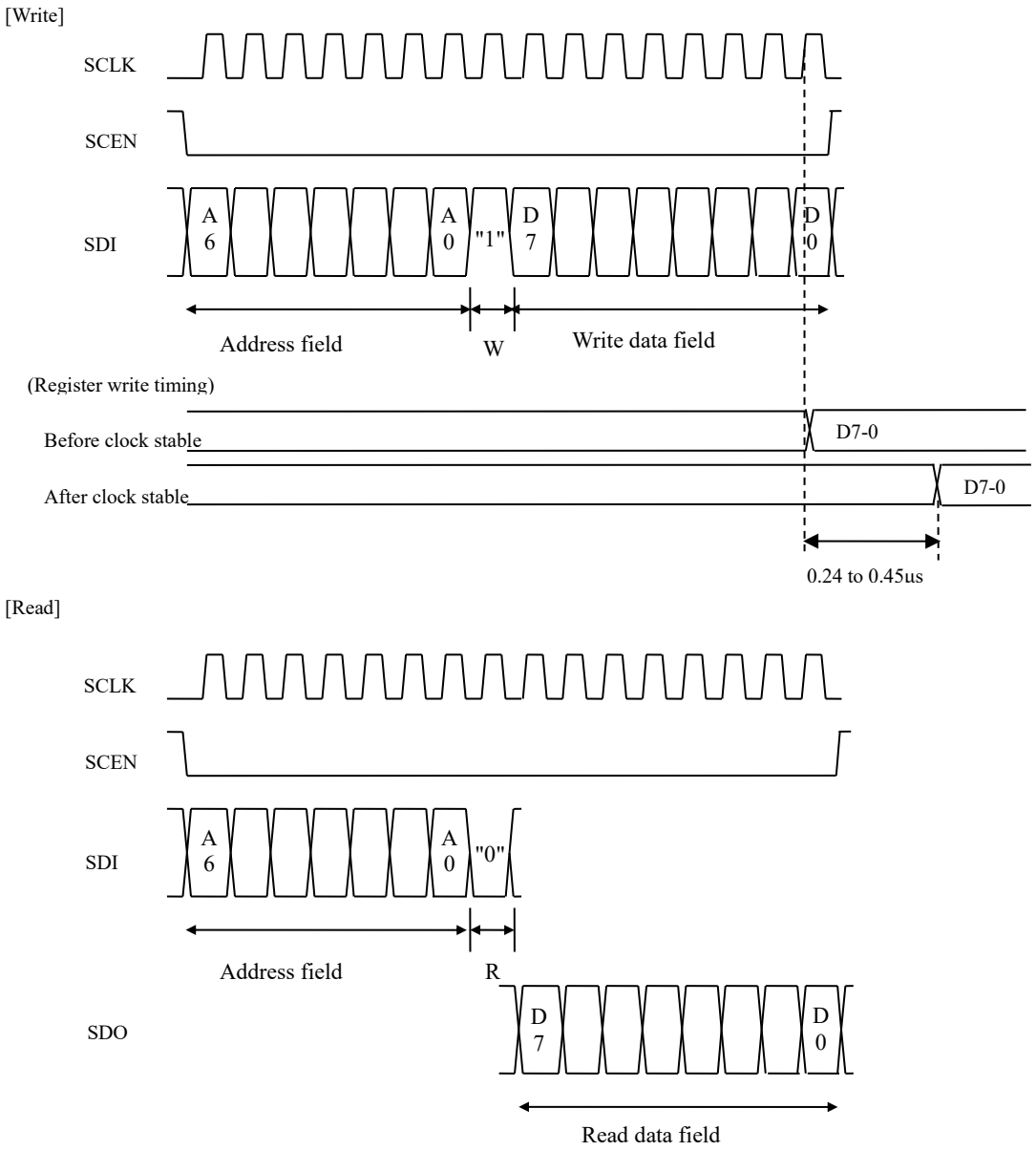
6-11-1. Host Interface

6-11-1-1 ○Serial Peripheral Interface (SPI)

ML7436N has a serial peripheral interface (hereafter referred to as SPI). SPI on ML7436N supports slave mode. Host MCU can read/write to the ML7436N registers and on-chip FIFO using MCU clock. Single access mode and burst access mode are also supported.

[Single access mode timing chart]

In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 data. During write operation, if SCEN is set to "H", the control section will be reset. After the internal clock is stabilized, the data will be written into the register in synchronization with the internal clock.



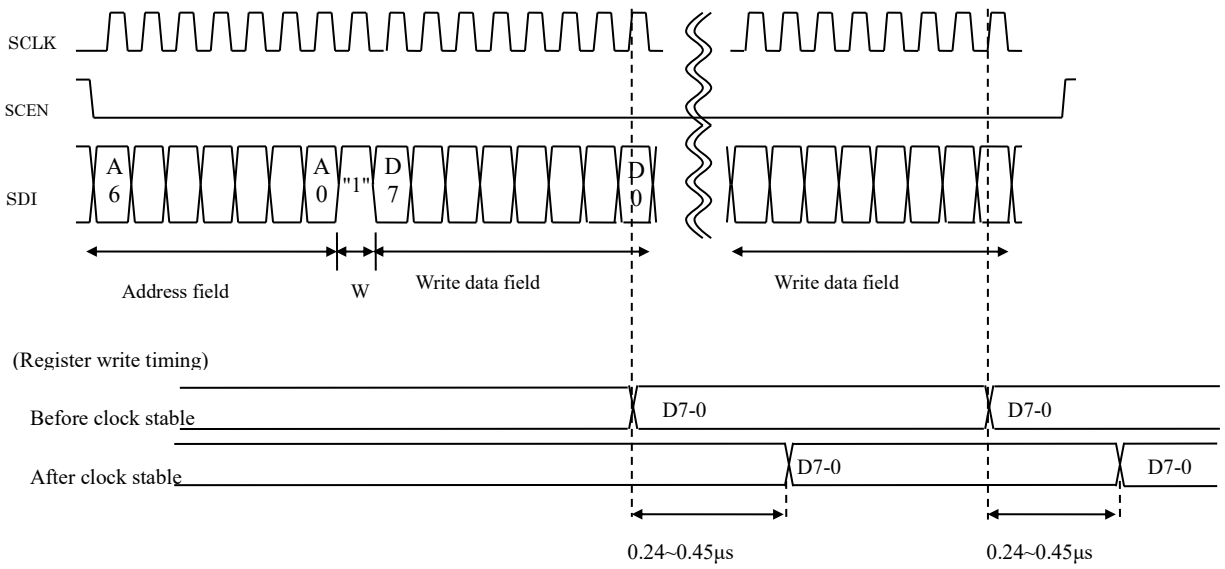
[Burst access mode timing chart]

By maintaining SCEN line as "L", Burst access mode will be active. By setting SCEN line to "H", releasing the burst access mode. During burst access mode, address will be automatically incremented. When SCEN line becomes "H" before Clock for D0 is input, data transaction will be aborted.

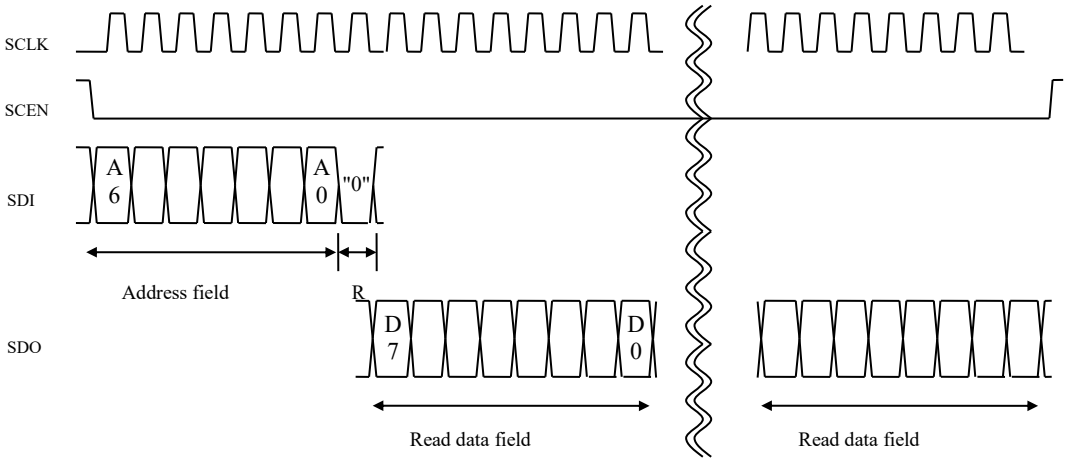
[Note]

If access destination is [WR_TX_FIFO: B0 0x7C] or [RD_FIFO: B0 0x7F] register, address will not be incremented, allowing continuous access to the FIFO.

[Write]


SCLK
SCEN
SDI
A 6
A 0
"1"
D 7
D 0
Address field
W
Write data field
Write data field
(Register write timing)
Before clock stable
After clock stable
D7-0
D7-0
D7-0
D7-0
0.24~0.45µs
0.24~0.45µs

[Read]


SCLK
SCEN
SDI
SDO
A 6
A 0
"0"
Address field
R
D 7
D 0
Read data field
Read data field

6-11-2. LSI State Control

State can be controlled from MCU by setting registers below.

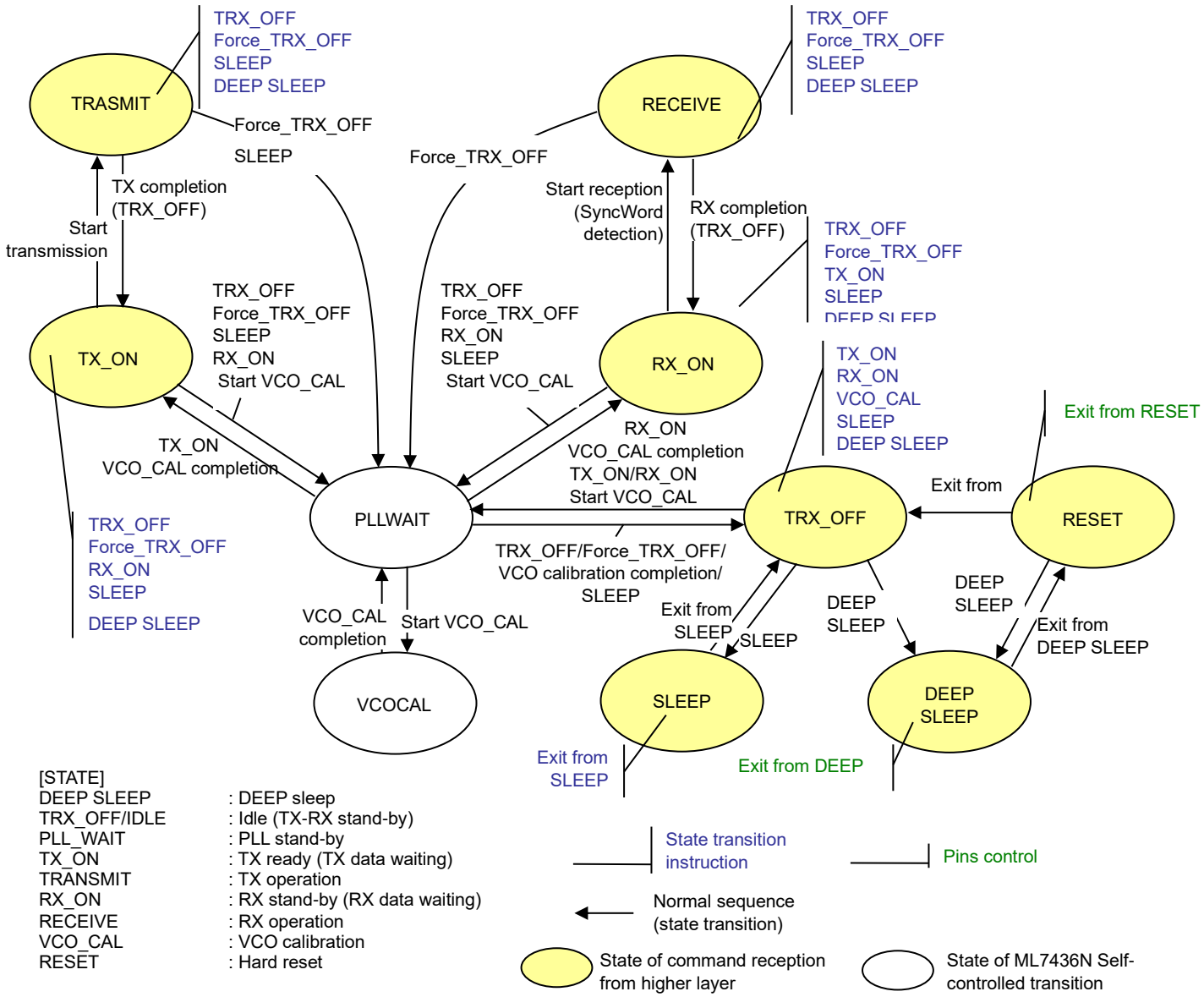
State transition command	Registers setting
TX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x9
RX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x6
TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x8
Force_TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x3
VCO_CAL	VCO_CAL_START([VCO_CAL_START: B0 0x6F(0)])= 0b1

State can be changed without command from MCU. If one of the following conditions is met, state is changed automatically according to the following table.

Function	Register
Automatic TXON after FIFO write completion (AUTO_TX)	AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)])
Automatic TXON during FIFO write (FAST_TX)	FAST_TX_EN([RF_STATUS_CTRL: B0 0x0A(5)])
RF state setting after packet transmission completion	TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)])
RF state setting after packet reception completion	RXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(3-2)])
Automatic RX_ON/TX_ON by Wake-up time	[SLEEP/WU_SET:B0 0x2D]
Automatic VCO calibration after state transition	AUTO_VCOCAL_EN([VCO_CAL_START: B0 0x6F(4)])
Automatic VCO calibration after channel change	AUTO_VCOCAL_CHCHG_EN([VCO_CAL_START:B0 0x6F(3)])
Automatic TX_ON by high speed carrier checking mode	CCADONE_MODE([ED_CTRL:B0 0x41(6)])
Force_TRX_OFF after PLL unlock detection during TX	PLL_LD_EN([PLL_LOCK_DETECT: B1 0x0B(7)])
RF state setting after clock stabilization	CLKINIT_TRX_EN([FIFO_SET: B0 0x78(2)])

Each LSI state transition control follows the state diagram shown below.

6-11-2-1 ○State Diagram



LSI State Diagram

6-11-2-2 ○SLEEP Setting

DEEP_Sleep mode: Powers for all blocks except IO pins are turned off.

Sleep mode: All the linear regulators and 48 MHz oscillation circuits are turned off. But sub-regulator is turned on.

The following registers can be programmed to control SLEEP state.

Function	Register
Power control	PDN_EN([SLEEP/WU_SET: B0 0x2D(1)])
Wake-up setting	WAKEUP_EN([SLEEP/WU_SET: B0 0x2D(4)])
Wake-up timer clock source setting	WUT_CLK_SOURCE([SLEEP/WU_SET: B0 0x2D(2)])
Internal RC oscillator control	RC32K_EN ([CLK_SET2: B0 0x03(3)])
SLEEP setting	SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]) SLEEP_LOW_VDD([DCDC_CTRL:B1 0x70(1)])

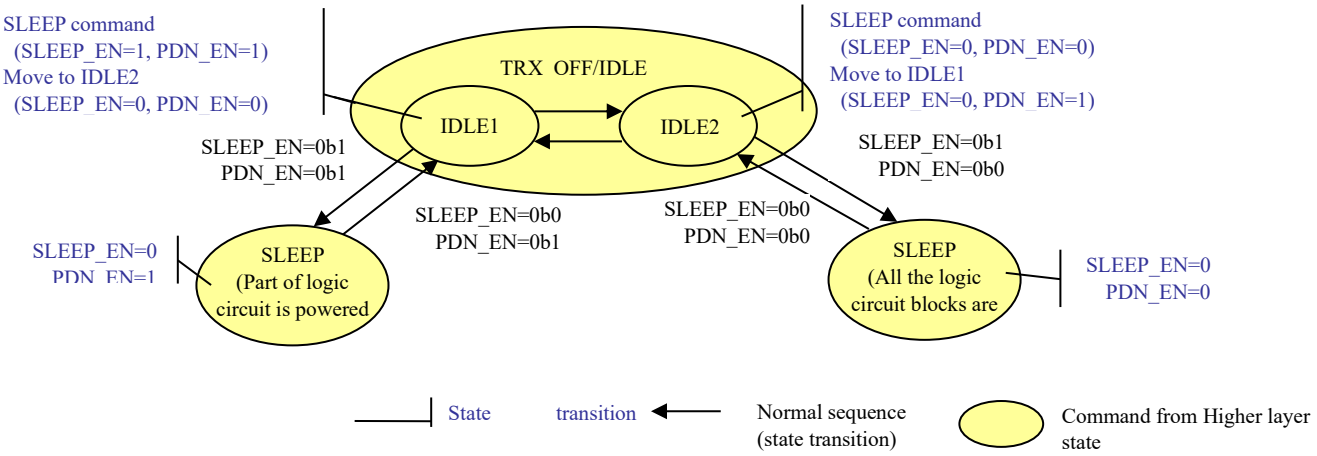
Setting method and internal state for DEEP_SLEEP and typical SLEEP modes are as follows.

SLEEP mode	Setting method	All the linear regulators	Sub regulator	48MHz oscillator	RC oscillation circuit	Low clock timer	TX FIFO
DEEP SLEEP	RESETN pin = "L" REGPDIN pin = "H"	OFF	OFF	OFF	OFF	OFF	OFF
SLEEP1	[SLEEP/WU_SET: B0 0x2D(5-0)] = 0b00_0111 [CLK_SET2: B0 0x03(3)] = 0b0	OFF	ON	OFF	OFF	OFF	OFF
SLEEP2	[SLEEP/WU_SET: B0 0x2D(5-0)] = 0b11_0111 [CLK_SET2: B0 0x03(3)] = 0b1	OFF	ON	OFF	ON	ON	OFF

Contents of registers are not kept during DEEP_SLEEP. Contents of registers are kept during SLEEP1 and SLEEP2. However, in SLEEP1 and SLEEP2, contents of TX FIFO are not kept, because power to FIFO is turned off.

[Note]

1. It takes 8 µs for the inside of the LSI to move to the SLEEP state after SLEEP is set from the IDLE state. To perform an SPI access after SLEEP is set, access after the inside of the LSI has moved to the SLEEP state (8 µs or more after SLEEP is set).
2. It takes 5 µs for the inside of the LSI to move to the SLEEP state after SLEEP is set from the TX/RX state and INT[3]([INT_SOURCE_GRP1: B0 0x0D(3)]) = 0b1. To perform an SPI access, access after the inside of the LSI has moved to the SLEEP state (5 µs or more after INT[3]).
3. Two types of SLEEP states are available according to a combination of the power control setting of the logic circuit block during SLEEP PDN_EN([SLEEP/WU_SET: B0 0x2D(1)]) and SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]). However, be sure to set to an IDLE state (IDLE1, IDLE2) from which a transition to each of the SLEEP states can be carried out, and then set to the SLEEP state. Incidentally, the LSI state of IDLE1 and IDLE2 are the same IDLE state and their internal states are the same.



SLEEP state diagram

4. It is neccesary to set the followling registers depending on SLEEP time.

SLEEP time	Register setting SLEEP_LOW_VDD ([DCDC_CTRL:B1 0x70(1)])	DCDC output (VDD_REG pin) State and Operation
Within 5s	0b0	Holds electric charge of external capacitance with HiZ
Over 5s	0b1	Holds electric charge as power voltage level

6-11-2-3 ○Notes to Set RF State

ML7436N is able to change the internal RF state transition autonomously (without commands from MCU) as well as RF state change commands from MCU. (please refer to ”LSI state transition instruction”). If both timing of operation (autonomous state and state change from MCU command) overlapped, unintentional RF state may occur. Timing of autonomous state RF change is described in the following table. Care must be taken not to overlap the conditions.

Function	RF state change (before → after)	RF state transition timing (not from Host MCU command)	Recommended process
Automatic TX	TRX_OFF/RX_ON → TX_ON	After TX data reception completion interrupt occurs, {[TX_RATE_H/L: B1 0x02/03)] setting value * 2 / FREF[MHz] / (MSTR_CLK_SEL1[CLK_SET1: B0 0x02(5)]+1)}[μs] duration	Perform a write access to [RF_STATUS:B0 0x0B] after RF state transition completion interrupt occurs or GET_TRX ([RF_STATUS:B0 0x0B(7-4)]) has changed to the expected state.
FAST_TX mode		After FIFO write access amount exceeds trigger level + 1, {[RX_RATE1_H/L:B1 0x04/05] setting value * 5 / FREF [MHz] / (MSTR_CLK_SEL1[CLK_SET1: B0 0x02(5)]+1)}[μs] duration	
RF state setting after TX completion	TX_ON → TRX_OFF	After TX completion interrupt occurs, {[TX_RATE_H/L:B1 0x02/03] setting value * 2 / FREF [MHz] / (MSTR_CLK_SEL1[CLK_SET1: B0 0x02(5)] + 1)}[μs] duration	
	TX_ON → RX_ON		
	TX_ON → SLEEP		
RF state setting after RX completion	RX_ON → TRX_OFF	After data RX completion interrupt occurs, {[RX_RATE1_H/L:B1 0x04/05] setting value * 2 / FREF [MHz] / (MSTR_CLK_SEL1[CLK_SET1: B0 0x02(5)]+1)}[μs] duration	
	RX_ON→TX_ON		
	RX_ON→SLEEP		
Wake-up timer	SLEEP → TX_ON	After wake-up timer completion,	

	SLEEP → RX_ON	low speed wake-up timer clock cycle duration	
Automatic VCO calibration	TRX_OFF→VCO_CAL→ TX_ON/RX_ON	Duration from TRX_OFF state to TX_ON/RX_ON state (execution of VCO calibration)	
	TX_ON→VCO_CAL→RX_ON	Duration from TX_ON state to RX_ON state (execution of VCO calibration)	
	RX_ON→VCO_CAL→TX_ON	Duration from RX_ON state to TX_ON state (execution of VCO calibration)	
	RX_ON → CH switch → VCO_CAL → RX_ON	From issuance of CH switch command to completion of VCO calibration (execution of VCO calibration)	After a VCO calibration completion interrupt occurs, conduct write access to [RF_STATUS:B0 0x0B].
Continuous operation timer	TX_ON → SLEEP	After continuous operation timer completion, low speed wake-up timer clock cycle duration	Perform a write access to [RF_STATUS:B0 0x0B] after RF state transition completion interrupt occurs or GET_TRX ([RF_STATUS:B0 0x0B(7-4)]) has changed to the expected state.
	RX_ON → SLEEP		
High speed carrier checking	RX_ON → SLEEP	After CCA completion interrupt occurs, (1/FREF [MHz]) * (MSTR_CLK_SEL1[CLK_SET1: B0 0x02(5)] + 1) * 12 [µs] duration	
	RX_ON → TX_ON		
PLL unlock detection	TX_ON → TRX_OFF	After PLL unlock detection interrupt occurs, (ramp down time + 6) [µs] (*1) duration	(Ramp down time + 6) [µs] (*1) after the interrupt occurs, perform a write access to [RF_STATUS:B0 0x0B].
RF state setting after the clock stabilization	TRX_OFF → TX_ON/RX_ON	After clock stabilization interrupt occurs, (1/FREF [MHz]) * (MSTR_CLK_SEL1[CLK_SET1: B0 0x02(5)] + 1) * 48 [µs] duration	Perform a write access to [RF_STATUS:B0 0x0B] after RF state transition completion interrupt occurs or GET_TRX ([RF_STATUS:B0

			0x0B(7-4)]) has changed to the expected state.

(*1) Depends on the ramp down time setting. For information on the ramp down time, refer to "TX Related Function."

6-11-3. Packet Handling Function

6-11-3-1 ○Packet Format

ML7436N supports Wireless M-Bus frame Format A/B, and Format C/D which is non Wireless M-Bus universal format. The following packet handling are supported in FIFO mode or DIO mode

- Preamble and SyncWord automatic insertion (TX) --- Common to DIO/FIFO mode
- Preamble and SyncWord automatic detection (RX) --- Common to DIO/FIFO mode
- Preamble and SyncWord automatic deletion (RX) --- Common to DIO/FIFO mode
- CRC data insertion --- FIFO mode only
- CRC check and error notification --- Common to DIO/FIFO mode

Packet format registers are as follows.

Function	Register
Packet format setting	PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)])
RX extended link layer mode disable	RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])
Data area bit order setting	DAT_LF_EN([PKT_CTRL1: B0 0x04(4)])
Length area bit order setting	LEN_LF_EN([PKT_CTRL1: B0 0x04(5)])
Extended link layer mode setting	EXT_PKT_MODE([PKT_CTRL1: B0 0x04(7-6)]) EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)])
Length field setting	LENGTH_MODE([PKT_CTRL2: B0 0x05(1-0)])

The following table shows packet format list that RF supports.

Packet Format	Relationship between the standard	
Format A	Wireless M-Bus Format A	Normal
		Extended Link Layer CI=0x8C
		Extended Link Layer CI=0x8D
		Extended Link Layer CI=0x8E
		Extended Link Layer CI=0x8F
Format B	Wireless M-Bus Format B	Normal
		Extended Link Layer CI=0x8C
		Extended Link Layer CI=0x8D

		Extended Link Layer CI=0x8E
		Extended Link Layer CI=0x8F
Format C	general purpose format1 (with L-field)	
Format D	general purpose format2 (without L-field)	

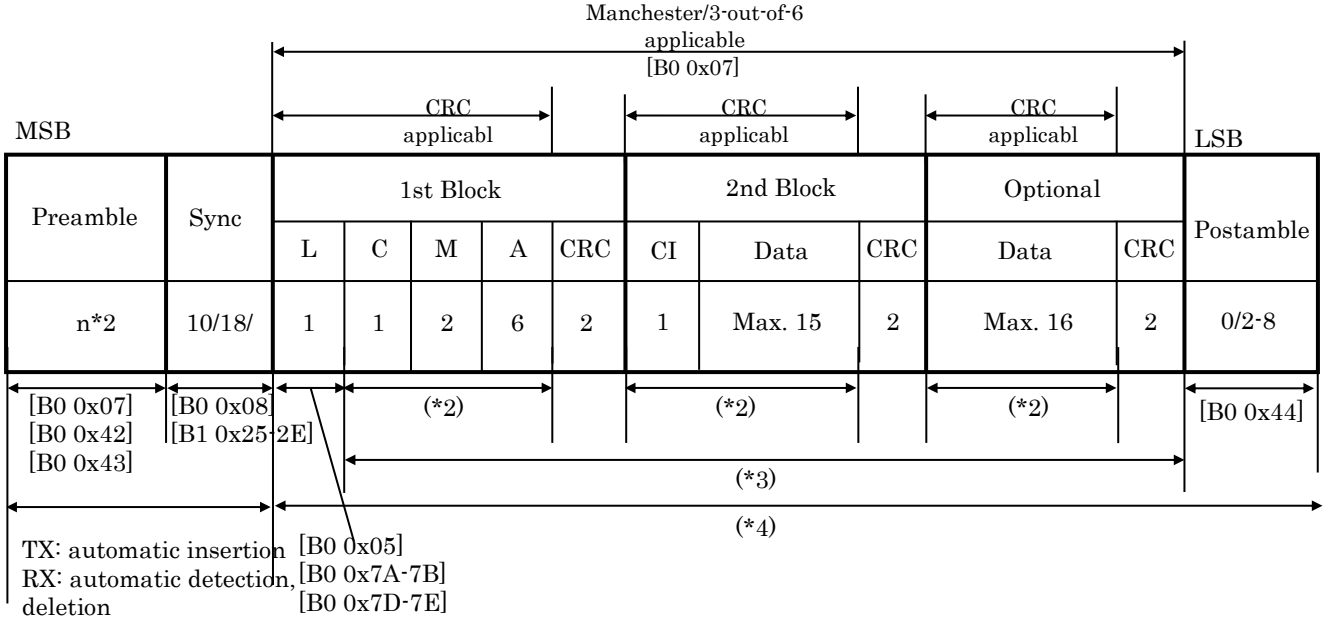
Packet formats supported by ML7436N are as follows.

(1) Format A (Wireless M-Bus)

To use Format A, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b00.

Format A consists of 1st Block, 2nd Block and Optional Block(s). Each block has 2 bytes of CRC. "L-field" (1st byte of 1st Block) indicates packet Length, which indicates the total byte count of data subsequent to C-field of the 1st Block excluding CRC and Postamble. In addition, the 2nd Block or Optional Block subsequent to the 1st Block is added according to the Length.

The following [] indicates register address [bank #, address].



*1: Each mode of Wireless M-Bus has different minimum value of n.

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

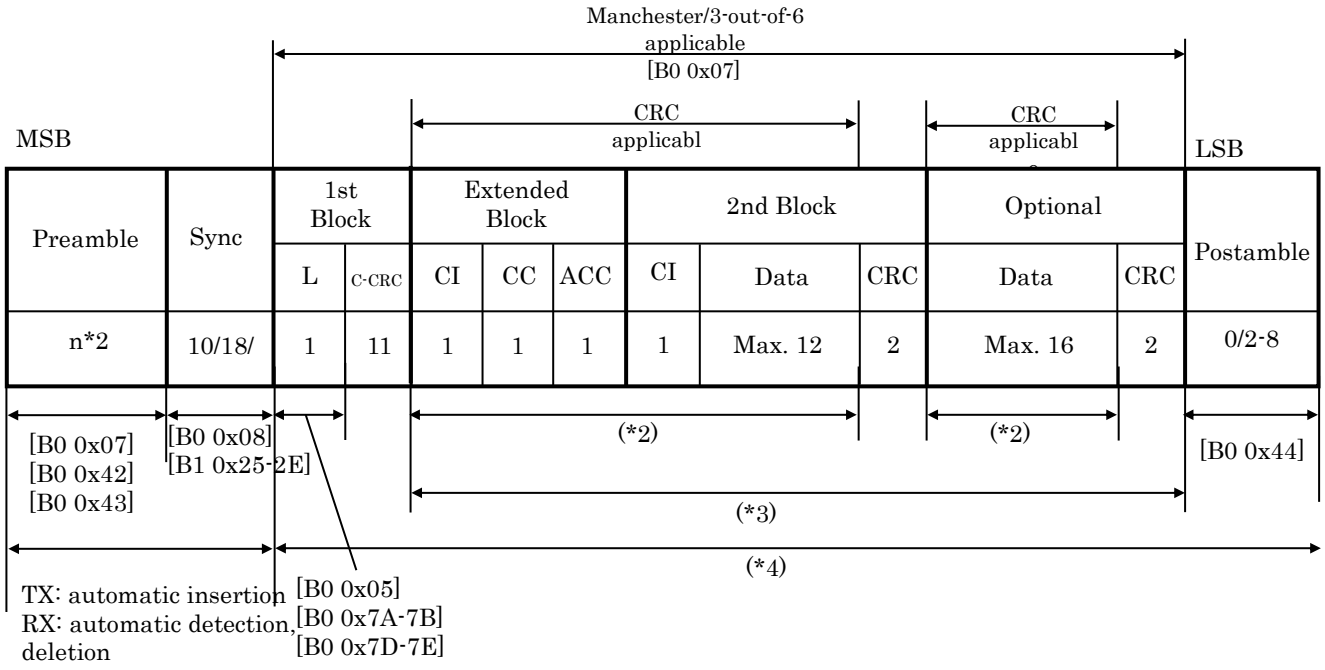
Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) is set to 0x8C/0x8D/0x8E/0x8F, Extended Link Layer Format is applied and the packet format is extended as follows.

(a) CI-field = 0x8C

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b01 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00 If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to the normal format of Format A.

*2: Indicates TX FIFO data storage area upon TX.

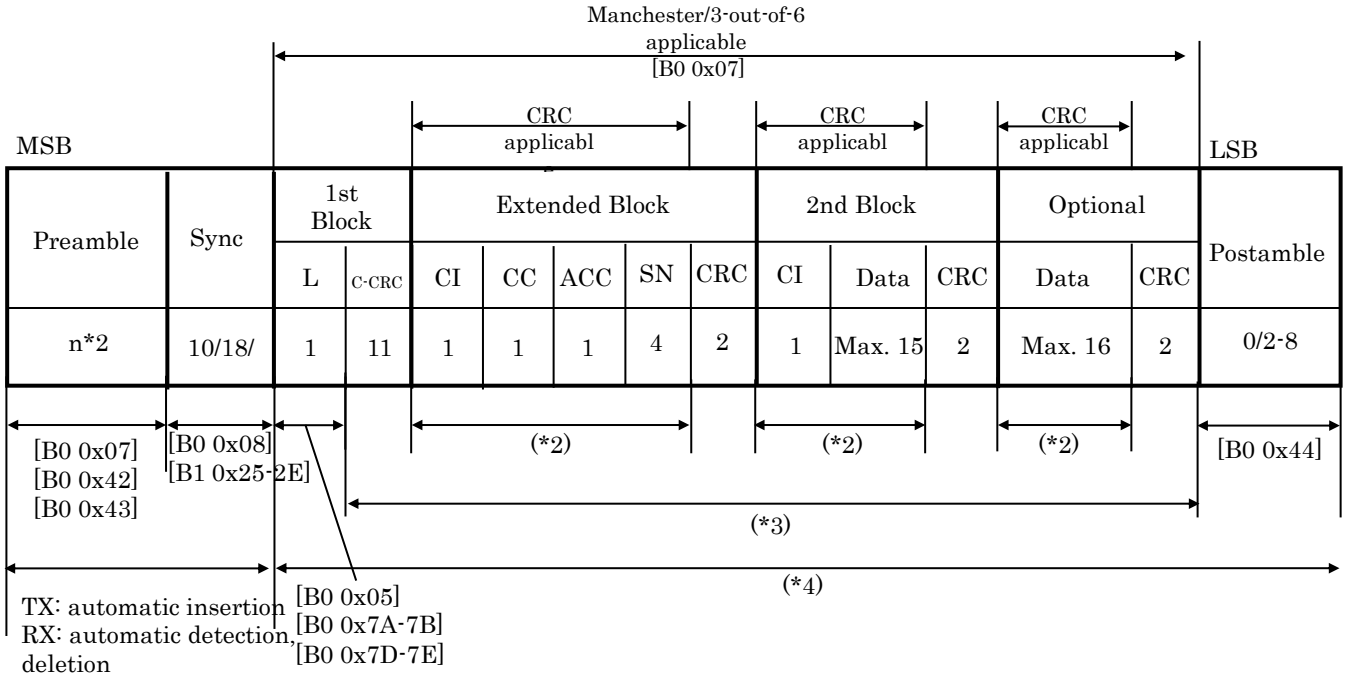
*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(b) CI-field = 0x8D

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b10 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00 If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to the normal format of Format A.

*2: Indicates TX FIFO data storage area upon TX.

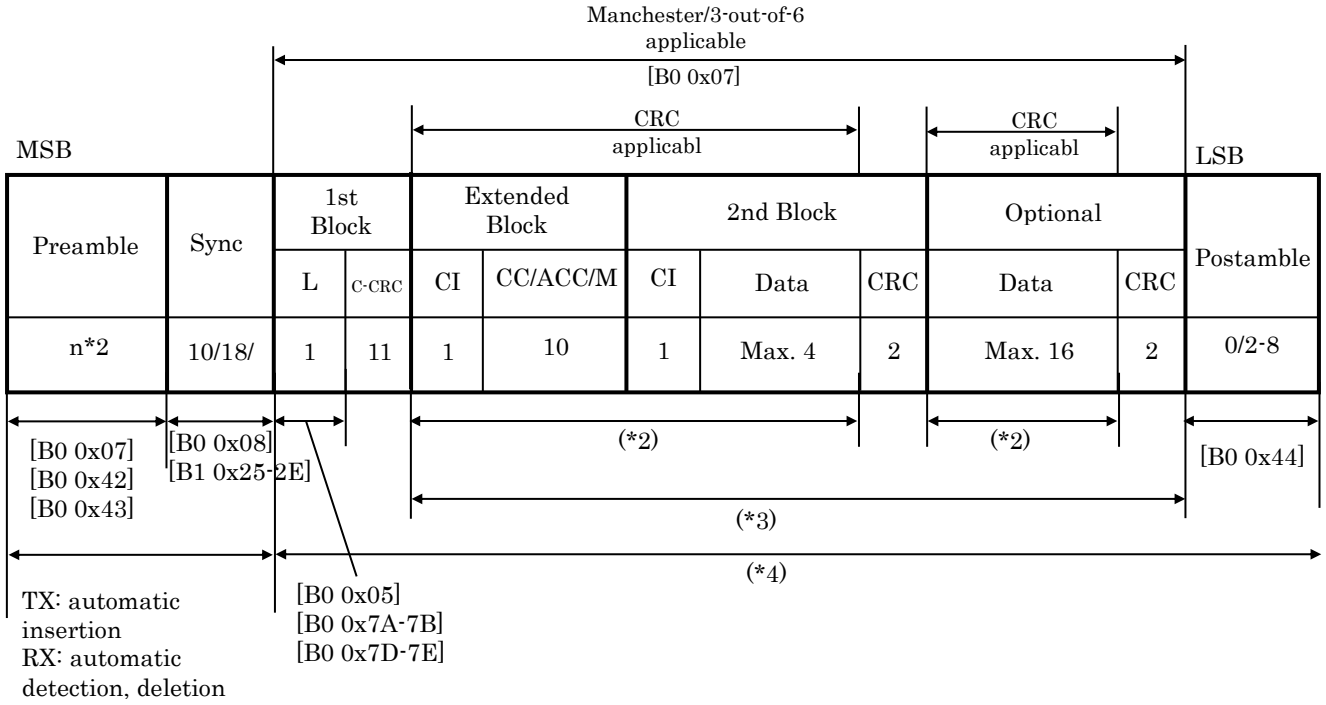
*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(c) CI-field = 0x8E

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b01. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to the normal format of Format A.

*2: Indicates TX FIFO data storage area upon TX.

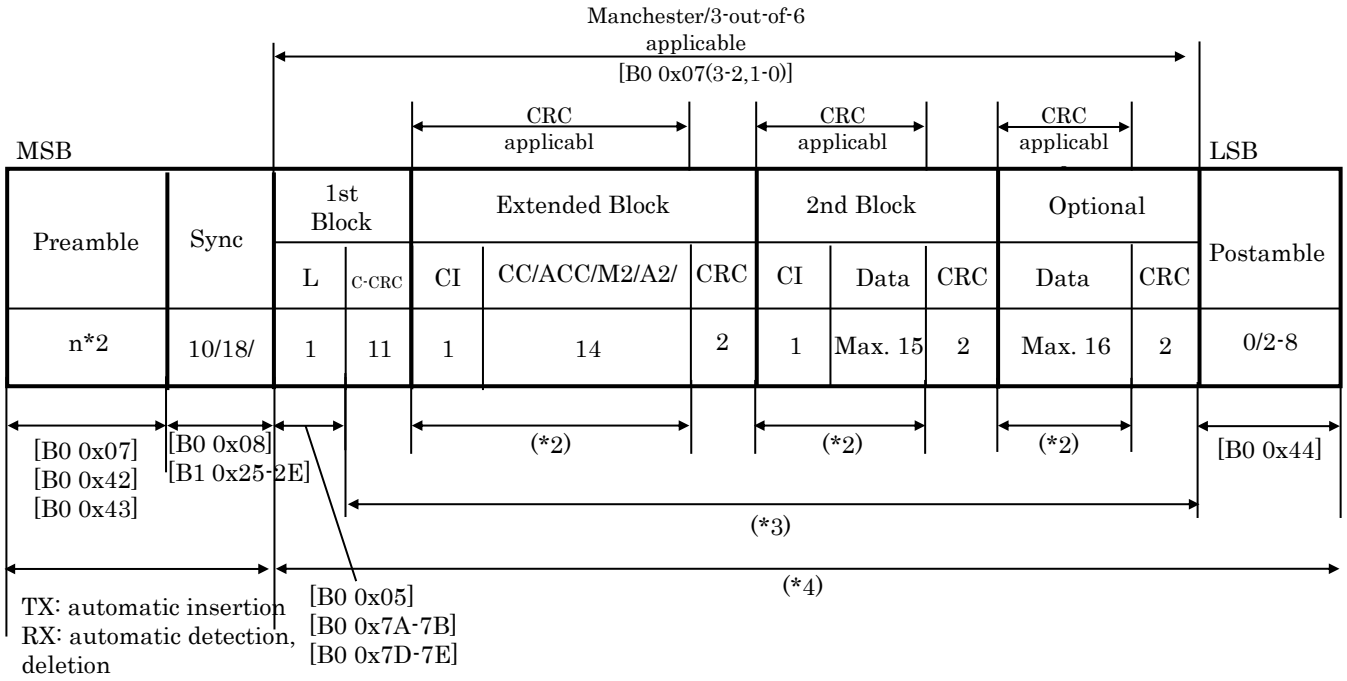
*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(d) CI-field = 0x8F

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b10. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to the normal format of Format A.

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

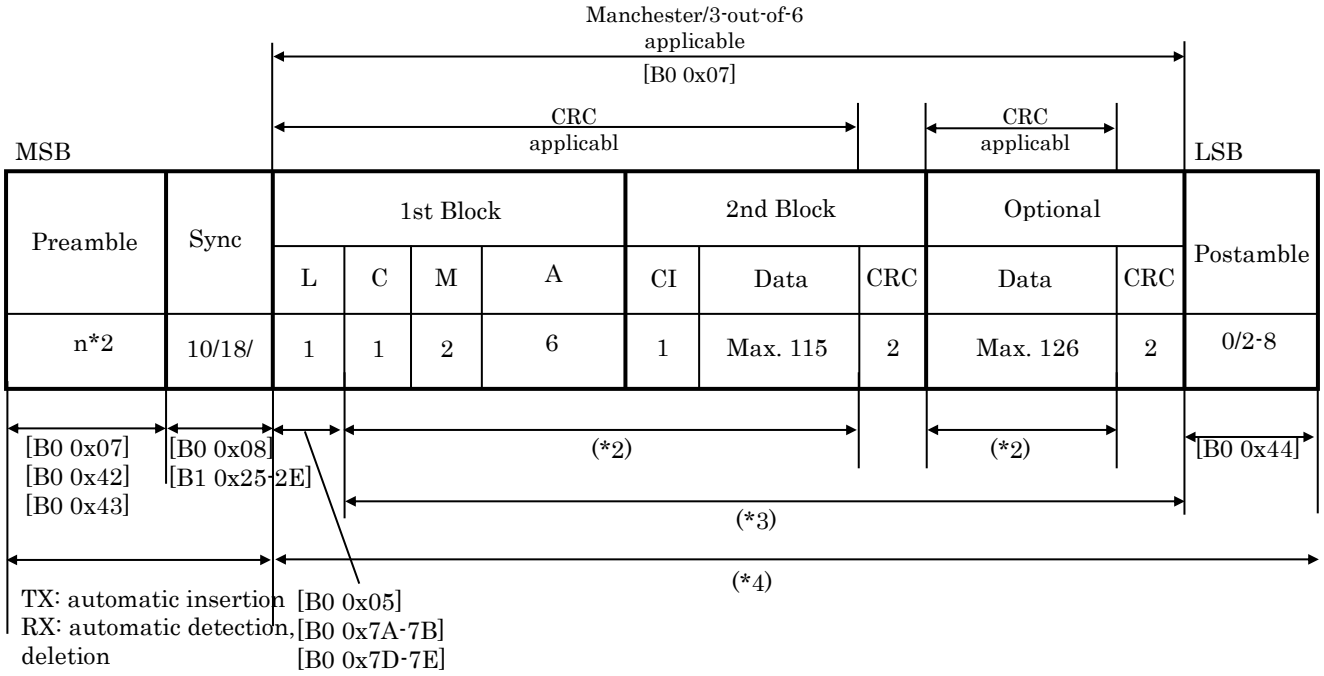
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(2) Format B(Wireless M-Bus)

To use Format B, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b01.

Format B consists of 1st Block, 2nd Block or Optional Block. Each block after 2nd Block has 2 bytes of CRC. "L-field" (1st byte of 1st Block) indicates packet Length, which indicates the total byte count of data from C-field to final CRC data of the 1st Block. In addition, the 2nd Block or Optional Block subsequent to the 1st Block is added according to the Length.

The following [] indicates register address [bank #, address].



*1: Each mode of Wireless M-BUS has different minimum value of n.

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

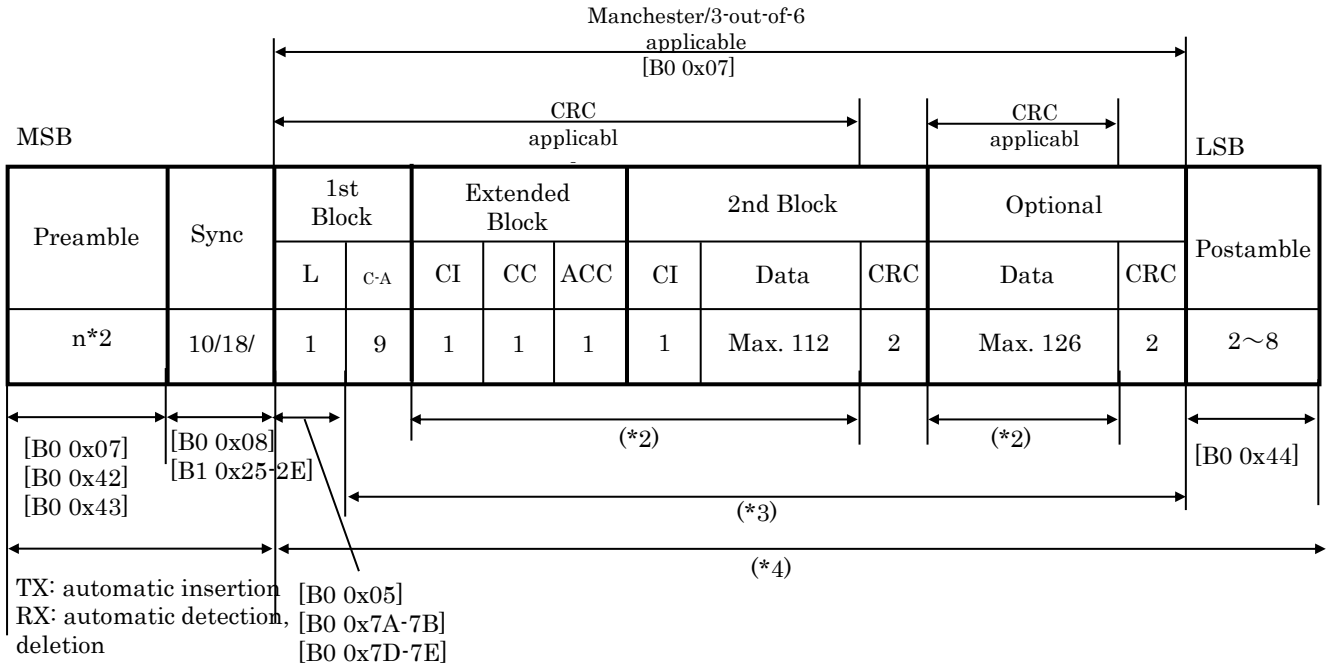
Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) is set to 0x8C/0x8D/0x8E/0x8, Extended Link Layer format is applied and the packet format is extended as follows:

(a) CI-field = 0x8C

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b01 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00 If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to the normal format of Format B.

*2: Indicates TX FIFO data storage area upon TX.

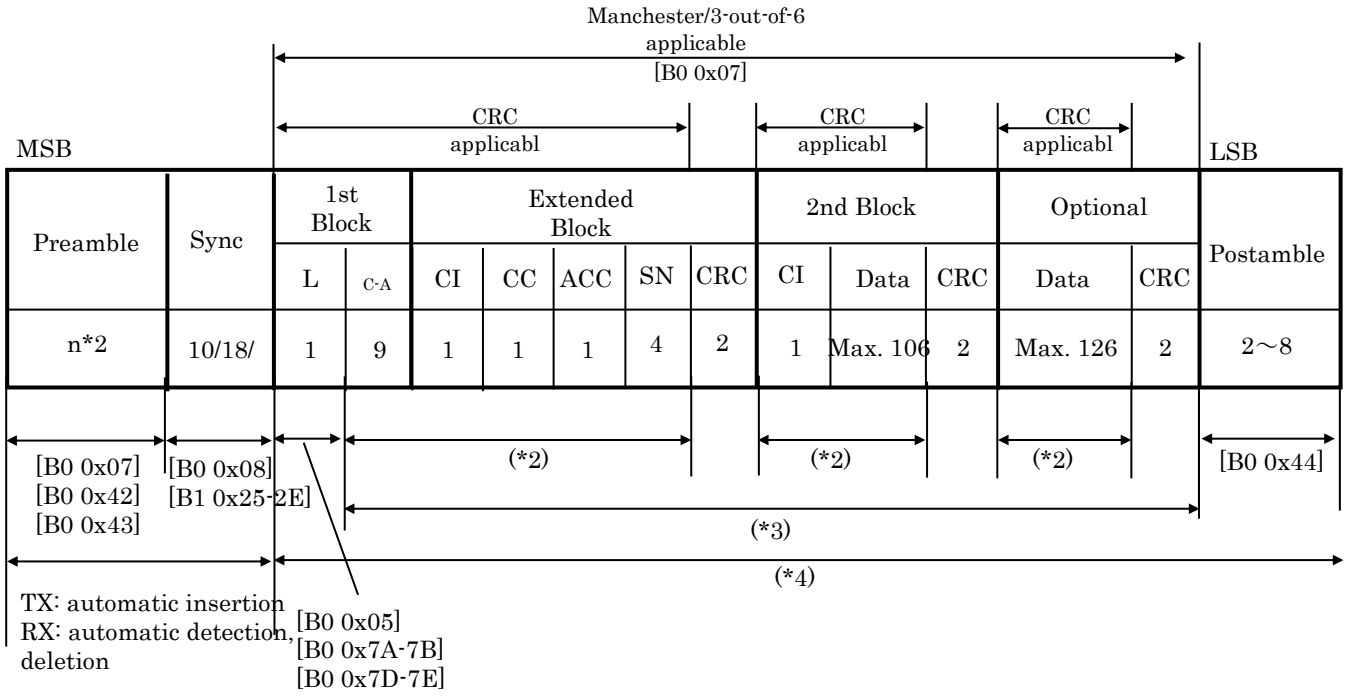
*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(b) CI-field = 0x8D

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b10 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00 If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to Format B without "Extended Block".

*2: Indicates TX FIFO data storage area upon TX.

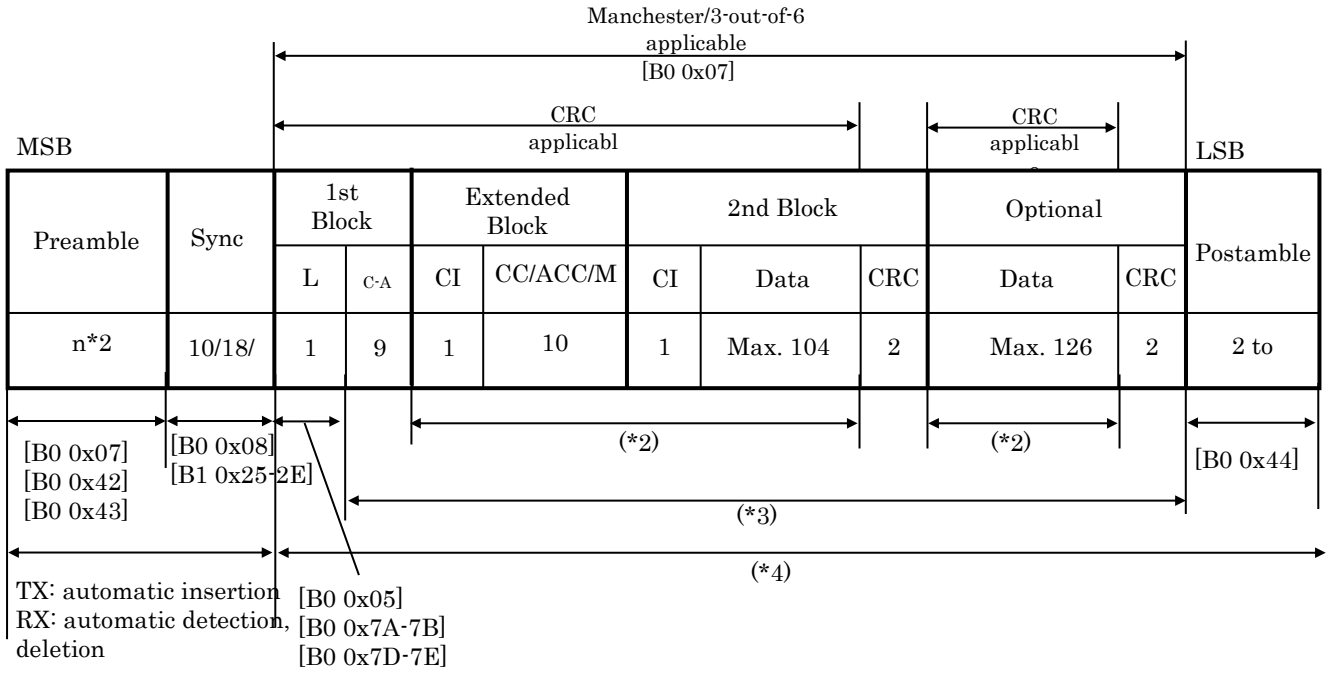
*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(c) CI-field = 0x8E

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b01. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to Format B without "Extended Block".

*2: Indicates TX FIFO data storage area upon TX.

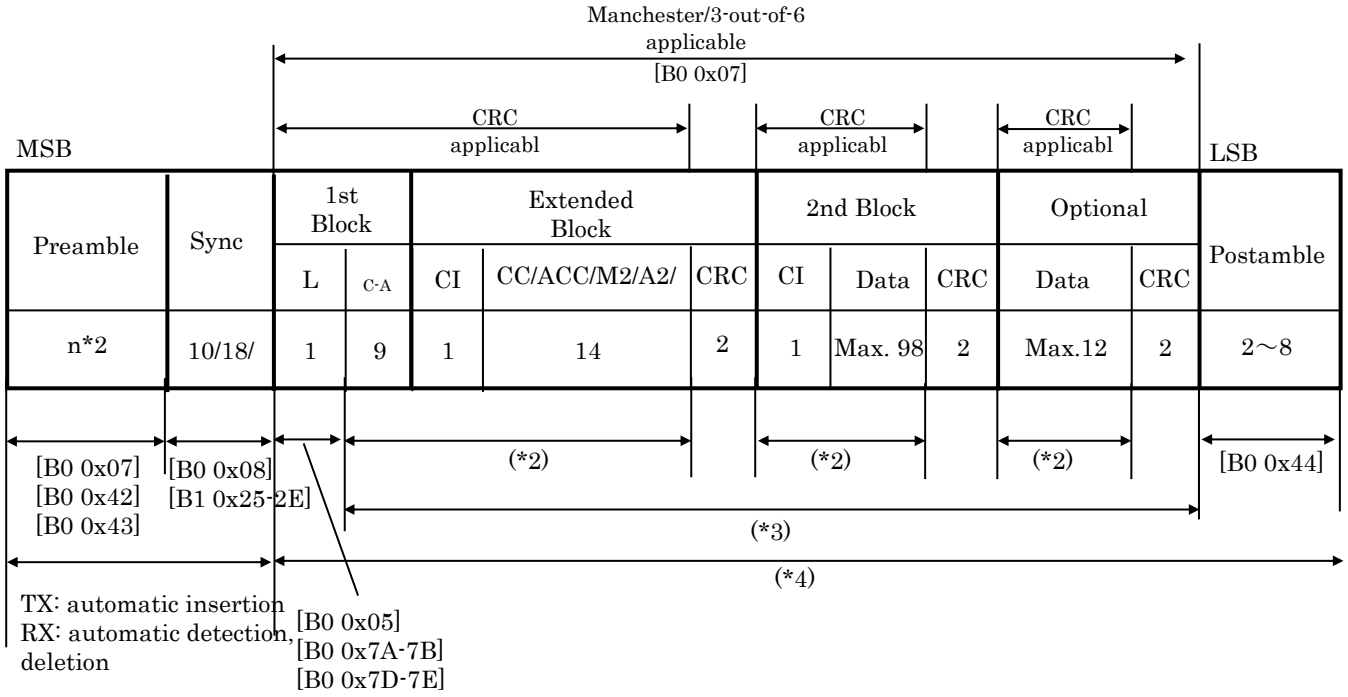
*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(d) CI-field = 0x8F

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b10. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

The following [] indicates register address [bank #, address].



*1: 1st Block is equal to Format B without Extended Block".

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

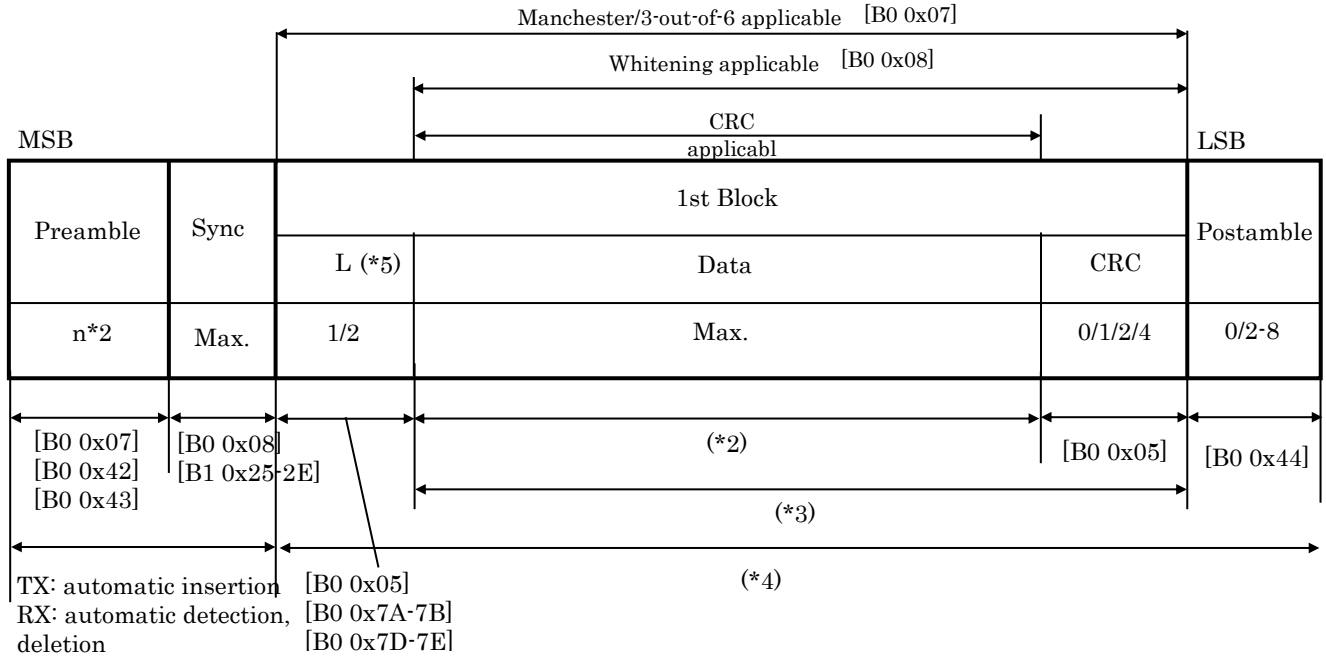
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(3) Format C (non-Wireless M-Bus, general purpose format)

To use Format C, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b10.

Format C consists of 1st Block only, which has 2 bytes of CRC. "L-field" (1st one or two bytes of 1st Block) indicates packet Length, which indicates the total byte count from Data-field to final CRC data. Data Whitening function is supported.

The following [] indicates register address [bank #, address].



*1: Preamble length (n) is programmable by [TXPR_LEN_H/L: B0 0x42/43] registers.

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

*5: IEEE802.15.4g can be supported by setting L-field to 2-byte mode (LENGTH_MODE([PKT_CTRL: B0 0x05(1-0)]) = 0b01). The correspondence between L-field and PHR format specified in IEEE802.15.4g is as follows. For information on other settings for supporting IEEE802.15.4g, refer to "Resister Setting - IEEE802.15.4g Mode Setting." Note that ML7436N does not support the Mode Switch function.

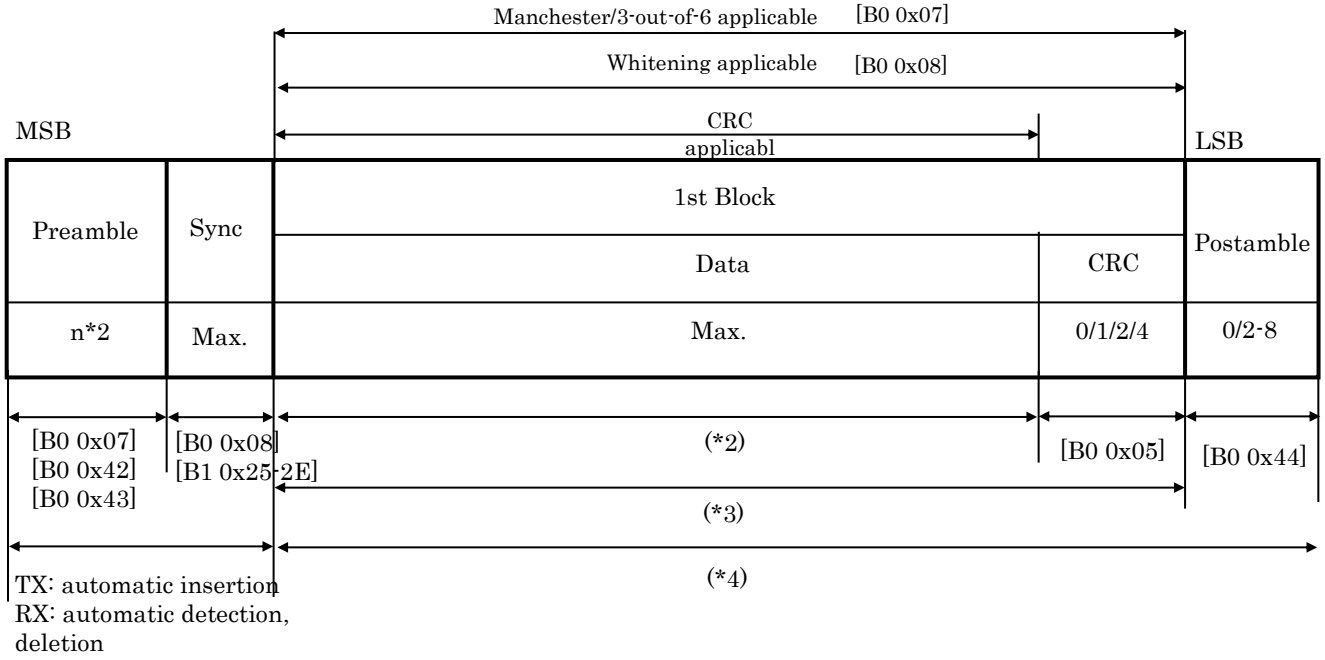
L-field		[TX_PKT_LEN: B0 0x7A]					[TX_PKT_LEN: B0 0x7B]
		Bit 7	Bit 6-5	Bit 4	Bit 3	Bit 2-0	Bit 7-0
IEEE802.15.4g PHR	Bits	0	1-2	3	4	5-7	8-15
	Function	Mode Switch	Reserved	FCS Type	Data Whitening	Frame Length(L_{10}-L_0)	

(4) Format D (non-Wireless M-Bus, general purpose format)

To use Format D, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b11.

Format D consists of 1st Block only, which starts with Data field followed by CRC-field (selectable from 0/1/2 bytes). "L-field" indicates the total byte count from Data-field to final CRC data and is set by [TX_PKT_LENGTH: B0 0x7A/0x7B] or [RX_PKT_LENGTH: B0 0x7D/0x7E].

The following [] indicates register address [bank #, address].



*1: Preamble length (n) is programmable by [TXPR_LEN_H/L: B0 0x42/43] registers.

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

*4: Indicates DCLK/DIO area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

6-11-3-2 ○CRC Function

ML7436N has CRC32,CRC16 and CRC8 function. CRC is calculated and appended to TX data. CRC is checked for RX data. The following modes are used for automatic CRC appending and automatic CRC check. In addition, they can be set using the registers shown in the following table.

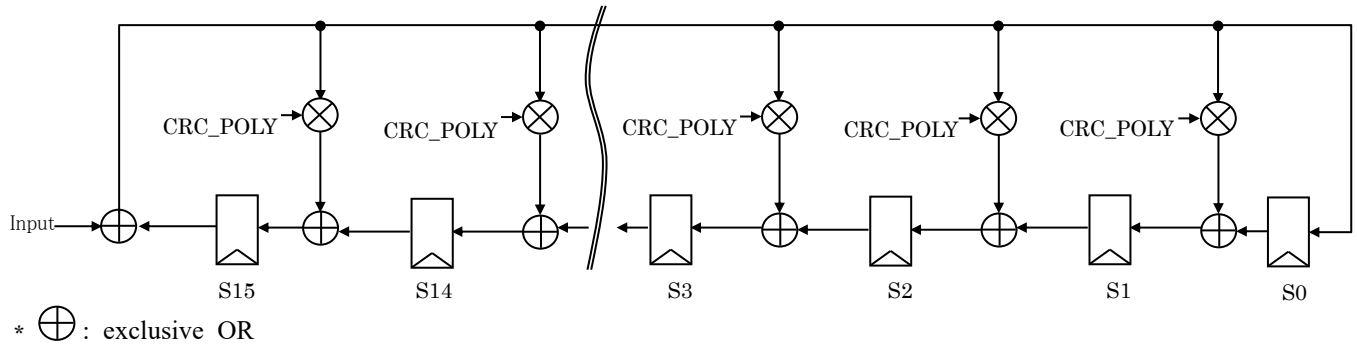
- FIFO mode --- RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b00
- DIO mode --- RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b11

Function	Register
TX CRC setting	TX_CRC_EN([PKT_CTRL2: B0 0x05(2)])
RX CRC setting	RX_CRC_EN([PKT_CTRL2: B0 0x05(3)])
CRC length setting	CRC_LEN([PKT_CTRL2: B0 0x05(5-4)])
CRC complement value OFF setting	CRC_COMP_OFF([PKT_CTRL2: B0 0x05(6)])
CRC polynomial setting	[CRC_POLY3/2/1/0: B1 0x16/17/18/19]
CRC error status	[CRC_ERR_H/M/L: B0 0x13/14/15]
CRC length setting 2 enable	CRC_LEN2_EN([CRC_ERR_H: B0 0x13(7)])
CRC length setting 2	CRC_LEN2([CRC_ERR_H: B0 0x13(6-5)])

Any CRC polynomials for CRC32/CRC16/CRC8 can be specified. Reset value is as follows:

CRC16 polynomial = $x^{16} + x^{12} + x^5 + 1$ (reset value)

CRC data will be generated by the following circuits. By programming [CRC_POLY3/2/1/0] registers, any CRC polynomials can be supported. Generated CRC will be transferred from the left most bit (S15). (Figure below) If the CRC function is used for data shorter than CRC length (3 bytes of CRC32 only), data 0s will be added before performing CRC calculation. CRC check result is indicated in [CRC_ERR_H/M/L] registers. Unlike Format C, Format A/B can include multiple CRC-fields in one packet. For multiple CRC-fields, the CRC check result closest to L-field will be indicated in CRC_ERR[0] ([CRC_ERR_L:B0 0x15(0)]). Subsequent bit will be indicated in CRC_ERR from MSB in sequence.



CRC polynomial circuits

General CRC polynomial can be programmed by below [CRC_POLY3/2/1/0] settings. CRC length can be set by CRC_LEN.

CRC polynomial		[CRC_POLY3/2/1/0]			
		(B1 0x16)	(B1 0x17)	(B1 0x18)	(B1 0x19)
CRC8	$x^8 + x^2 + x + 1$	0x00	0x00	0x00	0x03
CRC16	$x^{16} + x^{12} + x^5 + 1$	0x00	0x00	0x08	0x10
	$x^{16} + x^{15} + x^2 + 1$	0x00	0x00	0x40	0x02
	$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$	0x00	0x00	0x1E	0xB2
CRC32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	0x02	0x60	0x8E	0xDB

In addition, for ML7436N, CRC length for CRC calculation and CRC length for appending to packets (upon TX) or checking (upon RX) can be set individually. To do this, use CRC_LEN2_EN, CRC_LEN2, and CRC_LEN for setting.

CRC length for calculating CRC	CRC length for appending or checking CRC	CRC_LEN2_EN (B0 0x13(7))	CRC_LEN2 (B0 0x13(6-5))	CRC_LEN (B0 0x05(5-4))
CRC8	CRC8	0	-	0b00
CRC16	CRC8	1	0b01	0b00
	CRC16	0	-	0b01
CRC32	CRC8	1	0b10	0b00
	CRC16	1	0b10	0b01
	CRC32	0	-	0b10

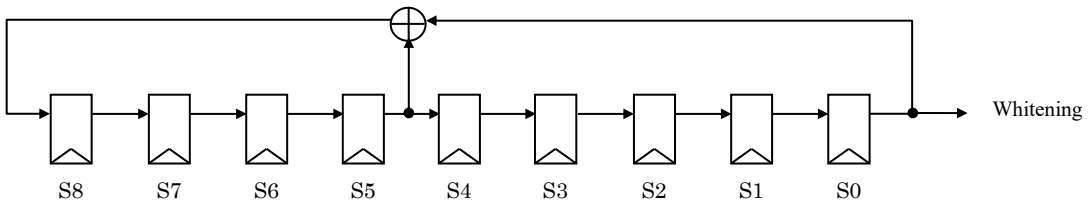
However, when different CRC lengths are set for calculating CRC and for appending to packets (upon TX) or checking (upon RX), "CRC length for calculating CRC" must be longer than or equal to "CRC length for appending to packets (upon TX) or checking (upon RX)."

6-11-3-3 ○Data Whitening Function

ML7436N supports the Data Whitening function. In packet format A/B, data succeeding C-field is the target area for Whitening. In packet format C, data succeeding Data-field is the target area for Whitening. Data generated by the following 9-bit pseudo random noise sequence (PN9) generation circuit will be XORed with TX data (encoded in 3-out-of-6 coding) before transmission and transmitted. Initialization value of the PN9 generation circuit shift register can be set by [WHT_INIT_H/L: B1 0x64/65] registers. PN9 polynomial can be set to any polynomial by [WHT_CFG: B1 0x66].

Function	Register
Data Whitening setting enable	WHT_SET ([DATA_SET2: B0 0x08(0)])
Data Whitening initialization value	[WHT_INIT_H/L: B1 0x64/65]
Whitening polynomial	[WHT_CFG: B1 0x66]

When [WHT_CFG: B1 0x66(0)] is set to 0b1, the polynomial setting function feeds back the shift register S1 output to XOR. In a similar way, when [WHT_CFG: B1 0x66(1)] is set to 0b1, it feeds back the shift register S2 output to XOR, and [WHT_CFG: B1 0x66(7-2)] also has a similar function. Two or more bits can be also set to 0b1. Therefore any type of PN9 polynomial can be programmed.



* ⊕ : Exclusive OR

Whitening data generation circuits
(Polynomial: $x^9 + x^5 + 1$)

The correspondence between typical PN9 polynomials and [WHT_CFG: B1 0x66] setting is as follows.

PN9 polynomial	[WHT_CFG: B1 0x66]
$x^9 + x^4 + 1$	0x08
$x^9 + x^5 + 1$	0x10

6-11-3-4 ○SyncWordDetection Function

ML7436N supports automatic SyncWord recognition function. By having two sets of SyncWord pattern storage area, it is possible to detect two different packet format (Format A/B) which are defined by Wireless M-Bus. (For details, please refer to Wireless M-BUS standard) Receiving packet format is indicated by SW_DET_RSLT([STM_STATE:B0 0x77(5)]). In addition, when Two SyncWords waiting setting is set for Format C/D, it is possible to wait for two SyncWords. but detected result is not indicated.

1) TX

SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. SyncWord length for TX is defined by SYNC_WORD_LEN ([SYNC_WORD_LEN: B1 0x25(5-0)]). Data of each SyncWord pattern of the defined SyncWord length will be transmitted from higher bit.

SYNCWORD_SEL	TX SyncWord pattern
0	SYNCWORD1_SET[31:0] ([SYNCWORD1_SET0/1/2/3: B1 0x27/28/29/2A])
1	SYNCWORD2_SET[31:0] ([SYNCWORD2_SET0/1/2/3: B1 0x2B/2C/2D/2E])

Example) SyncWord pattern and SyncWord length

If the following registers are programmed, 18 bits of SYNCWORD1_SET [17:0] will be transmitted from higher bit sequentially.

[SYNC_WORD_LEN: B1 0x25]=0x12

SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b0

If the following registers are programmed, 24 bits of SYNCWORD2_SET [23:0] will be transmitted from higher bit sequentially.

[SYNC_WORD_LEN: B1 0x25]=0x18

SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b1

2) RX

By setting SYNCWORD_SEL and 2SW_DET_EN ([DATA_SET2: B0 0x08(3)]), one pattern waiting or two patterns waiting can be selected as shown in the following table. Packet format automatic detection is valid only when 2SW_DET_EN = 0b1 and Format A/B is selected. Packet format automatic detection result for two patterns waiting is indicated in SW_DET_RSLT[STM_STATE: B0 0x77(5)].

2SW_DET_EN	SYNCWORD_SEL	SyncWord pattern During Sync Detection	SyncWord Detection operation	Automatic packet format detection	Data process after SyncWord
0	0	SYNCWORD1_SET[31:0]	Waiting for one pattern	No	Process according to each Format setting
0	1	SYNCWORD2_SET[31:0]	Waiting for one pattern	No	Process according to each Format setting
1	-	SYNCWORD1_SET[31:0] SYNCWORD2_SET[31:0]	Waiting for two patterns	Supported	[Format A or Format B setting] If matched with SYNCWORD1_SET, process as Format A. If matched with SYNCWORD2_SET, process as Format B. [Format C setting] Process as Format C

Length of SyncWord pattern referred to at detection can be defined by SYNC_WORD_LEN ([SYNC_WORD_LEN: B1 0x25(5-0)]). In this case, SyncWord pattern of the SyncWord length from the lowest bit of SYNCWORD1_SET or SYNCWORD2_SET will be the reference pattern.

Example) SyncWord length

If the following registers are set, 18 bits of SYNCWORD1_SET[17:0] or SYNCWORD2_SET[17:0] will be the reference pattern for the SyncWord detection. Higher bits (bit31-18) are not checked.
[SYNC_WORD_LEN: B1 0x25]=0x12
[SYNC_WORD_EN: B1 0x26]=0x0F

32bit SyncWord pattern can be controlled by enabling/disabling by each 8bit, when receiving SyncWord. The following table describes enable/disable control and SyncWord pattern. However, note that when the SyncWord length setting is outside the range of bits for enable/disable control, the expected SyncWord detection is unavailable.

[SYNC_WORD_EN] Register (B1 0x26)	SYNCWORD*_SET				SyncWord detection operation
	[31:24]	[23:16]	[15:8]	[7:0]	
0000					Prohibited
0001	D.C.(*1)			ON	Only [7:0] are valid. The timing of SyncWord detection is after receiving bit[0].
0010	D.C.		ON	D.C.	Only [15:8] are valid. The timing of SyncWord detection is after receiving bit[0].
0011	D.C.		ON	ON	Only [15:0] are valid. The timing of SyncWord detection is after receiving bit[0].
0100	D.C.	ON	D.C.		Only [23:16] are valid. The timing of SyncWord detection is after receiving bit[0].
0101	D.C.	ON	D.C.	ON	Only [23:16] and [7:0] are valid. The timing of SyncWord detection is after receiving bit[0].

0110	D.C.	ON	ON	D.C.	Only [23:8] are valid. The timing of SyncWord detection is after receiving bit[0].
0111	D.C.	ON	ON	ON	Only [23:0] are valid. The timing of SyncWord detection is after receiving bit[0].
1000	ON	D.C.			Only [31:24] are valid. The timing of SyncWord detection is after receiving bit[0].
1001	ON	D.C.		ON	Only [31:24] and [7:0] are valid. The timing of SyncWord detection is after receiving bit[0].
1010	ON	D.C.	ON	D.C.	Only [31:24] and [15:8] are valid. The timing of SyncWord detection is after receiving bit[0].
1011	ON	D.C.	ON	ON	Only [31:24] and [15:0] are valid. The timing of SyncWord detection is after receiving bit[0].
1100	ON	ON	D.C.		[31:16] are valid. The timing of SyncWord detection is after receiving bit[0].
1101	ON	ON	D.C.	ON	Only [31:16] and [7:0] are valid. The timing of SyncWord detection is after receiving bit[0].
1110	ON	ON	ON	D.C.	[31:8] are valid. The timing of SyncWord detection is after receiving bit[0].
1111	ON	ON	ON	ON	[31:0] are valid. The timing of SyncWord detection is after receiving bit[0].

*1: D.C. stands for Don' t Care.

*2: Preamble pattern connecting with SyncWord can be added to the SyncWord detection conditions in addition to SyncWord pattern. To include preamble pattern, set RXPR_LEN([SYNC_CONDITION1: B0 0x45(5:0)]).

6-11-3-5 ○Field Check Function

ML7436N has a function for comparing the 9 bytes following C-field (Format A/B) or 13 bytes following Data-field (Format C/D) in a receiving packet and notifying through an interrupt when matching or not matching (Field check function). Field check can be possible with the following register setting. The Field check function is enabled only in FIFO mode for discriminating L-field (RXDIO_CTRL[DIO_SET: B0 0x0C(7-6)] = 0b00) and data output mode 2 of DIO mode (RXDIO_CTRL[DIO_SET: B0 0x0C(7-6)]=0b11).

Function	Register
RX data process setting when Field check unmatched	[C_CHECK_CTRL: B0 0x1B(7)]
Field check interrupt setting	[C_CHECK_CTRL: B0 0x1B(6)]
C-field detection enable setting	[C_CHECK_CTRL: B0 0x1B(4-0)]
M-field detection enable setting	[M_CHECK_CTRL: B0 0x1C(3-0)]
A-field detection enable setting	[A_CHECK_CTRL: B0 0x1D(5-0)]
C-field code setting	[C_FIELD_CODE1: B4 0x05] [C_FIELD_CODE2: B4 0x06] [C_FIELD_CODE3: B4 0x07] [C_FIELD_CODE4: B4 0x08] [C_FIELD_CODE5: B4 0x09] [C2_FIELD_CODE1: B4 0x22] [C3_FIELD_CODE1: B4 0x32]
M-field code setting	[M_FIELD_CODE1: B0 0x23] [M_FIELD_CODE2: B0 0x24] [M_FIELD_CODE3: B0 0x25] [M_FIELD_CODE4: B0 0x26] [M2_FIELD_CODE1: B4 0x23] [M2_FIELD_CODE2: B4 0x24] [M3_FIELD_CODE1: B4 0x33] [M3_FIELD_CODE2: B4 0x34]
A-field code setting	[A_FIELD_CODE1: B4 0x0E] [A_FIELD_CODE2: B4 0x0F] [A_FIELD_CODE3: B4 0x10]

	[A_FIELD_CODE4: B4 0x11] [A_FIELD_CODE5: B4 0x12] [A_FIELD_CODE6: B4 0x13] [A_FIELD_CODE7: B4 0x14] [A_FIELD_CODE8: B4 0x15] [A_FIELD_CODE9: B4 0x16] [A_FIELD_CODE10: B4 0x17] [A2_FIELD_CODE1: B4 0x25] [A2_FIELD_CODE2: B4 0x26] [A2_FIELD_CODE3: B4 0x27] [A2_FIELD_CODE4: B4 0x28] [A2_FIELD_CODE5: B4 0x29] [A2_FIELD_CODE6: B4 0x2A] [A2_FIELD_CODE7: B4 0x2B] [A2_FIELD_CODE8: B4 0x2C] [A2_FIELD_CODE9: B4 0x2D] [A2_FIELD_CODE10: B4 0x2E] [A3_FIELD_CODE1: B4 0x35] [A3_FIELD_CODE2: B4 0x36] [A3_FIELD_CODE3: B4 0x37] [A3_FIELD_CODE4: B4 0x38] [A3_FIELD_CODE5: B4 0x39] [A3_FIELD_CODE6: B4 0x3A] [A3_FIELD_CODE7: B4 0x3B] [A3_FIELD_CODE8: B4 0x3C] [A3_FIELD_CODE9: B4 0x3D] [A3_FIELD_CODE10: B4 0x3E]
Field check result indication	[FIELD_CHECK_RSLT: B0 0x64]

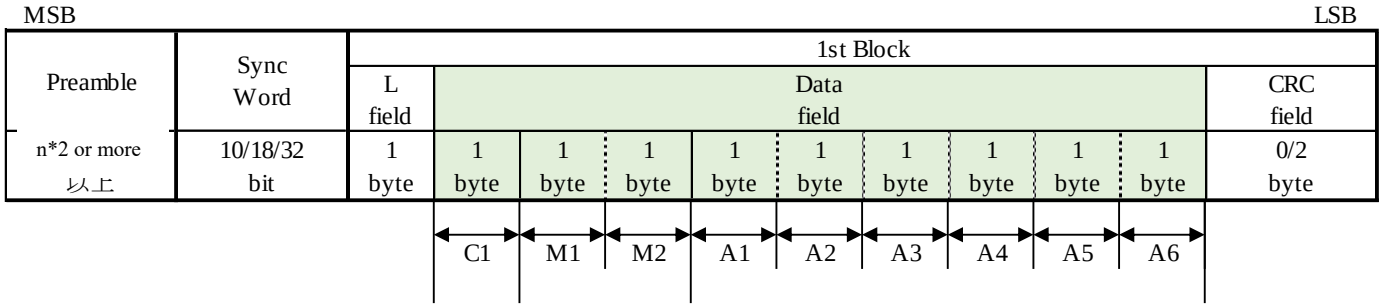
The following describes the relation between each comparison code and incoming RX data.

[Format A/B(Wireless M-Bus)]

Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all specified Field data (C-field/M-field/A-field) are matched, Field checking matching will be notified. However, if C-field data and C_FIELD_CODE5 are matched, even if other Field data (M-field/A-field) are not matched, Field check result will be notified as ”match”.

The following three patterns are settable, and Field data of different three patterns can be waited for and checked concurrently.

• Pattern 1



C1:[C2_FIELD_CODE1: B4 0x22]

M1:[M2_FIELD_CODE1: B4 0x23]
M2:[M2_FIELD_CODE2: B4 0x24]

A1:[A2_FIELD_CODE1: B4 0x25]
A2:[A2_FIELD_CODE2: B4 0x26]
A3:[A2_FIELD_CODE3: B4 0x27]
A4:[A2_FIELD_CODE4: B4 0x28]
A5:[A2_FIELD_CODE5: B4 0x29]
A6:[A2_FIELD_CODE6: B4 0x2A]

Check Field	Comparison Code	Conditions for match
C-field	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	Matches when one of the five comparison codes matches.
M-field 1st byte	M_FIELD_CODE1 or M_FIELD_CODE2	Matches when one of the two comparison codes matches.
M-field 2nd byte	M_FIELD_CODE3 or M_FIELD_CODE4	Matches when one of the two comparison codes matches.
A-field 1st byte	A_FIELD_CODE1	Matches when the comparison code matches.
A-field 2nd byte	A_FIELD_CODE2	Matches when the comparison code matches.

A-field 3rd byte	A_FIELD_CODE3	Matches when the comparison code matches.
A-field 4th byte	A_FIELD_CODE4	Matches when the comparison code matches.
A-field 5th byte	A_FIELD_CODE5	Matches when the comparison code matches.
A-field 6th byte	A_FIELD_CODE16	Matches when the comparison code matches.

• Pattern 2

MSB LSB

Preamble	Sync Word	1st Block										
		L field	Data field									CRC field
n*2 or more	10/18/32 bit	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	0/2 byte
			C1	M1	M2	A1	A2	A3	A4	A5	A6	

C1:[C2_FIELD_CODE1 : B4 0x22]

M1:[M2_FIELD_CODE1 : B4 0x23]
M2:[M2_FIELD_CODE2 : B4 0x24]

A1:[A2_FIELD_CODE1 : B4 0x25]
A2:[A2_FIELD_CODE2 : B4 0x26]
A3:[A2_FIELD_CODE3 : B4 0x27]
A4:[A2_FIELD_CODE4 : B4 0x28]
A5:[A2_FIELD_CODE5 : B4 0x29]
A6:[A2_FIELD_CODE6 : B4 0x2A]

Check Field	Comparison Code	Conditions for match
C-field	C2_FIELD_CODE1	Matches when the comparison code matches.
M-field 1st byte	M2_FIELD_CODE1	Matches when the comparison code matches.
M-field 2nd byte	M2_FIELD_CODE2	Matches when the comparison code matches.
A-field 1st byte	A_FIELD_CODE1	Matches when the comparison code matches.
A-field 2nd byte	A_FIELD_CODE2	Matches when the comparison code matches.
A-field 3rd byte	A_FIELD_CODE3	Matches when the comparison code matches.
A-field 4th byte	A_FIELD_CODE4	Matches when the comparison code matches.
A-field 5th byte	A_FIELD_CODE5	Matches when the comparison code matches.
A-field 6th byte	A_FIELD_CODE16	Matches when the comparison code matches.

• Pattern 3

MSB LSB

Preamble	Sync Word	1st Block										
		L field	Data field									CRC field
n*2 or more	10/18/32 bit	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	1 byte	0/2 byte
			C1	M1	M2	A1	A2	A3	A4	A5	A6	

C1:[C3_FIELD_CODE1 : B4 0x32]

M1:[M3_FIELD_CODE1 : B4 0x33]
M2:[M3_FIELD_CODE2 : B4 0x34]

A1:[A3_FIELD_CODE1 : B4 0x35]
A2:[A3_FIELD_CODE2 : B4 0x36]
A3:[A3_FIELD_CODE3 : B4 0x37]
A4:[A3_FIELD_CODE4 : B4 0x38]
A5:[A3_FIELD_CODE5 : B4 0x39]
A6:[A3_FIELD_CODE6 : B4 0x3A]

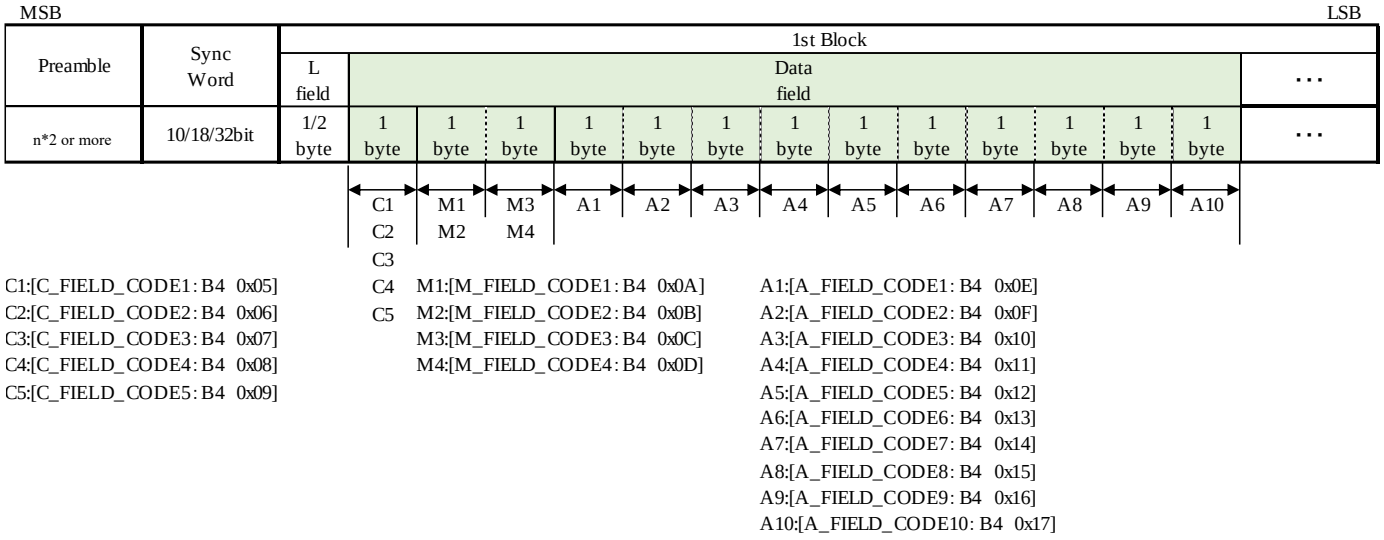
Check Field	Comparison Code	Conditions for match
C-field	C3_FIELD_CODE1	Matches when the comparison code matches.
M-field 1st byte	M2_FIELD_CODE1	Matches when the comparison code matches.
M-field 2nd byte	M2_FIELD_CODE2	Matches when the comparison code matches.
A-field 1st byte	A3_FIELD_CODE1	Matches when the comparison code matches.
A-field 2nd byte	A3_FIELD_CODE2	Matches when the comparison code matches.
A-field 3rd byte	A3_FIELD_CODE3	Matches when the comparison code matches.
A-field 4th byte	A3_FIELD_CODE4	Matches when the comparison code matches.
A-field 5th byte	A3_FIELD_CODE5	Matches when the comparison code matches.
A-field 6th byte	A3_FIELD_CODE6	Matches when the comparison code matches.

[Format C]

Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all the Data-field data satisfy the matching conditions shown in the following table, the Field check result will be notified as matching.. However, if the 1st byte of Data-field matches with C_FIELD_CODE5, the Field check result will be notified as matching even when other Field data (from 2nd byte to 9th byte of Data-field) do not match.

The following three patterns are settable, and Field data of different three patterns can be waited for and checked concurrently.

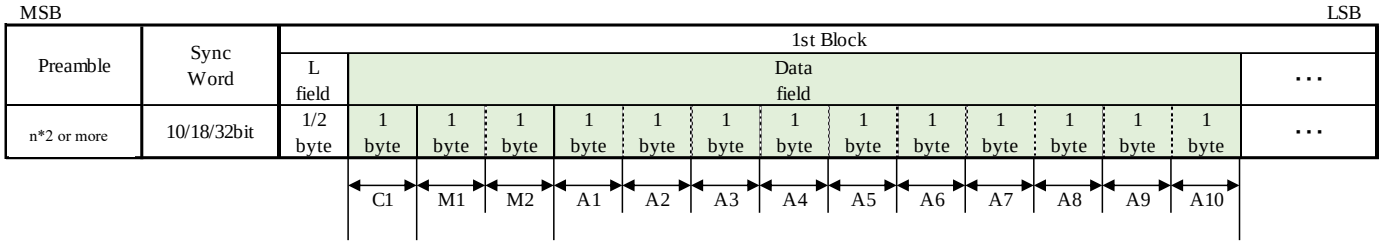
• Pattern 1



Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	Matches when one of the five comparison codes matches.
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	Matches when one of the two comparison codes matches.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	Matches when one of the two comparison codes matches.
Data-field 4th byte	A3_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A3_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A3_FIELD_CODE3	Matches when the comparison code matches.

Data-field 7th byte	A3_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A3_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A3_FIELD_CODE6	Matches when the comparison code matches.
Data-field 10th byte	A3_FIELD_CODE7	Matches when the comparison code matches.
Data-field 11th byte	A3_FIELD_CODE8	Matches when the comparison code matches.
Data-field 12th byte	A3_FIELD_CODE9	Matches when the comparison code matches.
Data-field 13th byte	A3_FIELD_CODE10	Matches when the comparison code matches.

• Pattern 2



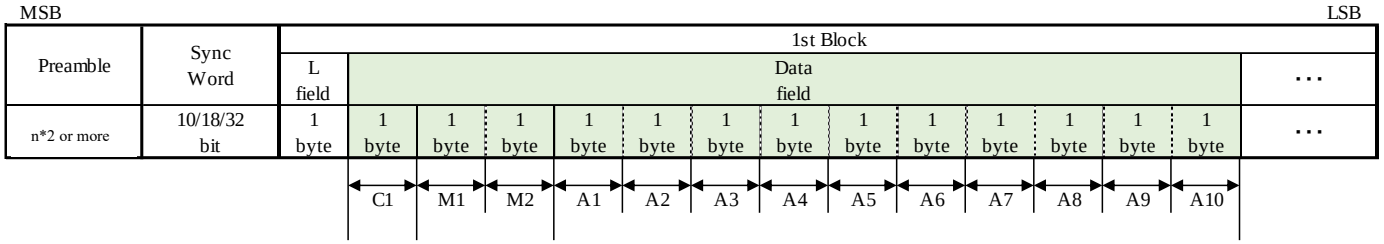
C1:[C2_FIELD_CODE1: B4 0x22]

M1:[M2_FIELD_CODE1: B4 0x23]
M2:[M2_FIELD_CODE2: B4 0x24]

A1:[A2_FIELD_CODE1: B4 0x25]
A2:[A2_FIELD_CODE2: B4 0x26]
A3:[A2_FIELD_CODE3: B4 0x27]
A4:[A2_FIELD_CODE4: B4 0x28]
A5:[A2_FIELD_CODE5: B4 0x29]
A6:[A2_FIELD_CODE6: B4 0x2A]
A7:[A2_FIELD_CODE7: B4 0x2B]
A8:[A2_FIELD_CODE8: B4 0x2C]
A9:[A2_FIELD_CODE9: B4 0x2D]
A10:[A2_FIELD_CODE10: B4 0x2E]

Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C2_FIELD_CODE1	Matches when the comparison code matches.
Data-field 2nd byte	M2_FIELD_CODE1	Matches when the comparison code matches.
Data-field 3rd byte	M2_FIELD_CODE2	Matches when the comparison code matches.
Data-field 4th byte	A3_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A3_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A3_FIELD_CODE3	Matches when the comparison code matches.
Data-field 7th byte	A3_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A3_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A3_FIELD_CODE6	Matches when the comparison code matches.
Data-field 10th byte	A3_FIELD_CODE7	Matches when the comparison code matches.
Data-field 11th byte	A3_FIELD_CODE8	Matches when the comparison code matches.
Data-field 12th byte	A3_FIELD_CODE9	Matches when the comparison code matches.
Data-field 13th byte	A3_FIELD_CODE10	Matches when the comparison code matches.

• Pattern 3



C1:[C3_FIELD_CODE1: B4 0x32]

M1:[M3_FIELD_CODE1: B4 0x33]
M2:[M3_FIELD_CODE2: B4 0x34]

A1:[A3_FIELD_CODE1: B4 0x35]
A2:[A3_FIELD_CODE2: B4 0x36]
A3:[A3_FIELD_CODE3: B4 0x37]
A4:[A3_FIELD_CODE4: B4 0x38]
A5:[A3_FIELD_CODE5: B4 0x39]
A6:[A3_FIELD_CODE6: B4 0x3A]
A7:[A3_FIELD_CODE7: B4 0x3B]
A8:[A3_FIELD_CODE8: B4 0x3C]
A9:[A3_FIELD_CODE9: B4 0x3D]
A10:[A3_FIELD_CODE10: B4 0x3E]

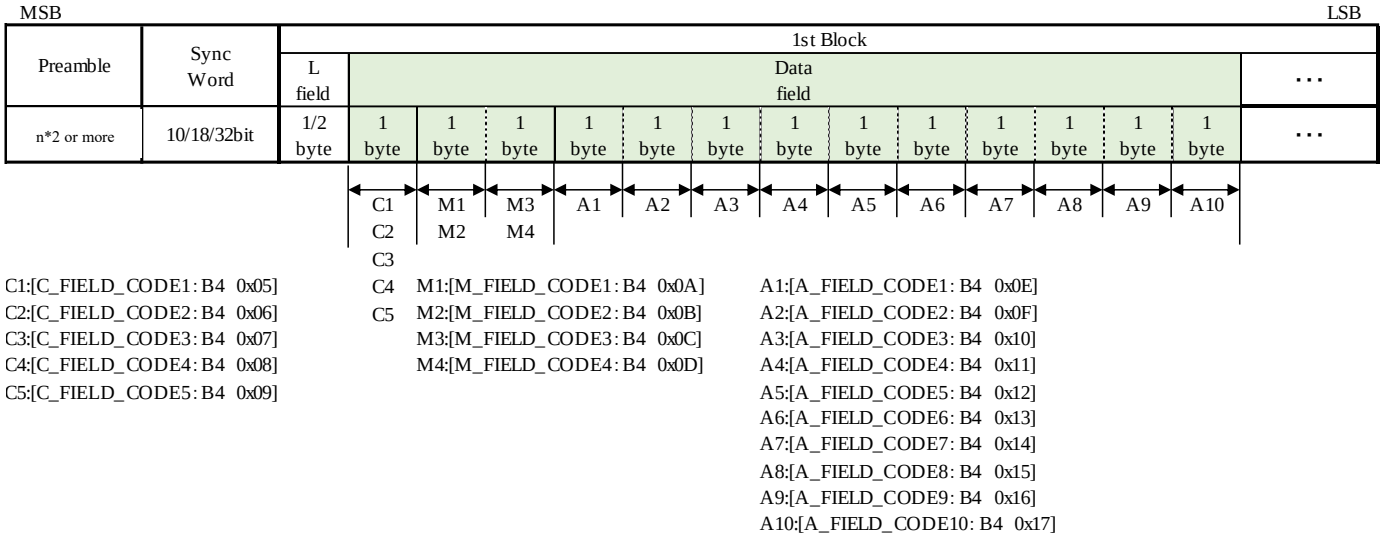
Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C3_FIELD_CODE1	Matches when the comparison code matches.
Data-field 2nd byte	M3_FIELD_CODE1	Matches when the comparison code matches.
Data-field 3rd byte	M3_FIELD_CODE2	Matches when the comparison code matches.
Data-field 4th byte	A_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A_FIELD_CODE3	Matches when the comparison code matches.
Data-field 7th byte	A_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A_FIELD_CODE6	Matches when the comparison code matches.
Data-field 10th byte	A_FIELD_CODE7	Matches when the comparison code matches.
Data-field 11th byte	A_FIELD_CODE8	Matches when the comparison code matches.
Data-field 12th byte	A_FIELD_CODE9	Matches when the comparison code matches.
Data-field 13th byte	A_FIELD_CODE10	Matches when the comparison code matches.

[Format D]

Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all specified Field data (specified table below) are matched, Field checking matching will be notified. However, if the 1st byte of Data-field matches with C_FIELD_CODE5, the Field check result will be notified as matching even when other Field data (from 2nd byte to 9th byte of Data-field) do not match.

The following three patterns are settable, and Field data of different three patterns can be waited for and checked concurrently.

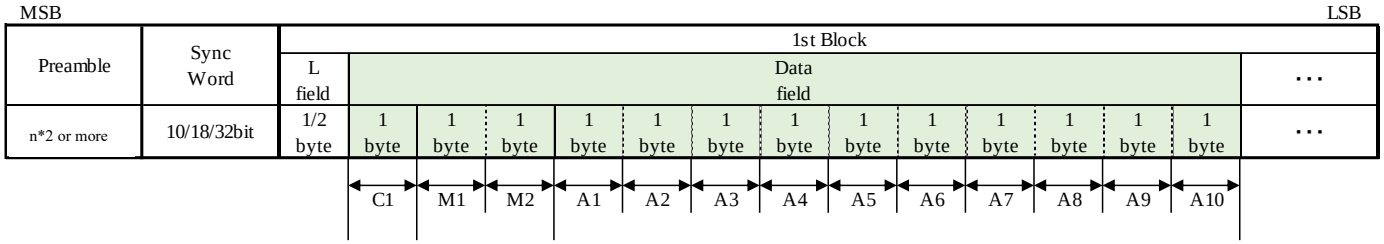
• Pattern 1



Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	Matches when one of the five comparison codes matches.
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	Matches when one of the two comparison codes matches.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	Matches when one of the two comparison codes matches.
Data-field 4th byte	A_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A_FIELD_CODE3	Matches when the comparison code matches.

Data-field 7th byte	A_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A_FIELD_CODE6	Matches when the comparison code matches.
Data-field 10th byte	A_FIELD_CODE7	Matches when the comparison code matches.
Data-field 11th byte	A_FIELD_CODE8	Matches when the comparison code matches.
Data-field 12th byte	A_FIELD_CODE9	Matches when the comparison code matches.
Data-field 13th byte	A_FIELD_CODE10	Matches when the comparison code matches.

• Pattern 2



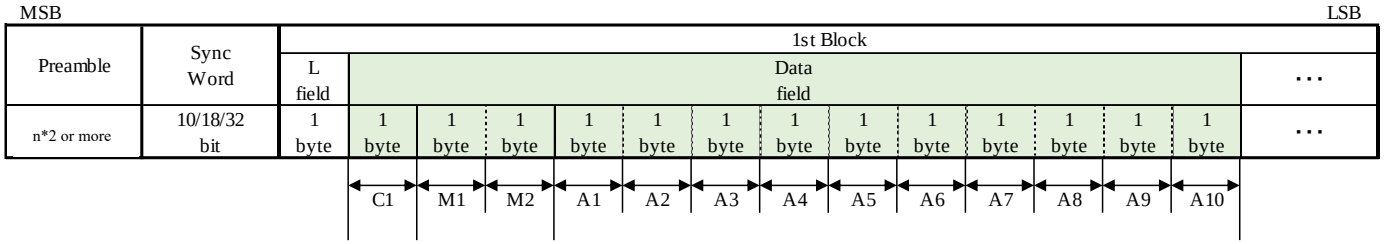
C1:[C2_FIELD_CODE1: B4 0x22]

M1:[M2_FIELD_CODE1: B4 0x23]
M2:[M2_FIELD_CODE2: B4 0x24]

A1:[A2_FIELD_CODE1: B4 0x25]
A2:[A2_FIELD_CODE2: B4 0x26]
A3:[A2_FIELD_CODE3: B4 0x27]
A4:[A2_FIELD_CODE4: B4 0x28]
A5:[A2_FIELD_CODE5: B4 0x29]
A6:[A2_FIELD_CODE6: B4 0x2A]
A7:[A2_FIELD_CODE7: B4 0x2B]
A8:[A2_FIELD_CODE8: B4 0x2C]
A9:[A2_FIELD_CODE9: B4 0x2D]
A10:[A2_FIELD_CODE10: B4 0x2E]

Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C2_FIELD_CODE1	Matches when the comparison code matches.
Data-field 2nd byte	M1_FIELD_CODE1	Matches when the comparison code matches.
Data-field 3rd byte	M2_FIELD_CODE2	Matches when the comparison code matches.
Data-field 4th byte	A2_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A2_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A2_FIELD_CODE3	Matches when the comparison code matches.
Data-field 7th byte	A2_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A2_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A2_FIELD_CODE6	Matches when the comparison code matches.
Data-field 10th byte	A2_FIELD_CODE7	Matches when the comparison code matches.
Data-field 11th byte	A2_FIELD_CODE8	Matches when the comparison code matches.
Data-field 12th byte	A2_FIELD_CODE9	Matches when the comparison code matches.
Data-field 13th byte	A2_FIELD_CODE10	Matches when the comparison code matches.

• Pattern 3



C1:[C3_FIELD_CODE1: B4 0x32]

M1:[M3_FIELD_CODE1: B4 0x33]
M2:[M3_FIELD_CODE2: B4 0x34]

A1:[A3_FIELD_CODE1: B4 0x35]
A2:[A3_FIELD_CODE2: B4 0x36]
A3:[A3_FIELD_CODE3: B4 0x37]
A4:[A3_FIELD_CODE4: B4 0x38]
A5:[A3_FIELD_CODE5: B4 0x39]
A6:[A3_FIELD_CODE6: B4 0x3A]
A7:[A3_FIELD_CODE7: B4 0x3B]
A8:[A3_FIELD_CODE8: B4 0x3C]
A9:[A3_FIELD_CODE9: B4 0x3D]
A10:[A3_FIELD_CODE10: B4 0x3E]

Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C3_FIELD_CODE1	Matches when the comparison code matches.
Data-field 2nd byte	M1_FIELD_CODE1	Matches when the comparison code matches.
Data-field 3rd byte	M2_FIELD_CODE2	Matches when the comparison code matches.
Data-field 4th byte	A3_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A3_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A3_FIELD_CODE3	Matches when the comparison code matches.
Data-field 7th byte	A3_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A3_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A3_FIELD_CODE6	Matches when the comparison code matches.
Data-field 10th byte	A3_FIELD_CODE7	Matches when the comparison code matches.
Data-field 11th byte	A3_FIELD_CODE8	Matches when the comparison code matches.
Data-field 12th byte	A3_FIELD_CODE9	Matches when the comparison code matches.
Data-field 13th byte	A3_FIELD_CODE10	Matches when the comparison code matches.

●Packet processing as a result of Field checking

By setting CA_RXD_CLR ([C_CHECK_CTRL: B0 0x1B(7)]) = 0b1 and CA_INT_CTRL ([C_CHECK_CTRL: B0 0x1B(6)]) = 0b1, if the result of Field check is unmatched, the data packet will be discarded and the state will become the next packet reception waiting state.

●Storing number of unmatched packets

Unmatched packets can be counted up to 2047 packets and results are indicated in [ADDR_CHK_CTR_H: B1 0x62] and [ADDR_CHK_CTR_L: B1 0x63]. This count value can be cleared by STATE_CLR4([STATE_CLR: B0 0x16(4)]).

●Field check result indication

Field check result of each pattern is indicated in FIELD_CHECK_RSLT1/2/3([FIELD_CHECK_RSLT: B0 0x64(2-0)]). In addition to that, when a packet complying with the IEEE802.15.4g packet is received, ACK request bit detection result is indicated in ACK_REQ_DET([FIELD_CHECK_RSLT: B0 0x64(3)]). They will be cleared when at the timing of SyncWord detection, and after that, the indication will be updated according to the Field check result and ACK request bit check result.

6-11-3-6 ○FIFO Control Function

ML7436N has on-chip TX FIFO (256 bytes) and RX FIFO (256 bytes). As TX/RX_FIFO do not support multiple packets, packet should be processed one by one. If RX FIFO keeps RX packet and next RX packet is received, RX FIFO will be overwritten. It applies to TX FIFO as well.
When receiving, RX data is stored in FIFO (byte by byte) and the host MCU will read RX data through SPI. When transmitting, host MCU write TX data to TX_FIFO through SPI and transmitting through RF.

Writing or reading to FIFO is through SPI with burst access. TX data is written to [WR_TX_FIFO: B0 0x7C] register. RX data is read from [RD_FIFO: B0 0x7F] register. Continuous access increments internal FIFO counter automatically and data is saved or output. If FIFO access is suspended during write or read operation, address will be kept until the packet process is completed. Therefore, when resuming FIFO access, next data will be resumed from the suspended address.

FIFO control register are as follows.

Function	Register
TX FIFO Full level setting	[TXFIFO_THRH: B0 0x17]
TX FIFO Empty level setting	[TXFIFO_THRL: B0 0x18]
RX FIFO Full level setting	[RXFIFO_THRH: B0 0x19]
RX FIFO Empty level setting	[RXFIFO_THRL: B0 0x1A]
FIFO readout setting	[FIFO_SET: B0 0x78]
RX FIFO data usage status indication	[RX_FIFO_LAST: B0 0x79]
TX packet Length setting	[TX_PKT_LEN_H/L: B0 0x7A/7B]
RX packet Length setting	[RX_PKT_LEN_H/L: B0 0x7D/7E]
TX FIFO	[WR_TX_FIFO: B0 0x7C]
FIFO read	[RD_FIFO: B0 0x7F]

TX – RX procedure using FIFO are as follows:
[TX]

(a) TX L-filed value is set to [TX_PKT_LEN_H: B0 0x7A], [TX_PKT_LEN_L: B0 0x7B]. If Length is 1 byte, [TX_PKT_LEN_L] register will be transmitted.
Length setting can be set by LENGTH_MODE([PKT_CTRL: B0 0x05(1-0)]).

(b) TX data is written to FIFO.

[Note]

1.If TX data write sequence is aborted during transmission, [STATE_CLR: B0 0x16] (TX FIFO clear) must be issued. Otherwise data pointer which manages data in the LSI keeps the status, preventing the proper FIFO process of the next packet.

For example, when an interrupt notification of TX FIFO access error ([INT_SOURCE_GRP3: B0 0x0F(4)]) is received, the TX data write sequence may be aborted. This interrupt can be generated when FIFO overrun (for example, data is written to TX FIFO when there is no available space in it) or underrun (for example, a transmission is attempted when FIFO is empty) occurs.

2.If the next writing sequence is performed when one packet data is stored, FIFO is overwritten.

3.Depending on the packet format, TX data Length value is different.
Format A: Data length excluding the Length and CRC areas is set as the Length value.
Format B: Data length excluding the Length area is set as the Length value.
Format C: Data length excluding the Length area is set as the Length value.
Format D: Data length from Data-field to CRC-field is set as the Length value.

[RX]

(1) Format A/B/C

(a) Read the L-field value (Length) from [RX_PKT_LEN_H: B0 0x7D], [RX_PKT_LEN_L: B0 0x7E].

(b) Read RX data from FIFO.

When reading from RX FIFO, set FIFO_R_SEL([FIFO_SET: B0 0x78(0)]) = 0b0. If FIFO_R_SEL=0b1 , TX_FIFO will be selected.

Data usage value of RX FIFO is indicated by [RX_FIFO_LAST: B0 0x79] register.

(2) Format D

(a) Set the data length (Length value) to [RX_PKT_LEN_H: B0 0x7D], [RX_PKT_LEN_L: B0 0x7E].

(b) Read RX data from FIFO.

When reading from RX FIFO, set FIFO_R_SEL([FIFO_SET: B0 0x78(0)]) = 0b0. If FIFO_R_SEL=0b1 , TX_FIFO will be selected.

Data usage value of RX FIFO is indicated by [RX_FIFO_LAST: B0 0x79] register.

[Note]

1. If reading RX data is terminated before reading all data, RX FIFO clear ([STATE_CLR: B0 0x16]) must be issued. Otherwise data pointer is kept in the LSI and the next packet is not processed properly.
2. If 1 packet data is kept in the RX_FIFO, next RX data will be overwritten. Read all the necessary RX data before receiving the next packet. Incidentally, to detect the next packet being received even though all the data has not been read, the SyncWord detection interrupt (INT[13](INT_SOURCE_GRP2: B0 0x0E(5))) can be used.
3. Control FIFO so that FIFO overrun and underrun do not occur.

There are following methods for controlling FIFO so that FIFO overrun and underrun do not occur.

(a) Read RX FIFO usage ([RX_FIFO_LAST: B0 0x79]) and read that amount of data from FIFO.

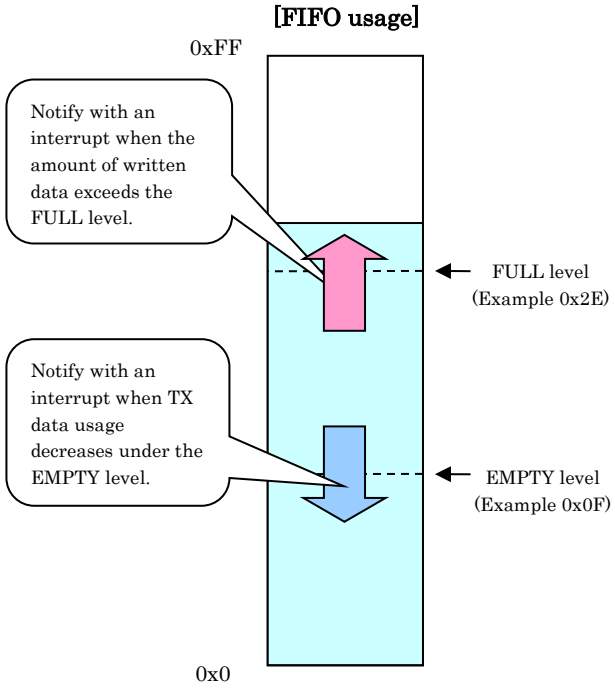
(b) Set the Full level of RX FIFO ([RXFIFO_THRH: B0 0x19]), and after a FIFO-Full interrupt (INT[5](INT_SOURCE_GRP1: B0 0x0D(5))) is generated, read data from FIFO up to the amount equivalent to the Full level of RX FIFO.

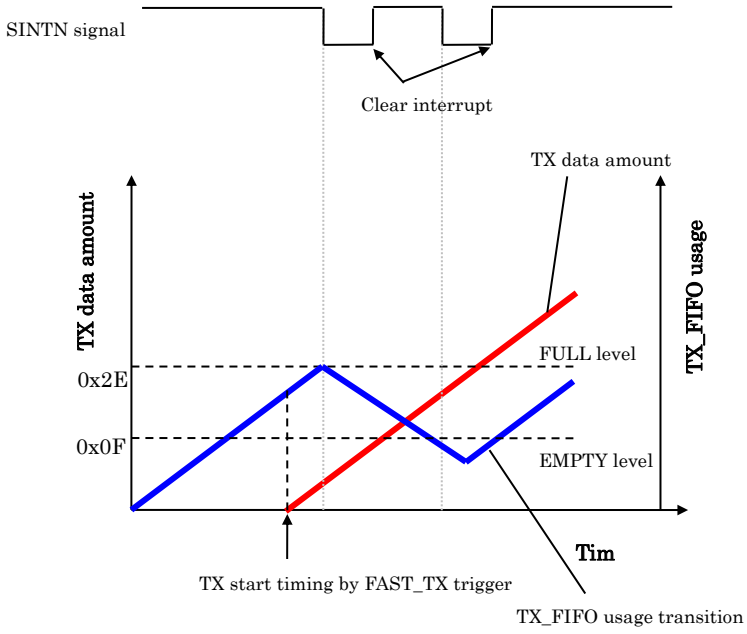
4. This function is valid during data receiving. FIFO-Empty interrupt does not occur after RX completion

If TX/RX packet is larger than the FIFO size, FIFO access control can be performed easily by using FIFO-Full trigger and FIFO-Empty trigger.

(1) TX FIFO usage notification function

This function is to notice TX_FIFO usage to the MCU using interrupt (SINTN). If the TX FIFO usage (un-transmitted data) exceeds the threshold (FULL level) set by [TXFIFO_THRH: B0 0x17], an interrupt will occur to notify about it. Also, if ML7436N transmits data and the TX FIFO usage decreases under the threshold (EMPTY level) set by [TXFIFO_THRL: B0 0x18], an interrupt will occur to notify about it. Interrupt notification signal (SINTN) can be output from GPIO*. For output settings, refer to [GPIO0_CTRL: B0 0x4E]、[GPIO1_CTRL: B0 0x4F]、[GPIO2_CTRL: B0 0x50]、[GPIO3_CTRL: B0 0x51]、[GPIO4_CTRL: B0 0x52]、[GPIO5_CTRL: B1 0x6D] (GPIO4 and GPIO5 are available for ML7436 only). Incidentally, the FULL level and EMPTY level become valid by setting 1 or more to [TXFIFO_THRH: B0 0x17], [TXFIFO_THRL: B0 0x18].





[Note]

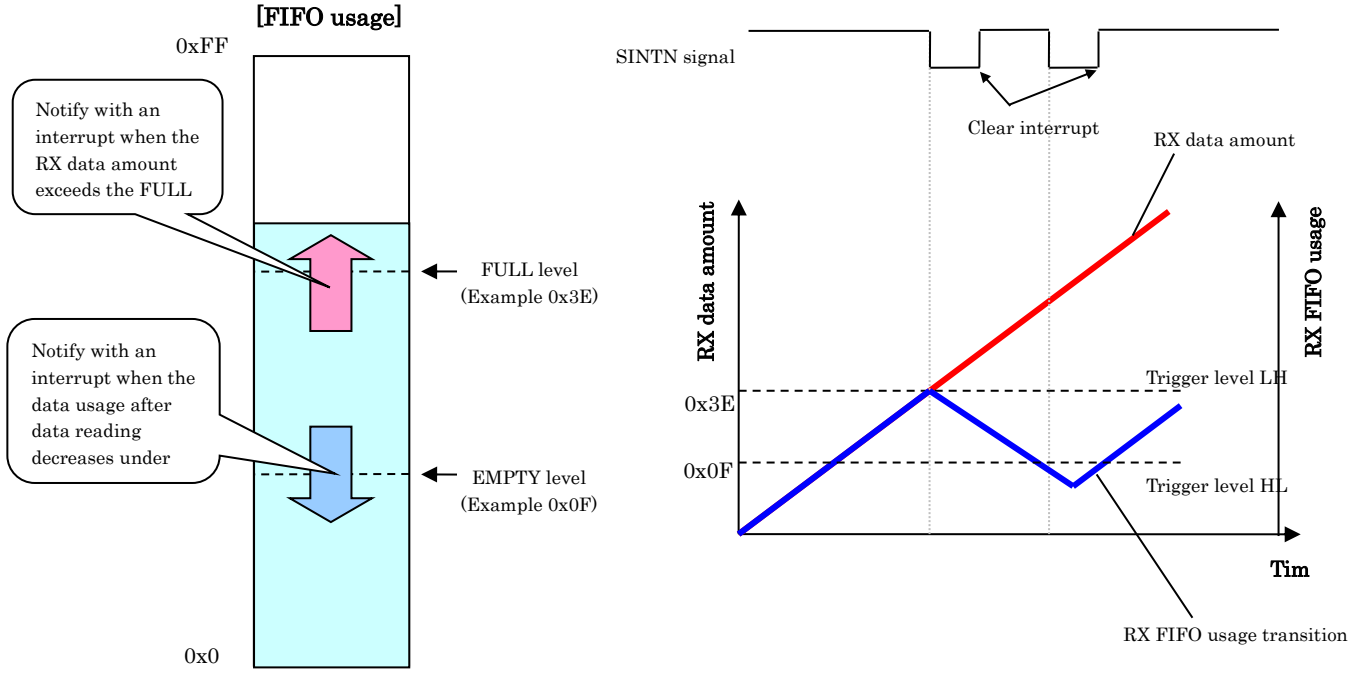
1. Do not set the notification levels of [TXFIFO_THRH] and [TXFIFO_THRL] to the same value._Set them as satisfying the condition [TXFIFO_THRH] > [TXFIFO_THRL].
2. The Full detection state in LSI is cleared at Full trigger ([TXFIFO_THRH])>FIFO usage, allowing the next Full trigger to be detected. Note that the above clear condition may be met during FIFO write, and the Full trigger may be detected, depending on the

timing of reading TX data (PHY) and FIFO write through SPI. To avoid such a case, disable the trigger level setting after the Full trigger is detected, and enable it again after the FIFO write is completed.

3. The Empty detection state of the inside of the LSI is cleared when the FIFO usage becomes larger than or equal to the Empty trigger ([TXFIFO_THRL]). After that, the next Empty trigger can be detected. Note that the above clear condition may be met during FIFO write, and the Empty trigger may be detected, depending on the timing of reading TX data (PHY) and FIFO write through SPI. To avoid such a case, make the trigger level setting disabled after the Empty trigger is detected, and make it enabled again after the FIFO write is completed.

(2) RX FIFO usage notification function

This function is to notify RX FIFO usage amount by using interrupt (SINTN) to the MCU. When the RX FIFO usage (un-read) exceeds the threshold set by [RXFIFO_THRH: B0 0x19] (FULL level), an interrupt will occur to notify about it. Also, after MCU reads RX data and un-read data amount of RX FIFO (FIFO usage) decreases under the threshold set by [RXFIFO_THRL: B0 0x1A] (EMPTY level), an interrupt will occur to notify about it. Interrupt notification signal (SINTN) can be output from GPIO*. For output settings, refer to [GPIO0_CTRL: B0 0x4E]、[GPIO1_CTRL: B0 0x4F]、[GPIO2_CTRL: B0 0x50]、[GPIO3_CTRL: B0 0[GPIO4_CTRL: B0 0x52]、[GPIO5_CTRL: B1 0x6D] (GPIO4 and GPIO5 are available for ML7436 only). Incidentally, the FULL level and EMPTY level become valid by setting 1 or more to [RXFIFO_THRH: B0 0x19], [RXFIFO_THRL: B0 0x1A].



[Note]

1. Do not set the notification levels of [RXFIFO_THRH] and [RXFIFO_THRL] to the same value. Set them as satisfying the condition [RXFIFO_THRH] > [RXFIFO_THRL].
2. The internal Full detection state is cleared at Full trigger ([RXFIFO_THRH])>FIFO usage, allowing the next Full trigger to be detected. Note that the above clear condition may be met during FIFO read, and the Full trigger may be detected, depending on the timing of writing RX data (PHY) and FIFO read through SPI. To avoid such a case, make the trigger level setting disabled after the Full trigger is detected, and make it enabled again after the FIFO read is completed.
3. The internal Empty detection state is cleared when the FIFO usage becomes larger than or equal to the Empty trigger ([RXFIFO_THRL]). After that, the next Empty trigger can be detected. Note that the above clear condition may be met during FIFO

read, and the Empty trigger may be detected, depending on the timing of writing RX data (PHY) and FIFO read through SPI. To avoid such a case, make the trigger level setting disabled after the Empty trigger is detected, and make it enabled again after the FIFO read is completed.

4. This function is valid during data receiving. FIFO-Empty interrupt does not occur after RX completion.

6-11-3-7 ○DIO Function

ML7436N can input/output TX/RX data with GPIO0 to 5 pins xor SDI/SDO pins. Output pins are controlled by [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [GPIO4_CTRL: B0 0x52], [GPIO5_CTRL: B1 0x6D], and [SPI/EXT_PA_CTRL: B0 0x53]. Data format for TX/RX are as follows.

TX --- TX data (NRZ or Manchester/3-out-of-6coding) will be input.

RX --- pre-decoded RX data or decoded RX data will be output. (Selectable by [DIO_SET: B0 0x0C])

DIO function registers are as follows.

Function	Register
DIO RX data output start setting	DIO_START([DIO_SET: B0 0x0C(0)])
DIO RX completion setting	DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)])
TX DIO mode setting	TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)])
RX DIO mode setting	RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)])
Enabling IO input/output direction setting for DIO	DIO_IODIR_SET_EN([DIO_SET: B0 0x0C(1)])
IO input/output direction setting for DIO	DIO_IODIR_SET([DIO_SET: B0 0x0C(3)])

(1) When using GPIO* pins

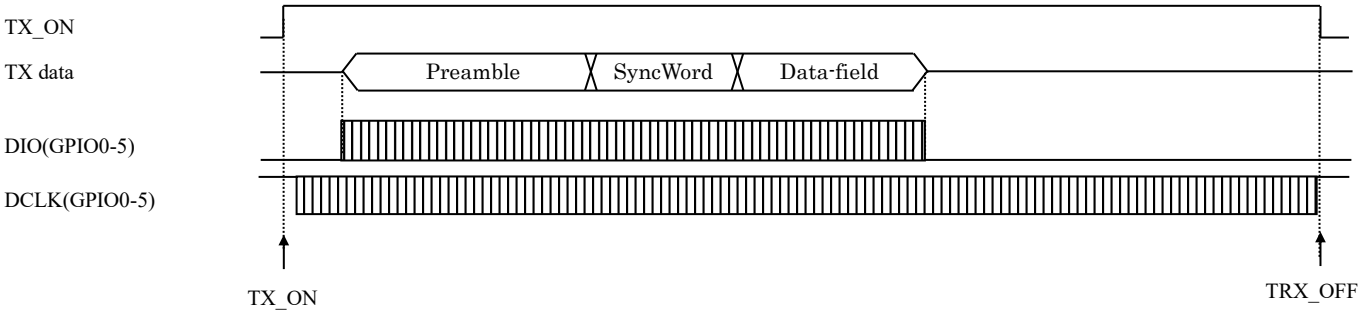
When GPIO0 to 5 pins are used to input/output TX/RX data, DCLK/DIO are controlled as follows. (below DIO/DCLK vertical line part indicate output or input period)

[TX]

(a) Continuous input mode

Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b01.

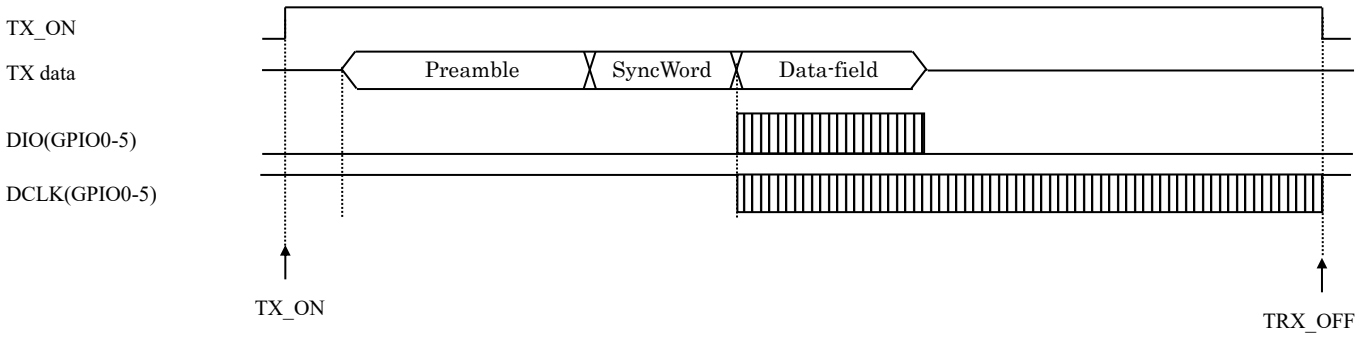
After TX_ON, the TX clock is output. At falling edge of the TX clock, TX data is input from the DIO pin. TX data must be encoded data.



(b) Data input mode

Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b10.

After TX_ON, the TX clock is output from data input timing after SyncWord. At falling edge of the TX clock, TX data is input from the DIO pin. TX data must be encoded data. Preamble and SyncWord generated automatically according to the registers setting.



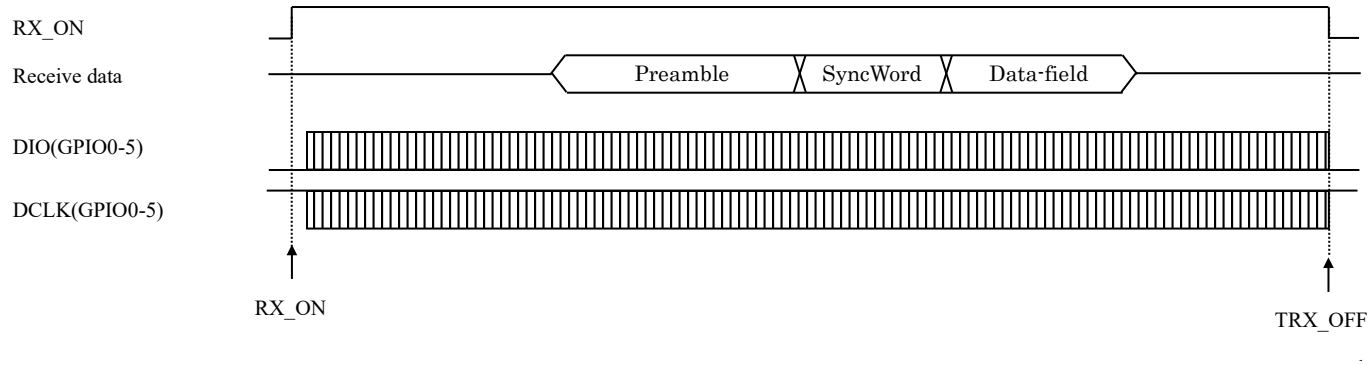
Preamble can be set by PB_PAT([DATA_SET1: B0 0x07(7)]、TXPR_LEN([TXPR_LEN_H/L: B0 0x42/43]). Also, SyncWord can be set by SYNCWORD_SEL([DATA_SET2:B0 0x08(4)) SYNCWORD_LEN([SYNC_WORD_LEN: B1 0x25)、SYNC_WORD_EN*([SYNC_WORD_EN: B1 0x26) SYNCWORD1_SET([SYNC WORD1_SET3/2/1/0: B1 0x27/28/29/2A) SYNCWORD2_SET([SYNCWORD2_SET3/2/1/0:B1 0x2B/2C/2D/2E).

[RX]

(a) Continuous output mode

Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b01.

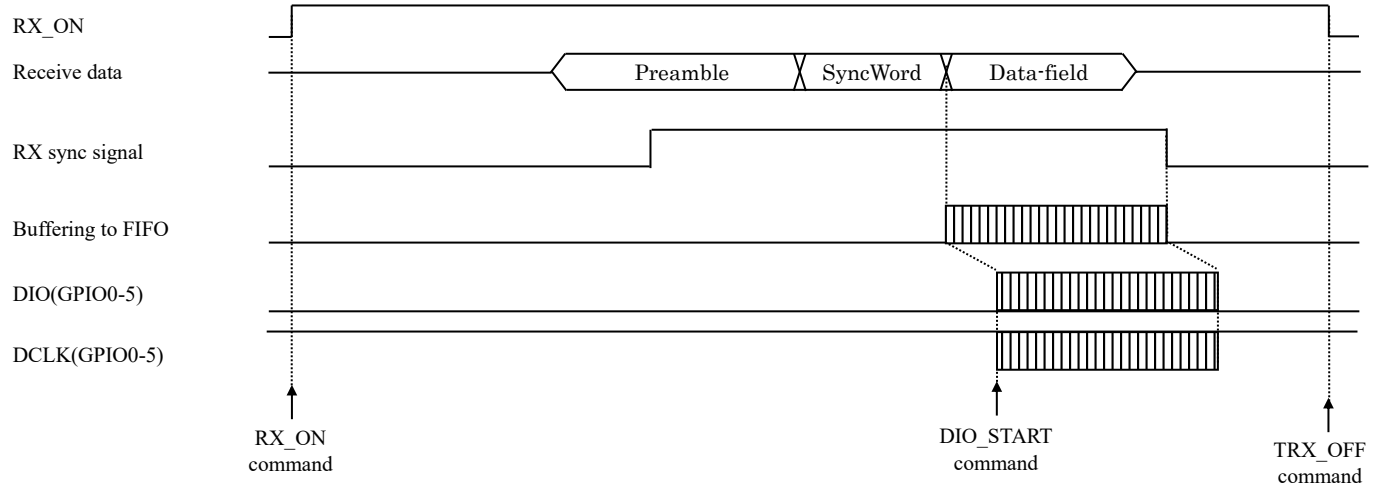
After RX_ON, the RX clock is output continuously. RX data (demodulated data) is output from the DIO output pin at falling edge of the RX clock. RX data is not buffered in FIFO.



(b) Data output mode 1

Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b10.

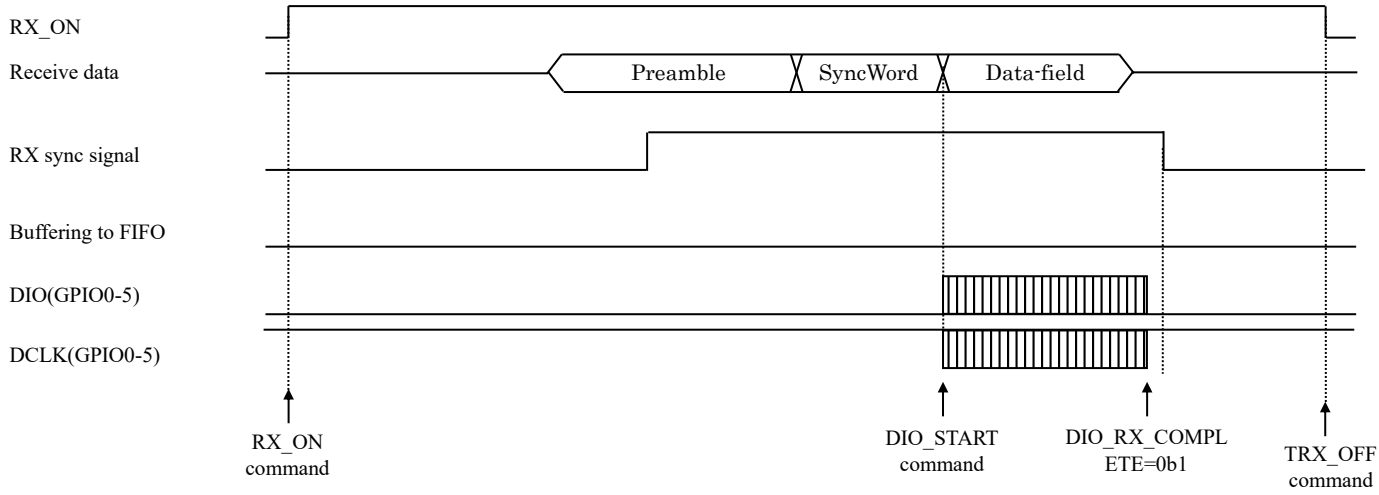
After SyncWord detection, RX data is buffered in RX FIFO. RX data buffering will continue until RX sync signal (SYNC) becomes "L". By RX data output setting DIO_START([DIO_SET: B0 0x0C(0)]), the buffered RX data will be output from the first byte through the DIO interface (DIO/DCLK) (RX data is output at falling edge of the RX clock). However, when RX data output setting is done after 256-byte time, data will be overwritten from the first byte. If all buffered data is output until SYNC becomes "L", RX completion interrupt (INT[8] group 2) will be generated. After RX completion, ready to receive next packet.



[Note]

1. RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after 1 byte access time upon SyncWord detection.
2. This mode does not process L-field. Field checking function is not supported.

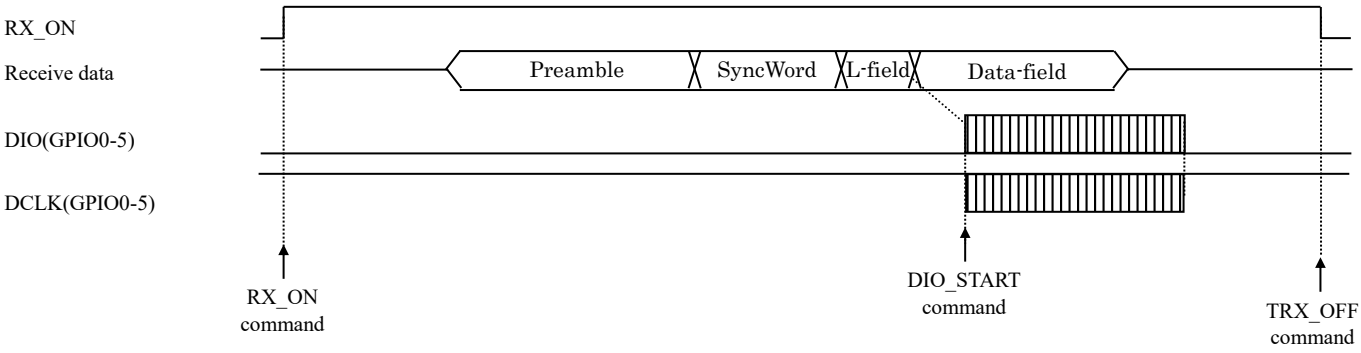
With this setting, when DIO_START is issued before SyncWord detection, data is not buffered in FIFO and RX data/clock is output after SyncWord detection. In order to complete RX before SYNC becomes L, set DIO RX completion setting (DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)])). After DIO_RX_COMPLETE setting, ready to receive the next packet.



(c) Data output mode 2

Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b11.

Only Data-field of RX data is buffered in FIFO. RX data of the amount of Length indicated by L-field is buffered in FIFO. By the RX data output setting (DIO_START([DIO_SET: B0 0x0C(0)])), buffered RX data is output from the first byte through the DIO interface (DIO/DCLK). However, if DIO_START setting is done after 256 byte timing, the top byte will be overwritten. If all data indicated by L-field is output, RX completion interrupt (INT[8] group2) will be generated. After RX completion, ready to receive next packet. Received Length information is indicated in [RX_PKT_LEN_H/L: B0 0x7D/7E]. This mode supports field check function.



[Note]

1. RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after elapsed time from SyncWord detection to L-field length + over 1byte access time.

(2) When using SDI/SDO pin (sharing with SPI interface)

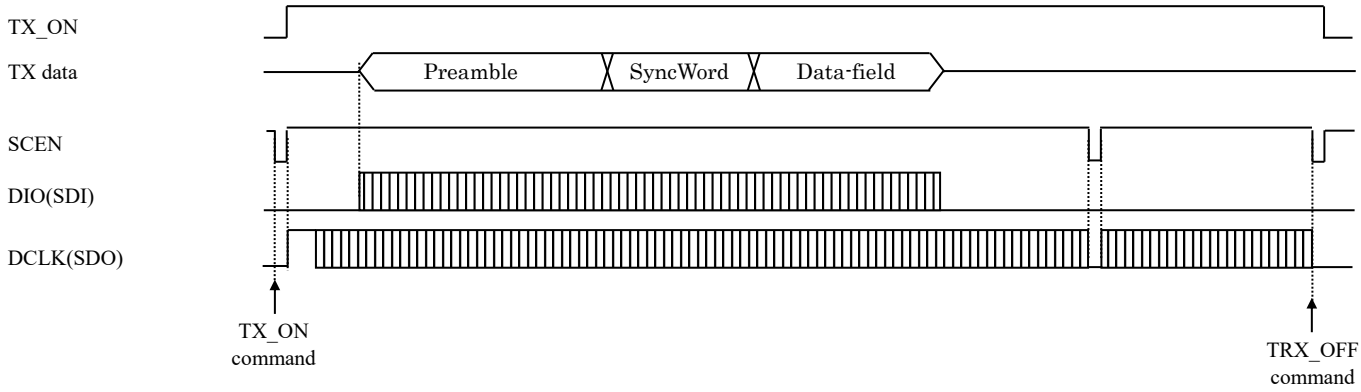
When the SPI interface (SDI/SDO) is used to input/output TX/RX data, DCLK/DIO are controlled as follows. (below DIO/DCLK vertical line part indicate output or input period) For information on the operation of each DIO mode, refer to the previous chapter "(1) When using GPIO* pins."

[TX]

(a) Continuous input mode

Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b01.

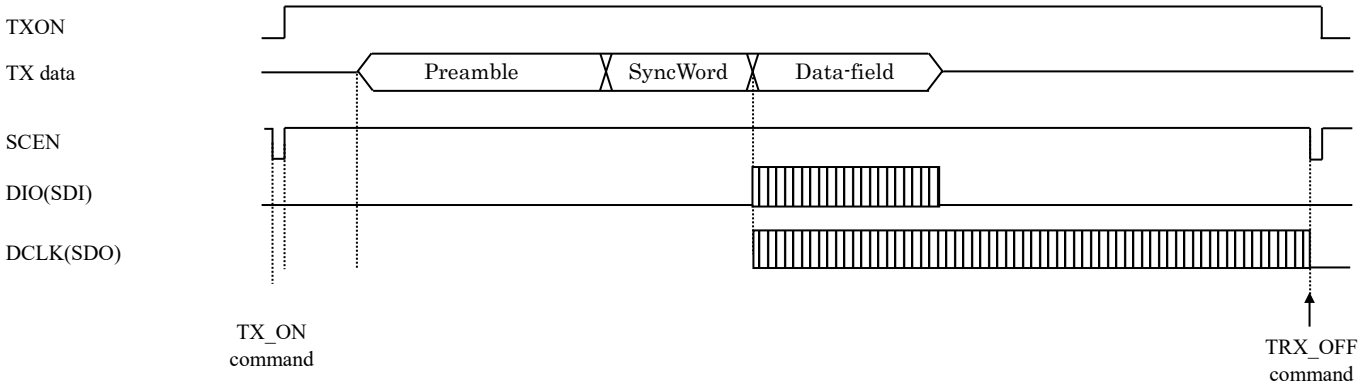
After a TX_ON command is issued ([RF_STATUS: B0 0x0B(3-0)] = 0x9), TX clock is output from the SDO pin while SCEN is H. Input TX data from the SDI pin. After TRX_OFF([RF_STATUS: B0 0x0B(3-0)] = 0x8) command is issued, input/output of TX data/clock will be disabled. In addition, even during DCLK output, if SCEN becomes L, the TX clock output will stop (SPI access has priority).



(b) Data input mode

Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b10.

After a TX_ON command is issued ([RF_STATUS: B0 0x0B(3-0)] = 0x9), TX clock is output from the SDO pin while SCEN is H. Input TX data from the SDI pin. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), TX data/clock input/output are invalid. In addition, even during TX clock output, if SCEN becomes L, the TX clock output will stop (SPI access has priority).



[Note]

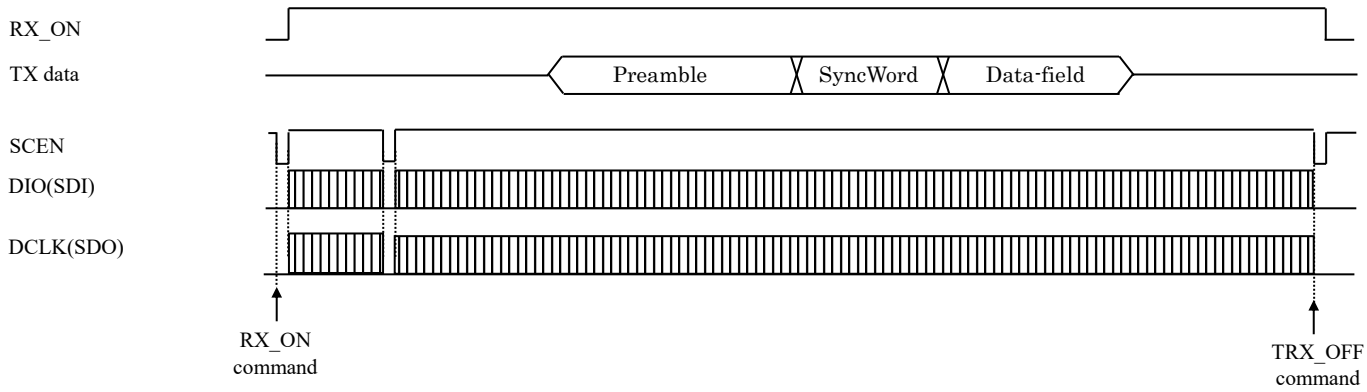
If SPI access is attempted during packet transmission, SPI access has a higher priority while the TX operation is continuing, thus TX data error can be expected. Do not attempt access SPI before TX completion.

[RX]

(a) Continuous output mode

When RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) = 0b01

After RX_ON command is issued (([RF_STATUS: B0 0x0B(3-0)] = 0x6), RX clock is output from the SDO pin and RX data is output from the SDI pin while SCEN is H. After TRX_OFF issuing, DCLK/DIO output will stop. In addition, even during RX data/clock output, if SCEN becomes L, the RX data/clock output will stop (SPI access has priority).



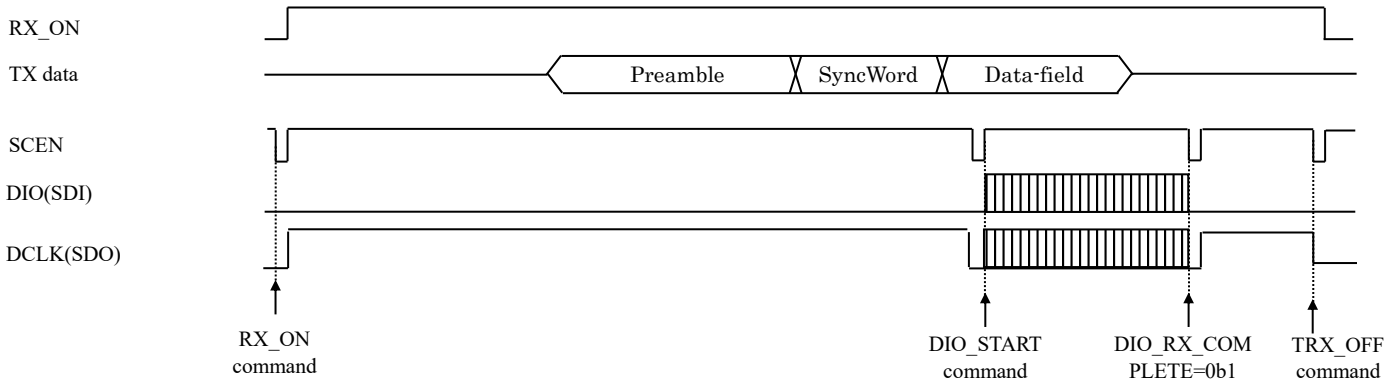
[Note]

During packet reception, if SPI access is attempted by the host, RX data error can be expected. At this time, reception data is not output causing missing bits, so do not conduct SPI access until reception is completed.

(b) Data output mode 1 or data output mode 2

Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b10/11.

After RX_ON command is issued ([RF_STATUS: B0 0x0B(3-0)] = 0x6), RX clock is output from the SDO pin and RX data is output from the SDI pin while SCEN is H. After TRX_OFF issuing, DCLK/DIO output will stop. In addition, even during RX data/clock output, if SCEN becomes L, the RX data/clock output will stop (SPI access has priority).



[Note]

During packet reception, if SPI access is attempted by the host, RX data error can be expected. At this time, reception data is not output causing missing bits, so do not conduct SPI access until reception is completed.

(3) GPIO input/output polarity setting

In DIO mode, input/output polarity of GPIO assigned to data input/output pin automatically switches according to TX/RX operations. GPIO input/output polarity of each state is as follows.

LSI state	GPIO input/output polarity
IDLE state	Output
RX state	Output
Transmitting state	Input
SLEEP state	Output

GPIO input/output polarity can be switched at desired timing by register control (DIO_IODIR_SET_EN([DIO_SET: B0 0x0C(1)]), DIO_IODIR_SET([DIO_SET: B0 0x0C(3)])) rather than being switched automatically. The relation between register setting and input/output polarity for when switching input/output polarity at desired timing is as follows.

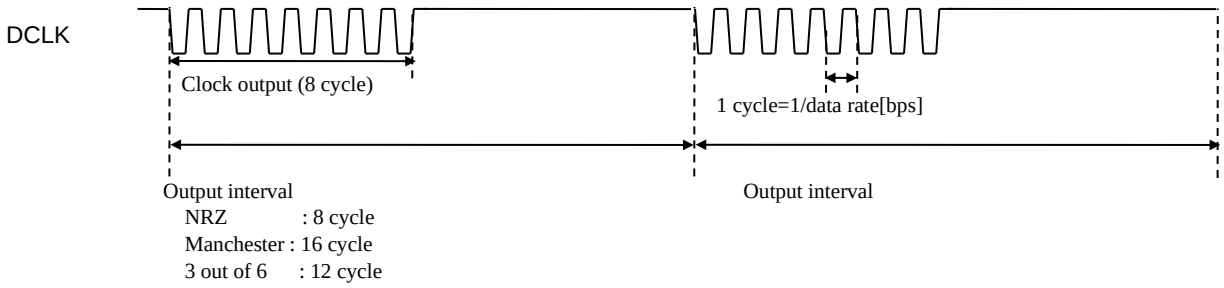
DIO_IODIR_SET_EN ([DIO_SET: B0 0x0C(1)])	DIO_IODIR_SET ([DIO_SET: B0 0x0C(3)])	GPIO input/output polarity
0	-	Automatic control
1	0	Input
1	1	Output

(4) DCLK output method

The DCLK output method depends on the DIO mode setting.

(a) Data output mode 2 (RXDIO_CTRL([DIO_SET: 0x0C(7-6)]) = 0b11)

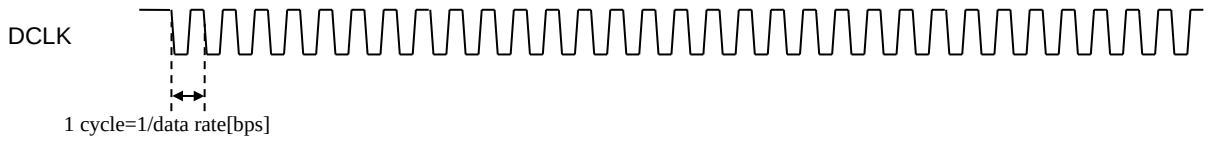
In this mode, decoded data is output. The DCLK output section in an output interval varies depending on the encoding method. DCLK output section is as follows.



(b) Mode other than (a) (RX continuous output mode/data output mode 1, TX continuous input mode/data input mode)

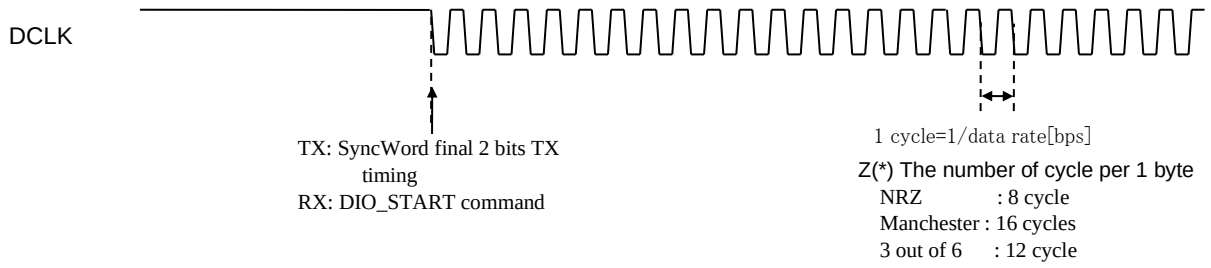
In this mode, undecoded data is input or output. DCLK is output continuously. It does not depend on the encoding method.

TX continuous input mode or RX continuous mode



(*) The number of cycle per 1 byte
NRZ : 8 cycle
Manchester : 16 cycles
3 out of 6 : 12 cycle

TX Data input mode / RX Data output mode 1



6-11-3-8 ○FEC(Forward Error Correction) Function

ML7436N is equipped with FEC and interleaver complying with IEEE802.15.4g.

FEC registers are as follows.

Function	Register
FEC setting	FEC_EN([FEC_CTRL: B6 0x02(0)])
FEC scheme setting	FEC_SCHEME([FEC_CTRL: B6 0x02(1)])
Interleave setting	INTLV_EN([FEC_CTRL: B6 0x02(2)])

[Note]

1. To use the FEC function, use it with the following settings.
   (a) Set TX data encoding mode setting (TX_DEC_SCHEME([DATA_SET1: B0 0x07(1-0)])) and RX data encoding mode setting (RX_DEC_SCHEME([DATA_SET1: B0 0x07(3-2)])) to NRZ.
   (b)Use Format C (PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b10) as the packet format.
   (c) Set the Length field length setting to 2-byte mode (LENGTH_MODE([PKT_CTRL2: B0 0x05(1-0)]) = 0b01).
2. When receiving data undergone Whitening, enable the Whitening setting (WHT_SET([DATA_SET2: B0 0x08(0)]) = 0b1) before receiving.

6-11-4. Timer Function

6-11-4-1 ○Wakeup Timer

ML7436N has automatic wake-up function using wake-up timer. Wake-up timer registers are as follows.

Function	Register
Wake-up enable setting	WAKEUP_EN([SLEEP/WU_SET: B0 0x2D(4)])
Continue operation timer enable setting after Wake-up.	WU_DURATION_EN([SLEEP/WU_SET: B0 0x2D(5)])
After Wake-up operation setting	WAKEUP_MODE([SLEEP/WU_SET: B0 0x2D(6)])
Wake-up timer operation mode setting	WUT_1SHOT_MODE([SLEEP/WU_SET: B0 0x2D(7)])
Wake-up timer clock source setting	WUT_CLK_SORCE([SLEEP/WU_SET: B0 0x2D(3)])
Wake-up timer clock setting	[WUT_CLK_SET: B0 0x2E]
Wake-up timer setting	[WUT_INTERVAL_H/L: B0 0x2F/30]
Continuous operation timer (after wake-up) setting	[WU_DURATION: B0 0x31]
Continued reception condition setting at continuous operation timer completion	RCV_CONT_SEL[1:0]([M_CHECK_CTRL: B0 0x1C(5-4)])
High speed carrier checking mode	FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)])

The following operations are possible by using wake-up timer.

- Upon timer completion, automatically wake-up from SLEEP state. Operation after wake-up can be selected from state changes to RX_ON state and TX_ON state by WAKEUP_MODE([SLEEP/WU_SET: B0 0x2D(6)]).
- By setting WUT_1SHOT_MODE[SLEEP/WU_SET] B0 0x2D(7)]), repetitive wake-up operations (interval operation) or a single operation (one-shot operation) can be selected.
- In interval operation, if RX_ON /TX_ON state is caused by wake-up timer, continuous operation timer is in operation.
- After moving to RX_ON state by the wake-up timer, when the continuous operation timer is completed, move to the SLEEP state automatically. However, if SyncWord is detected before timer completion, RX_ON state will be maintained. In this case, ML7436N does not go back to the SLEEP state automatically. SLEEP setting (SLEEP_EN ([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) is necessary

to go back to the SLEEP state. However, if RXDONE_ MODE[1:0]([RF_STATUS_CTRL:B0 0x0A(3-2)]) =0b11, after RX completion, move to SLEEP state automatically.

The timing to determine whether or not to continue RX after continuous operation timer completion is selectable from SyncWord detection, Field check detection, and synchronization detection by RCV_CONT_SEL([M_CHECK_CTRL: B0 0x1C(5:4)]).

- After moving to the TX_ON state by the wake-up timer, if the state is the IDLE state (TX completion) when the continuous operation timer is completed, it returns to SLEEP automatically. If TX is in progress, the TX_ON state continues. In this case, ML7436N does not go back to the SLEEP state automatically. SLEEP setting (SLEEP_EN ([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) is necessary to go back to the SLEEP state.
- After wake-up by combining with high speed carrier checking mode, CCA is automatically performed, if IDLE is detected, able to move to SLEEP state immediately. For details, please refer to the "(3) high speed carrier detection mode".
- By setting WUT_CLK_SOURCE([SLEEP/WU_SET: B0 0x2D(2]], the clock source for the wake-up timer is selectable from input from GPIO pins GPIO0/GPIO1/GPIO2/GPIO3/GPIO4/GPIO5 (GPIO4 and GPIO5 are available for ML7436 only) and on-chip RC OSC.

Wake-up interval, wake-up timer interval and continuous operation timer can be calculated in the following formula.

Wake-up interval [s] = Wake-up timer interval [s] + Continuous operation timer operating time [s]

Wake-uptimer interval [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) *
(Wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) + 1)

Continuous operation timer [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(7-4)]) *
(Continuous operation timer operating time setting ([WU_DURATION: B0 0x31]) – 1)

[Note]

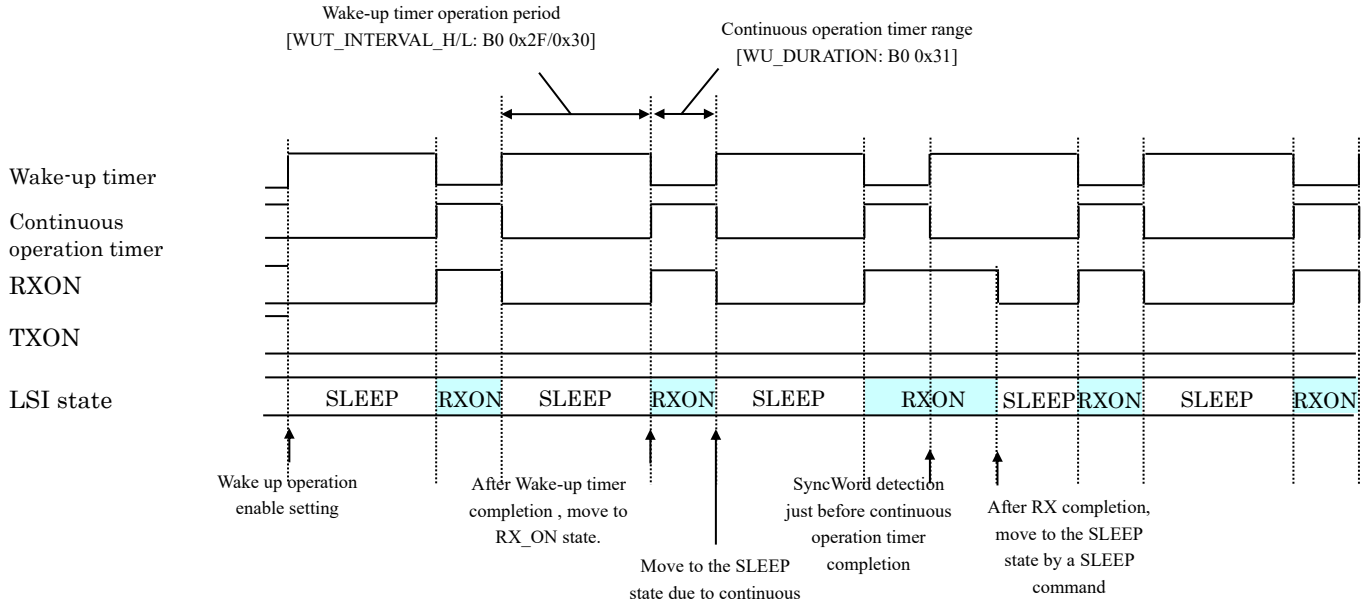
1. When set to move to TX_ON after wake-up, if the continuous operation timer is completed during TX, it is judged as TX in progress and TX continues. After TX is completed, RF state transition is performed according to TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)]) setting.
2. WUDT_CLK_SET ([WUT_CLK_SET: B0 0x2E(7-4)]) and WUT_CLK_SET ([WUT_CLK_SET: B0 0x2E(3-0)]) of dividing setting can be set independently. When using the continuous operation timer, set the same setting to WUDT_CLK_SET and WUT_CLK_SET.
3. The minimum setting for wake-up timer setting interval ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is 0x02. The minimum setting for continuous operation timer operating time setting ([WU_DURATION: B0 0x31]) is 0x01. Note that continuous operation timer operating time setting should be set so that the timer completion is occurred after a notification of a clock stabilization completion interrupt (INT[0]([INT_SOURCE_GRP1: B0 0x0D(0)])) caused by wake-up.
4. Since SyncWord detection is not conducted during reception of DIO mode set to RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) = 0b01, after continuous operation timer is completed, the state moves to the SLEEP state forcibly.

(1) Interval OPeration

(a) RX

After wake-up, RX_ON state. If continuous operation timer completed before SyncWord detection, automatically return to SLEEP state. If SyncWord detected, continue RX_ON. After RX completion, continue operation defined by RXDONE_MODE[1:0] ([RF_STATUS_CTRL: B0 0x0A(3-2)]). In addition, the state can be moved to the SLEEP state by setting SLEEP_EN(SLLEP/WU_SET:B0 0x2D(0)] = 0b1.

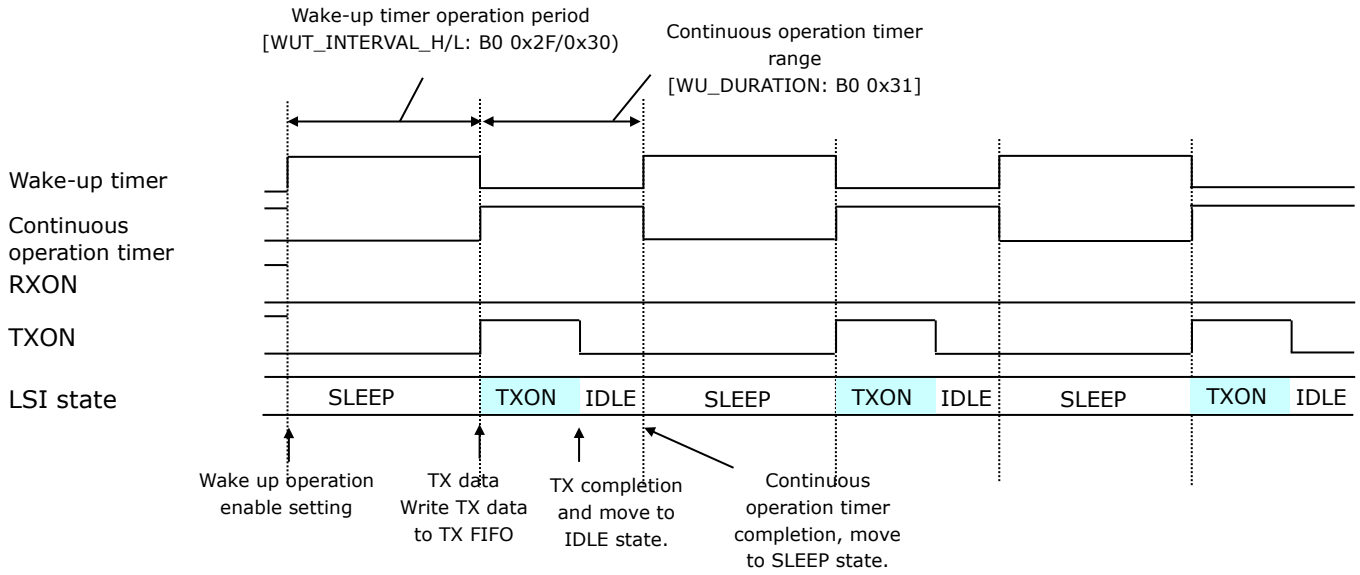
When [SLEEPWU_SET: B0 0x2D(6-4)] = 0b011 is set



(b) TX

After wake-up, TX_ON state. After TX completion, operate according to TXDONE_MODE[1:0] ([RF_STATUS_CTRL: B0 0x0A(1-0)]). If continuous operation timer completed, automatically return to SLEEP state. So continuous operation timer has to be set so that timer completion occurs after TX completion.

When [SLEEPWU_SET: B0 0x2D(6-4)] = 0b111 is set

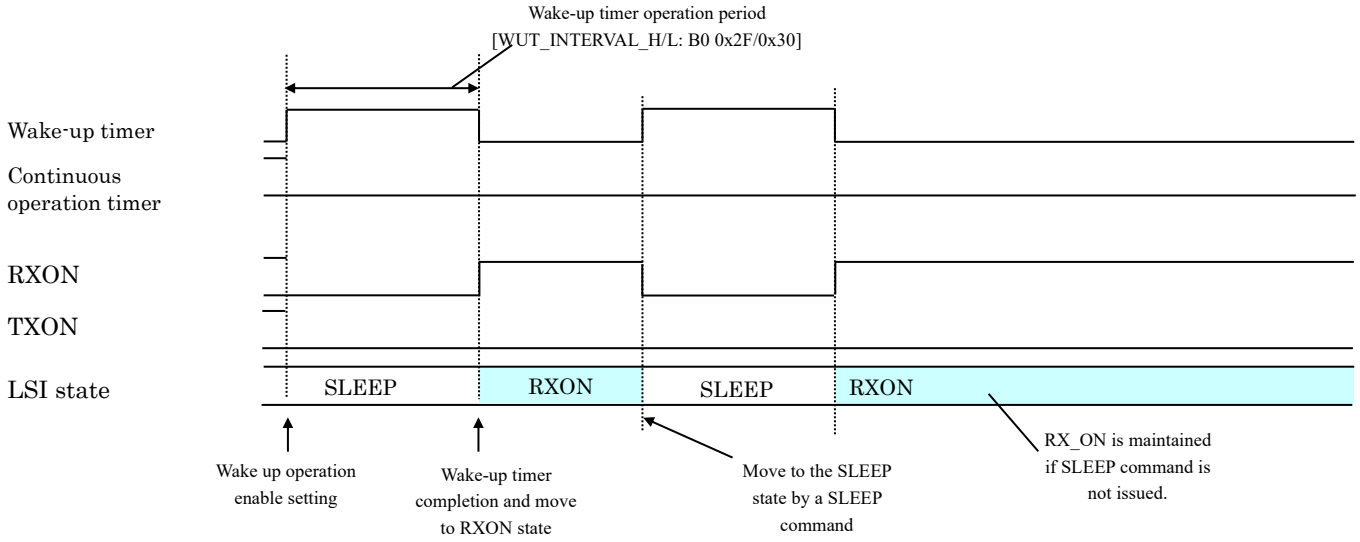


(2) 1 Shot Operation

(a) RX

After wake-up timer completion, move to RX_ON state. And continue RX_ON state. Move to SLEEP state by SLEEP command. Since wake-up timer setting interval ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is maintained, after a SLEEP command is issued, the one-shot operation will restart. Clear the wake-up interrupt ([INT_SOURCE_GRP1: B0 0x0D(6)]) before moving to the SLEEP state. If the wake-up interrupt is not cleared, the state does not move to the RX_ON state automatically. If RX completed during RX_ON, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) . Same manner in TX_ON state.

When [SLEEP/WU_SET: B0 0x2D(7-4)] = 0b1001 is set

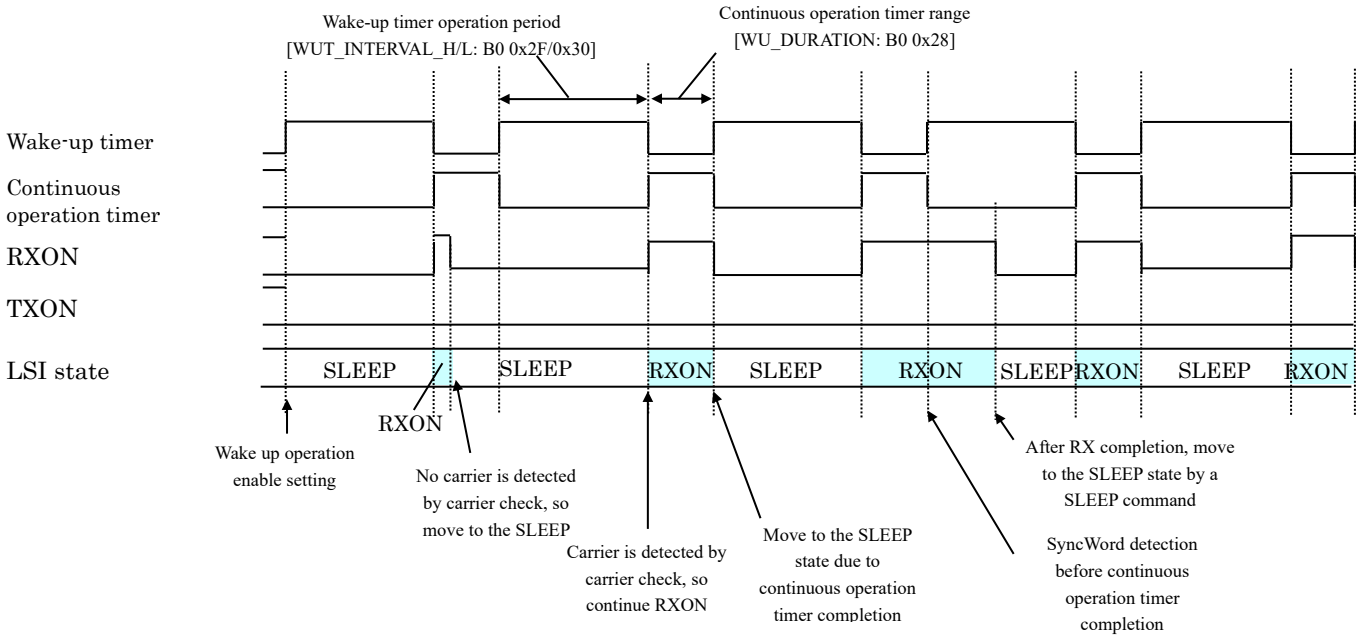


(3) Combination with high speed carrier detection

(a) Interval operation

After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier is detected, automatically move to SLEEP state. If carrier detected, maintaining RX_ON state and perform SuncWord detection. If continuous operation timer completed before SyncWord detection, automatically move to SLEEP state. And If SyncWord detected, continue RX_ON state.

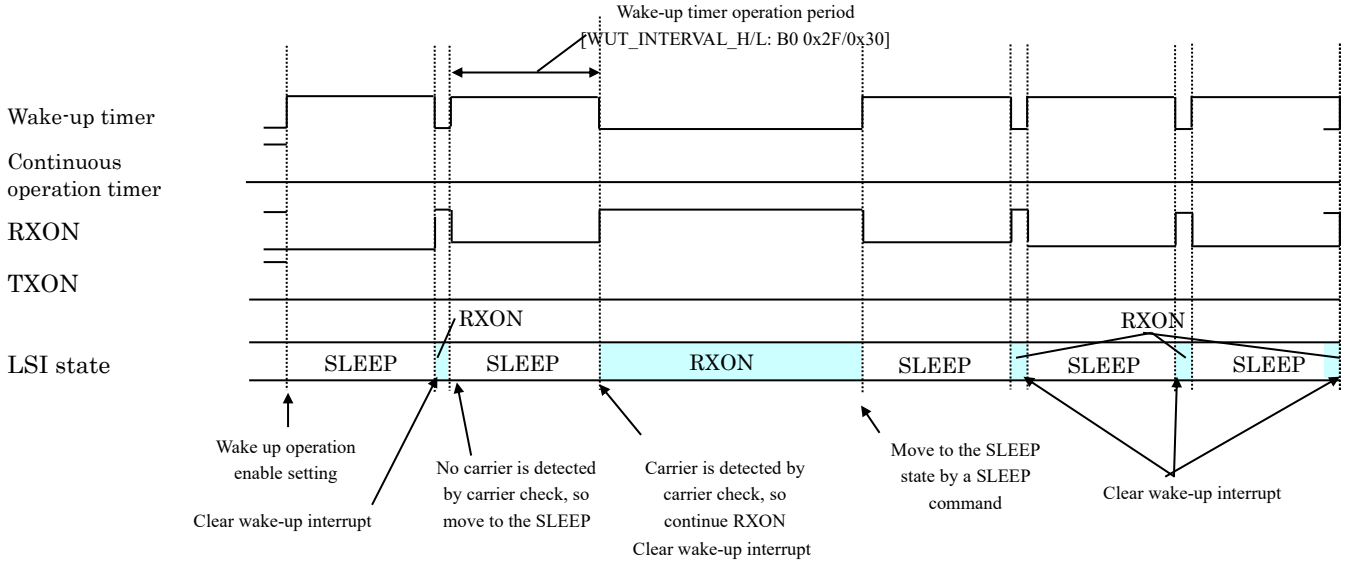
[SLEEP/WU_SET: B0 0x2D(7-4)]=0b0011
When FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)]) = 0b1 is set



(b) One-shot operation

After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier is detected, automatically move to SLEEP state. In case of no carrier detection, if periodic waking up at wake-up timer interval is necessary, clear the wake-up interrupt ([INT_SOURCE_GRP1: B0 0x0D(6)]) before moving to the SLEEP state. If the wake-up interrupt is not cleared, the state does not move to the RX_ON state automatically. If carrier is detected, continue RX state. Able to go back to SLEEP by setting SLEEP parameters.

[SLEEPWU_SET: B0 0x2D(7-4)]=0b1001
When FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)]) = 0b1 is set



6-11-4-2 ○General Purpose Timer

ML7436N has general purpose timer. 2 channels of timer are able to function independently. Clock sources, timer setting can be programmed independently. This timer is one-shot operation. When the timer is completed, notify by interrupt (INT[22] or INT[23]: [INT_SOUCE_GRP3:B0 0x0F]). To activate the timer again, be sure to clear the timer completion interrupt (INT[22] or INT[23]) before starting the timer.

Wake-up timer registers are as follows.

Function	Register
General purpose timer 1 execution	GT1_START([GT_SET: B0 0x32(0)])
General purpose timer #1 clock sources setting	GT1_CLK_SOURCE([GT_SET: B0 0x32(1)])
General purpose timer #1 period setting	[GT1_TIMER: B0 0x34]
General purpose timer 2 execution	GT2_START([GT_SET: B0 0x32(4)])
General purpose timer #2 clock sources setting	GT2_CLK_SOURCE([GT_SET: B0 0x32(5)])
General purpose timer #2 period setting	[GT2_TIMER: B0 0x35]
General purpose timer clock division setting	[GT_CLK_SET: B0 0x33]

General timer interval can be programmed as the following formula.

General purpose timer interval [sec] = general purpose timer clock cycle *
Division setting ([GT_CLK_SET: B0 0x33]) *
General purpose timer interval setting ([GT1_TIMER: B0 0x34] or [GT2_TIMER: B0 0x35])

By setting GT2/1_CLK_SOURCE [GT_SET: B0 0x32(5,1)], the clock source for general purpose timer is selectable from wake-up timer clock and 2 MHz. 2 MHz clock is generated by FREF and MSTR_CLK_SEL1, 2([CLK_SET1: B0 0x02(6,5)]). For details, refer to GT2/1_CLK_SOURCE [GT_SET: B0 0x32(5,1)].

[Note]

1. When GT1_START or GT2_START is set to 0b0 during general purpose timer operation, the timer stops at that time. After that, when GT1_START or GT2_START is set to 0b1 again, the timer restarts from the timer value at the time of the stop. The timer cannot restart from timer value 0 after stopped before completion.

6-11-5. Frequency Setting Function

Frequencies can be set by the following registers, divider ratio.

Frequency setting

Frequency			Register
PLL output divider ratio setting(Ndiv)			[PLL_DIV_SET: B1 0x1A(3-1)] : RF output divider ratio setting(Ndiv)
CH#0 frequency setting (Npll)	Sub-GHz	PLL dividing value (TX)	[TXFREQ_I: B1 0x1B] : Integer part of divider ratio value [TXFREQ_FH: B1 0x1C] : Fractional part of divider ratio value (high byte) [TXFREQ_FM: B1 0x1D] : Fractional part of divider ratio value (middle byte) [TXFREQ_FL: B1 0x1E] : Fractional part of divider ratio value (low byte)
		PLL dividing value (RX)	[RXFREQ_I: B1 0x1F] : Integer part of divider ratio value [RXFREQ_FH: B1 0x20] : Fractional part of divider ratio value (high byte) [RXFREQ_FM: B1 0x21] : Fractional part of divider ratio value (middle byte) [RXFREQ_FL: B1 0x22] : Fractional part of divider ratio value (low byte)
	2.4 GHz	PLL divider ratio value (TX)	[TXFREQ_I_2G: B4 0x60] : Integer part of divider ratio value [TXFREQ_FH_2G: B4 0x61] : Fractional part of divider ratio value (high byte) [TXFREQ_FM_2G: B4 0x62] : Fractional part of divider ratio value (middle byte) [TXFREQ_FL_2G: B4 0x63] : Fractional part of divider ratio value (low byte)
		PLL divider ratio value (RX)	[RXFREQ_I_2G: B4 0x64] : Integer part of divider ratio value [RXFREQ_FH_2G: B4 0x65] : Fractional part of divider ratio value (high byte) [RXFREQ_FM_2G: B4 0x66] : Fractional part of divider ratio value (middle byte) [RXFREQ_FL_2G: B4 0x67] : Fractional part of divider ratio value (low byte)
Channel interval (N_sp)	Sub-GHz		[CH_SPACE_H: B1 0x23] : Channel interval setting value (high byte) [CH_SPACE_L: B1 0x24] : Channel interval setting value (low byte)
	2.4 GHz		[CH_SPACE_H_2G: B4 0x68] : Channel interval setting value (high byte) [CH_SPACE_L_2G: B4 0x69] : Channel interval setting value (low byte)
Channel number (Nch)			[CH_SET: B0 0x09] : Channel number

Setting procedure of the above indicated registers is described below:

6-11-5-1 ○PLL output divider ratio setting

Depending on the RF frequency band, set each register as follows:

PLL output divider ratio and front divider ratio setting

RF frequency band [MHz]	RF output divider ratio (Ndiv)	[PLL_DIV_SET: B1 0x1A] (HEX)	
		PLL front divider ratio : 2	PLL front divider ratio : 4
420-470MHz	4	0x04	0x05
779-787MHz	2	0x02	0x03
843-847MHz	2	0x02	0x03
863-870MHz	2	0x02	0x03
902-930MHz	2	0x02	0x03
2402-2483.5MHz	1	0x00	0x01

[Note] PLL front divider ratio (S) can be selected by [PLL_DIV_SET: B1:0x1A(0)]. (B1:0x1A(0) = 0:divided by2, 1:divided by 4)

6-11-5-2 ○Channel Frequency Setting

Maximum 256 channel frequencies can be set (CH#0 to CH#255).

The setting of TX/RX frequencies can be performed by the following registers.

[Channel frequency setting]

Channel frequency is determined by the following formula.

$Frf\_0 = S * Npll / Ndiv * F_{ref}$ ...(1)

Frf_0: CH#0 frequency

Npll: PLL divider ratio

Ndiv: PLL output divider ratio

F_{ref}: Reference frequency

S: PLL front divider ratio(B1:0x1A(0) = 0:S=2, 1:S=4)

$Npll = Frf\_0 * Ndiv/(S* F_{ref})$ ...(2)

*** For setting of CH#0 frequency, Npll should be set to the following register.**

For Sub GHz band : [TXFREQ_I /FH/FM/FL: B1 0x1B～0x1E]
[RXFREQ_I /FH/FM/FL: B1 0x1F～0x22]

For 2.4GHz band : [TXFREQ_I /FH/FM/FL_2G: B4 0x60～0x63]
[RXFREQ_I /FH/FM/FL_2G: B4 0x64～0x67]

$Frf\_x = Frf\_0 + F\_sp * Nch$ ...(3)

Frf_x: Channel frequency

F_sp: Channel interval

Nch: Channel number

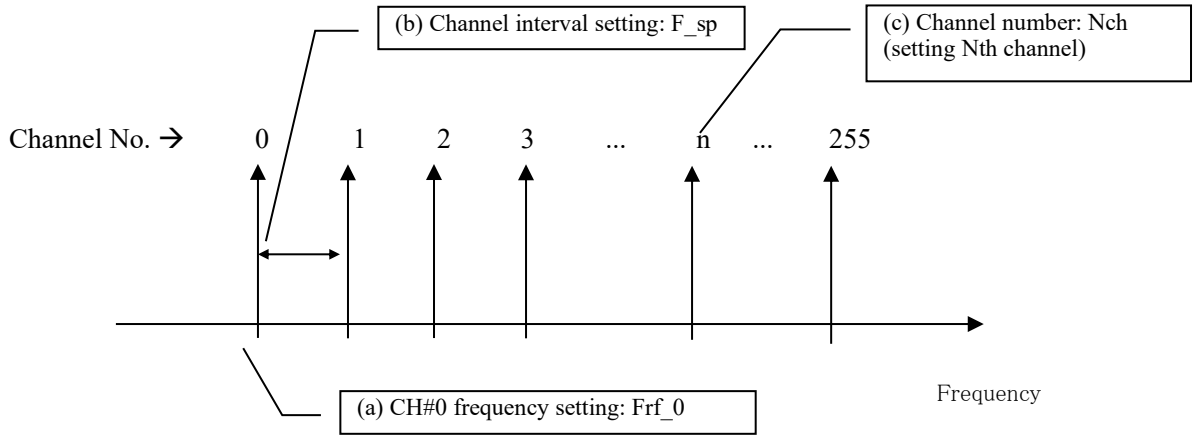
$N\_sp = F\_sp * Ndiv/(S* F_{ref})$ ...(4)

*** For setting the channel interval (F_sp), N_sp should be set to the following register.**

For Sub GHz band : [CH_SPACE_H /L: B1 0x23～0x24]

For 2.4GHz band : [CH_SPACE_H_2G : B4 0x68～0x69]

[Channel frequency allocation image]



(1) CH#0 frequency setting **(Frf_0)**

The setting procedure of CH#0 frequency is described below.
TX and RX frequencies are specified in a separate address.

For CH#0 frequency (**Frf_0**), PLL divider ratio **Npll** should be calculated by the formula (2)

Npll = Frf_0 * Ndiv/(S* F_{ref}) …(2)
Integer part**I = INT(Npll) …(5)** ***INT(X) : Integer part of X**
Fractional part **F =INT[{ Npll - INT(Npll) }*2^{20}] …(6)**

Example] When setting CH#0 frequency **Frf_0**=920.7 MHz (reference clock is **F_{ref}**=48 MHz)

Npll = Frf_0 * Ndiv/(S* F_{ref}) = 920.7 MHz * 2/(2*48 MHz) = 19.18125
(*Ndiv=2,S=2)

Integer part **I = 19[DEC]=13[HEX]**
Fractional part **F =INT((Npll - INT(Npll))*2^{20})**
=INT((19.18125 - 19) *2^{20})=190054[DEC] = 02_E6_66[HEX]

CH#0 frequency setting at Frf_0=920.7 MHz (**F_{ref}**=48 MHz)

PLL divider ratio Npll	TX register address	RX register address	Setting value [HEX]
Integer part I	[TXFREQ_I: B1 0x1B]	[RXFREQ_I: B1 0x1F]	13
Fractional part F_H (high)	[TXFREQ_FH: B1 0x1C]	[RXFREQ_FH: B1 0x20]	02
Fractional part F_M (middle)	[TXFREQ_FM: B1 0x1D]	[RXFREQ_FM: B1 0x21]	E6
Fractional part F_L (low)	[TXFREQ_FL: B: 0x1E]	[RXFREQ_FL: B1 0x22]	66

* Setting example for 2.4 GHz

CH#0 frequency setting at Frf_0=2405MHz (**F_{ref}**=48 MHz)

PLL divider ratio Npll	TX register		RX register	
	Address	Setting value [HEX]	Address	Setting value [HEX]
Integer part I	[TXFREQ_I_2G: B4 0x60]	19	[RXFREQ_I_2G: B4 0x64]	19
Fractional part F_H (high)	[TXFREQ_FH_2G: B4 0x61]	00	[RXFREQ_FH_2G: B4 0x65]	00
Fractional part F_M (middle)	[TXFREQ_FM_2G: B4 0x62]	D5	[RXFREQ_FM_2G: B4 0x66]	D5
Fractional part F_L (low)	[TXFREQ_FL_2G: B4 0x63]	55	[RXFREQ_FL_2G: B4 0x67]	55

(2) Channel interval setting **(F_sp)**

The setting procedure of channel interval is described below.

Channel interval **F_sp** is the center frequency interval of the adjacent channels.

To obtain channel interval **F_sp**, PLL divider ratio **N_sp** should be calculated by the formula (4). Only the fractional part F of the result should be set to the register.

$N\_sp = F\_sp * Ndiv/(S* F_{ref}) \quad ...(4)$

Fractional part **$F = INT((N\_sp)*2^{20}) \quad ...(7)$**

The maximum channel interval **F_sp_max** to be set is calculated by the following formula.

$F\_sp\_max < F_{ref}/2^4 \quad ...(8)$

[Example] When setting channel interval **F_sp** =400 kHz (reference clock is **F_{ref}**=48 MHz)

$N\_sp = F\_sp * Ndiv/(S* F_{ref}) = 400\ kHz * 2/(2*48\ MHz) = 0.008333$
(*Ndiv=2,S=2)

Fractional part **$F = INT((N\_sp)*2^{20}) = INT(0.008333 *2^{20})$**
$= 8738[DEC] = 00\_22\_22[HEX]$

Channel interval **(N_sp)** setting table at **F_sp**=400 kHz(**F_{ref}**=48 MHz)

PLL divider ratio N_sp	Register address	Setting value [HEX]
Integer part I	-	-
Fractional part F_H (high)	-	-
Fractional part F_M (middle)	[CH_SPACE_H: B1 0x23]	22
Fractional part F_L (low)	[CH_SPACE_L: B1 0x24]	22

* The maximum channel interval F_sp [MHz] < **F_{ref}/(2^4) [MHz](=3 MHz)**

* Setting example for 2.4 GHz

Channel interval **(N_sp)** setting table at **F_sp**=1000 kHz(**F_{ref}**=48 MHz)

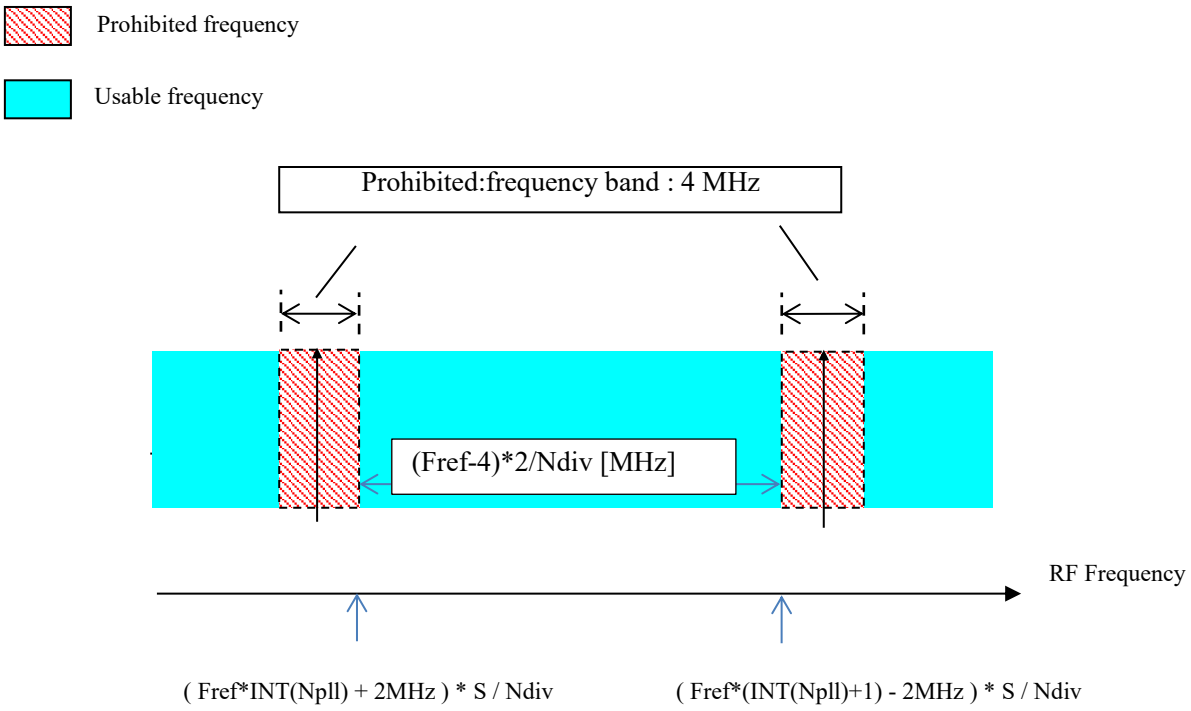
PLL divider ratio N_sp	Register address	Setting value [HEX]
Integer part I	-	-
Fractional part F_H (high)	-	-
Fractional part F_M (middle)	[CH_SPACE_H_2G: B1 0x68]	2A
Fractional part F_L (low)	[CH_SPACE_L_2G: B1 0x69]	AA

* The maximum channel interval F_sp [MHz] < **F_{ref}/(2^4) [MHz](=3 MHz)**

[Note]

(1) The RF frequency to be selected must meet the following conditions. If the following conditions cannot be met, change the reference clock frequency or channel #0 frequency.

(Fref*INT(Npll) + 2MHz) * S / Ndiv ≤ RF frequency to be selected
≤ (Fref*(INT(Npll)+1) - 2MHz) * S / Ndiv



(2) CH#0 frequency and channel interval settings may have error. Therefore, channel frequency has frequency error indicated by the following formula.

Channel frequency error [Hz]
= CH#0 frequency error [Hz] + Channel interval setting error [Hz] * Channel setting

When changing "channel frequency" by setting "channel setting" without "CH#0 frequency" change, the "channel frequency error" will become larger than by setting both "CH#0 frequency" and "channel setting". If the "channel frequency error" becomes larger, change "CH#0 frequency".

(3) If the 26-bit channel frequency (=CH#0 frequency + Channel interval x Channel setting) setting

value (integer and decimal parts, refer to "Channel #0 frequency setting") exceeds the maximum value 0x1FF_FFFF, the expected channel frequency is not achieved. Take this maximum value into account when deciding the channel #0 frequency, channel interval, and channel setting.

(4)The reference clock frequency (Fref) and the typical RF frequency is as following.

✓:Executable setting -:Unexecutable setting

PLL reference clock Fref[MHz]	30		32		36		38		38.88		39		40		40.96		41.6		48		52	
PLL prefixed divided ratio S	2	4	2	4	2	4	2	4	2	4	2	4	2	4	2	4	2	4	2	4	2	4
ETSI 863-870MHz	-	✓	-	✓	-	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-	-	✓	✓
ETSI 868-870MHz	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
STD-30 426MHz	✓	✓	✓	✓	✓	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
T67 426MHz	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
T67 429MHz	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	-	-	✓	✓	-	✓	✓	✓	✓	✓	✓	✓
T67 469MHz	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
T108 915-917MHz	✓	✓	✓	✓	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	-	-	✓	✓	✓	✓
T108 920-928MHz	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
T108 920-930MHz	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
T66 2402-2483.5MHz	-	-	-	-	-	-	-	-	-	✓	-	✓	-	-	-	-	-	✓	-	✓	✓	✓
FCC 902-928MHz	✓	-	-	✓	✓	✓	-	-	✓	✓	✓	✓	✓	✓	-	-	-	-	-	✓	✓	✓
FCC 2402-2478MHz	-	-	-	-	-	-	-	-	-	✓	-	✓	-	-	-	-	-	✓	-	✓	✓	✓

※The data rate and the reference clock frequency need to satisfy the following relationship. The reference clock frequency Freq is integer multiple of the reference clock.

(5) If PLL unlock occurs, PLL unlock detection interrupt (INT2[INT_SOURCE_GRP1: B0 0x0D(2)]) will be generated. The following tables show the relationship between the PLL lock detection setting (PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)]) and the LSI operation after the interrupt.

- When PLL unlock occurs

LSI state	PLL unlock detection period	PLL lock detection setting and LSI operation after interrupt generation	
		PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)] = 0b1	PLL_LD_EN[PLL_LOCK_DETECT:B1 0x0B(7)] = 0b0
TX	PA_ON =”H” period	Interrupt occurs, and TX is stopped forcibly	Interrupt occurs, and TX is continued
RX	RX enable =”H” period	Interrupt occurs, and RX is continued	Interrupt occurs, and RX is continued

6-11-5-3 ○IF Frequency Setting

IF frequency is set by [IF_FREQ: B0 0x61]. The following table shows the relationship between IF frequency setting value and IF frequency. These can be set separately for the normal receiving mode and during CCA.

Then Frequency can be set to half of the setting value by IF_RES_SEL_DIF([DIF_SET3: B3 0x31(4)]) and IF_RES_SEL_FMAP([DIF_SET3: B3 0x31(5)]).

IF_FREQ([IF_FREQ: B0 0x61(2-0)]) IF_FREQ_CCA([IF_FREQ: B0 0x61(6-4)])	IF Frequency(*1)		
	[DIF_SET3: B3 0x31]=0x00 (Digital signal processing circuit operation mode:Normal mode, IF frequency=Setting value x 1)	[DIF_SET3: B3 0x31]=0x25 (Digital signal processing circuit operation mode:Low-power consumption mode, IF frequency=Setting value x 1/2)	[DIF_SET3: B3 0x31]=0x35 (Digital signal processing circuit operation mode:Low-power consumption mode, IF frequency=Setting value x 1)
0x0	500kHz	250kHz	Prohibited
0x1	375kHz	187.5kHz	375kHz
0x2	300kHz	150kHz	300kHz
0x3	Prohibited	Prohibited	Prohibited
0x4	175kHz	87.5kHz	175kHz
0x5	200kHz	100kHz	200kHz
0x6	225kHz	112.5kHz	225kHz
0x7	250kHz	125kHz	250kHz
0x8	275kHz	137.5kHz	275kHz
0x9	325kHz	162.5kHz	325kHz
0xA	350kHz	175kHz	350kHz
0xB	400kHz	200kHz	Prohibited
0xC	425kHz	212.5kHz	Prohibited
0xD	450kHz	225kHz	Prohibited
0xE	475kHz	237.5kHz	Prohibited
0xF	525kHz	262.5kHz	Prohibited

(*1) This frequencies are used when FREF is 48 MHz. When FREF is 52 MHz, the above frequencies should be multiplied by 52/48.

[Note]

(1) RX local frequency is set to Lower local setting by default. To change the RX local frequency setting, refer to "Other setting - RX local Upper/Lower setting".

(2) If DIF_FREQ_SEL([DIF_SET3: B3 0x31(2)]) is set to 0b1 for low power mode, DIF_LP_MODE([DIF_SET3: B3 0x31(0)]) need to be set to 0b1. Also DIF_FREQ_SEL([DIF_SET3: B3 0x31(2)]) is set to 0b1, IF frequency can be set to half of the frequency that is set by [IF_FREQ: B0 0x61]. In that case, IF_RES_SEL_FMAP([DIF_SET3: B3 0x31(5)]) and IF_RES_SEL_DIF([DIF_SET3: B3 0x31(4)]) are used.

{ IF_RES_SEL_FMAP([DIF_SET3: B3 0x31(5)]) , IF_RES_SEL_DIF([DIF_SET3: B3 0x31(4)]) }	IF Frequency
0b11	is set by [IF_FREQ: B0 0x61]
0b10	is set by [IF_FREQ: B0 0x61] and halved
other setting	Prohibited

If DIF_FREQ_SEL([DIF_SET3: B3 0x31(2)]) is set to 0b0, IF_RES_SEL_FMAP([DIF_SET3: B3 0x31(5)]) and IF_RES_SEL_DIF([DIF_SET3: B3 0x31(4)]) need to be set to 0b0.

(3) Changing the IF frequency setting may cause a deterioration of receiving sensitivity. When changing the IF Frequency setting, the register value should be decided after enough evaluation.

6-11-6. RX Related Function

6-11-6-1 ○AFC Function

ML7436N supports AFC function. Frequency deviation (max ±20 ppm) between local signals within remote device and ML7436N can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved.
This function can be enabled by setting AFC_EN([AFC/GC_CTRL: B1 0x15(7)])=0b1.

6-11-6-2 ○Energy Detection Value (ED value) Acquisition Function

ML7436N supports the function to indicate the received signal strength indicator (RSSI) as the energy detection value (ED value).
ED value acquisition can be enabled by setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)])=0b1. As soon as a transition is made to RX_ON state, acquisition of ED value starts automatically.
While in RX_ON state, the ED value is constantly updated.
ED value is not RSSI value at given timing, but average values. The number of average processing can be specified by ED_AVG([ED_CTRL: B0 0x41(2-0)]). During diversity operation, this can be set by DIV_ED_AVG ([2DIV_MODE: B1 0x48(2-0)]). As soon as ED value is acquired for the number of average processing, ED_DONE([ED_CTRL: B0 0x41(4)]) is set to "1" and ED_VALUE([ED_RSLT: B0 0x3A]) will be updated.

ED_DONE bit will be cleared if one of the following conditions is met.

① Antenna is switched.
② Gain is switched.
③ Once stopping ED value acquisition and then resume it.

Timing from ED value starting point to ED value acquisition is calculated as below formula.
ED value average processing time = Average interval (16 μs(*1)) * ED value average times

(*1) The average interval can be calculated by the formulas indicated below based on the setting values of MSTR_CLK_SEL1([CLK_SET1: B0 0x02(5)]) and MSTR_CLK_SEL2([CLK_SET1: B0 0x02(6)]).
MSTR_CLK_SEL1=0b0, MSTR_CLK_SEL2=0b0 …$(1/F_{REF})*24*32$
MSTR_CLK_SEL1=0b0, MSTR_CLK_SEL2=0b1 …$(1/F_{REF})*26*32$

MSTR_CLK_SEL1=0b1, MSTR_CLK_SEL2=0b0 …$(1/F_{REF})*12*32$
MSTR_CLK_SEL1=0b1, MSTR_CLK_SEL2=0b1 …$(1/F_{REF})*13*32$

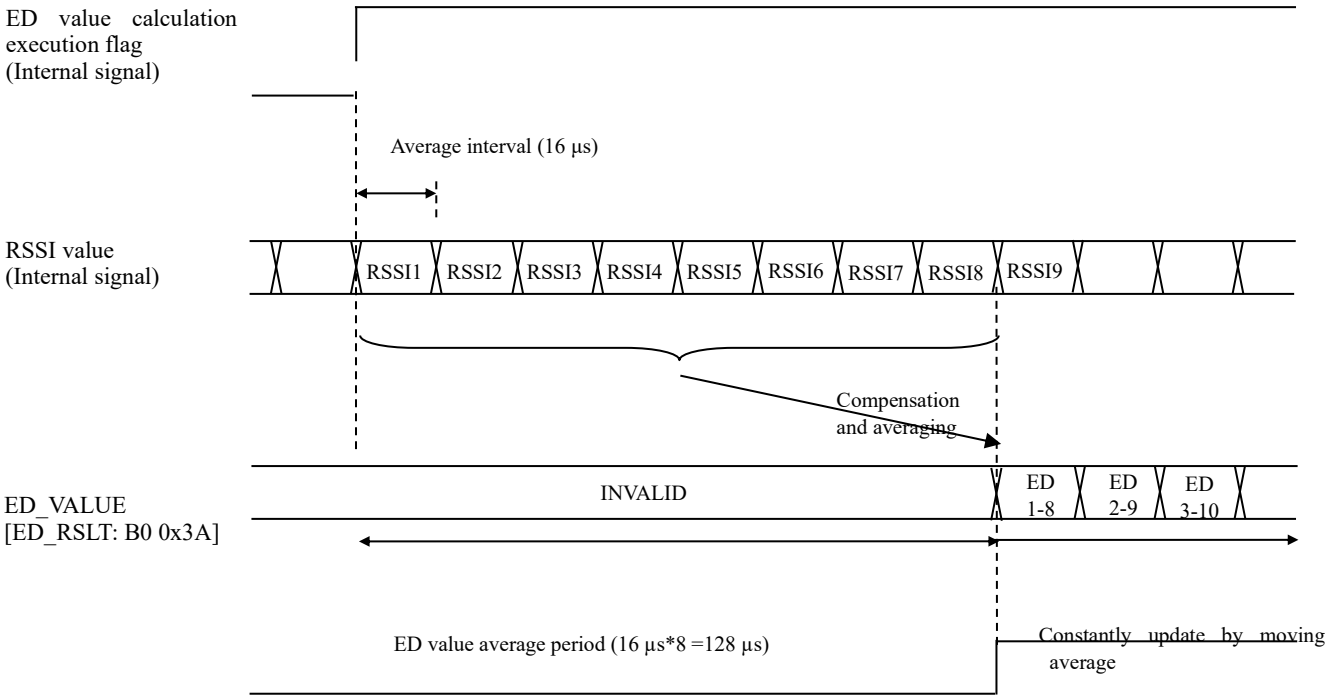
The relationship of ED value and the reception level is represented as the following formula.

Reception level [dBm] = (ED value – X) / Y

Data Rate	X	Y
4.8	452.36	3.9662
9.6	452.36	3.9662
50	433.2	3.969
100	425.98	3.9853
150	425.98	3.9853
200	425.98	3.9853
300	425.98	3.9853

The timing chart of ED value measurement is represented as following.

[Condition]
ED_AVG[2:0]=0b011 (ED value 8 times average) [ED_CTRL: B0 0x41(2-0)]



ED_DONE
([ED_CTRL:B0 0x41(4)])

6-11-6-3 ○Programmable Channel Filter Bandwidth Function

Channel filter bandwidth can be set by CHFIL_BW_ADJ[7:0]([CHFIL_BW: B0 0x54(7-0)]), CHFIL_BW_ADJ[9:8]([CHFIL_BW_OPTION: B0 0x6B(5-4)]), and CHFIL_CO_SEL([CHFIL_BW_OPTION: B0 0x6B(0)]), or CHFIL_CO_SEL_CCA([CHFIL_BW_OPTION: B0 0x6B(1)]). The relationship between the setting value and the channel filter bandwidth is expressed by the following formula.

When CHFIL_CO_SEL/CHFIL_CO_SEL_CCA=0b0,

Channel filter bandwidth [Hz] = {F_{REF}[Hz] / setting value / 43.33}

When CHFIL_CO_SEL/CHFIL_CO_SEL_CCA =0b1,

Channel filter bandwidth [Hz] = {F_{REF}[Hz] / setting value / 40}

See the following table for the channel filter bandwidth for each setting value. Channel filter bandwidth can be set separately for the normal receiving mode and during CCA. As the channel filter bandwidth during CCA, the setting values of CHFIL_BW_ADJ_CCA[7:0]([CHFIL_BW_CCA: B0 0x6A(7-0)]) and CHFIL_BW_ADJ_CCA[9:8]([CHFIL_BW_OPTION: B0 0x6B(7-6)]) are applied. The channel filter bandwidth needs to be optimized according to the data rate and the maximum frequency deviation.

(1) F_{REF}=48MHz、CHFIL_CO_SEL=0b1

CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]	CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]
0	Prohibited	16	75.0
1	1200.0	17	70.6
2	600.0	18	66.7
3	400.0	19	63.2
4	300.0	20	60.0
5	240.0	21	57.1
6	200.0	22	54.5
7	171.4	23	52.2
8	150.0	24	50.0
9	133.3	25	48.0
10	120.0	26	46.2
11	109.1	・・・	・・・

12	100.0	120	10.0
13	92.3	・・・	・・・
14	85.7	1022	1.74
15	80.0	1023	1.73

(2) FREF=48MHz、CHFIL_CO_SEL=0b0

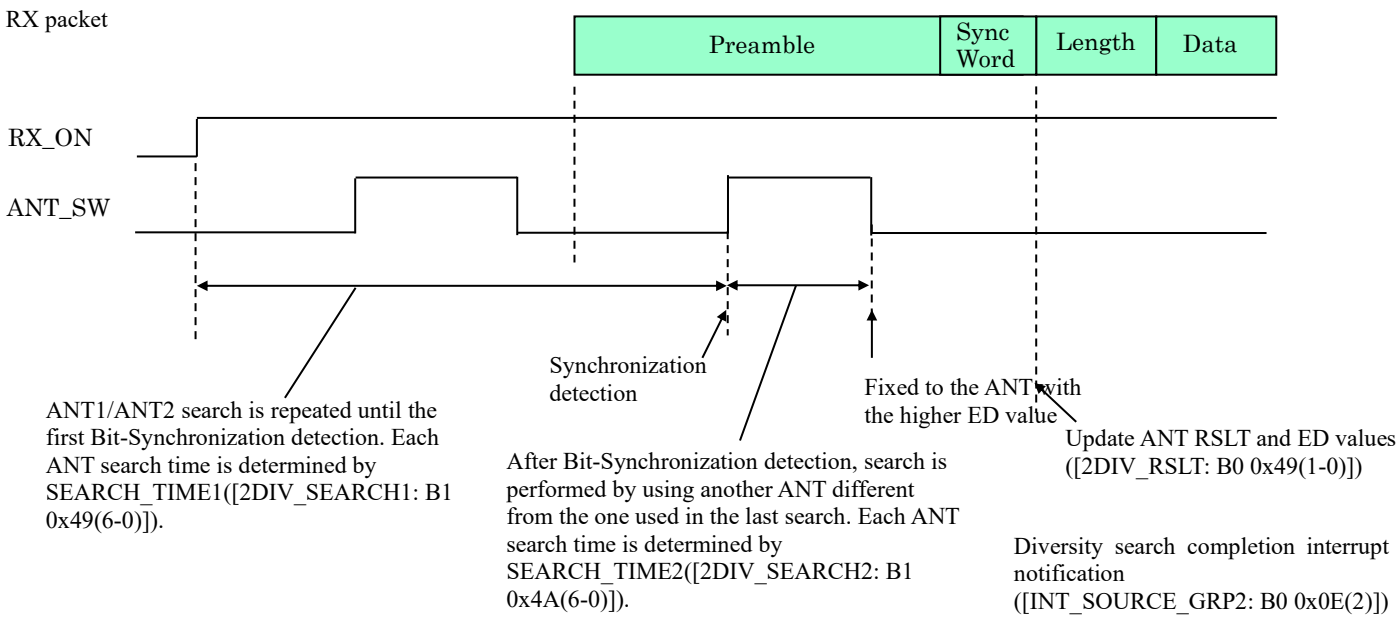
CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]	CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]
0	設定禁止	16	69.2
1	1107.8	17	65.2
2	553.9	18	61.5
3	369.3	19	58.3
4	276.9	20	55.4
5	221.6	21	52.8
6	184.6	22	50.4
7	158.3	23	48.2
8	138.5	24	46.2
9	123.1	25	44.3
10	110.8	26	42.6
11	100.7	・・・	・・・
12	92.3	120	9.23
13	85.2	・・・	・・・
14	79.1	1022	1.084
15	73.9	1023	1.083

6-11-6-4 ○Diversity Function

ML7436N supports two-antenna diversity function.

While in 2DIV_EN([2DIV_CTRL: B0 0x48(0)])=0b1 setting, as soon as RX_ON is set, the diversity mode will start. When diversity mode is started, and upon RX data detection, each ED value will be acquired by switching two antennas. And then antenna with higher ED value will be selected automatically. As diversity uses preamble data for ED value acquisition, longer preamble length is desirable. If preamble is too short, accurate ED values may not be obtained.

The timing diagrams are shown below.



ED value obtained by Diversity ([ANT1_ED: B0 0x4A]) or [ANT2_ED: B0 0x4B]) and Diversity antenna result ([2DIV_RSLT: B0 0x49(1-0)]) are updated and overwritten when SyncWord is detected.
The number of detection performed during the ED value calculation is specified by 2DIV_ED_AVG([2DIV_MODE: B1 0x48(2:0)]). Time resolution of search times ([SEARCH_TIME1] and [SEARCH_TIME2]) can be specified by SEARCH_TIME_SET([2DIV_SEARCH1: B1 0x49(7)]).

When Diversity search completion interrupt INT[10]([INT_SOURCE_GRP2: B0 0x0E(2)]) is cleared, the ED value obtained by Diversity ([ANT1_ED: B0 0x4A]) or [ANT2_ED: B0 0x4B]) and Diversity antenna result ([2DIV_RSLT: B0 0x49(1-0)]) are cleared to zero.

[Note]
In this function, when a diversity completion was determined to be false due to erroneous detection, antenna search is automatically executed again. However, when a desired signal was received since diversity search was completed due to erroneous detection until the time a false detection was determined, the obtained ED value ([ANT1_ED: B0 0x4A]) or [ANT2_ED: B0 0x4B]) shows a lower ED value which is different from the input level of desired wave. The occurrence of this event can be checked by reading out the ED value, which is displayed by [ED_RSLT: B0 0x3A], after the occurrence of SyncWord detection interrupt of desired wave INT[13]([INT_SOURCE_GRP2: B0 0x0E(5)]).

(1) Antenna Switching Function

By using [2DIV_CTRL: B0 0x48], [ANT_CTRL: B0 0x4C], and [SPI/EXT_PA_CTRL: B0 0x53] registers, TX-RX signal selection (TRX_SW), antenna switching signal (ANT_SW), and external PA control signal (DCNT) can be controlled.

Two types of antenna switches (SPDT switch/DPDT switch) can be controlled by [2DIV_CTRL: B0 0x48(3-1)] and [ANT_CTRL: B0 0x4C]). The relationship between the output status of ANT_SW and TRX_SW pins during each antenna switch control and [2DIV_CTRL: B0 0x48(2-1)] is indicated below.

(a) When DPDT switch is used

Set to 2PORT_SW([2DIV_CTRL: B0 0x48(1)])＝0b1 and ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b0. ANT_SW and TRX_SW are output as follows during IDLE, TX, and RX states (default setting): If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarities of ANT_SW and TRX_SW are reversed. The setting of INV_ANT_SW([2DIV_CTRL: B0 0x48(3)]) will become invalid and does not affect the following operations.

TX/RX state	INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0 (default setting)		INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	H	L	L	H	Idle state
TX	L	H	H	L	TX state
RX	H	L	L	H	This is the initial state when Diversity disable is set to 0b0 ([2DIV_CTRL: B0 0x48(0)]=0b0) and at the start of Diversity when Diversity is enabled ([2DIV_CTRL: B0 0x48(0)]=0b1).
	L/H	H/L	H/L	L/H	If diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1), (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternately during search. When diversity is complete, it is fixed to either state.

(b) When SPDT switch is used

Set to 2PORT_SW([2DIV_CTRL: B0 0x48(1)])=0b0. ANT_SW and TRX_SW are output as follows during IDLE, TX, and RX states (default setting): If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarity of TRX_SW is reversed If ANT_CTRL1([2DIV_CTRL: B0 0x48(5)]) is set to 0b0, the setting of INV_ANT_SW([2DIV_CTRL: B0 0x48(3)]) will become invalid and does not affect the following operations.

TX/RX state	INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0 (default setting)		INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idle state
TX	L	H	L	L	TX state
RX	L	L	L	H	This is the initial state when Diversity disable is set to 0b0 ([2DIV_CTRL: B0 0x48(0)]=0b0) and at the start of Diversity when Diversity is enabled ([2DIV_CTRL: B0 0x48(0)]=0b1).
	H/L	L	H/L	H	If diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1), (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternately during search. When the diversity is complete, it is fixed to either state.

By setting INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0b1 and ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b1 to the above default setting, the polarity of ANT_SW pin will be reversed.

TX/RX state	INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0 If ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0 (default setting)		INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=1 If ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	This is the initial state when Diversity disable is set to 0b0 ([2DIV_CTRL: B0 0x48(0)]=0b0) and at the start of Diversity when Diversity is enabled ([2DIV_CTRL: B0 0x48(0)]=0b1).
	H/L	L	L/H	L	If diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1), (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternately during search. When the diversity is complete, it is fixed to either state.

(2) Antenna switch forced setting

By using [ANT_CTRL: B0 0x4C] register, ANT_SW pin output status can be set forcibly.

TX: By setting TX_ANT_EN([ANT_CTRL: B0 0x4C(0)])=0b1, the setting value of TX_ANT([ANT_CTRL: B0 0x4C(1)]) will be output.

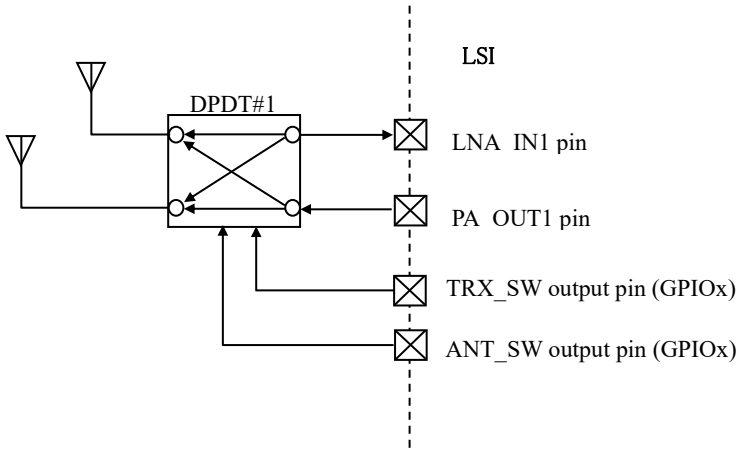
RX: By setting RX_ANT_EN([ANT_CTRL: B0 0x4C(4)])=0b1, the setting value of RX_ANT([ANT_CTRL: B0 0x4C(5)]) will be output.

However, when output is defined forcibly by [GPIO*_CTRL: B0 0x4E - 0x51] registers, [GPIO*_CTRL:B0 0x4E - 0x51] register settings have higher priority.

Antenna switching control signals can also be used as follows.

[Example 1] Using one DPDT switch

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) to 0b1.

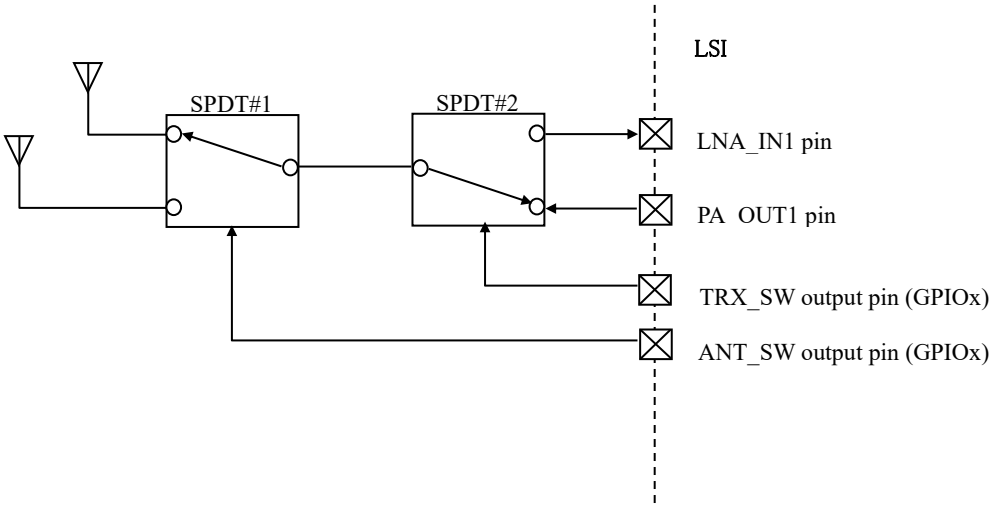


(*) By allocating one more GPIO to an external PA, it becomes possible to control both DPDT SW and the external PA.

(*) The external circuits around LNA_IN1 pin and PA_OUT1 pin, and antenna switch (DPDT#1) are omitted in this example.

[Example 2] Using two SPDT switches

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) to 0b0.



(*) By allocating one more GPIO to an external PA, it becomes possible to control both DPDT SW and the external PA.

(*) The external circuits around LNA_IN1 pin and PA_OUT1 pin, and antenna switch (DPDT#2) are omitted in this example.

6-11-6-5 ○CCA (Clear Channel Assessment) Function

ML36N7421 supports CCA function. Upon receipt of a frequency channel, the CCA function determines whether the specific channel is in-use (BUSY) or available (IDLE). ML7436N7421 supports three modes: Normal mode, Continuous mode, and IDLE detection mode. These modes can be set as follows:

[CCA mode setting]

	[CCA_CTRL: B0 0x39]			Termination condition
	Bit4 (CCA_EN)	Bit5 (CCA_CPU_EN)	Bit6 (CCA_IDLE_EN)	
Normal mode	0b1	0b0	0b0	When IDLE/BUSY is detected
Continuous mode	0b1	0b1	0b0	When stop instruction is given by CPU
IDLE detection mode	0b1	0b0	0b1	When IDLE is detected

CCA judgment is based on the comparison of average ED value [ED_RSLT: B0 0x3A] to CCA threshold [CCA_LVL: B0 0x37]. If the average ED value exceeds the CCA threshold value, it is determined as "BUSY" and CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)])=0b01 is set. If the average ED value continues to be smaller than CCA threshold value for the duration of IDLE detection period [IDLE_WAIT[9:0]([IDLE_WAIT_H: B0 0x3B], [IDLE_WAIT_L: B0 0x3C])] or longer, it is determined to be IDLE and sets CCA_RSLT[1:0]=0b00. For the detailed operation of IDLE_WAIT[9:0], refer to "(5) IDLE detection for long time period".

Also, when an instantaneous rise of ED value is detected while the average ED value is below CCA threshold, IDLE judgment is not given for a certain period of time. For the detailed operation, refer to "(4) IDLE determination exclusion under strong signal input".

(1) Normal mode

Normal mode continues CCA until IDLE/BUSY is detected. When CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b0, and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b0 are set, CCA (normal mode) is executed by RX_ON.

If "BUSY" or "IDLE" state is detected, CCA completion interrupt (INT[18] of group 3) is generated,

and CCA_EN bit is cleared to 0b0 automatically.

Upon clearing CCA completion interrupt, CCA_RSLT[1:0] is reset to 0b00. Therefore, CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

Time from CCA command issue to CCA completion is in the formula below.

[IDLE detection]

CCA execution time = (ED value average times + IDLE_WAIT setting) * Average interval (16 us (*1)) + Gain switching wait time (50 us (*2)) * Gain switching count)

[BUSY detection]

CCA execution time = ED value average times * Average interval (16 us (*1)) + Gain switching wait time (50 us (*2)) * Gain switching count)

(*1) The average interval can be calculated by the formulas indicated below based on the setting values of MSTR_CLK_SEL1([CLK_SET1: B0 0x02(5)]) and MSTR_CLK_SEL2([CLK_SET1: B0 0x02(6)]).

MSTR_CLK_SEL1=0b0, MSTR_CLK_SEL2=0b0 …$(1/F_{REF})*24*32$

MSTR_CLK_SEL1=0b0, MSTR_CLK_SEL2=0b1 …$(1/F_{REF})*26*32$

MSTR_CLK_SEL1=0b1, MSTR_CLK_SEL2=0b0 …$(1/F_{REF})*12*32$

MSTR_CLK_SEL1=0b1, MSTR_CLK_SEL2=0b1 …$(1/F_{REF})*13*32$

(*2) When F_{REF}=48 MHz, CHFIL_BW_ADJ[9:0]([CHFIL_BW: B0 0x54], [CHFIL_BW_OPTION: B0 0x6B(5-4)])=0x006, [RSSI_STABLE_TIME:B1 0x12]=0x00, [RSSI_STABLE_RES: B1 0x0F]=0x00 are set.

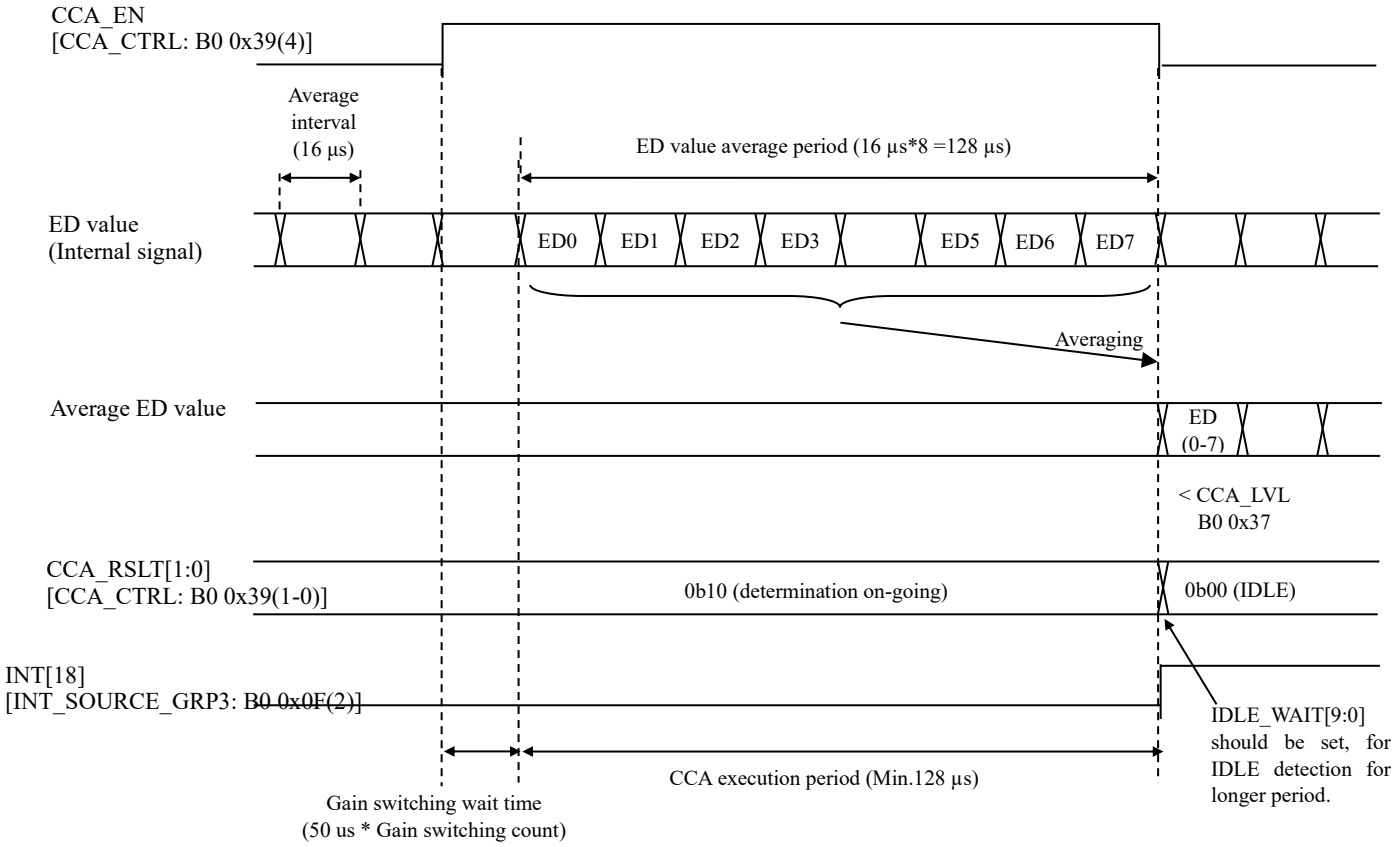
* The above formulas do not take the IDLE detection exclusion by [CCA_IGNORE_LVL: B0 0x36] into account.

For the detailed operation of [CCA_IGNORE_LVL: B0 0x36], refer to ”IDLE determination exclusion under strong signal input”.

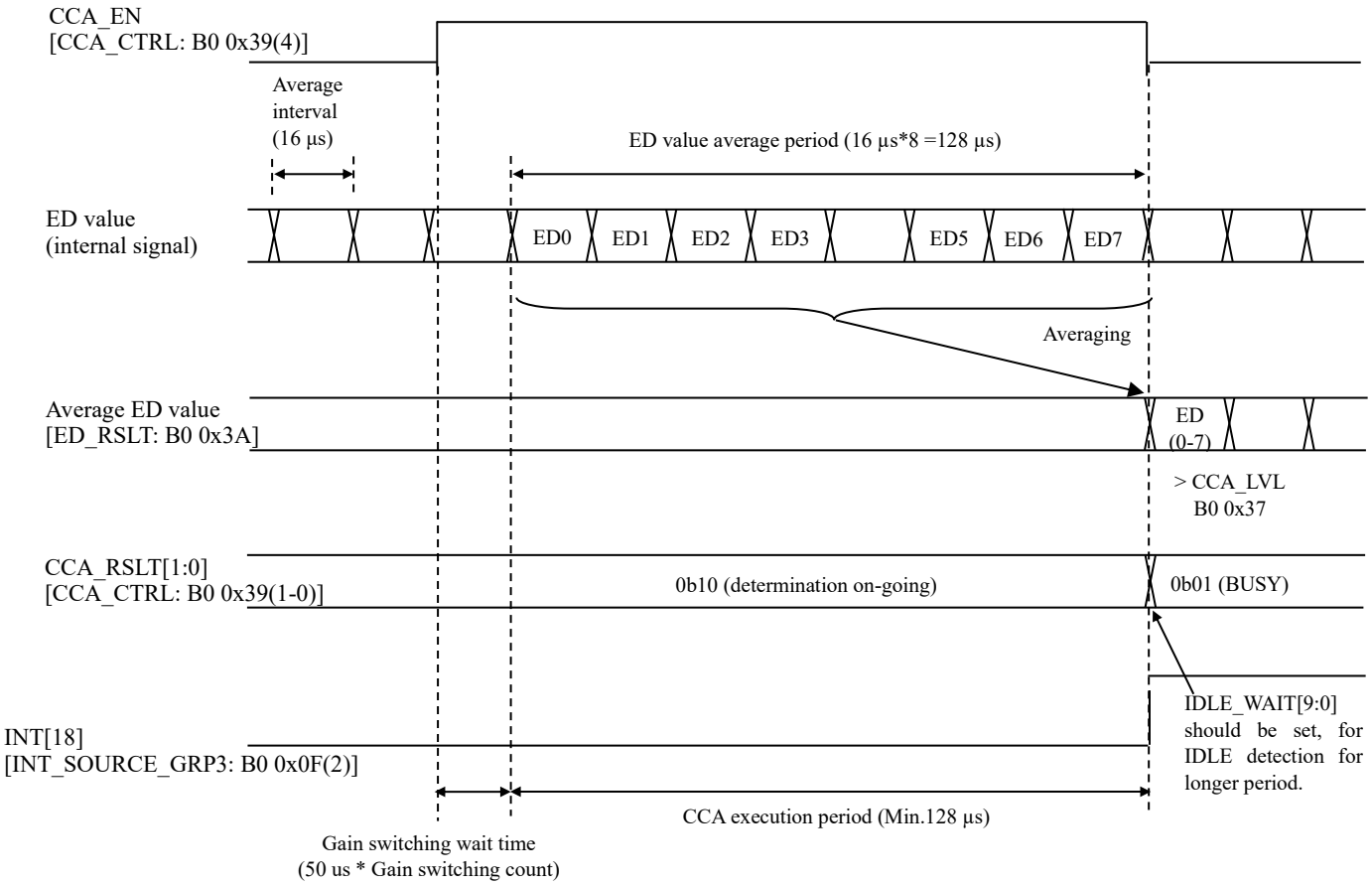
Following is the timing diagram of normal mode.

[Condition]	
ED_AVG[2:0]=0b011 (ED value 8 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection time 0 µs)	[IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]

[IDLE detection case]



[BUSY result case]



(2) Continuous mode

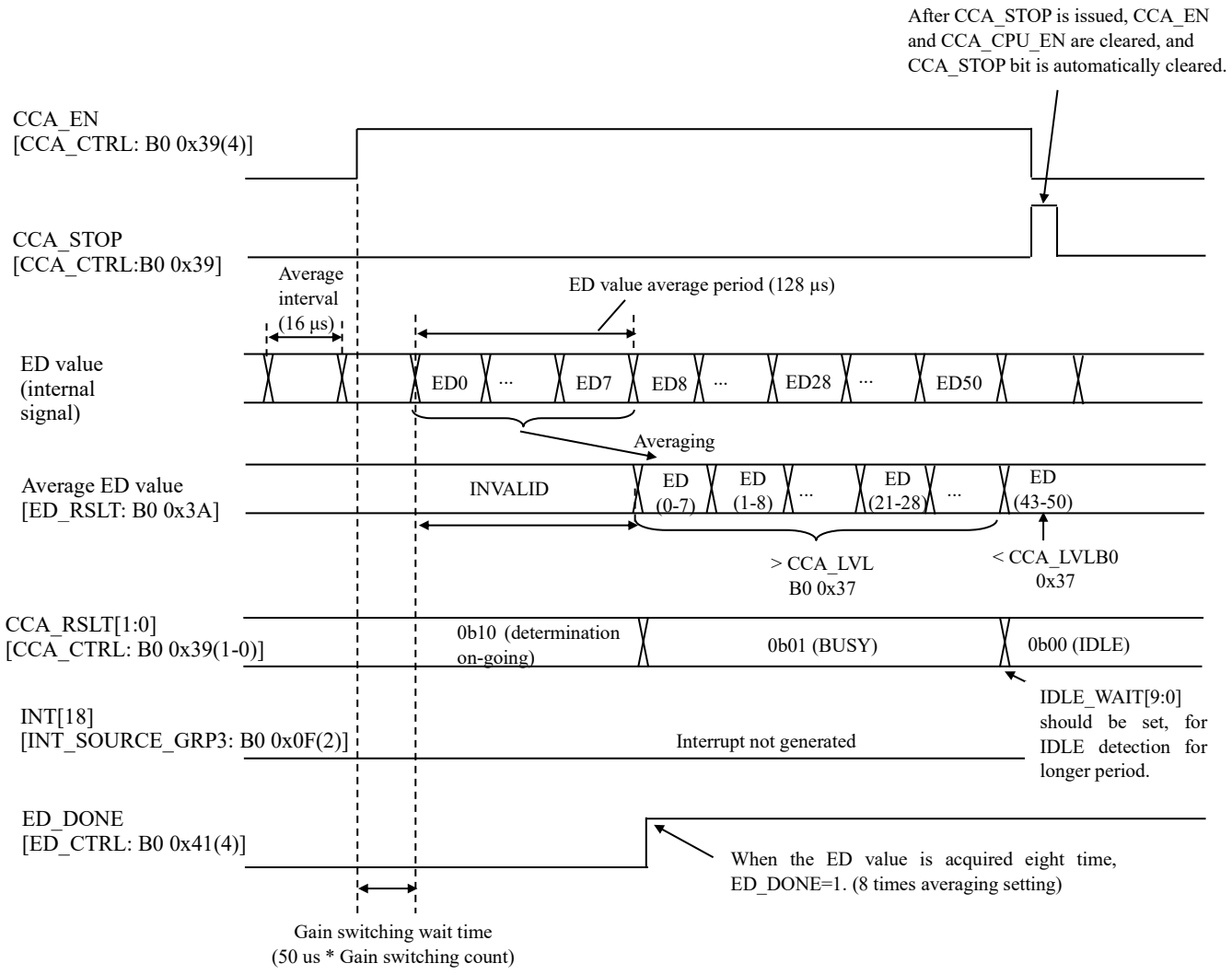
Continuous mode continues CCA until terminated by the host MCU. When CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b1, and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b0 are set, CCA (continuous mode) is executed by RX_ON.

The continuous mode does not stop the operation also when "BUSY" or "IDLE" is detected. CCA operation continues until 0b1 is set to CCA_STOP([CCA_CTRL: B0 0x39(7)]). Result is updated every time the ED value is acquired. At this time, CCA completion interrupt INT[18]([INT_SOURCE_GRP3:B0 0x0F(2)]) will not be generated.

Following is the timing diagram of continuous mode.

[Condition]	
ED_AVG[2:0]=0b011 (ED value 8 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection time 0 µs)	[IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]

[BUSY to IDLE transition, terminated with CCA_STOP]



(3) IDLE Detection mode

IDLE detection mode continues CCA until IDLE detection. When CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b0, and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b1 are set, CCA (IDLE detection mode) is executed by RX_ON.

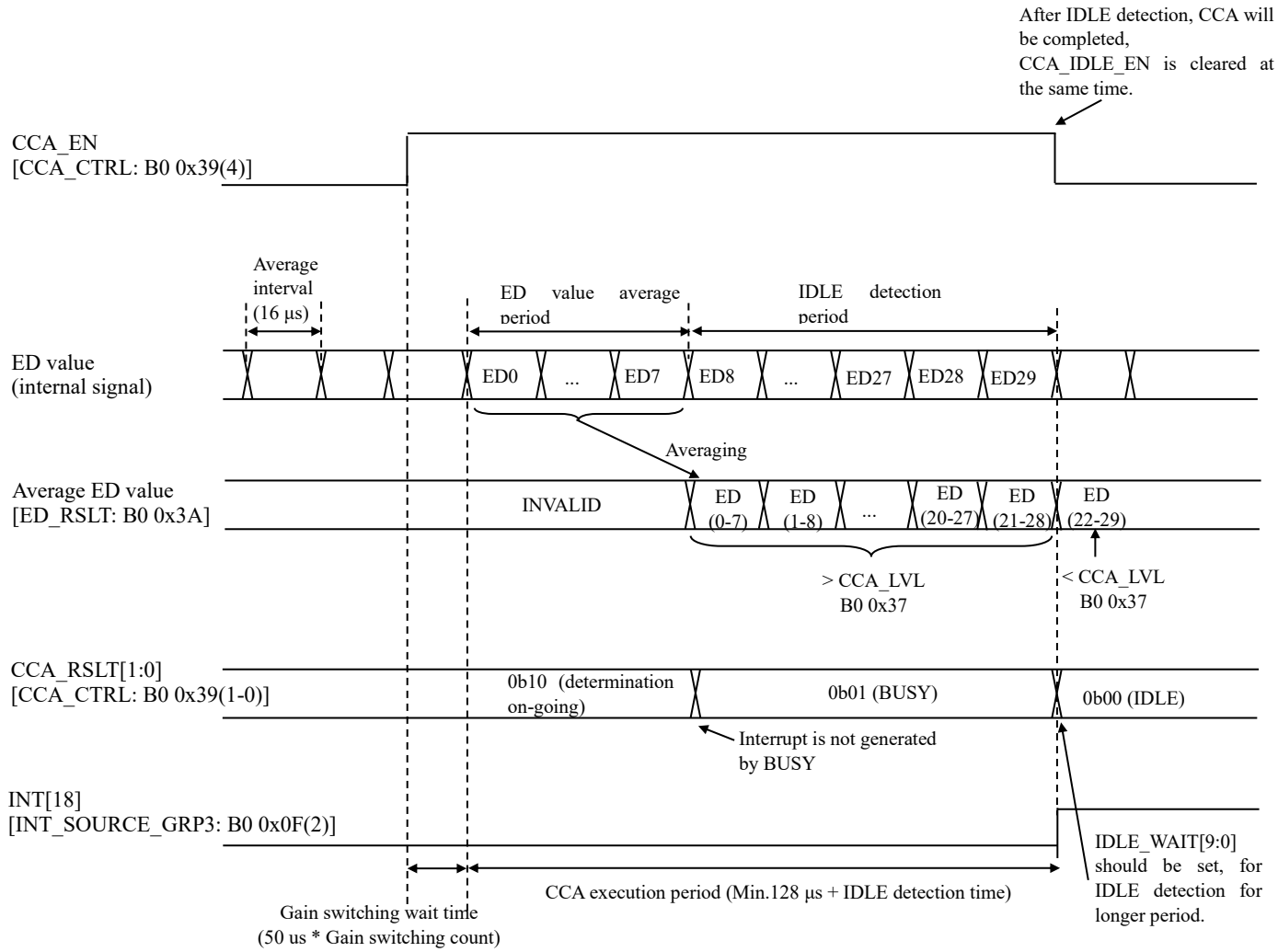
In IDLE detection mode, CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is generated only when IDLE is detected. Also, when CCA is executed by CCA_EN setting, CCA_EN(CCA_CTRL: B0 0x39(4)]) and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)]) are cleared to 0b0 automatically.

In IDLE detection mode, CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is not generated while BUSY is detected, and continues to detect IDLE. When CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is cleared, CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) is reset to 0b00. Therefore, CCA_RSLT[1:0] should be read before CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is cleared.

The following is the timing diagram of IDLE detection.

[Upon BUSY detection, continue CCA and IDLE detection case]

[Condition]	
ED_AVG[2:0]=0b011 (ED value 8 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection time 0 µs)	[IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]



(4) IDLE determination exclusion under strong signal input

If acquired ED value exceeds the value set by [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed as long as the given ED value is included in the averaging target range. If the average ED value including the ED value of strong signal input exceeds the CCA threshold value, it is determined as "carrier detected (BUSY)". And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) is set to 0b01. If this average ED value is equal to or smaller than the CCA threshold, it is determined as "CCA evaluation on-going (ED value excluded from CCA judgment acquired)", and CCA_RSLT[1:0] is set to 0b11.

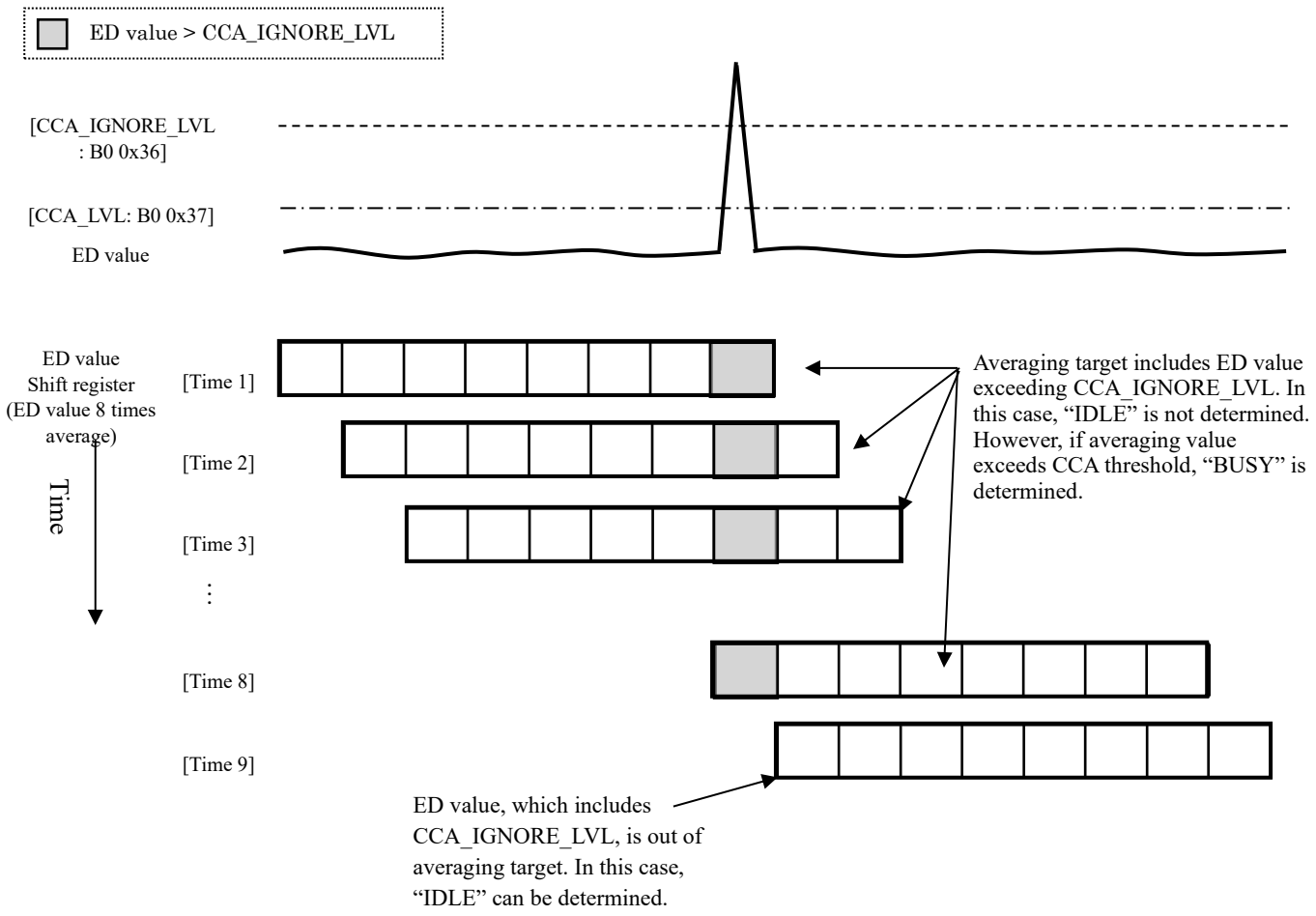
Even if the average ED value is equal to or smaller than [CCA_LVL: B0 0x37], if any of the ED values included in the averaging process exceeded [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed. At this time, CCA_RSLT[1:0] indicates 0b11 (determination on-going) and continues CCA.

If the average ED value exceeds [CCA_LVL: B0 0x37], it is determined as BUSY immediately regardless of the comparison result of [CCA_IGNORE_LVL: B0 0x36].

[Note]

1. CCA completion interrupt is notified of only when CCA result is judged as IDLE or BUSY. Therefore, if data whose ED value exceeds CCA_IGNORE_LVL is input intermittently, neither "IDLE" or "BUSY" can be determined and CCA may continue.
2. Set [CCA_IGNORE_LVL: B0 0x36] in a way so that the relationship of [CCA_IGNORE_LVL:B0 0x36] ≥ [CCA_LVL: B0 0x37] is maintained.

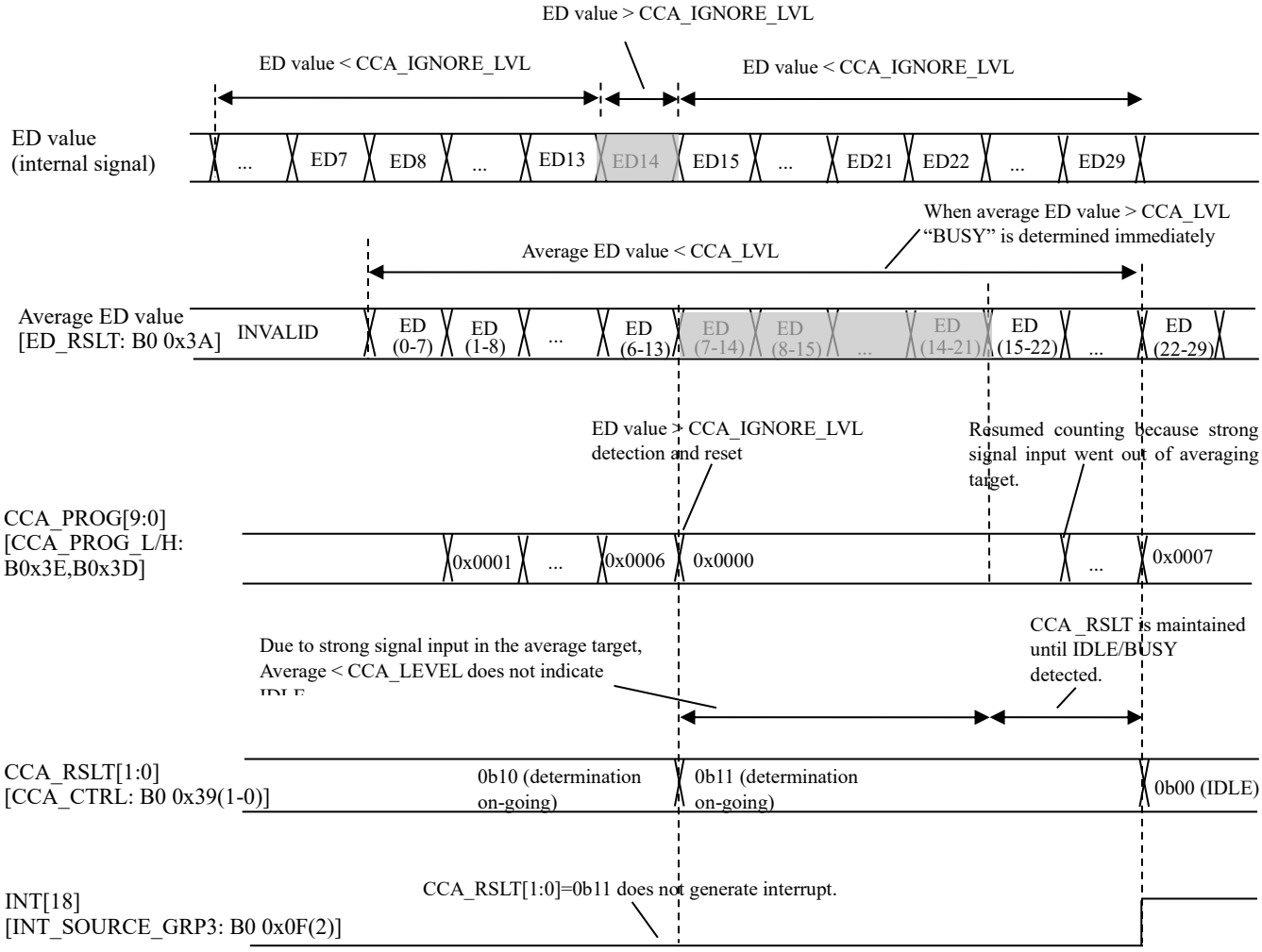
[ED value acquisition under strong signal input]


ED value > CCA_IGNORE_LVL
[CCA_IGNORE_LVL
: B0 0x36]
[CCA_LVL: B0 0x37]
ED value
ED value
Shift register
(ED value 8 times
average)
Time
[Time 1]
[Time 2]
[Time 3]
[Time 8]
[Time 9]
Averaging target includes ED value exceeding CCA_IGNORE_LVL. In this case, “IDLE” is not determined. However, if averaging value exceeds CCA threshold, “BUSY” is determined.
ED value, which includes CCA_IGNORE_LVL, is out of averaging target. In this case, “IDLE” can be determined.

The following is the timing diagram when ED value under strong signal input was acquired.

[During IDLE_WAIT counting, detected strong signal input. After the given signal is out of averaging target, IDLE detection case]

[Condition]	
CCA mode ED_AVG[2:0]=0b011(ED value 8 times average) IDLE_WAIT[9:0]=0b00_0000_0111 (IDLE detection time 112 µs)	Normal mode [ED_CTRL: B0 0x41(2-0)] [IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]



(5) IDLE Detection for long time period

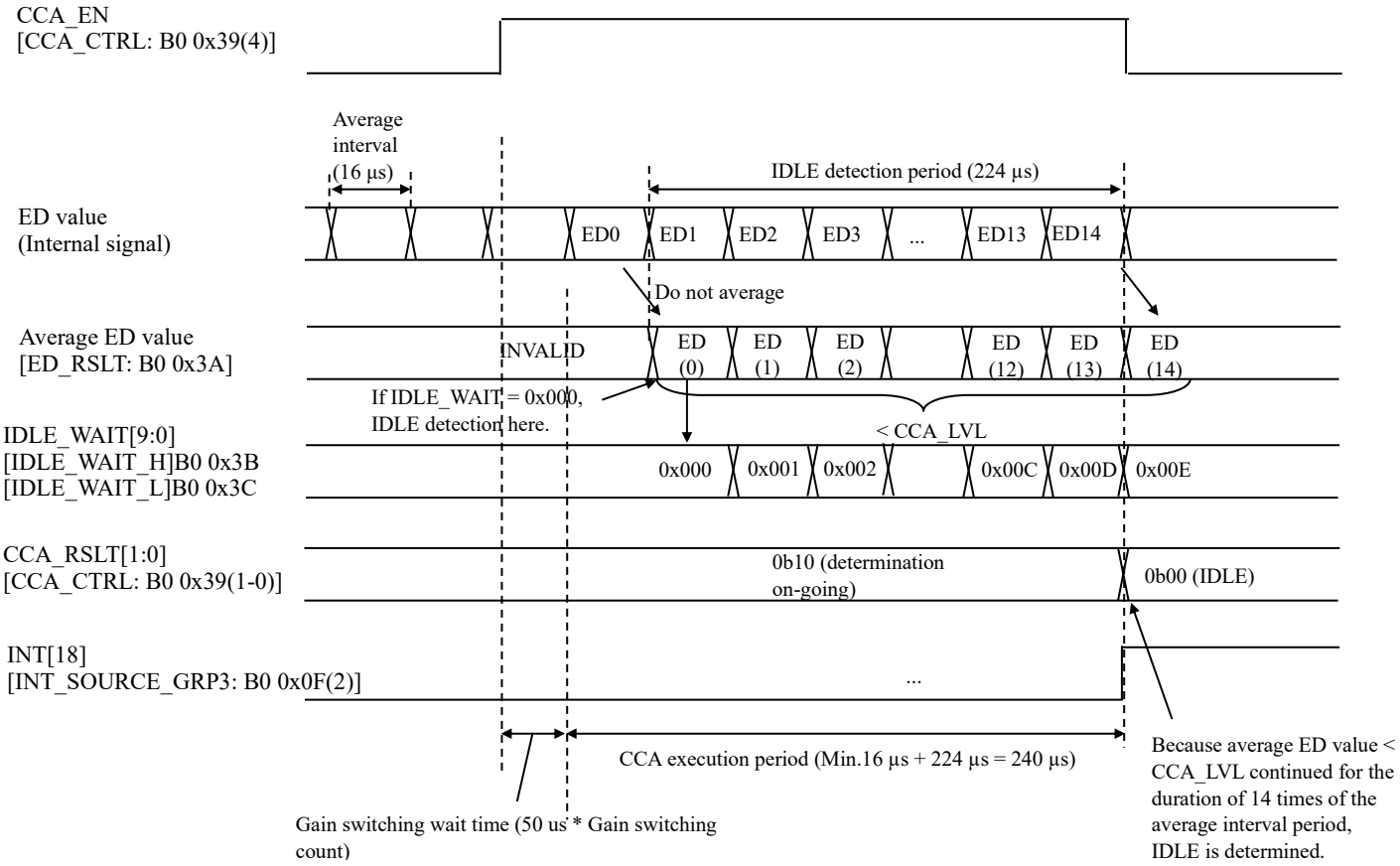
IDLE detection period can be adjusted by IDLE_WAIT [9:0] of [IDLE_WAIT_H: B0 0x3B(1-0)] and [IDLE_WAIT_L:B0 0x3C].

By using IDLE_WAIT [9:0] of [IDLE_WAIT_H: B0 0x3B(1-0)] and [IDLE_WAIT_L:B0 0x3C], it is possible to detect IDLE longer than the average period (128 μs for eight times of averaging process with 16 μs average interval). This function determines IDLE when the average ED value is equal to or below [CCA_LVL: B0 0x37] for the duration of time set by IDLE_WAIT [9:0] or longer. Even when this function is used, when the average ED value exceeds [CCA_LVL: B0 0x37], "BUSY" is determined immediately without waiting for the duration of time set by IDLE_WAIT [9:0] or longer.

The following timing diagram is IDLE detection setting IDLE_WAIT[9:0].

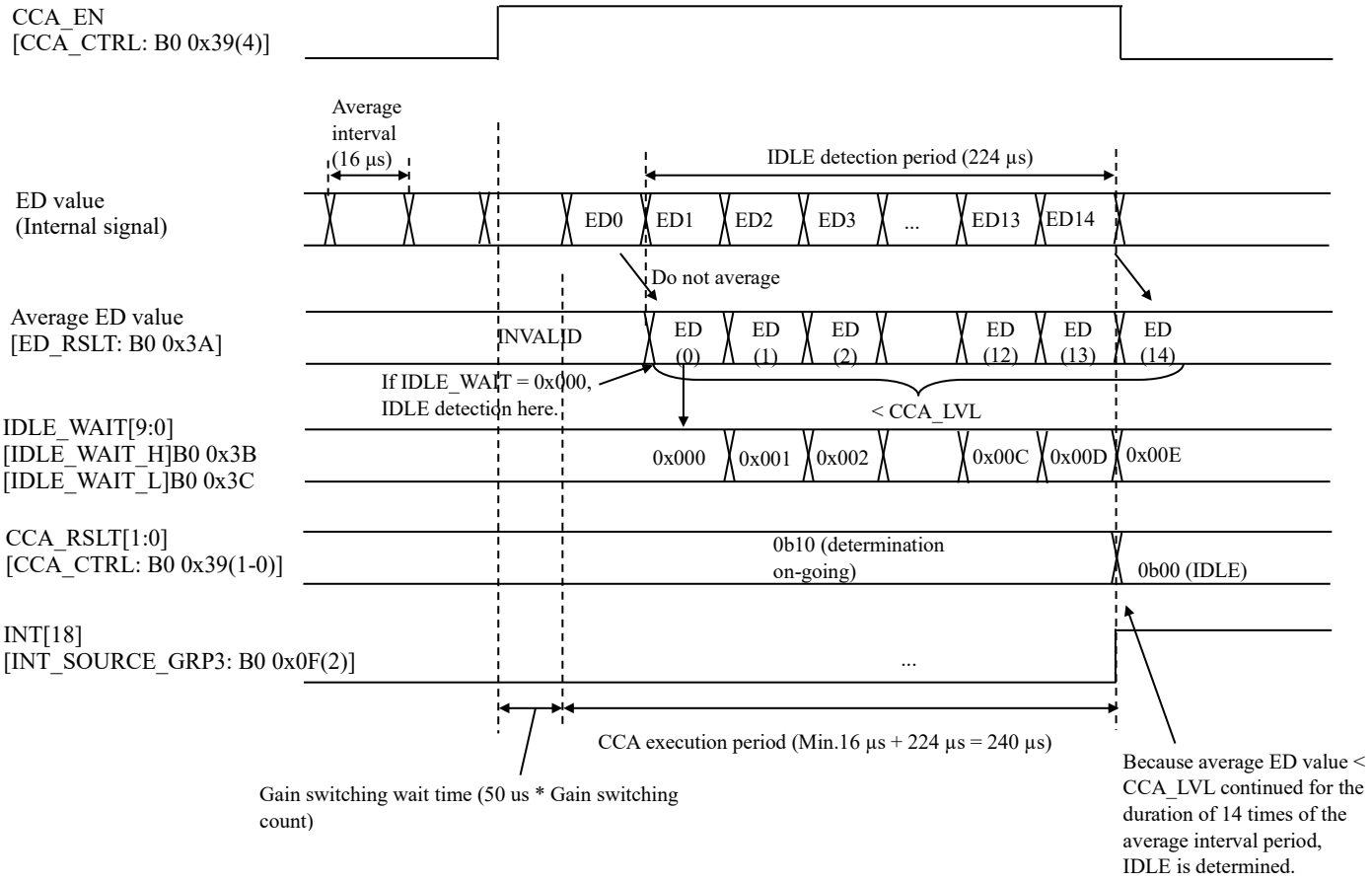
[ED value 8 time average IDLE detection case]

[Condition]	
CCA mode	Normal mode
ED_AVG[2:0]=0b011(ED value 8 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0011 (IDLE detection time 48 μs)	[IDLE_WAIT_H: B0 0x3B(1-0)], [IDLE_WAIT_L: B0 0x3C]


CCA_EN
[CCA_CTRL: B0 0x39(4)]
Average interval (16 µs)
IDLE detection period (224 µs)
ED value (Internal signal)
ED0
ED1
ED2
ED3
...
ED13
ED14
Do not average
Average ED value [ED_RSLT: B0 0x3A]
INVALID
ED (0)
ED (1)
ED (2)
ED (12)
ED (13)
ED (14)
If IDLE_WAIT = 0x000, IDLE detection here.
< CCA_LVL
IDLE_WAIT[9:0]
[IDLE_WAIT_H]B0 0x3B
[IDLE_WAIT_L]B0 0x3C
0x000
0x001
0x002
0x00C
0x00D
0x00E
CCA_RSLT[1:0]
[CCA_CTRL: B0 0x39(1-0)]
0b10 (determination on-going)
0b00 (IDLE)
INT[18]
[INT_SOURCE_GRP3: B0 0x0F(2)]
...
CCA execution period (Min.16 µs + 224 µs = 240 µs)
Gain switching wait time (50 us * Gain switching count)
Because average ED value < CCA_LVL continued for the duration of 14 times of the average interval period, IDLE is determined.

[ED value 1 times average IDLE detection case]

[Condition]	
CCA mode	Normal mode
ED_AVG[2:0]=0b000 (ED value 1 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_1110 (IDLE detection time 224 µs)	[IDLE_WAIT_H: B0 0x3B(1-0)], [IDLE_WAIT_L: B0 0x3C]



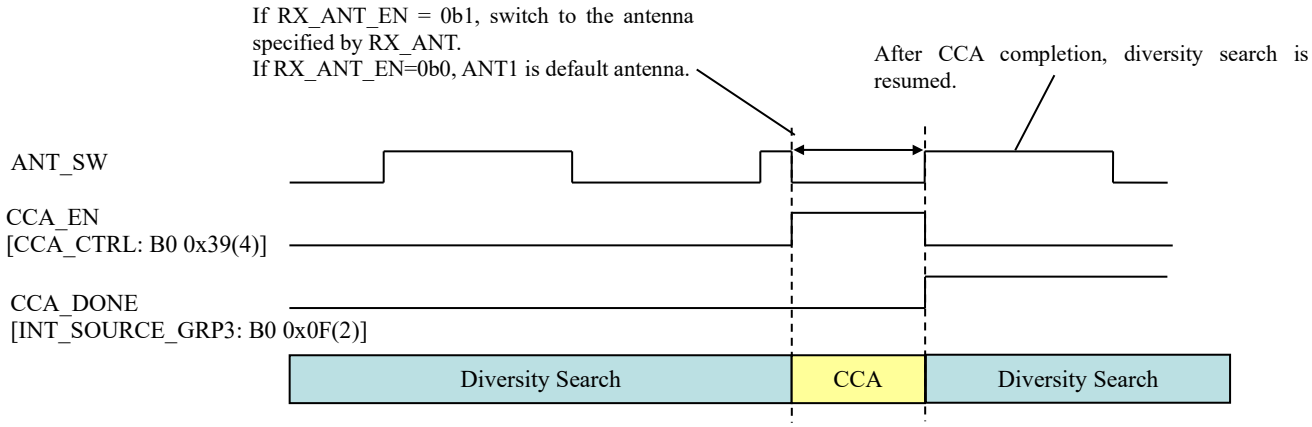
(6) CCA operation during diversity

(a) CCA operation during diversity search

During diversity search, if CCA command is issued, diversity search will be terminated and CCA will start.

Upon CCA starting, antenna is fixed to the reset value (*1), and is maintained until the next diversity search is conducted. However, if antenna specification function ([ANT_CTRL: B0 0x4C(5-4)]) is enabled, it is fixed to the antenna which was specified by the register function. After CCA completion, diversity search will be resumed.

*1: The setting is described in the upper most section of "RX" of each table in "Function Description Diversity Function ANT_SW/TRX_SW Setting".



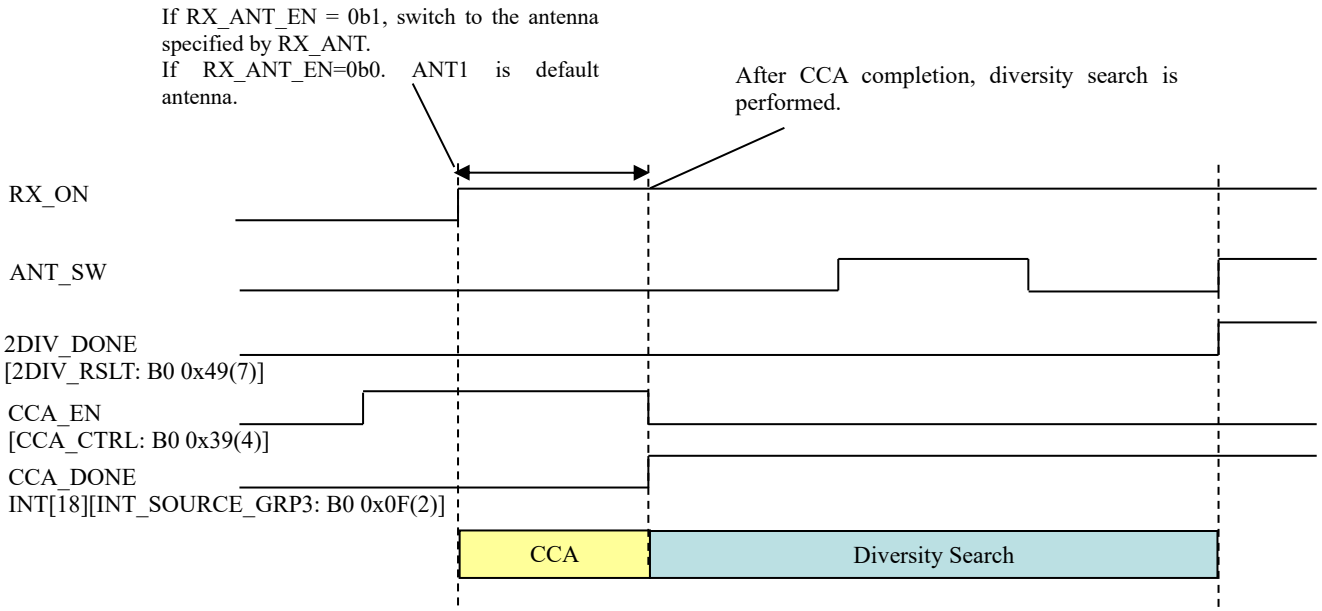
[Note]

During CCA operation, RX operation is performed at the same time. Even if CCA completion interrupt is not generated, SyncWord detection interrupt ([INT_SOURCE_GRP2: B0 0x0E(5)]), FIFO-Full trigger interrupt ([INT_SOURCE_GRP1: B0 0x0D(5)]), RX completion interrupt ([INT_SOURCE_GRP3: B0 0x0E(0)]), and CRC detection error interrupt ([INT_SOURCE_GRP3: B0 0x0E(1)]) may be generated.

For details of diversity function, refer to "Diversity Function".

(b) Operation when CCA is executed before RX_ON during diversity ON

If diversity ON setting and CCA operation setting are enabled before transition to RX_ON state, diversity search is executed only after transition to RX_ON state and CCA completion.



(7) CCA threshold setting

CCA threshold value, defined by [CCA_LVL: B0 0x37] register, should be set by considering the desired input level (ED value), variations (IC components variation, temperature fluctuation), and other losses (antenna, matching circuits, etc.). Relationship between input level and ED value are described in the 6-11-6-2 ○Energy Detection Value (ED value) Acquisition Function clause of "Energy Detection Value (ED value) Acquisition Function".

In order to validate whether CCA threshold is reasonable or not, CCA should be executed every time the input level has changed, in order to check the level where IDLE changes to BUSY.

6-11-6-6 ○Channel Search Function

ML36N7421 supports channel search function. Channel search function switches channels in RX_ON status and checks whether or not carrier is detected. If carrier is detected, the reception is continued on the channel, where the carrier was detected. Registers related to channel search are as follows:

Function	Register
Channel search enable setting	CH_SRCH_EN([SEARCH_CH_SET: B8 0x01(0)])
Channel search mode	CH_SRCH_MODE([SEARCH_CH_SET: B8 0x01(2-1)])
ED value calculation average times setting	SRCH_ED_AVG([SEARCH_CH_SET: B8 0x01(6-4)])
Synchronization detection wait time resolution setting	SRCH_TIME_RES([SEARCH_CH_SET: B8 0x01(7)])
Search channel enable (CH0-CH7)	[SEARCH_CH_EN: B8 0x02]
Search channel number setting (CH0-CH7)	[SEARCH_CH0: B8 0x03]- [SEARCH_CH7: B8 0x0A]
ED value threshold setting	[SRCH_ED_TH: B8 0x0B]
PLL convergence wait time setting	[PLL_WAIT_TIMER: B8 0x0C]
ED value convergence wait time setting	[ED_WAIT_TIMER: B8 0x0D]
Synchronization detection wait time setting	[SYNC_WAIT_TIMER: B8 0x0E] [SYNC_WAIT_TIMER2: B8 0x0F]
Acquired ED value display (ANT1/2)	[SRCH_ED_ANT1: B8 0x10]/ [SRCH_ED_ANT2: B8 0x11]
Channel number display after channel search complete	[SRCH_CH: B8 0x12]
Frequency hopping channel search setting	FH_CH_SRCH_EN([FH_MAX_CH: B8 0x14(0)])
Maximum channel setting of the frequency hopping channel search	[FH_MAX_CH: B8 0x15]
Random channel number generation setting	RANDOM_CH EN([FH_SET: B8 0x15(1)])
Random channel number display	[RANDOM_CH_DISP: B8 0x16]

(1) Arbitrary channel search

This function checks the availability of carriers and signals to be received on an arbitrary channel. When any carrier or signals to be received is detected, channel search is stopped, and the reception on the detected channel is continued. In case of RX completion or SYNC error (out-on-sync during RX), the

channel search is resumed from the next channel where search had stopped. As to the channels to be searched, maximum eight channels can be set whether or not to be searched by ON/OFF control ([SEARCH_CH_EN: B8 0x02]). To each of eight channels, any channel number (0 to 255 channel) can be assigned ([SEARCH_CH0: B8 0x03] - [SEARCH_CH7: B8 0x0A]) This function switches channels automatically during RX. During TX, channel numbers set in [CH_SET: B0 0x09] are applied.

[Note]

1. Although any channel can be set (0 to 255 channel), the channel to be set should be within the frequency range which was specified during the VCO calibration.
2. Execute VCO calibration at On-Demand method.

The channel detection condition can be set by the channel search mode (CH_SRCH_MODE([SEARCH_CH_SET: B8 0x01(2-1)])).

Channel search mode CH_SRCH_MODE([SEARCH_CH_SET: B8 0x01(2-1)])	Description
00	Mode which determines based on the ED values only
01	Mode which determines based on the ED values only (with antenna switching)
10	Mode which determines based on the ED values and synchronization state (with antenna switching)
11	Reserved

The details of each mode are listed below.

(1-1) Mode which determines based on the ED values only

Set to CH_SRCH_MODE([SEARCH_CH_SET: B8 0x01(2-1)])=0b00.
Set to CH_SRCH_EN([SEARCH_CH_SET: B8 0x01(0)])=0b1, and after RX_ON, channel search starts. After switching the channels and wait for the convergence of PLL and ED values, the ED value is compared with the threshold ([SRCH_ED_TH: B8 0x0B]). Depending on the result, it is determined whether the channel search should be stopped or continued. The average processing time of ED value can be set by (SRCH_ED_AVG([SEARCH_CH_SET: B8 0x01(6-4)])) exclusively for the channel search.

Judgment conditions of channel search are as follows:

Channel search judgment	Operation after judgment
ED value ≥ Threshold value	Judged as carrier detected. Channel search is stopped.
ED value < Threshold value	Judged as carrier not detected. Channel search is continued.

After the ED value became higher than the threshold value and the channel search was stopped, if synchronization is not established within the synchronization detection wait time set by [SYNC_WAIT_TIMER2: B8 0x0F], it is judged as carrier detected but no signals to be received, and the channel search is resumed.

PLL convergence wait time, ED value convergence wait time, and synchronization detection wait time are defined by the following formulas.

PLL convergence wait time [us] = [PLL_WAIT_TIMER: B8 0x0C] / { FREF [MHz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))} x240 [us] (5 us)
ED value convergence wait time [us] = [ED_WAIT_TIMER: B8 0x0D] / { FREF [MHz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))} x240 [us] (5 us)
Synchronization detection wait time after channel search completion [us] = [SYNC_WAIT_TIMER2: B8 0x0F] * time resolution

* Time resolution is set by SRCH_TIME_RES([SERCH_CH_SET: B3 0x72(7)]).
When SRCH_TIME_RES =0: 240 / { FREF [MHz] / (2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))}(10 us)
When SRCH_TIME_RES =1: 6000 / { FREF [MHz] / (2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))}(250 us)

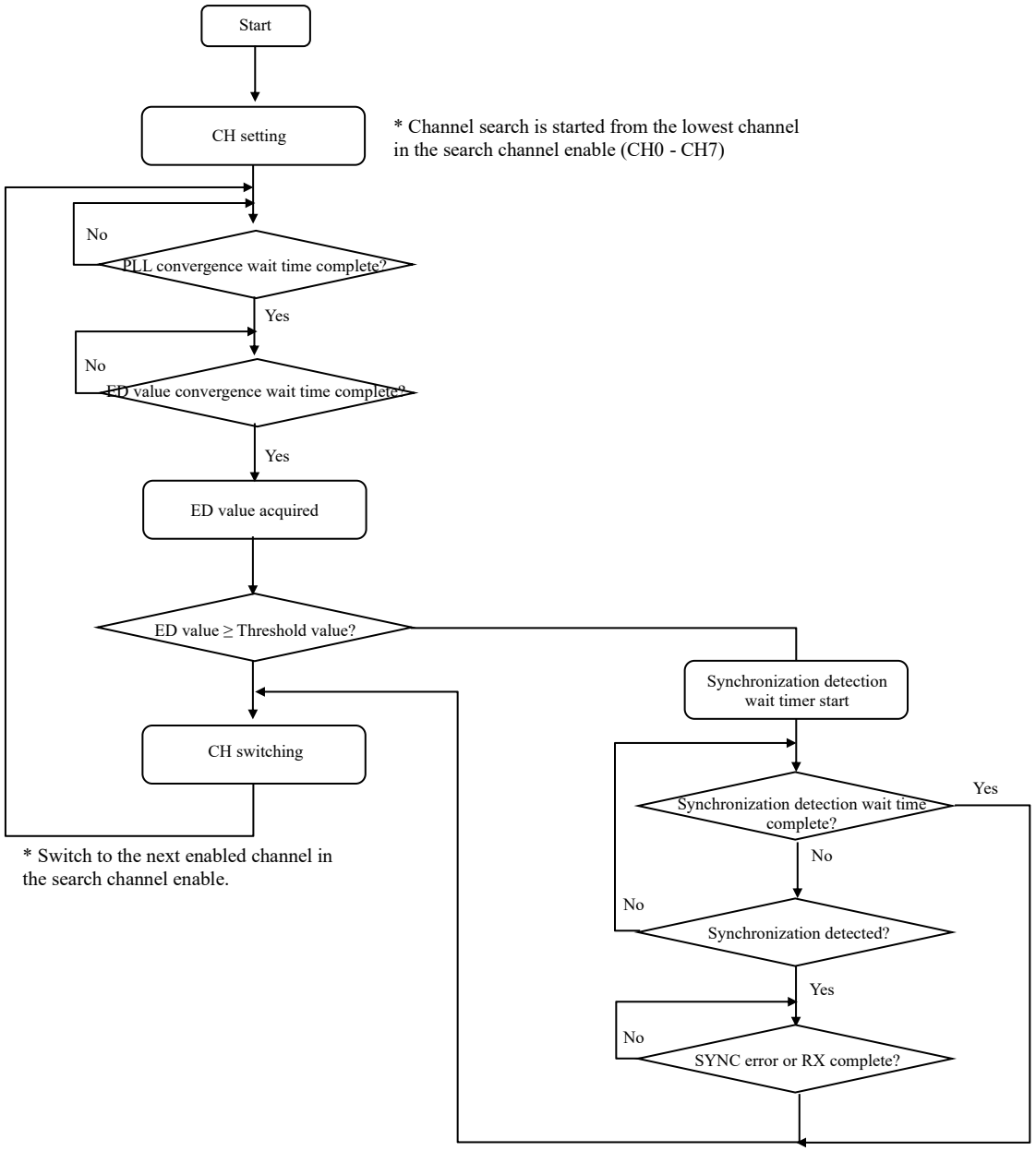
* The time resolution in the parentheses is the value when the reference clock frequency is 48 MHz.

[Note]

(a) ED value convergence wait time setting should be set appropriately according to the ED value average times setting during channel search.

(b) Synchronization detection wait time after channel search completion should be set appropriately according to the data rate.

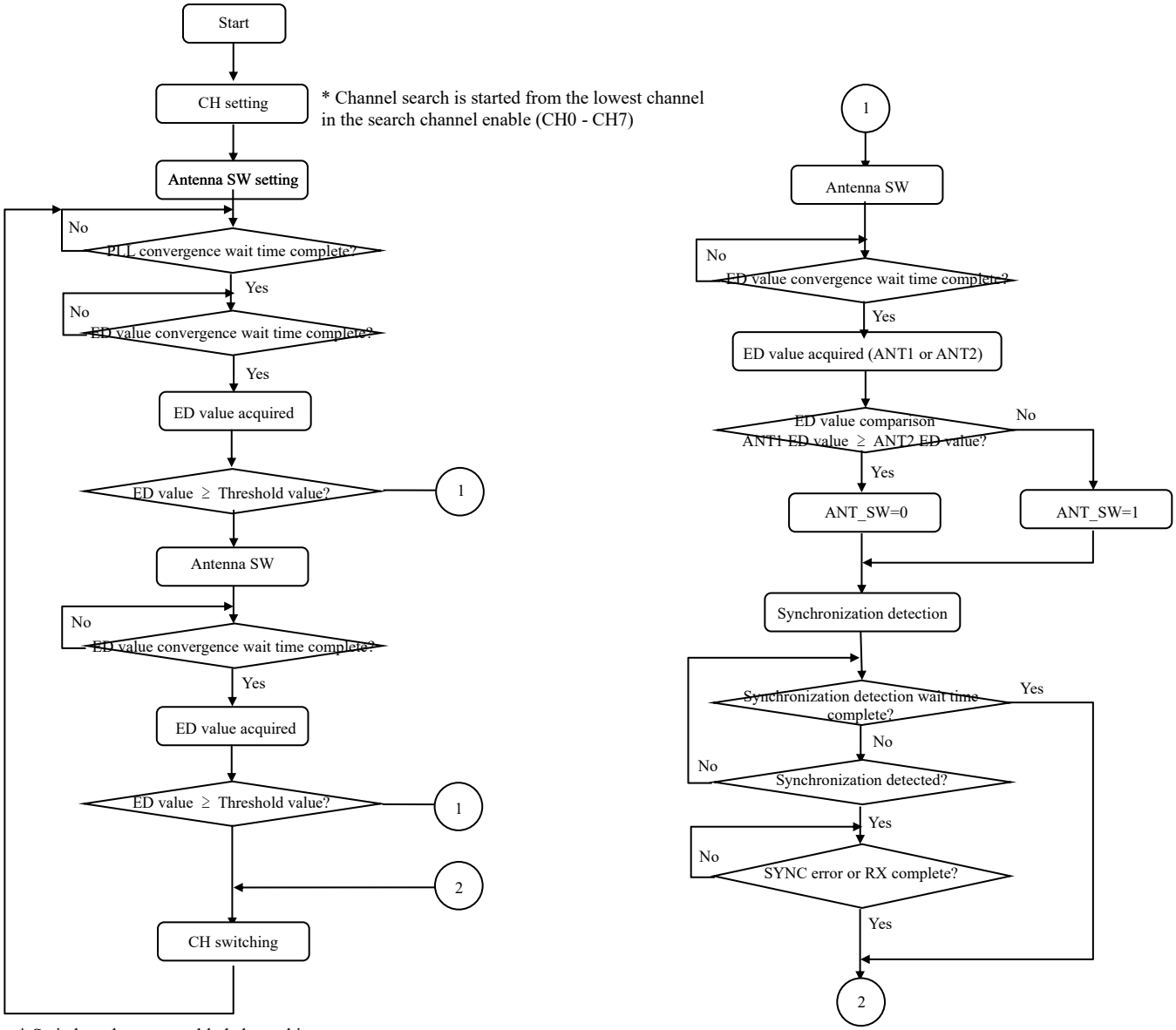
【LSI Operation Flow】



(1-2) Mode which determines based on the ED values only (with antenna switching)

Set to CH_SRCH_MODE([SEARCH_CH_SET: B8 0x01(2-1)])=0b01.
Set to CH_SRCH_EN([SEARCH_CH_SET: B8 0x01(0)])=0b1, and after RX_ON, channel search starts. After switching the channels and after the PLL and ED values convergence waiting times have passed, ED value is acquired and compared with the set threshold value ([SRCH_ED_TH: B8 0x0B]). If the ED value is smaller than the threshold value, antennas are switched. With the switched antenna, the ED value is compared with the threshold value. If the ED value is equal to or larger than the threshold value, the channel search is stopped. If the ED value is smaller than the threshold value, channels are switched, and the channel search is continued. Except for switching antennas, operations are same as with (a) Mode which determines based on the ED values only.

【LSI Operation Flow】



(1-3) Mode which determines based on the ED values and synchronization state (with antenna switching)

Set to CH_SRCH_MODE([SEARCH_CH_SET: B8 0x01(2-1)])=0b10.
Set to CH_SRCH_EN([SEARCH_CH_SET: B8 0x01(0)])=0b1, and after RX_ON, channel search starts. After switching the channels and wait for the convergence of PLL and ED values, the ED value is compared with the threshold ([SRCH_ED_TH: B8 0x0B]). Depending on the result of comparison and whether or not synchronization was detected within the set time period, it is determined as channel detected and the channel search is stopped. The average processing time of ED value can be set by (SRCH_ED_AVG([SEARCH_CH_SET: B8 0x01(6-4)])) exclusively for the channel search.

Judgment conditions of channel search are as follows:

Channel search judgment	Operation after judgment
ED value ≥ Threshold value and Synchronization detected	Judged as carrier detected (signals to be received) and channel search is stopped.
ED value < Threshold value	Judged as carrier not detected. Channel search is continued.

After the ED value became higher than the threshold value and the channel search was stopped, if synchronization is not established within the synchronization detection wait time set by [SYNC_WAIT_TIMER2: B8 0x0F], it is judged as carrier detected but no signals to be received, and the channel search is resumed.

PLL convergence wait time, ED value convergence wait time, and synchronization detection wait time are defined by the following formulas.

PLL convergence wait time [us] = [PLL_WAIT_TIMER: B8 0x0C] / { F_{REF} [MHz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))} ×240 [us] (5us)
ED value convergence wait time [us] = [ED_WAIT_TIMER: B8 0x0D] / { F_{REF} [MHz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))} ×240 [us] (5us)
Synchronization detection wait time during channel search =
[SYNC_WAIT_TIMER: B8 0x0E] × (10us or 250us)
Synchronization detection wait time after channel search completion =
[SYNC_WAIT_TIMER2: B8 0x0F] × (10us or 250us)

SRCH_TIME_RES =0: 240 / { FREF [MHz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))} (10us)
SRCH_TIME_RES =1: 6000 / { FREF [MHz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))} (250us)

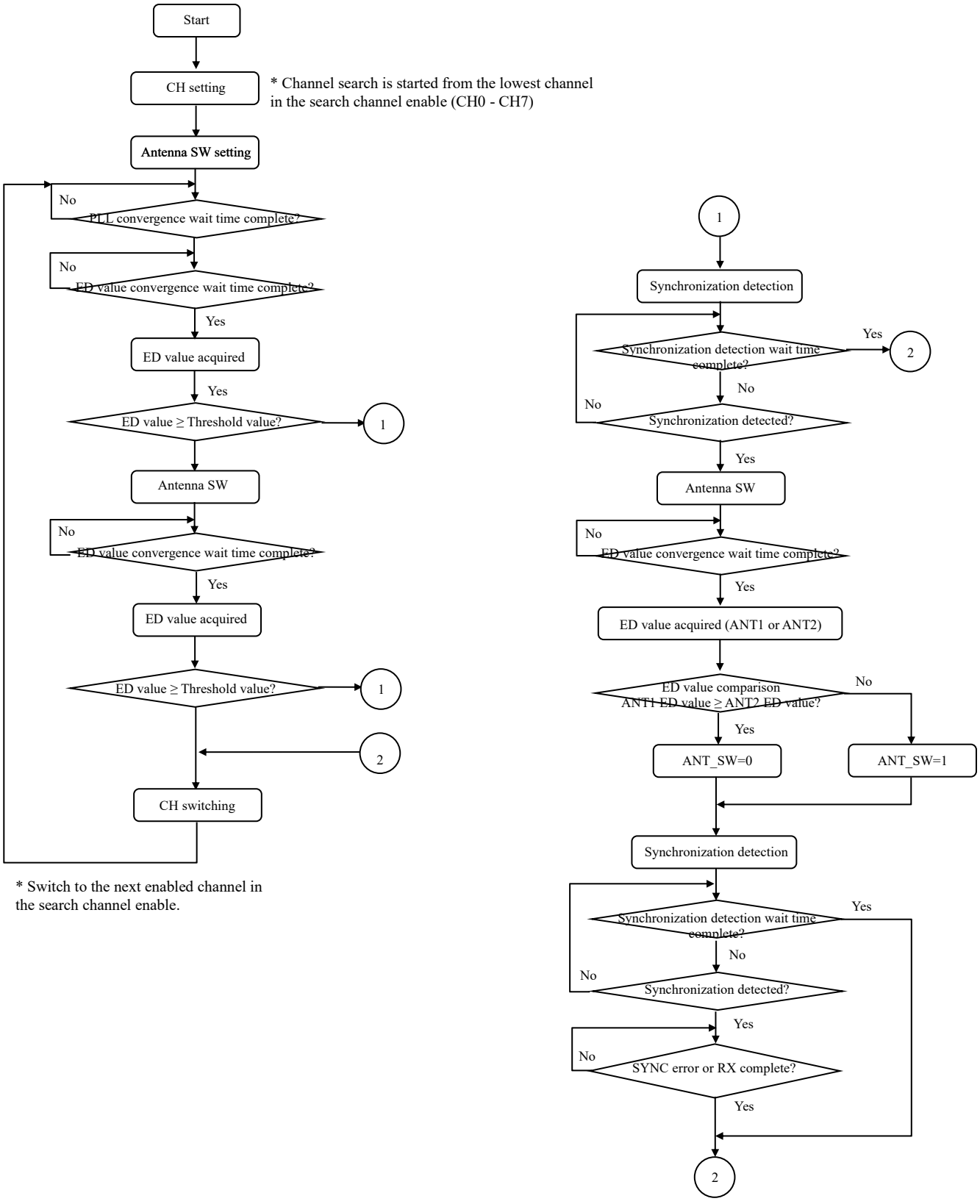
* The time resolution in the parentheses is the value when the reference clock frequency is 48 MHz.

[Note]

(a) ED value convergence wait time setting should be set appropriately according to the ED value average times setting during channel search.

(b) Synchronization detection wait time (during channel search and after channel search complete) should be set appropriately according to the data rate.

【LSI Operation Flow】



(2) Incremental channel search

Set to FH_CH_SRCH_EN([FH_MAX_CH: B8 0x14(0)])=0b1 and CH_SRCH_EN([SEARCH_CH_SET: B8 0x01(0)])=0b1. After RX_ON, channel search starts. The channel to be searched is incremented by 1, starting from channel 0 to the channel set by [FH_MAX_CH: B8 0x15]. Other operations are same as (1) Arbitrary channel search. Incremental channel search can be used to receive packets, when each of them is sent at a different frequency (frequency hopping).

[Note]

(a) Channel search needs to be completed within the preamble of packet which is sent. If the search is not completed within the preamble, SyncWord cannot be detected and packet reception may not be performed. Therefore, transmission preamble should be set longer than the time it takes to complete the channel search, with all the channels used to perform frequency hopping.

(b) Execute VCO calibration at On-Demand method.

(3) Random channel number generation

In frequency hopping, packet transmission should be performed via random channels. ML7436N has a function to generate random channel numbers. By setting RANDOM_CH EN([FH_SET: B8 0x15(1)])=0b1, random channel number generator is activated and is displayed on the random channel number display ([RANDOM_CH_DISP: B8 0x16]). The maximum channel number to be displayed is limited by the maximum channel number setting, which was specified at the time of frequency hopping channel search ([FH_MAX_CH: B8 0x15]). This function only displays the random channel numbers. To apply random channel numbers for transmission, the channel numbers which are read from the random channel number display ([RANDOM_CH_DISP: B8 0x16]) need to be set to the channel setting ([CH_SET: B0 0x09(1)]).

6-11-7. TX Related Function

6-11-7-1 ○Ramp Control Function

Ramp control function reduces the spurious emissions at the time of transmission startup and stop time.
Ramp control can be performed by the following registers.

Setting	Register
Ramp control counter increment setting	RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)])
Ramp control reference clock cycle setting	RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])
Ramp-up time setting	RAMP_CLK_SET_R([RAMP_CTRL2: B3 0x42])
Ramp-down time setting	RAMP_CLK_SET_F([RAMP_CTRL3: B3 0x43])

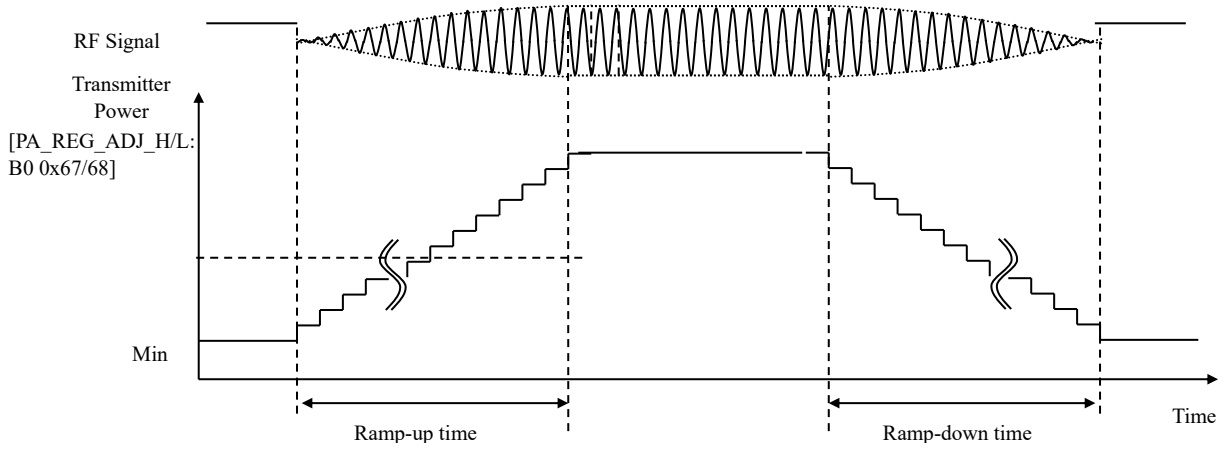
Ramp-up time and ramp-down time can be calculated by the following formulas.

Ramp-up time [s] = Ramp control reference clock cycle setting (RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])) * Ramp-up time setting (RAMP_CLK_SET_R[6:0]([RAMP_CTRL2: B3 0x42(6-0)]))} *
Maximum amplitude setting ([PA_REG_ADJ: B0 0x67(0), B0 0x68]) /
Ramp control counter increment setting (RAMP_INC[1:0]([RAMP_CTRL1: B3 0x41(1-0)]))

Ramp-down time [s] = Ramp control reference clock cycle setting (RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])) * Ramp-down time setting (RAMP_CLK_SET_F[6:0]([RAMP_CTRL3: B3 0x43(6-0)]))} *
Maximum amplitude setting ([PA_REG_ADJ: B0 0x67(0), B0 0x68]) /
Ramp control counter increment setting (RAMP_INC[1:0]([RAMP_CTRL1: B3 0x41(1-0)]))

Ramp control reference clock cycle setting can be set by the following registers.

RAMP_CLK_STEP=
0b0 …Ramp control reference clock cycle =(1/FREF)*(MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)])+1)x2
RAMP_CLK_STEP=
0b1 …Ramp control reference clock cycle =(1/FREF)*(MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)])+1)x32



In the reset state and the maximum value setting (F_{REF} =48MHz, PA output power + 13 dBm), the example of ramp-up and -down times will be as follows:

Setting register	Min Setting	Reset State	Max Setting
RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)])	0x3	0x0	0x0
RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])	0x0	0x0	0x1
RAMP_CLK_SET_R[6:0] ([RAMP_CTRL2: B3 0x42(6-0)])	0x01	0x01	0x7F
RAMP_CLK_SET_F[6:0] ([RAMP_CTRL3: B3 0x43(6-0)])	0x01	0x01	0x7F
[PA_REG_ADJ: B0 0x67/68]	0x0190	0x0190	0x0190
Ramp-up/Ramp-down time	20µs	40µs	38.6ms

6-11-7-2 ○FSK Modulation Function

(1) GFSK Modulation Function

To use GFSK mode, GFSK_EN ([DATA_SET1: B0 0x07(4)])=0b1 should be set. In GFKS modulation, frequency deviation can be set by the following registers, and the filter coefficient of Gaussian filter can be set by [FSK_DEV0_H/ GFIL0: B1 0x32] - [FSK_DEV3_H: B1 0x38] registers. 2FSK/4FSKcan be selected by FSK_SEL[DATA_SET2: B0 0x08(5)].

Frequency deviation setting	Register
Sub-GHz	[GFSK_DEV_H: B1 0x30]: Frequency deviation setting (high byte) [GFSK_DEV_L: B1 0x31]: Frequency deviation setting (low byte)
2.4GHz	[GFSK_DEV_H_2G: B4 0x6A] : Frequency deviation setting (high byte) [GFSK_DEV_L_2G: B4 0x6B] : Frequency deviation setting (low byte)

Refer to „Channel Frequency Setting" for N_{div}

(a) GFSK frequency deviation setting

F_DEV value can be calculated as the following formula

$F\_DEV = \{ f_{dev} / (S*f_{ref} / N_{div}) \} * 2^{20}$ (Integer part)

f_{dev} :Frequency deviation [Hz]

f_{ref} :PLL reference frequency（=reference clock frequency: F_{REF}）

N_{div} :PLL dividing setting value

S: PLL front divider raio (B1:0x1A(0)=0: divide by 2、1:divide by 4)

In 4GFSK mode, the value of maximum frequency deviation should be specified.

[Example] When setting the frequency deviation to 50kHz in 920MHz(Ndiv=2), the setting value be as follows (f_{REF} = 48MHz).

$F\_DEV = \{0.05MHz \div (2*48MHz/2)\} \times 2^{20} = 1092(0x0444)$ (Integer part)

[GFSK_FDEV_H/L: B1 0x30/31] should be set as below:

[GFSK_DEV_H: B1 0x30] = 0x04

[GFSK_DEV_L: B1 0x31] = 0x44

(b) Gaussian filter setting

GFSK mode can be set by GFSK_EN([DATA_SET1: B0 0x07(4)])=0b1.
The BT value of the Gaussian filter can be set by the following registers.

The following table is the relationship between the BT value and the register setting.

Register	BT value	
	0.5	1.0
[FSK_DEV0_H/GFIL0: B1 0x32]	0x24	0x00
[FSK_DEV0_L/GFIL1: B1 0x33]	0xD6	0x00
[FSK_DEV1_H/GFIL2: B1 0x34]	0x19	0x02
[FSK_DEV1_L/GFIL3: B1 0x35]	0x29	0x0C
[FSK_DEV2_H/GFIL4: B1 0x36]	0x3A	0x31
[FSK_DEV2_L/GFIL5: B1 0x37]	0x48	0x74
[FSK_DEV3_H/GFIL6: B1 0x38]	0x4C	0x9A

[Note]
GFSK filter coefficient setting registers and FSK frequency deviation setting registers are common. In GFSK mode, these registers set the filter coefficient. In FSK mode, these registers set the frequency deviation.

(2) FSK Modulation Setting

FSK mode can be set by GFSK_EN([DATA_SET1: B0 0x07(4)])=0b0. Also, fine frequency deviation can be set by [FSK_DEV0_H/GFIL0: B1 0x32] - [FSK_DEV4_L: B1 0x3B]. By adjusting the setting value of [FSK_TIM_ADJ4: B1 0x3C] - [FSK_TIM_ADJ0: B1 0x40]. FSK timing can be fine tuned. 2FSK/4FSK can be selected by FSK_SEL[DATA_SET2: B0 0x08(5)].

(a) FSK frequency deviation: F_DEV setting

F_DEV value can be calculated as the following formula

$F\_DEV = \{ f_{dev} / (S*f_{ref} / N_{div}) \} * 2^{20}$ (Integer part)

f_{dev} :Frequency deviation [Hz]

f_{ref} :PLL reference frequency（=reference clock frequency: F_{REF}）

N_{div} :PLL dividing setting value

S: PLL front divider ratio (B1:0x1A(0)=0: divide by 2、1:divide by 4)

[Example] When setting the frequency deviation to 50kHz in 920MHz(Ndiv=2), the setting value be as follows (f_{REF} = 48MHz).

$F\_DEV = \{0.05MHz \div (2*48MHz/2)\} \times 2^{20} = 1092(0x0444)$ (Integer part)

The 1st　frequency – the Max frequency deviation setting are represented by the next page table.

(b) FSK frequency deviation timing setting

Modulation timing time resolution is set by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

The center frequency time, the1st – the 4^{th} frequency deviation time depends on data patern and data rate.

These setting regsters are assigned to [FSK_TIM_ ADJ4:B1 0x3C] - [FSK_TIM_ ADJ0:B1 0x40]

Frequency deviation time is calculated by the following formula.

Frequency deviation time T = Time resolution * N

N is set to [FSK_TIM_ ADJ4:B1 0x3C]～[FSK_TIM_ ADJ0:B1 0x40] registers.

Set the register values to satisfy the relationship: Tmax < 1/(Data rate)/10.

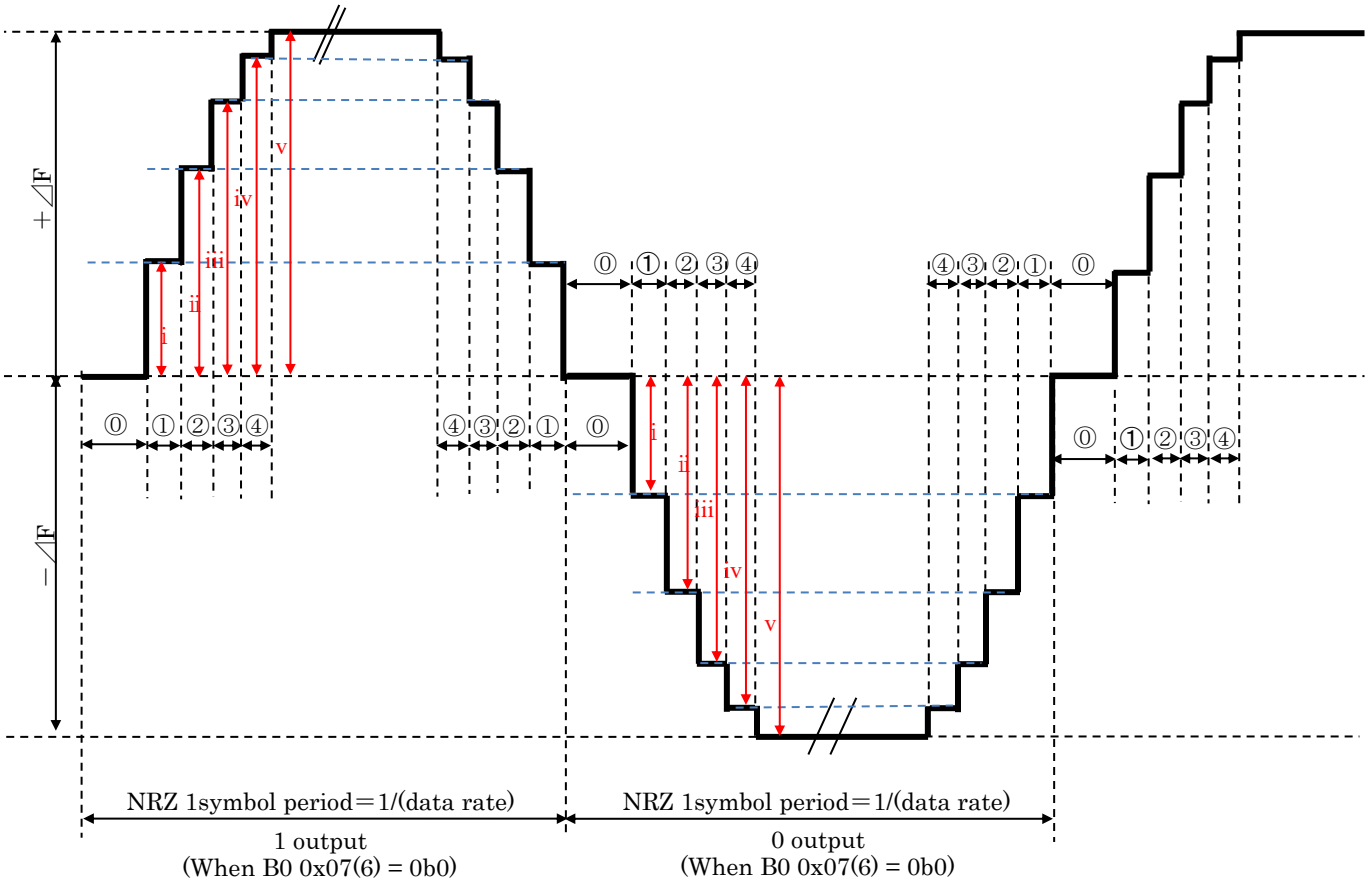
Refer to the following table to calculate the register value Nmax corresponding to the max frequency deviation time Tmax

Fref=48MHz

MSTR_CLK_SEL1 ([CLK_SET1: B0 0x02(4)])	FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)])	Time resolution (formula)	Time resolution [us] Tres	Data rate [kbps] R	Max frequency deviation time Tmax[us] =1/R/10	Max deviation timing setting (Nmax=Tmax/ Tres) [DEC]
0	0	1/(Fref/12)	0.25	100	1	4
0	0	1/(Fref/12)	0.25	100	1	4
0	1	1/(Fref/6)	0.13	100	1	8
0	1	1/(Fref/6)	0.13	100	1	8
1	0	1/(Fref/4)	0.08	100	1	12
1	0	1/(Fref/4)	0.08	100	1	12
1	1	1/(Fref/2)	0.04	100	1	24
1	1	1/(Fref/2)	0.04	100	1	24

[FSK_TIM_ ADJ4:B1 0x3C] - [FSK_TIM_ ADJ0:B1 0x40] is equally less than Max deviation timing setting Nmax. The value format is HEX.

[2FSK]


+⊿F
−⊿F
v
iv
iii
ii
i
⓪ ① ② ③ ④
④ ③ ② ① ⓪
NRZ 1symbol period＝1/(data rate)
1 output
(When B0 0x07(6) = 0b0)
NRZ 1symbol period＝1/(data rate)
0 output
(When B0 0x07(6) = 0b0)

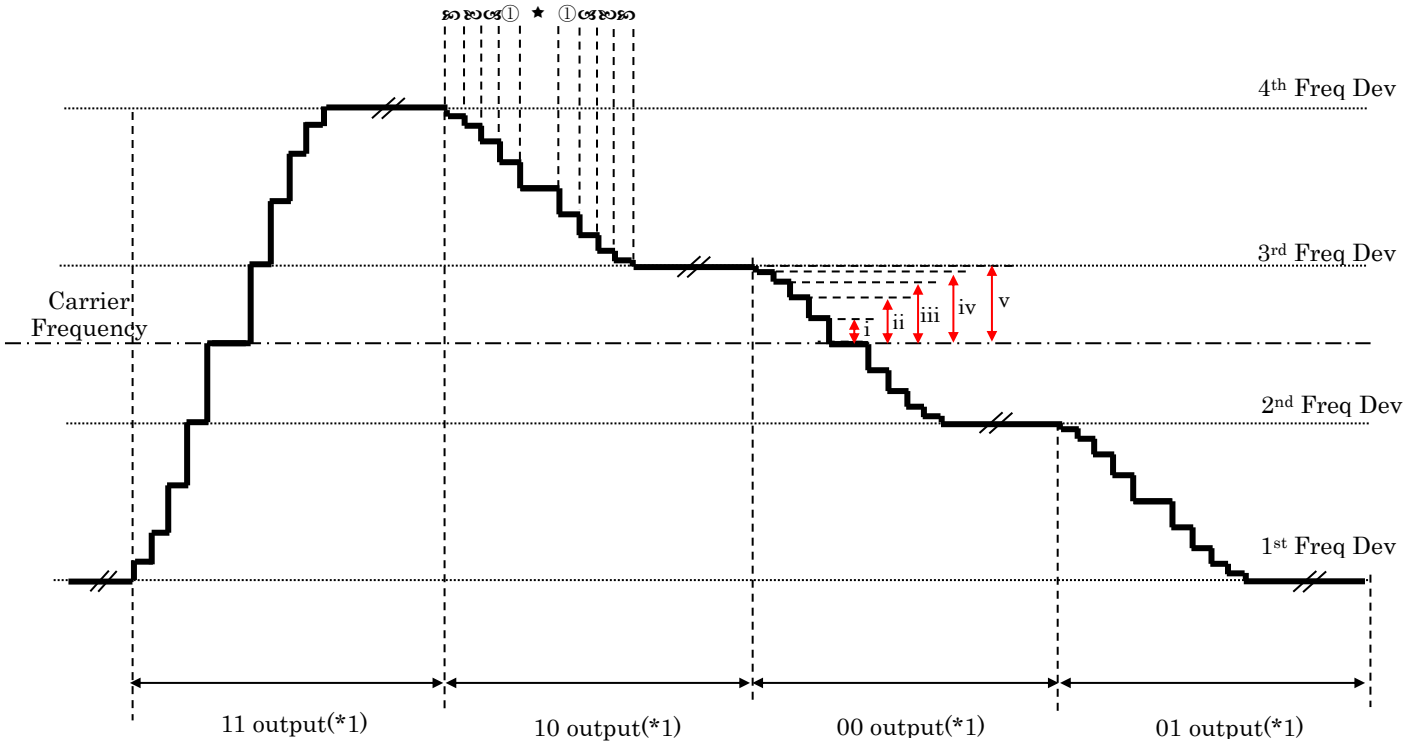
Frequency deviation setting				Time setting			
Symbol	Register name	Address	Function	Symbol	Register name	Address	Function
				⓪	FSK_TIM_ADJ0	B1 0x40	Center Frequency time (*1)
i	FSK_FDEV0_H/GFIL0 FSK_FDEV0_L/GFIL1	B1 0x32/33	1st Frequency deviation	①	FSK_TIM_ADJ1	B1 0x3F	1st Frequency time (*1)
ii	FSK_FDEV1_H/GFIL2 FSK_FDEV1_L/GFIL3	B1 0x34/35	2nd Frequency deviation	②	FSK_TIM_ADJ2	B1 0x3E	2nd Frequency time (*1)
iii	FSK_FDEV2_H/GFIL4 FSK_FDEV2_L/GFIL5	B1 0x36/37	3rd Frequency deviation	③	FSK_TIM_ADJ3	B1 0x3D	3rd Frequency time (*1)
iv	FSK_FDEV3_H/GFIL6 FSK_FDEV3_L	B1 0x38/39	4th Frequency deviation	④	FSK_TIM_ADJ4	B1 0x3C	4th Frequency time (*1)
v	FSK_FDEV4_H FSK_FDEV4_L	B1 0x3A/3B	Max Frequency deviation				

(*1) Modulation timing resolution is set by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)])

[Note]

GFSK filter coefficient setting registers and FSK frequency deviation setting registers are common. In GFSK mode, these registers set the filter coefficient. In FSK mode, these registers set frequency deviation.

[4FSK]



(*1) The mapping of the data (00/01/10/11) for each frequency deviation (1st to 4th) can be changed by [4FSK_DATA_MAP: B1 0x40].

(*2) If the frequency is changed by 2 levels such as from 1st to 3rd frequency deviation, the amount of the frequency change is 2 times as much as i to v. If the frequency is changed by 3 levels such as from 1st to 4th frequency deviation, the amount of the frequency change is 3 times as much as i to v.

The table below indicates the frequency deviation setting. The parameter of calculation formation is the register bit name.

Frequency deviation setting			
Symbol	Formula	Address	Function
i	FSK_FDEV4 - FSK_FDEV3	B1 0x3A/3B, B1 0x38/39	
ii	FSK_FDEV4 - FSK_FDEV2	B1 0x3A/3B, B1 0x36/37	
iii	FSK_FDEV4 - FSK_FDEV1	B1 0x3A/3B, B1 0x34/35	
iv	FSK_FDEV4 - FSK_FDEV0	B1 0x3A/3B, B1 0x32/33	
v	FSK_FDEV4	B1 0x3A/3B	Adjacent Symbol Frequency deviation x 1/2
v-i	FSK_FDEV3	B1 0x38/39	
v-ii	FSK_FDEV2	B1 0x36/37	
v-iii	FSK_FDEV1	B1 0x34/35	
v-iv	FSK_FDEV0	B1 0x32/33	

Time setting			
Symbol	Register name	Address	Function
④	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4MHz/12MHz counter value (*1)
③	FSK_TIM_ADJ3	B1 0x3D	
②	FSK_TIM_ADJ2	B1 0x3E	
①	FSK_TIM_ADJ1	B1 0x3F	
⓪	FSK_TIM_ADJ0	B1 0x40	

(*1) Modulation timing rsolution can be set by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)])

[Note]

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, this register set the filter coefficient. In FSK mode, this register set the frequency deviation.

6-11-8. Other Functions

6-11-8-1 ○Data Rate Setting Functions

(1) Data rate change setting

ML7436N supports various TX/RX data rate setting defined by the following registers.

TX ...[TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03]

RX ...[RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05], and [RX_RATE2: B1 0x06]

TX/RX data rate can be defined in the following formula.

[TX]

TX data rate [bps] = round (F_{REF}[Hz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)])) /
10 / [TX_RATE])

The following table shows the recommended value for each data rate. By setting TX_DRATE([DRATE_SET: B0 0x06(3-0)], following register setting values are automatically set to [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03].

F_{REF}=48 MHz

TX data rate [kbps]	[TX_RATE_H][TX_RATE_L] Setting value (decimal)	Data rate deviation [%] *1
1.2	2000	0.00
2.4	1000	0.00
4.8	500	0.00
9.6	250	0.00
10.0	240	0.00
15.0	160	0.00
19.2	125	0.00
20.0	120	0.00
32.768	73	0.06

40.0	60	0.00
50.0	48	0.00
100.0	24	0.00
200.0	12	0.00
300.0	8	0.00

*1 Data rate deviation assumes that the frequency deviation of FREF connected to ML7436N is 0 ppm.

If the data rate deviation becomes large by using the transmission data rate calculated by the formula above, the data rate deviation can be reduced by using [TX_RATE2_H: B1 0x7C] and [TX_RATE2_L: B1 0x7D].

TX_RATE2[13:0] = round [[{1/Data rate(bps)} –
{1 / (Clock frequency(Hz) / 2 / TX_RATE[11:0]) × 9}] /
{1 / Clock frequency(Hz) / 2}]

※Clock frequency = FREF[Hz] / (2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]))

[RX]

RX data rate [bps] = round ({FREF[Hz] /
(2-MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)])) / N} /
{[RX_RATE1] * [RX_RATE2])})
N=1(When LOW_RATE_EN=0)
N=2(When LOW_RATE_EN=1)

The following table shows the recommended value for each data rate (when LOW_RATE_EN([CLK_SET2: B0 0x03(0)])=0b1 is set). By setting RX_DRATE([DRATE_SET: B0 0x06(7-4)]), following register setting values are automatically set to [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05], and [RX_RATE2: B1 0x06].

FREF=48 MHz

RX data rate [kbps]	[RX_RATE1_H][RX_RATE1_L] Setting value (decimal)	[RX_RATE2] Setting value (decimal)
1.2	100	100
2.4	50	100
4.8	25	100
9.6	10	125
10.0	10	120
15.0	8	100
19.2	5	125
20.0	10	60
32.768	3	122
40.0	3	100
50.0	2	120
100.0	1	60
200.0	1	60
300.0	1	40

[Note]

1. When LOW_RATE_EN([CLK_SET2: B0 0x03(0)])=0b0 is set, the RX data rate should be calculated by the formula above. It should be noted that when LOW_RATE_EN=0b0 is set, even if TX/RX data

rate setting register ([DRATE_SET: B0 0x06]) is set, the optimum values are not set to [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05], and [RX_RATE2: B1 0x06] automatically.

(2) Other register settings associate with data rate change

When the data rate is changed, registers should be changed according to the Initialization table.

[Note]

1. Change data rate setting in TRX_OFF state.

6-11-8-2 ○Interrupt Generation Function

ML7436N support interrupt generation function. When interrupt occurs, interrupt notification signal (SINTN) becomes "L" to notify interrupt to the host MCU. Interrupt events are categorized into three groups: [INT_SOURCE_GRP1: B0 0x0D], [INT_SOURCE_GRP2: B0 0x0E], and [INT_SOURCE_GRP3: B0 0x0F]. Each interrupt event can be masked by [INT_EN_GRP1: B0 0x10], [INT_EN_GRP2: B0 0x11], and [INT_EN_GRP3: B0 0x12]. Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin. For output settings, refer to [GPIO1_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [GPIO4: B0 0x52], and [GPIO5: B1 0x6D] (GPIO4 and GPIO5 are available for ML7436 only).

[Note]
If any single unmasked interrupt event occurs, SINTN maintains Low.

(1) Interrupt Event Table

Each interrupt event is described below table.

Register	Interrupt name	Function
INT_SOURCE_GRP1	INT[0]	Clock stabilization completion interrupt
	INT[1]	VCO calibration completion interrupt or Fuse access completion interrupt or IQ adjustment completion interrupt
	INT[2]	PLL unlock interrupt
	INT[3]	RF state transition completion interrupt
	INT[4]	FIFO-Empty interrupt
	INT[5]	FIFO-Full interrupt
	INT[6]	Wake-up interrupt
	INT[7]	Clock calibration completion interrupt or Channel serch error interrupt
INT_SOURCE_GRP2	INT[8]	RX completion interrupt
	INT[9]	RX completion interrupt
	INT[10]	Diversity search completion interrupt
	INT[11]	RX Length error interrupt
	INT[12]	RX FIFO access error interrupt

	INT[13]	SyncWord detection interrupt
	INT[14]	Field checking interrupt
	INT[15]	Sync error interrupt
INT_SOURCE_GRP3	INT[16]	TX completion interrupt
	INT[17]	TX Data request accept completion interrupt
	INT[18]	CCA completion interrupt
	INT[19]	TX Length error interrupt
	INT[20]	TX FIFO access error interrupt
	INT[21]	Reserved
	INT[22]	General purpose timer 1 interrupt
	INT[23]	General purpose timer 2 interrupt

(2) Interrupt Generation Timing

In each interrupt generation, timing from reference point to interrupt generation (notification) is described in the following table. Timeout procedure for interrupt notification waiting is also described below.

[Note]
(1) The following table shows values at 100 kbps. For any symbol rate, replace the value described as symbol time with the symbol period in the following table.
(2) The following table uses the following format for TX/RX data.

10 bytes	2 bytes	1 byte	24 bytes	2 bytes
Preamble	SyncWord	Length	User data	CRC

(3) Even when an interrupt notification is set to OFF, ML7436N internally holds the interrupt. When the interrupt notification setting is then changed from OFF to ON without clearing the interrupt, it will be notified. When the interrupt occurs, it is recommended that interrupt should be cleared after turning off the

Interrupt notification		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	RESETN release (upon power-up)	1 to 1.25 ms
		Exit from SLEEP (recovered from SLEEP)	1 to 1.25 ms
INT[1]	VCO calibration completion	VCO calibration start	approx 6 ms
	IQ automatic adjustment completion	IQ adjustment execution start	Max: approx. 100 ms
	FUSE access completion	After RESETN release	Clock stabilization completion interrupt
INT[2]	PLL unlock detection	-	(TX) during TX after PA_ON (RX) during RX after RX enable.
INT[3]	RF state transition completion	TX_ON command	(IDLE) 232μs(VCO auto calibration) 160μs(VCO on-demand calibration) (RX) 219μs(VCO auto calibration) 72μs(VCO on-demand calibration)

Interrupt notification		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
		RX_ON command	(IDLE) 203μs(VCO auto calibration) 121μs(VCO on-demand calibration) (TX) 220μs(VCO auto calibration) 75μs(VCO on-demand calibration)
		TRX_OFF command	(TX) Ramp-down time+6μs (RX) 5μs
		Force_TRX_OFF command	(TX) Ramp-down time+6μs (RX) 5μs
INT[4]	FIFO-EMPTY	TX_ON command (TX) (*1)	Empty trigger level is set to 0x02. (NRZ encoding) RF wake-up (210 μs)+(preamble to 22nd Data byte)x10(bit time) = 3010 μs)
		-(RX)	By FIFO read, FIFO usage is under trigger level
INT[5]	FIFO-FULL	-(TX)	By FIFO write, FIFO usage exceed trigger level
		SyncWord detection (RX)	Full trigger level is set to 0x05. (NRZ encoding) 500 μs (5 bytes data x 10 μs(bit time))
INT[6]	Wake-up completion	RF_SLEEP setting	When Wake-up timer occurs Refer to the chapter [Wake-up timer]
INT[7]	Clock calibration completion	Calibration start	When Calibration timer occurs Refer to the Chapter [Low speed clock adjustment function]
	Channel search completion	-	When channel search error occurs
INT[8]	Data reception completion	SyncWord detection	When the length of L-field is 1 byte, and NRZ encoding is used, after 2160 μs (L-field length (8 bit)x10(symbol time)=80 μs, data length ((Data to CRC: bit)x10(symbol time)=2080 μs))

Interrupt notification		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[9]	CRC error	SyncWord detection	(Format A/B) each RX CRC block calculation completion (Format C/D) RX completion
INT[10]	Diversity search completion	-	SyncWord detection during diversity enable setting
INT[11]	RX Length error	SyncWord detection	80 μs(L-field 1 byte) 160 μs(L-field 2 byte)
INT[12]	RX FIFO access error interrupt	-	(1) Overflow occurs because FIFO read is too slow. (2) Underflow occurs because too many FIFO data is read
INT[13]	SyncWord detection	-	SyncWord detection
SyncWord detection	-	SyncWord detection	SyncWord detection
Field check	-	Match or mismatch detected in Field check	Field check
INT[16]	Data transmission completion	TX_ON command (*1)	RF wake-up+[TX data+3](bit) =210 μs+315 bits x 10 μs (bit time)=3360 μs
INT[17]	TX Data request accept completion	-	After full length data is written to the TX_FIFO. (It is considered as transmitting when using FIFO trigger to write additional data in FAST_TX mode)
INT[18]	CCA completion	CCA execution start	(1) Normal mode (ED value average times + IDLE_WAIT setting) x Average interval + Gain switching time (2) IDLE detection mode ○IDLE detection (ED value average times + IDLE_WAIT setting) x Average interval + Gain switching time

Interrupt notification		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
			○BUSY detection ED value average times x Average interval + Gain switching time Average interval is 16 μs.
INT[19]	TX Length error	-	When setting Length for [TX_PKT_LEN_H/L: B0 0x7A/0x7B]
INT[20]	TX FIFO access error	-	(1) When data was written when there was no free space on FIFO (2) When additional data was written to FIFO, overflow occurred (3) When there was no more data to transmit during transmission
INT[21]	Reserved	-	-
INT[22]	General purpose timer 1	Timer start	General purpose timer 1 completion General purpose timer clock cycle * Divider ratio setting [GT_CLK_SET: B0 0x33] * After general purpose timer interval setting ([GT1_TIMER: B0 0x34])
INT[23]	General purpose timer 2	Timer start	General purpose timer 2 completion General purpose timer clock cycle * Divider ratio setting [GT_CLK_SET: B0 0x33] * B0 0x33]) * After general purpose timer interval setting ([GT2_TIMER: B0 0x35])

(*1) Before issuing TX_ON, writing full-length TX data to the TX_FIFO.

(2) Clearing Interrupt Condition

Interrupt notification		Recommended clearing timing of interrupts
INT[0]	CLK stabilization completion	
INT[1]	VCO calibration completion or Fuse access completion or IQ adjustment completion interruption	
INT[2]	PLL unlock detection	
INT[3]	RF state transition completion	
INT[4]	FIFO-EMPTY	Clear before the next EMPTY trigger generation timing
INT[5]	FIFO-FULL	Clear before the next FULL trigger generation timing
INT[6]	Wake-up completion	
INT[7]	Clock calibration or Channel search error	
INT[8]	Data reception completion	Clear before the next packet reception
INT[9]	CRC error	Clear before the next packet reception
INT[10]	Diversity search completion	After interrupt generated
INT[11]	RX Length error	
INT[12]	RX FIFO access error	Clear before the next packet reception
INT[13]	SyncWord detection	
INT[14]	Field check	
INT[15]	Sync error	
INT[16/]	Data transmission completion	Clear before the next packet transmission
INT[17]	TX Data request accept completion	Clear before the next packet reception
INT[18]	CCA completion	Clear before the next CCA execution * Clearing interrupt erases CCA result as well.
INT[19]	TX Length error	
INT[20]	TX FIFO access error	Clear before the next packet transmission
INT[21]	Reserved	
INT[22]	General purpose timer 1	
INT[23]	General purpose timer 2	

6-11-8-3 ○Low speed clock adjustment function

ML7436N equips the function to detect Low speed clock frequency misalignment. It adjusts Wake-up timer clock (External, Internal RC circuit output) frequency. The following table registers set the Low speed frequency misalignment function. Wake-up timer period setting registers ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) and Continue operation timer register ([WU_DURATION: B0 0x31]) control the accurate timer operation that take Wake-up timer clock frequency misalignment into account. This chapter mentions the method to adjust Wake-up timer period to set Wake-up timer period setting registers ([WUT_INTERVAL_H/L: B0 0x2F/0x30]). Refer to [Wake-up timer] about Continuous operation timer register ([WU_DURATION: B0 0x31]).

Setting	Register
Clock division setting for frequency misalignment detection	[CLK_CAL_SET: B0 0x70]
Calibration time	[CLK_CAL_TIME: B0 0x71]
Counter display of high speed clock	[CLK_CAL_H: B0 0x72]および[CLK_CAL_L: B0 0x73]

This function counts the Wake-up timer low clock frequency period by the internal high accuracy, high speed clock and displays the counter result in the [CLK_CAL_H/L: B0 0x72/0x73] register. The relationship between register setting and the number of counter is as following.

The number of counter by high speed clock = {Wake-up timer clock frequency ([SLEEP/WU_SET:B0 0x2D(2)]) *
Calibration time setting ([CLK_CAL_TIME:B0 0x71(5-0)])} /
{Reference clock frequency *
(MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)])+1) *
Clock division setting for detection([CLK_CAL_SET: B0 0x70(7-4)])}

Calibration time is calculated as the following formula.

Calibration time [sec] = Wake-up timer clock frequency * Calibration time setting

(Wake-up timer adjustment example)
Internal high speed clock divisi on setting: disable, Calibration time:10cycle, Wake-up timer setting=1000(0x3E8)

Condition: wake-up timer clock frequency = 32.768kHz
Clock division setting for detection CLK_CAL_DIV[3:0] ([CLK_CAL_SET: B0 0x70(7-4)]) = 0b0000
Carlibration time setting [CLK_CAL_TIME] = 0x0A
Wake-up timer setting [WUT_INTERVAL:B0 0x2F,30] = 0x03E8(1000)
Reference clock frequency = 48MHz
MSTR_CLK_SEL1([CLK_SET2: B0 0x02(5)]) = 1

The ideal number of counter by high speed clock is the following,

Number of counter by high speed clock = (1/32.768kHz) * 10 / (1/{48MHz/2})
= 7324(0x1C9C)

If [CLK_CAL_H/L:B0 0x72,73] register indicate 0x1BB5(7093),

Counter misaligment value = 7093 – 7324 = -231
Frequency misaligment =1/[{1/32.768kHz + (- 231) / 10 * 1/24MHz}]- 32.768kHz = 1067.13Hz

It represens low speed clock frequency error = +3.26%. The result calculates the correction value (C) of wake-up timer counter.

C= Wake-up timer setting value（[WU_INTERVAL_H/L:B0 0x2F,30]）* Frequency misaligment / 32.768kHz
= 1000 * 1067.13Hz / 32.768kHz
= 37

In this case, Wake-up timer setting value(＝1000 + 37 = 1037 = 0x040D) is the best value to set 32.768kHz frequency.

[Note]

When calibration time is short, clock division setting value is large and low resolution of high clock counter, the calibration accuracy is low.

6-11-8-4 ○Low battery detection function

ML7436N equips voltage detection function for 3V system voltage (VDD_BIAS). The following register settings set the voltage detection function.

Setting	Register
Low battery detection enable	LOWBAT_DET_EN([LOWBAT_DET_CTRL1: B3 0x44(4)])
Battery value indication	[LOWBAT_DET_DISP: B3 0x44/45]

After low battery detection enable is set, the function compares 3V system voltage (VDD_BIAS) and the threshould voltage generated by LDO_XO voltage. If the threshould voltage is more than 1/3 of 3V system voltage (VDD_BIAS), The voltage value is indicated on Battery value indication register ([LOWBAT_DET_DISP: B3 0x44/45]). The relationship betwenn 3V system voltage and Battery indication value is represented by the following formula.

Estimated 3V system voltage [V] = LDO_XO pin voltage(Typ. 1.4V) * Battery indication value / 511 * 3 - 0.1

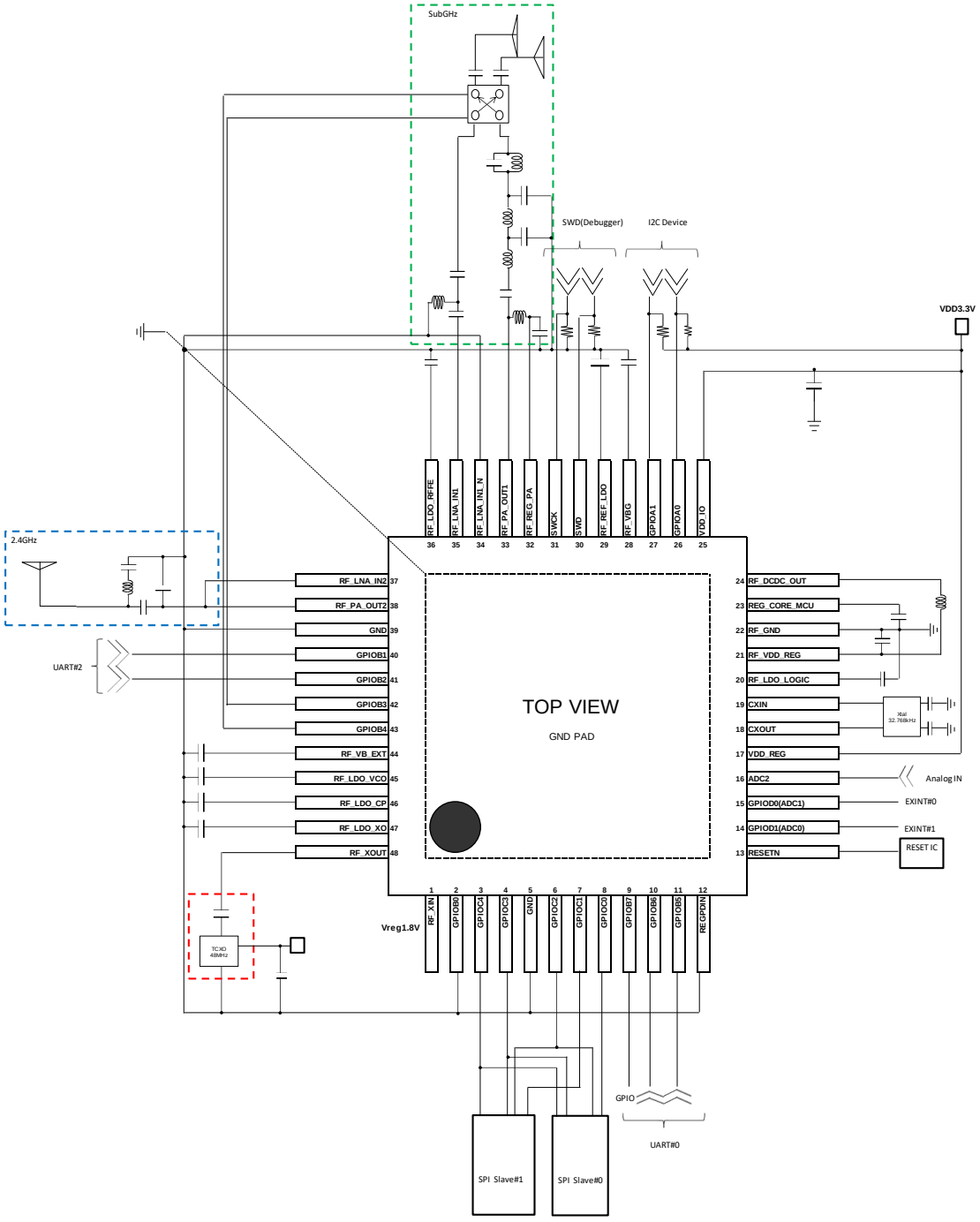
(Example) When Batery indication = 410(0x19A), the estimated 3V system voltage is following,
Estimated 3V system voltage = 1.4V(LDO_XO pin voltage) * 410 / 511 * 3 - 0.1 = 3.27 [V]

[Note]

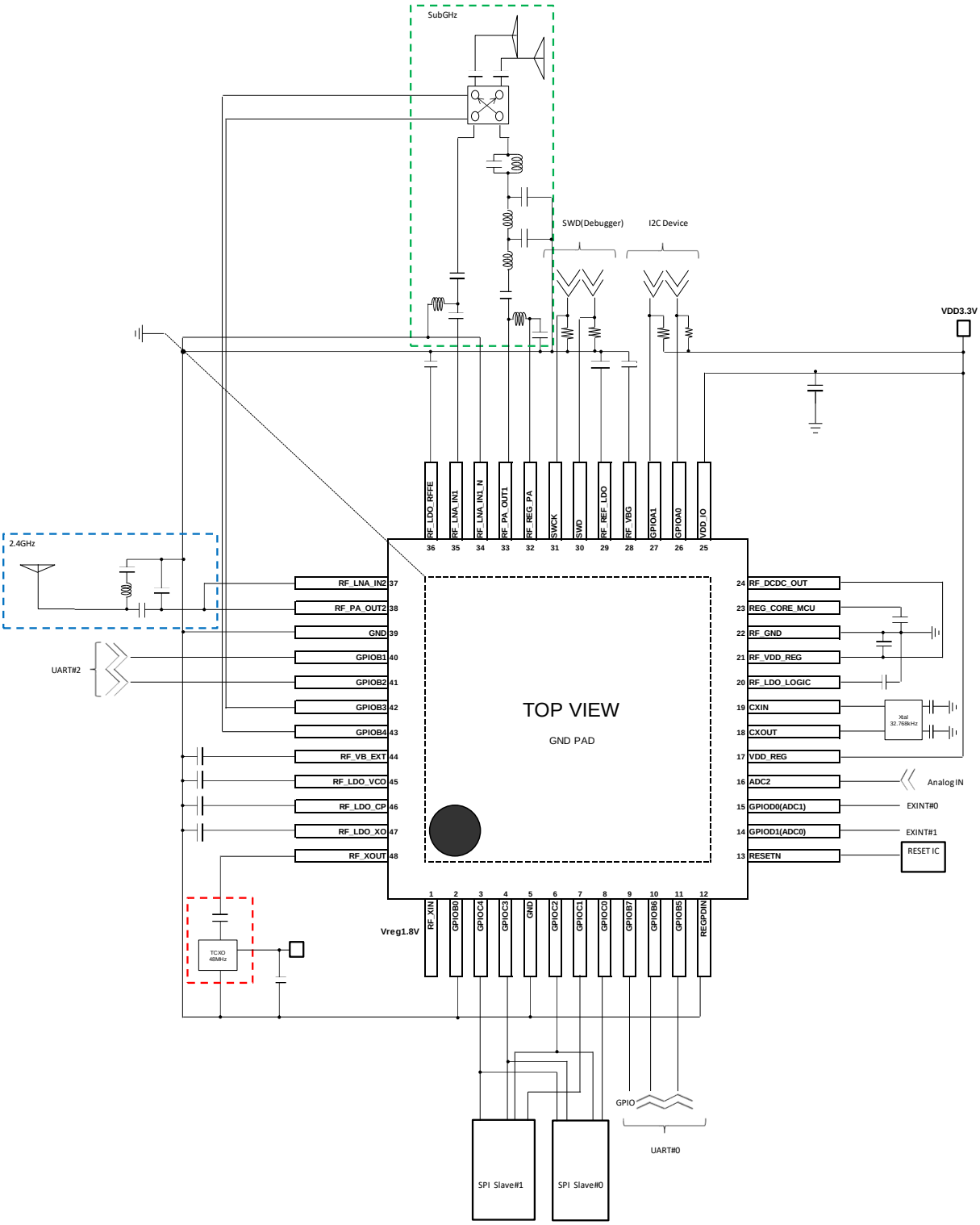
1. Execute low battery detection with IDLE or RX state.
2. If the result of comparison of low battery detection between 3V system voltage (VDD_BIAS) and the threshould voltage generated by LDO_XO voltage is less than 1/3 of V system voltage (VDD_BIAS), Battery indication value indicates 0x000.
3. The misaligment of LDO_XO pin voltage(1.4V) affects the 3V system voltage.
4. The calculation example aboveis the result when F_{REF}=48MHz.

■7. Examples of Application Circuit

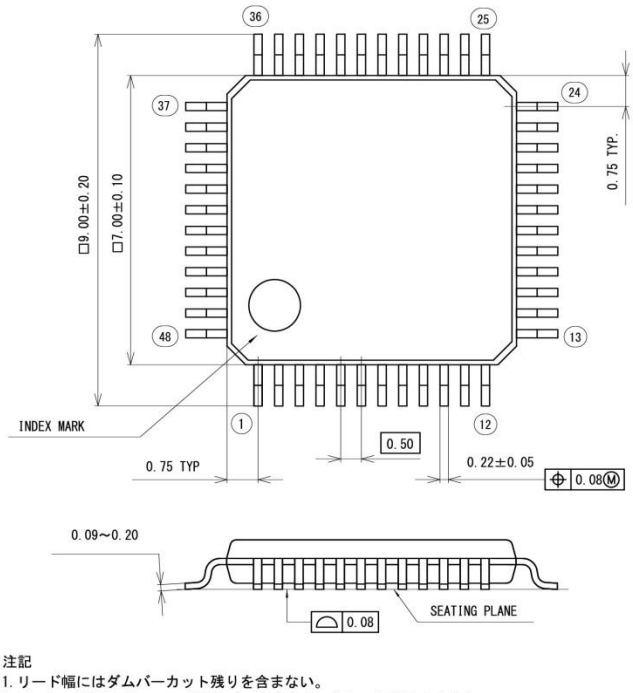
Using DCDC Converter

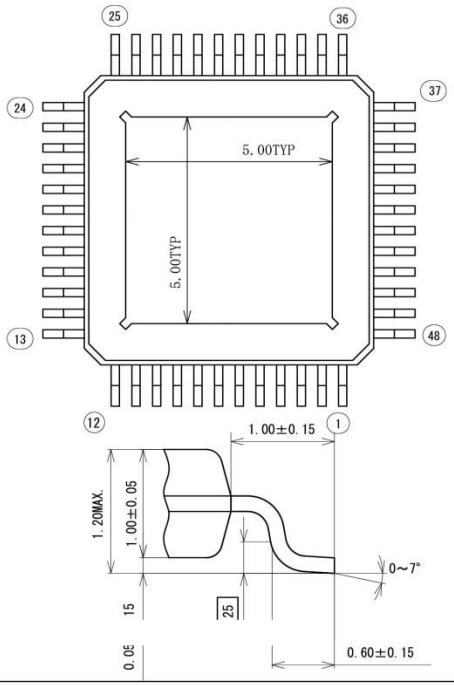


No using DCDC Converter



■8. Package Dimensions/Footprint Pattern





注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-Z9K6-MC		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69545
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jun/03/2020
PACKAGE MASS (g)	0.13TYP	REVISED	Nov/01/2020

■9. Revision History

Rev.	Changes	Date
01	Initial release	Dec. 29, 2020
03	Error fix(3/4/7)	Mar,15, 2021
	Add GND pin(4-1)	
04	Change max value(ACP) for reconsideration of the specidfication(5-4-1)	June,29, 2021
05	Add Product Name,application	Nov.1,2023
	The description of [Note] has been updated.	
06	The description of [Note] has been updated.	Jan,10, 2024

Notes

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