Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL7456N-05
Issue Date : Jan. 10, 2024

ML7456N

Sigfox Sub-GHz Microcontroller

■Overview

ML7456N is a Sigfox Sub-GHz Microcontroller, which integrates MCU and RF Transceiver in a single chip.

RF frequency corresponds to 315MHz - 920MHz. It applis to Sigfox, it is low consumption and implements long-range wireless communication.

MCU equips with an 16-bit CPU nX-U16/100(A35 core) and integrated with program memory(Flash memory), data memory(RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC generator, DMA controller, Clock generator, Simplified RTC, Timer, General Purpose Ports, UART, Synchronous serial port, I^2C bus interface unit(Master, Slave), Buzzer, Voltage Level Supervisor(VLS), Successive approximation type A/D converter, D/A converter , Analog comparator, Safety function(IEC60730/60335 Class B), and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP(In-System Programming) function supports the Flash programming in production line.

●Product Name　ML7456N-700AGD

●Application
Remote control
Home, Building Security
Sensor Network
Smart Meters
Logistics Tracking
Infrastructure Monitoring
Monitoring system

■Features

- Sigfox / IEEE802.15.4g , Sigfox RF chip (ML7414)(*1)
  - Supported standard
    - ✧ Sigfox Revision 2.E
    - ✧ ETSI EN 300 220(Europe)
    - ✧ EN 13757-4:2013(Wireless M-Bus)
    - ✧ RCR STD-30(III and IV types)
    - ✧ ARIB STD-T67
    - ✧ ARIB STD-T108
  - RF frequency: 315MHz - 960MHz supported
  - Realized high resolution modulation by using fractional N type PLL direct modulation
  - Modulation formats: BPSK (TX only), 4GFSK/4GMSK, GFSK/GMSK, FSK/MSK (MSK indicates FSK at modulation index = 0.5.)
  - Data transmission rate: 0.1 to 100 kbps
  - Data encoding/decoding by HW: NRZ, Manchester, 3 out of 6
  - Data whitening by HW
  - Programmable frequency channel filters
  - Programmable frequency deviation function
  - TX/RX data inverse function
  - 36MHz oscillator circuits/TCXO (36MHz) direct input supported
  - Programmable oscillator's circuit pins load capacitance
  - Super-power-saving low speed RC oscillator circuit
  - Low speed clock adjustment function
  - Frequency fine tuning function (using fractional N type PLL)
  - Synchronous serial peripheral interface(SPI)
  - On-chip TX PAPower control function
  - TX power fine tuning function (±0.2 dB)
  - TX power automatic ramping control
  - External TX PA control function
  - RSSI indicator and threshold judgment function
  - High speed carrier checking function
  - AFC function (IF frequency automatic adjustment by Fractional N type PLL adjustment)
  - Antenna diversity function
  - Automatic wake-up, auto SLEEP function (32kHz clock direct inputor internal RC oscillator circuit selectable)
  - General purpose timer (2ch)
  - TEST PATTERN GENERATOR (PN9 ,CW, 01 PATTERN, ALL"1", ALL"0" OUTPUT)
  - Packet mode function
    - ✧ Wireless M-BUS packet format (Format A/B)
    - ✧ General purpose packet format (Format C/D)
    - ✧ Max. 255-byte (Format A/B), 2047-byte (Format C/D) packet length
    - ✧ TX FIFO (64 byte), RX FIFO (64 byte)
    - ✧ RX Preamble pattern detection (Max.4 byte)
    - ✧ Automatic TX preamble length generation (Max.length 16383 byte)
    - ✧ SyncWord setting function (Max. 4byte × 2 type)
    - ✧ Program CRC function (CRC32/CRC16/CRC8 selectable, fully programmable polynomial)
    - ✧ Address check function (C-field/M-field/A-field in Wireless M-Bus can be detected)
      * Proprietary packet format is possible depending on setting
    - ✧ FEC function (IEEE802.15.4g compliant)

*Please refer to "ML7414 Application Note Hardware details" about RF part in detail.

◆ MCU 16 bit CPU nX-U16/100 A35 core chip(ML62Q1532)

- CPU
  - 16-bit RISC CPU: nX-U16/100 (A35 core)
  - Instruction system: 16-bit length instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function
  - Built-in ISP (In-System Programming) function
  - Minimum instruction execution time
    Approximately 30.5 μs (at 32.768 kHz system clock)
    Approximately 62.5ns/41.6ns (at 16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Multiplication : 16bit × 16bit (operation time : 4 cycles)
  - Division : 32bit ÷ 16bit (operation time : 8 cycles)
  - Division : 32bit ÷ 32bit (operation time : 16 cycles)
  - Multiply-accumulate (non-saturating) : 16bit × 16bit + 32bit (operation time : 4 cycles)
  - Multiply-accumulate (saturating) : 16bit × 16bit + 32bit (operation time : 4 cycles)
  - Signed or Unsigned is selectable

- Internal memory
  - Program memory area 64Kbyte
  - Rewrite count: 100 cycles
  - Write unit: 32bit (4byte)
  - Erase unit: 16Kbyte/1Kbyte
  - Erase/Write temperature: 0 °C to +40 °C
  - Data Flash memory area 4Kbyte
    Rewrite count 10,000 cycles
    Write unit: 8bit (1byte)
    Erase unit: all area/128byte
    Erase/Write temperature: -40 °C to +85 °C
    Back Ground Operation (CPU can work while erasing and rewriting)

    This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
  - Data RAM area 8Kbyte
    Rewrite unit: 8bit/16bit
    Parity check function is available (interrupt / reset is generatable at Parity error)

- Clock Generation Circuit
  - Low-speed clock (LSCLK)
    Internal low-speed RC oscillation: Approximately 32.768 kHz
    External low-speed clock input (ML62Q1500/ML62Q1800 and ML62Q1700 group only)
    : Approximately 32.768 kHz
    External low-speed crystal oscillation (ML62Q1500/ML62Q1800 and ML62Q1700 group only)
    : 32.768 kHz crystal resonator is connectable.
    3 selectable crystal oscillation mode (Tough, Normal, and Low current consumption)
    -Tough mode: Largest oscillation allowance to make highest resistance against leakage between the pins
    -Normal mode: Normal oscillation allowance and current consumption
    -Low current consumption mode: Smallest oscillation allowance to make lower current consumption
  - High-speed clock (HSCLK)
    PLL oscillation: 2 selectable oscillation frequency (24MHz and 16MHz) by code option
  - Watch Dog Timer (WDT): built-in independent clock for WDT (RC1K: Approximately 1kHz)

- Reset
  - Reset by reset input pin
  - Reset by Power-On Reset
  - Reset by WDT overflow
  - Reset by WDT invalid clear
  - Reset by RAM parity error
  - Reset by unused ROM area access (instruction access)
  - Reset by voltage level supervisor (VLS)
  - Software reset by BRK instruction (reset CPU only)
  - Reset the peripherals individually
  - Collective reset to the all control pins and peripheral circuits.

- Power management
  - HALT mode: CPU stops executing instruction, peripheral circuits continue working
  - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits continue working with low-speed clock
  - STOP mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stops.
  - STOP-D mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stops. The internal logic voltage (V_{DDL}) goes down to reduce the current consumption (RAM data is retained).
  - Clock gear: High-speed system clock frequency can be changed (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of HSCLK)
  - Block Control Function: Powers down the unused function blocks (reset the block or stop supplying the clock)

- Interrupt controller
  - External interrupt ports : max. 6
  - Non-maskable interrupt source: 1 (Internal source: WDT)
  - Maskable interrupt sources: max. 51
  - Four step interrupt levels

- Watchdog timer (WDT)
  - Selectable Operating clock : select RC1K or LSCLK by code option
  - Overflow period: 8selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2s and 8s)
  - Selectable window function (enable or disable): configurable clear enable period (50% or 75% of overflow period)
  - Selectable WDT operation : select Enable or Disable by code option
  - Readable WDT counter : WDT counter monitor function

- DMA (Direct Memory Access) controller
  - Channel : 2channels
  - Transfer unit: 8bit/16bit
  - Transfer count: 1 to 1024
  - Transfer cycle: 2 cycle transfer
  - Transfer address: Fixed addressing mode, inclement addressing mode , and decrement addressing mode
  - Transfer target: Special Function Register (SFR)/RAM → SFR/RAM (Transfer from/to Flash is not supported)
  - Transfer request: External pins, Serial communication unit, Successive approximation type A/D converter, 16bit timer, and Functional timer

- Low-speed Time base counter
  - Generate 8 frequency (128Hz to1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
  - Selectable 3 interrupts from eight frequency internal pulse signals
  - 1Hz or 2Hz output from general purpose port
  - Built-in Frequency adjust function (Adjust range: Approximately -488ppm to +488ppm, adjust resolution: Approximately 0.119ppm)

- Simplified RTC
  - Channel: 1 channel
  - Count by a unit for one second from "00 min. 00 sec" to "59 min. 59 sec"
  - Selectable Periodical interrupt request from four periods (0.5s, 1s, 30s or 60s)
  - Built-in minute and second writing error protraction function

- Functional timer
  - Channel: Max. 6 channels (output 4 channels)
  - Built-in timer, capture, and PWM function by 16 bit counter
  - Continuous mode, One shot mode is available
  - Two types of PWM output with the same period and different duties, and complementary PWM output with the dead time
  - Monitor input signal duty and the period by capture function
  - Generate periodical interrupts, duty interrupts, and interrupts coincided with set value.
  - Counter Start, Stop, Counter clear triggered by an external inputs or Timer
  - Generate Emergency stop and emergency stop interrupt triggered by an external input
  - Same start/stop among different channels of the functional timer
  - Selectable counter clock(external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channels

- 16bit General timers
  - Channel: Max. 6 channels (output 2 channels)
  - 8 bits timer mode and 16-bit timer mode
    (16bit x 1channel can be used as 8bit x 2channels)
  - Same start/stop among different channels of 16bit (8bit) timer
  - Timer output (toggled by overflow)
  - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channels

- Serial communication unit
  - Synchronous Serial Port (SSIO) mode or UART mode is selectable
  - Channel: Max. 2 channels

  < Synchronous Serial Port mode >
  - Selectable from Master and Slave
  - Selectable from LSB first or MSB first
  - Selectable 8-bit length or 16-bit length

  < UART mode>
  - Selectable from Full-duplex communication mode or Half-duplex communication mode
  - 5 to 8 bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits
  - Selectable from Positive logic or Negative logic
  - Selectable from LSB first or MSB first
  - Configurable wide range communication speed
    32.768kHz operation clock : 1 bit/s to 4,800 bit/s
    24MHz operation clock : 600 bit/s to 3M bit/s
    16MHz operation clock : 300 bit/s to 2M bit/s
  - Built-in baud rate generator

- I^2C bus unit (Master / Slave)
  - Selectable from Master mode or Slave mode
  - Channel: 1 channel

  < Master function >
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

  < Slave function >

- Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
- Clock stretch function
- 7bit address format

- I^2C bus Master
  - Channel: 1 channel
  - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

- General-purpose ports (GPIO)
  - I/O port: Max. 15 (Including one pin for on-chip debug and pins for other shared functions)
  - Input port: Max. 2 (Including a shared function)
  - External interrupt port: Max. 6
  - LED driver port : Max. 12
  - Carrier frequency output function (for IR communication)

- Successive approximation type A/D converter(SA-ADC)
  - Channel: Max. 5 channels
  - Resolution: 10bit
  - Conversion time: Min. 2.25μs/channel (When the conversion clock speed is 8MHz)
  - Reference voltages are selectable
    (V_{DD} pin / Internal reference voltage(V_{REFI} = Approximately 1.55V) / External reference voltage (V_{REF} pin))
  - Selected channel repeat conversion
  - Dedicated result register for each channel
  - Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage Level Supervisor (VLS)
  - Accuracy: ±4%
  - Threshold voltage: 12 selectable (from 1.85V to 4.00V)
  - Functional Voltage level detection reset (VLS reset)
  - Functional Voltage level detection interrupt (VLS0 interrupt)

- Analog comparator
  - Channel: Max. 2 channels
  - Selectable interrupt from the comparator output (rising edge or falling edge)
  - Comparable with external input and internal reference voltage (0.8V)

- D/A converter
  - Channel: Max. 1 channel
  - Resolution: 8bit
  - Output impedance: 6k ohm (Typ.)
  - R-2R ladder type

- Buzzer
  - 4 buzzer mode (Continuous sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
  - frequencies (4.096kHz to 293Hz)
  - 15 step duty (1/16 to 15/16)
  - Selectable from positive logic buzzer output or negative logic buzzer output

- CRC(Cyclic Redundancy Check) generator
  - Generation equation: $X^{16}+X^{12}+X^5+1$
  - Selectable from LSB first or MSB first
  - Built-in Automatic program memory CRC calculation mode in HALT mode

- Safety Function (IEC60730/60335 Class B)
  - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
  - RAM/SFR guard
  - Automatic program memory CRC calculation
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - Clock mutual monitoring
  - WDT counter monitoring
  - SA-ADC test
  - UART test
  - Synchronous serial I/O test
  - I^2C bus test
  - GPIO test

◆ Operating Voltage 2.6V to 3.6V

◆ Operating temperature -40℃ to 85℃ (Guaranteed Operation)
-30℃ to 75℃ (Guaranteed RF characteristics)

◆ Current consumption

Sleep mode		3.45uA (RF=IDD_SLP1/MCU=IDD2-2)
TX	20mW	44.7mA (RF=IDD_TX20/MCU=IDD5)
RX		18.2mA (RF=IDD_RX/MCU=IDD5)

◆ Package
48 pin WQFN
Lead free, RoHS Compliant

(*1)Supported Standard and frequency differs from products
ML7456N-700AGDZ0ANL Sigfox(RC3), ARIB STD-T108

■Related Documents

Please refer to “ML7414 Application Note Hardware details” about RF part in details.

Please refer to “ML62Q1000 Series User’s Manual” about MCU part of ML61Q1532 in details. ML7456N uses a part of pins of ML62Q1532. Prioritize this document information about the pin explanation, the number of equipped functions which relates to the number of pins.
Replace pin names between this document and “ML62Q1000 User’s Manual” as following the table.

This document	ML62Q1000 Series User’s Manual
VDDIO_MCU	VDD
REG_CORE_MCU	VDDL

■Description Convention

1) Numbers description
'0xnn' indicates hexadecimal. '0bnn' indicates binary.
Example: 0x11= 17(decimal), 0b11= 3(decimal)

2) Registers description
Registers are described as follows.
[<register name>: B<Bank No> <register address>] register

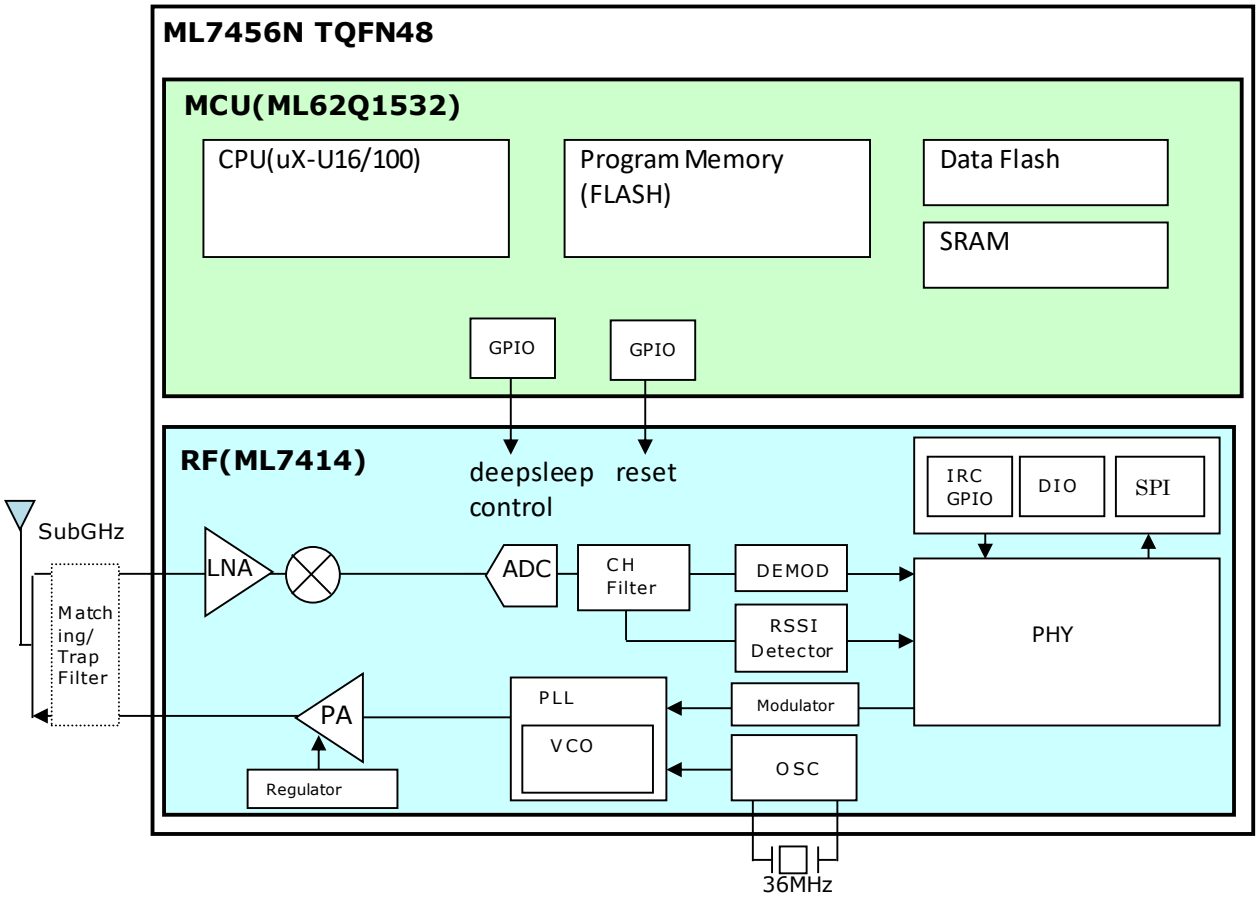
Example: [RF_STATUS: B0 0x0B(3-0)]
Register name: RF_STATUS
Bank No: 0
Register address: 0x0B

3) Bit name description
Bit names are described as follows.
<bit name> ([<register name>: B<Bank No> <register address>(<bit location>)])

Example: SET_TRX([RF_STATUS: B0 0x0B(3-0)])
Register name: RF_STATUS
Bank No: 0
Register address: 0x0B
Bit: Bit3 to bit0

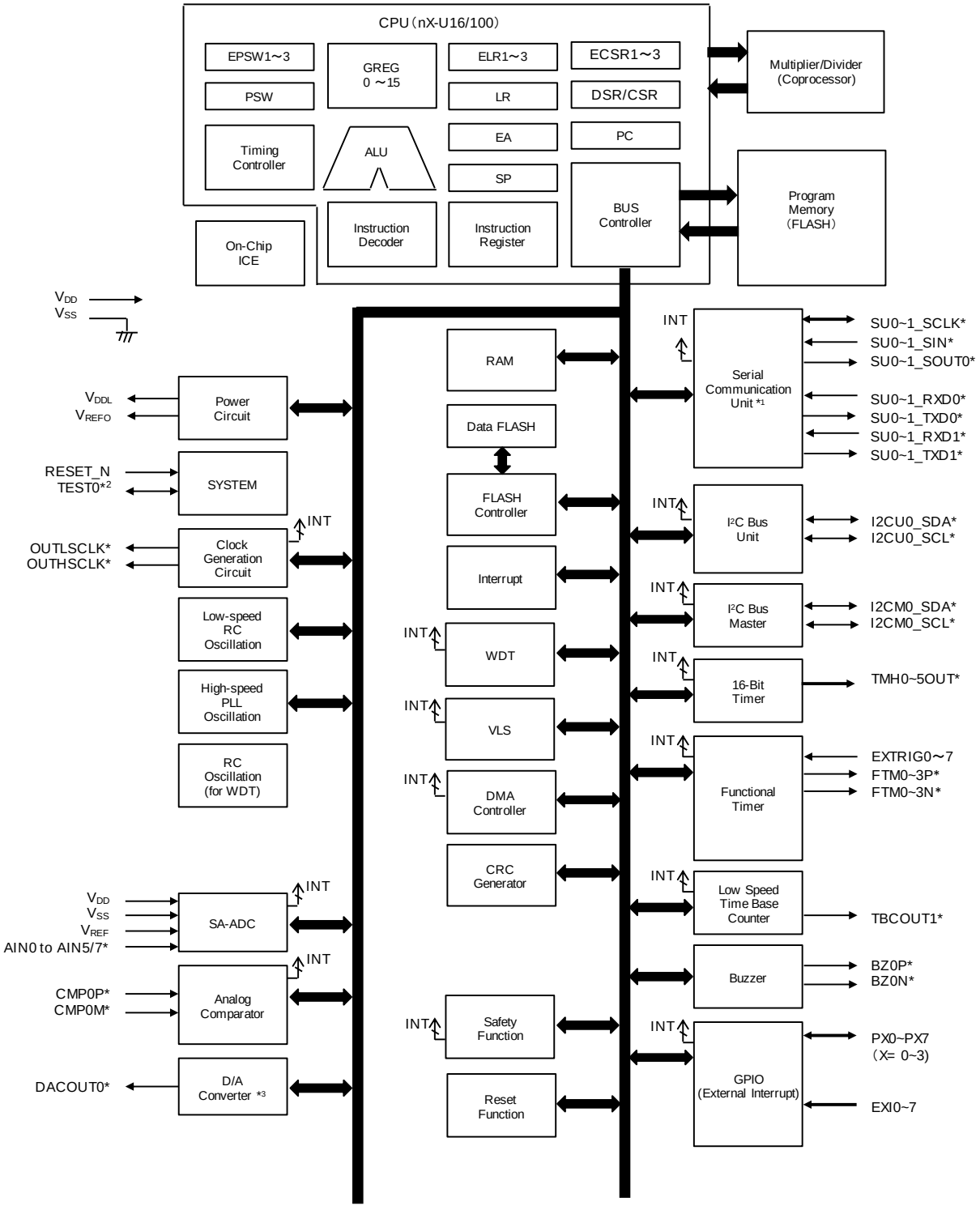
■Block Diagram

●Whole/RF part



●MCU part

Block diagram of MCU part ML62Q1500/1800 group



* : Indicates the shared function of general ports. For available pins, refer to the pin list and pin definitions.

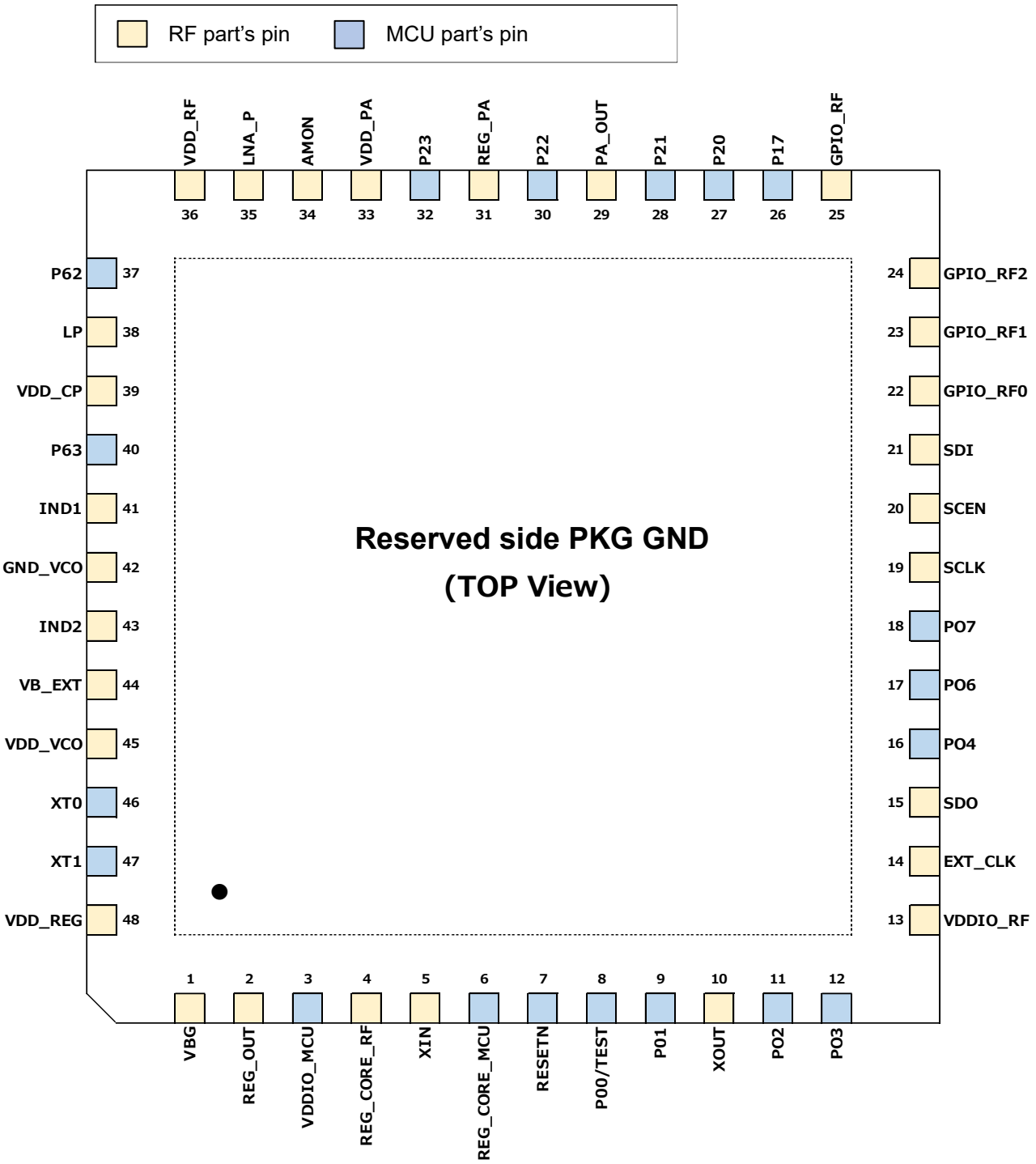
*1 : Shared UART and Synchronous Serial Port.

*2 : Not available as the input port when connecting to the on-chip debug emulator.

*3 : Not available as the input port when connecting to the crystal resonator.

■PIN Layout

48 pin WQFN



Note: GND pad in the middle of the LSI is reverse side (name: reversed side GND).

■PIN List

Table PIN List(1/2)

Pin No.	PIN Name (Primary Function)	Primary Function Others	2nd function communications	3rd function communications	4th function communications	5th function Timers	6th function Others	7th function Others	8th function ADC
1	VBG	-	-	-	-	-	-	-	-
2	REG_OUT	-	-	-	-	-	-	-	-
3	VDDIO_MCU	-	-	-	-	-	-	-	-
4	REG_CORE_RF	-	-	-	-	-	-	-	-
5	XIN	-	-	-	-	-	-	-	-
6	REG_CORE_MCU	-	-	-	-	-	-	-	-
7	RESET_N *1	-	-	-	-	-	-	-	-
8	P00/TEST *2	-	-	-	-	-	-	-	-
9	P01	DACOUT0	-	-	-	-	TBCOUT0	TBCOUT1	-
10	XOUT	-	-	-	-	-	-	-	-
11	P02	EXI0 EXTRG0	SU0_RXD0 SU0_SIN	-	-	FTM0P	OUTLSCLK	CMP0M	-
12	P03	EXI1 EXTRG1	SU0_TXD0 SU0_SOUT	SU0_TXD1	I2CU0_SDA	FTM0N	OUTHSCLK	CMP0P	AIN11
13	VDDIO_RF	-	-	-	-	-	-	-	-
14	EXT_CLK	-	-	-	-	-	-	-	-
15	SDO	-	-	-	-	-	-	-	-
16	P04	EXI2 EXTRG2	SU0_SCLK	-	I2CU0_SCL	TMH0OUT	-	-	-
17	P06	-	-	-	I2CM0_SDA	-	-	-	-
18	P07	-	SU0_RXD1	SU0_RXD0	I2CM0_SCL	-	-	-	-
19	SCLK	-	-	-	-	-	-	-	-
20	SCEN	-	-	-	-	-	-	-	-
21	SDI	-	-	-	-	-	-	-	-
22	GPIO_RF0	-	-	-	-	-	-	-	-
23	GPIO_RF1	-	-	-	-	-	-	-	-
24	GPIO_RF2	-	-	-	-	-	-	-	-
25	GPIO_RF3	-	-	-	-	-	-	-	-
26	P17	EXI3 EXTRG3	SU0_RXD1	SU0_RXD0	-	FTM1P	TBCOUT0	BZ0P	AIN0
27	P20	-	SU0_TXD1	-	-	FTM1N	TBCOUT1	BZ0N	AIN1
28	P21	EXI4 EXTRG4	SU1_RXD0 SU1_SIN	-	-	FTM2P	OUTLSCLK	-	AIN2
29	PA_OUT	-	-	-	-	-	-	-	-
30	P22	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	I2CM0_SDA	FTM2N	OUTHSCLK	-	AIN3
31	REG_PA	-	-	-	-	-	-	-	-
32	P23	EXI5 EXTRG5 V_{REF}	SU1_SCLK	-	I2CM0_SCL	TMH2OUT	-	-	V_{REFO}

Table PIN List(2/2)

Pin No.	PIN Name (Primary Function)	Primary Function Others	2nd function communications	3rd function communications	4th function communications	5th function Timers	6th function Others	7th function Others	8th function ADC
33	VDD_PA	-	-	-	-	-	-	-	-
34	AMON	-	-	-	-	-	-	-	-
35	LNA_P	-	-	-	-	-	-	-	-
36	VDD_RF	-	-	-	-	-	-	-	-
37	P62	-	-	-	-	FTM4N	-	CMP1P	-
38	LP	-	-	-	-	-	-	-	-
39	VDD_CP	-	-	-	-	-	-	-	-
40	P63	-	-	-	-	FTM4P	-	CMP1M	-
41	IND1	-	-	-	-	-	-	-	-
42	GND_VCO	-	-	-	-	-	-	-	-
43	IND2	-	-	-	-	-	-	-	-
44	VB_EXT	-	-	-	-	-	-	-	-
45	VDD_VCO	-	-	-	-	-	-	-	-
46	XT0	PI00	-	-	-	-	-	-	-
47	XT1	PI01	-	-	-	-	-	-	-
48	VDD_REG	-	-	-	-	-	-	-	-

*1 Connect RESET_N pin to VDD when On-chip debug function is not used.
*2 Connect P00/TEST0 pin to VDD when On-chip debug function is not used.

■PIN Definitions

I/O Definition			Symbols in reset state			Active Level		
I	:	Digital input	I	:	Input state	H	:	H level
O	:	Digital output	O	:	Output state	L	:	L level
IS	:	Schmitt trigger input	Hi-Z	:	High impedance	OD	:	Open drain
IO	:	Digital input/output				P	:	Rising
IA	:	Analog input				N	:	Falling
OA	:	Analog output 1						
OAH	:	Analog output 2						
IOA	:	Analog input/output						
IRF	:	RF input						
ORF	:	RF output						
VDDIO	:	I/O power supply						
VDDRF	:	RF power supply						
GND	:	Ground						

●MCU Part

The following Table shows each function's pin lists of ML7456N MCU part. "-" indicates the VDD pin, "(I)" indicates the input pin, "O" indicates the output pin and "(I/O)" indicates the input/output pin.

Function	Signal name	Pin name	I/O	Description	Logic
Power	-	Reserved Side GND	-	Negative Power Supply	-
	-	V_{DDIO_MCU}	-	Positive Power Supply Connect a Capacitor Cv between V_{DDIO_MCU} and V_{SS}	-
	-	REG_CORE_MCU	-	Power supply pin for internal logic (internal regulator's output).Connect a Capacitor C_L(1μF)between this pin and V_{SS}	-
Test	TEST0	P00	I/O	Input for testing, is used as on-chip debug interface and ISP function. If this pin is used for on-chip debug, this pin can not be used for general port. P00 is initialized as pull-up input mode by the system reset.	-
System	V_{REFO}	P23	—	Reference voltage output	-
	RESET_N	RESET_N	I	Reset input. Applying "L" level shifts the MCU in system reset mode. Applying "H" level shifts the CPU in program running mode. Used for on-chip debug interface and ISP function. No pull-up resistor is installed.	Negative
	XT0	XT0	I	Low speed crystal oscillation pins Connect 32.768kHz crystal resonator and Connect capacitors between the pin and V_{SS}.	-
	XT1	XT1	O		-
	OUTLSCLK	P02 P21	O	Low-speed clock output.	-
	OUTHSCLK	P03 P22	O	High-speed clock output.	-
General Purpose Port	PI00,PI01	XT0,XT1	I	General purpose input. Not available as general inputs when using the crystal oscillator, because this pin is combined use with Low-speed oscillator pin.	Positive
	P00	P00	I/O	General purpose I/O port - High-impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output Not available to use as general port when using for on-chip debug interface or ISP function, because this pin is combined use with TEST0 pin.	Positive
	P01 to P07	P01 to P07	I/O	General purpose I/O - High-impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P17	P17			
	P20 to P23	P20 to P23			
	P62 to P63	P62 to P63			

Function	Signal name	Pin name	I/O	Description	Logic
Serial communication unit (UART mode)	SU0_TXD0	P03	O	Serial communication unit0 UART0 data output	Positive
	SU0_RXD0	P02 P07 P17	I	Serial communication unit0 Full-duplex data input Serial communication unit0 UART0 data input	Positive
	SU0_TXD1	P03 P20	O	Serial communication unit0 Full-duplex data output Serial communication unit0 UART1 data output	Positive
	SU0_RXD1	P07 P17	I	Serial communication unit0 UART1 data input	Positive
	SU1_TXD0	P22	O	Serial communication unit1 UART0 data output	Positive
	SU1_RXD0	P21	I	Serial communication unit1 Full-duplex data input Serial communication unit1 UART0 data input	Positive
	SU1_TXD1	P22	O	Serial communication unit1 Full-duplex data input Serial communication unit1 UART0 data input	Positive

Function	Signal name	Pin name	I/O	Description	Logic
Serial communication unit (Synchronous Serial Port)	SU0_SIN	P02	I	Serial communication unit0 Synchronous serial data input	Positive
	SU0_SCLK	P04	I/O	Serial communication unit0 Synchronous serial clock I/O	Positive
	SU0_SOUT	P03	O	Serial communication unit0 Synchronous serial data output	Positive
	SU1_SIN	P21	I	Serial communication unit1 Synchronous serial data input	Positive
	SU1_SCLK	P23	I/O	Serial communication unit1 Synchronous serial clock I/O	Positive
	SU1_SOUT	P22	O	Serial communication unit1 Synchronous serial data output	Positive
I^2C Bus	I2CU0_SDA	P03	I/O	I^2C Unit0 (Master and Salve) Data I/O N-channel open drain Connect a pull-up resistor externally	Positive
	I2CU0_SCL	P04	I/O	I^2C Unit0 (Master and Salve) Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
	I2CM0_SDA	P06 P22	I/O	I^2C Master0 Data I/O pin N-channel open drain output Connect a pull-up resistor externally	Positive
	I2CM0_SCL	P07 P23	I/O	I^2C Master0 Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer	FTM0P	P02	O	Functional Timer 0 P Output	Positive
	FTM0N	P03	O	Functional Timer 0 N Output	Negative
	FTM1P	P17	O	Functional Timer 1 P Output	Positive
	FTM1N	P20	O	Functional Timer 1 N Output	Negative
	FTM2P	P21	O	Functional Timer 2 P Output	Positive
	FTM2N	P22	O	Functional Timer 2 N Output	Negative
	FTM4P	P63	O	Functional Timer 4 P Output	Positive
	FTM4N	P62	O	Functional Timer 4 N Output	Negative
	EXTRG0	P02	I	Functional Timer Event Trigger Input	-
	EXTRG1	P03	I	Functional Timer Event Trigger Input	-
	EXTRG2	P04	I	Functional Timer Event Trigger Input	-
	EXTRG3	P17	I	Functional Timer Event Trigger Input	-
	EXTRG4	P21	I	Functional Timer Event Trigger Input	-
	EXTRG5	P23	I	Functional Timer Event Trigger Input	-
16 bit timer	TMH0OUT	P04	O	16 bit Timer 0 Output	Positive
	TMH2OUT	P23	O	16 bit Timer 2 Output	Positive
	EXTRG0	P02	I	16 bit Timer Event Trigger Input	-
	EXTRG1	P03	I	16 bit Timer Event Trigger Input	-
Low-speed Time Base Counter	TBCOUT0	P01 P17	O	The virtual frequency adjustment output signal	Positive
	TBCOUT1	P01	O	Low speed time base counter output signal 1Hz/2Hz	Positive
Buzzer	BZ0P	P17	O	Buzzer output (positive phase)	Positive

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	External Interrupt 0 Input	-
	EXI1	P03	I	External Interrupt 1 Input	-
	EXI2	P04	I	External Interrupt 2 Input	-
	EXI3	P17	I	External Interrupt 3 Input	-
	EXI4	P21	I	External Interrupt 4 Input	-
	EXI5	P23	I	External Interrupt 5 Input	-
Successive approximation type A/D converter (SA-ADC)	V_{REF}	P23	-	SA-ADC external reference voltage input	-
	AIN0	P17	I	SA-ADC channel 0 input	-
	AIN1	P20	I	SA-ADC channel 1 input	-
	AIN2	P21	I	SA-ADC channel 2 input	-
	AIN3	P22	I	SA-ADC channel 3 input	-
	AIN11	P03	I	SA-ADC channel 11 input	-
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	-
	CMP0M	P02	I	Comparator input 0 (inverting input)	-
	CMP1P	P62	I	Comparator input 1 (noninverting input)	-
	CMP1M	P63	I	Comparator input 1 (inverting input)	-
D/A converter	DACOUT0	P01	O	D/A converter 0 output	-

●RF Part

○RF and Analog Pins

Pin name	Reset State	I/O	Active Level	Pin Function
PA_OUT	O	ORF	-	RF antenna output
AMON	Hi-Z	IOA	-	Test (*1)
LNA_P	I	IA	-	RF antenna input
LP	-	IOA	-	Pin for loop filter
IND1	-	IOA	-	Inductor connection pin for VCO tank
IND2	-	IOA	-	Inductor connection pin for VCO tank
VB_EXT	-	IOA	-	Pin for smoothing capacitor for internal bias

[Note]
*1 Used for checking analog functions at LAPIS Technology.

○SPI Interface Pins

Pin name	Reset State	I/O	Active Level	Pin Function
SDO	Hi-Z	O	H or L or OD	SPI data output or DCLK output(*1) * OpenDrain output is selected in the reset state. When using SDO as CMOS output, set SDO_OD([SPI/EXT_PA_CTRL: B0 0x53(7)]) to 0b0.
SCLK	Hi-Z	IS	P or N	SPI clock input
SCEN	Hi-Z	IS	L	SPI chip enable L: Enabled H: Disabled
SDI	Hi-Z	I	H or L	SPI data input or DIO I/O(*1)

[Note]
*1 Please refer to “DIO function”

○Regulator Pins

Pin name	Reset State	I/O	Active Level	Pin Function
VBG	-	OAH	-	Pin for decoupling capacitor
REG_OUT	-	OAH	-	Requlator1 output (typ. 1.5V)
REG_CORE_RF	-	OA	-	Requlator2 output (typ. 1.5V)
REGPDIN	I	I	H	Power down control pin for regulator Fix to “L” for normal use. “H” is for deep sleep mode.
REG_PA	-	OAH	-	Regulator output for PA block

PIN definitions (continued)

○Miscellaneous Pins

Pin name	Reset State	I/O	Active Level	Pin Function
XIN N.C.(*2)	I -	IA -	P or N -	36MHz crystal pin 1 * When using TCXO, this must be open.
XOUT TCXO(*2)	-	OA	P or N	36MHz crystal pin 2 (TCXO input)
EXT_CLK	Hi-Z	IO	-	Digital I/O (*3) Reset state: External PA control signal output
GPIO_RF0	Hi-Z	IO	H or L or OD(*1)	Digital I/O (*4) Reset state: Interrupt indication signal output
GPIO_RF1	Hi-Z	IO	H or L or OD(*1)	Digital I/O (*5) Reset state: Clock output
GPIO_RF2	Hi-Z	IO	H or L or OD(*1)	Digital I/O (*6) Reset state: Antenna diversity selection control signal
GPIO_RF3	Hi-Z	IO	H or L or OD(*1)	Digital I/O (*7) Reset state: TX – RX selection signal output

[Note]
- *1 OD is open drain output.
- *2 When using TCXO, set TCXO_EN = 0b1. Please make sure only one of the registers TCXO_EN and XTAL_EN is set to 0b1.
- *3 Refer to [EXTCLK_CTRL: B3 0x2C].
- *4 Refer to [GPIO0_CTRL: B3 0x28].
- *5 Refer to [GPIO1_CTRL: B3 0x29].
- *6 Refer to [GPIO2_CTRL: B3 0x2A].
- *7 Refer to [GPIO3_CTRL: B3 0x2B].

PIN definitions (continued)

○Power Supply/GND Pins

Pin name	Reset State	I/O	Active Level	Pin Function
VDD_REG	-	V_{DDIO}	-	Power supply pin for Regulator (Input voltage: 2.6 to 3.6 V)
VDDIO_RF	-	V_{DDIO}	-	Power supply for digital I/O (Input voltage: 2.6 to 3.6 V)
VDD_PA	-	V_{DDIO}	-	Power supply for PA block (Input voltage: 2.6 to 3.6 V, depending on TX mode)
VDD_RF	-	V_{DDRF}	-	Power supply for RF blocks (REG_OUT is connected, typ. 1.5 V)
VDD_CP	-	V_{DDRF}	-	Power supply for charge pump (REG_OUT is connected, typ. 1.5 V)
GND	-	GND	-	GND for VCO
VDD_VCO	-	V_{DDRF}	-	Power supply for VCO (REG_OUT is connected, typ. 1.5 V)

●Unused Pins Treatment

Unused pins treatment are as follows: The treatments that impair the basic operations of this LSI are not included.

Unused pins treatment

Pin Name	Recommended treatment
XIN	Open (with TCXO)
EXT_CLK	Open
GPIO_RF0	Open
GPIO_RF1	Open
GPIO_RF2	Open
GPIO_RF3	Open
AMON	GND
RESET_N	Connect to VDDIO_MCU
P00/TEST0	Connect to VDDIO_MCU with Pull-UP (Initial Value) that is Input mode.
XT0/PI00, XT1/PI01	Set the pin to Open with HiZ (Initila Value) state.
P00	Set the pin to Open with HiZ (Initila Value) state.
P01 to P07	
P17	
P20 to P23	
P62 to P63	

[Note]
If unused input pins, input/output pins are set to input and are high-impedance state and leave open (Input mode without Pull-UP or Input/Output mode), excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.

●Internal Pins

This product is configured woth RF and MCU parts. This chapter explains internal pins in the package.

The following table shows internal connections in the package.

Table. Internal Connection in the package

MCU part Internal Pins Name	RF part Internal Pins Name
P73	REGPDIN
P74	RESETN

The following table shows the internal pins in the package.

Table. Internal Pins in the package (MCU part)

Function	Signal Nmae	Pin Name	I/O	Description	Logic
General Purpose Port	P73	P73	I/O	General Input/Output ・HiZ (Initial Value) ・Input with Pull-UP resister ・Input without Pull-UP resister ・CMOS output ・N-ch Open drain output	Positive
	P74	P74			

The following table shows the RF part's internal pins in the package.

Table. Internal Pins in the package (RF part)

Pin Name	Input/Output	Active Level	Reset State	Description
RESETN	Is	L	I / -	RF Hardware Reset Pin L: Initialize, Stop H: Operation * If this pin is set to "L", RF part is initialized. Set this pin to "L" when RF is deepsleep state.
REGPDIN	I	H	I / -	RF Regulator Power Down Control Pin Fix this pin to "L" when normal operation. Set this pin to "H" when RF is deepsleep state.

■Electrical Characteristics

●Absolute Maximum Ratings

Ta = -40 to +85 ˚C and GND = 0 V are the typical conditions if not defined specifically.

Item	Symbol	Condition	Rating	Unit
I/O power supply	V_{DDIO} V_{DDIO_MCU}	-	-0.3 to +4.6	V
RF power supply	V_{DDRF}	-	-0.3 to +2.0	V
RF input level	P_{RFI}	Antenna input in RX	+10	dBm
RF output voltage	V_{RFO}	PA_OUT pin	-0.3 to 4.6	V
Voltage on Analog Pins 1	V_A	-	-0.3 to 2.0	V
Voltage on Analog Pins 2	V_{AH}	-	-0.3 to 4.6	V
Voltage on Digital input Pins	V_{IN}	-	-0.3 to V_{DDIO}+0.3[*1] -0.3 toV_{DDIO_MCU}+0.3[*1]	V
Voltage on Digital output Pins	V_{OUT}	-	-0.3 to V_{DDIO}+0.3[*1] -0.3 to V_{DDIO_MCU}+0.3[*1]	V
Digital output current (RF part)	I_{DO}	-	-8 to +8	mA
Digital output current (MCU part)	I_{DO2}	-	-15 to +15	mA
Power dissipation	Pd	Ta= +25℃	1.2	W
Storage temperature	T_{stg}	-	-55 to +150	℃

*1: It needs to be less than 4.6V

*2: Minus sign shows current direction from internal side of LSI to pin.
The current absolute value is the maximum value.
Example: -1mA shows that the maximum 1mA current flows from internal side of LSI to pin.

[Note]
Absolute Maximum Ratings are the tolerance to protect the product's physical quality, do not guarantee the normal operaton.

●Recommended Operating Conditions

Item	Symbol	Condition	Min.	Standard	Max.	Unit
Power Supply	V_{DDIO}	VDDIO_RF pin VDD_REG pin VDD_PA pin VDDIO_MCU pin (*1)	2.6	3.3	3.6	V
Operating temperature	T_a	-	-40	+25	+85	℃
Digital input rise time	T_{IR}	Digital input pins (*1)	-	-	20	ns
Digital input fall time	T_{IF}	Digital input pins (*1)	-	-	20	ns
Digital output load	C_{DL}	All Digital Output pins	-	-	20	pF
Master clock frequency (XIN/XOUT pin)	F_{MCK1}	-	-	36	-	MHz
Master clock accuracy (*2)	A_{CMCK1}	FSK 時	-20	-	+20	ppm
X' tal equivalent series resistance	ESR	-	―	-	80	ohm
TCXO input voltage	V_{TCXO}	DC cut *TCXO opetions selected	0.8	-	1.5	Vpp
Operating frequency(CPU)	f_{OP}	-	30k	-	25M	Hz
REG_CORE_MCU attached capacity	C_L	-	1.0-30%	1.0	1.0+30%	uF
RF frequency	F_{RF}	-	315	-	450	MHz
			750	-	960	MHz

*1 In the pin description, I or Is are specified as the I/O.

*2 Indicating frequency deviation during TX-RX operation. In order to support various standards, please apply the frequency accuracy for each standard to meet the requirements.

Specification	**Required accuracy**
ARIB STD T-108	±20 ppm

*Below typical values indicate typical center values. They are not guaranteed values with consideration given to a variety of ICs.

●MCU

○Power Consumption

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 ºC if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.*3	Max.	
Power Consumption 0	IDD0	CPU is STOP-D state All oscillators are stopped	—	0.8	23	μA
Power Consumption 1	IDD1	CPU is STOP state All oscillators are stopped	—	1.0	26	μA
Power Consumption 2	IDD2-1	Low RC oscillation*1 CPU is HALT state PLL oscillation is stopped	—	4.7	35	μA
Power Consumption 2-2	IDD2-2	Low oscillator*1*4 CPU is HALT state PLL oscillation is stopped	—	3.0	32	μA
Power Consumption 3	IDD3	CPU is operated with RC*1*2 PLL oscillation is stopped	—	17	105	μA
Power Consumption 4	IDD4	CPU is operated 16MHz *1*2 When PLL 16MHz oscillation V_{DDIO_MCU}=2.6 to 3.6V	—	3.3	4.5	mA
Power Consumption 5	IDD5	CPU is operated with 24MHz*1*2 When PLL 24MHz oscillation V_{DDIO_MCU}=2.6 to 3.6V	—	4.7	6.0	mA

*1: LTBC, WDT operating state, All controllable bits of Block Control Register（BCKCONn） and Block Reset Control Register（BRECONn） are set to “1”.

*2: CPU is operated with Wait mode.

*3: V_{DDIO_MCU}=3.0V,Ta=+25 ºC

*4: Low current consumption mode, Noise removal filter is set to off.

○Low Speed Crystal Oscillator Characteristics

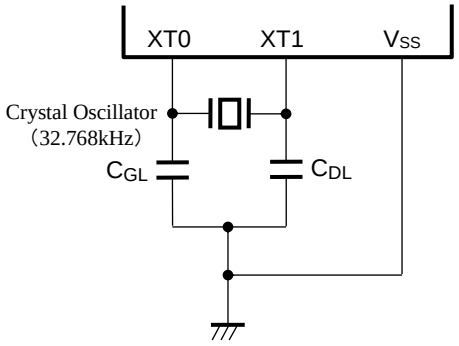
(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Crystal Oscillator Frequency*1 *2	f_{XTL}	-	-	32.768	-	kHz
Crystal Oscillator Starting time	T_{XTL}	-	-	-	2	s

*1: Oscillation frequency depends on oscllator circuit, crystal oscillator and circuit constant of capacitor with attached crystal oscillator(CGL/CDL).
Matching evaluation on the implemented curcuit is neccesary because the circuit constant depends on crystal oscillator.
Receive confirmation of oscillation characteristic from oscillator manifacture with marching evaluation.

*2: There is a possibility that the expected oscilation characterictic is not guaranteed. It depends on material, writing pattern of circuit board, writing, parasitic capacitance of crystal oscillator and pins.
Please take care of attached external circuit.
- Make the writing pattern of external circuit as short as possible.
- Make the writing pattern between capacitor of the attached crystal oscaillator and the crystal oscillator as short as possible.
- Make the external circuit writing pattern and the writing pattern that large current flows not to cross or be close each other.
- Make the external circuit writing pattern and the other signal's writing pattern not to cross.
- Make the external capacitor of crystal oscillator to connect the GND whose current fluctuation and voltage fluctuation as small as possible.
- There is a possibility that the expected oscillation characteristic is not guaranteed because of the environment of moisture absorption of board, condensation of board surface. Resin sealed of circuit board and so on are recommended.

Example of circuit diagram of Low-speed crystal oscillator



○External Clock Input Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	—	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input Pulse Width	t_{EXCKW}	—	$1/f_{EXCK}$ x 0.4		$1/f_{EXCK}$ x 0.6	s

○On-Chip Oscillator Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 ºC if not defined specifically.)

Item	Symbol	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Low speed RC Oscillator Frequency1 without software correction	f_{RCL1}	Ta=+25 ºC, V_{DDIO_MCU}=2.6 to 3.6V	Typ. -2.0%	32.768	Typ. +2.0%	kHz	
		Ta=-40 to +85 ºC, V_{DDIO_MCU}=2.6 to 3.6V	Typ. -3.5%	32.768	Typ. +3.5%		
Low speed RC Oscillator Frequency 2 with software correction	f_{RCL2}	Ta=-40 to +85 ºC, V_{DDIO_MCU}=2.6 to 3.6V	Typ. -2.0%	32.768	Typ. +2.0%		
PLL Oscillation Frequency 1 Internal low speed RC without software correction	f_{PLL1}	Ta=-40 to +85 ºC, V_{DDIO_MCU}=2.6 to 3.6V	Typ. -2.5%	16/24	Typ. +2.5%	MHz	
PLL Oscillation Frequency 2 Internal Low speed RC with software correction	f_{PLL2}	Ta=-40 to +85 ºC, V_{DDIO_MCU}=2.6 to 3.6V	Typ. -1.0%	16/24	Typ. +1.0%		
PLL Oscillation Stable Time	T_{PLL}	Ta=-40 to +85 ºC, V_{DDIO_MCU}=2.6 to 3.6V	-	-	2	ms	
Low speed RC1K Oscillator Frequency （Only for Watchdog timer）	f_{RC1K}	Ta=-40 to +85 ºC, V_{DDIO_MCU}=2.6 to 3.6V	0.5	1	2.5	kHz	

○Input,Output Pins Characteristics 1

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition		Standard			Unit	
				Min.	Typ.	Max.		
"H"/"L" Level Output Voltage 1 (P00) (P01 to P07) (P17) (P20 to P23) (P62 to P63)	VOH1	IOH1=-1mA V_{DDIO_MCU}≧2.6V		V_{DD} -0.5	-	-	V	
	VOL1	IOL1=+1mA V_{DDIO_MCU}≧2.6V		-	-	0.5		
"L" Level Output Voltage 2 (P01 to P07) (P17) (P20 to P23) (P62 to P63)	VOL2	When N-ch Open drain output selected	IOL2=+8mA V_{DDIO_MCU}≧3.0V	-	-	0.5		
			IOL2=+3mA V_{DDIO_MCU}≧2.6V	-	-	0.4		

○Input, Output Pins Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition		Standard Min.	Standard Typ.	Standard Max.	Unit
"H" Level Output Current 1 *6	IOH1	1 pin	V_{DD}≧2.6V	-1 *3*5	-	-	mA
"H" Level Output total Current *1*4	IOH3	"Sum of P00 to P07" or "Sum of P17, P20 to P23, P62 to P63" (When Duty≦50%)	V_{DD}≧2.6V	-20 *5	-	-	
		Sum of all pins (When Duty≦50%)	V_{DD}≧2.6V	-40 *5			
"L" Level Output Current 1 *6	IOL1	1 pin (When CMOS Output selected)	V_{DD}≧2.6V	-	-	1 *3	
"L" Level Output Current 2 *6	IOL2	1 pin (When N-ch Open drain output selected)	V_{DD}≧3.0V	-	-	8 *3	
			V_{DD}≧2.6V	-	-	3 *3	
"L" Level Output Total Current *2*4	IOL3	"Sum of P00 to P07" or "Sum of P17, P20 to P23, P62 to P63" (When N-ch Open drain Output selected, Duty≦50%)	V_{DD}≧3.0V	-	-	40	
			V_{DD}≧2.6V	-	-	15	
		Sum of all pins (When N-ch Open drain Output selected, Duty≦50%)	V_{DD}≧2.6V			20	
Output Leak (P00) (P01 to P07) (P17) (P20 to P23) (P62 to P63)	IOOH	VOH=V_{DD} (When HiZ)		-	-	+1	μA
	IOOL	VOL=V_{SS} (When HiZ)		-1*5	-	-	

*1 : This current value guarantees the device normal operation if it flows from V_{DDIO_MCU} pin to output pin.

*2 : This current value guarantees the device normal operation if it flows from output pin to V_{SS} pin.

*3 : Do not exceed the total output current.

*4 : This is the output current when Duty≦50%.

On the condition of Duty＞50%, the output current is calculated as the following formula,

Total output current of pins＝IOL3 x 50/n (When Duty is n%)

＜Example of calculation＞

When IOL3=100mA, n=80%,

Total output current of pins＝ IOL3 x 50/80=62.5mA

The current that can be flowed to 1 pin is the same, and follows IOL1, IOL2.

It is impossible to flow the current more than Absolute Maximum Ratings.

*5 : If current flows from internal side of LSI to pin, minus sign is written.
Absolute current value is the maximum value.
Example : -1mA means the maximum 1mA current flows from LSI pin.

*6 : It is condition to satisfy VOH1,VOL1,VOL2.

○Input, Output Pins Characteristics 3

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Input Current1 (RESET_N)	IIH1	VIH1=V_{DD}	-	-	1	μA	
	IIL1	VIL1=V_{SS}	-1*1	-	-		
Input Current 2 (P00/TEST0)	IIL2	VIL2=V_{SS} (When Pull-UP)*2	-1500*1	-300*1	-20*1		
	V/IIL2	VIL2=V_{SS} (When Pull-UP)*2	3.7	10	80	kΩ	
	IIH2Z	VIH2=V_{DD} (When HiZ)	-	-	1	μA	
	IIL2Z	VIL2=V_{SS} (When HiZ)	-1*1	-	-		
Input Current 3 (P01-P07) (P17) (P20-P23) (P62-P63)	IIL3	VIL1=V_{SS} (When Pull-UP)*2	-250*1	-30*1	-2*1		
	V/IIL3	VIL1=V_{SS} (When Pull-UP)*2	22	100	800	kΩ	
	IIH3Z	VIH1=V_{DD} (When HiZ)	-	-	1	μA	
	IIL3Z	VIL1=V_{SS} (When HiZ)	-1*1	-	-		
Input Current 4 (PI00-PI01)	IIH4	VIH1=V_{DD}	-	-	1		
	IIL4	VIL1=V_{SS}	-1*1	-	-		
Input Voltage 1 (RESET_N) (P01-P07) (P17) (P20-P23) (P62-P63) (PI00-PI01)	VIH1	-	0.7 xV_{DD}	-	V_{DD}	V	5
	VIL1	-	0	-	0.3 xV_{DD}		
Input Voltage 2 (P00/TEST0)	VIH2	-	0.7 xV_{DD}	-	V_{DD}		
	VIL2	-	0	-	0.25 xV_{DD}		
Pin Capacitor (RESET_N) (P00/TEST0) (P01-P07) (P17) (P20-P23) (P62-P63) (PI00-PI01)	CPIN	f = 10kHz Ta = +25°C	-	-	10	pF	-

*1: If current flows from internal side of LSI to pin, minus sign is written.
Absolute current value is the maximum value.
Example: -1mA means the maximum 1mA current flows from LSI pin.

*2: Typ. value is a condition of V_{DDIO_MCU} =3.0V. Max. value is a condition of V_{DDIO_MCU} =2.6V, Min.value V_{DDIO_MCU} =3.6V.

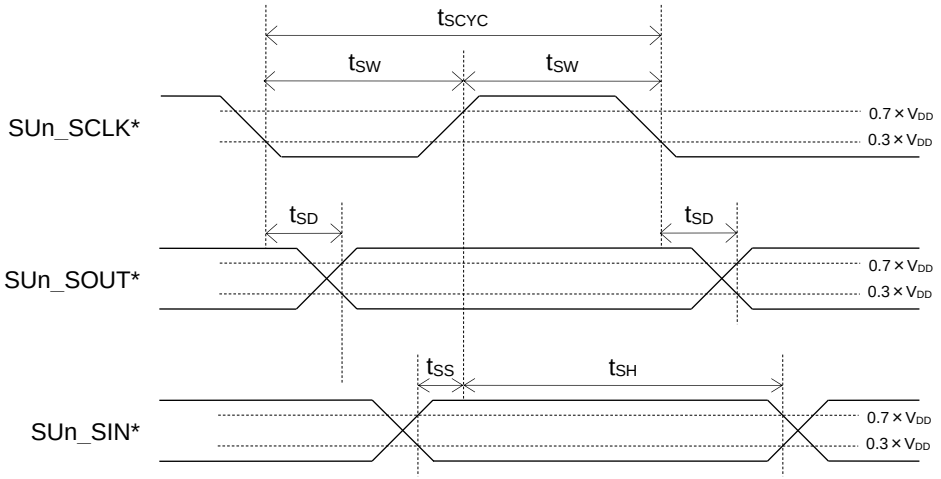
○Synchronous Serial Port Characteristics

Slave Mode

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
SCLK Input Cycle	t_{SCYC}	-	1*2	-	-	μs
SCLK Input Pulse Width	t_{SW}	-	0.5*3	-	-	μs
SOUT Output Delay Time	t_{SD}	-	-	-	100+ HSCLK*1×3	ns
SIN Input Setup Time	t_{SS}	-	HSCLK*1×1	-	-	ns
SIN Input Hold Time	t_{SH}	-	80+ HSCLK*1×3	-	-	ns

*1: High speed clock frequency
*2: More than HSCLK × 8 input cycle is neccesary.
*3: More than HSCLK × 4 input cycle is neccesary.



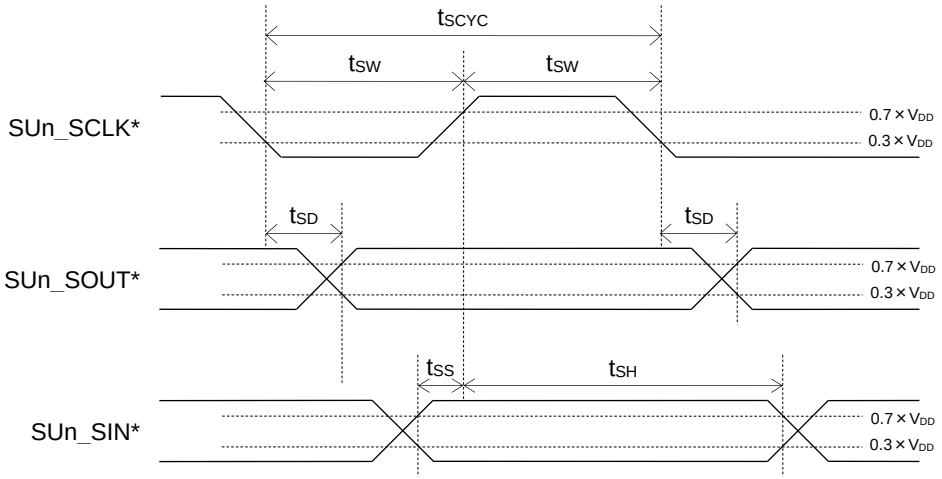
*: Port's 2nd to 8th functions.
n: 0 to 5

Master Mode

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
SCLK Output Cycle	t_{SCYC}	-	-	SCLK*1	-	ns
SCLK Output Pulse Width	t_{SW}	-	SCLK*1×0.4	SCLK*1×0.5	SCLK*1×0.6	ns
SOUT Output Delay Time	t_{SD}	-	-	-	100	ns
SIN Input Setup Time	t_{SS}	-	120	-	-	ns
SIN Input Hold Time	t_{SH}	-	80	-	-	ns

*1 : Clock frequency that is selected by bit 12-8(SnCK4-0) of Synchronous Serial Port n Mode Register(SIOnMOD).
(When V_{DDIO_MCU}≧2.6V : min250ns)



*: Port's 2nd – 8th functions.
n : 0 to 5

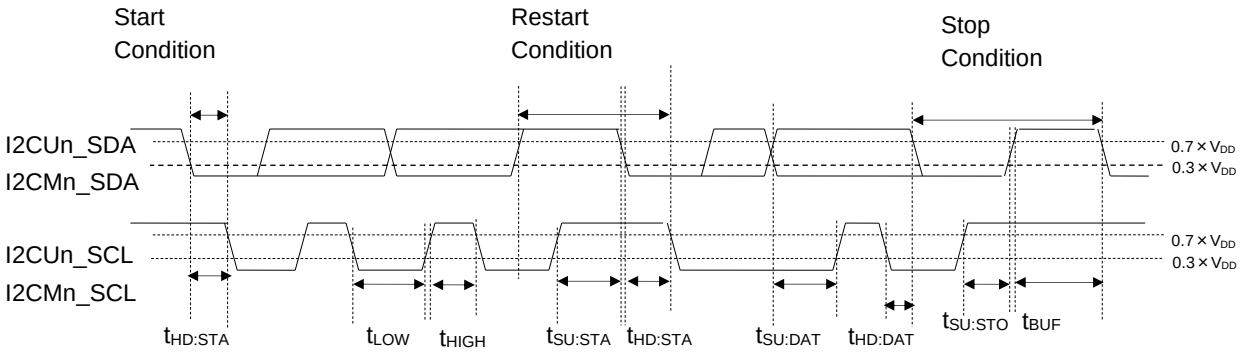
○I²C Bus Interface Characteristics

Standard Mode（100kbps）

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.）

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
SCL Clock Frequency	f_{SCL}	-	0	-	100	kHz
SCL Hold Time (Start/Restart Condition)	$t_{HD:STA}$	-	4.0	-	-	µs
SCL“L” Level time	t_{LOW}	-	4.7	-	-	µs
SCL“H” Level Time	t_{HIGH}	-	4.0	-	-	µs
SCL Setup Time (Restart Condition)	$t_{SU:STA}$	-	4.7	-	-	µs
SDA Hold Time	$t_{HD:DAT}$	-	0	-	-	µs
SDA Setup Time	$t_{SU:DAT}$	-	0.25	-	-	µs
SDA Setup Time (Stop Condition)	$t_{SU:STO}$	-	4.0	-	-	µs
Bus Free Time	t_{BUF}	-	4.7	-	-	µs

When it is used for I²C bus master, set I²C Master n Mode Register (I2MnMOD), I²C Bus 0 Mode Register (Master side) (I2UM0MOD) to conform to the above standard.



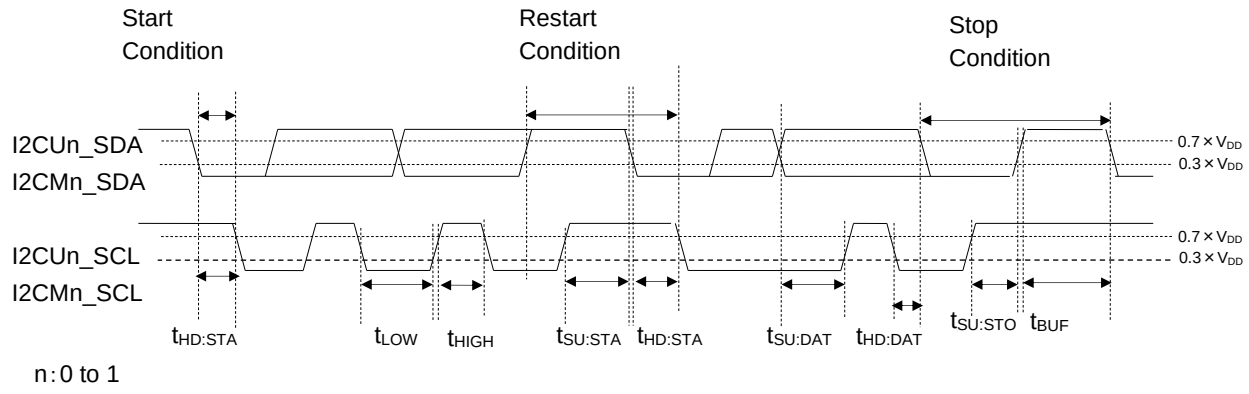
n：0 to 1

Fast Mode（400kbps）

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.）

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
SCL Clock Frequency	f_{SCL}	-	0	-	400	kHz
SCL Hold Time (Start/Restart Condition)	$t_{HD:STA}$	-	0.6	-	-	µs
SCL“L” Level Time	t_{LOW}	-	1.3	-	-	µs
SCL“H” Level Time	t_{HIGH}	-	0.6	-	-	µs
SCL Setup Time (Restart Condition)	$t_{SU:STA}$	-	0.6	-	-	µs
SDA Hold Time	$t_{HD:DAT}$	-	0	-	-	µs
SDA Setup Time	$t_{SU:DAT}$	-	0.1	-	-	µs
SDA Setup Time (Stop Condition)	$t_{SU:STO}$	-	0.6	-	-	µs
Bus Free Time	t_{BUF}	-	1.3	-	-	µs

When it is used for I²C bus master, set I²C Master n Mode Register (I2MnMOD), I²C Bus 0 Mode Register (Master side) (I2UM0MOD) to conform to the above standard.



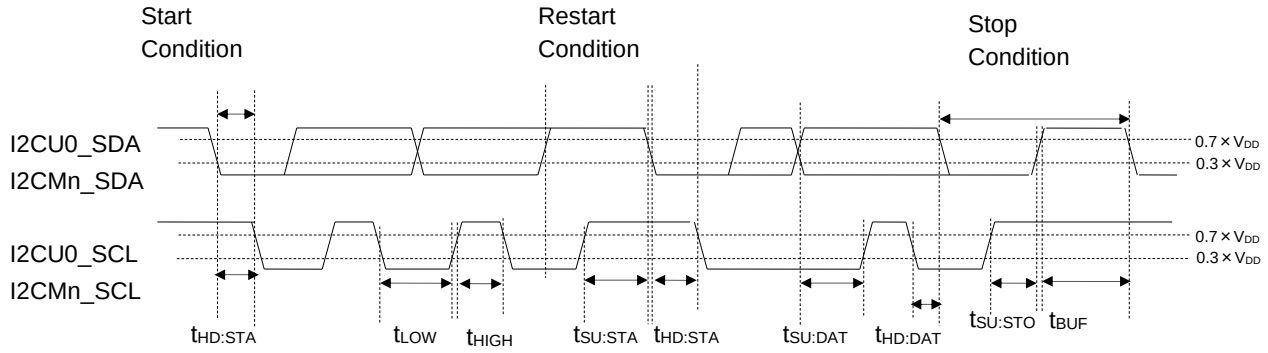
n：0 to 1

1Mbps Mode

(V_{DDIO_MCU} = 2.7 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
SCL Clock Frequency	f_{SCL}	-	0	-	1000	kHz
SCL Hold Time (Start/Restart Condition)	$t_{HD:STA}$	-	0.26	-	-	µs
SCL"L" Level Time	t_{LOW}	-	0.5	-	-	µs
SCL"H" Level Time	t_{HIGH}	-	0.26	-	-	µs
SCL Setup Time (Restart Condition)	$t_{SU:STA}$	-	0.26	-	-	µs
SDA Hold Time	$t_{HD:DAT}$	-	0	-	-	µs
SDA Setup Time	$t_{SU:DAT}$	-	0.1	-	-	µs
SDA Setup Time (Stop Condition)	$t_{SU:STO}$	-	0.26	-	-	µs
Bus Free Time	t_{BUF}	-	0.5	-	-	µs

When it is used for I²C bus master, set I²C Master n Mode Register (I2MnMOD), I²C Bus 0 Mode Register (Master side) (I2UM0MOD) to conform to the above standard.



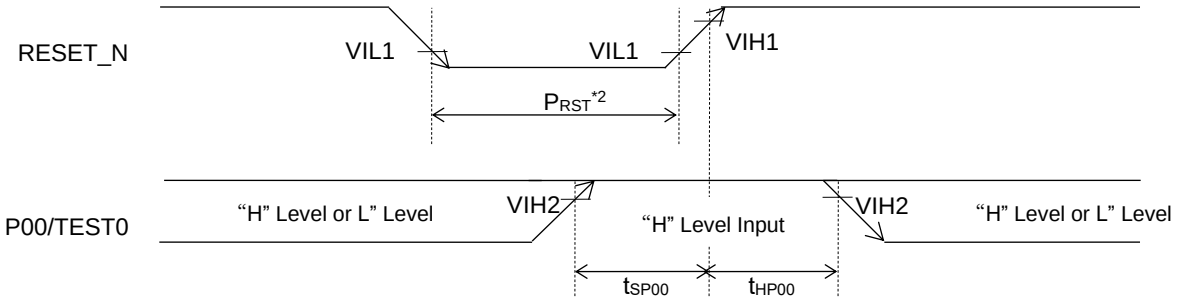
n : 0 to 1

○ Reset Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Reset Enable Time	P_{RST}	-	2	-	-	ms
P00“H” Level Setup Time	t_{SP00}	-	1	-	-	ms
P00“H”Level Hold Time*1	t_{HP00}*1	-	1	-	-	ms

*1: It is the regulation without ISP mode. When ISP mode is used, refer to the timing of ISP mode of User's Manual “25.4 In-System Programing Function”.



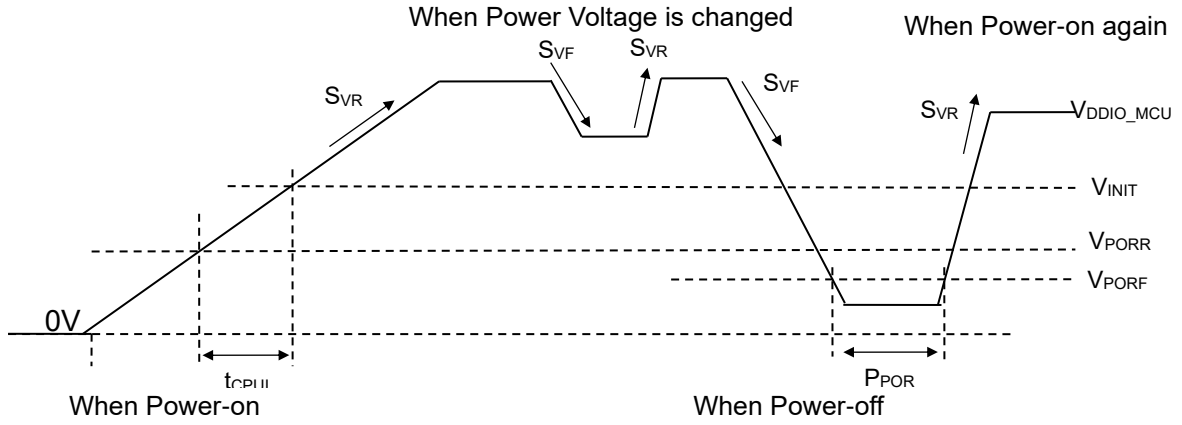
*2: When Power on reset, the time is counted after V_{DDIO_MCU}=2.6V.

[Note]
- If the pulse that is shorter than Reset Enable Time (PRST) is inputted into Reset pin, unexpected operation will be caused. Do not input short pulse than Reset Enable Time.

○Power Slope, Power-on Reset Characteristics

(V_{SS}=0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Power Rising Slope	S_{VR}	-	-	-	60	V/ms	
Power Falling Slope	S_{VF}	-	-	-	2	V/ms	
Power-on Reset Judgement Voltage	V_{PORR}	When Power-on Rising	1.47	1.57	1.80	V	
	V_{PORF}	When Power-on Falling	1.33	1.49	1.58	V	
Power-on Reset Minimum Pulse Width	P_{POR}	-	200	-	-	µs	
Power-on Initial Voltage	V_{INIT}	When Power-on	1.8	-	-	V	
CPU Operation Start time (Time between releasing Reset and CPU Operation Start)	t_{CPUI}	-	11	16	-	ms	-



[Note]
- If short pulse that is shorter than Power-on Reset response time is inputted into, there is a possibility that LSI is not reset and operated incorrectly. Prevent low power voltage by Bypass capacitors or reset by Reset input pin.
- Start High speed clock after V_{DDIO_MCU} voltage becomes within the operating voltage.

○VLS Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 ºC if not defined specifically.)

Item	Symbol	Condition		Standard			Unit	
		VLS0LV[*1]	Power Voltage	Min.	Typ.	Max.		
VLS Judgement Voltage[*2]	V_{VLSR}	00H	Rising	3.86	4.06	4.26	V	
	V_{VLSF}		Falling	3.84	4.00	4.16		
	V_{VLSR}	01H	Rising	3.57	3.76	3.95		
	V_{VLSF}		Falling	3.55	3.70	3.85		
	V_{VLSR}	02H	Rising	2.94	3.11	3.28		
	V_{VLSF}		Falling	2.92	3.05	3.18		
	V_{VLSR}	03H	Rising	2.85	3.01	3.17		
	V_{VLSF}		Falling	2.83	2.95	3.07		
	V_{VLSR}	04H	Rising	2.75	2.91	3.07		
	V_{VLSF}		Falling	2.73	2.85	2.97		
	V_{VLSR}	05H	Rising	2.66	2.81	2.96		
	V_{VLSF}		Falling	2.64	2.75	2.86		
	V_{VLSR}	06H	Rising	2.56	2.71	2.86		
	V_{VLSF}		Falling	2.54	2.65	2.76		
	V_{VLSR}	07H	Rising	2.46	2.61	2.76		
	V_{VLSF}		Falling	2.44	2.55	2.66		
	V_{VLSR}	08H	Rising	2.37	2.51	2.65		
	V_{VLSF}		Falling	2.35	2.45	2.55		
	V_{VLSR}	09H	Rising	1.98	2.11	2.24		
	V_{VLSF}		Falling	1.96	2.05	2.14		
	V_{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V_{VLSF}		Falling	1.87	1.95	2.03		
	V_{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V_{VLSF}		Falling	1.77	1.85	1.93		
VLS Current Consumption	I_{VLS}	-		-	50	-	nA	

[*1]: Bit3 to 0 of Voltage Level Supervisor Function 0 Level Register (VLS0LV)

[*2]: Setting VLS0LV=0CH - 0FH of VLS Judgement Voltage is inhibited.

○Analog Comparator Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS}=0V, Ta=-40 to +85 ºC if not defined specifically.)

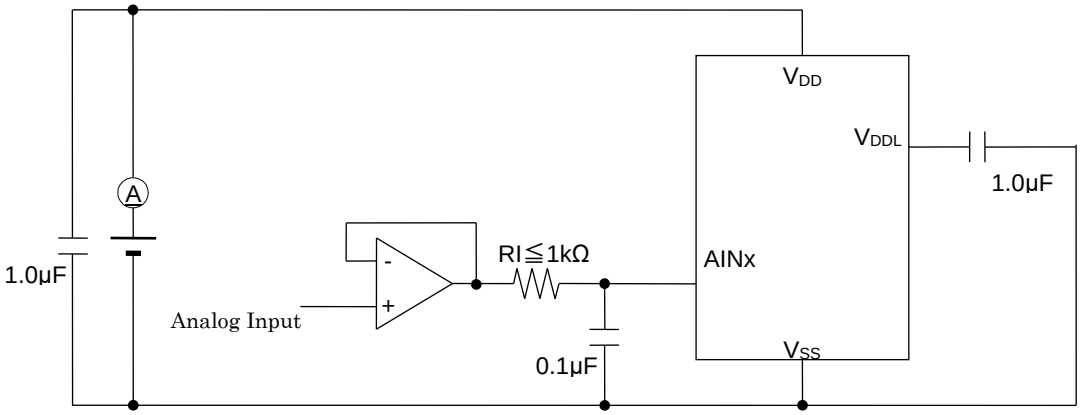
Item	Symbol	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Comparator In-Phase Input Voltage Range	V_{CMR}	-	0.1	-	V_{DDIO_MCU} -1.5	V	
Comparator Input Offset	V_{CMOF}	Ta=+25 ºC, V_{DDIO_MCU}=3.3V	-	5	-	mV	
Comparator Reference Voltage	V_{CMREF}	-	0.75	0.8	0.85	V	

○Successive Approximation Type A/D Converter

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Resolution	n_{AD}	-	-	-	10	Bit
Integral Nonlinearity	INL_{AD}	2.7V≦SA-ADC Ref Voltage *1≦3.6V	-4	-	4	LSB
		2.2V≦SA-ADC Ref Voltage *1＜2.7V	-6	-	6	
		1.8V≦SA-ADC Ref Voltage *1＜2.2V	-10	-	10	
		SA-ADC Ref Voltage = Internal Ref Voltage（V_{REFI}）	-15	-	15	
Differential Nonlinearity	DNL_{AD}	2.7V≦SA-ADC Ref Voltage *1≦3.6V	-3	-	3	
		2.2V≦SA-ADC Ref Voltage *1＜2.7V	-5	-	5	
		1.8V≦SA-ADC Ref Voltage *1＜2.2V	-9	-	9	
		SA-ADC Ref Voltage =Internal Ref Voltage（V_{REFI}）	-14	-	14	
Zero Scale Error	ZSE	RI≦1kΩ	-6	-	6	
Full Scale Error	FSE	RI≦1kΩ	-6	-	6	
A/D Reference Voltage	V_{REF}	-	1.8	-	V_{DD}	V
Internal Reference Voltage	V_{REFI}	-	1.5	1.55	1.6	
Conversion Time	t_{CONV}	2.2V≦V_{DD}≦3.6V	4.5	-	427	μs
		1.8V≦V_{DD}≦3.6V	18	-	427	

*1: It is the case that V_{DDIO_MCU}, P23/V_{REF} are selected as SA-ADC Reference Voltage.
Current flows to charge in capacitors during SA-ADC sampling. Set the output impedance of analog input resource to less than 1 kΩ for getting enougth sampling result. It is recommended to implement about 0.1μF capacitor to reduce noise.



○D/A Converter Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Resolution	n_{DA}	-	-	-	8	Bit
Conversion Frequency	tc	-	10	-	-	μs
Integral Nonlinearity	INL_{DA}	RL=4MΩ	-2	-	2	LSB
Differential Nonlinearity	DNL_{DA}	RL=4MΩ	-1	-	1	
Output Impedance	Ro	-	3	6	9	kΩ

○Reference Voltage Output Characteristics

(V_{DDIO_MCU}=2.6 to 3.6V, V_{SS} = 0V, Ta=-40 to +85 °C if not defined specifically.)

Item	Symbol	Condition	Standard			Unit
			Min.	Typ.	Max.	
Output Voltage Value	V_{REFO}	-	-	1.55	-	V
Output Impedance	R_{VREFO}	-	-	-	500	kΩ

○Flash Memory Operation Condition

(V_{SS}= 0V)

Item	Symbol	Condition		Standard	Unit
Operation Temperature (surroundings)	Ta	Data Area: Program/Erase		-40 to +85	°C
		Program Area: Program/Erase		0 to +40	
Operation Voltage	V_{DDIO_MCU}	Program/Erase		2.6 to 3.6	V
Programming cycle	CEPD	Data Area		10000	times
	CEPP	Program Area		100	
Erasing Unit	-	Block Erase	Program Area	16K	B
			Data Area	All Areas	
	-	Sector Erase	Program Area	1K	B
			Data Area	128	
Erasing Time(Max)	-	Block Erase/ Sector Erase		50	ms
Programming Unit	-	Program Area		4	B
		Data Area		1	
Programming Time(Max)	-	Program Area		80	μs
	-	Data Area		40	
Data Retention Years	YDR	-		15	Year

●RF

○Power Consumption

Values are under the condition of the master clock frequency = 36 MHz (Typ.).

Item	Symbol	Condition	Min.	Typ. (*2)	Max (*3)	Unit
Power Consumption (*1)	I_{DD_DSLP}	Deep Sleep mode (Not retaining Registers, all function halt)	-	0.1	14 (0.24)	µA
	I_{DD_SLP1}	Sleep mode 1 (*4)	-	0.45	33 (2.3)	µA
	I_{DD_IDLE}	Idle state (*5)	-	1.0	1.2	mA
	I_{DD_RX}	RX state (*6) (*7)	-	13.5	16	mA
	I_{DD_TX20}	TX state (20 mW) (*5) (*7) (*8)	-	40	49	mA
	I_{DD_XTAL}	Crystal oscillator circuit (*7)	-	0.3	0.4	mA

*1 Power consumption is sum of current consumption of all power supply pins.
*2 Typical value is a center value under the condition of VDDIO = 3.3 V, 25 ˚C.
*3 Value in parentheses indicates the maximum (reference) value at normal temperature.
*4 The definition of each sleep state is shown in the following table.

State	Register	FIFO	RC Osc. circuit state	Low clock timer
Sleep mode 1	Retain	Retain RXFIFO only	OFF	-
Sleep mode 2	Retain	Retain RXFIFO only	ON	ON

*5 Indicates a current value under the following LSI conditions: FSK mode, 100 kbps, frequency 920 MHz, TCXO used, LOW_RATE_EN([CLK_SET2:B0 0x03(0)]) = 0b1.
*6 Indicates a current value under following LSI conditions: Sigfox mode, frequency:920MHz, TCXO used.
*7 When using crystal oscillator, the operating current of crystal oscillator circuit is added to the power consumption except for the sleep and deep sleep modes.
*8 It is the current of CW mode.

○DC Characteristics

Values are under the condition of the master clock frequency = 36 MHz (Typ.).

Item	Symbol	Condition	Min.	Standard	Max.	Unit
Voltage input high	VIH1	Digital input Pin	V_{DDIO} x 0.75	−	V_{DDIO}	V
Voltage input low	VIL1	Digital input pin	0	−	V_{DDIO} x 0.18	V
Schmitt trigger high-level decision threshold value	VT+	RESETN、SDI、SCLK、SCEN、EXT_CLK、REGPDIN、GPIO1 pins	−	1.2	V_{DDIO} x 0.75	V
Schmitt trigger low-level decision threshold value	VT-	RESETN、SDI、SCLK、SCEN、EXT_CLK、REGPDIN、GPIO1pins	V_{DDIO} x 0.18	0.8	−	V
Input leakage current	IIH1	Digital input pin	-1	−	1	µA
	IIL1	Digital input pin	-1	−	1	µA
Tri-state output leakage current	IOZH	Digital input pin	-1	−	1	µA
	IOZL	Digital input pin	-1	−	1	µA
Voltage output high	VOH	IOH=-4mA	V_{DDIO} x 0.78	−	V_{DDIO}	V
Voltage output low	VOL	IOL=4mA	0	−	0.3	V
Regulator output voltage	MAIN_REG	REG_CORE pin all states except SLEEP state	1.4	1.5	1.6	V
	SUB_REG	REG_CORE pin Sleep state	1.2	1.5	1.65	V
Input capacitance	CIN	Input pin	−	6	−	pF
	COUT	Output pin	−	9	−	pF
	CRFIO	RF I/O pin	−	9	−	pF
	CAI	Analog input pin	−	9	−	pF

○RF Characteristics

The measurement point is at antenna end specified in the recommended circuits.

[TX characteristics]

Values are under the condition of the master clock frequency = 36 MHz (Typ.).

920MHz Band

Item	Condition	Min.	Standard (*1)	Max.	Unit
TX Power	20mW(13dBm) setting	9	13	17	dBm
Spurious emission level	13dBm, with LC trap circuit, 2^{nd} to 5^{th} Harmonics	-	-	-30	dBm

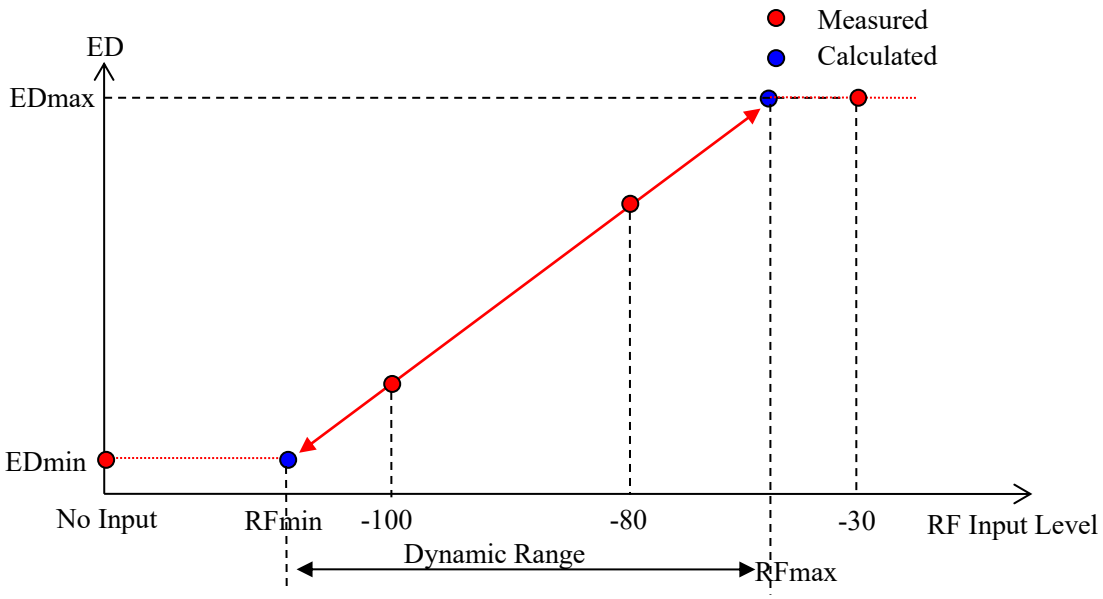
(*1) Typical value is a center value under the condition of VDDIO = 3.3 V, 25 ˚C.

[RX characteristics]

Values are under the condition of the master clock frequency = 36 MHz (Typ.).
920MHz Band

Item	Condition		Min.	Standard	Max.	Unit
Sensitivity (min)	100kbps mode BER<1% GFSK, 50kHz deviation	Ta= -30 to +75℃	—	-103	-94	dBm
		Ta= 15 to 30℃	—	-103	-96	
Adjacent channel interference (*1)	400kHz spacing, Ta=25℃, 100kbps mode Undesired wave: CW		20	37	—	dB
RX Blocking (*1)	2MHz offset, Ta=25℃, 100kbps mode		—	52	—	dB
	10MHz offset, Ta=25℃, 100kbps mode		—	62	—	dB
Minimum energy detection level (ED value)	RFmin in RSSI characteristics diagram (*2) 100kbps, Channel filter band = 200kHz setting		—	-105	-96	dBm
energy detection range	Dynamic range in RSSI characteristics diagram (*2)		55	65	—	dB
Spurious emission			—	—	-54	dBm

*1. The measurement conditions on the interference-related characteristics are as follows.
Using the desired input level as [Level achieving BER = 1 % (= reference sensitivity) + 3 dB], the level achieving BER = 1 % is searched by varying the undesired wave level and defined as U/D [dB] = (Undesired wave level) - (Level achieving BER = 1 %).
*2. The following diagram shows the RSSI characteristics.



○RC Oscillator Circuit Characteristics

ML7456N has 32 kHz clock generation function for timer. For details, please refer to “LSI state transition control/SLEEP setting” section.

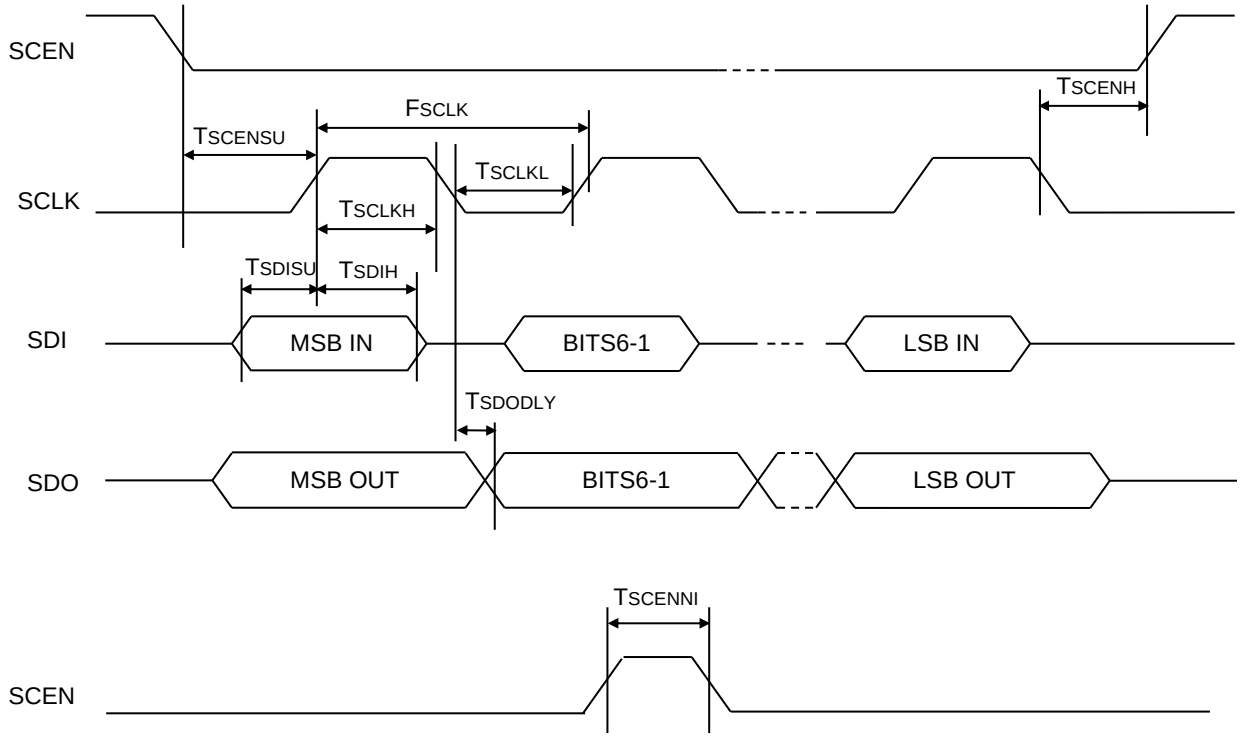
Item	Symbol	Condition	Min.	Standard	Max.	Unit
RCOSC oscillation frequency	F_{RCOSC}	After trimming	27	32	38	kHz
RCOSC stable time	T_{RCOSC}		—	—	100	ms

○SPI Interface Characteristics

Item	Symbol	Condition	Min.	Standard	Max.	Unit
SCLK clock frequency	F_{SCLK}	Load capacitance CL=20pF	0.032	2	16	MHz
SPI clock input duty ratio	D_{SCLK}		45	50	55	%
SCEN input setup time	T_{SCENSU}		30	-	-	ns
SCEN input hold time	T_{SCENH}		30	-	-	ns
SCLK high pulse width	T_{SCLKH}		31	-	-	ns
SCLK low pulse width	T_{SCLKL}		31	-	-	ns
SDI input setup time	T_{SDISU}		5	-	-	ns
SDI input hold time	T_{SDIH}		15	-	-	ns
SCEN negate period	T_{SCENNI}		200	-	-	ns
SDO output delay time	T_{SDODLY}		0	-	25	ns

[Note]

All timing measurement conditions are V_{DDIO} * 20 % level and V_{DDIO} * 80 % level.

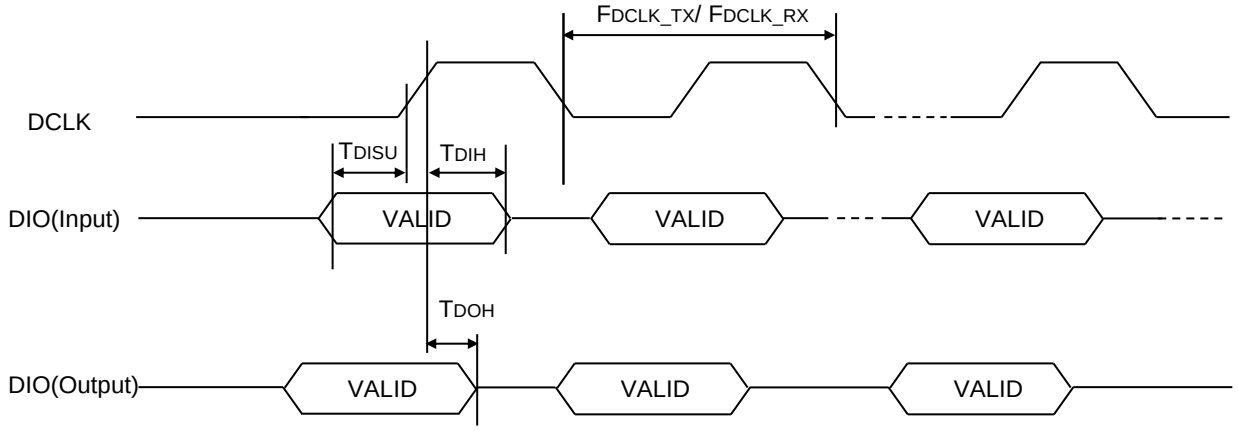


○TX/RX Data Interface Characteristics

Item	Symbol	Condition	Min.	Standard	Max.	Unit
DIO input setup time	T_{DISU}	Load capacitance CL=20pF	1	-	-	µs
DIO input hold time	T_{DIH}		0	-	-	ns
DIO output hold time	T_{DOH}		20	-	-	ns
DCLK frequency accuracy (*1) (TX)	F_{DCLK_TX}		Negative clock frequency deviation	-	Positive clock frequency deviation	kHz
DCLK frequency accuracy (*2) (RX)	F_{DCLK_RX}		-30	-	+30	%
DCLK output duty ratio (TX)	D_{DCLK_TX}		45	-	55	%
DCLK output duty ratio (RX)	D_{DCLK_RX}		30	-	70	%

*1 If there is no decimal point generated in the TX data rate setting calculation (see [TX_RATE_H: B1 0x02]), the maximum and minimum values of TX DCLK frequency become the master clock frequency deviation.
*2 Max.and min.of RX DCLK frequency indicates jitter amount of recovered clock from RX signal upon synchronization established.

[Note]
All timing measurement conditions are VDDIO * 20 % level and VDDIO * 80 % level.



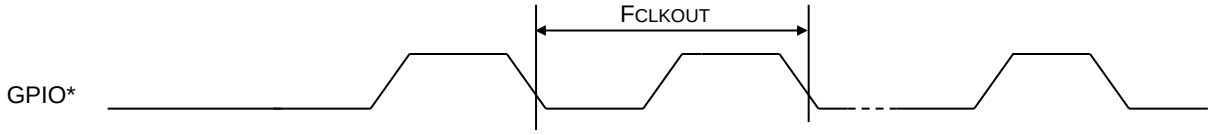
○Clock Output Characteristics

ML7456N has clock output function. DMON_SET([MON_CTRL: B3 0x27(3-0)]) and [GPIO*_CTRL: B0 0x28-0x2A] are used for control. Upon reset, clock is output through GPIO1 pin.

Item	Symbol	Condition		Min.	Standard	Max.	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20pF		0.0088	3	36(*2)	MHz
Clock output duty ratio (*1)	D_{CLKOUT}		12MHz	33	-	67	%
			Other than above	47	50	53	%

*1 Duty cycle is High:Low = 1:2 , only when 8MHz is used. [CLK_OUT: B0 0x03].
*2 Indicates the frequency with the setting of LOW_RATE_EN([CLK_SET2: B3 0x01(0)] = 0b0.

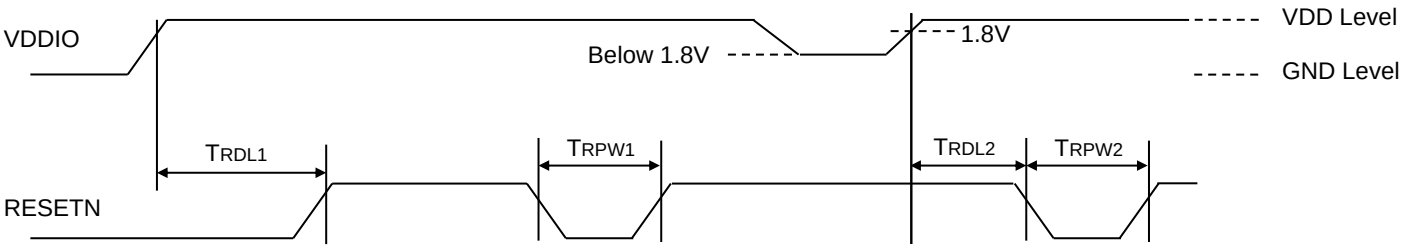
[Note]
All timing measurement conditions are VDDIO * 20 % level and VDDIO * 80 % level.



○Reset Characteristics (Internal Pins)

Item	Symbol	Condition	Min.	Standard	Max.	Unit
RESETN release delay time (power on period)	T_{RDL1}	All power pins After Power On	0.5	-	-	ms
RESETN pulse period (start-up from VDDIO=0V)	T_{RPW1}		0.5	-	-	ms
RESETN pulse period 2 (*1) (start-up from VDDIO≠0V)	T_{RPW2}		0.5	-	-	ms
RESETN input delay time	T_{RDL2}	After VDDIO>1.8V	1	-	-	µs

[Note]
All timing measurement conditions are V_{DDIO} * 20 % level and V_{DDIO} * 80 % level.

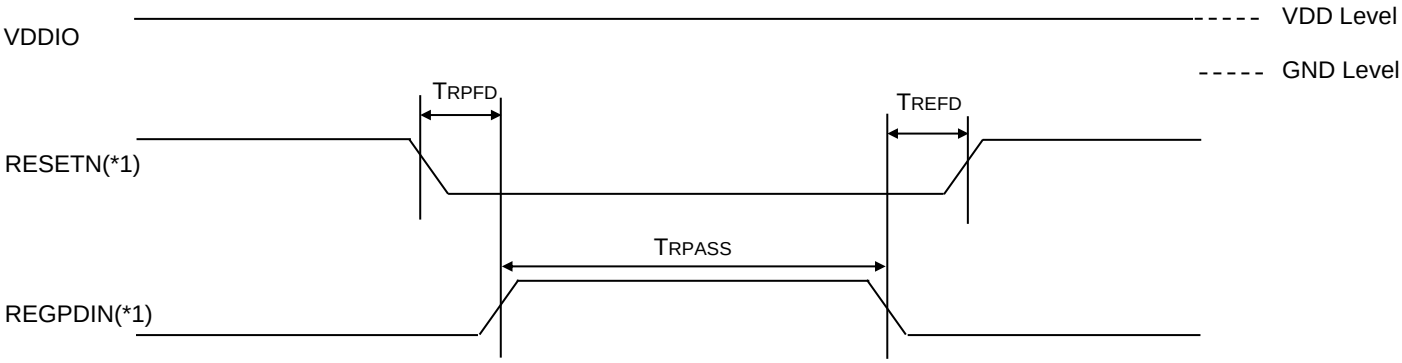


(*1) When starting from VDDIO ≠ 0 V, a pulse must be sent to RESETN after VDDIO exceeds 1.8 V.
(*2) RESETN is a internal pin. MCU (Software) need to control the above timing.

○Deep Sleep Mode Characteristics

Item	Symbol	Condition	Min.	Standard	Max.	Unit
REGPDIN rising edge delay time	TRPFD	VDDIO="H"	0	-	-	µs
REGPDIN assert time	TRPASS	VDDIO="H"	0.3	-	-	ms
RESETN input delay time	TREFD	VDDIO="H"	0.5	-	-	ms

[Note]
All timing measurement conditions are VDDIO * 20 % level and VDDIO * 80 % level.

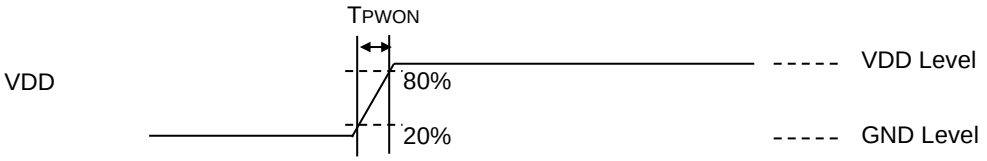


(*1) REGPDIN, RESETN is a internal pin in PKG. MCU (Software) need to control the above timing.

○Power-on Characteristics

Item	Symbol	Condition	Min.	Standard	Max.	Unit
Power-on time difference	TPWON	Power on state (all power pins)	-	-	5	ms

[Note]
All timing measurement conditions are VDDIO * 20 % level and VDDIO * 80 % level.



■Functional Description

■MCU

●CPU and Memory Space

ML62Q1532 has LAPIS Technology's original 16-bit CPU nX-U16/100 (A35 core), the multiplier/divider in the coprocessor, flash memory in the program memory space, and RAM and data flash in the data memory space. In addition, it has the built-in remap function that remaps a 4 Kbyte area in the program memory space.

●Reset Function

ML7456N has a function to reset the CPU, peripheral circuits and other hardware due to the causes described in Table 3-1. This chapter describes the system reset mode, reset input pin reset and power-on reset (POR). See reference chapters in Table 3-1 for other causes of resets. See Table 3-2 for the availability of resets for each cause.

Table 3-1 Reference for Details of Causes of Resets

Cause	Reference (ML62Q1000 Series User's Manual)
Reset input pin reset (pin reset)	This chapter
Power-On Reset (POR)	This chapter
Watchdog timer (WDT) overflow reset	Chapter 10 Watchdog Timer
Watchdog timer (WDT) invalid clear reset	Chapter 10 Watchdog Timer
Voltage Level Supervisor reset (VLS0 reset)	Chapter 22 Voltage Level Supervisor
RAM parity error reset	Chapter 29 Safety Function
Unused ROM area access reset	Chapter 29 Safety Function
CPU reset by BRK instruction execution (when ELEVEL is 2 or higher)	"nX-U16/100 Core Instruction Manual"
Individual reset to the peripheral circuits(Block reset)	Chapter 4 Power Management
One-time reset to the all peripheral circuits and port controller (SOFTR reset)	Chapter 4 Power Management

○Features

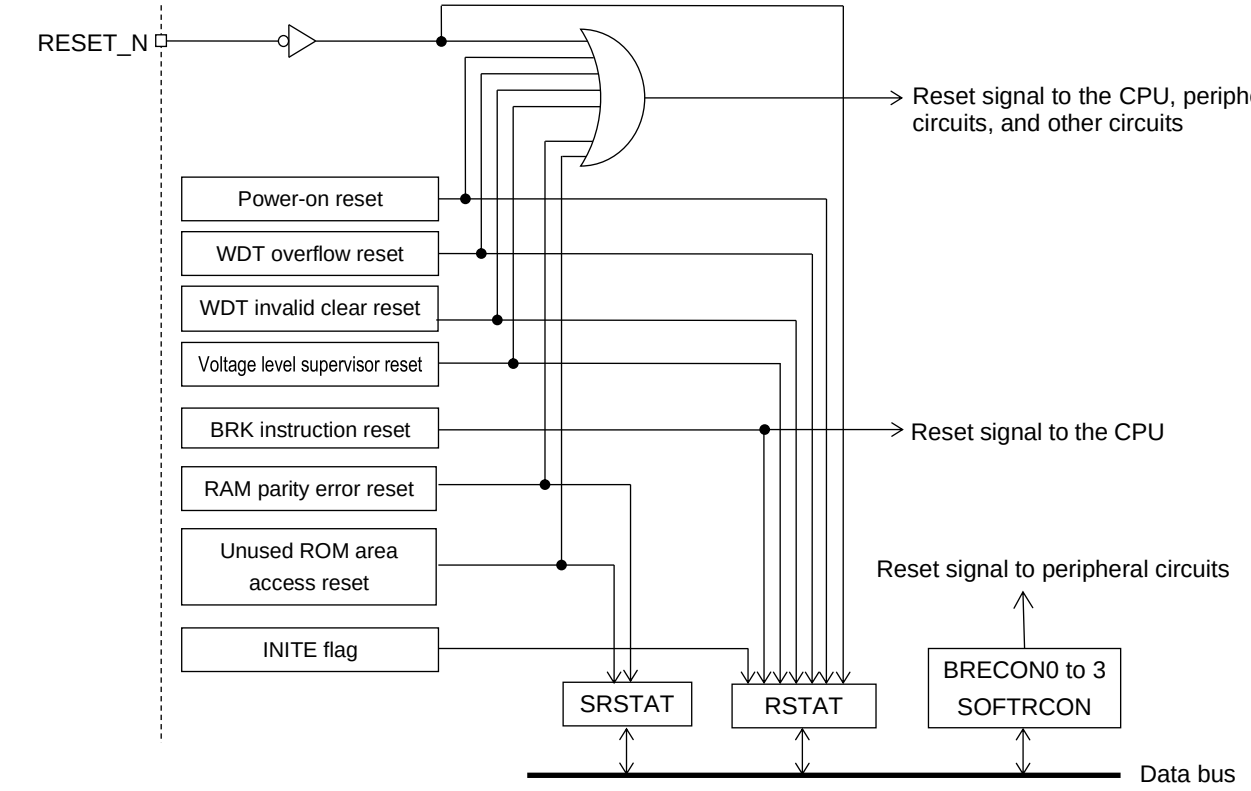
Each reset can uniquely be managed depending on its cause as this function contains following features to identify the cause in an early stage.

- Reset status register (RSTAT) to indicate the cause of the reset
- Reset status register (SRSTAT) to indicate the cause of the safety function reset

In addition, it has the INITE flag function to detect abnormal start-up of the LSI.

○Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT : Reset status register
SRSTAT : Safety function reset status register
BRECON 0 to 3 : Block reset control register 0 to 3
SOFTRCON : Software reset control register
Hardware(Other circuits) : Power supply and oscillation circuits, start control part, etc.

Figure 3-1 Configuration of Reset Generation Circuit

○List of Pins

Pin name	I/O	Function
RESET_N	I	Reset input pin

●Power Management

ML62Q1532 has four power management modes to save the current consumption.

- HALT mode : Stop the CPU and peripherals continue to work.
- HALT-H mode : Stop the CPU, peripherals continue to work with low-speed clock only,
- forcely stop high-speed clock and forcely start the high-speed clock after releasing the mode.
- STOP mode : Stop the CPU, peripheral circuits, low-speed clock and high-speed clock.
- STOP-D mode : Stop the CPU, peripheral circuits, low-speed clock and high-speed clock.
  Internal logic voltage(REG_CORE_MCU) is minimized to lower the current consumption.

○Features

- Stop code acceptor qualifies for entering STOP mode and STOP-D mode
- Data of RAM and SFR are retained even in the STOP-D mode
- Clock supply is control-able peripheral by peripheral to reduce the current consumption, by block clock control registers
- Reset is control-able peripheral by peripheral by block reset control registers

○Configuration

Figure 4-1 shows the transition diagram of the operating state.
The bit symbols in the figure are assigned to the standby control register (SBYCON).

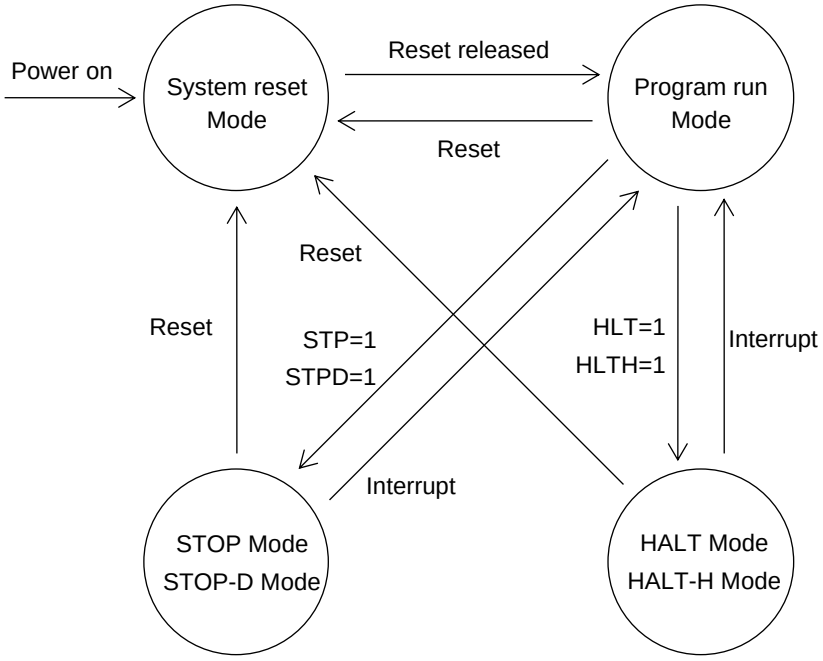


Figure 4-1 Operating State Transition Diagram

●Interrupt

ML62Q1532 has the non-maskable interrupt, maskable interrupts and the software interrupt (SWI).
For details of each interrupt, see the corresponding Chapters.
See Chapter 29 "Safety Function" for the MCU status interrupt.
See "Table 1-4 Main Function List" for ML62Q1300 group, "Table 1-5 Main Function List" for ML62Q1500/ML62Q1800 group and "Table 1-6 Main Function List" for ML62Q1700 group in the Chapter 1 to confirm the presence/absence of function in each product.

○Features

- Master Interrupt Enable (MIE) flag enables or disables collectively the all maskable interrupts. For more details about MIE, see "nX-U16/100 Core Instruction Manual".
- Each maskable interrupt has the enable flag in the register IE0 to IE7.
- The occurrence of interrupt request is confirmable by checking the request flag in IRQ registers.
- The occurrence of interrupt is maskable by setting each request flag by the software in IRQ registers.
- Four interrupt levels are available for each maskable interrupt.

●Clock Generation Circuit

The clock generation circuit generates following kinds of clock and supplied them to the CPU or the peripheral circuits.

Table 6-1 Clocks generated by the clock generation circuit

Clock Name	Symbol	Description
Low-speed clock	LSCLK	Low speed clock for peripherals (32.768kHz)
Simplified RTC clock	RTCCLK	Low speed clock for the simplified RTC (32.768kHz)
High-speed clock	HSCLK	High speed clock for peripherals (Max. 24MHz)
CPU clock	CPUCLK	CPU operating clock (32.768kHz or Max. 24MHz): The maximum frequency depends on the CPU operation mode(See Table 6-2)
System clock	SYSTEMCLK	System control clock: The frequency is the same as CPU clock.
Low-speed output clock	OUTLSCLK	Low speed output from a general port (32.768kHz)
High-speed output clock	OUTHSCLK	High speed output from a general port (Max. 12MHz)
WDT clock	WDTCLK	Clock for the watch dog timer (Approx 1kHz)

○Features

- Low-speed clock generation circuit
  - Low-speed RC oscillation circuit
  - Adjustable to ±1% by using the frequency adjustment function ($V_{DDIO\_MCU} \geq 2.6V$)
  - A crystal resonator is connectable*1
  - In case the low-speed crystal oscillation stopped, the clock is automatically switched to the low-speed RC oscillation (clock backup function).*1
  - A low-speed external clock is available to input to XT1 pin*1
  - The crystal oscillation clock and the low-speed external clock each is continuously supplied during the reset input pin reset.*1
- Simplified RTC clock
  - Operating by the low-speed clock
- High-speed oscillation circuit
  - PLL oscillation mode (16 MHz or 24 MHz is choosable for the PLL reference frequency by the code option)
  - High-speed clock wake-up time is choosable
- WDT clock
  - RC1K oscillation circuit
  - The RC1K clock or the 1.024 kHz divided from the LSCLK is choosable by the code option.

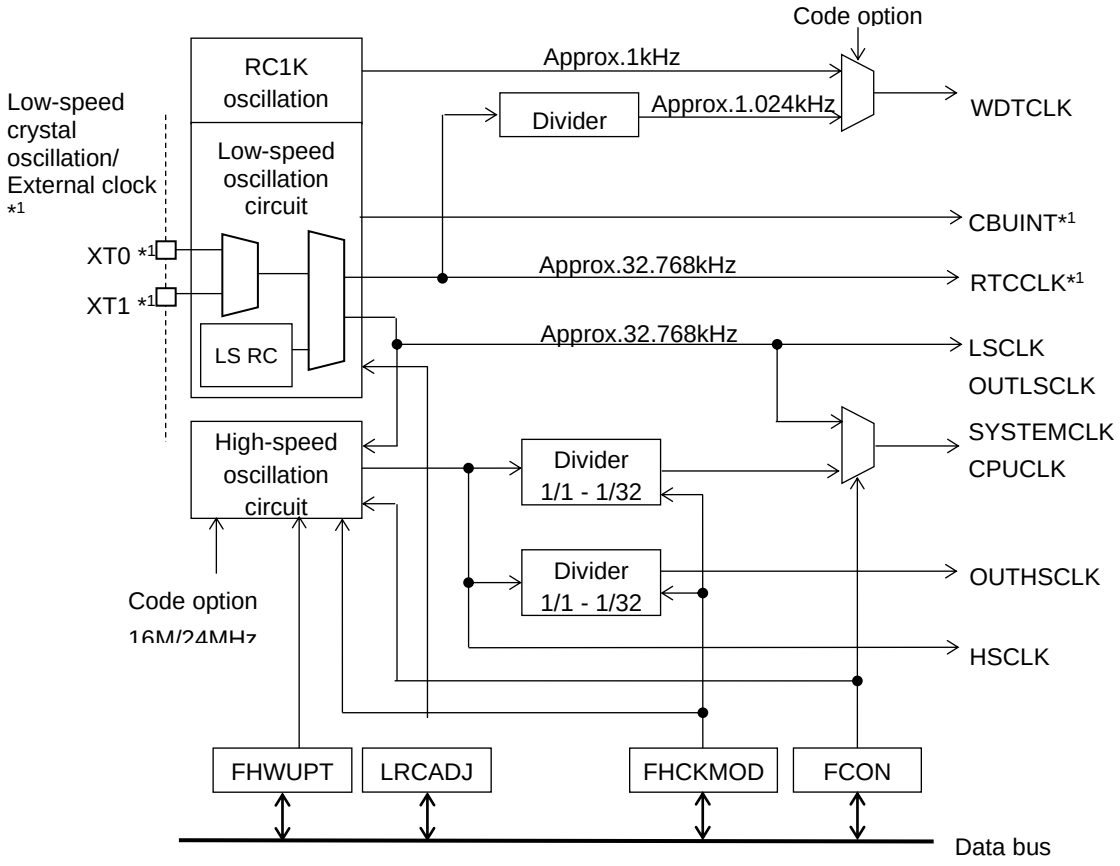
Table 6-2 shows relation of CPU operation mode and PLL oscillation reference frequency.
The CPU operation mode and the PLL oscillation reference frequency are choosable by the code option. See Chapter 26 "Code Option" for more details.

Table 6-2 CPU operation mode and PLL oscillation reference frequency

PLL oscillation reference frequency	Maximum operating frequency		
	SYSTEMCLK		HSCLK
	Wait mode	No wait mode	
24MHz	24MHz	6MHz	24MHz
16MHz	16MHz	8MHz	16MHz

○Configuration

Figure 6-1 shows the configuration of the clock generation circuit.
Table 6-3 shows the list of operation clocks for each function.



FHCKMOD : High-speed clock mode register
FCON : Frequency control register
FHWUPT : High-speed clock wake-up time setting register
LRCADJ : Low-speed RC oscillation frequency adjustment register
CBUINT* : Clock backup interrupt register

*1 : Available except for ML62Q1300 group

Figure 6-1 Configuration of Clock Generation Circuit

[Note]

- **After the power-on or the system reset, LSCLK (32.768 kHz) is initially chosen as SYSTEMCLK.**

Table 6-3 Operating clock list in each function

Function	System clock or CPU clock SYSTEMCLK/ CPUCLK	Low-speed clock LSCLK	Simplified RTC clock RTCCLK	High speed clock HSCLK	WDT clock WDTCLK
CPU	●	–	–	–	–
RAM	●	–	–	–	–
Watchdog timer	●	–	–	–	●
External interrupt control	●	●*1	–	●*1	–
Low speed time base counter	●	●	–	–	–
16-bit timer	●	●	–	●	–
Functional timer	●	●	–	●	–
Serial communication unit	●	●	–	●	–
I^2C bus unit	●	●	–	●	–
I^2C bus master	●	–	–	●	–
Buzzer	●	●	–	–	–
SA type A/D converter	●	●	–	●	–
D/A converter	●	–	–	–	–
Analog comparator	●	●*1	–	●*1	–
Voltage Level Supervisor(VLS）	●	●*1	–	●*1	–
Simplified RTC	●	–	●	–	–
DMA controller	●	–	–	–	–
CRC calculator	●	–	–	–	–
Flash (BGO operation)	●	–	–	●	–

●: The clock is supplied -: The clock is Not supplied

*1 : The clock is supplied for start control or sampling

○List of Pins

The output pins of the high-speed/low-speed clocks are assigned to the shared function of general purpose ports.
For details of pin assignment and the shared function of general purpose ports, see the list of pins.

Pin Name	I/O	Function
OUTLSCLK	O	Low-speed clock output
OUTHSCLK	O	High-speed clock output
XT0	I	Low-speed crystal resonator connect pin
XT1	O/I	Low-speed crystal resonator connect pin / Low-speed external clock input pin

●Low Speed Time Base Counter

The low speed time base counter enables following functions.

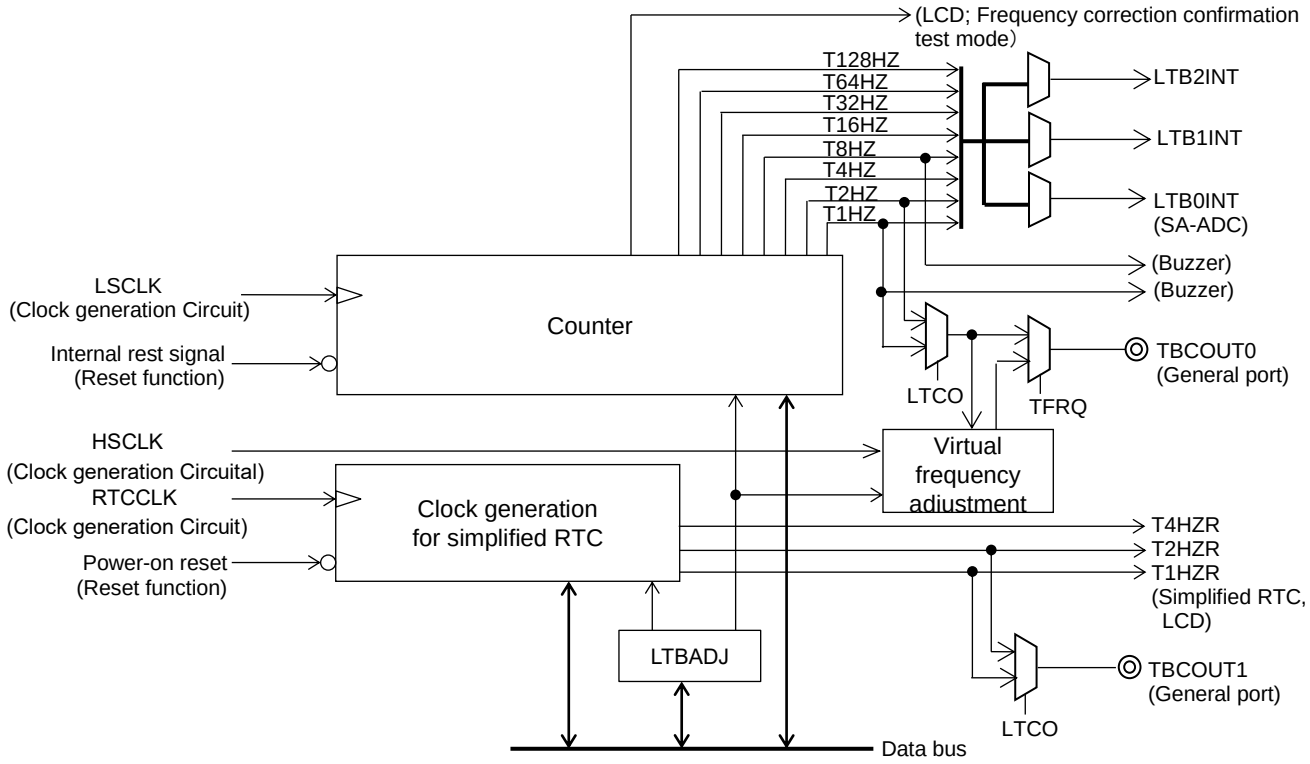
- Generate periodical interrupt requests
- Output periodical pulse signals to the general ports
- Adjust the frequency of simplified RTC clock

○Features

- Generate eight frequency (128Hz, 64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz and 1Hz) of pulse signals by dividing the low-speed clock (LSCLK)
- Three interrupt requests can be chosen among eight periodical interrupt requests
- The 1Hz or 2Hz signal can be output from general ports
- An interrupt request (LTB0INT) can be used for a trigger event source of the Successive Approximation type A-D Converter.
- The clock frequency adjust function
  - Allows to adjust in a range approx.-488ppm to +488ppm with the resolution approx.0.119ppm.
  - Two confirmation methods with the low-speed clock or high-speed clock.
- The 1Hz or 2Hz signal is used for the simplified RTC clock

○Configuration

Figure 7-2 shows the configuration of the low speed time base counter on ML7456N.



LTBADJ	:	Low speed time base counter frequency adjustment register
T1HZ to T128HZ	:	Time base counter output signals
LTB2INT	:	Low speed time base counter 2 interrupt request
LTB1INT	:	Low speed time base counter 1 interrupt request
LTB0INT	:	Low speed time base counter 0 interrupt request
T1HZR to T4HZR	:	Simplified RTC time base counter output signals

Figure 7-2 Configuration of Low Speed Time Base Counter

○List of Pins

The output pins of the low speed time base counter are assigned to the shared function of genral purpose ports.

Signal name	I/O	Function
TBCOUT0	O	The virtual frequency adjustment output signal or the low speed time base counter output signal
TBCOUT1	O	Hz/2Hz clock for the Simplified RTC

Table 7-1 shows the list of the general purpose ports and the register setting.

Table 7-1 Low speed time base counter function port and the register setting

Pin Name	Shared Port		Setting Register	Setting Value
TBCOUT0	P01	6th function	P0MOD1	0101_XXXX*1
	P17	6th function	P1MOD7	0101_XXXX*1
TBCOUT1	P01	7th function	P0MOD1	0110_XXXX*1
	P20	6th function	P2MOD0	0101_XXXX*1

*1: XXXX determines the port output condition

XXXX	Port output condition
0010	CMOS output
1010	Nch open drain (without pull-up)
1111	Nch open drain (with pull-up)

●16-Bit Timer

The 16-bit timer enables following functions.

- Generate periodical interrupts in an arbitrary period
- Generate one shot interrupts in an arbitrary period
- Output pulse signals with an arbitrary frequency to the general ports
- Output one shot pulse signals to the general ports
- Count up the rising edges of the external input signal

ML62Q1532 equips 6 channels (n=0 to 6)16-bit timers.

○Features

- Two timer modes and two operation modes are available

Timer mode	Operation mode	Description
16-bit timer mode	Repeat mode	Count-able to the max. 0xffff Repeat the specified operation until stop by the software.
	One shot mode	Count-able to the max. 0xffff Run the specified operation once and stop it.
8-bit timer mode	Repeat mode	Count-able to the max. 0xff Repeat the specified operation until stop by the software.
	One shot mode	Count-able to the max. 0xff Run the specified operation once and stop it.

- One channel of 16-bit timer is configurable as two channels of 8-bit timer
- LSCLK or HSCLK can be chosen for the timer clock
- A timer clock, a divided time clock or an external input can be chosen for the count clock.
- A timer interrupt request is generated when the value of the timer counter register value coincides with that of the 16-bit timer n data register
- A port output is reversed when the value of the timer counter register value coincides with that of the 16-bit timer n data register
- The initial value of the port can be chosen by a register.

○Configuration

Figure 8-1 shows configuration of the 16-bit timer and Figure 8-2 shows configuration of the 8-bit timer

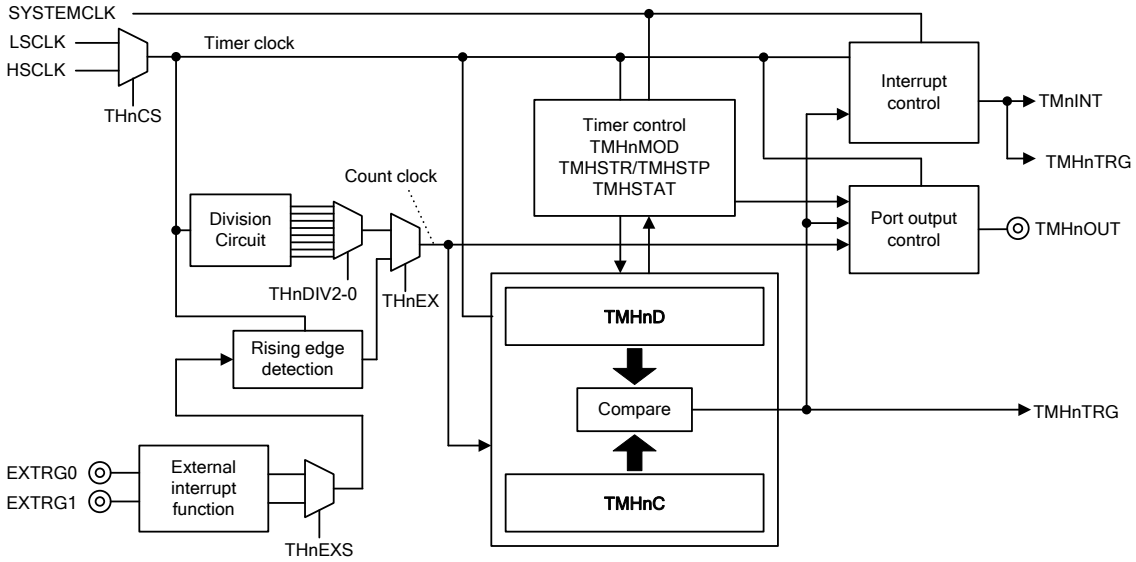


Figure 8-1 Configuration of the timer in 16-bit timer mode

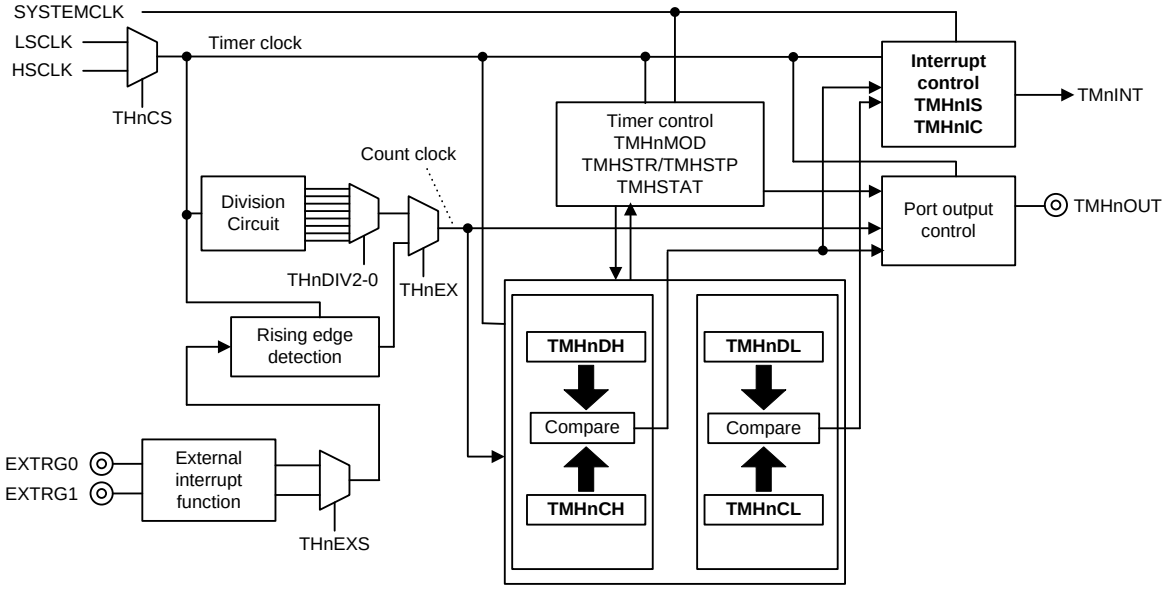


Figure 8-2 Configuration of the timer in 8-bit timer mode

TMnINT	: 16-bit timer n interrupt request	TMHnTRG	: 16-bit timer n trigger
EXTRG0	: EXI0 pin input (come through the noise filter of the external interrupt function)		
EXTRG1	: EXI1 pin input (come through the noise filter of the external interrupt function)		

TMHnD	: 16-bit timer n data register	TMHnC	: 16-bit timer n counter register
TMHnDH	: 16-bit timer n data register upper 8 bit	TMHnCH	: 16-bit timer n counter register upper 8 bit
TMHnDL	: 16-bit timer n data register lower 8 bit	TMHnCL	: 16-bit timer n counter register lower 8 bit

[Note]

- **When the 16-bit timer is used as two channels of 8-bit timer, the same clock settings and interrupts are applied.**
- **In the 8-bit timer mode, the TMHnOUT outputs the comparison result of the upper side ("TMHnDH" and "TMHnCH").**
- **Choose the 16-bit timer mode when using the 16-bit timer DMA request or SA-ADC trigger.**

○List of Pin

The I/O pins of the 16-bit timer are assigned to the shared function of the general ports.

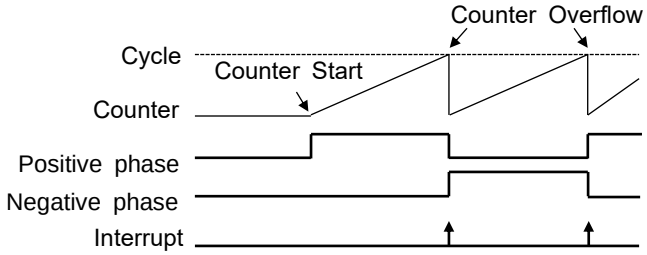
Pin name	I/O	Description
EXTRG0	I	External trigger input 0
EXTRG1	I	External trigger input 1
TMHnOUT	O	16-bit timer channel n output When used in an 8-bit timer, only the upper 8-bit timer can output the signal.

●Functional Timer

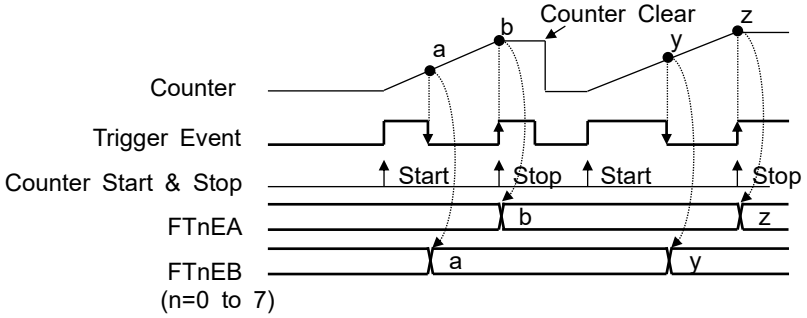
The Functional timer enables following functions in four operation modes (TIMER/CAPTURE/PWM1/PWM2).

ML62Q1532 equips 6 channels (n=0 to 5) Functional Timers.

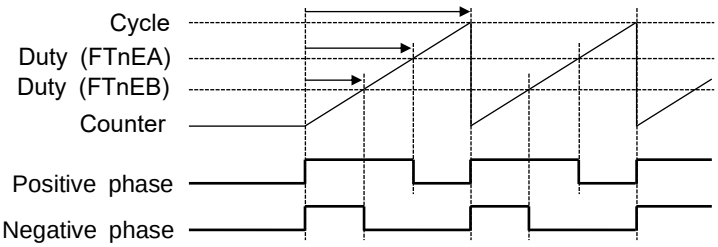
TIMER mode:
In this mode, the Functional Timer generates pulse signals, levels of which are reversed in sync with the counter start and the counter overflow. Also, it generates the interrupt when the counter overflows.



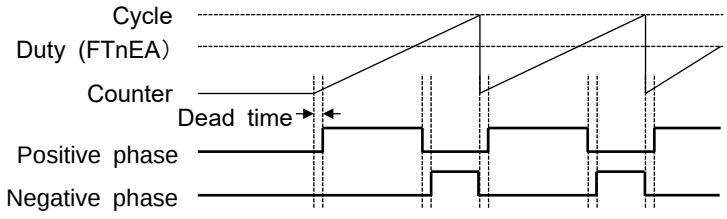
CAPTURE mode:
In this mode, the Functional Timer stores the value of counter into FTnEA register at the rising edge of a trigger event, into FTnEB register at the falling edge of a trigger event.



PWM1 mode:
In this mode, the Functional Timer generates two types of PWM waveform that have the same cycle and the start timing.
The setting value of FTnEA register makes the duty of the positive phase output and the setting value of FTnEB register makes the duty of the negative phase output.



PWM2 mode:
In this mode, the Functional Timer generates the complimentary PWM waveform of which the positive phase output and the negative phase output works exclusively. The setting of FTnEA register makes the duty of the positive phase output. Also, a dead time can be configured by setting FTnDT register.

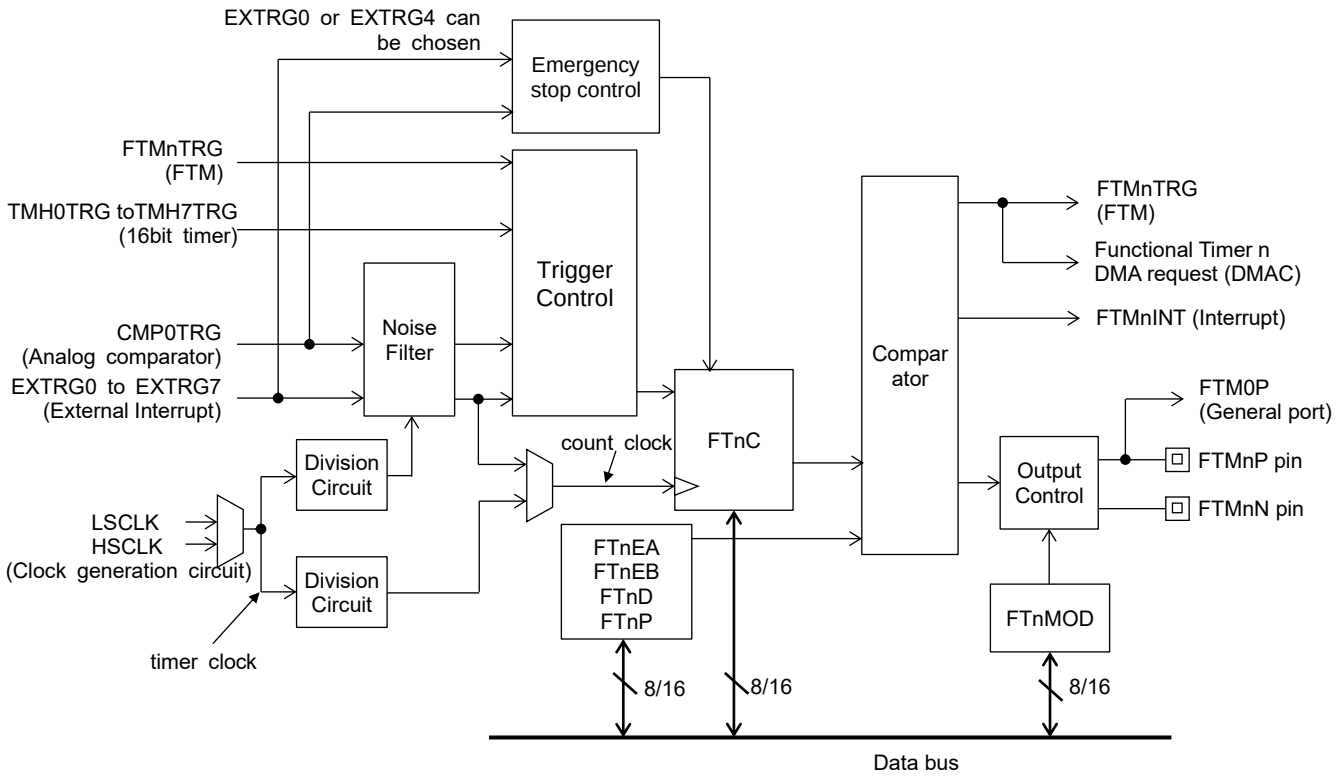


○Features

- The Timer/Capture/PWM functions using the 16-bit counter
- The count clock can apply the LSCLK/HSCLK divided by 1 to 128 and the external clock input
- The timer output signal can be switched (Positive logic or Negative logic)
- Generate a cyclic interrupt, a duty interrupt and a coincident interrupt with the setting value
- One-shot mode
- Start/stop/clear the timer by an external trigger input or a timer interrupt request(event triggers)
- Emergency stop and emergency stop interrupt by an external trigger input
- Two types of PWM output with the same cycle and different duties, and complementary PWM output with the dead time
- Input signal duty/cycle measurement by the capture function
- Chosen interrupt source can be notified
- DMA request signal can be used

○Configuration

Figure 9-1 shows the configuration of the FTM circuit.



FTnEA	: FTMn event A register
FTnEB	: FTMn event B register
FTnDT	: FTMn dead time register
FTnP	: FTMn cycle register
FTnC	: FTMn counter register
FTnMOD	: FTMn mode register

FTMnTRG	: Functional Timer n trigger
EXTRG0 to EXTRG 7	: External trigger n / external clock
CMP0TRG	: Analog comparator 0 trigger
TMH0TRG to TMH7TRG (n=0 to 7)	: 16-bit Timer n trigger

Figure 9-1 Configuration of the Functional Timer

○List of Pins

The I/O pins of the Functional timer are assigned to the shared function of the general ports.

Pin name	I/O	Description
EXTRG0 to EXTRG7	I	External trigger 0 to 7 / External clock 0 to 7
FTMnP	O	Functional timer channel n output P
FTMnN	O	Functional timer channel n output N

（n=0 to 7）

●Watchdog Timer

The watchdog timer (WDT) is equipped with the following functions and can detect the runaway state of program or the undefined state of the CPU by generating an interrupt or reset when an abnormality occurs.

- If the counter is not cleared for more than a certain time period in program operation and overflows, the WDT interrupt is generated in the first overflow and the WDT reset in the second overflow (if the window function is disabled).
- If the counter is not cleared for more than a certain time period in program operation and overflow occurs, the WDT reset is generated in the first overflow (if the window function is enabled).
- If the counter is cleared in the unexpected time period, the WDT invalid clear reset is generated (if the window function is enabled).

The window function refers to the function through which "the time period during which WDT counter clear is enabled" = "the time period during which the window is opened" and
"the time period in which WDT counter clear is disabled" = "the time period in which the window is closed" can be set.

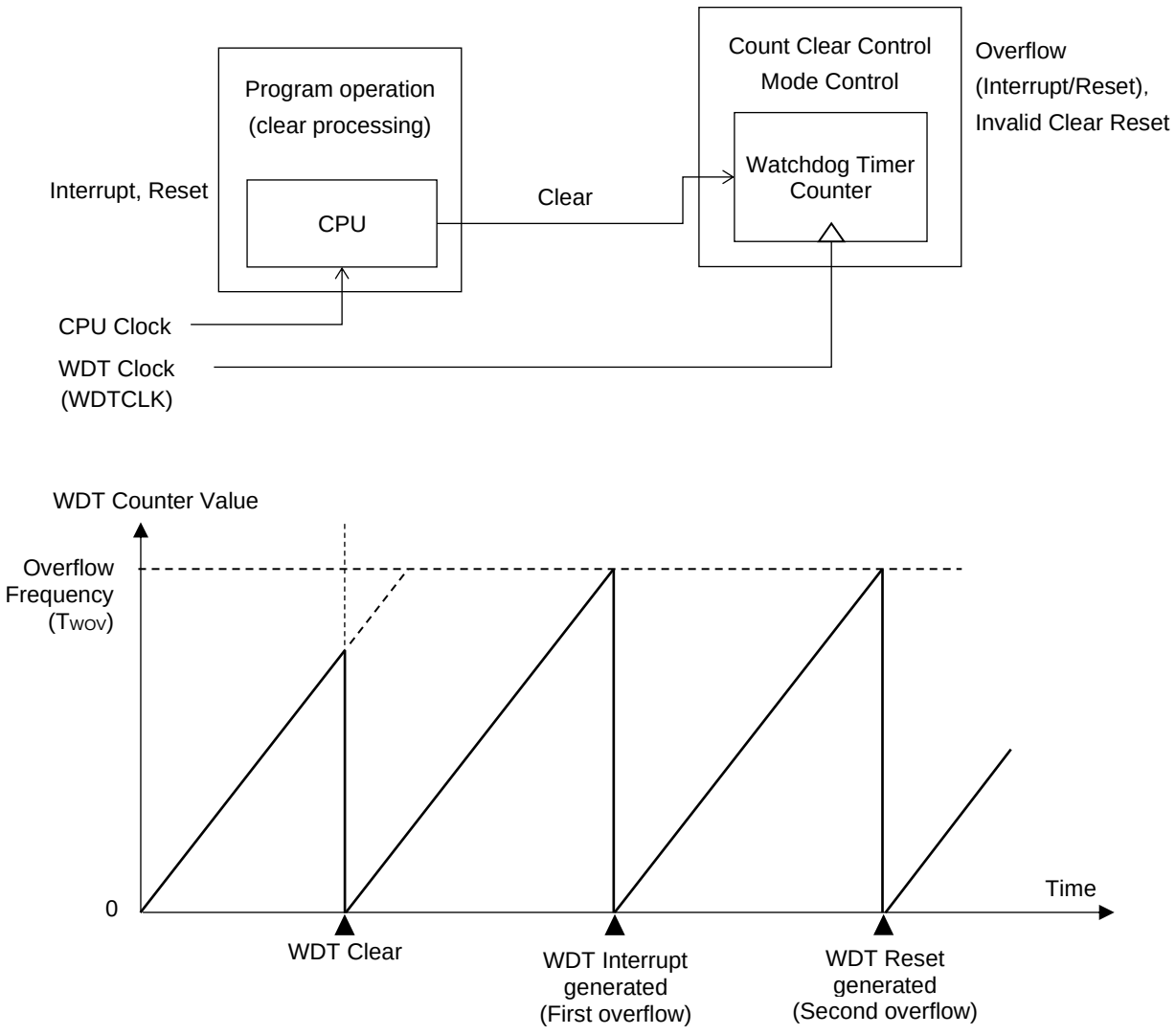


Figure10-1 Watchdog Timer Overview (With the Window Function Disabled)

○Features

- Eight types of overflow periods can be chosen (7.8 ms, 15.6 ms, 31.3 ms, 62.5 ms, 125 ms, 500 ms, 2 s, or 8 s)
- Two types of use are available:
  ・Window function disabled mode
  The WDT counter can always be cleared. The WDT interrupt is generated when the first counter overflow occurs, and the WDT reset is generated when the second counter overflow occurs.
  ・Window function enabled mode
  The periods during which WDT counter clear is enabled and disabled respectively can be set. The WDT reset is generated when the first counter overflow occurs, and the WDT invalid clear reset is generated when the counter is cleared in the period during which WDT counter clear is disabled.

Table 10-1 Watchdog Timer Operation Modes

Mode	Overflow		WDT invalid clear reset
	First	Second	
Window function disabled mode	Interrupt	Reset	Window function disabled mode
Window function enabled mode	Reset	-	Window function enabled mode

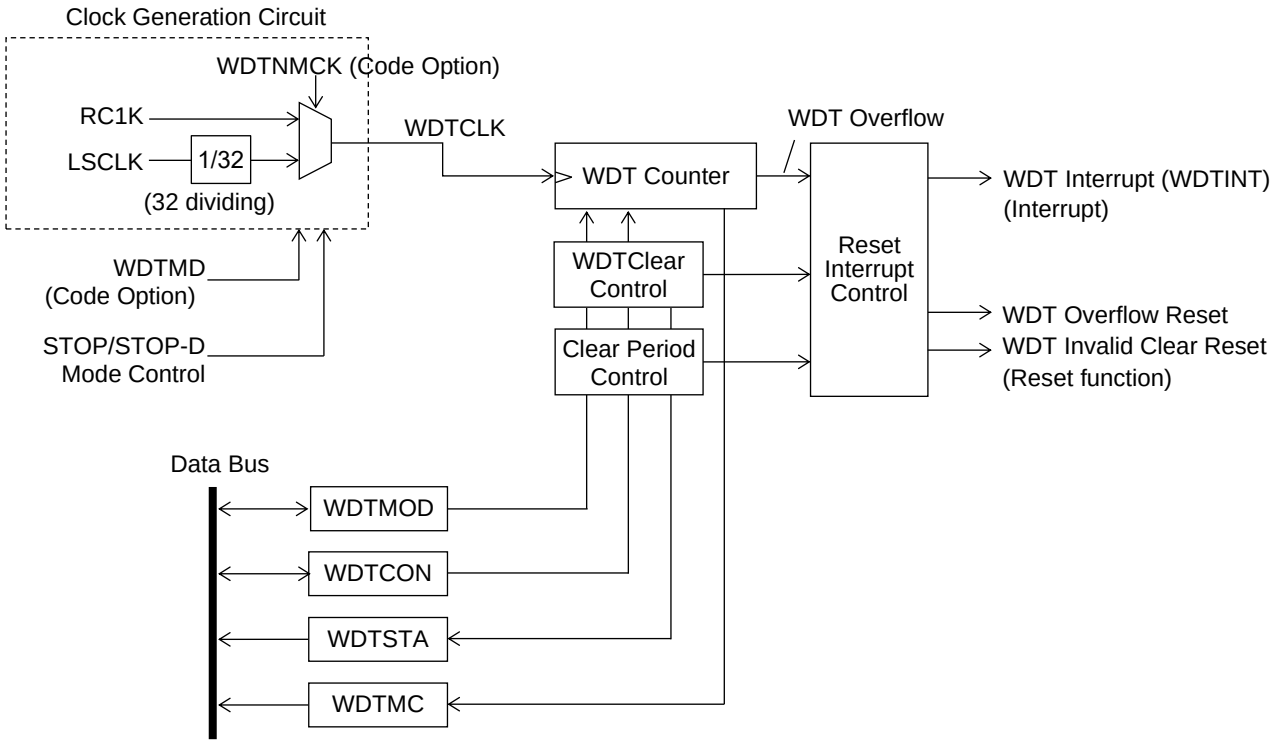
- The following items can be chosen by the code option. See the Chapter 26 "Code Option" for details of the code option.
  ・Enabling/disabling the WDT timer operation
  ・Operation clock of the WDT counter (32 dividing of low-speed clock LSCLK, WDTCLK RC1K oscillation)

[Note]

- **WDT is the function used to monitor the CPU runaway. Its function as an ordinary timer is not guaranteed.**
- **The watchdog timer is undetectable to all the abnormal operations. Even if the CPU loses control, the watchdog timer is undetectable to the abnormality in the operation state in which the WDT counter is cleared. It is recommended that the WDT counter is cleared at one place in the main loop of the program as a fail-safe.**
- **WDT can be operated based on the clock independent of the system clock by using RC1K oscillation for the WDTCLK, resulting in further improvement of safety. However, it is recommended to choose LSCLK if high accuracy of the frequency is required, since the RC1K oscillation is less accurate than the LSCLK.**

○Configuration

The following diagram shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register
WDTMC : Watchdog timer counter register
WDTSTA : Watchdog timer status register

Figure 10-2 Configuration of Watchdog Timer

●Serial Communication Unit

ML62Q1532 has two types of the serial communication function.

- 8-bit/16-bit synchronous serial port (SSIO)
- Asynchronous serial interface UART (Universal Asynchronous Receiver Transmitter)

ML62Q1532 equips 2 channels Serial Communication Units.

○Features

Two serial communication modes are available. Table 11-2 shows features of the serial communication.

Table 11-2 Features of the Serial Communication

Serial Communication mode	Operation mode	Features
Synchronous Serial I/O Port (SSIO)	・8-bit mode ・16-bit mode	・ Max. 2ch (Both SSIO and UART are unavailable to use in the same channel) ・ Master mode / Slave mode ・ MSB first / LSB first ・ 8bit / 16bit data length ・ Self-test function using the master and slave modes. For the self-test functions, see "Safety Function."
UART mode	・Half-duplex communication mode ・Full-duplex communication mode	・ 5-bit/6-bit/7-bit/8-bit data length ・ Odd parity/even parity/0 parity/1 parity/and no parity ・ One stop bit/Two stop bits ・ Positive logic/negative logic for communication logic ・ MSB first / LSB first ・ Wide range of communication speed - 1bps to 4,800bps (Clock frequency is 32.768kHz) - 600bps to 3Mbps (Clock frequency is 24MHz) - 300bps to 2Mbps(Clock frequency is 16MHz) ・ Built-in baud rate generator for each channel ・ Parity error flag, overrun error flag, framing error flag, transmission buffer status flag, reception buffer status flag ・ Self-test function using transmission and reception For the self-test functions, see "Safety Function."

○Configuration

Figure 11-1 shows configuration of the serial communication unit.

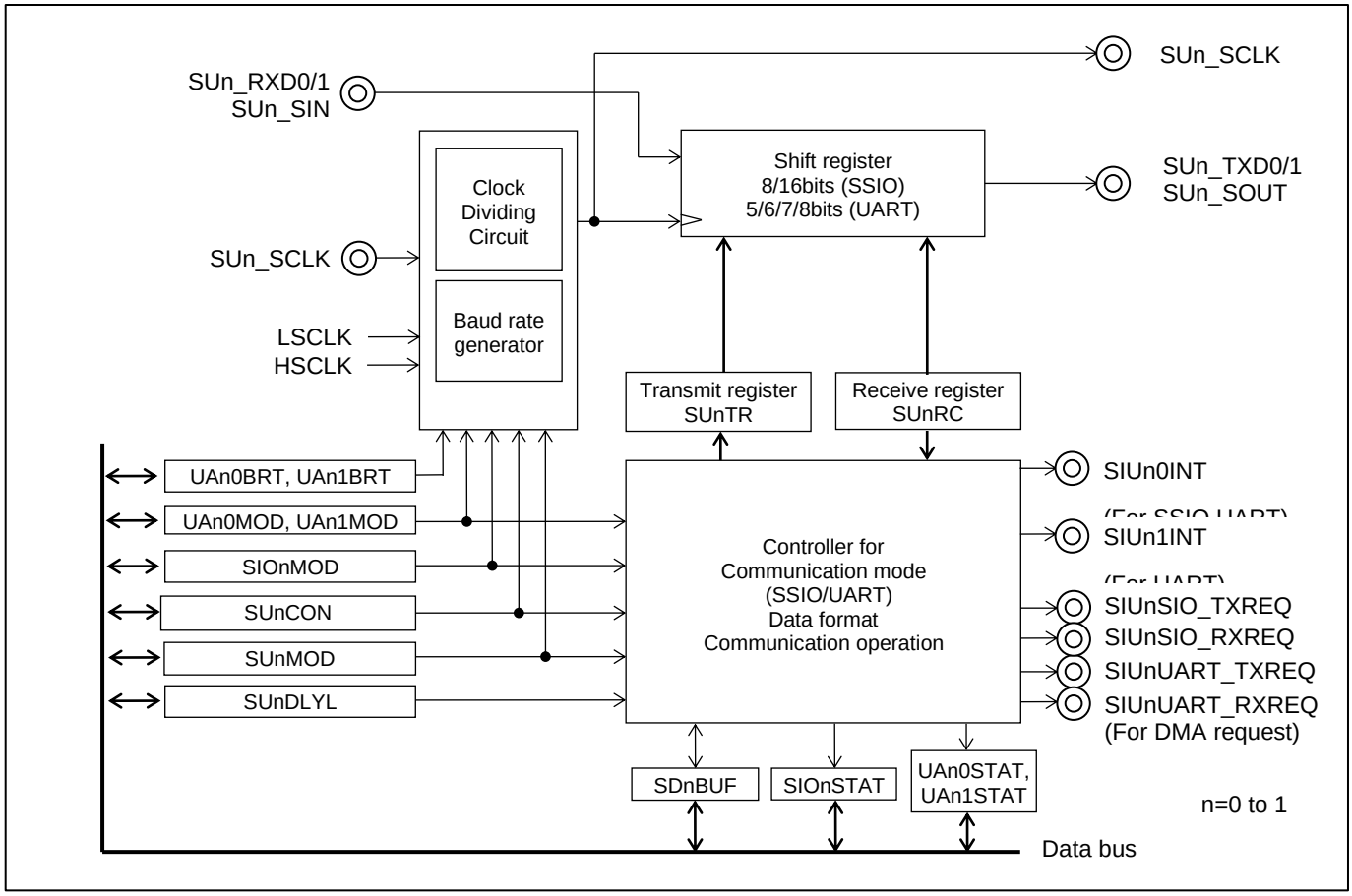


Figure 11-1 Configuration of the Serial Communication Unit

SDnBUF	: Serial communication unit n transmission/reception buffer
SUnMOD	: Serial communication unit n mode register
SUnCON	: Serial communication unit n control register
SUnDLYL	: Serial communication unit n transmission interval setting register
SIOnMOD	: Synchronous serial port n mode register
SIOnSTAT	: Synchronous serial port n status register
UAn0MOD, UAn1MOD	: UARTn0 mode register, UARTn1 mode register
UAn0BRT, UAn1BRT	: UARTn0 baud rate register, UARTn1 baud rate register
UAn0STAT, UAn1STAT	: UARTn0 status register, UARTn1 status register
SIUn0INT	: Serial communication unit n0 Interrupt
SIUn1INT	: Serial communication unit n1 Interrupt
SIUnSIO_TXREQ	: Serial communication unit n SSIO transmission DMA request
SIUnSIO_RXREQ	: Serial communication unit n SSIO reception DMA request
SIUnUART_TXREQ	: Serial communication unit n UART transmission DMA request
SIUnUART_RXREQ	: Serial communication unit n UART reception DMA request

○List of Pins

The I/O pins of the serial communication unit are assigned to the shared function of the general ports.

Pin name	I/O	Description
SUn_RXD0	I	Full-duplex data input UART0 data input of serial communication unit n
SUn_RXD1	I	UART1 data input of serial communication unit n
SUn_TXD0	O	UART0 data output of serial communication unit n
SUn_TXD1	O	Full-duplex data output UART1 data output of serial communication unit n
SUn_SCLK	I/O	SSIO synchronous clock input/output of serial communication unit n
SUn_SOUT	O	SSIO transmission data output of serial communication unit n
SUn_SIN	I	SSIO reception data input of serial communication unit n

(n=0 to 1)

Table 11-3 (1) and (2) show the list of the general ports used for the serial communication unit and the register settings of the ports.

Table 11-3(1) Ports used for the serial communication unit and the register settings (UART)

Channel no.	Pin name	Shared port		Setting register	Setting value
0	SU0_TXD0	P03	2nd Func.	P0MOD3	0001_XXXX*2
	SU0_RXD0	P02	2nd Func.	P0MOD2	0001_XXXX*1
		P07	3rd Func.	P0MOD7	0010_XXXX*1
		P17	3rd Func.	P1MOD7	0010_XXXX*1
	SU0_TXD1	P03	3rd Func.	P0MOD3	0010_XXXX*2
		P20	2nd Func.	P2MOD0	0001_XXXX*2
	SU0_RXD1	P07	2nd Func.	P0MOD7	0001_XXXX*1
		P17	2nd Func.	P1MOD7	0001_XXXX*1
1	SU1_TXD0	P22	2nd Func.	P2MOD2	0001_XXXX*2
	SU1_RXD0	P21	2nd Func.	P2MOD1	0001_XXXX*1
	SU1_TXD1	P22	3rd Func.	P2MOD2	0010_XXXX*2

*1: “XXXX” determines the condition of the port input

XXXX	Condition of the port input
0001	Input (without Pull-UP)
0101	Input (with Pull-UP)

*2: “XXXX” determines the condition of the port input

XXXX	Condition of the port output
0010	CMOS output
1010	Nch open drain output (without Pull-UP)
1111	Nch open drain output (with Pull-UP)

Table 11-3(2) Ports used in the serial communication unit and the register settings (SSIO)

Channel no.	Pin name	Shared port		Setting register	Setting value
0	SU0_SIN	P02	2nd Func.	P0MOD2	0001_XXXX*1
	SU0_SCLK	P04	2nd Func.	P0MOD4	0001_XXXX*3
	SU0_SOUT	P03	2nd Func.	P0MOD3	0001_XXXX*2
1	SU1_SIN	P21	2nd Func.	P2MOD1	0001_XXXX*1
	SU1_SCLK	P23	2nd Func.	P2MOD3	0001_XXXX*3
	SU1_SOUT	P22	2nd Func.	P2MOD2	0001_XXXX*2

*1: “XXXX” determines the condition of the port input

XXXX	Condition of the port
0001	Input (without Pull-UP)
0101	Input (with Pull-UP)

*2: “XXXX” determines the condition of the port output

XXXX	Condition of the port
0010	CMOS output
1010	Nch open drain output (without Pull-UP)
1111	Nch open drain output (with Pull-UP)

*3: “XXXX” determines the condition of the port input/output

XXXX	Condition of the port
0010	CMOS output (SSIO master mode)
0001	Input (SSIO slave mode)

○Combination of SSIO port

SUn_SIN, SUn_SOUT and SUn_SCLK are assigned to multiple general ports.
Be sure to use the ports in following combinations.

Combination	Channel No	Port		
		SUn_SIN*	SUn_SOUT*	SUn_SCLK*
1	0	P02	P03	P04
2	1	P21	P22	P23

*: n= Channel Number.

○Combination of UART port

The pin assignment depends on the communication mode. See Table 11-4 in section 11.2.1 of [ML62Q1000 Series User's Manual] for details of the pin assignment.

●I²C Bus Unit

ML62Q1532 has one channel of I²C bus unit that supports both master and slave function.
Either of master or slave can be chosen to use and both functions of master and slave are unworkable at the same time.

○Features

Table 12-2 shows the features of I^2C bus unit.

Table 12-2 Features of I^2C bus unit

Function	Operation mode	Features
I^2C bus unit	Master function	・ Communication speed: Standard mode (100 kbps), fast mode (400 kbps), and original standard 1 Mbps mode (1Mbps) ・ Support clock stretch function for the Slave ・ 7-bit address format (only the master function supports 10-bit address format) ・ Self-test function by reading transmitted data onto the I^2C bus (Safety function)
	Slave function	・ Communication speed: Standard mode (100 kbps), fast mode (400 kbps), and original standard 1 Mbps mode (1Mbps) ・ Clock stretch function ・ 7-bit address format ・ Wake-up from STOP mode by matching slave address

○Configuration

Figure 12-1 shows the configuration diagram of the I²C bus unit circuit.

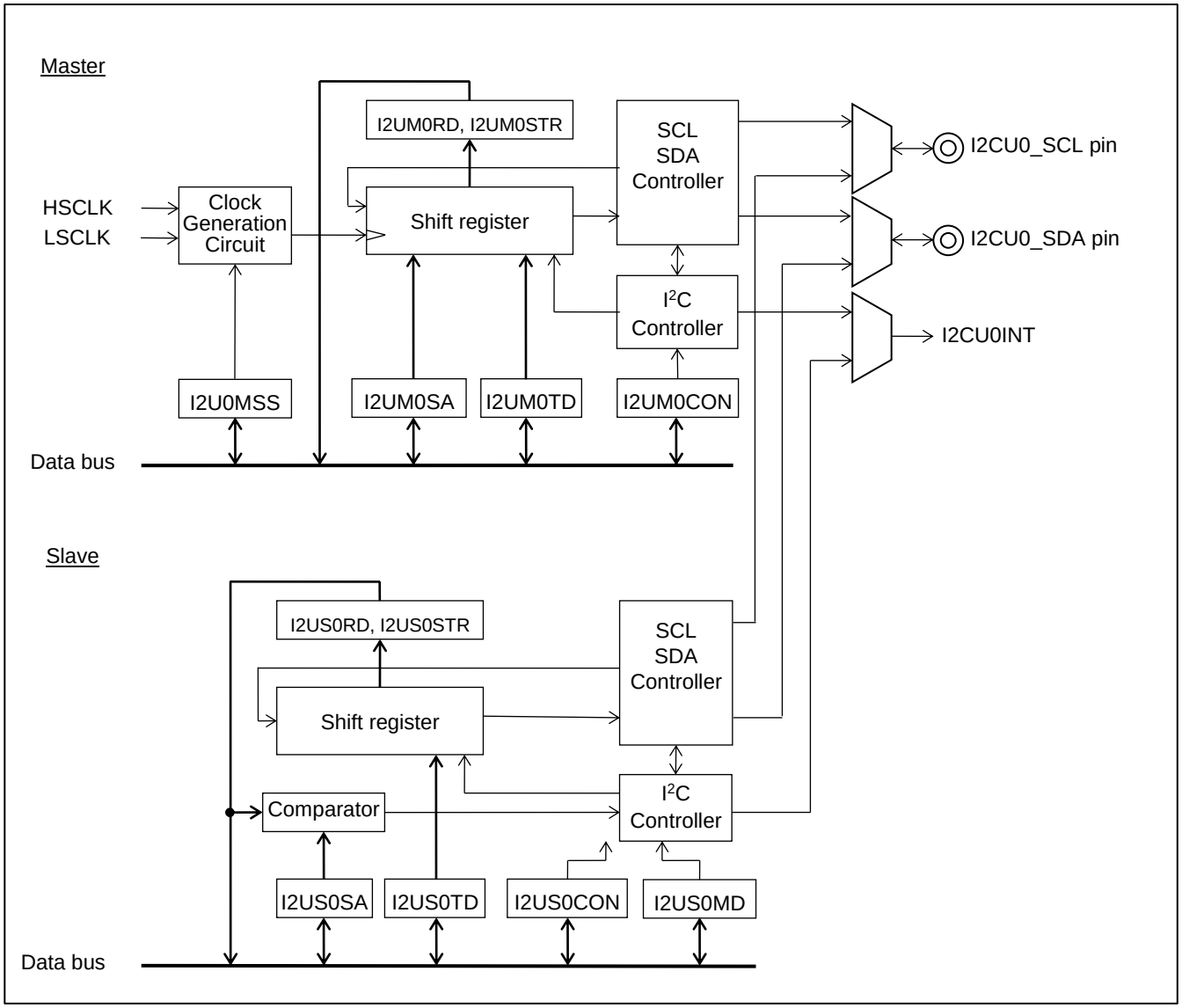


Figure 12-1 Configuration of I²C Bus Unit

I2CU0_SCL: Serial Clock
I2CU0_SDA: Serial Data
I2U0MSS: I²C bus unit n mode register
I2UM0RD: I²C bus 0 receive register (master)
I2UM0SA: I²C bus 0 slave address register (master)
I2UM0TD: I²C bus 0 transmit data register (master)
I2UM0CON: I²C bus 0 control register (master)
I2UM0STR: I²C bus 0 status register (master)
I2US0RD : I²C bus 0 receive register (slave)
I2US0SA: I²C bus 0 slave address register (slave)
I2US0TD: I²C bus 0 transmit data register (slave)
I2US0CON: I²C bus 0 control register (slave)
I2US0MD: I²C bus 0 mode register (slave)
I2US0STR: I²C bus 0 status register (slave)

○List of Pins

The I/O pins of the I^2C bus unit are assigned to the shared function of the general ports.

Pin name	I/O	Description
I2CU0_SDA	I/O	I^2C bus unit 0 data I/O pin
I2CU0_SCL	I/O	I^2C bus unit 0 clock I/O pin

○Pin Setting

I2CU0_SDA pin and I2CU0_SCL pin are assigned to multiple general ports.
Be sure to use the ports in following combinations.

Pin name	Combination 1
I2CU0_SDA	P03
I2CU0_SCL	P04

In addition to the mode setting of the shared function, choose "Enable Input, Enable Output, Nch open drain output and without pull-up" by setting following data to the port n mode register m (PnMODm).

Table 12-3 I^2C bus unit general port combinations

Port name	PnMODm	Combination	Setting data
P03	P0MOD3	1	0x3B

[Note]

- **Use external pull-up resistors for SDA pin and SCL pin referring to the I^2C bus specification. The internal pull-up resistors unsatisfy the I^2C bus specification. See the data sheet for each product for the value of internal pull-up resistors.**
- **If powering off this LSI in the slave mode, it disables communications of other devices on the I^2C bus. Keep this LSI powered on when it works as a slave mode until the master device is powered off.**
- **When using the master function, do not connect multiple master devices on the I^2C bus.**

●I²C Bus Master

ML62Q1532 has two channels of I²C bus master that support only the master function on the I²C bus specification. This unit has the function of the I²C bus unit, described in Chapter 12, not containing the slave function and the low-speed clock (LSCLK) operation.

○Features

Table 13-2 shows the features of I²C bus master.

Table 13-2 Features of I2C bus master

Function	Operation mode	Features
I²C bus master	Master mode	・ Communication speed: Standard mode (100 kbps), fast mode (400 kbps), and original standard 1 Mbps mode (1Mbps) ・ Support clock stretch function for the Slave ・ 7-bit address format (only the master function supports 10-bit address format) ・ Self-test function by reading transmitted data onto the I2C bus (Safety function)

○Configuration

Figure 13-1 shows the configuration diagram of the I²C bus master circuit.

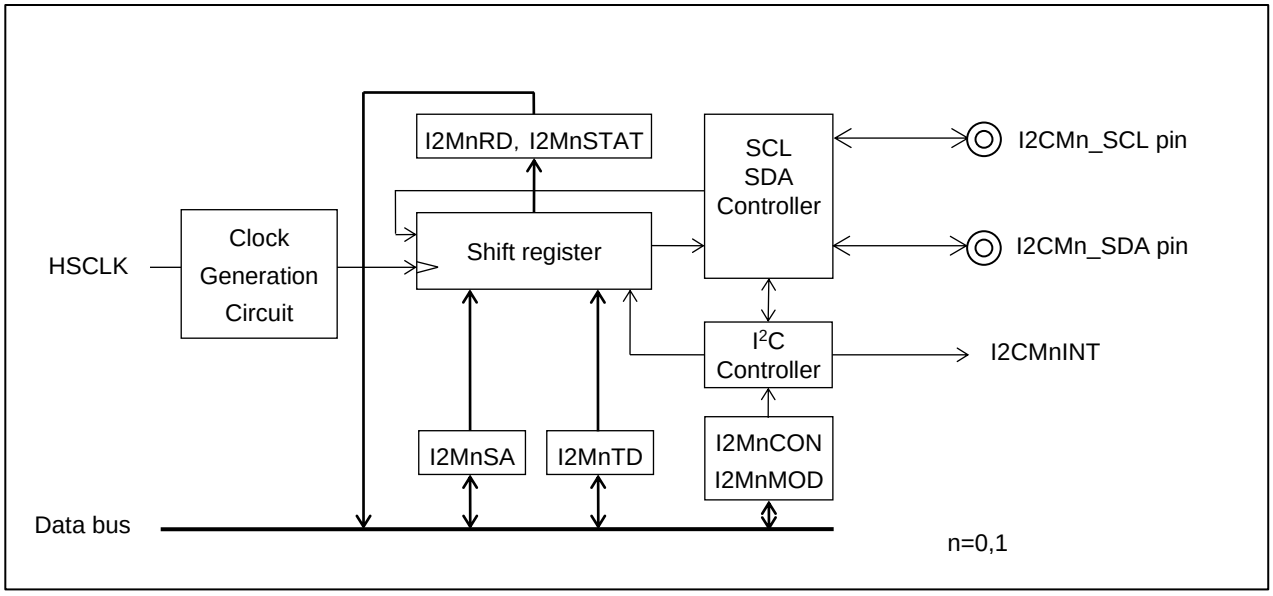


Figure 13-1 Configuration of I²C Bus Master

I2CMn_SCL:	Serial Clock
I2CMn_SDA:	Serial Data
I2MnRD:	I²C master n receive register
I2MnSA:	I²C master n slave address register
I2MnTD:	I²C master n transmit data register
I2MnCON:	I²C master n control register
I2MnMOD:	I²C master n mode register
I2MnSTAT:	I²C master n status register

○List of Pins

The I/O pins of the I^2C bus master are assigned to the shared function of the general ports.

Pin name	I/O	Function
I2CMn_SDA	I/O	I^2C bus master n data I/O pin
I2CMn_SCL	I/O	I^2C bus master n clock I/O pin

○Pin Setting

I2CMn_SDA pin and I2CMn_SCL pin are assigned to multiple general ports.
Be sure to use the ports in following combinations.

Pin name	Combination 1	Combination 2
I2CM0_SDA	P06	P22
I2CM0_SCL	P07	P23

In addition to the mode setting of the shared function, choose "Enable Input, Enable Output, Nch open drain output and without pull-up" by setting following data to the port n mode register m (PnMODm).

Table 13-3 I^2C bus master general port combinations

Port name	PnMODm	Combination	Setting data
P06	P0MOD6	1	0x3B
P07	P0MOD7	1	0x3B
P22	P2MOD2	2	0x3B
P23	P2MOD3	2	0x3B

[Note]

- **Use external pull-up resistors for SDA pin and SCL pin referring to the I^2C bus specification. The internal pull-up resistors unsatisfy the I^2C bus specification. See the data sheet for each product for the value of internal pull-up resistors.**
- **Do not connect multiple master devices on the I^2C bus.**

●DMA Controller

ML62Q1532 has two channels of the Direct Memory Access Controller (DMAC), which enables to transfer data between SFR of peripheral circuits and the built-in RAM without the CPU operation.
Table 14-1 in the section 14.3.6 "DMA Transfer Target Block" of "ML62Q1000 Series User's Manual" shows available peripheral blocks to use as the DMA transfer source or destination.

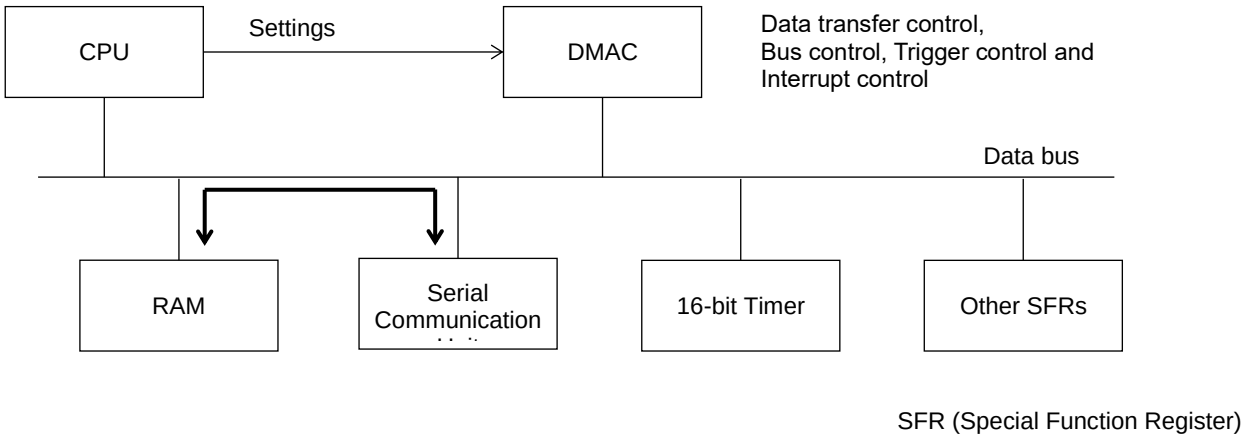


Figure 14-1 DMA Controller Overview

[Note]

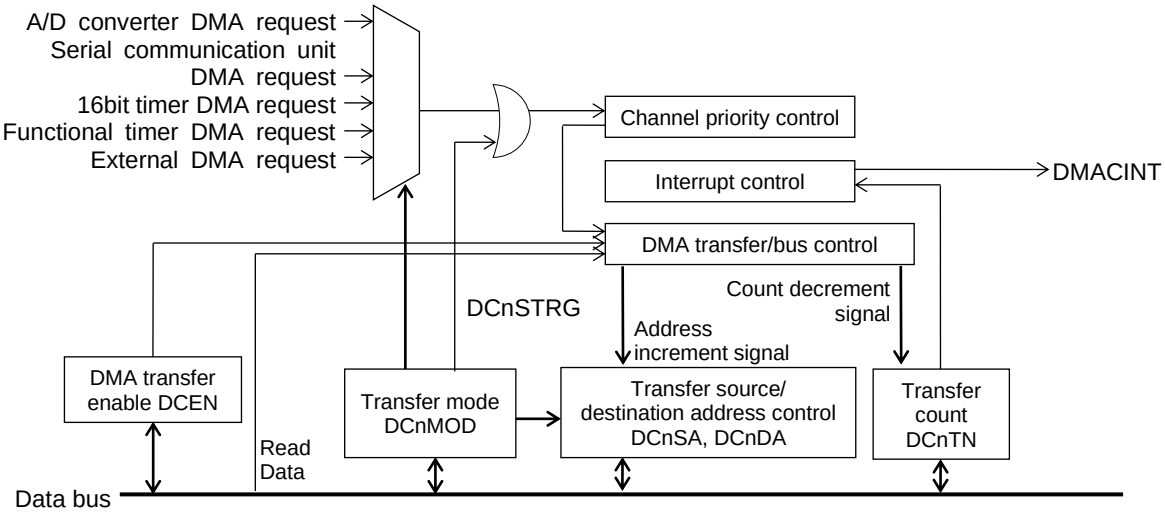
- **Do not use the DMA controller and the Coprocessor (Hardware multiplier/divider) simultaneously.**

○Features

- Transfer unit : 8bit/16bit
- Transfer count : 1 to 1024 time
- Transfer cycle : 2 cycle (CPU operation has priority if the access is competed)
- Transfer address : Fixed address / Increment address / Decrement address
- Transfer target : SFR/RAM → SFR/RAM (Transfer from/to Flash is not supported)
- Transfer request : Serial communication DMA request, SA-ADC DMA request, 16bit timer DMA request, Functional timer DMA request, External DMA request and the software DMA request
- Transfer priority : Channel 0 > Channel 1 (Channel 0 has higher priority)
- Interrupt : The DMA Controller interrupt occurs when the all transfers are completed.

○Configuration

Figure 14-2 shows the configuration of the DMA Control circuit.



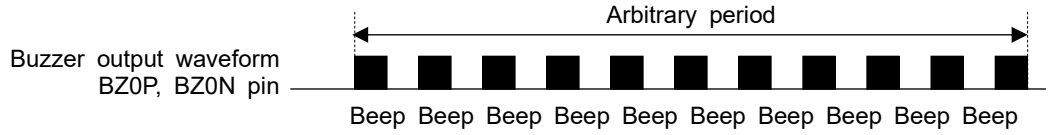
DCnMOD : DMA channel n transfer mode register
DCnTN : DMA channel n transfer count register
DCnSA : DMA channel n transfer source address register
DCnDA : DMA channel n transfer destination address register
DCEN : DMA transfer enable register
DCnSTRG : DMA channel n software request
(n = 0,1)

Figure 14-2 Configuration of DMA Controller Circuit

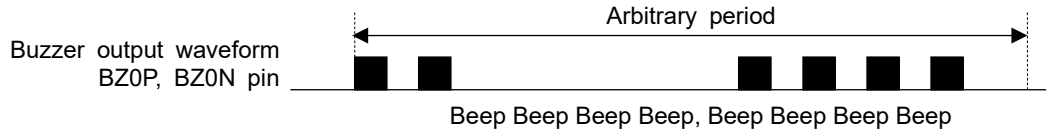
●Buzzer

The buzzer circuit generates a base signal in combination of 8 frequencies and 15 duties and outputs the signal in four modes.

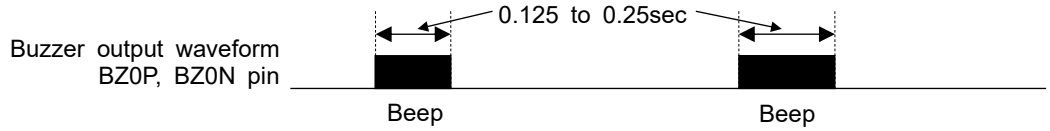
Intermittent sound 1 mode:



Intermittent sound 2 mode:



Single sound mode:



Continuous sound:

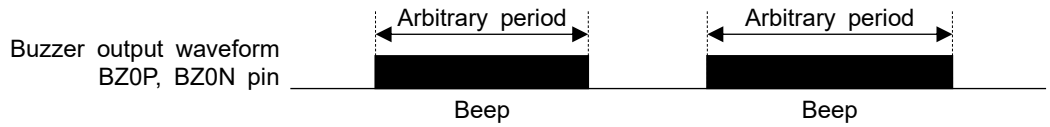


Figure 15-1 Buzzer output image

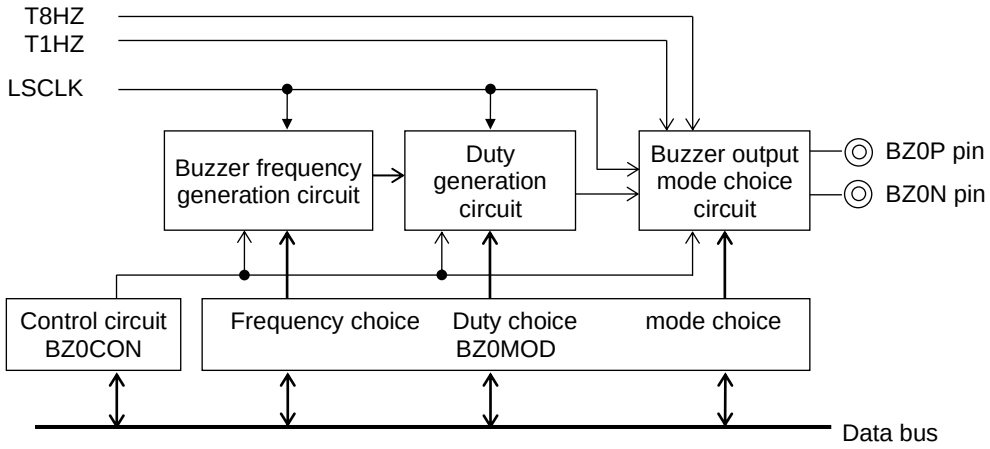
The buzzer circuit outputs a positive phase pulse (BZ0P) and negative phase pulse (BZ0N).
Also, for details of the clock used in the buzzer block (T8HZ, T1HZ), see "Low Speed Time Base Counter".

○Features

- Four types of buzzer mode (Intermittent sound 1, Intermittent sound 2, Single sound and Continuous sound)
- Eight types of frequency (4.096 kHz to 293 Hz)
- 15 duties (1/16 to 15/16 = 6.25% to 93.75%)
  Only seven duties (1/8 to 7/8 = 12.5% to 87.5%) are available when the buzzer frequency is 4.096 kHz.
- The initial level (positive logic or negative logic) of the buzzer output pins can be chosen

○Configuration

Figure 15-2 shows the configuration of the buzzer circuit.



BZ0CON : Buzzer 0 control register
BZ0MOD : Buzzer 0 mode register

Figure 15-2 Configuration of Buzzer

○List of Pins

The output pins of the buzzer signal are assigned to the shared function of the general port.

Pin name	I/O	Function
BZ0P	O	Buzzer output (positive phase)
BZ0N	O	Buzzer output (negative phase)

Table 15-1 shows the list of the general ports used for the buzzer output and the register settings of the ports.

Table 15-1 Ports used for the buzzer and the register settings

Pin name	Shared port		Setting register	Setting value
BZ0P	P17	7th Func.	P1MOD7	0110_XXXX
BZ0N	P20	7th Func.	P2MOD0	0110_XXXX

"XXXX" determines the condition of the port output

XXXX	Condition of the port output
0010	CMOS output
1010	Nch open drain output (without the pull-up)
1111	Nch open drain output (with the pull-up)

●Simplified RTC

ML62Q1532 has the simplified RTC (RTC: Real Time Clock).
The simplified RTC counts up from 00 minutes 00 seconds to 59 minutes 59 seconds in the unit of one second and also generates an interrupt request periodically.
For the interrupt enable/request flags, etc. described in this chapter, refer to Chapter "Interrupts".

○Features

- A desired periodical interrupt request can be chosen from among four types (0.5, 1, 30 and 60 seconds).
- A function to prevent erroneous writing to the simplified RTC minute/second counter included.
- The simplified RTC minute/second counter continues counting operation even when a reset (other than power-on reset) is generated.
- Counting operation is continued all the time, except when operating in the STOP/STOP-D mode.

○Configuration

Figure 16-1 shows the configuration of simplified RTC.

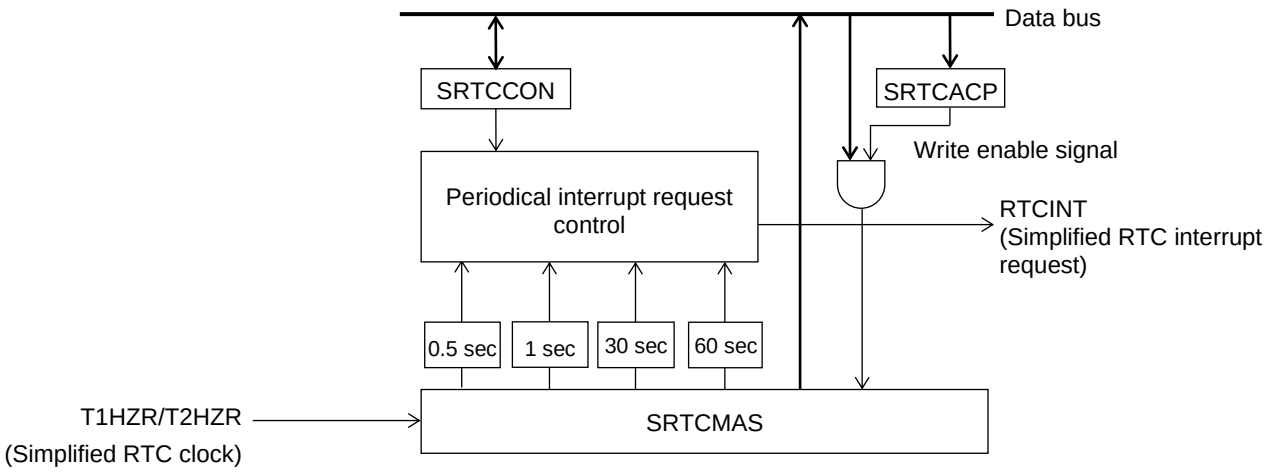


Figure 16-1 Simplified RTC Configuration

SRTCACP	: Simplified RTC acceptor
SRTCMAS	: Simplified RTC minute/second counter SRTCMIN (minute counter), SRTCSEC (second counter)
SRTCCON	: Simplified RTC control register

●General Purpose Port

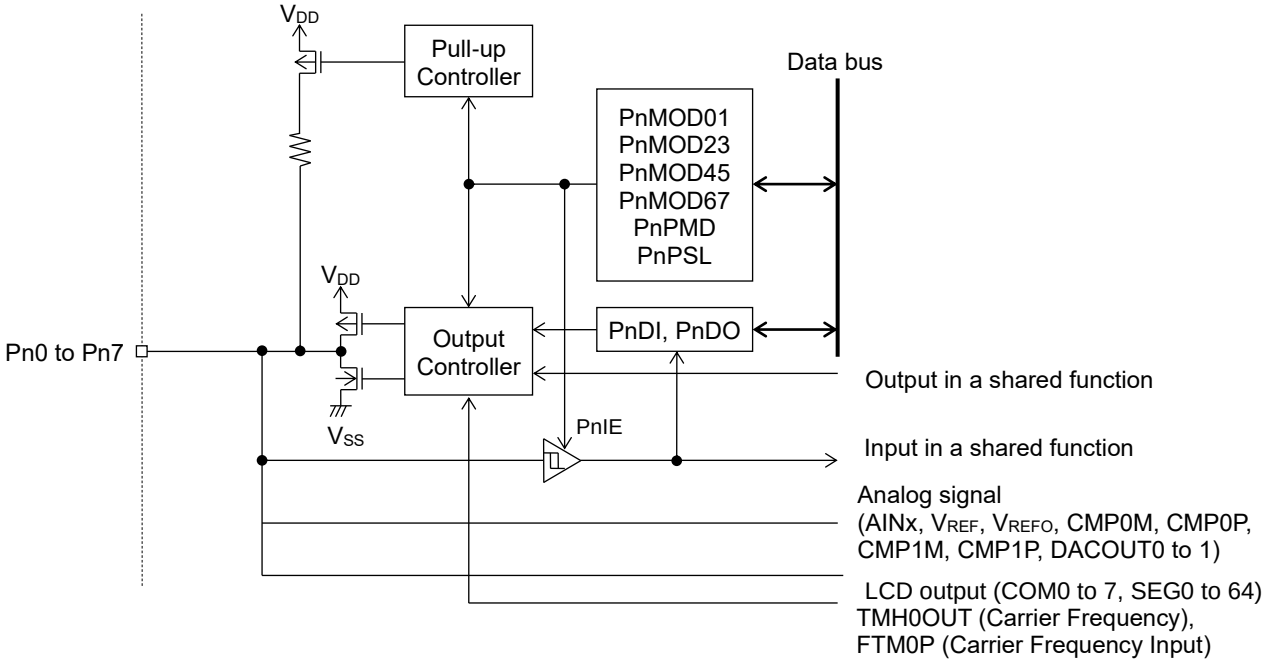
The general purpose port is used as an input port or an output port.
The input and output are switchable on each pin. A general input port or output port shares a number of functions. See "List of Pins" or "Description of Pins"for more detail.
Two general input ports are shared with the crystal resonator connection pins.
The number of general ports is dependent of each product. See Table 17-1 "List of Pins".

○Features

- Input or output can be chosen in each pin
- Pull-up resistor can be chosen in each pin
- CMOS output or N-channel open drain output is can be chosen in each pin
- Direct driving LEDs is supported when the N-channel open drain output is chosen
- Carrier frequency output function
- Port output level test function

○Configuration

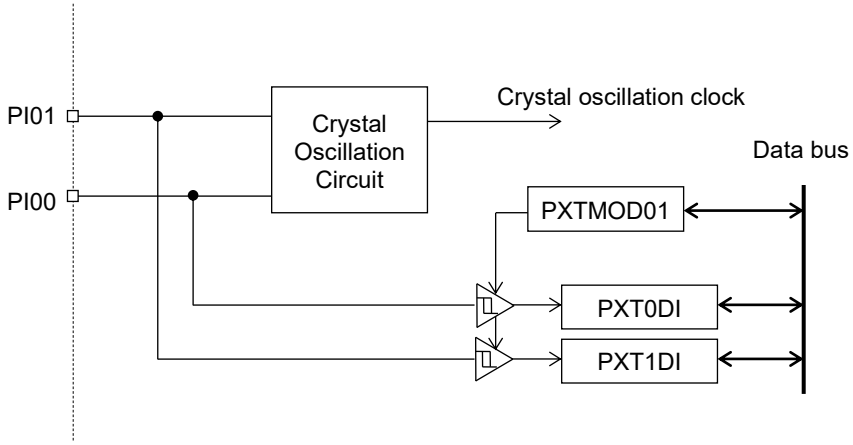
Figure 17-1 shows the configuration of the general purpose port.



PnDI	: Port n data register(bit 7 to 0)
PnDO	: Port n data register(bit 15 to 8)
PnMOD01	: Port n mode register 01
PnMOD23	: Port n mode register 23
PnMOD45	: Port n mode register 45
PnMOD67	: Port n mode register 67
PnPMD	: Port n pulse mode register
PnPSL	: Port n pulse selection register

Figure 17-1 Configuration of General Purpose I/O port n

図 17-2 に汎用入力ポートの構成を示します。



PXT0DI	: PORTXT data input register(bit 0)
PXT1DI	: PORTXT data input register(bit 1)
PXTMOD01	: PORTXT mode register01

Figure 17-2 Configuration of General Purpose Input Port

○List of Pins

Table 17-1 List of Pins

Pin Name	Primary Function
PI00	General purpose Input/ Crystal Oscillator Input
PI01	General purpose Input/ Crystal Oscillator Input/ External Clock Input
P00	General purpose Input/Output
P01	General purpose Input/Output / DACOUT0
P02	General purpose Input/Output /EXI0
P03	General purpose Input/Output /EXI1
P04	General purpose Input/Output /EXI2
P05	General purpose Input/Output
P06	General purpose Input/Output
P07	General purpose Input/Output
P17	General purpose Input/Output /EXI3
P20	General purpose Input/Output
P21	General purpose Input/Output /EXI4
P22	General purpose Input/Output
P23	General purpose Input/Output /EXI5
P62	General purpose Input/Output
P63	General purpose Input/Output

●External Interrupt Function

The external interrupt function generates interrupts by signals input to the general ports.
The interrupt channel has each dedicated interrupt vector.
The number of general ports with the external interrupt function is dependent of each product. See Table 18-1 " Ports used for the external interrupt and the register settings".

○Features

- Maskable 6 interrupts
- Available to choose the interrupt mode: interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode or both-edge interrupt mode
- Available to choose "with sampling" or "without sampling" for the input signal (the sampling clock is LSCLK or HSCLK)

○Configuration

Figure 18-1 shows the configuration of the external interrupt function (EXI0 to EXI7)

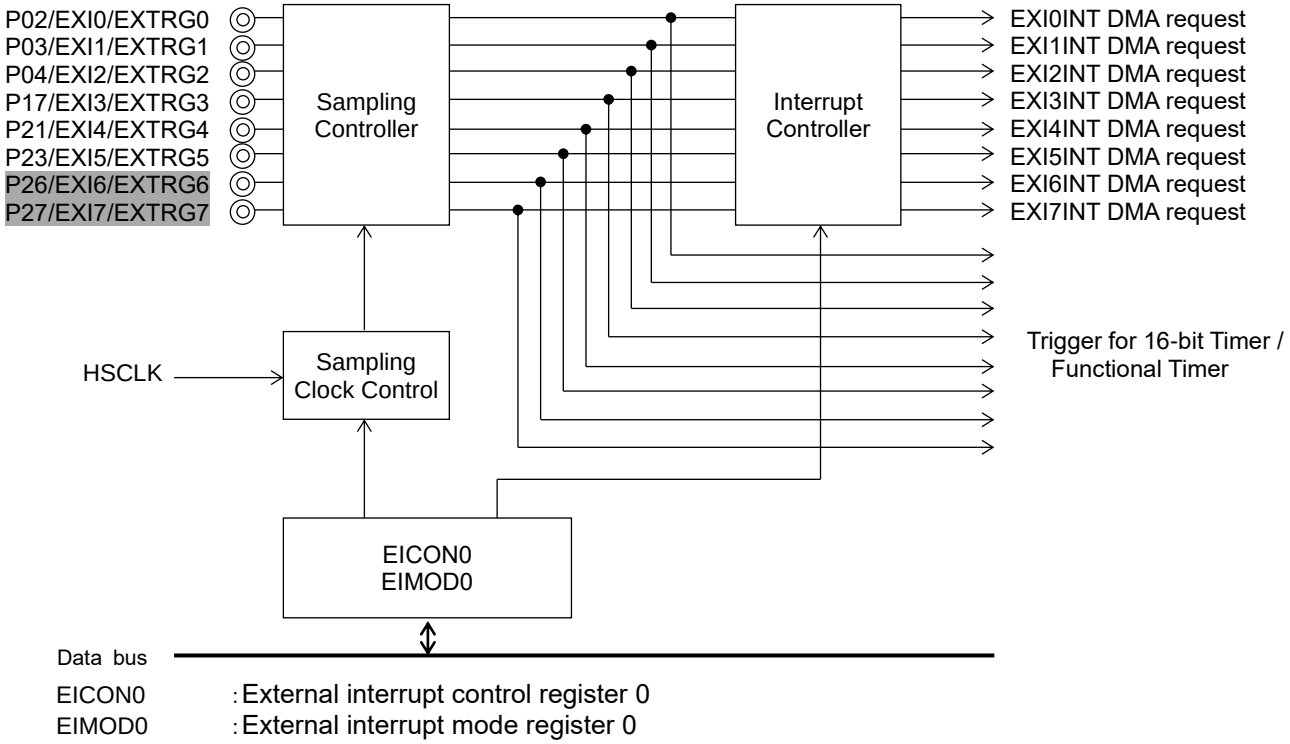


Figure 18-1 Configuration of External Interrupt Function

[Note]
ML7456N does not equips P26/EXI6/EXTRG6 and P27/EXI7/EXTRG7.

○List of Pins

External interrupt is assigned to the primary function of the general port.

Pin name	I/O	Function
EXI0	I	External Interrupt Input 0
EXI1	I	External Interrupt Input 1
EXI2	I	External Interrupt Input 2
EXI3	I	External Interrupt Input 3
EXI4	I	External Interrupt Input 4
EXI5	I	External Interrupt Input 5

Table 18-1 shows the list of the general ports used for the external interrupt and the register settings of the ports.

Table 18-1 Ports used for the external interrupt and the register settings

Pin name	Shared port		Setting register	Setting value
EXI0	P02	Primary Function	P0MOD2	0000_0X01[*1]
EXI1	P03	Primary Function	P0MOD3	0000_0X01[*1]
EXI2	P04	Primary Function	P0MOD4	0000_0X01[*1]
EXI3	P17	Primary Function	P1MOD7	0000_0X01[*1]
EXI4	P21	Primary Function	P2MOD1	0000_0X01[*1]
EXI5	P23	Primary Function	P2MOD3	0000_0X01[*1]

[*1]: "X" of “01X1” determines the condition of the port input

X	Condition of the port input
0	Input (without an internal pull-up resistor)
1	Input (with an internal pull-up resistor)

●CRC Calculator

ML7456N has the CRC (Cyclic Redundancy Check) generator that performs CRC calculation and generates the CRC data used for error detection in serial communications.
Also, the CRC generator has automatic CRC calculation mode to check data in program memory, available in HALT mode or HALT-H mode.

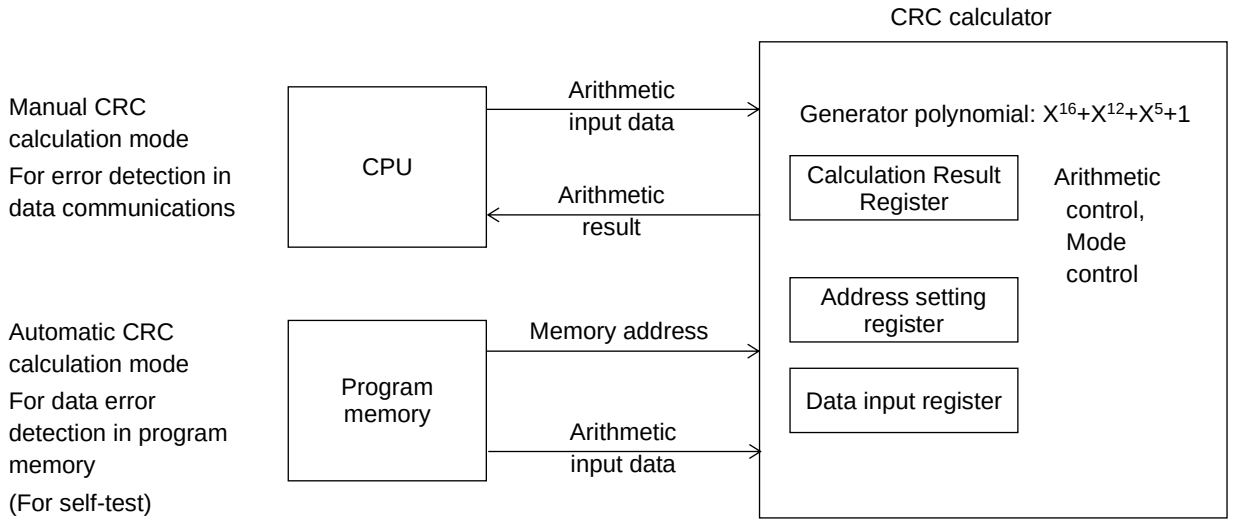


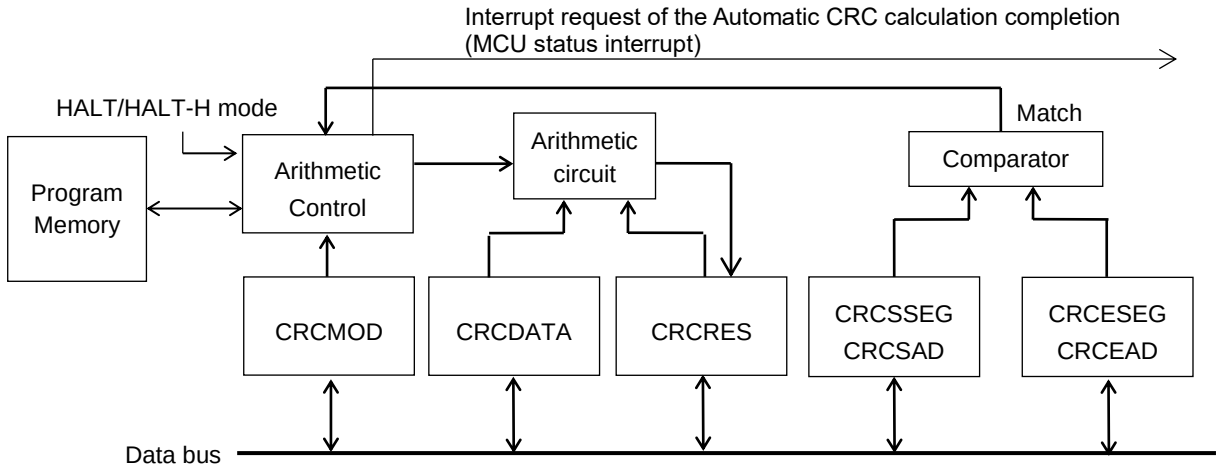
Figure 19-1 CRC generator overview

○Features

- Manual CRC calculation mode
  Generates CRC data from data set in CRC calculation register by the software
  Calculation unit is 8bit
- Automatic CRC calculation mode
  Automatic CRC calculation by the hardware to check data in program memory in HALT or HALT-H mode and generates CRC data
  Calculation unit is 32bit. The interrupt occurs when the arithmetic operation is completed
- Generator polynomial: $X^{16}+X^{12}+X^{5}+1$
- MSB first or LSB first selectable

○Configuration

Figure 19-2 shows the configuration of the CRC generator.



CRCMOD : CRC Calculation Mode Register
CRCDATA : CRC Calculation Data Register
CRCRES : CRC Calculation Result Register
CRCSSEG : Automatic CRC Calculation Start Segment Setting Register
CRCESEG : Automatic CRC Calculation End Segment Setting Register
CRCSAD : Automatic CRC Calculation Start Address Setting Register
CRCEAD : Automatic CRC Calculation End Address Setting Register

Figure 19-2 Configuration of CRC Generator

●Analog Comparator

The Analog Comparator enables to use following functions.

- Compare voltages input to the two pins
- Compare a voltage input to the one pin with the internal reference voltage (Approx. 0.8V)

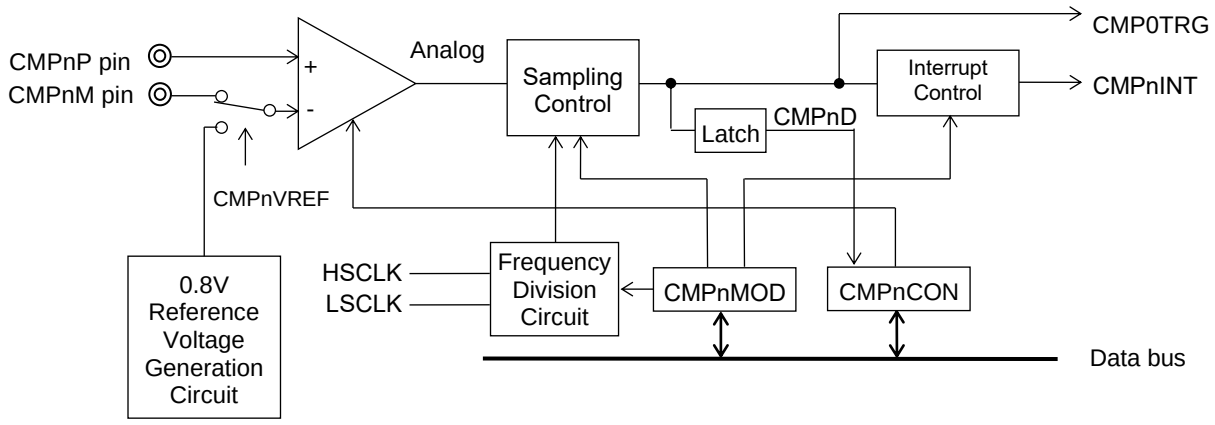
ML7456N equips 2 channels analog comparator.

○Features

- Comparable with external 2 voltage inputs.
- Comparable with external voltage input and internal reference voltage (approx. 0.8V).
- Three types of interrupt timing generated by the voltage comparison are available.
  - Rising edge of the comparison result
  - Falling edge of the comparison result
  - Rising edge and Falling edge of the comparison result
- The sampling with a clock is optional for the comparison result
  - HSCLK
  - LSCLK
  - 1/2 HSCLK to 1/64 HSCLK
  - 1/2 LSCLK to 1/64 HSCLK
- Last comparison result CMPnD(n=0,1) is retained when the analog comparator is stopped
- The analog comparator result output can be used as a trigger event source for the Functional Timer.

○Configuration

Figure 20-1 shows the configuration of the analog comparator (n=0 to 1).



CMPnCON : Comparator n control register
CMPnMOD : Comparator n mode register
CMPnD : Analog Comparator n result
CMPnINT : Analog Comparator n Interrupt
CMPnVREF : Reference voltage select setting
CMP0TRG : Analog Comparator 0 output. Trigger event source for the Functional Timer.

Figure 20-1 Configuration of Analog Comparator

○List of Pins

The I/O pins of the Analog Comparator are assigned to the shared function of the general ports (n=0 to 1).

Pin name	I/O	Function
CMPnP	I	Analog comparator n non-inverting input
CMPnM	I	Analog comparator n inverting input

Table 20-2 shows the list of the general ports used for the Analog Comparator and the register settings of the ports.

Table 20-2 Ports used in the Analog Comparator and the register settings

Pin name	Shared port		Setting Register	Setting value
CMP0P	P03	7th Func.	P0MOD3	0110_0000
CMP0M	P02	7th Func.	P0MOD2	0110_0000
CMP1P	P62	7th Func.	P6MOD2	0110_0000
CMP1M	P63	7th Func.	P6MOD3	0110_0000

[Note]

- **When using the analog comparator, write "0" to the target PnmIE bit and PnmOE bit of port n mode registers (n=0 to 9, A, B, m=0 to 7) to set the general port to Hi-impedance, otherwise a shoot-through current may flow.**
- **An influence of the noise is reducible by preventing the switching of neighboring pins when the comparator enables.**

●D/A Converter

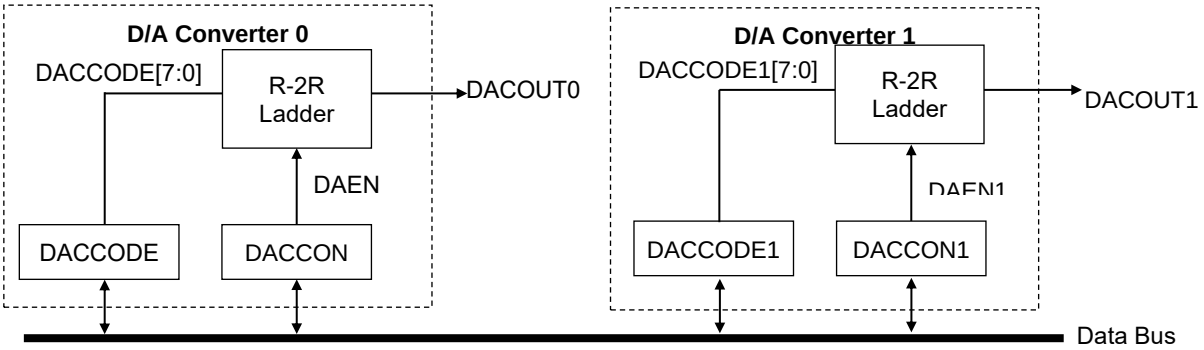
ML62Q1532 has one channel 8-bit resolution D/A converter that converts digital input signals to analog signals.

○Features

- 8-bit resolution
- R-2R ladder method
- Analog output voltage (DACOUT0/DACOUT1)
  - Output voltage: V_{DDIO_MCU} x (Setting value in the SFR) /256
  - Output impedance: 6kΩ (Typ.)

○Configuration

Figure 21-1 shows the configuration of the D/A converter.



DACCON : D/A converter 0 control register
DACCODE : D/A converter 0 code register
DACCON1 : D/A converter 1 control register
DACCODE1 : D/A converter 1 code register

Figure 21-1 Configuration of D/A Converter Circuit

[Note]
ML7456N equips only D/A converter 0.

○List of Pins

The I/O pins of the D/A converter are assigned to the shared function of the general ports.

Pin name	I/O	Function
DACOUT0	O	D/A converter 0 output

Table 21-2 shows the list of the general ports used for the D/A converter and the register settings of the ports.

Table 21-2 Ports used in the D/A converter and the register settings

Channel no.	Pin name	Shared port		Setting Register	Setting value
0	DACOUT0	P01	Primary Func.	P0MOD1	0000_0000

[Note]

- **When using the D/A converter, write "0" to the target PnmIE bit and PnmOE bit of port n mode registers (n=0 to 9, A, B, m=0 to 7) to set the general port to Hi-impedance (input and output disabled), othewise a shoot-through current may flow.**
- **An infuluence of the noise is reduceable by preventing the switching of neighboring pins while the D/A conveter is operating.**

●Voltage Level Supervisor

ML62Q1532 has the Voltage Level Supervisor (VLS0) that detects whether the voltage level of V_{DD} is lower or higher than the specified threshold voltage.

○Features

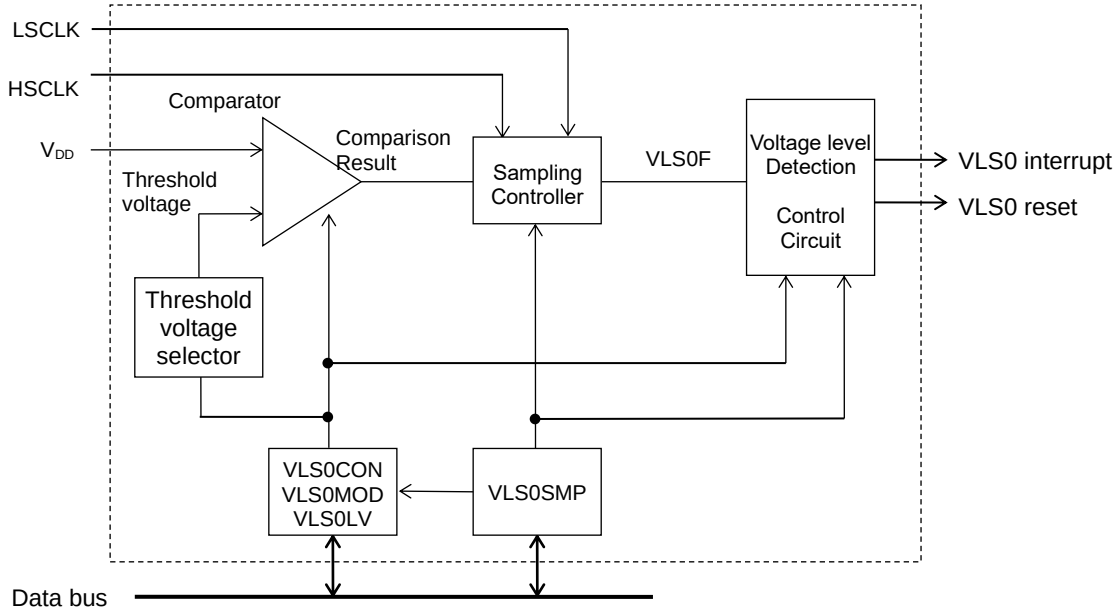
- Accuracy: ±4 %
- Threshold voltage: Selectable from 12 values (1.85 to 4.00 V)
- Operation mode: Supervisor mode (continuous detection) or single mode (one detection)

Mode	Description
Single mode 1	Detect the voltage level of V_{VDD_MCU} only once. The interrupt occurs after detecting the voltage of V_{DD}, indicates the detection has been completed.
Single mode 2	Detect the voltage level of V_{VDD_MCU} only once. The interrupt occurs after detecting the voltage of V_{DD} is lower than the threshold voltage, indicates the MCU is in the low voltage condition.
Supervisor mode	Detect continuously the voltage level of V_{VDD_MCU}, suitable for always detecting the low voltage level of V_{VDD_MCU} and generating the interrupt or reset. The interrupt or reset occurs according to the setting in the VLS0MOD register. The VLS0 reset function is available by choosing the supervisor mode.

- Voltage level supervisor reset (VLS0 reset)
- Voltage level supervisor interrupt (VLS0 interrupt)
- Initialized by the power-on reset (POR) or pin reset

○Configuration

The voltage level supervisor (VLS0) consists of a comparator, a sampling control circuit, and a voltage level detection control circuit. Figure 22-1 shows the configuration of the VLS0.



VLS0CON : Voltage level supervisor 0 control register
VLS0MOD : Voltage level supervisor 0 mode register
VLS0LV : Voltage level supervisor 0 level register
VLS0SMP : Voltage level supervisor 0 sampling register

Figure 22-1 Configuration of Voltage Level Supervisor

●Successive Approximation Type A/D Converter

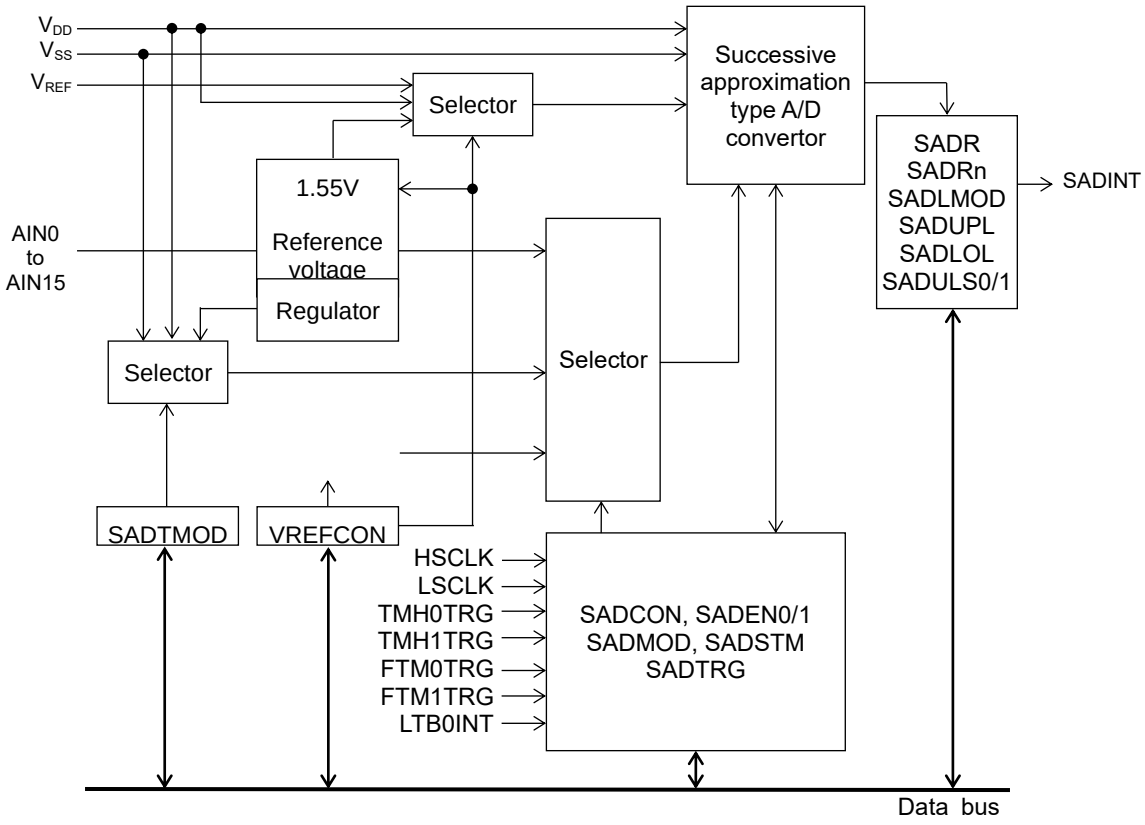
ML62Q1532 has the Successive Approximation type A/D Converter (SA-ADC), converts an analog input level to a digital value.
The number of A/D Converter channels is dependent of the product specification.
ML7456N equips 5 channels (n=0,1,2,3,11)

○Features

- Resolution : 10bit
- Conversion time : Min. 2.25μs/channel (conversion clock is 8MHz)
- Number of input channel : Max. 5ch
- Reference voltage: Voltage input from the V_{DD} pin, Internal reference voltage(approx.1.55V) or External reference voltage(V_{REF} pin)
- Sampling time can be chosen
- Consecutive scan conversion function for target channels
- Consecutive scan conversion with a specific interval time
- One conversion result register for each channel
- Upper /Lower limit is configurable for the conversion result, generates an interrupt
- A built-in temperature sensor usable for the low-speed RC oscillation adjustment
- A/D converter self-test function (full scale, zero scale, internal reference voltage)
- Following triggers is available to start the A/D conversion
  - 16-bit Timer 0 trigger (TMH0TRG)
  - 16-bit Timer 1 trigger (TMH1TRG)
  - Functional Timer 0 trigger (FTM0TRG)
  - Functional Timer 1 trigger (FTM1TRG)
  - Low-speed Time Base Counter interrupt (LTB0INT)

○Configuration

Figure 23-1 shows the configuration of SA-ADC.



SADCON	: SA-ADC control register
SADEN0/1	: SA-ADC enable register 0, 1
SADMOD	: SA-ADC mode register
SADSTM	: SA-ADC scan conversion interval setting register
SADR	: SA-ADC result register
SADRn	: SA-ADC result register n (n = 0 to 16)
SADLMOD	: SA-ADC upper/lower limit mode register
SADUPL	: SA-ADC upper limit setting register
SADLOL	: SA-ADC lower limit setting register
SADULSn	: SA-ADC upper/lower limit status register n (n=0,1)
VREFCON	: Reference voltage control register
SADTRG	: SA-ADC trigger register
SADTMOD	: SA-ADC test mode register
SADINT	: SA-ADC interrupt request, SA-ADC DMA request
TMH0TRG, TMH1TRG	: 16-bit Timer 0, 1 interrupt
FTM0TRG, FTM1TRG	: Functional Timer 0, 1 interrupt
LTB0INT	: Low speed time base counter 0 interrupt request

Figure 23-1 Configuration of successive approximation type A/D Converter

○List of Pins

The I/O pins of the Successive Approximation type A/D converter are assigned to the shared function of the general ports.

Pin name	I/O	Description
V_{DDIO_MCU}	-	Positive power supply for SA-ADC
V_{SS}	-	Negative power supply for SA-ADC
V_{REF}	-	Reference power supply for SA-ADC
AIN0	I	SA-ADC channel 0 analog input
AIN1	I	SA-ADC channel 1 analog input
AIN2	I	SA-ADC channel 2 analog input
AIN3	I	SA-ADC channel 3 analog input
AIN11	I	SA-ADC channel 11 analog input

●Regulator

ML62Q1532 incorporates the regulator.
Figure 24-1 shows the general scheme of the regulator.
The regulator generates a constant internal logic voltage (REG_CORE_MCU) independent of the variation of V_{DDIO_MCU} (2.6 V to 3.6 V) using an amplifier for the low power consumption. The REG_CORE_MCU generated by the regulator is supplied to peripheral circuits such as the internal logic circuit, flash memory, RAM, and oscillation circuit.
In order to stabilize the REG_CORE_MCU, connect the REG_CORE_MCU pin to V_{SS} via a capacitor (1 µF).

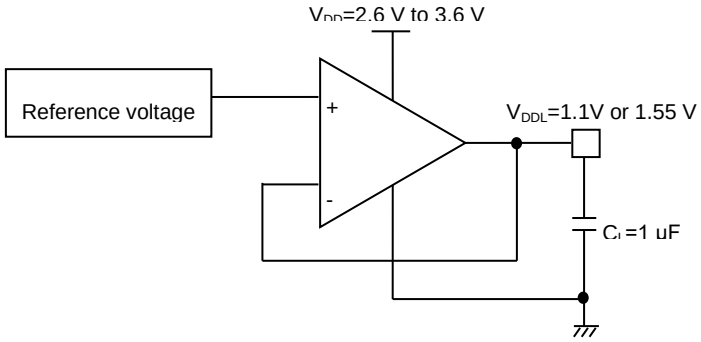


Figure 24-1 General Scheme of Regulator

○Features

Mode	REG_CORE_MCU voltage
STOP mode	1.55 V
HALT mode	1.55 V
HALT-H mode	1.55 V
Program run mode	1.55 V
STOP-D mode (content of RAM and SFR can be retained)	1.1 V

○Configuration

Figure 24-2 shows the configuration of the internal power supply.

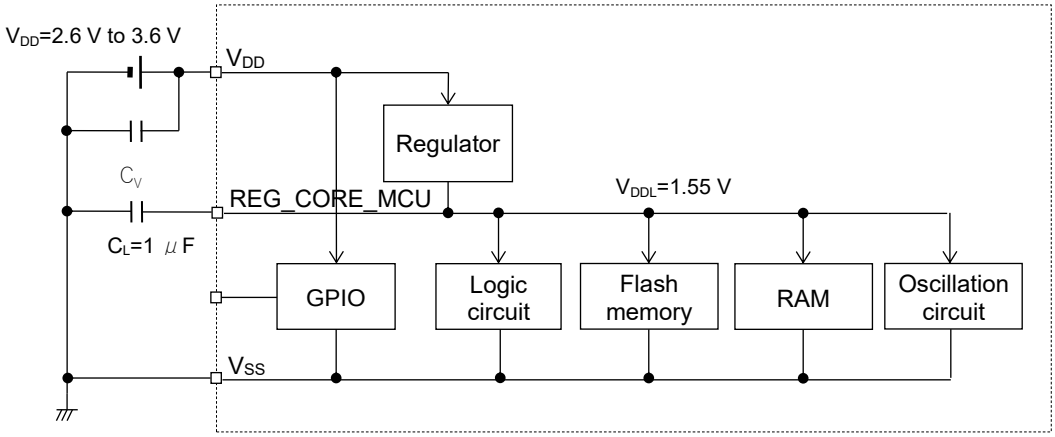


Figure 24-2 Internal Power Supply Configuration

○List of Pins

In order to stabilize REG_CORE_MCU, connect the REG_CORE_MCU pin to V_{SS} via a capacitor (1 μF).

Pin name	I/O	Function
REG_CORE_MCU	-	Internal logic power supply (Internal generated)
V_{REFO}	-	Reference voltage output

[Note]

- **In order to improve the noise resistance, place the inter-power supply bypass capacitor (C_V) and the internal logic voltage (REG_CORE_MCU) capacitor (C_L: 1 μF) in the vicinity of LSI on the user board using the shortest possible wiring without passing through via holes.**
- **The internal logic voltage (REG_CORE_MCU) is unavailable to use for an external device voltage.**

●Flash Memory

ML62Q1532 has the flash memory in the program memory space and data flash area. For details of the program memory space and data flash area, see Chapter 2 "CPU and Memory Space" of “ML62Q1000 Series User’s Manual”. The flash memory is programmable by following three ways.

- The ways of programming the flash memory

Programming method	Tool/Register/Communication	Reference Chapter (ML62Q1000 Series User’s Manual)
Programming by the on-chip debug function	On-chip debug emulator or other flash programmers	Chapter 28 "On chip Debug function"
Self-Programming by using the special function register(SFR)	Special Function Registers(SFRs) for programming the flash memory	Section 25.3 "Self-programming"
Programming by the ISP (In-System Programming) function	UART communication with an external device 3rd Party Flash programmers (*1)	Section 25.4 "ISP function"

*1: Contact the 3rd party manufacturers for details about the Flash programmer.

The specification of the program memory space and data flash of ML7456N is following.

- Program memory space and Data flash area Overview

Product Name	Program memory space		Data flash area	
	Size	Address	Size	Address
ML7456N(ML62Q1532)	64K Byte	0x0:0000 to 0x0:FFFF	4K Byte （128 Byte x 32 Sector）	0x1F:0000 to 0x1F:0FFF

- Program memory space and Data flash area Overview

Item		Program memory space	Data flash area
Erasing and programming unit	Chip erase(ISP only)	All area	All area
	Block erase	16K Byte	All area
	Sector erase	1K Byte	128 Byte
	Programming	4 Byte（32bit）	1 Byte（8bit）
Erasing and programming time	Max. 50ms	Max. 50ms	Max. 50ms
	Block erase		
	Sector erase		
	Max. 80μs	Max. 80μs	Max. 40μs
Programming cycle		100 times	10,000 回
Erasing and programming temperature		0ºC to +40ºC	-40ºC to +85ºC
Background operation(BGO) function		-	Yes
Erasing and programming completion Interrupt		No	Yes

○List of Pins

Programming by the ISP function uses the following pins.

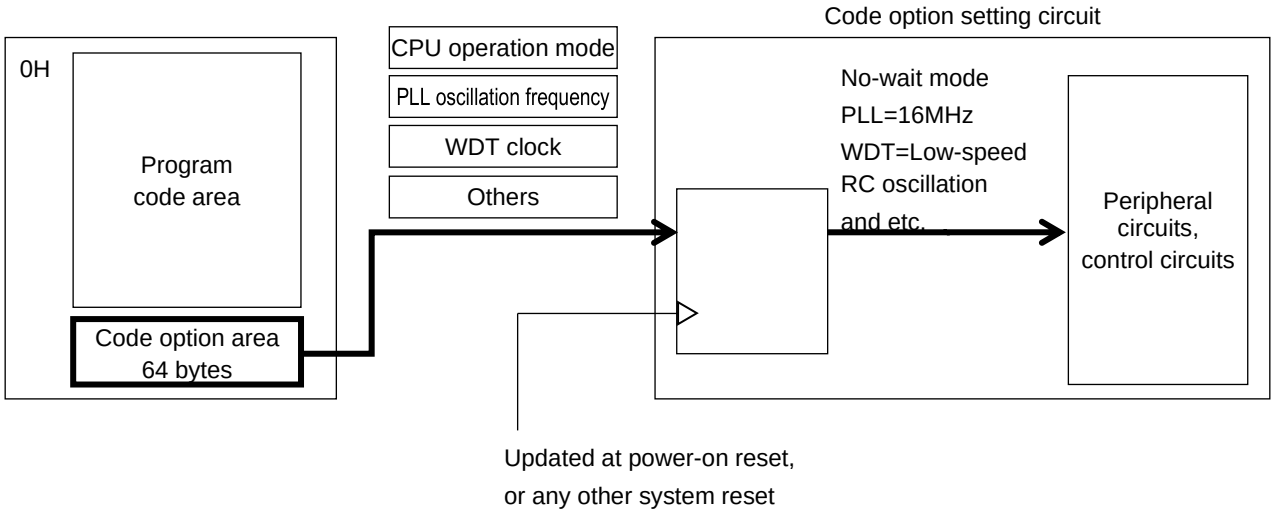
Signal name	I/O	Function
RESET_N	I	Input signal for entering the ISP mode
TEST0	I/O	Input signal for entering the ISP mode and data input/output data in the single wired UART communication

●Code Option

The code option is used to choose the CPU operating mode, PLL reference frequency, watchdog timer operation clock, etc. depending on values written in the code option area of the program memory space.

The hardware automatically refers to data in the code option area when the microcontroller starts up due to one of system resets described below to set each function.

- Power-on reset
- Voltage Level Supervisor reset
- RESET_N pin reset
- Watchdog timer (WDT) overflow reset
- Watchdog timer (WDT) invalid clear reset
- RAM parity error reset
- Unused ROM area access reset



The code option area can be erased or programmed through the on-chip debug function, self-rewrite function of flash memory, or ISP function.

Figure 26-1 Code Option Overview

○Function List

- Enabling or disabling the unused ROM area access reset
- Enabling or disabling the remapping function
- Watchdog timer operation clock (low-speed oscillation LSCLK/WDT oscillation)
- Enabling or disabling the watchdog timer operation
- PLL reference frequency (16 MHz or 24 MHz)
- CPU operation mode (wait mode or no-wait mode)
- The software remap or hardware remap is selectable for the remap function

●On-Chip Debug Function

This function is used by connecting the host PC and LSI through the on-chip debug emulator (hereafter referred to as "On-chip emulator").
On-board debugging or programming is available by using the program development environment software (debugger) installed on the host PC.

○Features

- The following debug functions are provided using the debugger by connecting LSI and On-chip emulator
  - − Emulation
    - Real time emulation
    - Single step emulation
  - − Break
    - Hardware break point break (four points)
    - RAM data matching break
    - Sequential break
    - Trace overflow break
    - Stack overflow/underflow break
    - Unused ROM area access break
    - RAM parity error break
  - − Trace
    - Branch trace
  - − Real time watch
  - − CPU resource display/change
    - Program memory reference/disassembly
    - RAM and SFR display/change
    - Register display/change in the CPU
  - − Program download
    - Program download/read/erase to/from flash memory
    - Data write/read/erase to/from data flash
  - − Peripheral circuit operation continue/stop control during break

    Target peripheral circuits
    - External interrupt
    - Low-speed time base counter
    - 16-bit timer
    - Functional timer
    - Serial communication unit (synchronous serial port/UART)
    - I^2C bus master
    - I^2C bus unit (master/slave)
    - DMA controller
    - Buzzer
    - Analog module

      (Analog comparator, successive approximation type A/D converter, voltage level supervisor (VLS))

- The following program download function is provided using the flash multi-writer by connecting LSI and On-chip emulator.
  - Program download
  - Erasing/Programming the program memory space
  - Erasing/Programming the data flash memory area

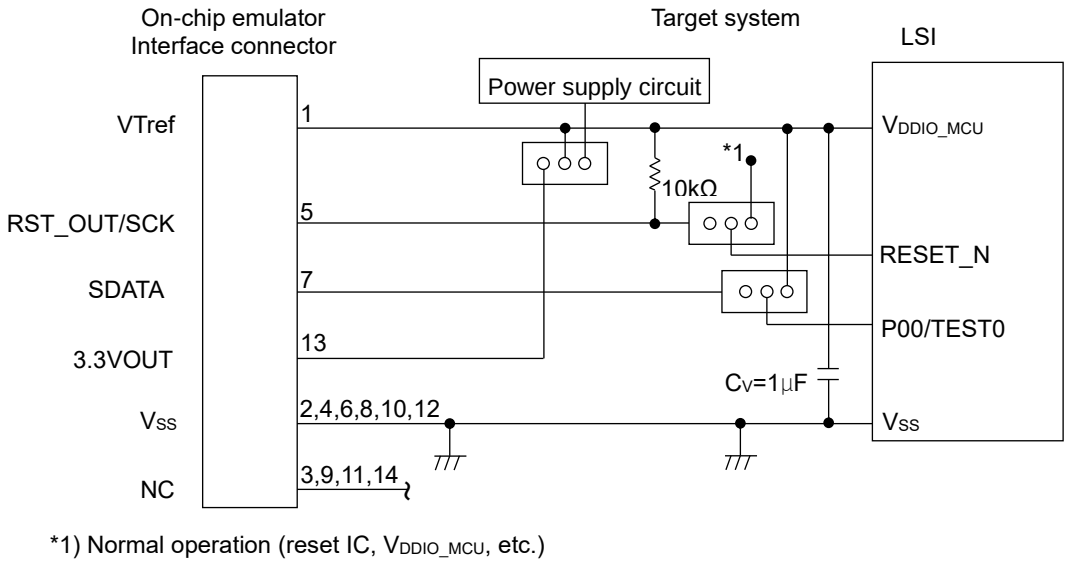
○Configuration

When using the on-chip debug function, two methods are available for power supply to LSI as described below:

- Use the 3.3 VOUT power supply (+3.3 V/100 mA) of On-chip emulator
- Use the power supply of the target system (V_{DDIO_MCU}=2.6 V to 3.6 V)

・ Using 3.3 VOUT Power Supply (+3.3 V/100 mA) of On-chip Emulator

Figure 28-1 shows a connection example when using the 3.3 VOUT power supply (+3.3 V/100 mA) of On-chip emulator.

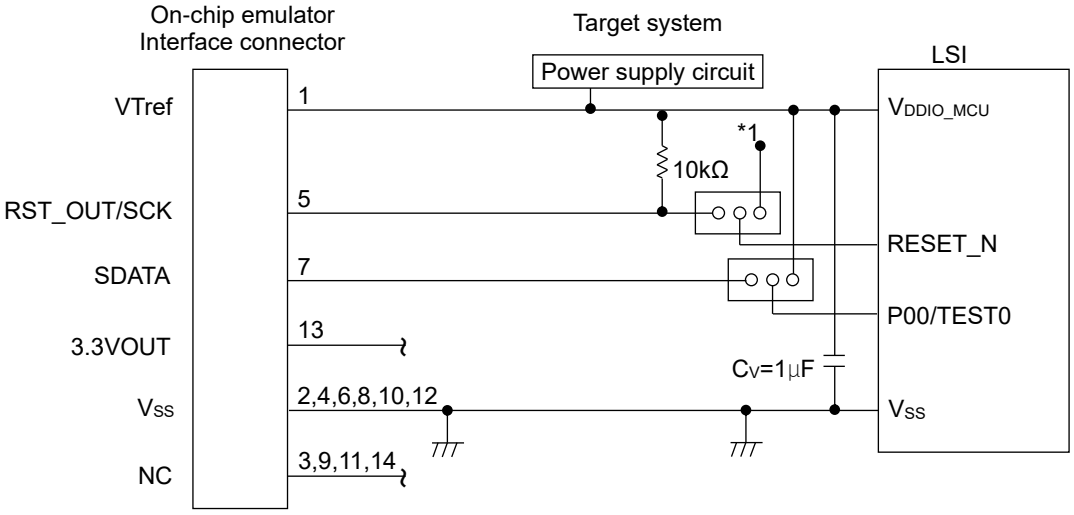


*1) Normal operation (reset IC, V_{DDIO_MCU}, etc.)

Figure 28-1 Connection Example When Using On-chip Emulator 3.3 VOUT Power Supply

・ Using Power Supply of Target System (V_{DDIO_MCU}=2.6 V to 3.6 V)

Figure 28-2 shows a connection example when using the power supply (V_{DDIO_MCU}=2.6 V to 3.6 V) of the target system.



*1) Normal operation (reset IC, $V_{DDIO\ MCU}$, etc.)

Figure 28-2 Connection Example When Using Target System Power Supply

○List of Pins

The following pins are used for the on-chip debug function.

Signal name	I/O	Function
RESET_N	I	Reset input
P00/TEST0	I/O	On-chip debug function signal input/output

●Safety Function

ML62Q1532 has the safety functions to make a safe stop in case a failure is detected by executing the self-diagnosis software, available to support IEC60730/60335 Class B.

○Features

- Safety Functions on the LSI

Function Name	Description	Control by SFR
RAM guard	Protect from the miss-writing to the specified RAM area	Available
SFR guard	Protect from the miss-writing to the specified SFR	Available
Successive approximation type A/D converter test	Successive approximation type AD converter test function	Available
RAM parity error detection	RAM parity error check and generates a reset on error (enable/disable reset by SFR, with reset status flag and parity error flag)	Available
ROM unused area access reset	Make a reset in case the CPU executes an instruction in the unused area (enable/disable reset by the code option, with reset status flag)	-
Clock mutual monitoring	Monitor to check whether the oscillation of the high-speed and low-speed clocks are normal	Available
CRC calculation	Detect data error in the flash memory or data error in communications	Available
UART self-test function	Make the UART self-test	Available
SSIO self-test function	Make the SSIO self-test	Available
I^2C self-test function	Make the I^2C self-test function	Available
WDT counter read	WDT counter read function	Available
Port output level self-test function	General port self-test function	Available
Clock backup function and the self-test	Switch automatically to the low-speed RC oscillation in case the low-speed crystal oscillation stopped	Available
MCU status interrupt	Control interrupts generated by RAM parity error, automatic CRC calculation completion, and data flash erase/program completion.	Available

■RF

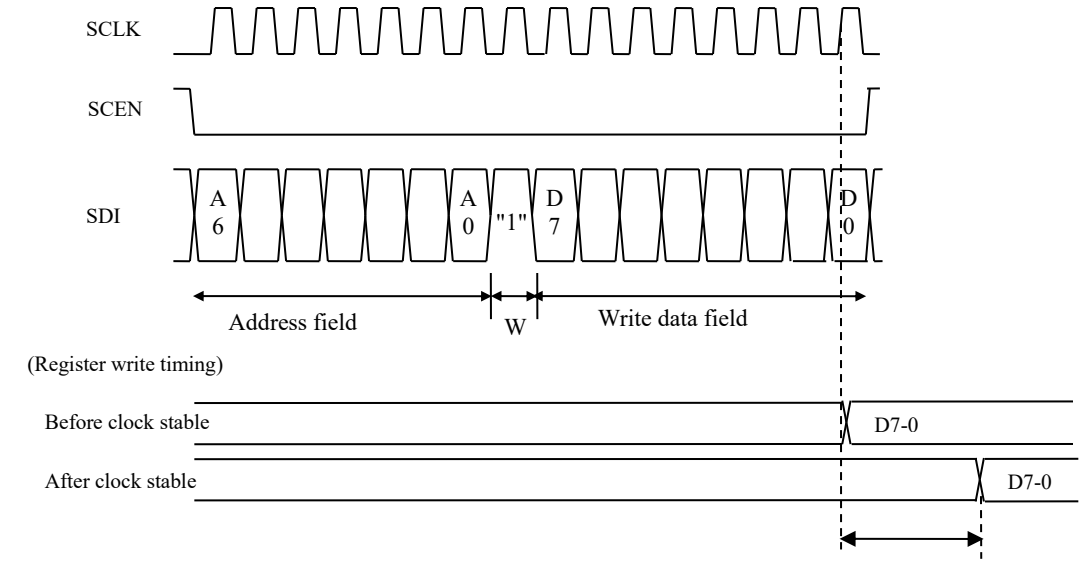
●Host Interface

○Serial Peripheral Interface (SPI)

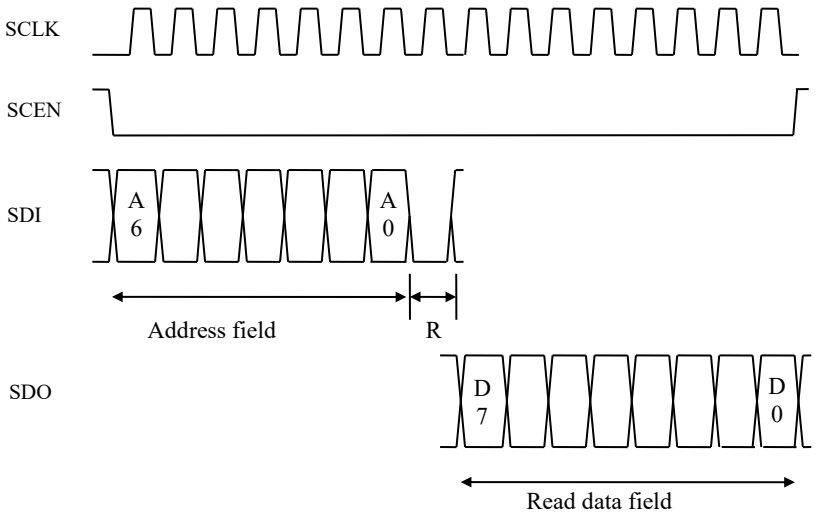
This LSI has a serial peripheral interface (hereafter referred to as SPI). This LSI has a SPI, which supports slave mode. Host MCU can read/write to the RF part registers and on-chip FIFO using MCU clock. Single access mode and burst access mode are also supported.

[Single access mode timing chart]
In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 data. During write operation, if SCEN is set to “H”, the control section will be reset. After the internal clock is stabilized, the data will be written into the register in synchronization with the internal clock.

[Write]



[Read]



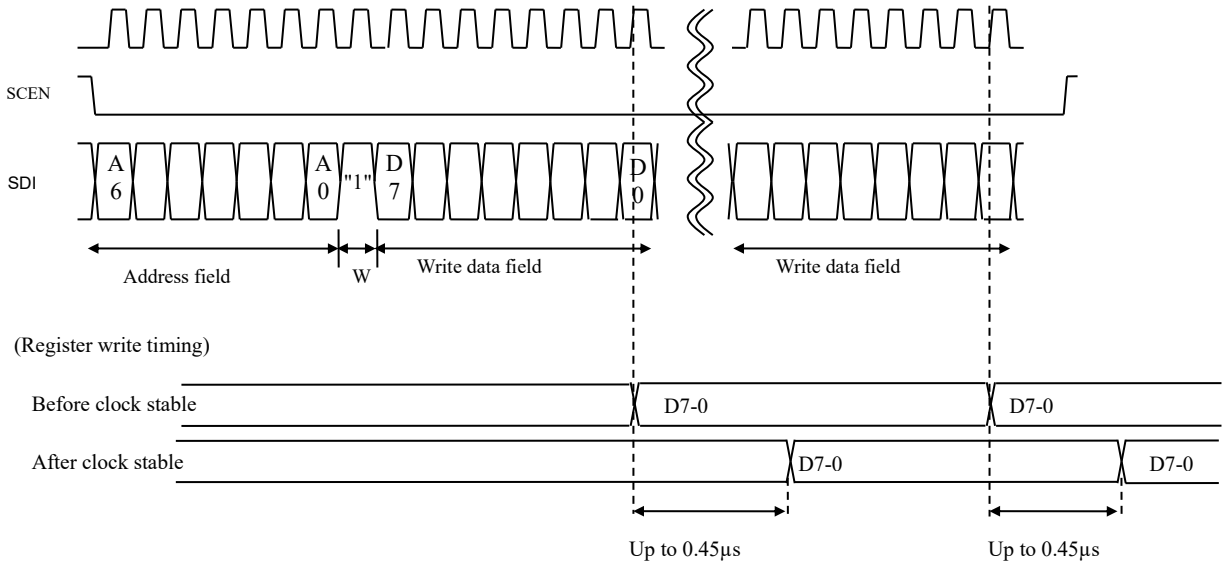
[Burst access mode timing chart]

By maintaining SCEN line as “L”, Burst access mode will be active. By setting SCEN line to “H”, exiting from the burst access mode. During burst access mode, address will be automatically incremented. When SCEN line becomes “H” before Clock for D0 is input, data transaction will be aborted.

[Note]

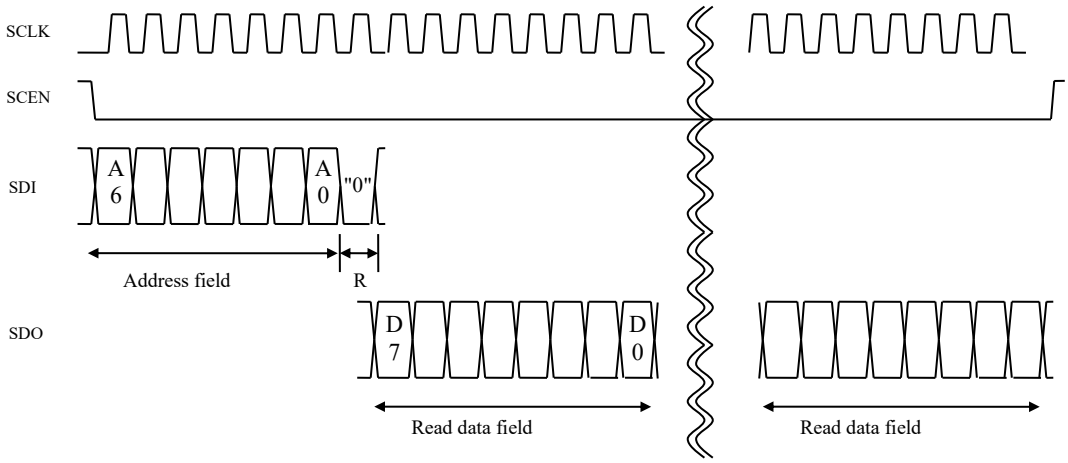
If access destination is [WR_TX_FIFO: B0 0x7C] or [RD_FIFO: B0 0x7F] register, address will not be incremented, allowing continuous access to the FIFO.

[Write]



(Register write timing)

[Read]



●LSI State Control

The LSI state can be changed by setting registers below.

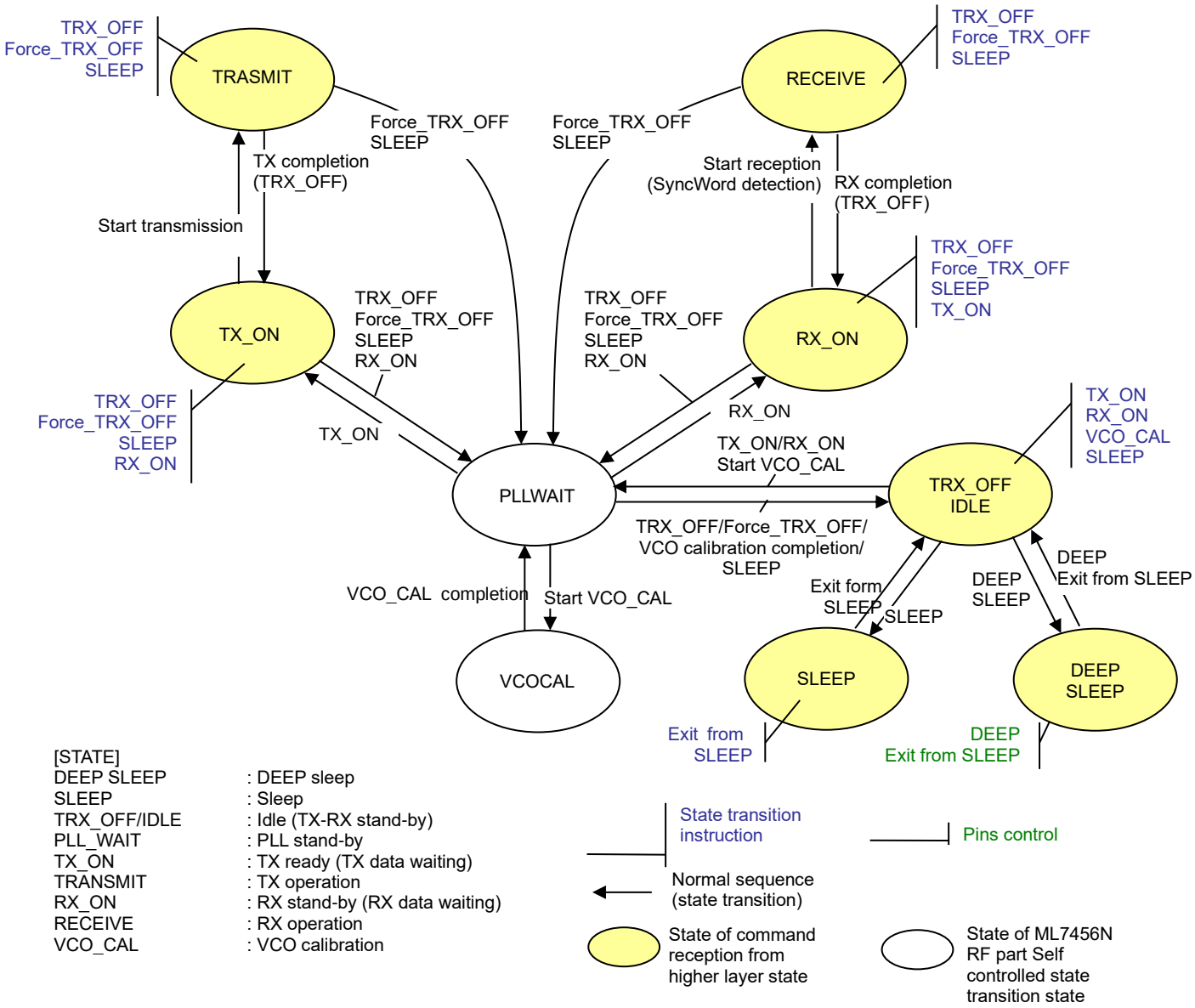
State transition command	Registers setting
TX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x9
RX_ON	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x6
TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x8
Force_TRX_OFF	SET_TRX ([RF_STATUS: B0 0x0B(3-0)]) = 0x3
SLEEP	SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1
VCO_CAL	VCO_CAL_START([VCO_CAL_START: B0 0x6F(0)])= 0b1

The LSI state can be changed autonomously (please refer to the following table.) If one of the following conditions is met, state is changed automatically according to the following table.

Function	Register
Automatic TXON after FIFO write completion	AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)])
Automatic TXON during FIFO write	FAST_TX_EN([RF_STATUS_CTRL: B0 0x0A(5)])
RF state setting after packet transmission completion	TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)])
RF state setting after packet reception completion	RXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(3-2)])
Automatic RXON/TXON by Wake-up timer function	[SLEEP/WU_SET:B0 0x2D]
Automatic VCO calibration after recovering from SLEEP	AUTO_VCOCAL_EN([VCO_CAL_START: B0 0x6F(4)])
Automatic SLEEP by Timer	[SLEEP/WU_SET: B0 0x2D]
Automatic SLEEP by high speed carrier checking mode	FAST_DET_MODE_EN ([CCA_CTRL:B0 0x39(3)])
Automatic TX_ON by high speed carrier checking mode	CCADONE_MODE([ED_CTRL:B0 0x41(6)])
Force_TRX_OFF after PLL unlock detection during TX	PLL_LD_EN([PLL_LOCK_DETECT: B1 0x0B(7)])

Each LSI state transition control follows the state diagram shown below.

○LSI State Transition Diagram



LSI state diagram

○SLEEP Setting

DEEP_Sleep mode: Powers for all blocks except IO pins are turned off.
Sleep mode: Main regulator and 36MHz oscillation circuits are turned off. But sub-regulator is turned-on.
The following registers can be programmed to control SLEEP state.

Function	Register
Power control	PDN_EN([SLEEP/WU_SET: B0 0x2D(1)])
Wake-up setting	WAKEUP_EN([SLEEP/WU_SET: B0 0x2D(4)])
Wake-up timer clock source setting	WUT_CLK_SOURCE([SLEEP/WU_SET: B0 0x2D(2)])
Internal RC oscillator circuit control	RC32K_EN ([CLK_SET2: B0 0x03(3)])

Setting method and internal state for DEEP_SLEEP and various SLEEP modes are as follows:

SLEEP mode	Setting method	Main regulator	Sub regulator	36MHz oscillator circuit	RC oscillator circuit	Low clock timer	TX FIFO
DEEP SLEEP	RESETN pin="L" REGPDIN pin="H"	OFF	OFF	OFF	OFF	OFF	OFF
SLEEP1	[SLEEP/WU_SET: B0 0x2D(5-0)] = 0b00_0111 [CLK_SET2: B0 0x03(3)] = 0b0	OFF	ON	OFF	OFF	OFF	OFF
SLEEP2	[SLEEP/WU_SET: B0 0x2D(5-0)] = 0b11_0111 [CLK_SET2: B0 0x03(3)] = 0b1	OFF	ON	OFF	ON	ON	OFF

Contents of registers are not kept during DEEP_SLEEP. Contents of registers are kept during SLEEP1 and SLEEP2. However, in SLEEP1 and SLEEP2, contents of TX FIFO are not kept, because power to FIFO is turned off.

○Notes to Set RF State

This LSI is able to change the RF state transition autonomously (without RF state transition commands by register settings), by issuing RF state transition commands from LSI . (please refer to ”LSI state transition instruction”). If both timing of operation (autonomous state and state change from MCU command) overlapped, unintentional RF state may occur. Timing of autonomous state RF change is described in the following table. Care must be taken not to overlap the conditions.

Function	RF state change (before => after)	RF state transition timing (not from Host MCU command)	Recommended process
Automatic TX	TRX_OFF/RX_ON => TX_ON	After TX data reception completion interrupt occurs, {[TX_RATE_H/L: B1 0x02/03)] setting value * 2 / 36} [µs] period	Perform a write access to [RF_STATUS:B0 0x0B] after RF state transition completion interrupt occurs or GET_TRX ([RF_STATUS:B0 0x0B(7-4)]) has changed to the expected state.
FAST_TX mode		After FIFO write access amount exceeds trigger level + 1, {[RX_RATE1_H/L:B1 0x04/05] setting value * 5 / 36} [µs] period	
After TX completion RF status setting	TX_ON => TRX_OFF	After TX completion interrupt occurs, {[TX_RATE_H/L:B1 0x02/03] setting value * 2 / 36} [µs] period	
	TX_ON => RX_ON		
	TX_ON => SLEEP		
After RX completion RF status setting	RX_ON => TRX_OFF	After data RX completion interrupt occurs, {[RX_RATE1_H/L:B1 0x04/05] setting value * 2 / 36} [µs] period	
	RX_ON => TX_ON		
	RX_ON => SLEEP		
Wake-up timer	SLEEP => TX_ON	After wake-up timer completion, low speed wake-up timer clock cycle duration	
	SLEEP => RX_ON		
	SLEEP => VCO_CAL => TX_ON	After wake-up timer completion interrupt (INT[6]: group1), before VCO calibration completion interrupt (INT[1] group1).	After a VCO calibration completion interrupt occurs, perform an access to [RF_STATUS:B0 0x0B] and BANK2.
	SLEEP => VCO_CAL => RX_ON		
Continuous operation timer	TX_ON => SLEEP	After continuous operation timer completion, low speed wake-up timer clock cycle duration	Perform a write access to [RF_STATUS:B0 0x0B] after RF state transition completion interrupt occurs or GET_TRX ([RF_STATUS:B0 0x0B(7-4)]) has changed to the expected state.
	RX_ON => SLEEP		
High speed carrier checking	RX_ON => SLEEP	After CCA completion interrupt, 6.3 [µs] period.	
	RX_ON => TX_ON		
PLL unlock detection	TX_ON => TRX_OFF	After PLL unlock detection interrupt (INT[2] group1), 24 [µs] (*1) period.	24 µs (*1) after the interrupt occurs, perform a write access to [RF_STATUS:B0 0x0B].

(*1) Depends on the ramp down time setting.

●Packet Handling Function

○Packet Format

ML7456N RF part supports Wireless M-Bus frame Format A/B, and Format C/D which is non Wireless M-Bus universal format. The following packet handling are supported in FIFO mode or DIO mode

- Preamble and SyncWord automatic insertion (TX) --- Common to DIO/FIFO mode
- Preamble and SyncWord automatic detection (RX) --- Common to DIO/FIFO mode
- Preamble and SyncWord automatic deletion (RX) --- Common to DIO/FIFO mode
- CRC data insertion --- FIFO mode only
- CRC check and error notification --- Common to DIO/FIFO mode

Packet format registers are as follows:

Function	Register
Packet format setting	PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)])
RX extended link layer mode disable	RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])
Data area bit order setting	DAT_LF_EN([PKT_CTRL1: B0 0x04(4)])
Length area bit order setting	LEN_LF_EN([PKT_CTRL1: B0 0x04(5)])
Extended link layer mode setting	EXT_PKT_MODE([PKT_CTRL1: B0 0x04(7-6)]) EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)])
Length field setting	LENGTH_MODE([PKT_CTRL2: B0 0x05(1-0)])

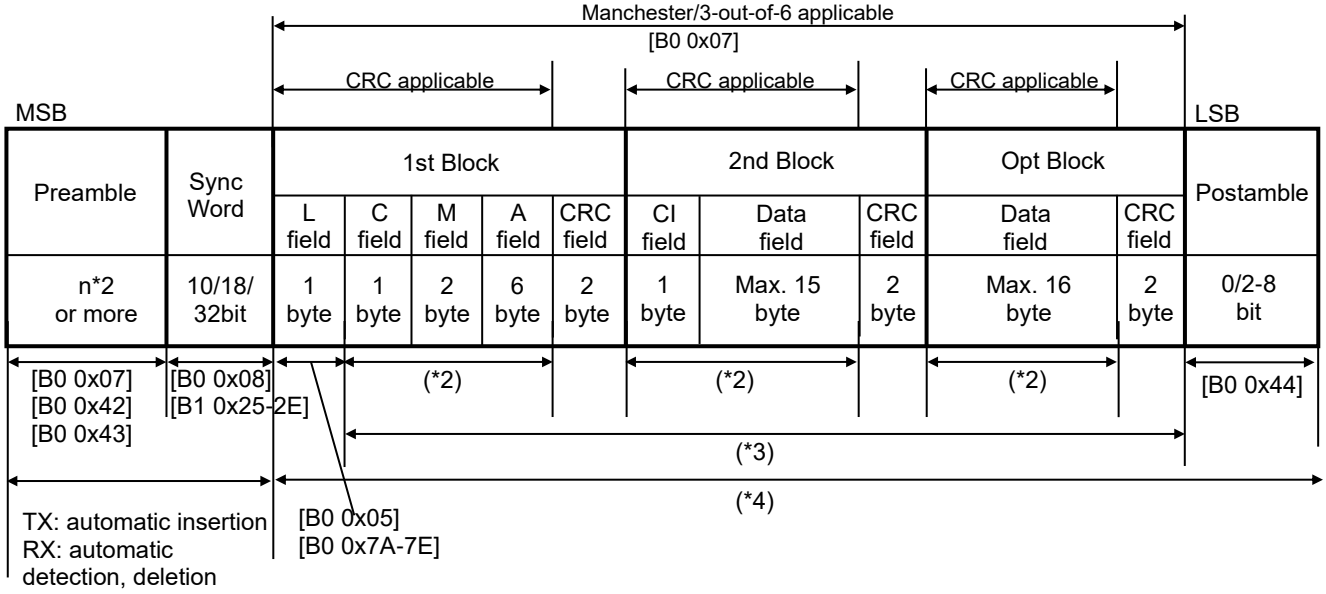
Packet formats supported by ML7456N RF part are as follows.

(1) Format A (Wireless M-Bus)

To use Format A, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b00. B0 0x04(1-0)]) = 0b00

Format A consists of 1st Block, 2nd Block and Optional Block(s). Each block has 2 bytes of CRC. “L-field” (1st byte of 1st Block) indicates packet Length, which indicates the total byte count of data subsequent to C-field of the 1st Block excluding CRC and Postamble. In addition, the 2nd Block or Optional Block subsequent to the 1st Block is added according to the Length.

The following [] indicates register address [bank #, address].



*1: Each mode of Wireless M-Bus has different minimum value of n.

*2: Indicates TX FIFO data storage area upon TX.

*3: Indicates RX FIFO data storage area upon RX.

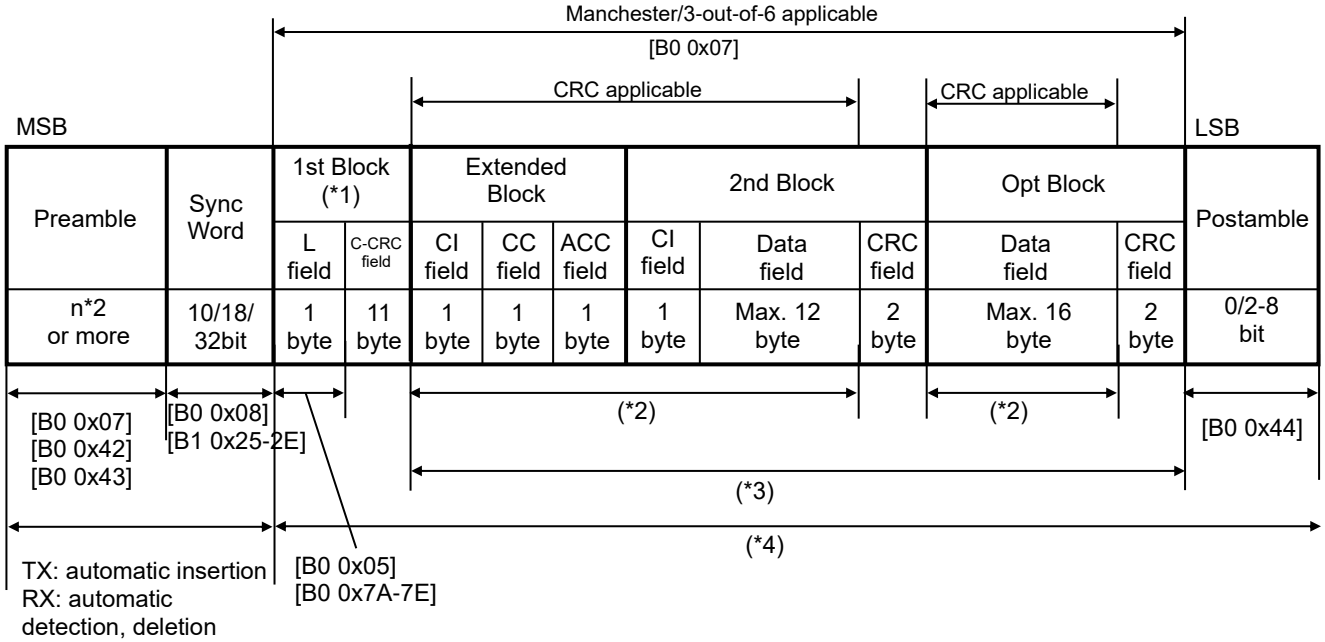
*4: Indicates DCLK/DIO output area at RXDIO_CTRL [DIO_SET: B0 0x0C(7-6)])=0b10)

Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) is set to 0x8C/0x8D/0x8E/0x8F, Extended Link Layer Format is applied and the packet format is extended as follows.

(a) CI-field = 0x8C

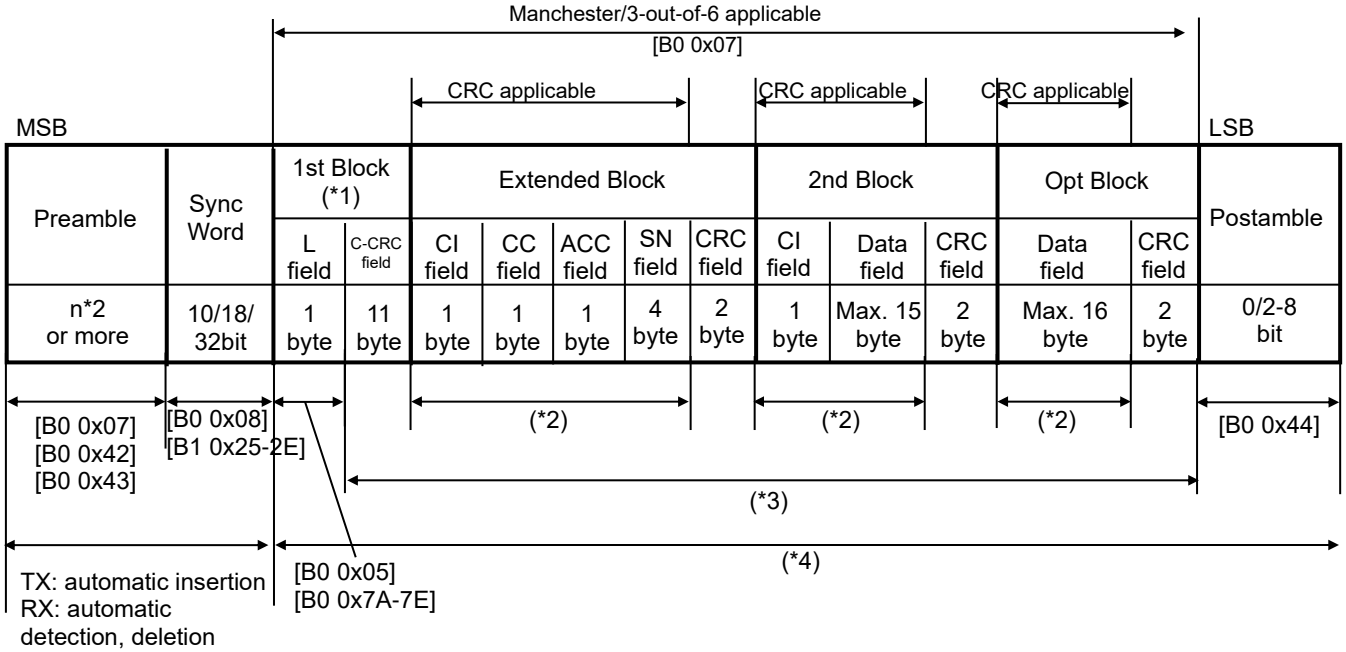
If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b01 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



*1: 1st Block is identical to normal Format A.
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(b) CI-field = 0x8D

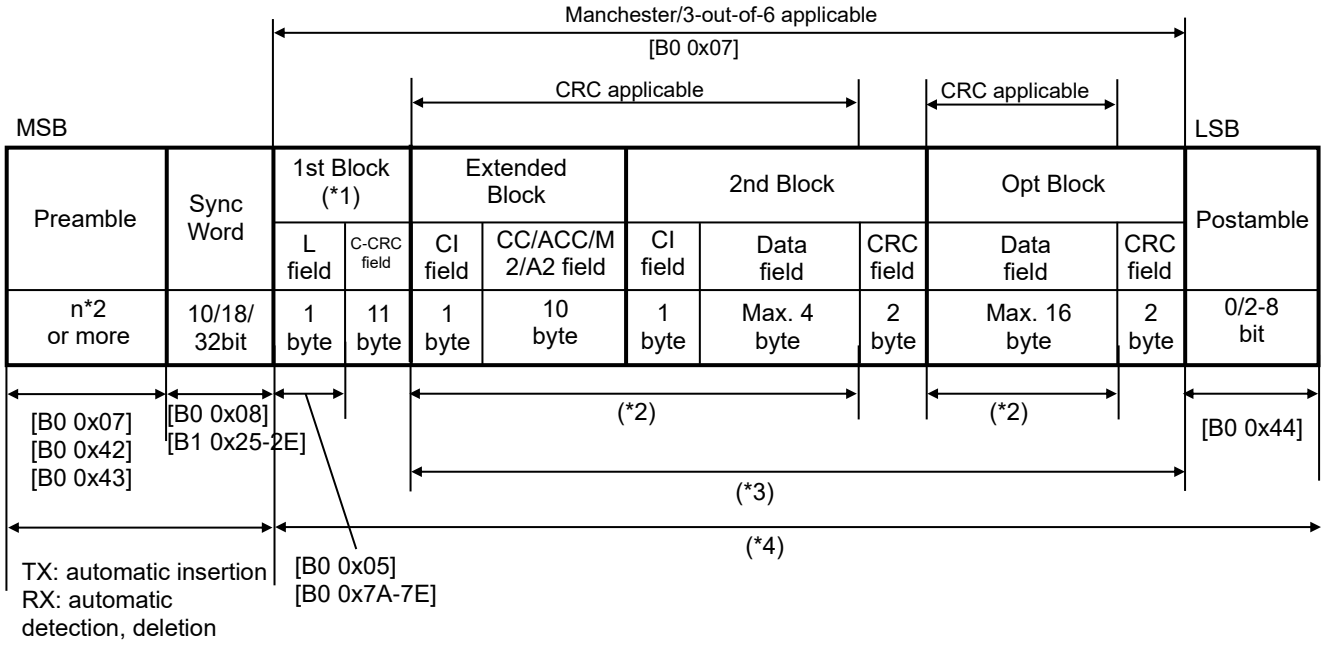
If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b10 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



*1: 1st Block is identical to normal Format A..
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(c) CI-field = 0x8E

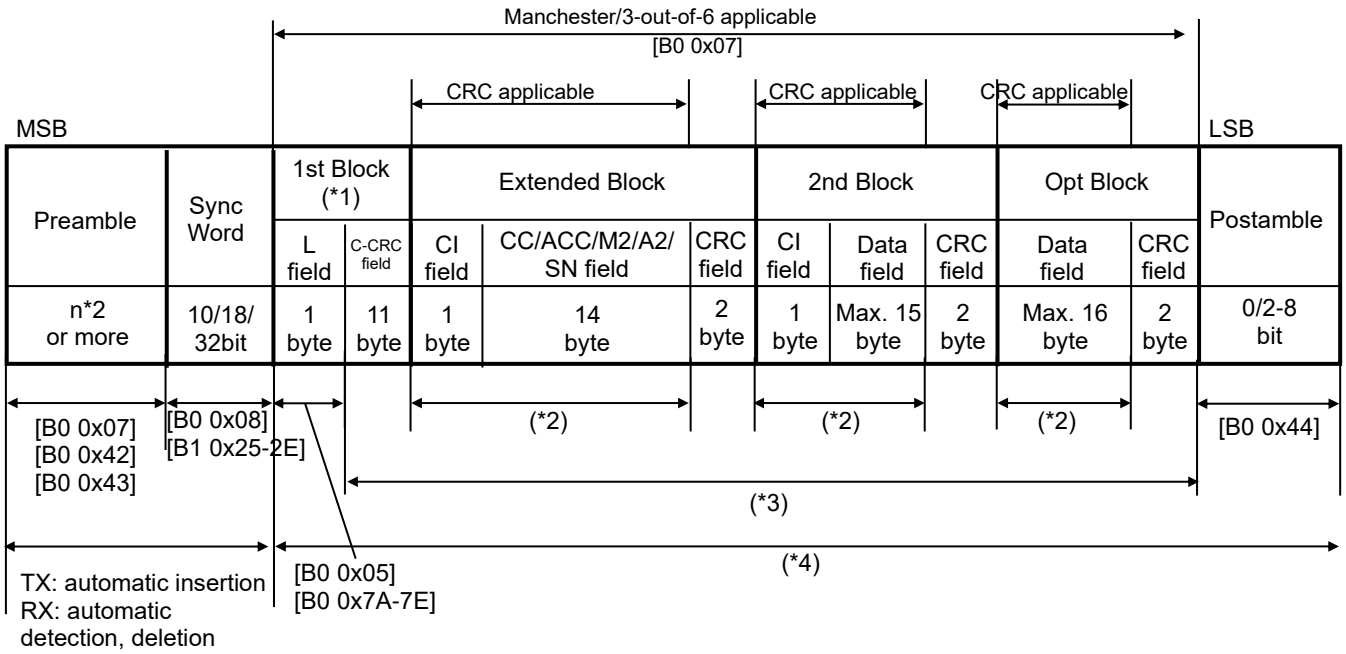
If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b01. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



*1: 1st Block is identical to normal Format A.
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(d) CI-field = 0x8F

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b10. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.

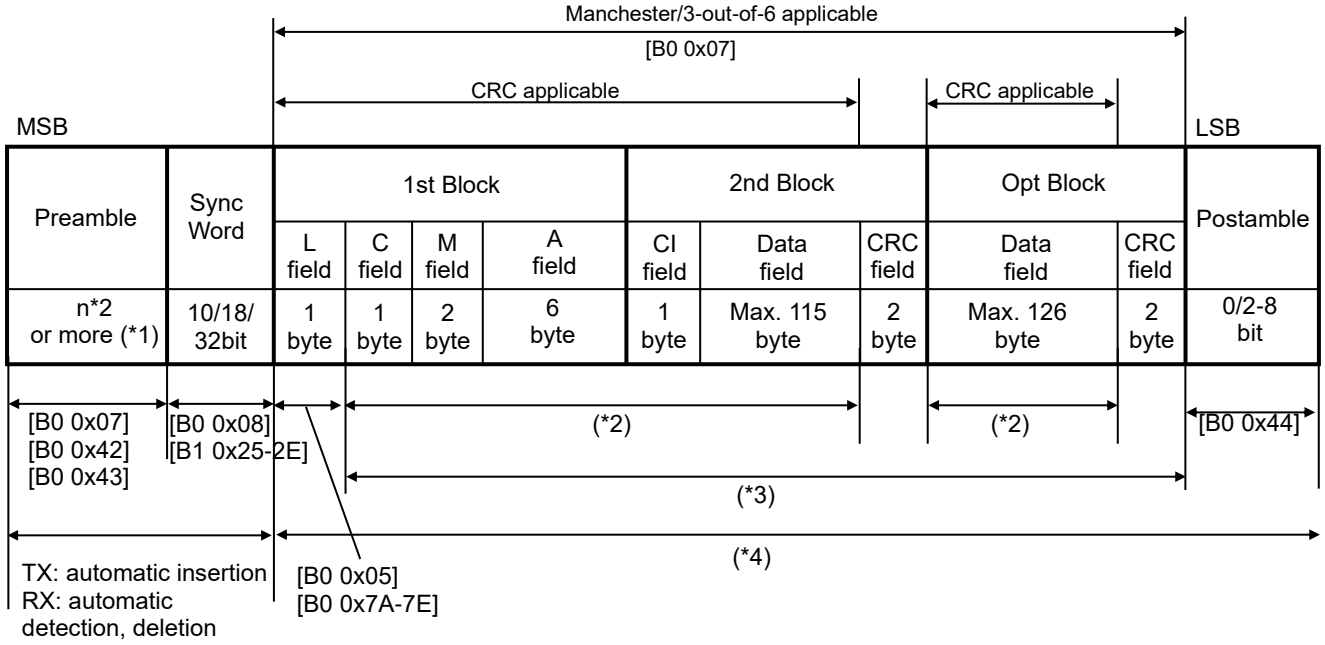


*1: 1st Block is identical to normal Format A..
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(2) Format B (Wireless M-Bus)

To use Format B, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b01.
Format B consists of 1st Block, 2nd Block or Optional Block. Each block after 2nd Block has 2 bytes of CRC. “L-field” (1st byte of 1st Block) indicates packet Length, which indicates the total byte count of data from C-field to final CRC data of the 1st Block. In addition, the 2nd Block or Optional Block subsequent to the 1st Block is added according to the Length.

The following [] indicates register address [bank #, address].



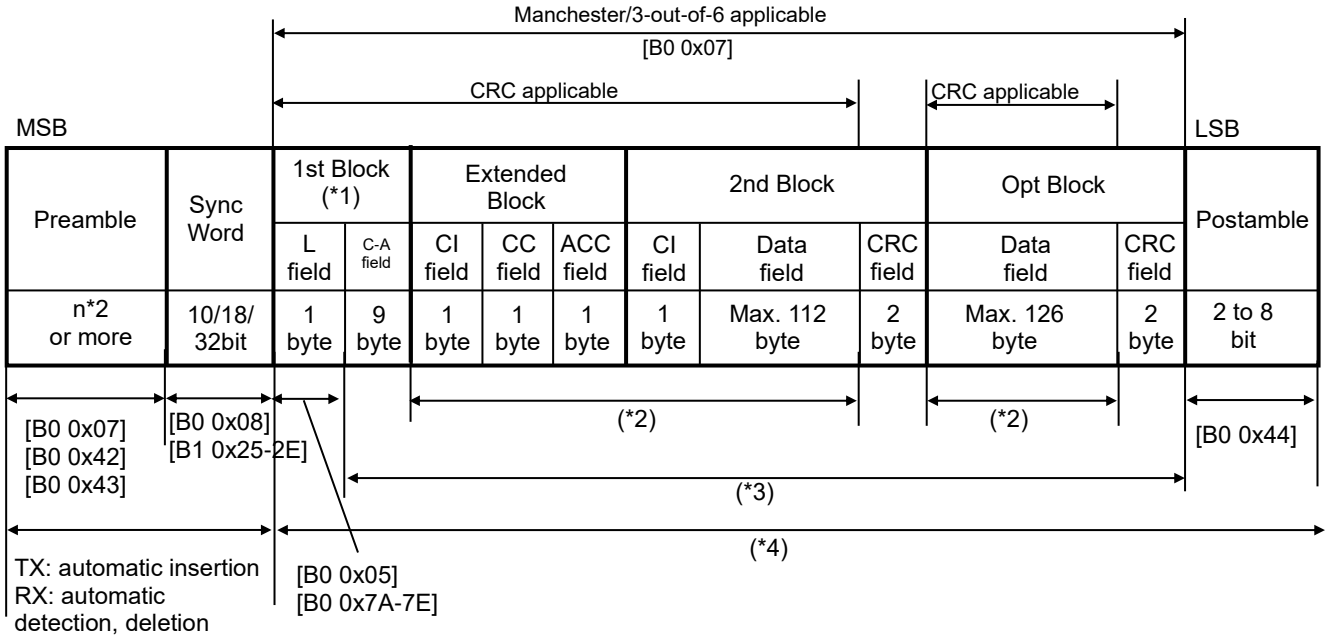
*1: Each mode of Wireless M-Bus has different minimum value of n.
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block) is set to 0x8C/0x8D/0x8E/0x8F, Extended Link Layer Format is applied and the packet format is extended as follows.

(a) CI-field = 0x8C

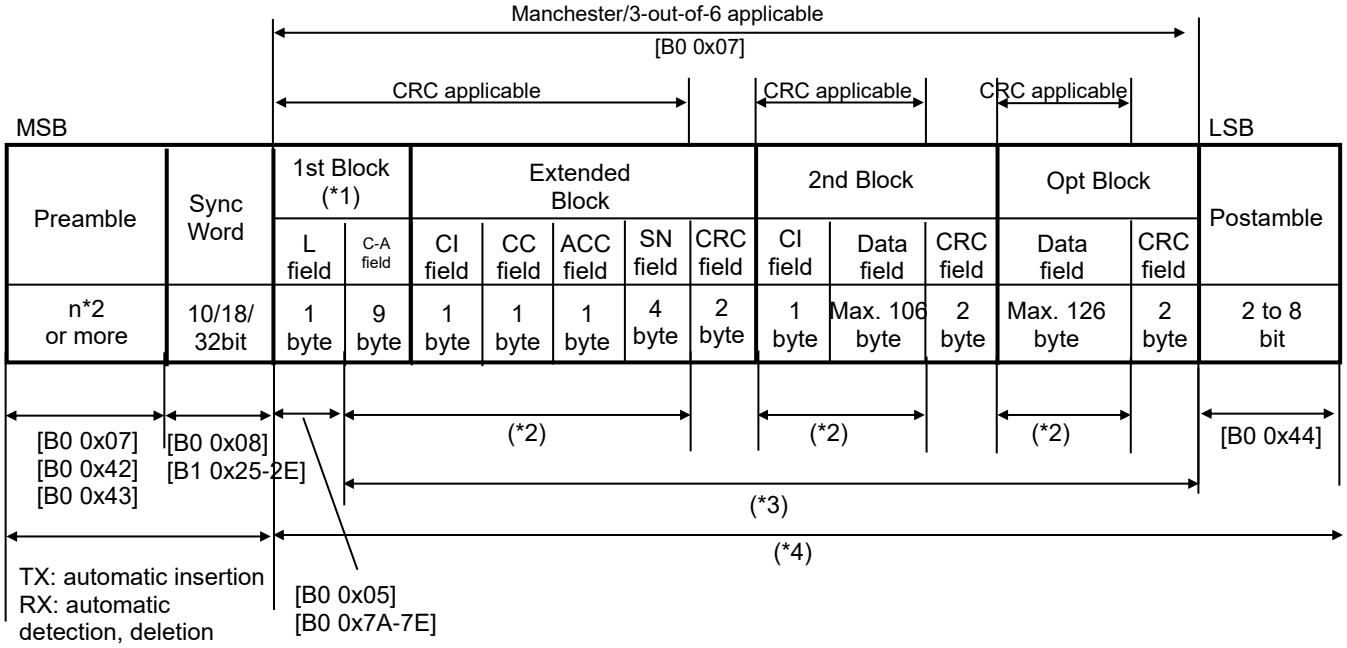
If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b01 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



*1: 1st Block is identical to normal Format B..
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(b) CI-field = 0x8D

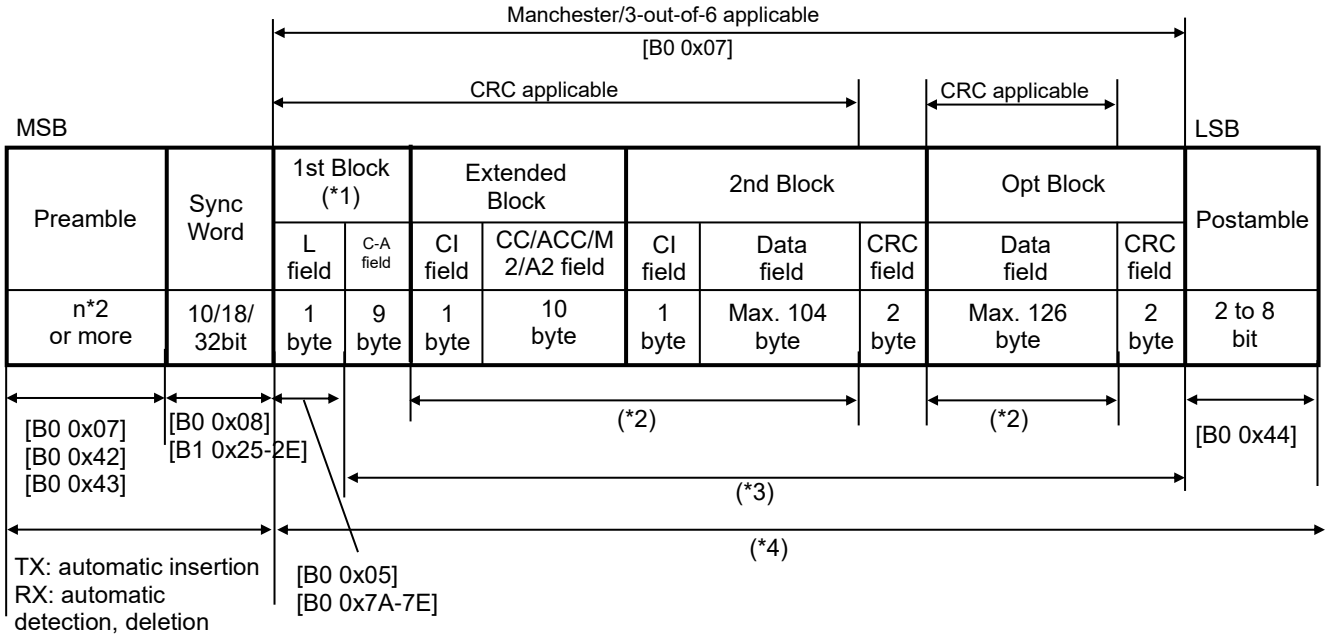
If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b10 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b00. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



*1: 1st Block is identical to normal Format B.
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(c) CI-field = 0x8E

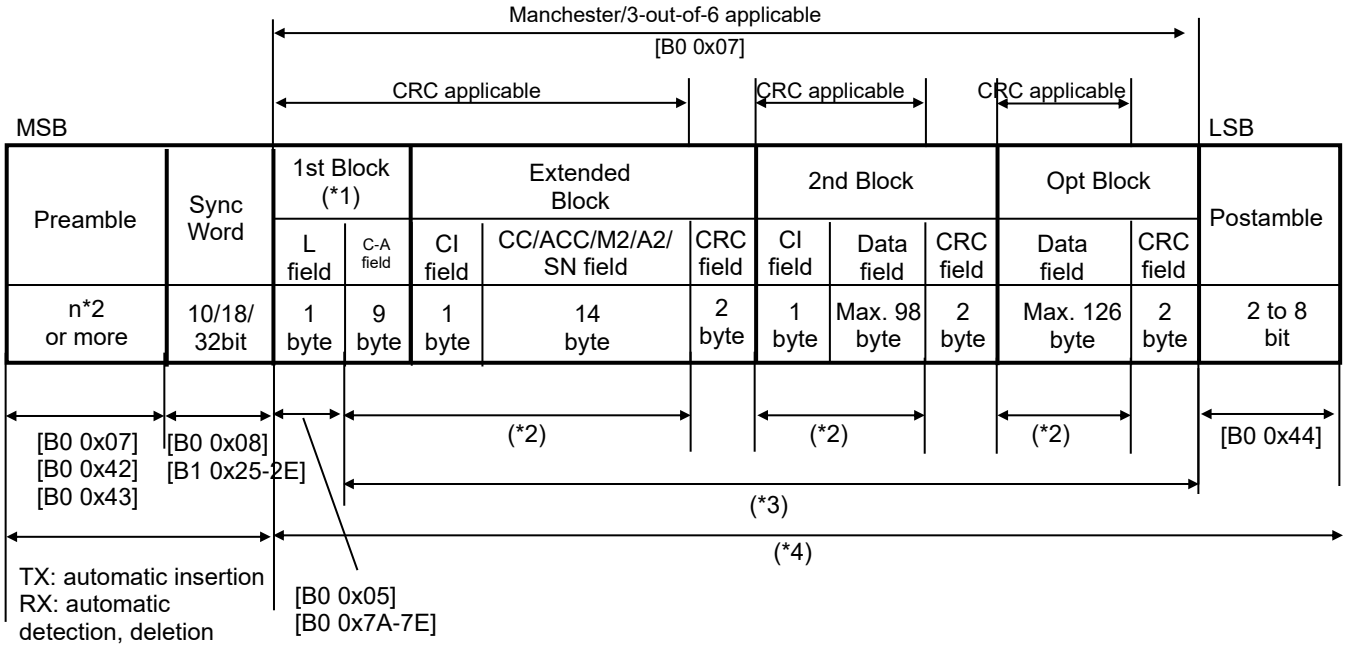
If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b01. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



*1: 1st Block is identical to normal Format B..
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(d) CI-field = 0x8F

If using the extended format upon TX, set EXT_PKT_MODE[PKT_CTRL1: B0 0x04(7-6)]) = 0b00 and EXT_PKT_MODE2([DATA_SET2: B0 0x08(7-6)]) = 0b10. If RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)]) = 0b0 is set for RX, whether or not the RX packets are extended packet format is judged automatically and the RX process is carried out.



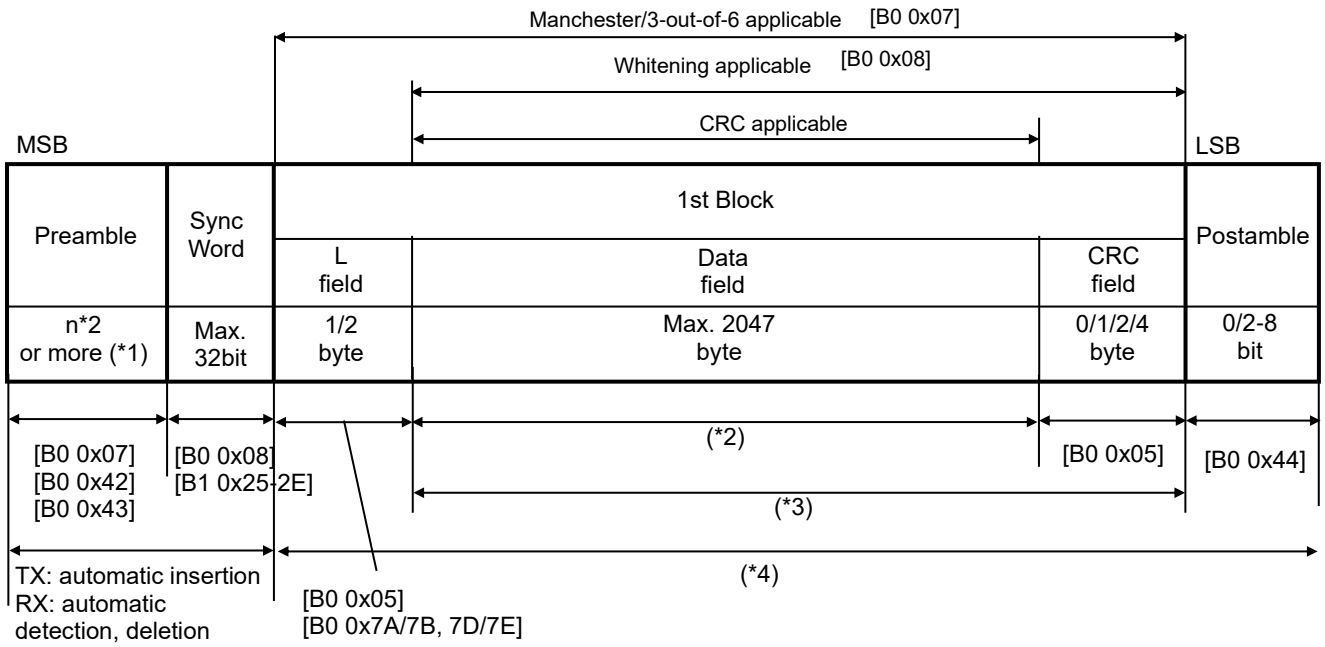
*1: 1st Block is identical to normal Format B..
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(3) Format C (non-Wireless M-Bus, general purpose format)

To use Format C, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b10.

Format C consists of 1st Block only, which has 2 bytes of CRC. "L-field" (first one or two bytes of 1st Block) indicates packet Length, which indicates the total byte count from Data-field to final CRC data. Data Whitening function is supported.

The following [] indicates register address [bank #, address].

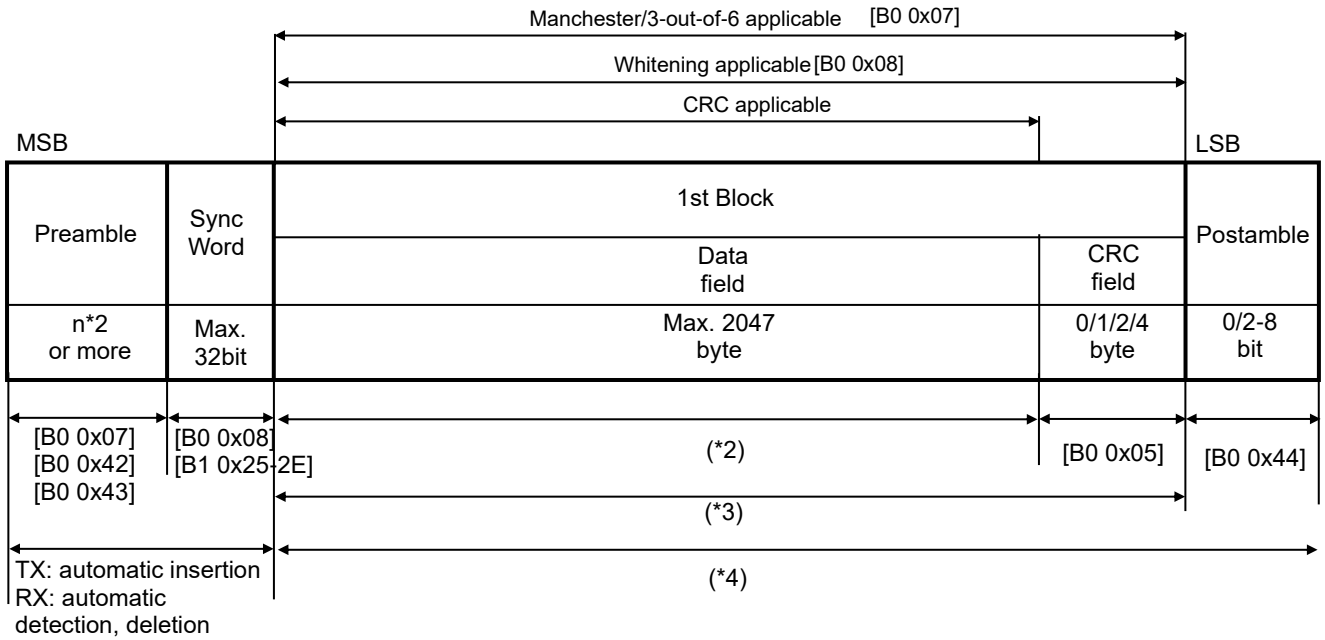


*1: Preamble length (n) is can be set to arbitrary value.
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

(4) Format D (non-Wireless M-Bus, general purpose format)

To use Format D, set PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b11. B0 0x04(1-0)]) = 0b11.
Format D consists of 1st Block only, which starts with Data field followed by CRC-field (selectable from 0/1/2 bytes). "L-field" indicates the total byte count from Data-field to final CRC data and is set by [TX_PKT_LENGTH: B0 0x7A/0x7B] or [RX_PKT_LENGTH: B0 0x7D/0x7E].

The following [] indicates register address [bank #, address].



*1: Preamble length (n) is can be set to arbitrary value.
*2: Indicates TX FIFO data storage area upon TX.
*3: Indicates RX FIFO data storage area upon RX.
*4: Indicates DCLK/DIO output area at RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b10.

○CRC Function

ML7456N RF part has CRC32,CRC16 and CRC8 function. CRC is calculated and appended to TX data. CRC is checked for RX data. The following modes are used for automatic CRC function. In addition, they can be set using the registers shown in the following table.

- FIFO mode --- RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b00
- DIO mode --- RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b11

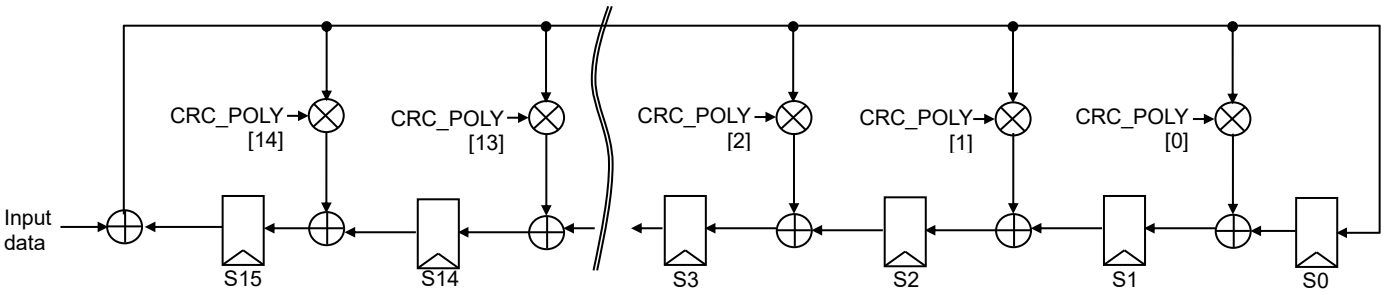
Function	Register
TX CRC setting	TX_CRC_EN([PKT_CTRL2: B0 0x05(2)])
RX CRC setting	RX_CRC_EN([PKT_CTRL2: B0 0x05(3)])
CRC length setting	CRC_LEN([PKT_CTRL2: B0 0x05(5-4)])
CRC complement value OFF setting	CRC_COMP_OFF([PKT_CTRL2: B0 0x05(6)])
CRC polynomial setting	[CRC_POLY3/2/1/0: B1 0x16/17/18/19]
CRC error status	[CRC_ERR_H/M/L: B0 0x13/14/15]
CRC length setting 2 enable	CRC_LEN2_EN([CRC_ERR_H: B0 0x13(7)])
CRC length setting 2	CRC_LEN2([CRC_ERR_H: B0 0x13(6-5)])

Any CRC polynomials for CRC32/CRC16/CRC8 can be specified. Reset value is as follows:

CRC16 polynomial = $x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$ (reset value)

* CRC result data can be inverted by CRC complement value OFF setting.

CRC data will be generated by the following circuits. By programming [CRC_POLY3/2/1/0] registers, any CRC polynomials can be supported. Generated CRC will be transferred from the left most bit (S15). If the CRC function is used for data shorter than CRC length (3-byte data of CRC32 only), data 0s will be added before performing CRC calculation. CRC check result is indicated in [CRC_ERR_H/M/L] registers. Unlike Format C, Format A/B can include multiple CRC-fields in one packet. For multiple CRC-fields, the CRC check result closest to L-field will be indicated in CRC_ERR[0] ([CRC_ERR_L:B0 0x15(0)]). Subsequent bit will be indicated in CRC_ERR from MSB in sequence.



※ ⊕ : Exclusive OR

Example: CRC generation circuits

General polynomial can be programmed by below [CRC_POLY3/2/1/0] register setting. CRC length can be set by CRC_LEN.

CRC polynomial		[CRC_POLY3/2/1/0]			
		(B1 0x16)	(B1 0x17)	(B1 0x18)	(B1 0x19)
CRC8	$x^8 + x^2 + x + 1$	0x00	0x00	0x00	0x03
CRC16	$x^{16} + x^{12} + x^5 + 1$	0x00	0x00	0x08	0x10
	$x^{16} + x^{15} + x^2 + 1$	0x00	0x00	0x40	0x02
	$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$	0x00	0x00	0x1E	0xB2
CRC32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	0x02	0x60	0x8E	0xDB

In addition, for ML7456N RF part, CRC length for CRC calculation and CRC length for appending to packets (upon TX) or checking (upon RX) can be set individually. To do this, use CRC_LEN2_EN, CRC_LEN2, and CRC_LEN for setting.

CRC length for calculating CRC	CRC length for appending or checking CRC	CRC_LEN2_EN (B0 0x13)	CRC_LEN2 (B0 0x13)	CRC_LEN (B0 0x05)
CRC8	CRC8	0	-	0b00
CRC16	CRC8	1	0b01	0b00
	CRC16	0	-	0b01
CRC32	CRC8	1	0b10	0b00
	CRC16	1	0b10	0b01
	CRC32	0	-	0b10

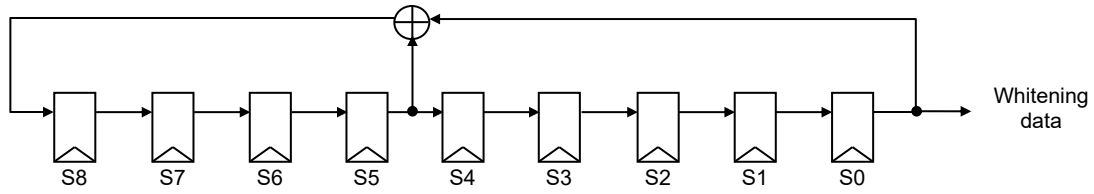
However, when different CRC lengths are set for calculating CRC and for appending to packets (upon TX) or checking (upon RX), "CRC length for calculating CRC" must be longer than or equal to "CRC length for appending to packets (upon TX) or checking (upon RX)."

○Data Whitening Function

ML7456N RF part supports the Data Whitening function. In packet format A/B, data succeeding C-field is the target area for Whitening. In packet format C, data succeeding Data-field is the target area for Whitening. Data generated by the following 9-bit pseudo random noise sequence (PN9) generation circuit will be XORed with TX data (encoded in 3-out-of-6 coding) before transmission and transmitted. Initialization value of the PN9 generation circuit shift register can be set by [WHT_INIT_H/L: B1 0x64/65] registers. PN9 polynomial can be set to any polynomial by [WHT_CFG: B1 0x66]. B1 0x66], any polynomial can be programmed.

- Data Whitening setting enable : WHT_SET ([DATA_SET2: B0 0x08(0)])
- Data Whitening initialization value : [WHT_INIT_H/L: B1 0x64/65]
- Whitening polynomial : [WHT_CFG: B1 0x66]

When [WHT_CFG: B1 0x66(0)] is set to 0b1, the polynomial setting function feeds back the shift register S1 output to XOR. In a similar way, when [WHT_CFG: B1 0x66(1)] is set to 0b1, it feeds back the shift register S2 output to XOR, and [WHT_CFG: B1 0x66(7-2)] also has a similar function. Two or more bits can be also set to 0b1. Therefore any type of PN9 polynomial can be programmed.



* ⊕ : Exclusive OR

Whitening data generation circuits
(Polynomial: $x^9 + x^5 + 1$)

The relation ship between General PN9 polynomial and [WHT_CFG] settings are as follows.

PN9 polynomial	[WHT_CFG: B1 0x66]
$x^9 + x^4 + 1$	0x08
$x^9 + x^5 + 1$	0x10

○SyncWord Detection function

This LSI supports automatic SyncWord recognition function. By having two sets of SyncWord pattern storage area, it is possible to detect two different packet format (Format A/B) which are defined by Wireless M-Bus. (For details, please refer to Wireless M-BUS standard) Receiving packet format is indicated by SW_DET_RSLT([STM_STATE:B0 0x77(5)]). In addition, when Two SyncWords waiting setting is set for Format C/D, it is possible to wait for two SyncWords. but detected result is not indicated.

1) TX

SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. SyncWord length for TX is defined by SYNC_WORD_LEN ([SYNC_WORD_LEN: B1 0x25(5-0)]). Data of each SyncWord pattern of the defined SyncWord length will be transmitted from higher bit.

SYNCWORD_SEL	TX SyncWord pattern
0	SYNCWORD1_SET[31:0] ([SYNCWORD1_SET3/2/1/0: B1 0x27/28/29/2A])
1	SYNCWORD2_SET[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E])

Example) SyncWord pattern and SyncWord length

If the following registers are programmed, 18 bits of SYNCWORD1_SET [17:0] will be transmitted from higher bit sequentially.
[SYNC_WORD_LEN: B1 0x25]=0x12
SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. B0 0x08(4)]) = 0b0

If the following registers are programmed, 24 bits of SYNCWORD2_SET [23:0] will be transmitted from higher bit sequentially.
[SYNC_WORD_LEN: B1 0x25]=0x18
SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. B0 0x08(4)]) = 0b1

2) RX

By setting SYNCWORD_SEL and 2SW_DET_EN ([DATA_SET2: B0 0x08(5)]), one pattern waiting or two patterns waiting can be selected as shown in the following table. Packet format automatic detection is valid only when 2SW_DET_EN = 0b1 and Format A/B is selected. Packet format automatic detection result for two patterns waiting is indicated in SW_DET_RSLT[STM_STATE: B0 0x77(5)]. B0 0x77(5)].

2SW_DET_EN	SYNCWORD_SEL	SyncWord pattern during sync detection	SyncWord detection operation	Automatic packet format detection	Data process after SyncWord
0	0	SYNCWORD_SET1[31:0]	Waiting for 1 pattern	No	Process according to each Format setting
0	1	SYNCWORD_SET2[31:0]	Waiting for 1 pattern	No	Process according to each Format setting
1	-	SYNCWORD_SET1[31:0] SYNCWORD_SET2[31:0]	Waiting for 2 patterns	Supported	[Format A or Format B setting] If matched with SYNCWORD1_SET, process as Format A. If matched with SYNCWORD2_SET, process as Format B. [Format C setting] Process as Format C

Length of SyncWord pattern referred to at detection can be defined by SYNC_WORD_LEN ([SYNC_WORD_LEN: B1 0x25(5-0)]). In this case, SyncWord pattern of the SyncWord length from the lowest bit of SYNCWORD1_SET or SYNCWORD2_SET will be the reference pattern.

Example) SyncWord length

If the following registers are set, 18 bits of SYNCWORD1_SET[17:0] or SYNCWORD2_SET[17:0] will be the reference pattern for the SyncWord detection. Higher bits (bit31-18) are not checked.
[SYNC_WORD_LEN: B1 0x25]=0x12
[SYNC_WORD_EN: B1 0x26]=0x0F

32bit SyncWord pattern can be controlled by enabling/disabling by each 8bit, when receiving SyncWord. The following table describes enable/disable control and SyncWord pattern. However, note that when the SyncWord length setting is outside the range of bits for enable/disable control, the expected SyncWord detection is unavailable.

[SYNC_WORD_EN] Register (B1 0x26)	SYNCWORD*_SET				SyncWord detection operation
	[31:24]	[23:16]	[15:8]	[7:0]	
0000					Prohibited
0001	D.C.(*1)			ON	Only [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0010	D.C.		ON	D.C.	Only [15:8] are valid. Upon [7:0] detection, SyncWord detection.
0011	D.C.		ON	ON	Only [15:0] are valid. Upon [7:0] detection, SyncWord detection.
0100	D.C.	ON	D.C.		Only [23:16] are valid. Upon [7:0] detection, SyncWord detection.
0101	D.C.	ON	D.C.	ON	Only [23:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0110	D.C.	ON	ON	D.C.	Only [23:8] are valid. Upon [7:0] detection, SyncWord detection.
0111	D.C.	ON	ON	ON	Only [23:0] are valid. Upon [7:0] detection, SyncWord detection.
1000	ON	D.C.			Only [31:24] are valid. Upon [7:0] detection, SyncWord detection.
1001	ON	D.C.		ON	Only [31:24] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1010	ON	D.C.	ON	D.C.	Only [31:24] and [15:8] are valid. Upon [7:0] detection, SyncWord detection.
1011	ON	D.C.	ON	ON	Only [31:24] and [15:0] are valid. Upon [7:0] detection, SyncWord detection.
1100	ON	ON	D.C.		[31:16] are valid. Upon [7:0] detection, SyncWord detection.
1101	ON	ON	D.C.	ON	Only [31:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1110	ON	ON	ON	D.C.	[31:8] are valid. Upon [7:0] detection, SyncWord detection.
1111	ON	ON	ON	ON	Whole [31:0] are valid. Upon [7:0] detection, SyncWord detection.

*1: D.C. stands for Don' t Care.
*2: Preamble pattern connecting with SyncWord can be added to the SyncWord detection conditions in addition to SyncWord pattern. To include preamble pattern, set RXPR_LEN([SYNC_CONDITION1: B0 0x45(5:0)]).

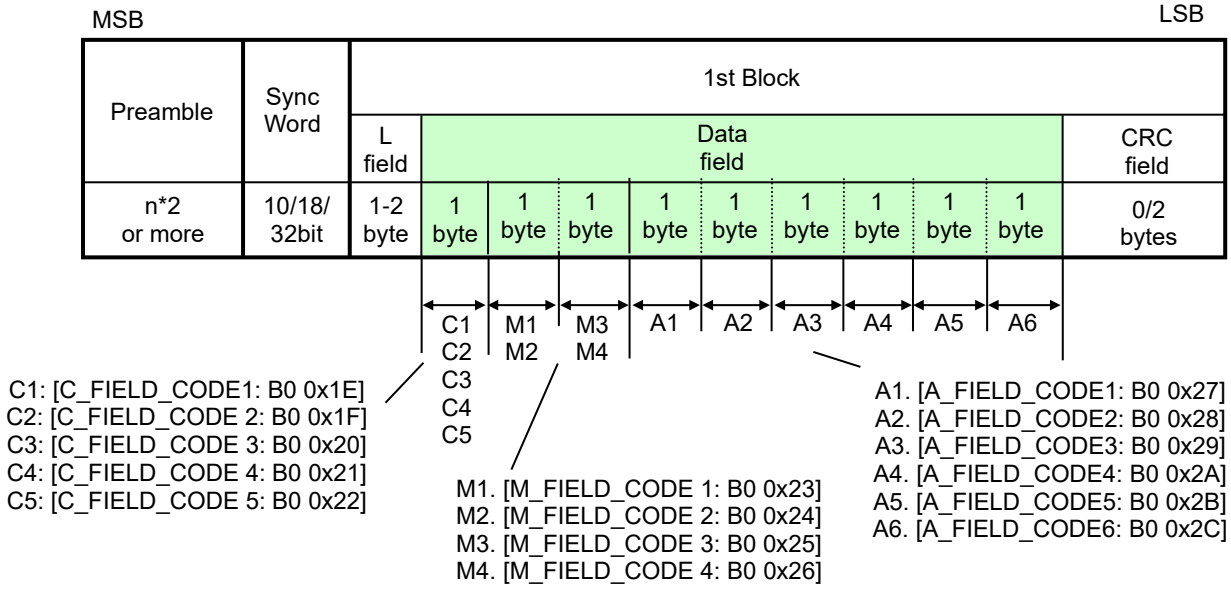
○Field Check Function

ML7456N RF part has a function for comparing the 9 bytes following C-field (Format A/B) or 9 bytes following Data-field (Format C) in a receiving packet and notifying through an interrupt when matching or not matching (field check function). Field check can be possible with the following register setting. The Field check function is enabled only in FIFO mode for discriminating L-field (RXDIO_CTRL[DIO_SET: B0 0x0C(7-6)] = 0b00) and data output mode 2 of DIO mode (RXDIO_CTRL[DIO_SET: B0 0x0C(7-6)]=0b11).

Function	Register
RX data process setting when Field check unmatched	[C_CHECK_CTRL: B0 0x1B(7)]
Field check interrupt setting	[C_CHECK_CTRL: B0 0x1B(6)]
C-field detection enable setting	[C_CHECK_CTRL: B0 0x1B(4-0)]
M-field detection enable setting	[M_CHECK_CTRL: B0 0x1C(3-0)]
A-field detection enable setting	[A_CHECK_CTRL: B0 0x1D(5-0)]
C-field code setting	[C_FIELD_CODE1: B0 0x1E] [C_FIELD_CODE2: B0 0x1F] [C_FIELD_CODE3: B0 0x20] [C_FIELD_CODE4: B0 0x21] [C_FIELD_CODE5: B0 0x22]
M-field code setting	[M_FIELD_CODE1: B0 0x23] [M_FIELD_CODE2: B0 0x24] [M_FIELD_CODE3: B0 0x25] [M_FIELD_CODE4: B0 0x26]
A-field code setting	[A_FIELD_CODE1: B0 0x27] [A_FIELD_CODE2: B0 0x28] [A_FIELD_CODE3: B0 0x29] [A_FIELD_CODE4: B0 0x2A] [A_FIELD_CODE5: B0 0x2B] [A_FIELD_CODE6: B0 0x2C]

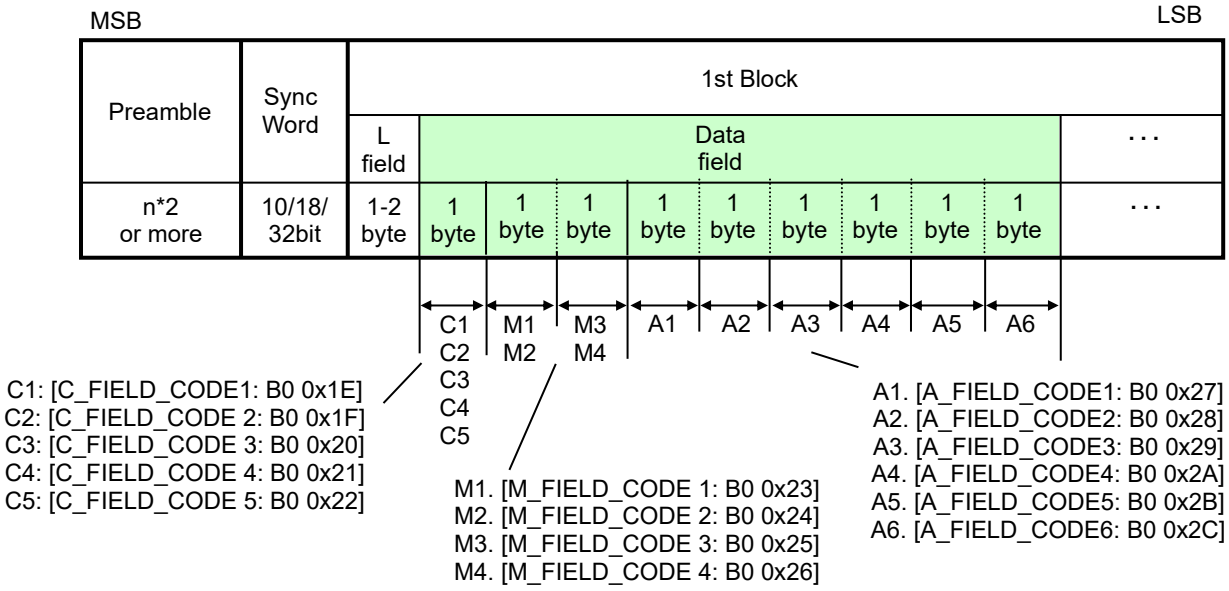
The following describes the relation between each comparison code and incoming RX data.

[Format A/B(Wireless M-Bus)]
Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all specified Field data (C-field/M-field/A-field) are matched, Field checking matching will be notified. However, if C-field data and C_FIELD_CODE5 are matched, even if other Field data (M-field/A-field) are not matched, Field check result will be notified as ”match”.



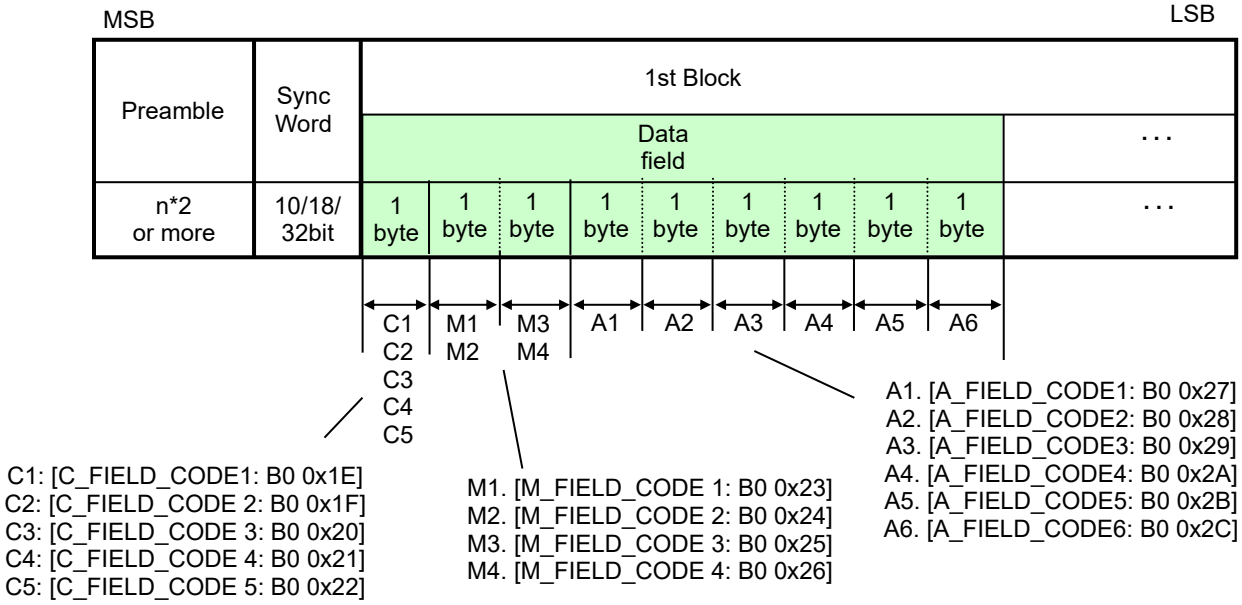
Check field	Comparison code	Conditions for match
C-field	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	Matches when one of the five comparison codes matches.
M-field 1st byte	M_FIELD_CODE1 or M_FIELD_CODE2	Matches when one of the two comparison codes matches.
M-field 2nd byte	M_FIELD_CODE3 or M_FIELD_CODE4	Matches when one of the two comparison codes matches.
A-field	A_FIELD_CODE1/2/3/4/5/6	Matches when the comparison code matches.

[Format C]
Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all the Data-field data satisfy the matching conditions shown in the following table, the Field check result will be notified as matching. However, if the 1st byte of Data-field matches with C_FIELD_CODE5, the Field check result will be notified as matching even when other Field data (from 2nd byte to 9th byte of Data-field) do not match.



Check field	Comparison code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	Matches when one of the five comparison codes matches.
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	Matches when one of the two comparison codes matches.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	Matches when one of the two comparison codes matches.
Data-field 4th byte	A_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A_FIELD_CODE3	Matches when the comparison code matches.
Data-field 7th byte	A_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A_FIELD_CODE6	Matches when the comparison code matches.

[Format D]
Field check can be controlled by setting disabled/enabled for each comparison code (1byte). If all the Data-field data satisfy the matching conditions shown in the following table, the Field check result will be notified as matching. However, if the 1st byte of Data-field matches with C_FIELD_CODE5, the Field check result will be notified as matching even when other Field data (from 2nd byte to 9th byte of Data-field) do not match.



Check field	Comparison code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	Matches when one of the five comparison codes matches.
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	Matches when one of the two comparison codes matches.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	Matches when one of the two comparison codes matches.
Data-field 4th byte	A_FIELD_CODE1	Matches when the comparison code matches.
Data-field 5th byte	A_FIELD_CODE2	Matches when the comparison code matches.
Data-field 6th byte	A_FIELD_CODE3	Matches when the comparison code matches.
Data-field 7th byte	A_FIELD_CODE4	Matches when the comparison code matches.
Data-field 8th byte	A_FIELD_CODE5	Matches when the comparison code matches.
Data-field 9th byte	A_FIELD_CODE6	Matches when the comparison code matches.

●Packet processing as a result of Field checking
By setting CA_RXD_CLR ([C_CHECK_CTRL: B0 0x1B(7)]) = 0b1, if the result of Field check is unmatched, the data packet will be aborted and the state will become the next packet reception waiting state.

●Storing number of unmatched packets
Unmatched packets can be counted up to 2047 packets and results are indicated in [ADDR_CHK_CTR_H: B1 0x62] and [ADDR_CHK_CTR_L: B1 0x63]. This count value can be cleared by STATE_CLR4([STATE_CLR: B0 0x16(4)]).

○FIFO Control Function

ML7456N RF part has on-chip TX_FIFO(64Byte) and RX_FIFO(64Byte). As TX/RX_FIFO do not support multiple packets, packet should be processed one by one. If RX FIFO keeps RX packet and next RX packet is received, RX FIFO will be overwritten. It applies to TX FIFO as well.
When receiving, RX data is stored in FIFO (byte by byte) and the host MCU will read RX data through SPI. When transmitting, host MCU write TX data to TX_FIFO through SPI and transmitting through RF.

Writing or reading to/from FIFO is through SPI with burst access. The data is written to [WR_TX_FIFO: B0 0x7C] register on TX, read from [RD_FIFO: B0 0x7F] register on RX. Continuous access to the FIFO increments internal FIFO counter automatically and data is saved or output. If FIFO access is suspended during write or read operation, address will be kept until the packet process is completed. Therefore, when resuming FIFO access, next data will be resumed from the suspended address.

FIFO control register are as follows:

Function	Register
TX FIFO Full level setting	[TXFIFO_THRH: B0 0x17]
TX FIFO Empty level setting	[TXFIFO_THRL: B0 0x18]
RX FIFO Full level setting	[RXFIFO_THRH: B0 0x19]
RX FIFO Empty level setting	[RXFIFO_THRL: B0 0x1A]
FIFO readout setting	[FIFO_SET: B0 0x78]
RX FIFO data usage status indication	[RX_FIFO_LAST: B0 0x79]
TX packet Length setting	[TX_PKT_LEN_H/L: B0 0x7A/7B]
RX packet Length setting	[RX_PKT_LEN_H/L: B0 0x7D/7E]
TX FIFO	[WR_TX_FIFO: B0 0x7C]
FIFO read	[RD_FIFO: B0 0x7F]

TX – RX procedure using FIFO are as follows:
[TX]

(a) TX L-filed value is set to [TX_PKT_LEN_H: B0 0x7A], [TX_PKT_LEN_L: B0 0x7B]. If Length is 1 byte, [TX_PKT_LEN_L] register will be transmitted.
Length setting can be set by LENGTH_MODE([PKT_CTRL: B0 0x05(1-0)]).

(b) TX data is written to FIFO.

[Note]

1. If TX data write sequence is aborted during transmission, [STATE_CLR: B0 0x16] (TX FIFO clear) must be issued. Otherwise data pointer which manages data in the LSI keeps the status, preventing the proper FIFO process of the next packet.
   For example, when an interrupt notification of TX FIFO access error ([INT_SOURCE_GRP3: B0 0x0F(4)]) is received, the TX data write sequence may be aborted. This interrupt can be generated when FIFO overrun (for example, data is written to TX FIFO when there is no available space in it) or underrun (for example, a transmission is attempted when FIFO is empty) occurs.
2. If the next writing sequence is performed when one packet data is stored, FIFO is overwritten.
3. Depending on the packet format, TX data Length value is different.
   Format A: Data length excluding the Length and CRC areas is set as the Length value.
   Format B: Data length excluding the Length area is set as the Length value.
   Format C: Data length excluding the Length area is set as the Length value.
   Format D: Data length from Data-field to CRC-field is set as the Length value.

[RX]
(1) Format A/B/C
(a) Read the L-field value (Length) from [RX_PKT_LEN_H: B0 0x7D], [RX_PKT_LEN_L: B0 0x7E].
(b) Read RX data from FIFO.
When reading from RX FIFO, set FIFO_R_SEL([FIFO_SET: B0 0x78(0)]) = 0b0. B0 0x78(0)]) to 0b0. If FIFO_R_SEL=0b1 , TX_FIFO will be selected.
Data usage value of RX FIFO is indicated by [RX_FIFO_LAST: B0 0x79] register.

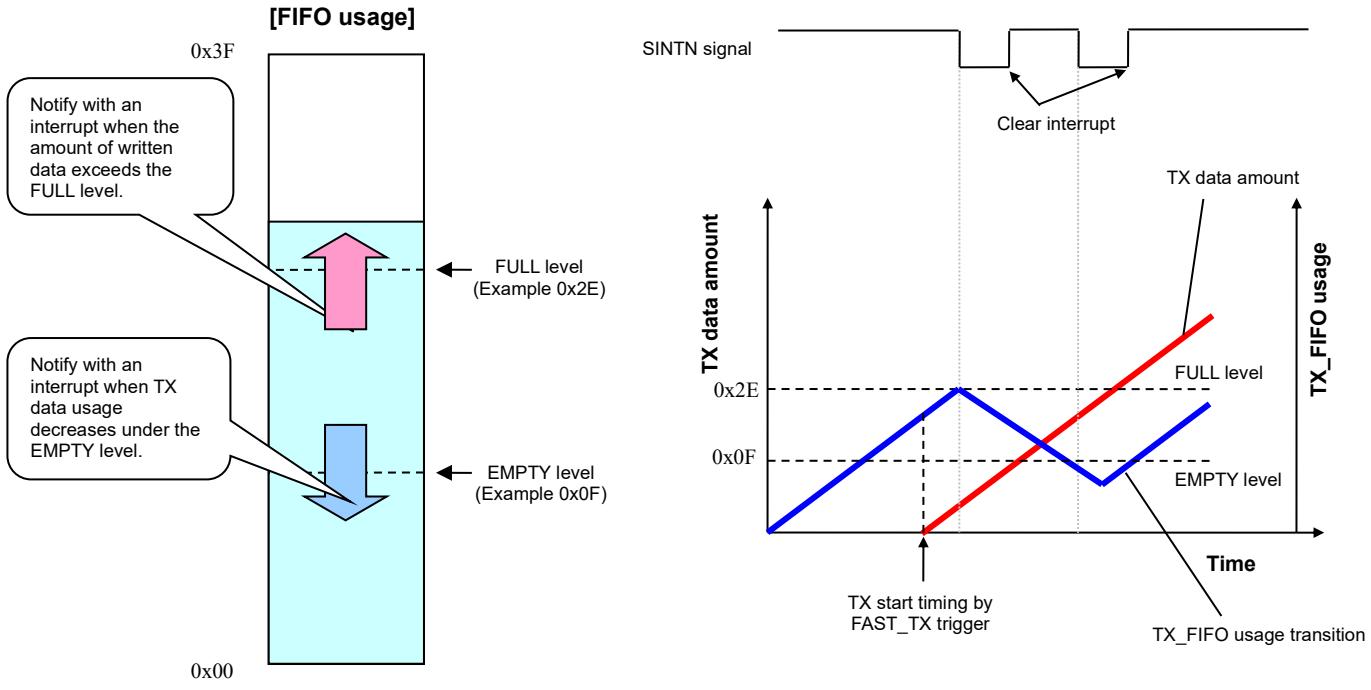
(2) Format D
(a) Set the data length (Length value) to [RX_PKT_LEN_H: B0 0x7D], [RX_PKT_LEN_L: B0 0x7E].
(b) Read RX data from FIFO.
When reading from RX FIFO, set FIFO_R_SEL([FIFO_SET: B0 0x78(0)]) = 0b0. B0 0x78(0)]) to 0b0. If FIFO_R_SEL=0b1 , TX_FIFO will be selected.
Data usage value of RX FIFO is indicated by [RX_FIFO_LAST: B0 0x79] register.

[Note]
1. If reading RX data is terminated before reading all data, RX FIFO clear ([STATE_CLR: B0 0x16]) must be issued. Otherwise data pointer which manages data in the LSI keeps the status, preventing the proper FIFO process of the next packet.
2. If 1 packet data is kept in the RX_FIFO, next RX data will be overwritten. Read all the necessary RX data before receiving the next packet. Incidentally, to detect the next packet being received even though all the data has not been read, the SyncWord detection interrupt (INT[13](INT_SOURCE_GRP2: B0 0x0E(5))) can be used.
3. Control FIFO so that FIFO overrun and underrun do not occur.
There are following methods for controlling FIFO so that FIFO overrun and underrun do not occur.
(a) Read RX FIFO usage ([RX_FIFO_LAST: B0 0x79]) and read that amount of data from FIFO.
(b) Set the Full level of RX FIFO ([RXFIFO_THRH: B0 0x19]), and after a FIFO-Full interrupt (INT[5](INT_SOURCE_GRP1: B0 0x0D(5))) is generated, read data from FIFO up to the amount equivalent to the Full level of RX FIFO.

IF TX/RX packet is larger than FIFO size, FIFO access can be controlled easily by FIFO-Full trigger or FIFO-Empty trigger.

(1) TX FIFO usage notification function

This function is to notice TX_FIFO usage to the MCU using interrupt (SINTN). If the TX FIFO usage (un-transmitted data) exceeds the threshold (FULL level) set by [TXFIFO_THRH: B0 0x17], an interrupt will occur to notify about it. Also, if ML7456N RF part transmits data and the TX FIFO usage decreases under the threshold (EMPTY level) set by [TXFIFO_THRL: B0 0x18], an interrupt will occur to notify about it. Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin. For output settings, refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52].

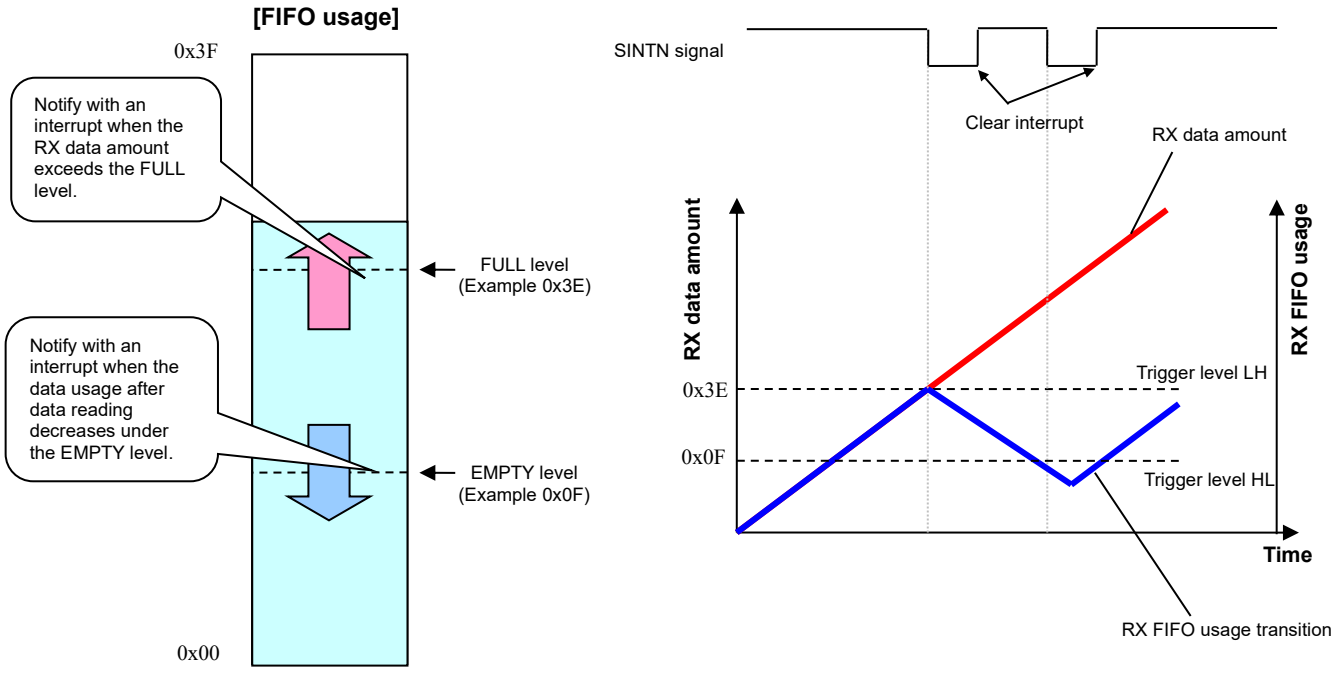


[Note]

1. Do not set the notification levels of [TXFIFO_THRH] and [TXFIFO_THRL] to the same value.
   Set them as satisfying the condition [TXFIFO_THRH] > [TXFIFO_THRL].
2. The Full detection state in LSI is cleared at Full trigger ([TXFIFO_THRH])>FIFO usage, allowing the next Full trigger to be detected. Note that the above clear condition may be met during FIFO write, and the Full trigger may be detected, depending on the timing of reading TX data (PHY) and FIFO write through SPI. To avoid such a case, disable the trigger level setting after the Full trigger is detected, and enable it again after the FIFO write is completed.
3. The Empty detection state of the inside of the LSI is cleared when the FIFO usage becomes larger than or equal to the Empty trigger ([TXFIFO_THRL]). After that, the next Empty trigger can be detected. Note that the above clear condition may be met during FIFO write, and the Empty trigger may be detected, depending on the timing of reading TX data (PHY) and FIFO write through SPI. To avoid such a case, make the trigger level setting disabled after the Empty trigger is detected, and make it enabled again after the FIFO write is completed.

(2) RX FIFO usage notification function

This function is to notify TX FIFO unread data amount (FIFO usage amount) by using interrupt (SINTN) to the MCU. When the RX FIFO usage (un-read) exceeds the threshold set by [RXFIFO_THRH: B0 0x19] (FULL level), an interrupt will occur to notify about it. Also, after MCU reads RX data and un-read data amount of RX FIFO (FIFO usage) decreases under the threshold set by [RXFIFO_THRL: B0 0x1A] (EMPTY level), an interrupt will occur to notify about it. Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin. For output settings, refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52].



[Note]

1. Do not set the notification levels of [RXFIFO_THRH] and [RXFIFO_THRL] to the same value.
   Set them as satisfying the condition [RXFIFO_THRH] > [RXFIFO_THRL].
2. The internal Full detection state is cleared at Full trigger ([RXFIFO_THRH])>FIFO usage, allowing the next Full trigger to be detected. Note that the above clear condition may be met during FIFO read, and the Full trigger may be detected, depending on the timing of writing RX data (PHY) and FIFO read through SPI. To avoid such a case, make the trigger level setting disabled after the Full trigger is detected, and make it enabled again after the FIFO read is completed.
3. The internal Empty detection state is cleared when the FIFO usage becomes larger than or equal to the Empty trigger ([RXFIFO_THRL]). After that, the next Empty trigger can be detected. Note that the above clear condition may be met during FIFO read, and the Empty trigger may be detected, depending on the timing of writing RX data (PHY) and FIFO read through SPI. To avoid such a case, make the trigger level setting disabled after the Empty trigger is detected, and make it enabled again after the FIFO read is completed.
4. This function is valid during data receiving. FIFO-Empty interrupt does not occur after RX completion.

○DIO Function

Using GPIO0-3, EXT_CLK or SDI/SDO pins, TX/RX data can be input/output. Output pins are controlled by [GPIO*_CTRL: B0 0x4E/0x4F/0x50/0x51], [EXTCLK_CTRL: B0 0x52], and [SPI/EXT_PA_CTRL: B0 0x53]. Data format for TX/RX are as follows:

TX --- TX data (NRZ or Manchester/3-out-of-6coding) will be input.
RX --- pre-decoded RX data or decoded RX data will be output. (Selectable by [DIO_SET: B0 0x0C])

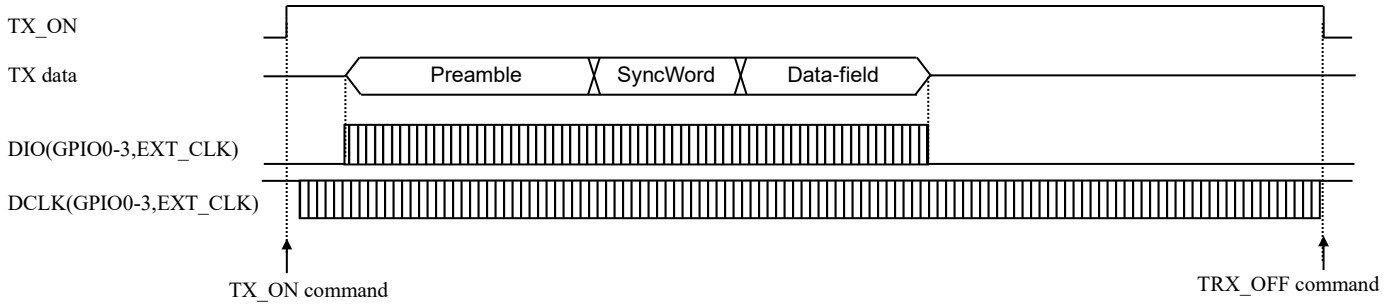
DIO function registers are as follows:

Function	Register
DIO RX data output start setting	[DIO_SET: B0 0x0C(0)]
DIO RX completion setting	[DIO_SET: B0 0x0C(2)]
TX DIO mode setting	[DIO_SET: B0 0x0C(5-4)]
RX DIO mode setting	[DIO_SET: B0 0x0C(7-6)]

(1) In case of using GPIO*, EXT_CLK pins

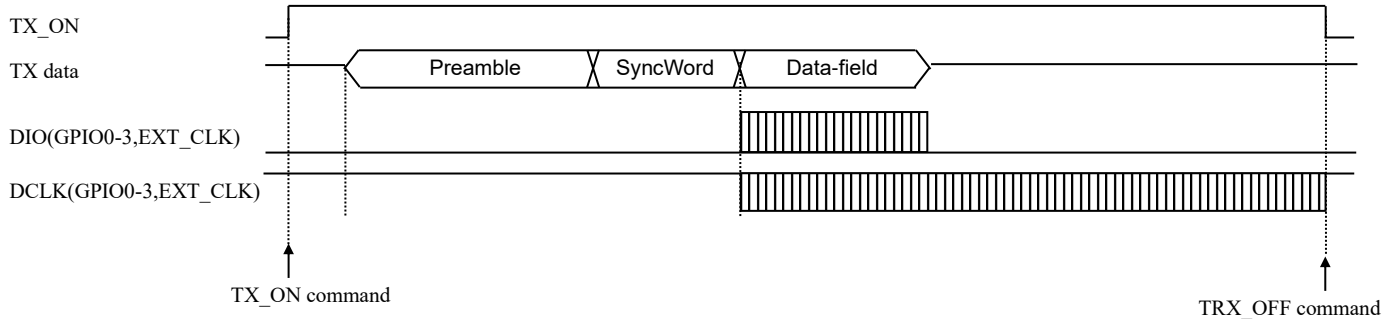
If GPIO0-3 pins are used for input/output of TX/RX data, DCLK/DIO should be controlled as follow. (below DIO/DCLK vertical line part indicate output or input period)

[TX]
(a) Continuous input mode
Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b01.
After TX_ON, the TX clock is output. At falling edge of the TX clock, TX data is input from the DIO pin. TX data must be encoded data.



* For details of timing, please refer to the “TX” in the “Timing Chart”.

(b) Data input mode
Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b10.
After TX_ON, the TX clock is output from data input timing after SyncWord. At falling edge of the TX clock, TX data is input from the DIO pin. TX data must be encoded data. Preamble and SyncWords generated automatically according to the registers setting.



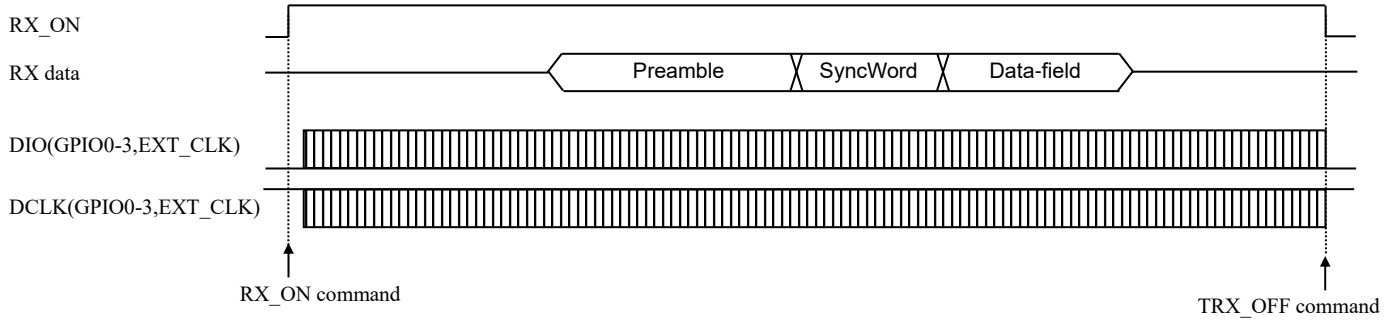
Preamble can be set by PB_PAT([DATA_SET1: B0 0x07(7)], TXPR_LEN([TXPR_LEN_H/L: B0 0x42/43]). Also, SyncWord can be set by SYNCWORD_SEL([DATA_SET2: B0 0x08(4)]), SYNCWORD_LEN([SYNC_WORD_LEN: B1 0x25]), SYNC_WORD_EN*([SYNC_WORD_EN: B1 0x26), SYNCWORD1_SET([SYNCWORD1_SET3/2/1/0: B1 0x27/28/29/2A]) and SYNCWORD2_SET([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E]).

[RX]

(a) Continuous output mode

When RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) = 0b01

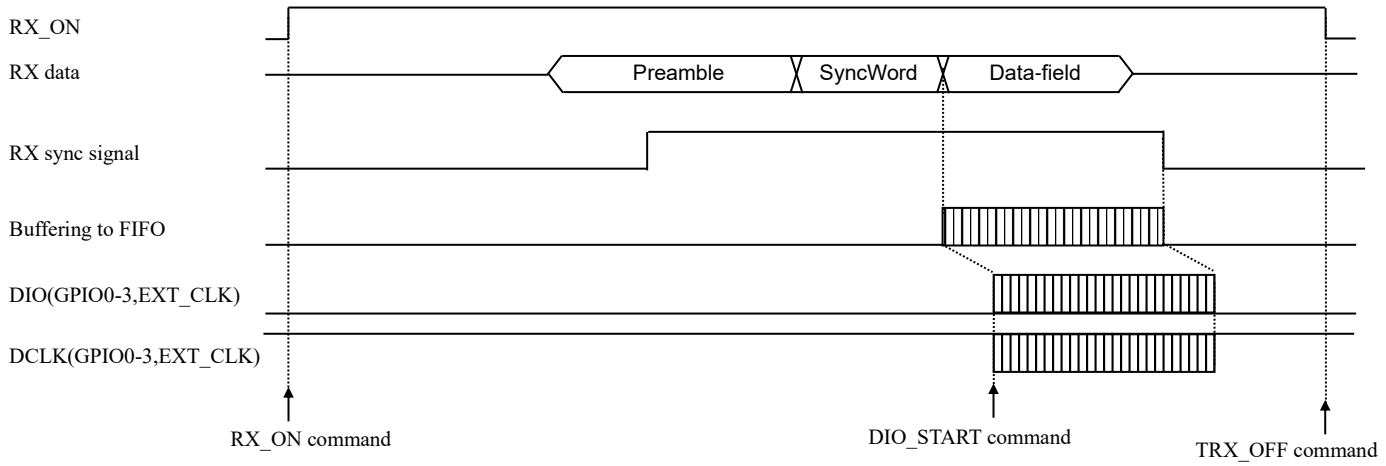
After RX_ON, the RX clock is output continuously. RX data (demodulated data) is output from the DIO output pin at falling edge of the RX clock. RX data is not buffered in FIFO.



(b) Data output mode 1

Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b10.

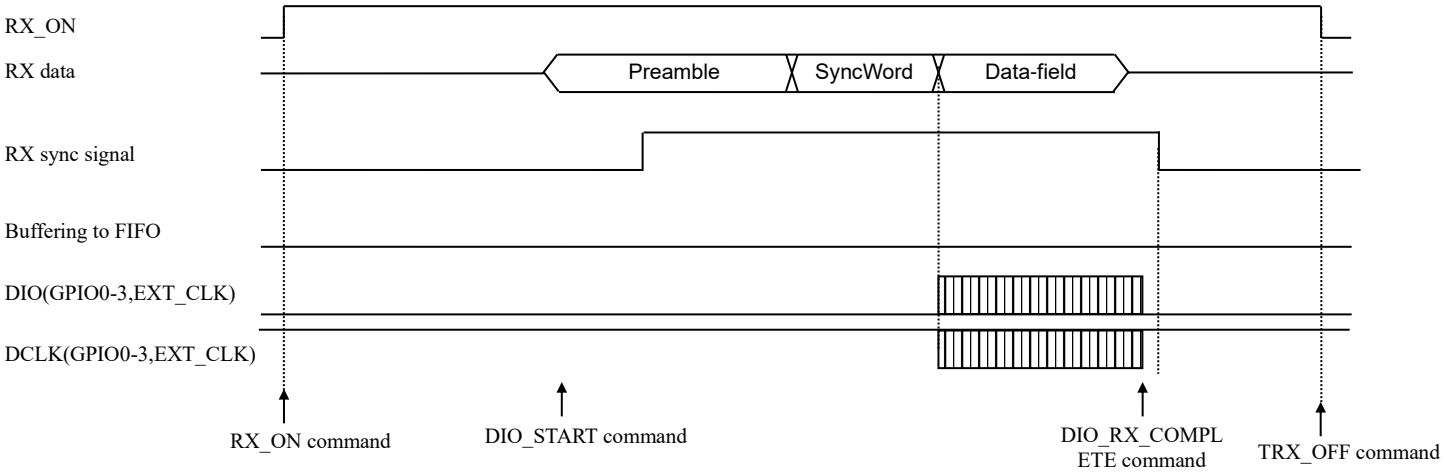
After SyncWord detection, RX data is buffered in RX FIFO. RX data buffering will continue until RX sync signal (SYNC) becomes “L”. By RX data output setting DIO_START([DIO_SET: B0 0x0C(0)]), the buffered RX data will be output from the first byte through the DIO interface (DIO/DCLK) (RX data is output at falling edge of the RX clock). However, when RX data output setting is done after 64-byte time, data will be overwritten from the first byte. If all buffered data is output until SYNC becomes “L”, RX completion interrupt (INT[8] group 2) will be generated. After RX completion, ready to receive next packet.



[Note]

1. RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after 1 byte access time upon SyncWord detection.
2. This mode does not process L-field. Field checking function is not supported.

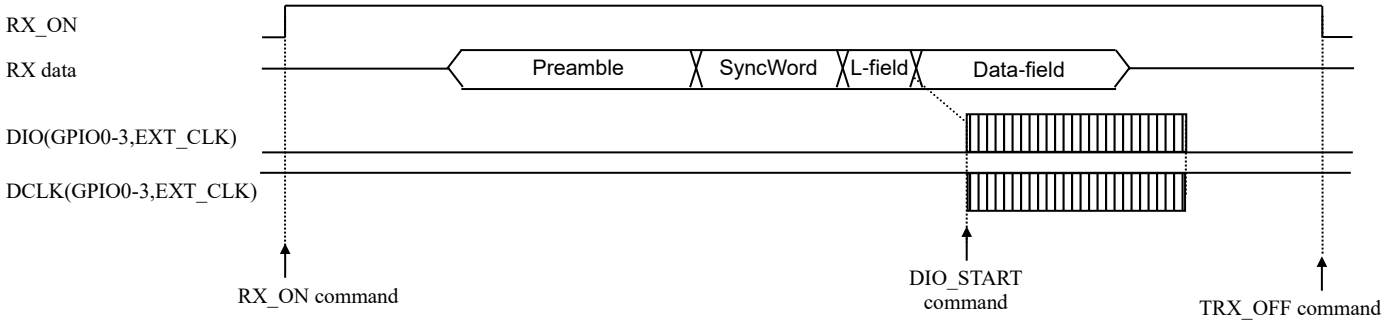
With this setting, when DIO_START is issued before SyncWord detection, data is not buffered in FIFO and RX data/clock is output after SyncWord detection. In order to complete RX before SYNC becomes L, set DIO RX completion setting (DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)])). After DIO_RX_COMPLETE setting, ready to receive the next packet.



(c) Data output mode 2

Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b11.

Only Data-field of RX data is buffered in FIFO. RX data of the amount of Length indicated by L-field is buffered in FIFO. By the RX data output setting (DIO_START([DIO_SET: B0 0x0C(0)])), buffered RX data is output from the first byte through the DIO interface (DIO/DCLK). However, when RX data output setting is done after 64-byte time, data will be overwritten from the first byte. If all data indicated by L-field is output, RX completion interrupt (INT[8] group2) will be generated. After RX completion, ready to receive next packet. Received Length information is indicated in [RX_PKT_LEN_H/L: B0 0x7D/7E]. This mode supports field check function.



[Note]

1. RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after elapsed time from SyncWord detection to L-field length + over 1byte access time.

(2) In case of using SDI/SDO pin (sharing with SPI interface)

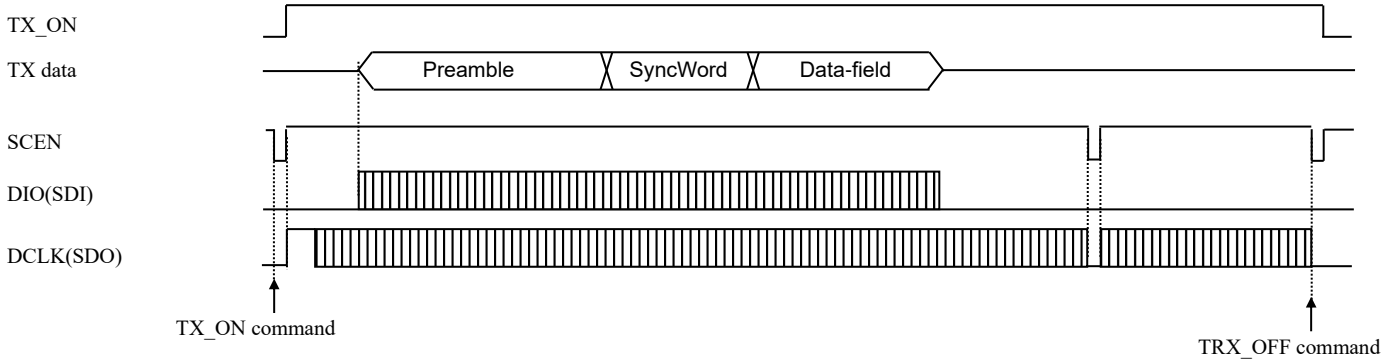
When the SPI interface (SDI/SDO) is used to input/output TX/RX data, DCLK/DIO are controlled as follows. (below DIO/DCLK vertical line part indicate output or input period) For the operation of LSI about each DIO mode, please refer to the previous chapter "(1) In case of using GPIO*, EXT_CLK pins".

[TX]

(a) Continuous input mode

Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b01.

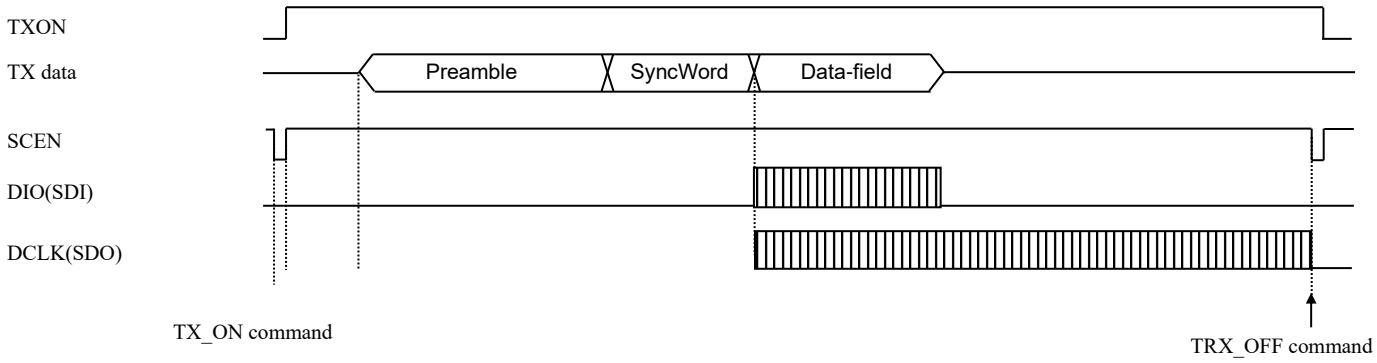
After a TX_ON command is issued ([RF_STATUS: B0 0x0B(3-0)] = 0x9), TX clock is output from the SDO pin while SCEN is H. Input TX data from the SDI pin. After TRX_OFF([RF_STATUS: B0 0x0B(3-0)] = 0x8) command is issued, input/output of TX data/clock will be disabled. In addition, even during DCLK output, if SCEN becomes L, the TX clock output will stop (SPI access has priority).



(b) Data input mode

Set TXDIO_CTRL([DIO_SET: B0 0x0C(5-4)]) to 0b10.

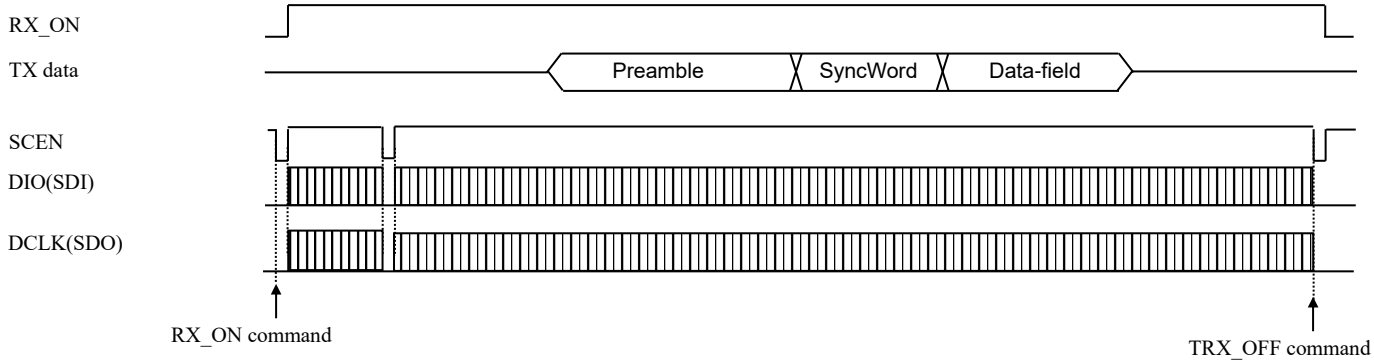
After a TX_ON command is issued ([RF_STATUS: B0 0x0B(3-0)] = 0x9), TX clock is output from the SDO pin while SCEN is H. Input TX data from the SDI pin. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), TX data/clock input/output are invalid. In addition, even during TX clock output, if SCEN becomes L, the TX clock output will stop (SPI access has priority).



[Note]

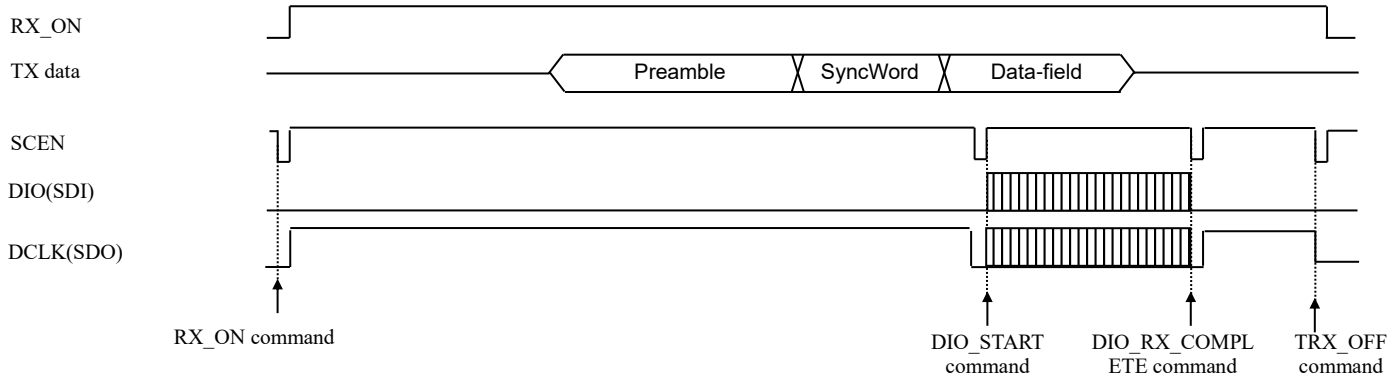
If SPI access is attempted during packet transmission, SPI access has a higher priority while the TX operation is continuing, thus TX data error can be expected. Do not attempt access SPI before TX completion.

[RX]
(a) Continuous output mode
When RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) = 0b01
After RX_ON command is issued (([RF_STATUS: B0 0x0B(3-0)] = 0x6), RX clock is output from the SDO pin and RX data is output from the SDI pin while SCEN is H. After TRX_OFF issuing, DCLK/DIO output will stop. In addition, even during RX data/clock output, if SCEN becomes L, the RX data/clock output will stop (SPI access has priority).



[Note]
During packet reception, if SPI access is attempted by the host, RX data error can be expected. At this time, reception data is not output causing missing bits, so do not conduct SPI access until reception is completed.

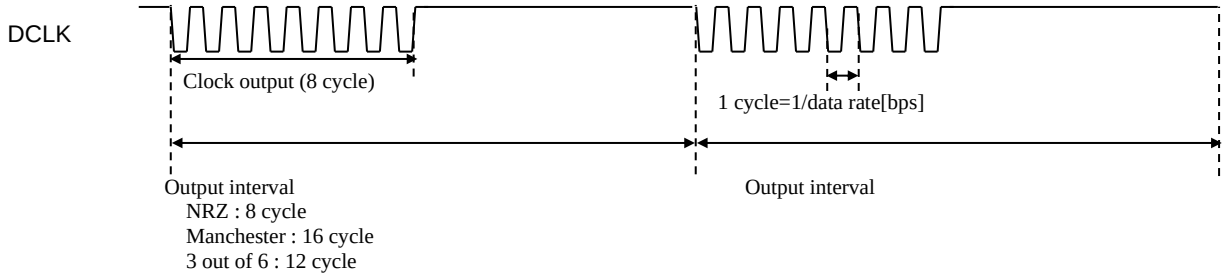
(b) Data output mode 1 or data output mode 2
Set RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) to 0b10/11.
After RX_ON command is issued ([RF_STATUS: B0 0x0B(3-0)] = 0x6), RX clock is output from the SDO pin and RX data is output from the SDI pin while SCEN is H. After TRX_OFF issuing, DCLK/DIO output will stop. In addition, even during RX data/clock output, if SCEN becomes L, the RX data/clock output will stop (SPI access has priority).



[Note]
During packet reception, if SPI access is attempted by the host, RX data error can be expected. At this time, reception data is not output causing missing bits, so do not conduct SPI access until reception is completed.

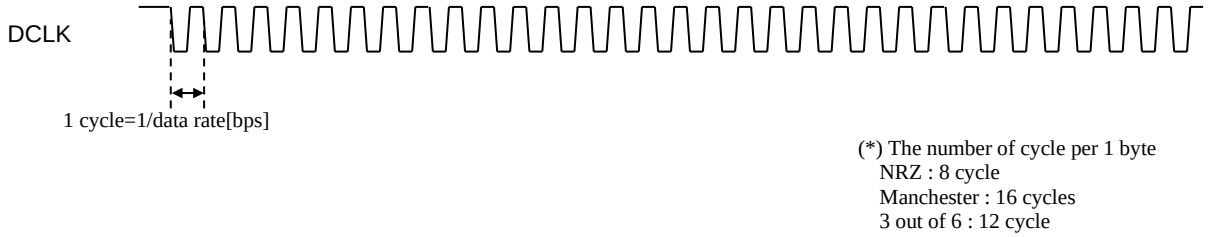
(3) DCLK output method
The DCLK output method depends on the DIO mode setting.

(a) Data output mode 2 (RXDIO_CTRL([DIO_SET: 0x0C(7-6)]) = 0b11)
In this mode, decoded data is output. The DCLK output section in an output interval varies depending on the encoding method. DCLK output section is as follows.

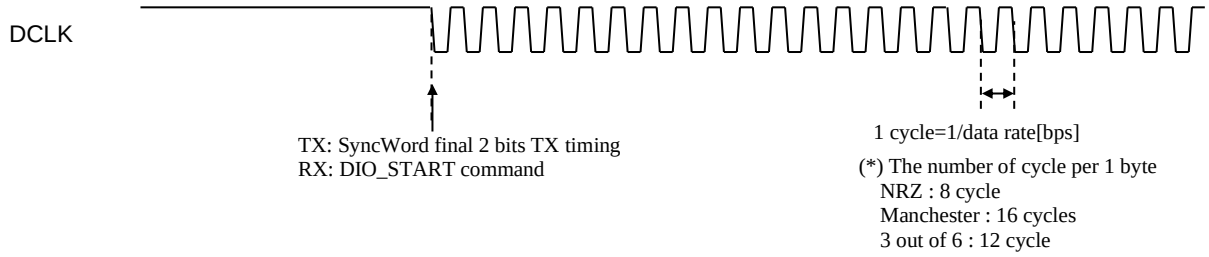


(b) Mode other than (a) (RX continuous output mode/data output mode 1, TX continuous input mode/data input mode)
In this mode, undecoded data is input or output. DCLK is output continuously. It does not depend on the encoding method.

TX continuous input mode or RX continuous mode



TX Data input mode / RX Data output mode 1



○FEC (Forward Error Correction) Function

This LSI is equipped with FEC and interleaver complying with IEEE802.15.4g.

FEC registers are as follows:

Function	Register
FEC setting	FEC_EN([FEC_CTRL: B6 0x02(0)])
FEC scheme setting	FEC_SCHEME([FEC_CTRL: B6 0x02(1)])
Interleave setting	INTLV_EN([FEC_CTRL: B6 0x02(2)])

[Note]

1. To use the FEC function, use it with the following settings.
   (a) Set TX data encoding mode setting (TX_DEC_SCHEME([DATA_SET1: B0 0x07(1-0)])) and RX data encoding mode setting (RX_DEC_SCHEME([DATA_SET1: B0 0x07(3-2)])) to NRZ.
   (b)Use Format C (PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)]) = 0b10) as the packet format.
   (c) Set the Length field length setting to 2-byte mode (LENGTH_MODE([PKT_CTRL2: B0 0x05(1-0)]) = 0b01).
2. When receiving data undergone Whitening, enable the Whitening setting (WHT_SET([DATA_SET2: B0 0x08(0)]) = 0b1) before receiving.

●Timer Function

○Wake-up Timer

ML7456N RF part has automatic wake-up function using wake-up timer. The following operations are possible by using wake-up timer.

- Upon timer completion, automatically wake-up from SLEEP state. Operation after wake-up can be selected from state changes to RX_ON state and TX_ON state by WAKEUP_MODE([SLEEP/WU_SET: B0 0x2D(6)]).
- By setting WUT_1SHOT_MODE[SLEEP/WU_SET] B0 0x2D(7)]), repetitive wake-up operations (interval operation) or a single operation (one-shot operation) can be selected.
- In interval operation, if RX_ON /TX_ON state is caused by wake-up timer, continuous operation timer is in operation..
- After moving to the RX_ON state by the wake-up timer, when the continuous operation timer is completed, move to the SLEEP state automatically. However, if SyncWord is detected before timer completion, RX_ON state will be maintained. In this case, ML7406 does not go back to the SLEEP state automatically. SLEEP setting (SLEEP_EN ([SLEEP/WU_SET: B0 0x2D(0)]) = 0b1) is necessary to go back to the SLEEP state. However if RXDONE_ MODE[1:0]([RF_STATUS_CTRL:B0 0x0A(3-2)]) =0b11, after RX completion, move to SLEEP state automatically. The timing to determine whether or not to continue RX after continuous operation timer completion is selectable from SyncWord detection, Field check detection, and synchronization detection by RCV_CONT_SEL([M_CHECK_CTRL: B0 0x1C(5:4)]).
- After moving to the TX_ON state by the wake-up timer, automatic return to the SLEEP state is not made even when the continuous operation timer is completed. To enter the SLEEP state after the completion of TX operation, configure the SLEEP setting (SLEEP_EN ([SLEEP/WU_SET: B0 0x2D(0)])=0b1).
- After wake-up by combining with high speed carrier checking mode, CCA is automatically performed, if IDLE is detected, able to move to SLEEP state immediately. For details, please refer to the "(3) high speed carrier detection mode".
- By setting WUT_CLK_SOURCE ([SLEEP/WU_SET:B0 0x2D(2)]), the clock source for wake-up timer can be selected from EXT_CLK pin or on-chip RC OSC circuit.

Wake-up interval, wake-up timer interval and continuous operation timer can be calculated in the following formula.

Wake-up interval [s] = Wake-up timer interval [s] + Continuous operation timer [s]

Wake-up timer interval [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) *
(Wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) + 1)

Continuous operation timer [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(7-4)]) *
(Continuous operation timer operating time setting ([WU_DURATION: B0 0x31]) – 1)

[Note]

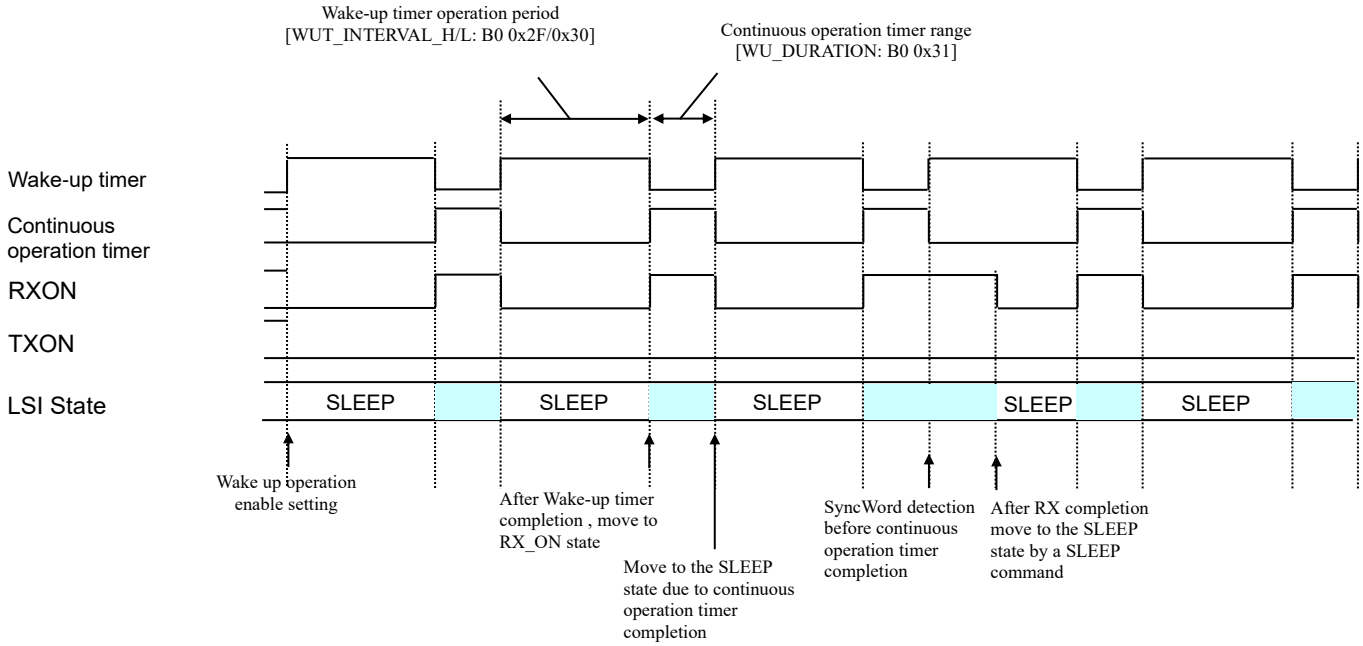
1. When set to move to TX_ON after wake-up, if the continuous operation timer is completed during TX, it is judged as TX in progress and TX continues. After TX is completed, RF state transition is performed according to TXDONE_MODE([RF_STATUS_CTRL: B0 0x0A(1-0)]) setting.
2. WUDT_CLK_SET ([WUT_CLK_SET: B0 0x2E(7-4)]) and WUT_CLK_SET ([WUT_CLK_SET: B0 0x2E(3-0)]) of dividing setting can be set independently. When using the continuous operation timer, set the same setting to WUDT_CLK_SET and WUT_CLK_SET.
3. The minimum setting for wake-up timer setting interval ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is 0x02. The minimum setting for continuous operation timer operating time setting ([WU_DURATION: B0 0x31]) is 0x01. Note that continuous operation timer operating time setting should be set so that the timer completion is occurred after a notification of a clock stabilization completion interrupt (INT[0]([INT_SOURCE_GRP1: B0 0x0D(0)])) caused by wake-up.
4. Since SyncWord detection is not conducted during reception of DIO mode set to RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) = 0b01, after continuous operation timer is completed, the state moves to the SLEEP state forcibly. Note that the SyncWord detection is not issued when in DIO mode with RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)])=0b01. Therefore, when continuous operation timer completed, forcibly move to SLEEP state.
5. ML7456N RF part automatically moves to the SLEEP state by timer operation, and if the SLEEP state transition and a SPI access occurs at the same time, the SPI access will become invalid. Please take some measure so that SLEEP state transition and SPI access do not happen at the same time.

(1) Interval operation

(a) RX

After wake-up, RX_ON state. If continuous operation timer completed before SyncWord detection, automatically return to SLEEP state. If SyncWord detected, continue RX_ON. After RX completion, continue operation defined by RXDONE_MODE[1:0] ([RF_STATUS_CTRL: B0 0x0A(3-2)]). In addition, the state can be moved to the SLEEP state by setting SLEEP_EN(SLLEP/WU_SET:B0 0x2D(0)] = 0b1.

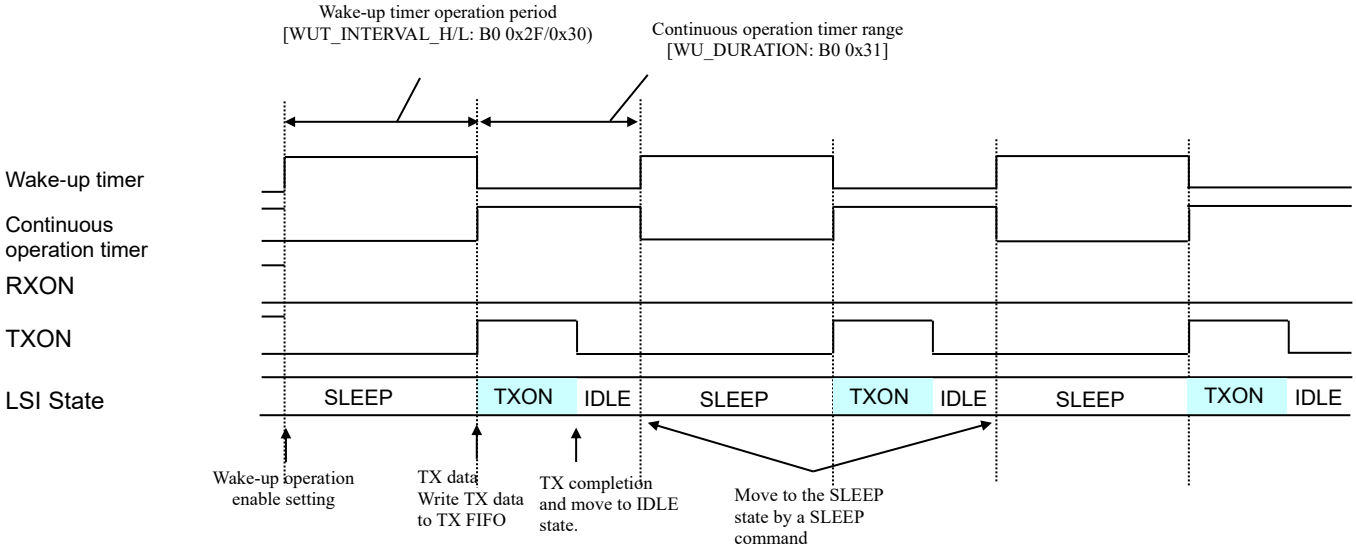
When [SLEEPWU_SET: B0 0x2D(6-4)] = 0b011 is set



(b) TX

After wake-up, TX_ON state. After TX completion, operate according to TXDONE_MODE[1:0] ([RF_STATUS_CTRL: B0 0x0A(1-0)]). Even when the continuous operation timer is completed, a return to the SLEEP state is not made. Therefore, set SLEEP_EN(SLLEP/WU_SET:B0 0x2D(0)] = 0b1 after completion of TX operation to enter the SLEEP state.

When [SLEEPWU_SET: B0 0x2D(6-4)] = 0b111 is set

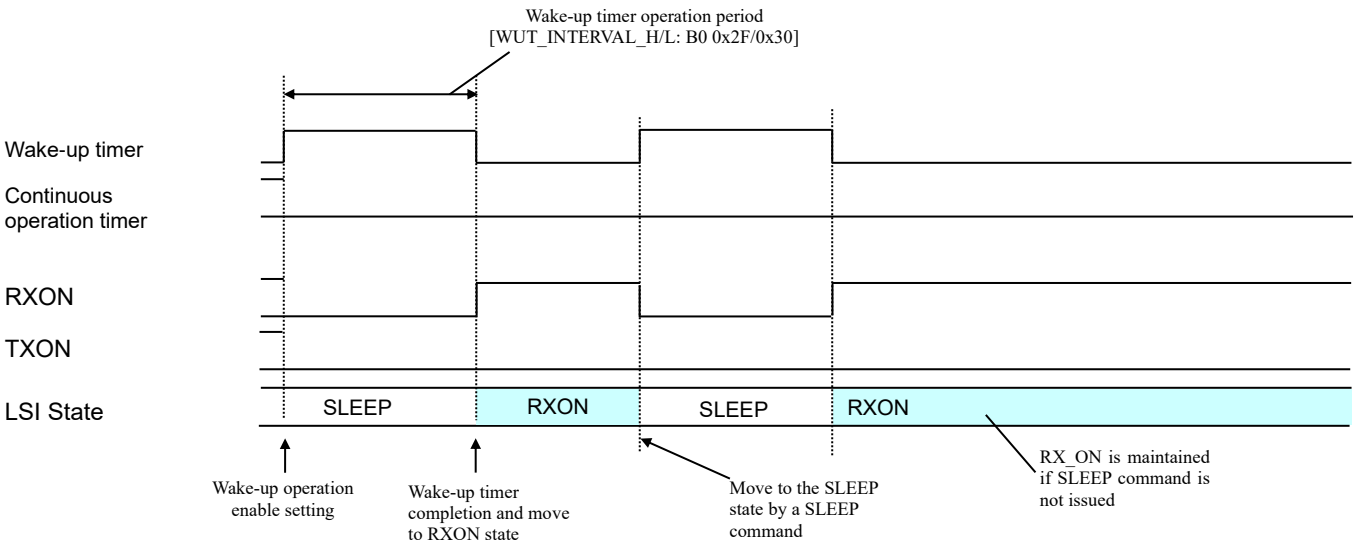


(2) One-shot operation

(a) RX

After wake-up timer completion, move to RX_ON state. And continue RX_ON state. Move to SLEEP state by SLEEP command. Since wake-up timer setting interval ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is maintained, after a SLEEP command is issued, the one-shot operation will restart. Clear the wake-up interrupt ([INT_SOURCE_GRP1: B0 0x0D(6)]) before moving to the SLEEP state. If RX completed during RX_ON, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) . Same manner in TX_ON state.

When [SLEEP/WU_SET: B0 0x2D(7-4)] = 0b1001 is set

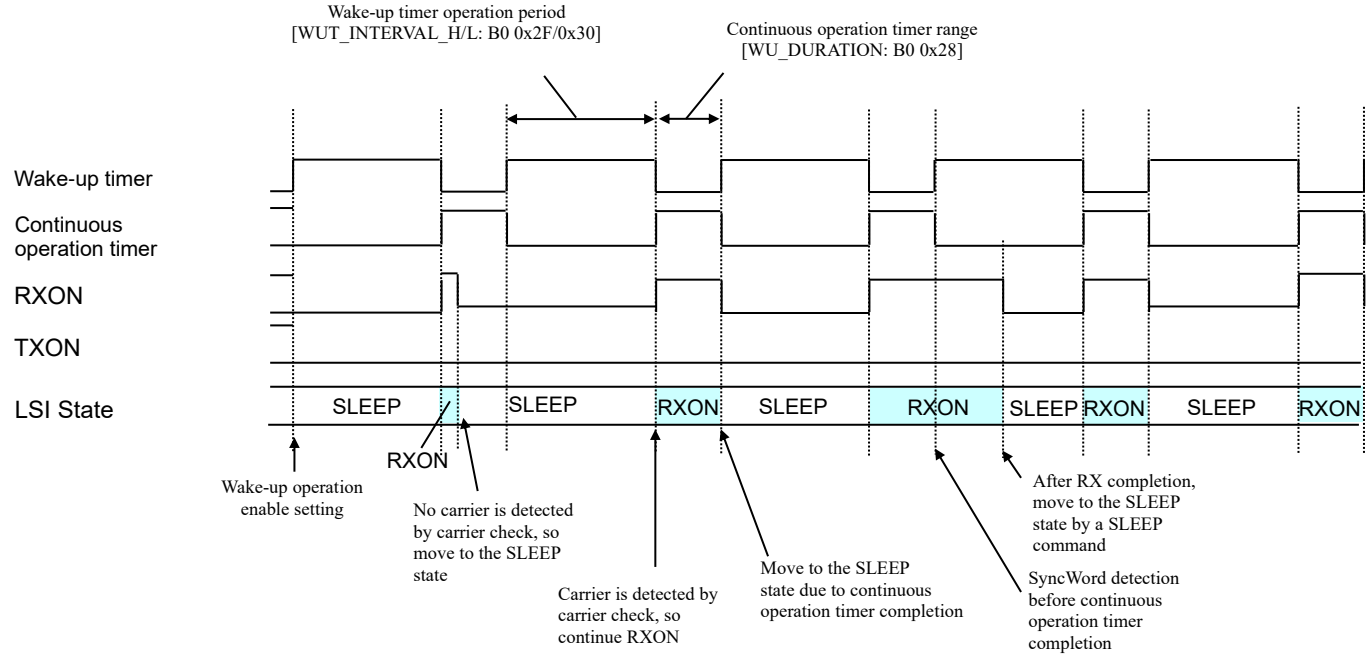


(3) Combination with high speed carrier detection

(a) Interval operation

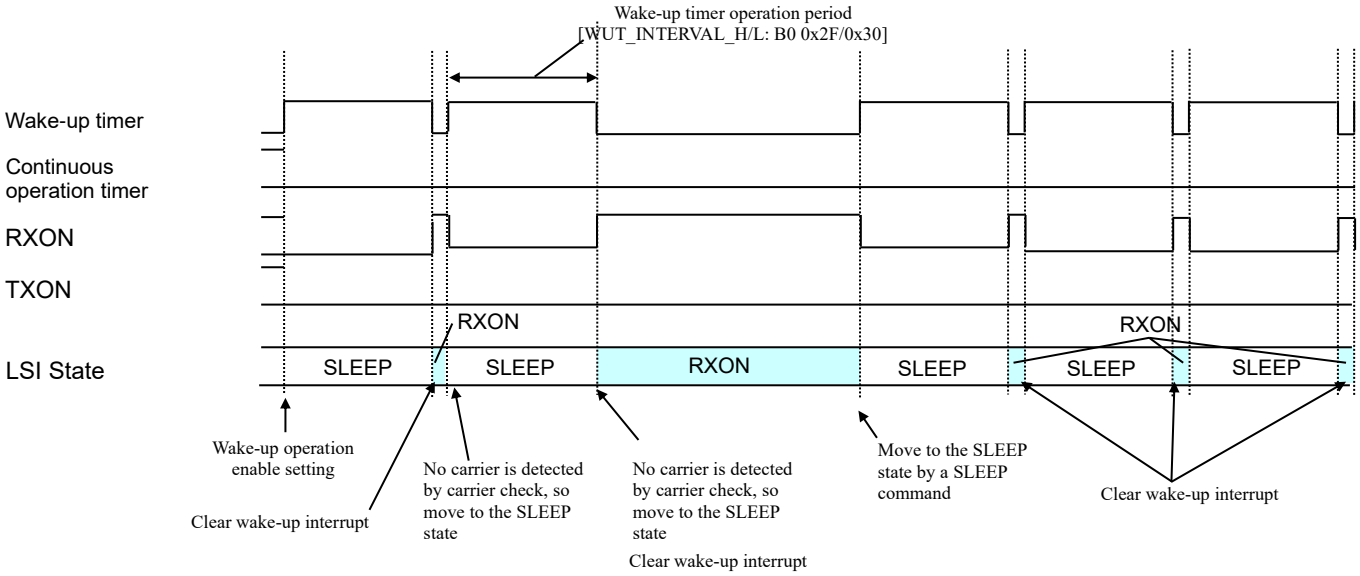
After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier is detected, automatically move to SLEEP state. If carrier detected, maintaining RX_ON state and perform SyncWord detection. If continuous operation timer completed before SyncWord detection, automatically move to SLEEP state. And If SyncWord detected, continue RX_ON state state.

[SLEEP/WU_SET: B0 0x2D(7-4)]=0b0011
When FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)]) = 0b1 is set



(b) One-shot operation
After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier is detected, automatically move to SLEEP state. In case of no carrier detection, if periodic waking up at wake-up timer interval is necessary, clear the wake-up interrupt ([INT_SOURCE_GRP1: B0 0x0D(6)]) before moving to the SLEEP state. If carrier is detected, continue RX state. Able to go back to SLEEP by setting SLEEP parameters.

When [SLEEPWU_SET: B0 0x2D(7-4)]=0b1001
When FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)]) = 0b1 is set



○General Purpose Timer

This LSI has general purpose timer. 2 channels of timer are able to function independently. Clock sources, timer setting can be programmed independently. This timer uses 1-shot operation. When timer is completed, General purpose timer 1 interrupt (INT[22] group3) or General purpose timer 2 interrupt (INT[23] group3) will be generated.

General timer interval can be programmed as the following formula.

General purpose timer interval [sec] = general purpose timer clock cycle *
Division setting ([GT_CLK_SET: B0 0x33]) *
After general purpose timer interval setting ([GT1_TIMER: B0 0x35]) B0 0x34] or [GT2_TIMER: B0 0x35])

By setting GT2/1_CLK_SOURCE [GT_SET: B0 0x32(5,1)], the clock source for general purpose timer is selectable from wake-up timer clock and 2 MHz.

●Frequency Setting Function

○Channel Frequency Setting

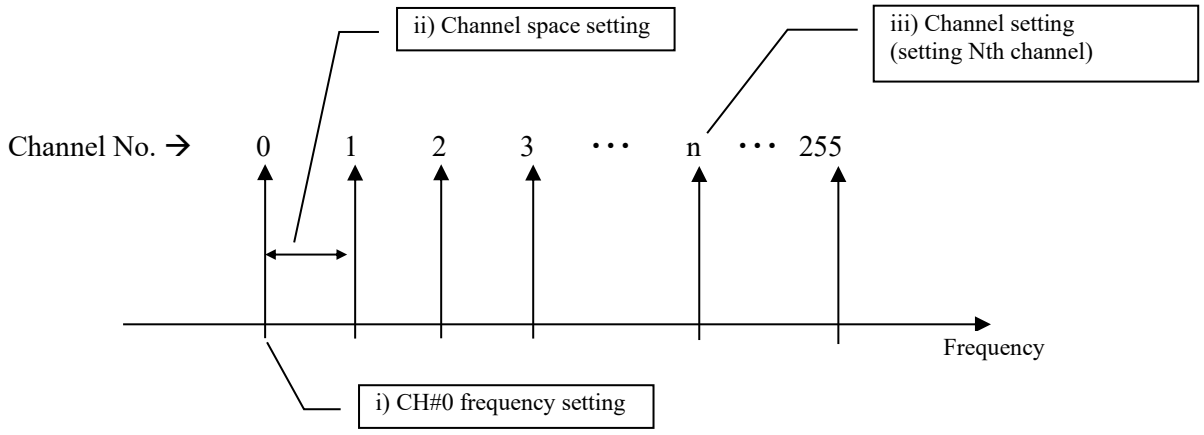
Maximum 256 channel frequencies can be set (CH#0 to CH#255). The setting of TX/RX frequencies can be performed by the following registers.

Frequency		Register
CH#0 frequency	TX	[TXFREQ_I: B1 0x1B]、[TXFREQ_FH: B1 0x1C]、[TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]
	RX	[RXFREQ_I: B1 0x1F]、[RXFREQ_FH: B1 0x20]、[RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22]
Channel spacing		[CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24]
Channel setting		[CH_SET: B0 0x09]
PLL dividing setting		[PLL_DIV_SET: B1 0x1A]

[Channel frequency setting]
Using above registers, channel frequency is defined as following formula.

Channel frequency = CH#0 frequency + Channel spacing * Channel setting

[Channel frequency allocation image]



Set the PLL dividing setting according to the RF frequency (for each frequency band) as shown below.

PLL dividing setting [PLL_DIV_SET: B1 0x1A]	
315 to 510 MHz band	900 MHz band
0x02 (divided by 2)	0x00 (divided by 1)

[Note]

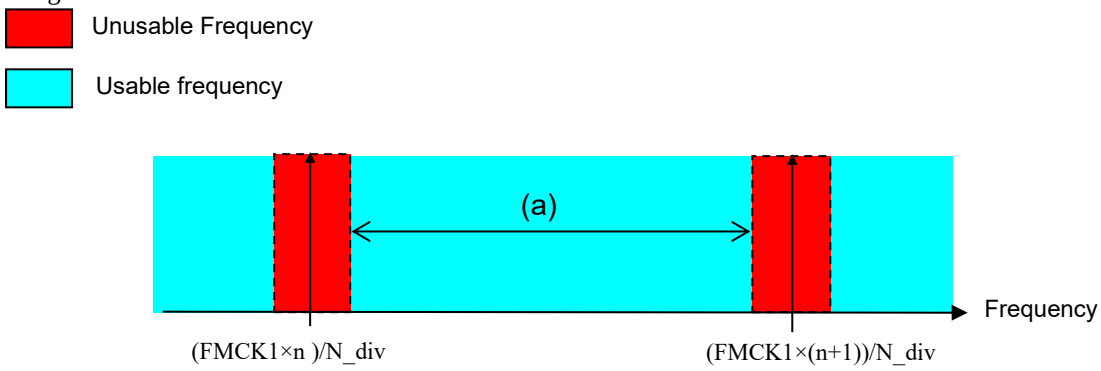
(1) The channel frequency to be selected must meet the following conditions. If the following conditions cannot be met, please change channel #0 frequency or use other channels. If this formula cannot be met, expected frequency is not functional or PLL may not be locked.

F_{MCK1}: Master clock frequency

N_{div} = 1,2

$$(F_{MCK1}*n + 1\ MHz) / N_{div} \leq \text{Used channel frequency} \leq (F_{MCK1} * (n + 1) - 1\ MHz) / N_{div} \qquad * n = \text{integer}$$

Concept diagram



(Example of calculating Range (a) shown above)

For 1 division mode (N_div = 1), master clock 36 MHz, n = 25

(36 MHz x 25 + 1) MHz ≤ Channel frequency to be used ≤ (36 MHz x (25 + 1) - 1)

=> 901 MHz ≤ Channel frequency to be used ≤ 935 MHz

(2) CH#0 frequency and channel interval settings may have error. Therefore, channel frequency has frequency error indicated by the following formula.

Channel frequency error [Hz] = CH#0 frequency error [Hz] + Channel interval setting error [Hz] * Channel setting

When changing “channel frequency” by setting “channel setting” without “CH#0 frequency” change, the “channel frequency error” will become larger than by setting both “CH#0 frequency” and “channel setting”. If the “channel frequency error” becomes larger, please change “CH#0 frequency”.

(3) If the 26-bit channel frequency (= CH#0 frequency + Channel spacing x Channel setting) setting value (integer and decimal parts, refer to “Channel #0 frequency setting”) exceeds the maximum value 0x3FF_FFFF, the expected channel frequency is not achieved. Take this maximum value into account when deciding the channel #0 frequency, channel interval, and channel setting.

(1) Channel #0 frequency setting

TX frequency can be set by [TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E], and RX frequency can be set by [RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22].

Refer to "Channel Frequency Setting" for N_{div}.

Channel #0 frequency setting value can be calculated using the following formula.

$$I = \frac{f_{rf}}{f_{ref} / N_{div}} \quad \text{(Integer part)}$$

$$F = \left\{ \frac{f_{rf}}{f_{ref} / N_{div}} - I \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Where

f_{rf} : Channel #0 frequency
f_{ref} : PLL reference frequency (= master clock frequency: F_{MCK1})
I : Integer part of frequency setting
F : Fractional part of frequency setting
N_{div} : Division setting (1 or 2)

I (hex) is set to [TXFREQ_I: B1 0x1B] and [RXFREQ_I: B1 0x1F]. Also, F (hex) is set to the following registers.
For TX, set [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E] in this order from MSB.
For RX, set [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22] in this order from MSB.

Frequency error f_{err} is calculated as follows :

$$f_{err} = \left\{ I + \frac{F}{2^{20}} \right\} \cdot (f_{ref} / N_{div}) - f_{rf}$$

[Example] When setting TX CH#0 frequency f_{rf} to 920 MHz (master clock 36 MHz, Ndiv = 1), following calculations are performed.

$$I = \frac{920MHz}{(36MHz/1)} \text{ (Integer part) } = 25(0x19)$$

$$F = \left\{ \frac{920MHz}{(36MHz/1)} - 25 \right\} \cdot 2^{20} \text{ (Integer part)} = 582542(0x8E38E)$$

[TXFREQ_I: B1 0x1B] = 0x19
[TXFREQ _FH: B1 0x1C] = 0x08
[TXFREQ _FM: B1 0x1D] = 0xE3
[TXFREQ _FL: B1 0x1E] = 0x8E

Frequency error f_{err} is calculated as follows:

$$f_{err} = \left\{ 25 + \frac{582542}{2^{20}} \right\} \cdot (36MHz/1) - 920MHz = 0Hz$$

(2) Channel space setting

Channel space can be set by [CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24]. Convert the channel space calculated by the following formula into hexadecimal value and set it to [CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24] in this order from MSB.
Channel space is from the center frequency of given channel to adjacent channel center frequency.

Refer to "Channel Frequency Setting" for N_{div}.

The setting values of [CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24] are obtained by the following formula.

$$CH\_SPACE = \left\{ \frac{f_{sp}}{f_{ref} / N_{div}} \right\} \cdot 2^{20} \text{ (Integer part)}$$

Where,

CH_SPACE : Channel space setting

f_{sp} : Channel space [MHz]

f_{ref} : PLL reference frequency (= master clock frequency: F_{MCK1})

N_{div} : Division setting (1 or 2)

[Example] When setting channel space to 400 kHz (master clock 36 MHz, Ndiv = 1), following calculation is performed.

$$CH\_SPACE = \left\{ \frac{0.4MHz}{36MHz/1} \right\} \cdot 2^{20} \text{ (Integer part)} = 11650(0x2D82)$$

[CH_SPACE_H: B1 0x23] = 0x2D
[CH_SPACE_L: B1 0x24] = 0x82

○IF Frequency Setting

IF frequency is set by [IF_FREQ: B0 0x61]. See the following table for the IF frequency for each IF frequency setting value. These can be set separately for the normal receiving mode and during CCA.

IF_FREQ([IF_FREQ: B0 0x61(2-0)] IF_FREQ_CCA([IF_FREQ: B0 0x61(6-4)]	IF frequency (*1)
0b000	225kHz
0b001	150kHz
0b010	Prohibited
0b011	112.5kHz
0b100	Prohibited
0b101	75kHz
0b110	180kHz
0b111	0kHz

(*1) These IF frequency values are for a master clock of 36MHz. When using another frequency as master clock, the IF frequency varies depending on the amount of frequency change from 36 MHz.

●Modulation Function

○ FSK Modulation

To use FSK modulation, set MOD_TYPE([MOD_CTRL: B6 0x01(1-0)]) = 0b00.

(1) GFSK modulation setting

To use GFSK mode, GFSK_EN([DATA_SET1: B0 0x07(4)])=0b1 should be set. In GFSK modulation, frequency deviation can be set by [GFSK_DEV_H: B1 0x30] and [GFSK_DEV_L: B1 0x31] registers, and the filter coefficient of Gaussian filter can be set by [FSK_DEV0_H/ GFIL0: B1 0x32] to [FSK_DEV3_H: B1 0x38] registers. 2FSK/4FSK can be selected by FSK_SEL[DATA_SET2: B0 0x08(5)].

Refer to "Channel Frequency Setting" for N_{div}.

(a) GFSK frequency deviation setting

F_DEV value can be calculated as the following formula:

$$F\_DEV = \left\{ \frac{f_{dev}}{f_{ref} / N_{div}} \right\} \cdot 2^{20} \text{ (Integer part)}$$

Where,

f_{dev} : Frequency deviation [Hz]

f_{ref} : PLL reference frequency (= master clock frequency: F_{MCK1})

N_{div} : Division setting (1 or 2)

In 4GFSK mode, the value of maximum frequency deviation should be specified.

[Example] When setting frequency deviation to 50 kHz, the setting value for the case of f_{REF} = 36 MHz and N_{div} = 1 is calculated as follows.

F_DEV = {0.05 MHz ÷ (36 MHz/1)} x 2^{20} (integer value) = 1456 (0x05B0)

Here, [GFSK_FDEV_H/L: B1 0x30/31] should be set as below:

[GFSK_DEV_H: B1 0x30] = 0x05

[GFSK_DEV_L: B1 0x31] = 0xB0

(b) Gaussian filter setting

GFSK mode can be set by GFSK_EN([DATA_SET1: B0 0x07(4)])=0b1.

The BT value of the Gaussian filter can be set by the following registers.

Here is the relationship between the BT value and the register setting.

Register	BT value	
	0.5	1.0
[FSK_DEV0_H/GFIL0: B1 0x32]	0x24	0x00
[FSK_DEV0_L/GFIL1: B1 0x33]	0xD6	0x00
[FSK_DEV1_H/GFIL2: B1 0x34]	0x19	0x02
[FSK_DEV1_L/GFIL3: B1 0x35]	0x29	0x0C
[FSK_DEV2_H/GFIL4: B1 0x36]	0x3A	0x31
[FSK_DEV2_L/GFIL5: B1 0x37]	0x48	0x74
[FSK_DEV3_H/GFIL6: B1 0x38]	0x4C	0x9A

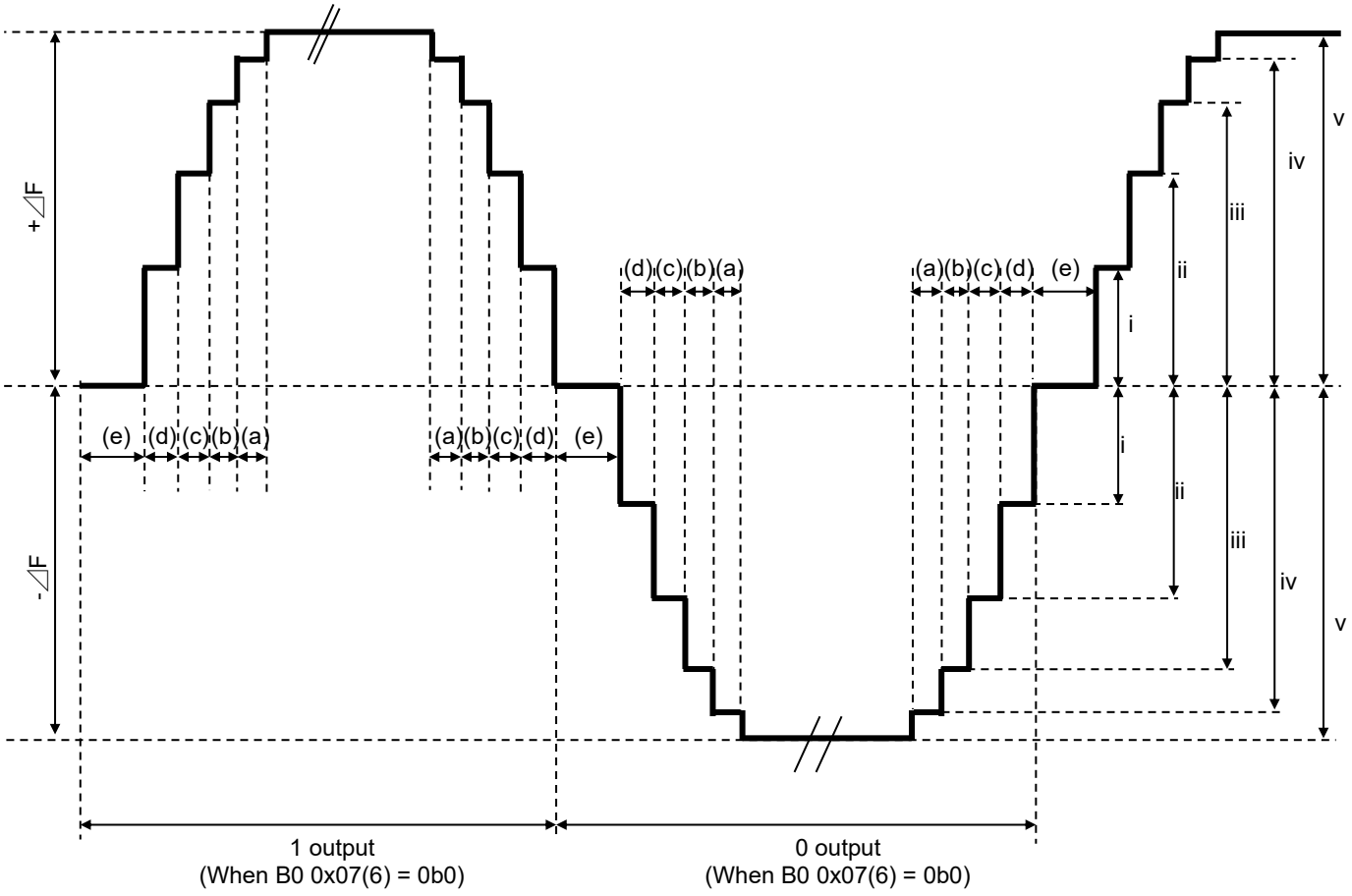
[Note]

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

(2) FSK modulation setting

FSK mode can be set by GFSK_EN([DATA_SET1: B0 0x07(4)])=0b0. Also, fine frequency deviation can be set by [FSK_DEV0_H/GFIL0: B1 0x32] - [FSK_DEV4_L: B1 0x3B]. By adjusting the setting value of [FSK_TIM_ADJ4: B1 0x3C] - [FSK_TIM_ADJ0: B1 0x40], FSK timing can be fine tuned. 2FSK/4FSK can be selected by FSK_SEL[DATA_SET2: B0 0x08(5)].

[2FSK]

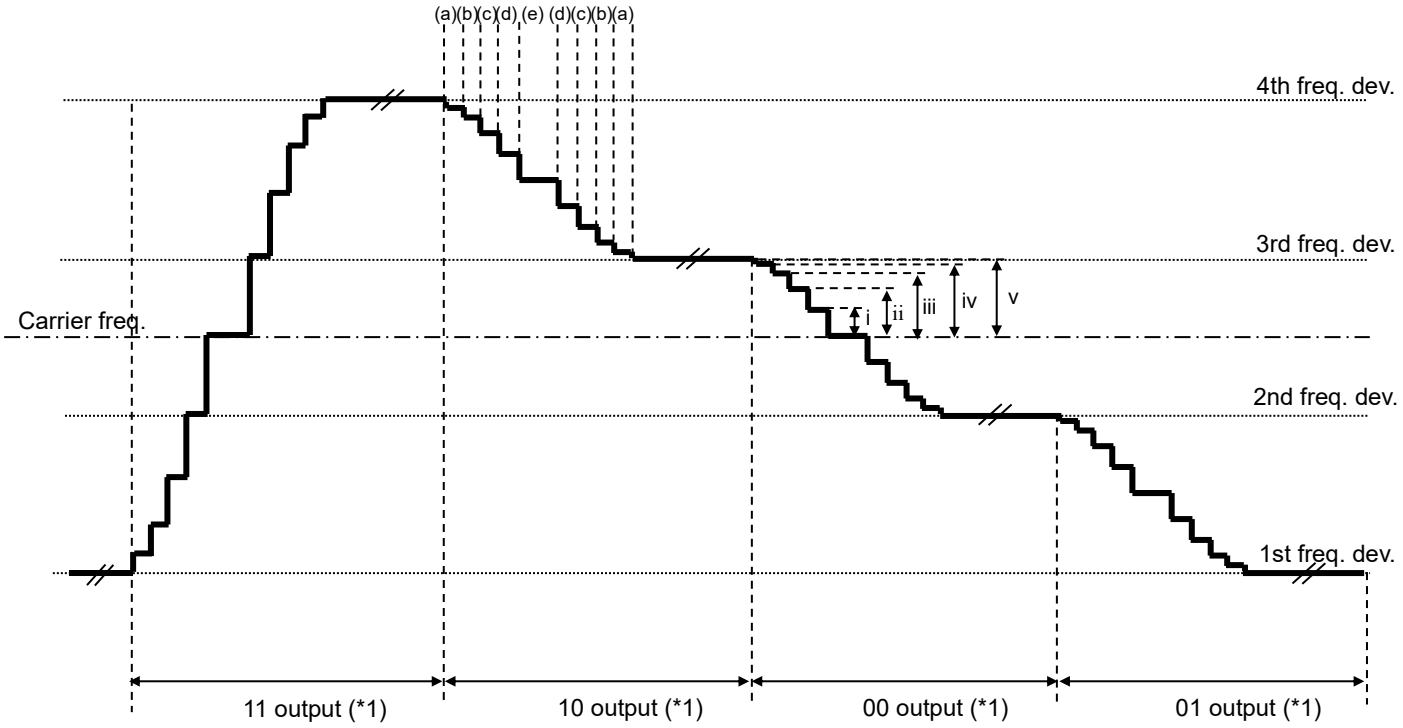


Frequency deviation setting				Time setting			
Symbol	Register name	Address	Function	Symbol	Register name	Address	Function
i	FSK_FDEV0_H/GFIL0 FSK_FDEV0_L/GFIL1	B1 0x32/33	Frequency deviation approx. 34 (Hz)	(a)	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4 MHz/12 MHz counter value (*1)
ii	FSK_FDEV1_H/GFIL2 FSK_FDEV1_L/GFIL3	B1 0x34/35		(b)	FSK_TIM_ADJ3	B1 0x3D	
iii	FSK_FDEV2_H/GFIL4 FSK_FDEV2_L/GFIL5	B1 0x36/37		(c)	FSK_TIM_ADJ2	B1 0x3E	
iv	FSK_FDEV3_H/GFIL6 FSK_FDEV3_L	B1 0x38/39		(d)	FSK_TIM_ADJ1	B1 0x3F	
v	FSK_FDEV4_H FSK_FDEV4_L	B1 0x3A/3B		(e)	FSK_TIM_ADJ0	B1 0x40	

(*1) Modulation timing resolution can be switched by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

[Note]
GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

[4FSK]



(*1) The mapping of the data (00/101/0/11) for each frequency deviation (1st to 4th) can be changed by [4FSK_DATA_MAP: B1 0x40].

(*2) If the frequency is changed by 2 levels such as from 1st to 3rd frequency deviation, the amount of the frequency change is 2 times as much as i to v. If the frequency is changed by 3 levels such as from 1st to 4th frequency deviation, the amount of the frequency change is 3 times as much as i to v.

The table below indicates the frequency deviation setting. The parameter of calculation formula is the register bit name.

Frequency deviation setting			
Symbol	Formula	Address	Function
i	FSK_FDEV4 - FSK_FDEV3	B1 0x3A/3B, B1 0x38/39	Frequency deviation approx. 34 (Hz)
ii	FSK_FDEV4 - FSK_FDEV2	B1 0x3A/3B, B1 0x36/37	
iii	FSK_FDEV4 - FSK_FDEV1	B1 0x3A/3B, B1 0x34/35	
iv	FSK_FDEV4 - FSK_FDEV0	B1 0x3A/3B, B1 0x32/33	
v	FSK_FDEV4	B1 0x3A/3B	

Time setting			
Symbol	Register name	Address	Function
(a)	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4 MHz/12 MHz counter value (*1)
(b)	FSK_TIM_ADJ3	B1 0x3D	
(c)	FSK_TIM_ADJ2	B1 0x3E	
(d)	FSK_TIM_ADJ1	B1 0x3F	
(e)	FSK_TIM_ADJ0	B1 0x40	

(*1) Modulation timing resolution can be switched by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

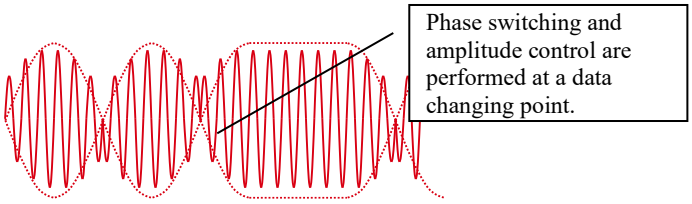
[Note]

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

○BPSK Modulation

This LSI is equipped with the following two methods for BPSK modulation.

- Phase switching method
  Switch the phase of carrier signal between 0 and 180 ° according to TX data.
- Frequency control method
  Control the frequency of carrier signal according to TX data to switch the phase.



BPSK modulation waveform (PA output image)
Modulation is performed through phase switching and PA (amplitude) control.

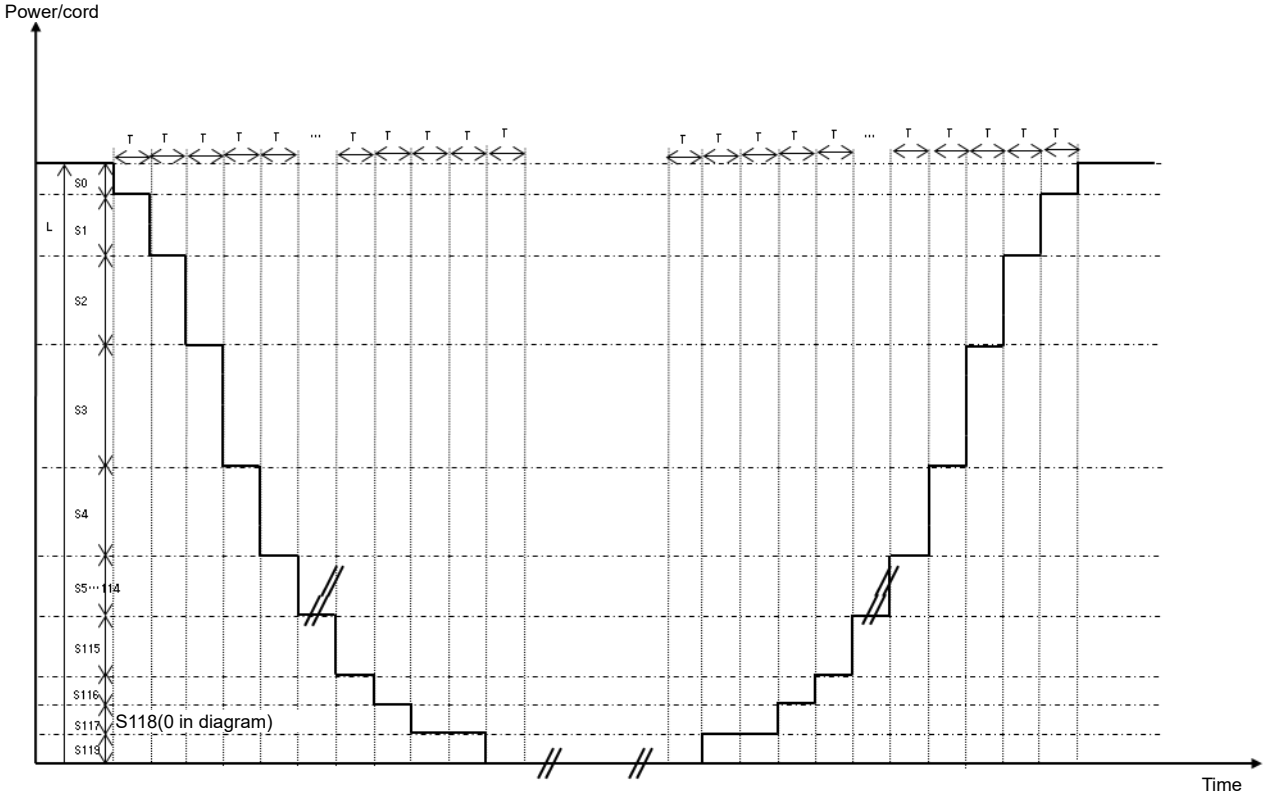
The following registers need to be set for BPSK method/PA control setting. For the setting value, use the value specified in "Initialization Table".

Bit name	Address	BPSK method	
		Phase switching	Phase switching
MOD_TYPE[1:0]	[MOD_CTRL: B6 0x01(1-0)]	✓ (0b01)	✓ (0b01)
BPSK_PLL_CTRL	[BPSK_PLL_CTRL: B0 0x7B(0)]	✓ (0b0)	✓ (0b1)
GFSK_EN	[DATA_SET1: B0 0x07(4)]	✓ (0b1)	✓ (0b1)
BPSK_P_CLKEL	[BPSK_PLL_CTRL: B6 0x7B(1)]	-	✓
BPSK_P_START[10:0]	[BPSK_P_START_H/L: B6 0x7C(2-0)/7D(7-0)]	-	✓
BPSK_P_HOLD[11:0]	[BPSK_P_HOLD_H/L: B6 0x7E(3-0)/7F(7-0)]	-	✓
BPSK_STEP_EN	[BPSK_STEP_CTRL:B10 0x01(4)]	✓ (0b1)	✓ (0b1)
BPSK_STEP_SEL	[BPSK_STEP_CTRL:B10 0x01(5)]	✓	✓
BPSK_CLK_SEL	[BPSK_STEP_CTRL:B10 0x01(6)]	✓	✓
BPSK_CLK_SET[8:0]	[BPSK_STEP_CTRL:B10 0x01(0)] [BPSK_STEP_CLK_SET:B10 0x02(7-0)]	✓	✓
STEP0[3:0]-STEP119[3:0]	[BPSK_STEP_SET0:B10 0x04(3-0)] [BPSK_STEP_SET0:B10 0x04(7-4)] … [BPSK_STEP_SET59:B10 0x3F(3-0)] [BPSK_STEP_SET59:B10 0x3F(7-4)]	✓	✓

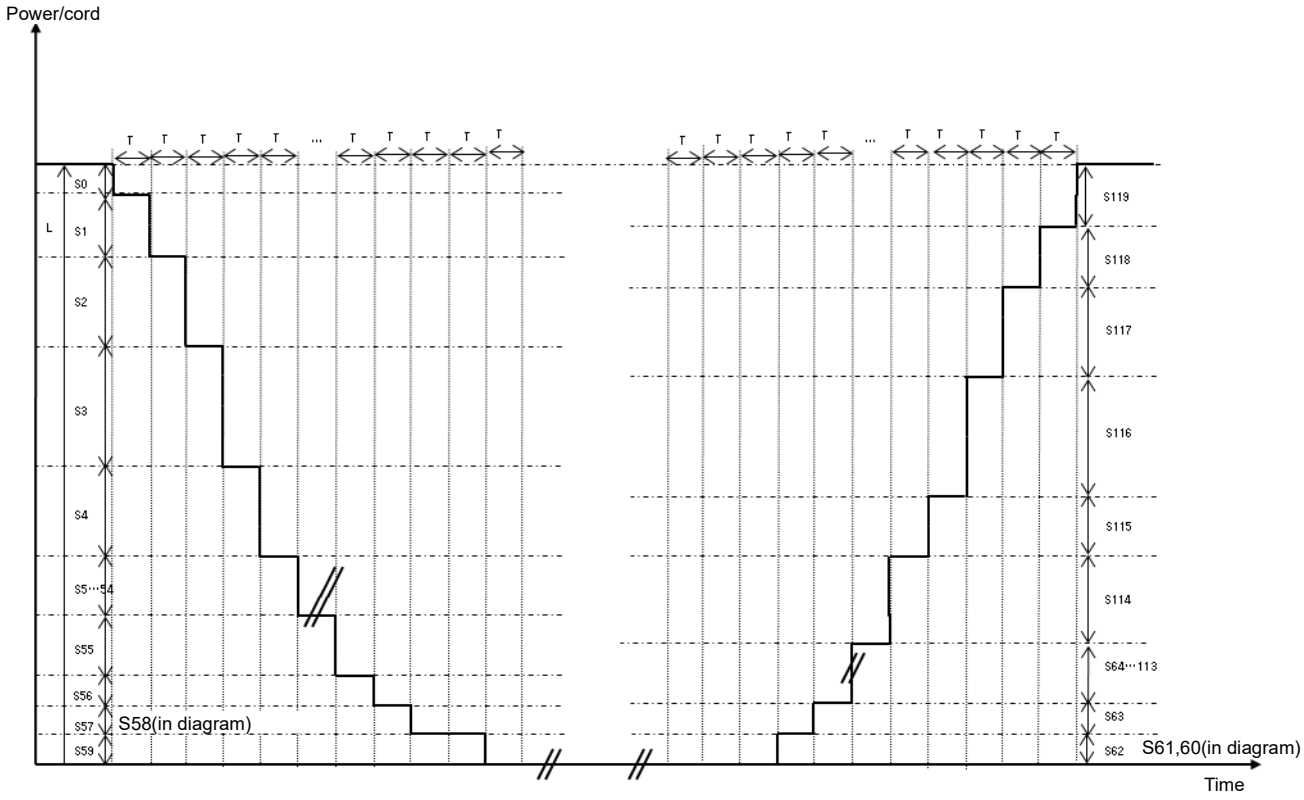
To suppress harmonics generated at the time of phase/frequency switching, TX power control is performed by PA before and after phase/frequency switching. The PA controls shown in the following table are available for the above two methods:

(a) Common PA power down/up setting
(b) Individual PA power down/up setting

(a) Common PA power down/up setting (BPSK_STEP_SEL([BPSK_STEP_CTLR: B10 0x01(5)]) = 0b1)



(b) Individual PA power down/up setting (BPSK_STEP_SEL([BPSK_STEP_CTLR: B10 0x01(5)]) = 0b0)



PA control related registers in BPSK modulation are as follows:

Symbol	Bit name	Address	Function	Remarks
S0	STEP0[3:0]	[B10 0x04(3-0)]	BPSK step control 0	
S1	STEP1[3:0]	[B10 0x04(7-4)]	BPSK step control 1	
S2	STEP2[3:0]	[B10 0x05(3-0)]	BPSK step control 2	
S3	STEP3[3:0]	[B10 0x05(7-4)]	BPSK step control 3	
S4	STEP4[3:0]	[B10 0x06(3-0)]	BPSK step control 4	
S5	STEP5[3:0]	[B10 0x06(7-4)]	BPSK step control 5	
S6	STEP6[3:0]	[B10 0x07(3-0)]	BPSK step control 6	
S7	STEP7[3:0]	[B10 0x07(7-4)]	BPSK step control 7	
S8	STEP8[3:0]	[B10 0x08(3-0)]	BPSK step control 8	
S9	STEP9[3:0]	[B10 0x08(7-4)]	BPSK step control 9	
S10	STEP10[3:0]	[B10 0x09(3-0)]	BPSK step control 10	
S11	STEP11[3:0]	[B10 0x09(7-4)]	BPSK step control 11	
S12	STEP12[3:0]	[B10 0x0A(3-0)]	BPSK step control 12	
S13	STEP13[3:0]	[B10 0x0A(7-4)]	BPSK step control 13	
S14	STEP14[3:0]	[B10 0x0B(3-0)]	BPSK step control 14	
S15	STEP15[3:0]	[B10 0x0B(7-4)]	BPSK step control 15	
S16	STEP16[3:0]	[B10 0x0C(3-0)]	BPSK step control 16	
S17	STEP17[3:0]	[B10 0x0C(7-4)]	BPSK step control 17	
S18	STEP18[3:0]	[B10 0x0D(3-0)]	BPSK step control 18	
S19	STEP19[3:0]	[B10 0x0D(7-4)]	BPSK step control 19	
S20	STEP20[3:0]	[B10 0x0E(3-0)]	BPSK step control 20	
S21	STEP21[3:0]	[B10 0x0E(7-4)]	BPSK step control 21	
S22	STEP22[3:0]	[B10 0x0F(3-0)]	BPSK step control 22	
S23	STEP23[3:0]	[B10 0x0F(7-4)]	BPSK step control 23	
S24	STEP24[3:0]	[B10 0x10(3-0)]	BPSK step control 24	
S25	STEP25[3:0]	[B10 0x10(7-4)]	BPSK step control 25	
S26	STEP26[3:0]	[B10 0x11(3-0)]	BPSK step control 26	
S27	STEP27[3:0]	[B10 0x11(7-4)]	BPSK step control 27	
S28	STEP28[3:0]	[B10 0x12(3-0)]	BPSK step control 28	
S29	STEP29[3:0]	[B10 0x12(7-4)]	BPSK step control 29	
S30	STEP30[3:0]	[B10 0x13(3-0)]	BPSK step control 30	
S31	STEP31[3:0]	[B10 0x13(7-4)]	BPSK step control 31	
S32	STEP32[3:0]	[B10 0x14(3-0)]	BPSK step control 32	
S33	STEP33[3:0]	[B10 0x14(7-4)]	BPSK step control 33	
S34	STEP34[3:0]	[B10 0x15(3-0)]	BPSK step control 34	
S35	STEP35[3:0]	[B10 0x15(7-4)]	BPSK step control 35	
S36	STEP36[3:0]	[B10 0x16(3-0)]	BPSK step control 36	
S37	STEP37[3:0]	[B10 0x16(7-4)]	BPSK step control 37	
S38	STEP38[3:0]	[B10 0x17(3-0)]	BPSK step control 38	
S39	STEP39[3:0]	[B10 0x17(7-4)]	BPSK step control 39	
S40	STEP40[3:0]	[B10 0x18(3-0)]	BPSK step control 40	
S41	STEP41[3:0]	[B10 0x18(7-4)]	BPSK step control 41	
S42	STEP42[3:0]	[B10 0x19(3-0)]	BPSK step control 42	
S43	STEP43[3:0]	[B10 0x19(7-4)]	BPSK step control 43	
S44	STEP44[3:0]	[B10 0x1A(3-0)]	BPSK step control 44	
S45	STEP45[3:0]	[B10 0x1A(7-4)]	BPSK step control 45	
S46	STEP46[3:0]	[B10 0x1B(3-0)]	BPSK step control 46	
S47	STEP47[3:0]	[B10 0x1B(7-4)]	BPSK step control 47	
S48	STEP48[3:0]	[B10 0x1C(3-0)]	BPSK step control 48	
S49	STEP49[3:0]	[B10 0x1C(7-4)]	BPSK step control 49	
S50	STEP50[3:0]	[B10 0x1D(3-0)]	BPSK step control 50	
S51	STEP51[3:0]	[B10 0x1D(7-4)]	BPSK step control 51	
S52	STEP52[3:0]	[B10 0x1E(3-0)]	BPSK step control 52	
S53	STEP53[3:0]	[B10 0x1E(7-4)]	BPSK step control 53	

PA control register list (continued)

Symbol	Bit name	Address	Function	Remarks
S54	STEP54[3:0]	[B10 0x1F(3-0)]	BPSK step control 54	
S55	STEP55[3:0]	[B10 0x1F(7-4)]	BPSK step control 55	
S56	STEP56[3:0]	[B10 0x20(3-0)]	BPSK step control 56	
S57	STEP57[3:0]	[B10 0x20(7-4)]	BPSK step control 57	
S58	STEP58[3:0]	[B10 0x21(3-0)]	BPSK step control 58	
S59	STEP59[3:0]	[B10 0x21(7-4)]	BPSK step control 59	
S60	STEP60[3:0]	[B10 0x22(3-0)]	BPSK step control 60	
S61	STEP61[3:0]	[B10 0x22(7-4)]	BPSK step control 61	
S62	STEP62[3:0]	[B10 0x23(3-0)]	BPSK step control 62	
S63	STEP63[3:0]	[B10 0x23(7-4)]	BPSK step control 63	
S64	STEP64[3:0]	[B10 0x24(3-0)]	BPSK step control 64	
S65	STEP65[3:0]	[B10 0x24(7-4)]	BPSK step control 65	
S66	STEP66[3:0]	[B10 0x25(3-0)]	BPSK step control 66	
S67	STEP67[3:0]	[B10 0x25(7-4)]	BPSK step control 67	
S68	STEP68[3:0]	[B10 0x26(3-0)]	BPSK step control 68	
S69	STEP69[3:0]	[B10 0x26(7-4)]	BPSK step control 69	
S70	STEP70[3:0]	[B10 0x27(3-0)]	BPSK step control 70	
S71	STEP71[3:0]	[B10 0x27(7-4)]	BPSK step control 71	
S72	STEP72[3:0]	[B10 0x28(3-0)]	BPSK step control 72	
S73	STEP73[3:0]	[B10 0x28(7-4)]	BPSK step control 73	
S74	STEP74[3:0]	[B10 0x29(3-0)]	BPSK step control 74	
S75	STEP75[3:0]	[B10 0x29(7-4)]	BPSK step control 75	
S76	STEP76[3:0]	[B10 0x2A(3-0)]	BPSK step control 76	
S77	STEP77[3:0]	[B10 0x2A(7-4)]	BPSK step control 77	
S78	STEP78[3:0]	[B10 0x2B(3-0)]	BPSK step control 78	
S79	STEP79[3:0]	[B10 0x2B(7-4)]	BPSK step control 79	
S80	STEP80[3:0]	[B10 0x2C(3-0)]	BPSK step control 80	
S81	STEP81[3:0]	[B10 0x2C(7-4)]	BPSK step control 81	
S82	STEP82[3:0]	[B10 0x2D(3-0)]	BPSK step control 82	
S83	STEP83[3:0]	[B10 0x2D(7-4)]	BPSK step control 83	
S84	STEP84[3:0]	[B10 0x2E(3-0)]	BPSK step control 84	
S85	STEP85[3:0]	[B10 0x2E(7-4)]	BPSK step control 85	
S86	STEP86[3:0]	[B10 0x2F(3-0)]	BPSK step control 86	
S87	STEP87[3:0]	[B10 0x2F(7-4)]	BPSK step control 87	
S88	STEP88[3:0]	[B10 0x30(3-0)]	BPSK step control 88	
S89	STEP89[3:0]	[B10 0x30(7-4)]	BPSK step control 89	
S90	STEP90[3:0]	[B10 0x31(3-0)]	BPSK step control 90	
S91	STEP91[3:0]	[B10 0x31(7-4)]	BPSK step control 91	
S92	STEP92[3:0]	[B10 0x32(3-0)]	BPSK step control 92	
S93	STEP93[3:0]	[B10 0x32(7-4)]	BPSK step control 93	
S94	STEP94[3:0]	[B10 0x33(3-0)]	BPSK step control 94	
S95	STEP95[3:0]	[B10 0x33(7-4)]	BPSK step control 95	
S96	STEP96[3:0]	[B10 0x34(3-0)]	BPSK step control 96	
S97	STEP97[3:0]	[B10 0x34(7-4)]	BPSK step control 97	
S98	STEP98[3:0]	[B10 0x35(3-0)]	BPSK step control 98	
S99	STEP99[3:0]	[B10 0x35(7-4)]	BPSK step control 99	
S100	STEP100[3:0]	[B10 0x36(3-0)]	BPSK step control 100	
S101	STEP101[3:0]	[B10 0x36(7-4)]	BPSK step control 101	
S102	STEP102[3:0]	[B10 0x37(3-0)]	BPSK step control 102	
S103	STEP103[3:0]	[B10 0x37(7-4)]	BPSK step control 103	
S104	STEP104[3:0]	[B10 0x38(3-0)]	BPSK step control 104	
S105	STEP105[3:0]	[B10 0x38(7-4)]	BPSK step control 105	
S106	STEP106[3:0]	[B10 0x39(3-0)]	BPSK step control 106	

PA control register list (continued)

Symbol	Bit name	Address	Function	Remarks
S107	STEP107[3:0]	[B10 0x39(7-4)]	BPSK step control 107	
S108	STEP108[3:0]	[B10 0x3A(3-0)]	BPSK step control 108	
S109	STEP109[3:0]	[B10 0x3A(7-4)]	BPSK step control 109	
S110	STEP110[3:0]	[B10 0x3B(3-0)]	BPSK step control 110	
S111	STEP111[3:0]	[B10 0x3B(7-4)]	BPSK step control 111	
S112	STEP112[3:0]	[B10 0x3C(3-0)]	BPSK step control 112	
S113	STEP113[3:0]	[B10 0x3C(7-4)]	BPSK step control 113	
S114	STEP114[3:0]	[B10 0x3D(3-0)]	BPSK step control 114	
S115	STEP115[3:0]	[B10 0x3D(7-4)]	BPSK step control 115	
S116	STEP116[3:0]	[B10 0x3E(3-0)]	BPSK step control 116	
S117	STEP117[3:0]	[B10 0x3E(7-4)]	BPSK step control 117	
S118	STEP118[3:0]	[B10 0x3F(3-0)]	BPSK step control 118	
S119	STEP119[3:0]	[B10 0x3F(7-4)]	BPSK step control 119	
T	BPSK_STEP_CLK_SEL	[B10 0x01(5)]	Step control clock selection setting 0: Master clock frequency / 2 (18 MHz) 1: Master clock frequency / 4 (9 MHz)	Step control clock cycle T = Clock cycle for step control x Step control clock selection setting
	CLK_SET[8:0]	[B0 0x02(0), B0 0x03(7-0)]	Step control clock cycle setting	
L	PA_REG_ADJ[8:0]	[B0 0x67(0), B0 68(7:0)]	PA regulator output voltage adjustment setting	

●RX Related Function

○AFC Function

This LSI part supports AFC function in RX. Frequency deviation (max±20ppm) between remote device and local device can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved. This function can be enabled by setting AFC_EN([AFC/GC_CTRL: B1 0x15(7)])=0b1. Note that the AFC function used to compensate local signals does not work when the spread spectrum function is used.

○Energy Detection Value (ED value) Acquisition Function

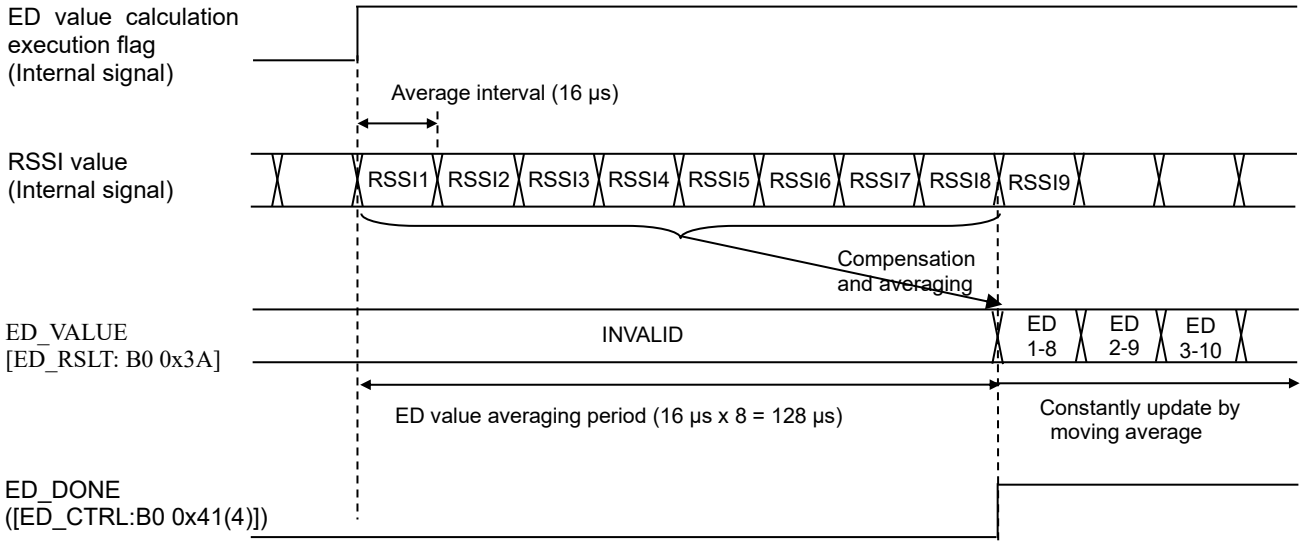
This LSI supports the function to indicate the received signal strength indicator (RSSI) as the energy detection value (ED value). ED value acquisition can be enabled by setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)])=0b1. As soon as a transition is made to RX_ON state, acquisition of ED value starts automatically.
While in RX_ON state, the ED value is constantly updated. ED value is not RSSI value at given timing, but average values. A number of average times can be specified by ED_AVG([ED_CTRL: B0 0x41(2-0)]). During diversity operation, this can be set by 2DIV_ED_AVG([2DIV_MODE: B1 0x48(2-0)]). As soon as ED value is acquired for the number of average processing, ED_DONE([ED_CTRL: B0 0x41(4)]) is set to “1” and ED_VALUE([ED_RSLT: B0 0x3A]) will be updated.

ED_DONE bit will be cleared if one of the following conditions is met.
(a) Antenna is switched.
(b) Gain is switched.
(c) Once stopping ED value acquisition and then resume it.

Timing from ED value starting point to ED value acquisition is calculated as below formula.
ED value average time = Average interval (16μs) * ED value number of average times

The timing example is as follows:

[Condition] ED_AVG[2:0]=0b011 (ED value 8 times average) [ED_CTRL: B0 0x41(2-0)]



○Programmable Channel Filter Bandwidth Function

Channel filter bandwidth can be set by CHFIL_BW_ADJ([CHFIL_BW: B0 0x54(6-0)]), CHFIL_WIDE_SET([CHFIL_BW: B0 0x54(7)]) and CHFIL_BW_OPTION([CHFIL_BW_OPTION: B0 0x6B]). The relationship between the setting value and the channel filter bandwidth is expressed by the following formula.

Channel filter bandwidth [Hz] = {Master clock frequency [Hz] * (CHFIL_WIDE_SET + 1)} / {CHFIL_BW_ADJ * 180} * Magnification setting (CHFIL_BW_OPTION)

See the following table for the channel filter bandwidth for each setting value. Channel filter bandwidth can be set separately for the normal receiving mode and during CCA. For the channel filter bandwidth during CCA, the setting values of CHFIL_BW_ADJ_CCA([CHFIL_BW_CCA: B0 0x6A(6-0)]) and CHFIL_WIDE_SET_CCA([CHFIL_BW_CCA: B0 0x6A(7)]) will be applied.

(1) For the case of CHFIL_WIDE_SET = 0b0 and CHFIL_BW_OPTION = 0b000

CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]	CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]
0	Prohibited	16	12.5
1	200	17	11.8
2	100	18	11.1
3	66.7	19	10.5
4	50	20	10
5	40	21	9.5
6	33.3	22	9.1
7	28.6	23	8.7
8	25	24	8.3
9	22.2	25	8
10	20	26	7.7
11	18.2	27	7.4
12	16.7	28	7.1
13	15.4	・・・	・・・
14	14.3	126	1.59
15	13.3	127	1.57

(2) For the case of CHFIL_WIDE_SET = 0b1 and CHFIL_BW_OPTION = 0b000

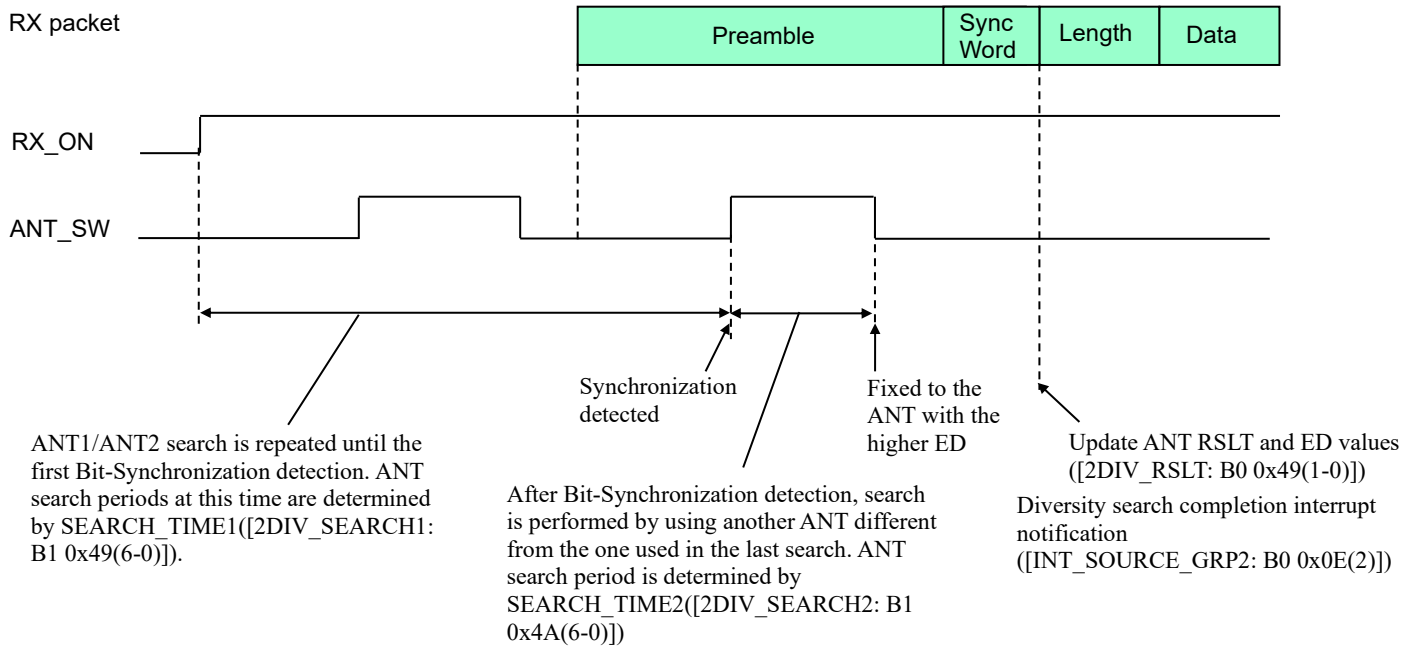
CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]	CHFIL_BW_ADJ [dec]	Channel filter bandwidth [kHz]
0	Prohibited	16	25
1	400	17	23.5
2	200	18	22.2
3	133.3	19	21.1
4	100	20	20
5	80	21	19
6	66.7	22	18.2
7	57.1	23	17.4
8	50	24	16.7
9	44.4	25	16
10	40	26	15.4
11	36.4	27	14.8
12	33.3	28	14.3
13	30.8	・・・	・・・
14	28.6	126	3.18
15	26.7	127	3.14

The channel filter bandwidth needs to be optimized according to the data rate and the maximum frequency deviation.

○Diversity Function

This LSI supports two antenna diversity function.
While in 2DIV_EN([2DIV_CTRL: B0 0x48(0)])=0b1 setting, as soon as RX_ON is set, the diversity mode will start. When diversity mode is started, and upon RX data detection, each ED value will be acquired by switching two antennas. And then antenna with higher ED value will be selected automatically. As diversity uses preamble data for ED value acquisition, longer preamble length is desirable. If preamble is too short, accurate ED values may not be obtained.

The timing diagrams are shown below.



ED value obtained by Diversity ([ANT1_ED: B0 0x4A] or [ANT2_ED: B0 0x4B]) and Diversity antenna result ([2DIV_RSLT: B0 0x49(1-0)]) are updated and overwritten when SyncWord is detected.
The number of detection performed during the ED value calculation is specified by 2DIV_ED_AVG([2DIV_MODE: B1 0x48(2:0)]).
Time resolution of search times ([SEARCH_TIME1] and [SEARCH_TIME2]) can be specified by SEARCH_TIME_SET([2DIV_SEARCH1: B1 0x49(7)]).

When Diversity search completion interrupt INT[10] ([INT__SOURCE_GRP2: B0 0x0E(2)]) is cleared, the ED value obtained by Diversity ([ANT1_ED: B0 0x4A]) or [ANT2_ED: B0 0x4B]) and Diversity antenna result ([2DIV_RSLT: B0 0x49(1-0)]) are cleared to zero.

[Note]
When an incorrect diversity completion is caused by erroneous detection, ML7456N RF part re-executes antenna search automatically. However, when a desired wave is received during the period from the completion of diversity search caused by erroneous detection to the determination of erroneous detection, the obtained ED value ([ANT1_ED: B0 0x4A]) or [ANT2_ED: B0 0x4B]) shows a low ED value different from the input level of desired wave.
The occurrence of this event can be checked by reading out the ED value, which is displayed by [ED_RSLT: B0 0x41], after the occurrence of SyncWord detection interrupt of desired wave INT[13] ([INT_SOURCE_GRP2: B0 0x0E(5)]).

(1) Antenna switching function

Using [2DIV_CTRL: B0 0x48], [ANT_CTRL: B0 0x4C] and [EXT_PA_CTRL: B0 0x53], TX-RX signal selection (TRX_SW), antenna switching signal (ANT_SW), and external PA control signal (DCNT) can be controlled.

Two types of antenna switches (SPDT switch/DPDT switch) can be controlled by [2DIV_CTRL: B0 0x48(3-1)] and [ANT_CTRL: B0 0x4C]). The relationship between the output status of ANT_SW and TRX_SW pins during each antenna switch control and [2DIV_CTRL: B0 0x48(2-1)] is indicated below.

(a) When DPDT switch is used

Set 2PORT_SW([2DIV_CTRL: B0 0x48(1)]) = 0b1 and ANT_CTRL1([2DIV_CTRL: B0 0x48(5)]) = 0b0. ANT_SW and TRX_SW are output as follows during IDLE, TX, and RX states

(default setting): INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarities of ANT_SW and TRX_SW are reversed.

TX/RX state	INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0 (default setting)		INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	H	L	L	H	Idle state
TX	L	H	H	L	TX state
RX	H	L	L	H	This is the initial state when Diversity disable is set to 0b0 ([2DIV_CTRL: B0 0x48(0)]=0b0) and at the start of Diversity when Diversity is enabled ([2DIV_CTRL: B0 0x48(0)]=0b1).
	L/H	H/L	H/L	L/H	If diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1), (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternately during search. When the diversity is complete, it is fixed to either state.

(b) When SPDT switch is used

2PORT_SW([2DIV_CTRL: B0 0x48(1)])=0b0. ANT_SW and TRX_SW are output as follows during IDLE, TX, and RX states

(default setting): INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarity of TRX_SW is reversed

TX/RX state	INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0 (default setting)		INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=1 (reversed polarity)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idle state
TX	L	H	L	L	TX state
RX	L	L	L	H	This is the initial state when Diversity disable is set to 0b0 ([2DIV_CTRL: B0 0x48(0)]=0b0) and at the start of Diversity when Diversity is enabled ([2DIV_CTRL: B0 0x48(0)]=0b1).
	H/L	L	H/L	H	If diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1), (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternately during search. When the diversity is complete, it is fixed to either state.

By setting INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0b1 and ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b1 to the above default setting, the polarity of ANT_SW pin will be reversed.

TX/RX state	INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0 ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0 (default setting)		INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=1 ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	This is the initial state when Diversity disable is set to 0b0 ([2DIV_CTRL: B0 0x48(0)]=0b0) and at the start of Diversity when Diversity is enabled ([2DIV_CTRL: B0 0x48(0)]=0b1).
	H/L	L	L/H	L	If diversity enable is set ([2DIV_CTRL: B0 0x48(0)]=0b1), (ANT_SW=H, TRX_SW=L) and (ANT_SW=L, TRX_SW=H) are switched alternately during search. When the diversity is complete, it is fixed to either state.

(2) Antenna switch forced setting

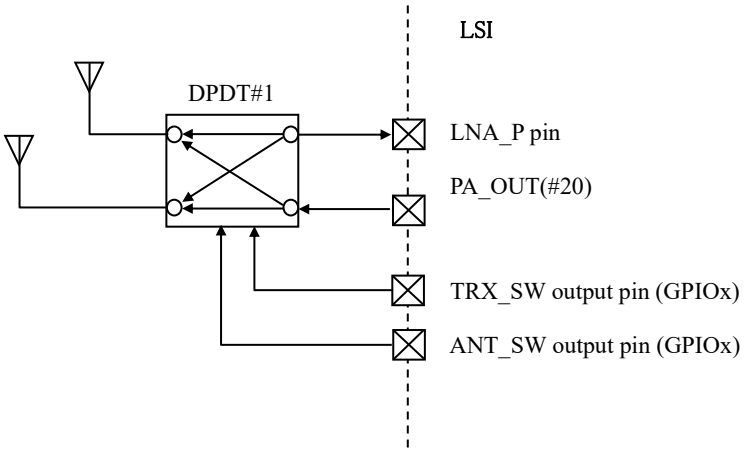
By using [ANT_CTRL: B0 0x4C] register, ANT_SW pin output status can be set forcibly.

TX: By setting TX_ANT_EN([ANT_CTRL: B0 0x4C(0)])=0b1, the setting value of TX_ANT([ANT_CTRL: B0 0x4C(1)]) will be output.
RX: By setting RX_ANT_EN([ANT_CTRL: B0 0x4C(4)])=0b1, the setting value of RX_ANT([ANT_CTRL: B0 0x4C(5)]) will be output.

However, when output is defined forcibly by [GPIO*_CTRL: B0 0x4E - 0x51] registers, [GPIO*_CTRL:B0 0x4E - 0x51] register settings have higher priority.

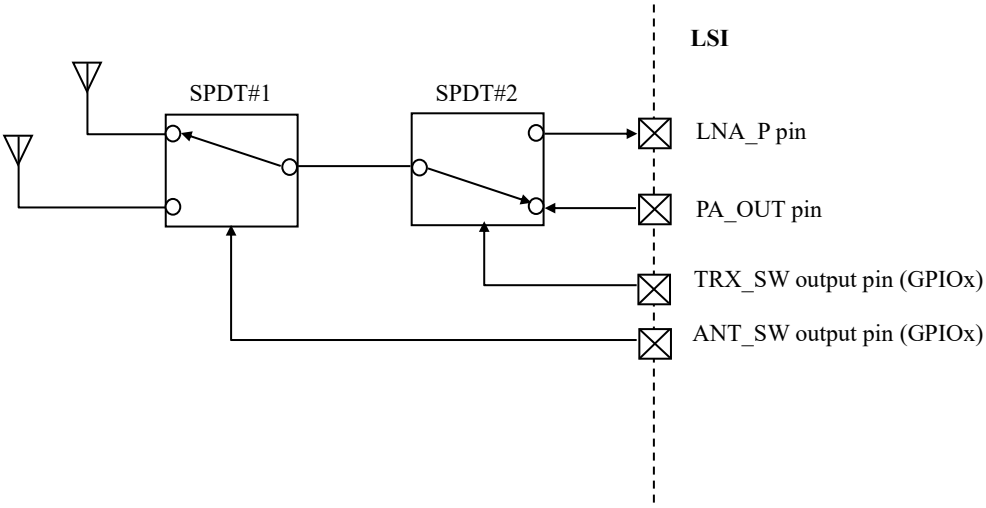
Antenna switching control signals can also be used as follows.

[Example 1] Using one DPDT switch
2PORT_SW([2DIV_CTRL: B0 0x48(1)]) to 0b1.



(*) By allocating one more GPIO to an external PA, it becomes possible to control both DPDT SW and the external PA.
(*) External circuits between LNA_P/PA_OUT pin and antenna switch (DPDT#1) are omitted in this example.

[Example 2] Using two SPDT switches
2PORT_SW([2DIV_CTRL: B0 0x48(1)]) to 0b0.



(*) By allocating one more GPIO to an external PA, it becomes possible to control both DPDT SW and the external PA.
(*) External circuits between LNA_P/PA_OUT pin and antenna switch (SPDT#2) are omitted in this example.

○CCA (Clear Channel Assessment) Function

This LSI supports CCA function. CCA is a function that receives frequency channels and makes a judgment whether the specified frequency channel is busy or idle. This LSI supports Normal mode, Continuous mode and IDLE detection mode. These modes can be set as follows:

[CCA mode setting]

	[CCA_CTRL: B0 0x39]		
	Bit4 (CCA_EN)	Bit5 (CCA_CPU_EN)	Bit6 (CCA_IDLE_EN)
Normal mode	0b1	0b0	0b0
Continuous mode	0b1	0b1	0b0
IDLE detection mode	0b1	0b0	0b1

(1) Normal mode

Normal mode determines IDLE or BUSY. When CCA_EN(CCA_CTRL: B0 0x39(4)]) = 0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)]) = 0b0, and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)]) = 0b0, CCA (normal mode) is executed by RX_ON. CCA judgment is based on the comparison of the average ED value displayed by the [ED_RSLT: B0 0x3A] register with the CCA threshold set by the [CCA_LVL: B0 0x37] register. If the average ED value displayed by [ED_RSLT: B0 0x3A] exceeds the CCA threshold, it is determined as BUSY, and CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) is set to 0b01. If the average ED value continues to be smaller than the CCA threshold for the IDLE detection period set by IDLE_WAIT[9:0] of [IDLE_WAIT_L: B0 0x3C] and [IDLE_WAIT_H: B0 0x3B])], it is determined as IDLE, and CCA_RSLT[1:0] is set to 0b00. For the detailed operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long time period”.
If “BUSY” or “IDLE” state is detected, CCA completion interrupt (INT[18] of group 3) is generated, and CCA_EN bit is cleared to 0b0 automatically.
Upon clearing CCA completion interrupt, CCA_RSLT[1:0] is reset to 0b00. Therefore, CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.
If the ED value exceeds the value set by [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed as long as the target ED value is included in the averaging target range. At this time, if the average ED value is larger than [CCA_LVL: B0 0x37], it is determined as BUSY, and CCA is completed. However, if the average ED value is smaller than [CCA_LVL: B0 0x37], IDLE determination is not performed, and 0b11 is displayed in CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]). In this case, CCA continues until BUSY determination is made or IDLE determination is made after the target ED value is excluded from the averaging target range. For the detailed operation for the case where the ED value exceeds [CCA_IGNORE_LVL: B0 0x36], please refer to “IDLE determination exclusion under strong signal input”.

Time from CCA command issue to CCA completion is in the formula below.

[IDLE detection]
CCA execution time = (ED value average times + IDLE_WAIT setting) x Average interval (16 us)

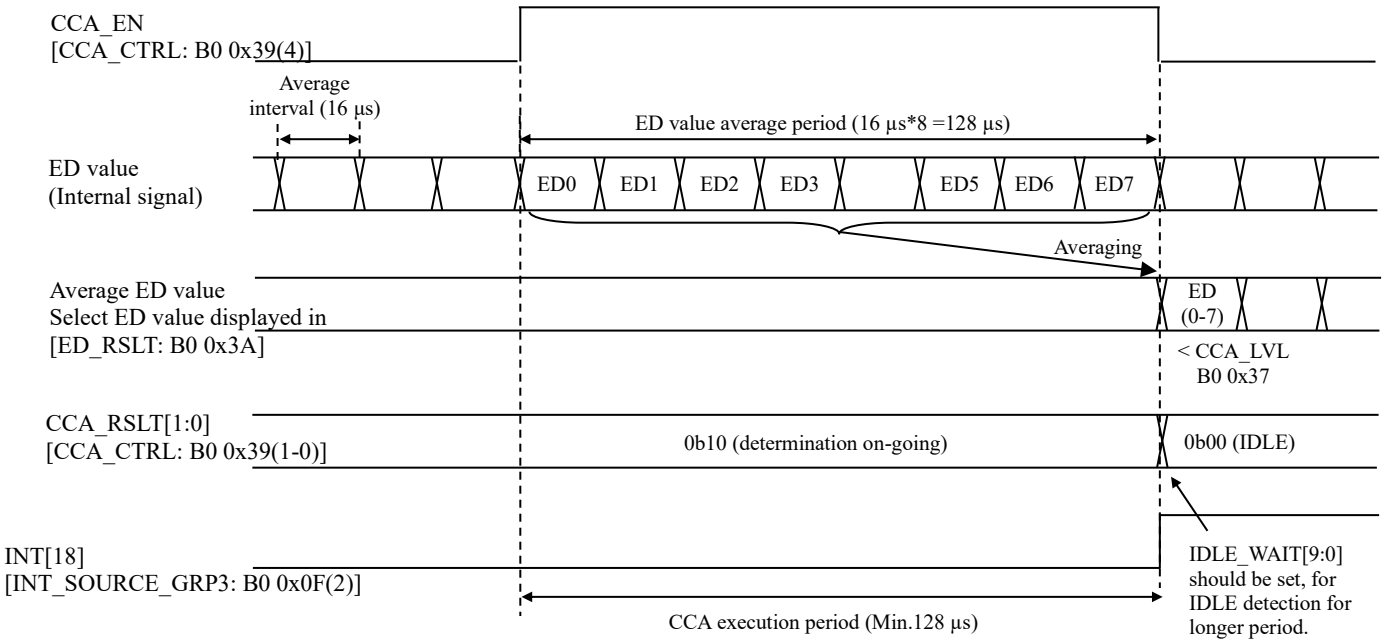
[BUSY detection]
CCA execution time = ED value average times x Average interval (16 us)

* The above formulas do not take the IDLE detection exclusion by [CCA_IGNORE_LVL: B0 0x36] into account. Set [CCA_IGNORE_LVL: B0 0x36] in a way so that the relationship of [CCA_IGNORE_LVL:B0 0x36] >= [CCA_LVL: B0 0x37] is maintained. B0 0x36], please refer to ”IDLE determination exclusion under strong signal input”.

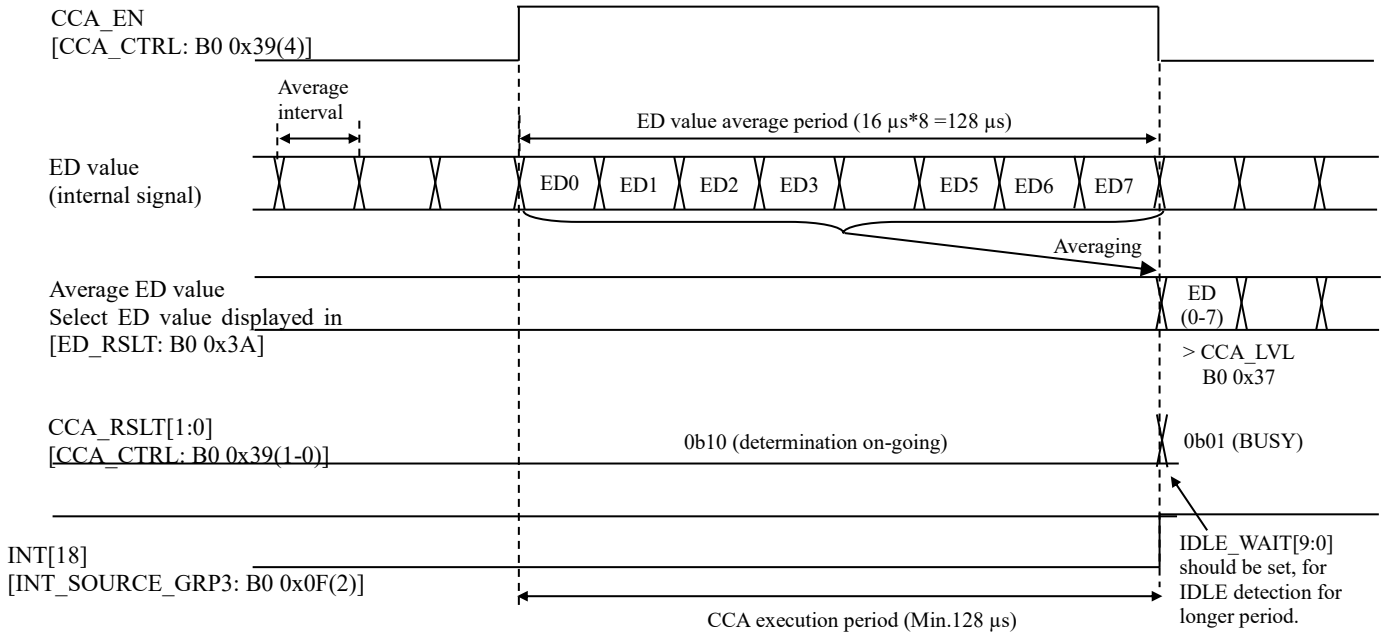
The following is timing chart for normal mode.

[Condition]
ED_AVG[2:0]=0b011 (ED value 8 times average) [ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection time 0 µs) [IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]

[IDLE detection case]



[BUSY result case]



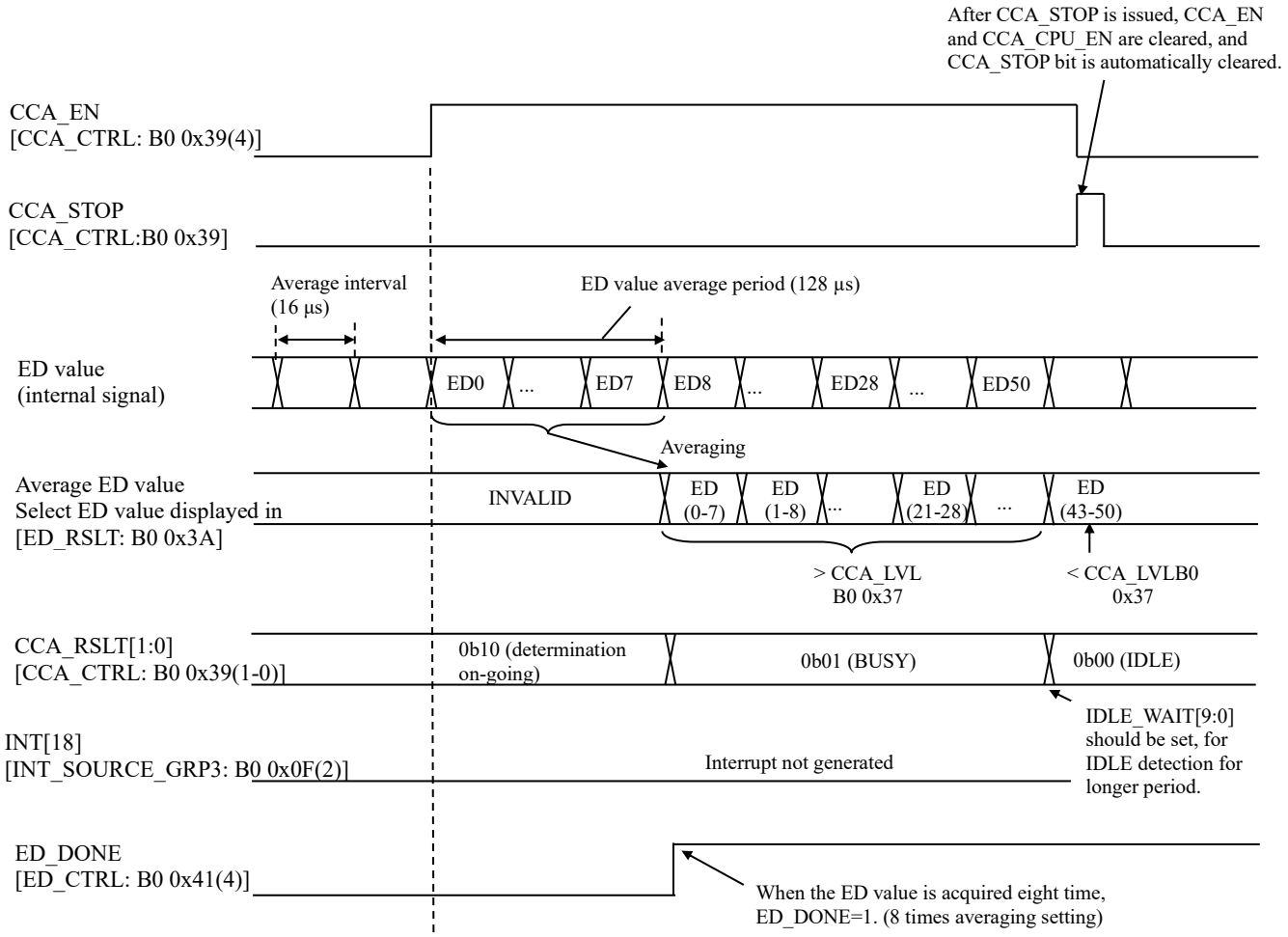
(2) Continuous mode

Continuous mode continues CCA until terminated by the host CPU. When CCA_EN(CCA_CTRL: B0 0x39(4)]) = 0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)]) = 0b1, and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)]) = 0b0, CCA (continuous mode) is executed by RX_ON.
As with the normal mode, CCA judgment is based on the comparison of the average ED value displayed by the [ED_RSLT: B0 0x3A] register with the CCA threshold set by the [CCA_LVL: B0 0x37] register. If the average ED value displayed by ED_VALUE ([ED_RSLT:B0 0x3A]) exceeds the CCA threshold, it is determined as "BUSY, and CCA_RSLT[1:0] is set to 0b01. If the average ED value continues to be smaller than the CCA threshold for the IDLE detection period set by IDLE_WAIT[9:0] of [IDLE_WAIT_L:B0 0x3C] and [IDLE_WAIT_H: B0 0x3B(1-0)], it is determined as IDLE, and CCA_RSLT[1:0] is set to 0b00. For the detailed operation of IDLE_WAIT[9:0], please refer to "IDLE detection for long time period".
If the ED value exceeds the value set by [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed as long as the target ED value is included in the averaging target range. At this time, if the average ED value is larger than [CCA_LVL: B0 0x37], it is determined as BUSY, and CCA_RSLT[1:0] is set to 0b01. However, if the average ED value is smaller than [CCA_LVL: B0 0x37], IDLE determination is not performed, and CCA_RSLT[1:0] is set to 0b11. For the detailed operation for the case where the ED value exceeds [CCA_IGNORE_LVL: B0 0x36], please refer to "IDLE determination exclusion under strong signal input".
The continuous mode does not stop the operation even when BUSY or IDLE is detected. CCA operation continues until 0b1 is set to CCA_STOP ([CCA_CTRL: B0 0x39(7)]). The result is updated every time the ED value is acquired. At this time, CCA completion interrupt INT[18]([INT_SOURCE_GRP2:B0 0x0F(2)]) will not be generated.

The following is timing chart for continuous mode.

[Condition]
ED_AVG[2:0]=0b011 (ED value 8 times average) [ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection time 0 µs) [IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]

[BUSY to IDLE transition, terminated with CCA_STOP]



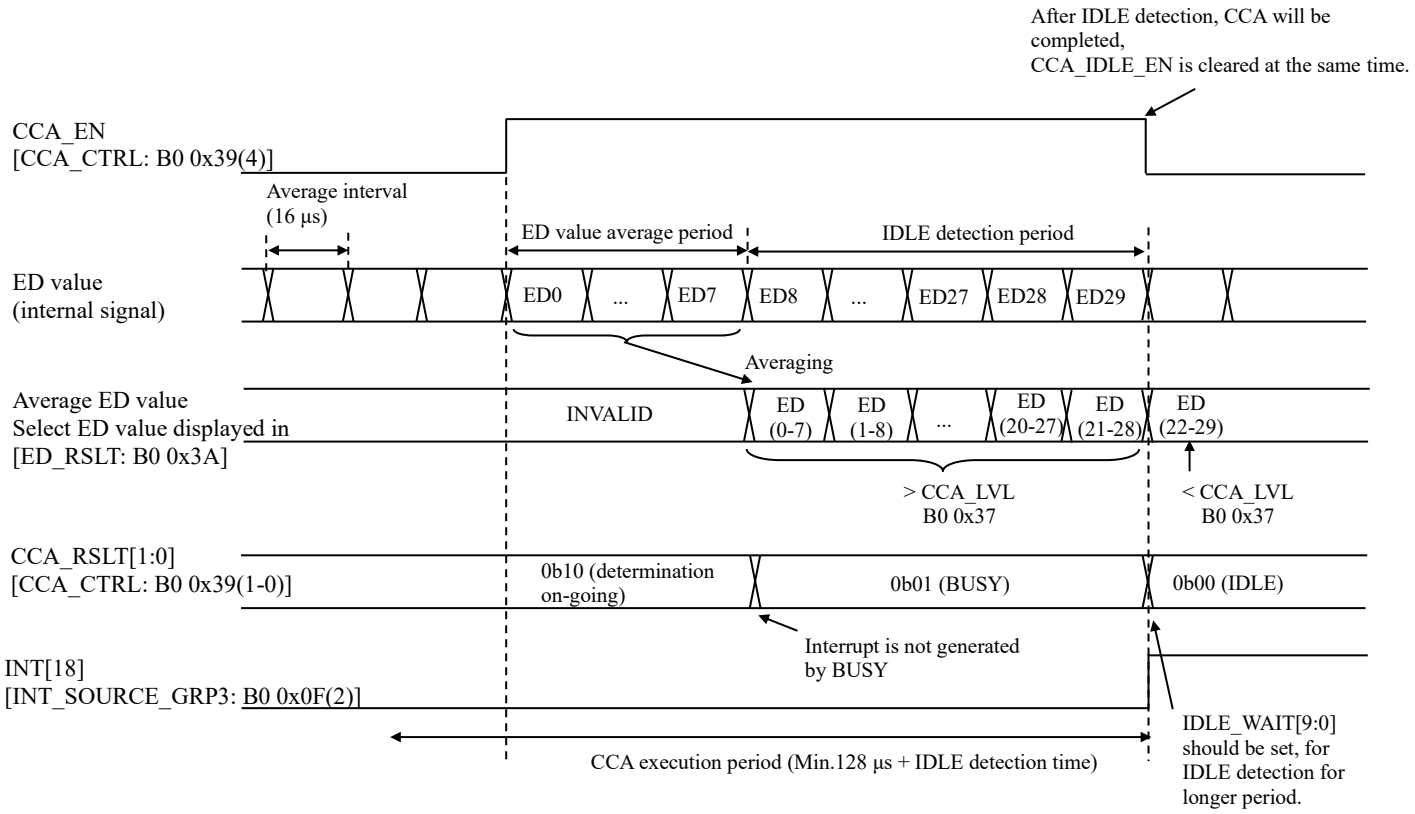
(3) IDLE detection mode

IDLE detection mode continues CCA until IDLE detection. When CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b0, and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b1 are set, CCA (IDLE detection mode) is executed by RX_ON.
As with the normal mode, CCA judgment is based on the comparison of the average ED value displayed by the [ED_RSLT: B0 0x3A] register with the CCA threshold set by the [CCA_LVL: B0 0x37] register. If the average ED value exceeds the CCA threshold, it is determined as BUSY, and CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) is set to 0b01. If the average ED value continues to be smaller than the CCA threshold for the IDLE detection period set by IDLE_WAIT[9:0] of [IDLE_WAIT_L] and [IDLE_WAIT_H]: B0 0x3B,0x3C], it is determined as “IDLE”, and CCA_RSLT[1:0] is set to 0b00. For the detailed operation of IDLE_WAIT[9:0], please refer to “IDLE detection for long time period”.
In IDLE detection mode, CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is generated only when IDLE is detected. B0 0x0F(2)]) is generated. Also, when CCA is executed by CCA_EN setting, CCA_EN(CCA_CTRL: B0 0x39(4)]) and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)]) are cleared to 0b0 automatically.
In IDLE detection mode, CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is not generated while BUSY is detected, and continues to detect IDLE. When CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is cleared, CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) is reset to 0b00. Therefore, CCA_RSLT[1:0] should be read before CCA completion interrupt INT[18]([INT_SOURCE_GRP3: B0 0x0F(2)]) is cleared.
If the ED value exceeds [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed as long as the target ED value is included in the averaging target range. IDLE determination is not performed also when the average ED value is smaller than [CCA_LVL: B0 0x37]. In this case, 0b11 is displayed in CCA_RSLT[1:0], and CCA is continued until IDLE determination is made after the target ED value is excluded from the averaging target range. For the detailed operation for the case where the ED value exceeds [CCA_IGNORE_LVL: B0 0x36], please refer to “IDLE determination exclusion under strong signal input”.

The following is the timing diagram of IDLE detection.

[Upon BUSY detection, continue CCA and IDLE detection case]

[Condition]
ED_AVG[2:0]=0b011 (ED value 8 times average) [ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0000 (IDLE detection time 0 µs) [IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]

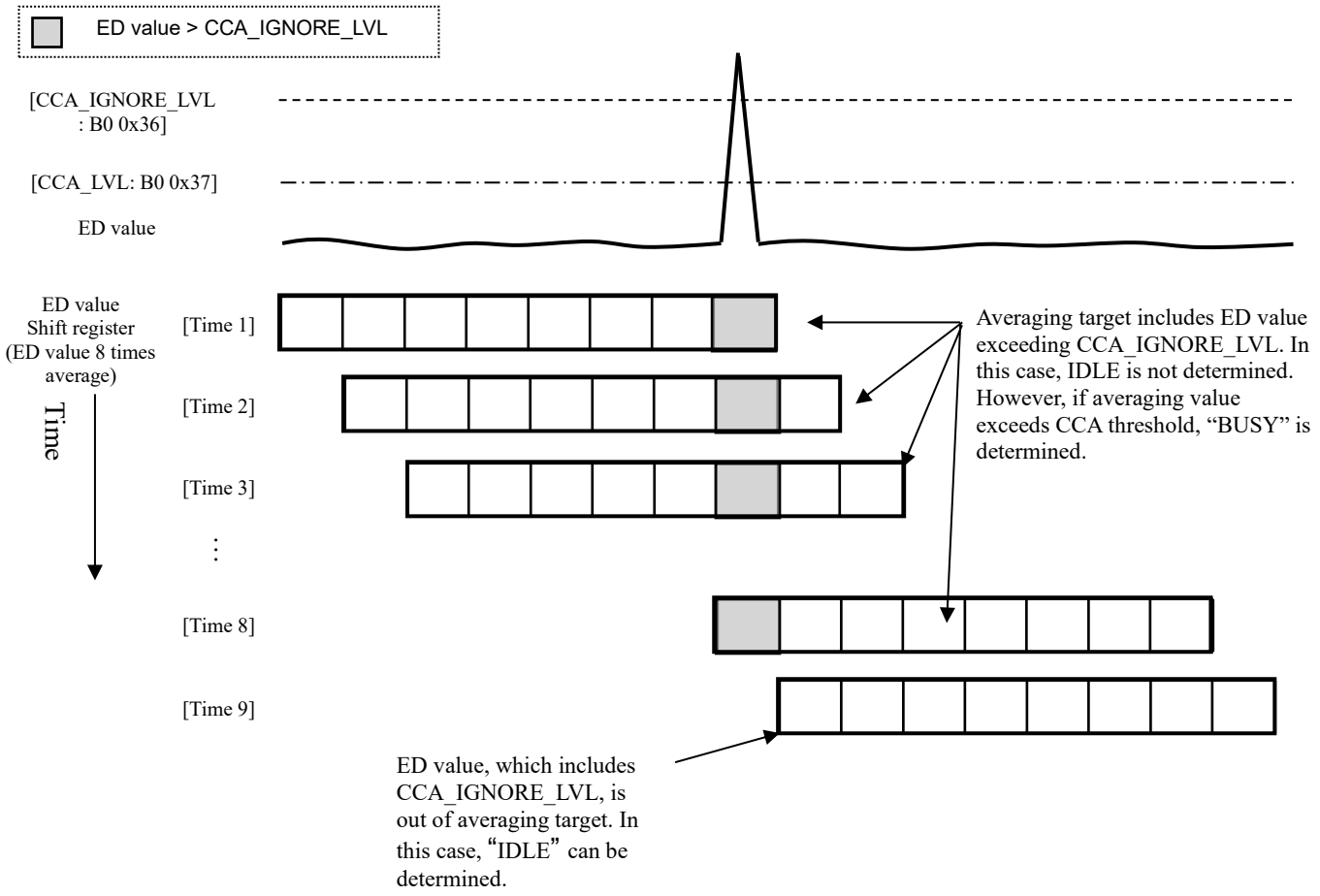


(4) IDLE determination exclusion under strong signal input

If acquired ED value exceeds the value set by [CCA_IGNORE_LVL: B0 0x36], IDLE determination is not performed as long as the given ED value is included in the averaging target range. If the average ED value including this strong ED value displayed by [ED_RSLT: B0 0x39] exceeds the CCA threshold set by [CCA_LVL: B0 0x37], it is determined as "carrier detected (BUSY)", and CCA_RSLT[1:0] ([CCA_CTRL: B0 0x39(1-0)]) is set to 0b01. Also, if this average ED value is equal to or smaller than the CCA threshold, it is determined as "CCA evaluation on-going (ED value excluded from CCA judgment acquired)", and CCA_RSLT[1:0] is set to 0b11.
Even if the moving average of the ED value is equal to or smaller than [CCA_LVL: B0 0x37], IDLE determination is not made when the ED value to be moving-averaged contains a value larger than [CCA_IGNORE_LVL: B0 0x36]. In this case, CCA_RSLT[1:0] indicates 0b11 (on-going), and CCA operation continues until IDLE or BUSY is determined (until IDLE is determined in the IDLE detection mode, or CCA_STOP([CCA_CTRL: B0 0x39(7)]) is issued in the continuous mode).
If the moving average of the ED value exceeds [CCA_LVL: B0 0x37], BUSY is determined immediately regardless of the comparison result of [CCA_IGNORE_LVL: B0 0x36].

[Note]
CCA completion interrupt is notified of only when CCA result is judged as IDLE or BUSY. Therefore, if data whose ED value exceeds CCA_IGNORE_LVL is input intermittently, neither "IDLE" or "BUSY" can be determined and CCA may continues.

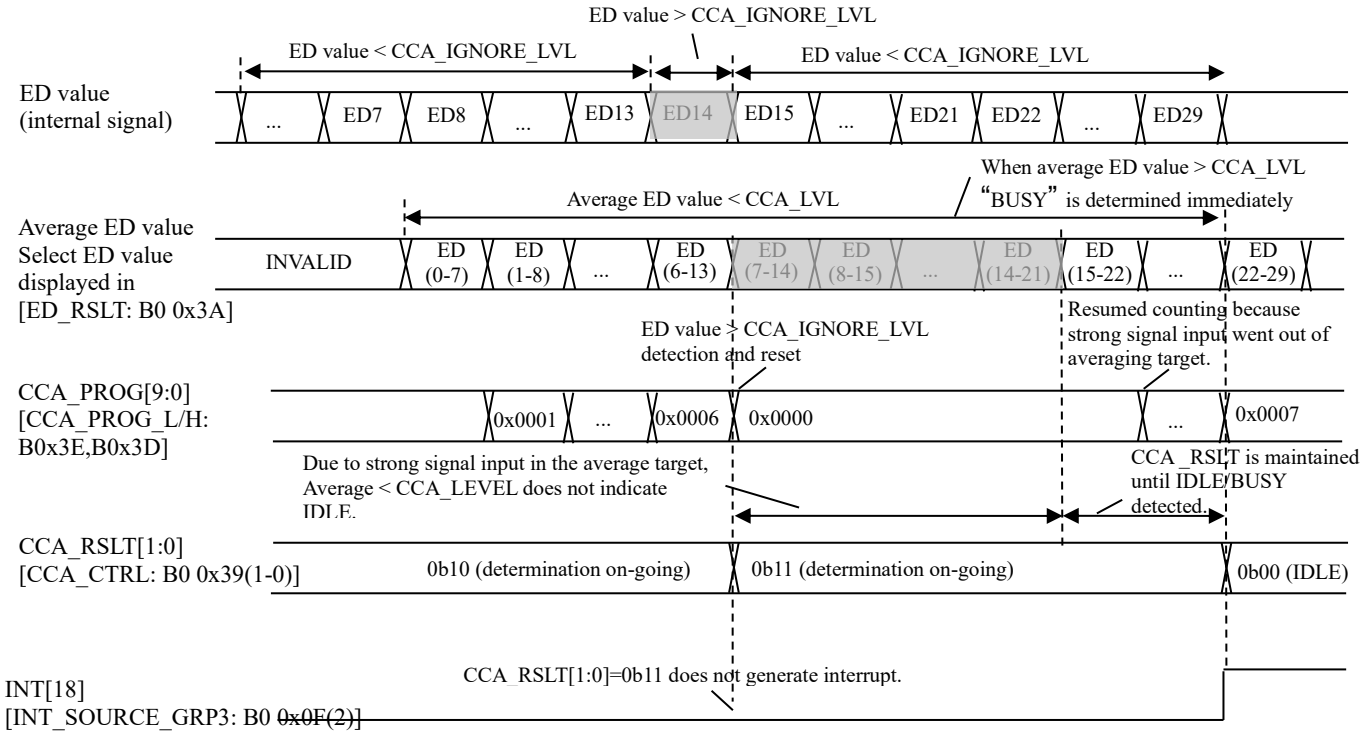
[ED value acquisition under strong signal input]



The following is the timing diagram when ED value under strong signal input was acquired.

[During IDLE_WAIT counting, detected strong signal input. After the given signal is out of averaging target, IDLE detection case]

[Condition]	
CCA mode	Normal mode
ED_AVG[2:0]=0b011 (ED value 8 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0]=0b00_0000_0111 (IDLE detection time 112 μs)	[IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]



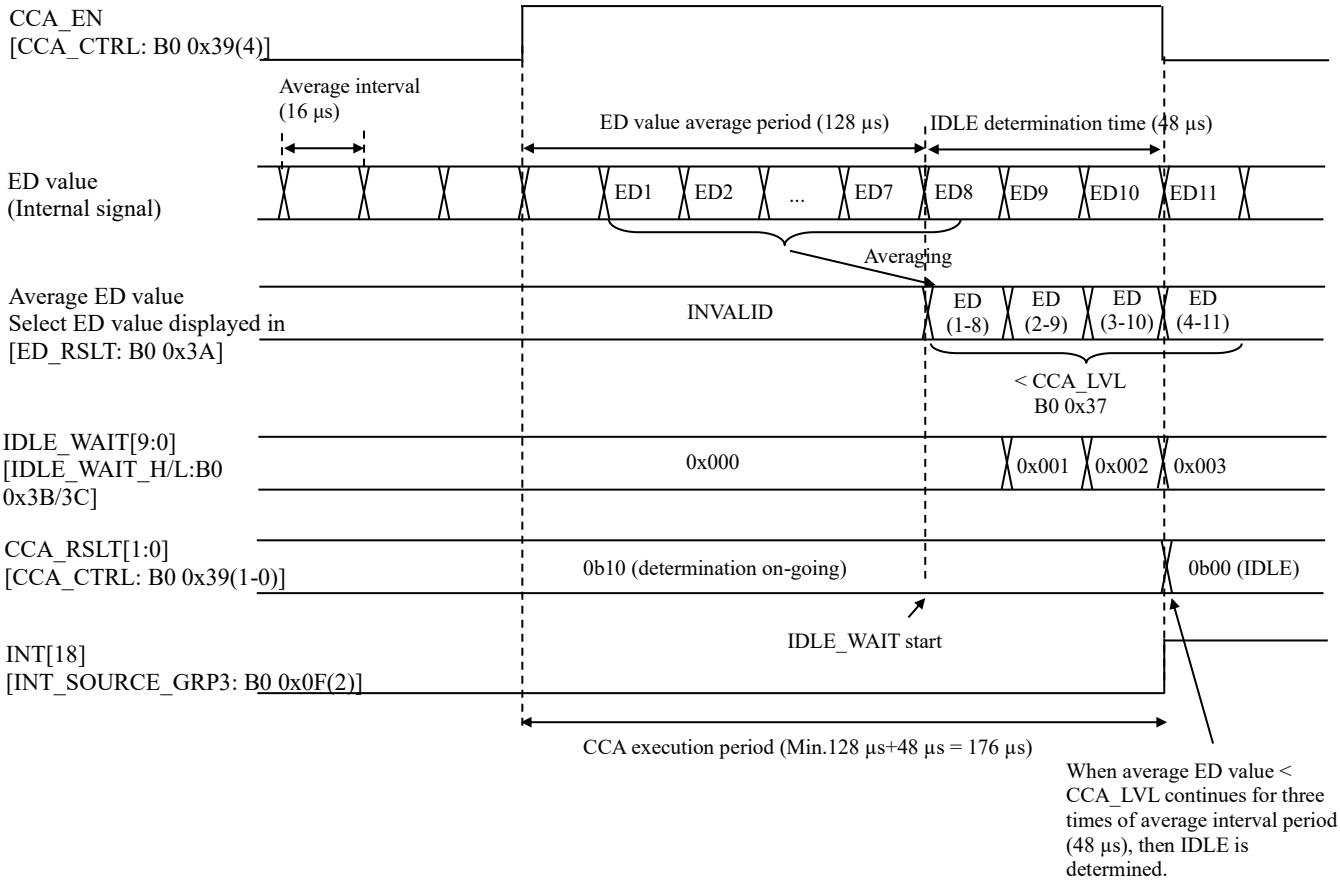
(5) IDLE detection for long time period

To perform CCA IDLE detection for a long time, it can be set by IDLE_WAIT [9:0] of [IDLE_WAIT_L:B0 0x3C] and [IDLE_WAIT_H: B0 0x3B(1-0)].
Using IDLE_WAIT [9:0] of [IDLE_WAIT_L:B0 0x3C] and [IDLE_WAIT_H: B0 0x3B(1-0)], it is possible to detect IDLE longer than the average period (128 µs for eight times of averaging process with 16 µs average interval). This function counts how many times the state where the moving average of ED value becomes equal to or smaller than [CCA_LVL: B0 0x37] is continued, and it makes IDLE determination when the count reaches or exceeds IDLE_WAIT [9:0]. Even when this function is used, when the moving average of ED value exceeds [CCA_LVL: B0 0x37], BUSY is determined immediately without waiting for the duration of time set by IDLE_WAIT [9:0].

The following timing diagram is IDLE detection setting IDLE_WAIT[9:0].

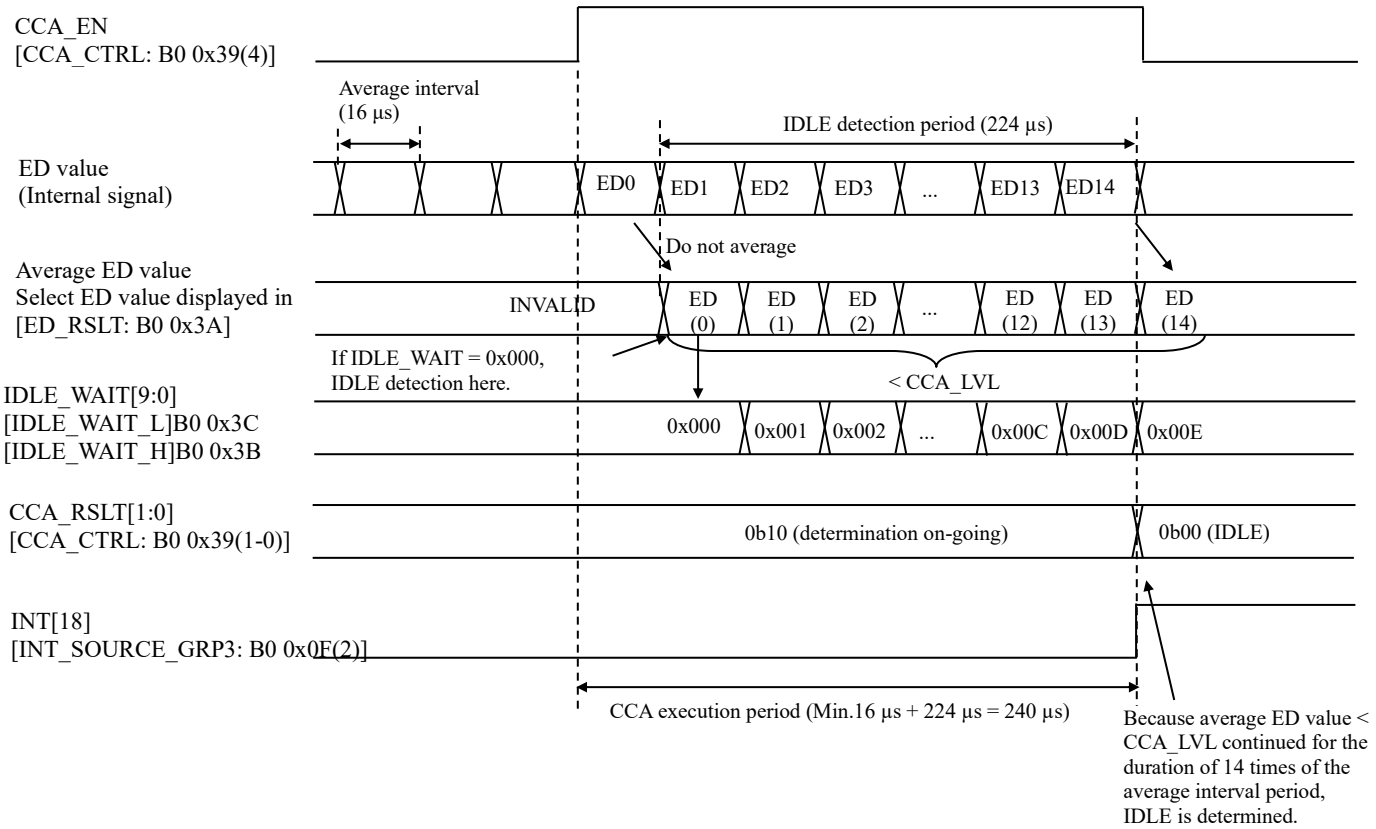
[ED value 8 times average IDLE detection case]

[Condition]	
CCA mode	Normal mode
ED_AVG[2:0]=0b011 (ED value 8 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0] = 0b00_0000_0011 (IDLE detection time 48 µs)	[IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]



[ED value single average IDLE detection case]

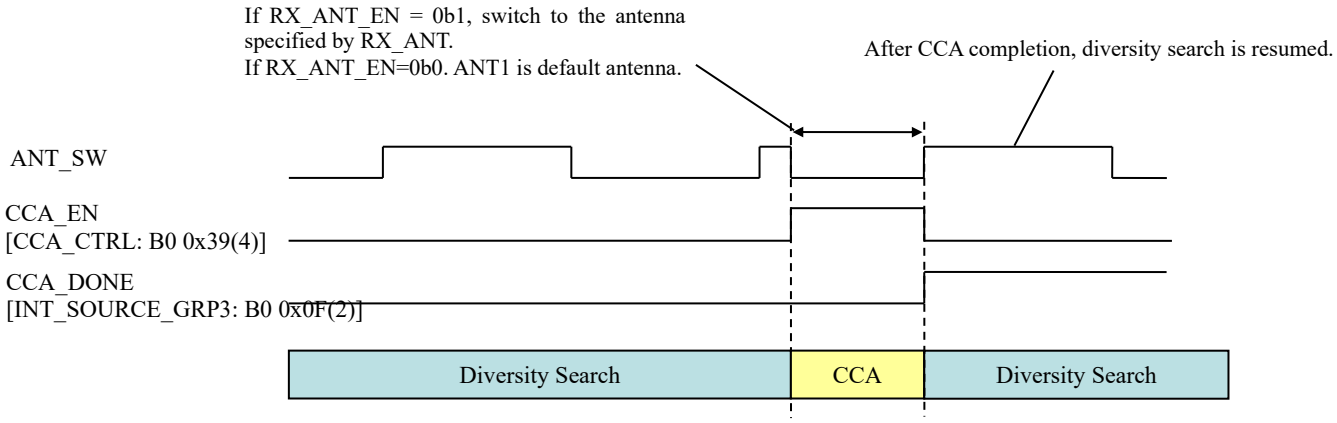
[Condition]	
CCA mode	Normal mode
ED_AVG[2:0]=0b000 (ED value 1 times average)	[ED_CTRL: B0 0x41(2-0)]
IDLE_WAIT[9:0] = 0b00_0000_1110 (IDLE detection time 224 µs)	[IDLE_WAIT_L: B0 0x3C], [IDLE_WAIT_H: B0 0x3B(1-0)]



(6) CCA operation during diversity

(a) CCA operation during diversity search

During diversity search, if CCA command is issued, diversity search will be terminated and CCA will start.
Upon CCA starting, antenna is fixed to the reset value (*1), and is maintained until the next diversity search is conducted. However, if antenna specification function ([ANT_CTRL: B0 0x4C(5-4)]) is enabled, it is fixed to the antenna which was specified by the register function. After CCA completion, diversity search will be resumed.
*1: The setting is described in the upper most section of "RX" of each table in "Function Description Diversity Function ANT_SW/TRX_SW Setting".

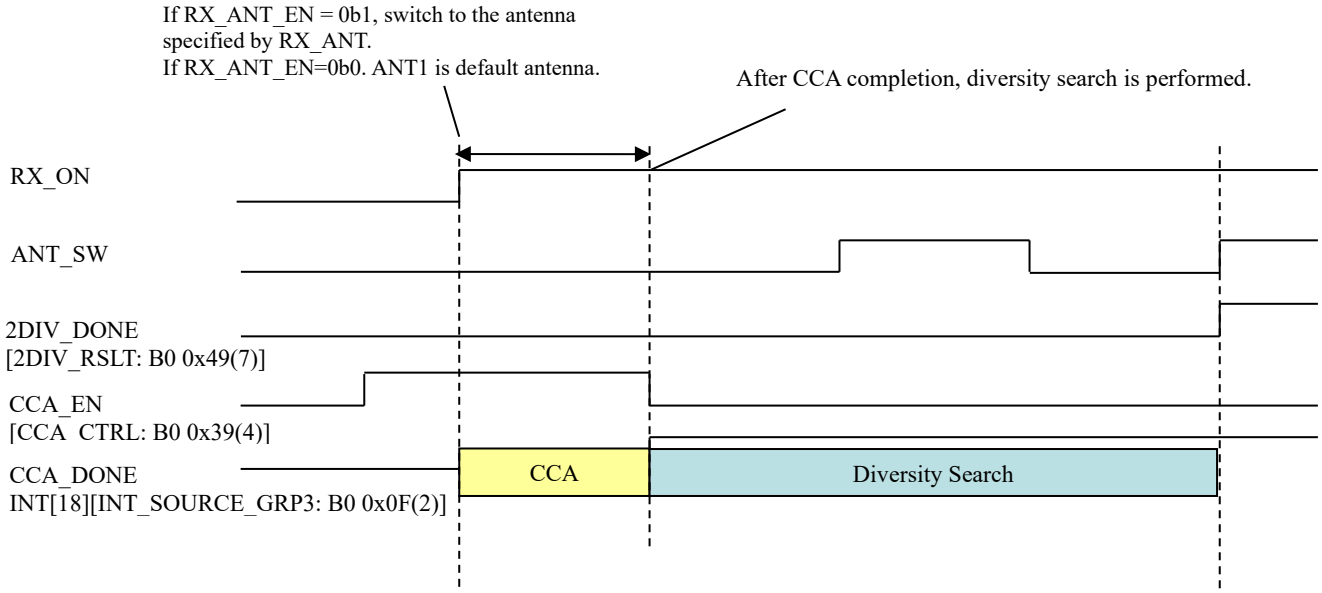


[Note]
During CCA operation, RX operation is performed at the same time. Even if CCA completion interrupt is not generated, SyncWord detection interrupt ([INT_SOURCE_GRP2: B0 0x0E(5)]), FIFO-Full trigger interrupt ([INT_SOURCE_GRP1: B0 0x0D(5)]), RX completion interrupt ([INT_SOURCE_GRP3: B0 0x0E(0)]), and CRC detection error interrupt ([INT_SOURCE_GRP3: B0 0x0E(1)]) may be generated.

For details of diversity function, please refer to "Diversity Function".

(b) Operation when CCA is executed before RX_ON during diversity ON

If diversity ON setting and CCA operation setting are enabled before RX_ON state, CCA will start without the diversity search operation after RX_ON state transition. After CCA completion, diversity search will be performed.



(7) CCA threshold setting

CCA threshold value, defined by [CCA_LVL: B0 0x37] register, should be set by considering the desired input level (ED value), variations (IC components variation, temperature fluctuation), and other losses (antenna, matching circuits, etc.). Relationship between input level and ED value are described in the following formula.

[2.4 k/4.8 kbps]
ED value = 255/80 * (120 + Input level [dBm] - Variation - Other loss)

In order to validate whether CCA threshold is optimized or not, CCA should be executed to confirm the level changing from IDLE to BUSY, every time input level is changed.

●TX Related Function

○Ramp Control Function

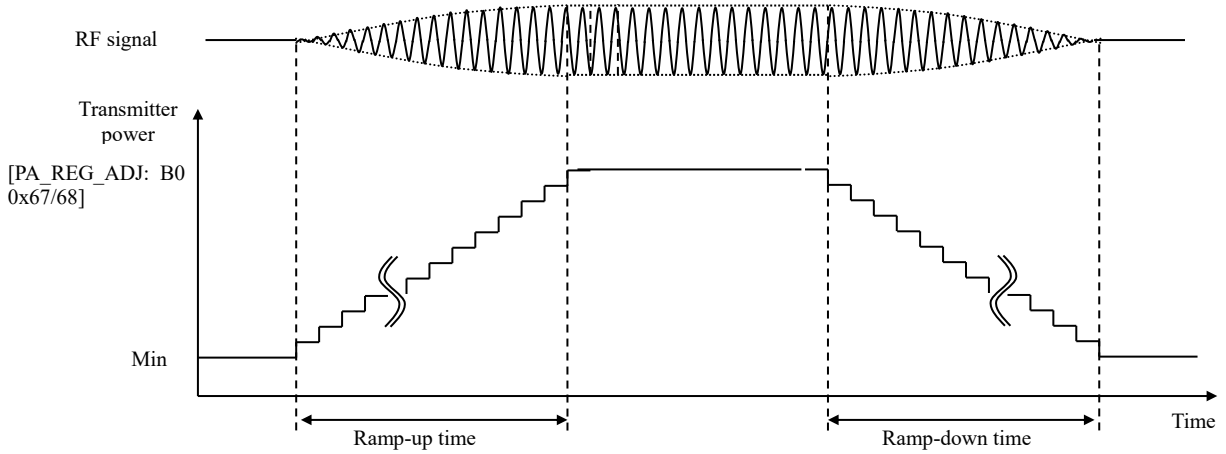
Ramp control function reduces the spurious emissions at the time of transmission startup and stop time.
Ramp control can be performed by the following registers.

Setting	Register
Ramp control counter increment setting	RAMP_INC([RAMP_CTRL1: B3 0x41(1-0)])
Ramp control reference clock cycle setting	RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])
Ramp-up time setting	RAMP_CLK_SET_R([RAMP_CTRL2: B3 0x42])
Ramp-down time setting	RAMP_CLK_SET_F([RAMP_CTRL3: B3 0x43])

Ramp-up time and ramp-down time can be calculated by the following formulas.

Ramp-up time [s] = Ramp control reference clock cycle setting (RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])) *
Ramp-up time setting (RAMP_CLK_SET_R[6:0]([RAMP_CTRL2: B3 0x42(6-0)]))} *
Maximum amplitude setting (PA_REG_ADJ[8:0]([PA_REG_ADJ_H: B0 0x67(0), PA_REG_ADJ_L: B0 0x68(7-0)])) /
Ramp control counter increment setting (RAMP_INC[1:0]([RAMP_CTRL1: B3 0x41(1-0)]))

Ramp-down time [s] = Ramp control reference clock cycle setting (RAMP_CLK_STEP([RAMP_CTRL1: B3 0x41(2)])) *
Ramp-down time setting (RAMP_CLK_SET_F[6:0]([RAMP_CTRL3: B3 0x43(6-0)]))} *
Maximum amplitude setting (PA_REG_ADJ[8:0]([PA_REG_ADJ_H: B0 0x67(0), PA_REG_ADJ_L:B0 0x68(7-0)])) /
Ramp control counter increment setting (RAMP_INC[1:0]([RAMP_CTRL1: B3 0x41(1-0)]))



In the reset, maximum setting or Sigfox setting state (PA output power + 13 dBm), the ramp-up and -down times (example) will be as follows:

Setting register	Reset state (min.)	Sigfox setting	Maximum setting
RAMP_INC[1:0] ([RAMP_CTRL1: B3 0x41(1-0)])	0x0	0x0	0x0
RAMP_CLK_STEP ([RAMP_CTRL1: B3 0x41(2)])	0x0	0x1	0x1
RAMP_CLK_SET_R[6:0] ([RAMP_CTRL2: B3 0x42(6-0)])	0x01	0x3F	0x7F
RAMP_CLK_SET_F[6:0] ([RAMP_CTRL3: B3 0x43(6-0)])	0x01	0x3F	0x7F
PA_REG_ADJ[8:0]([PA_REG_ADJ_H: B0 0x67(0), PA_REG_ADJ_L:B0 0x68(7-0)])	0x0E4	0x0E4	0x0E4
Ramp-up/down time	17.7us	17.8ms	25.7ms

●Other Functions

○Data Rate Setting Function

(1) Data rate change setting

ML7456N RF part supports various TX/RX data rate setting defined by the following registers.

TX ... [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03]

RX ... [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05] and [RX_RATE2: B1 0x06]

TX/RX data rate can be defined in the following formula.

[TX]

TX data rate [bps] = round (Master clock frequency [Hz] / 10/ [TX_RATE])

The following table shows the recommended value for each data rate. By setting TX_DRATE([DRATE_SET: B0 0x06(3-0)], following register setting values are automatically set to [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03].

TX data rate [kbps]	[TX_RATE_H][TX_RATE_L] setting value (decimal)	Data rate deviation [%] *1
1.2	3000	0.00
2.4	1500	0.00
4.8	750	0.00
9.6	375	0.00
10.0	360	0.00
19.2	188	-0.27
15.0	240	0.00
32.768	110	-0.12
50	72	0.00
100	36	0.00

*1 Data rate deviation is assumption that frequency deviation of master clock is 0ppm.

If the data rate deviation becomes large by using the transmission data rate calculated by the formula above, the data rate deviation can be reduced by using [TX_RATE2_H: B1 0x7C] and [TX_RATE2_L: B1 0x7D].

TX_RATE2[13:0] = round [[{1/data rate (bps)} –
{1 / (Master clock frequency (Hz) / TX_RATE[11:0]) x 9}] /
{1 / Master clock frequency (Hz)}]

[RX]

RX data rate [bps] = round ({Master clock frequency [Hz] / N} / {[RX_RATE1] * [RX_RATE2]})
*** When N=1(LOW_RATE_EN=0b0)**
When N=2(LOW_RATE_EN=0b1)

The following table shows the recommended value for each data rate (when LOW_RATE_EN([CLK_SET2: B0 0x03(0)])=0b1 is set). By setting RX_DRATE([DRATE_SET: B0 0x06(7-4)]), following register setting values are automatically set to [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05], and [RX_RATE2: B1 0x06].

RX data rate [kbps]	[RX_RATE1_H][RX_RATE1_L] setting value (decimal)	[RX_RATE2] setting value (decimal)
1.2	120	125
2.4	60	125
4.8	30	125
9.6	15	125
10.0	15	120
19.2	8	117
15.0	12	100
20	9	100
32.768	5	110
40	5	90
50	3	120
100	2	90

[Note]
1. When LOW_RATE_EN([CLK_SET2: B0 0x03(0)])=0b0 is set, the RX data rate should be calculated by the formula above. It should be noted that when LOW_RATE_EN=0b0 is set, even if TX/RX data rate setting register ([DRATE_SET: B0 0x06]) is set, the optimum values are not set to [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05], and [RX_RATE2: B1 0x06] automatically.

(2) Other register settings associate with data rate change

When the data rate is changed, registers should be changed according to the Initialization table.

[Note]
1. Please change data rate setting in TRX_OFF state.

○Interrupt Generation Function

This LSI supports interrupt generation function. When interrupt occurs, interrupt notification signal (SINTN) becomes “L” to notify interrupt to the host MCU. Interrupt events are categorized into three groups: [INT_SOURCE_GRP1: B0 0x0D], and [INT_SOURCE_GRP2: B0 0x0E], and [INT_SOURCE_GRP3: B0 0x0F]. Each interrupt event can be masked by [INT_EN_GRP1: B0 0x10], and [INT_EN_GRP2: B0 0x11], and [INT_EN_GRP3: B0 0x12]. Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin. For output settings, refer to [GPIO1_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51] and [EXTCLK_CTRL: B0 0x52].

[Note]
If any single unmasked interrupt event occurs, SINTN maintains Low.

(1) Interrupt events table

Each interrupt event is described below table.

Register	Interrupt name	Function
INT_SOURCE_GRP1	INT[0]	Clock stabilization completion interrupt
	INT[1]	VCO calibration completion interrupt or Fuse access completion interrupt or IQ adjustment completion interrupt
	INT[2]	PLL unlock interrupt/ Out of VCO adjusting voltage range detected interrupt
	INT[3]	RF state transition completion interrupt
	INT[4]	FIFO-Empty interrupt
	INT[5]	FIFO-Full interrupt
	INT[6]	Wake-up timer completion interrupt
	INT[7]	Clock calibration completion interrupt
INT_SOURCE_GRP2	INT[8]	RX completion interrupt
	INT[9]	CRC error interrupt
	INT[10]	Diversity search completion interrupt
	INT[11]	RX Length error interrupt
	INT[12]	Reserved
	INT[13]	SyncWord detection interrupt
	INT[14]	Field checking interrupt
	INT[15]	Sync error interrupt
INT_SOURCE_GRP3	INT[16]	TX completion interrupt
	INT[17]	TX Data request accept completion interrupt
	INT[18]	CCA completion interrupt
	INT[19]	TX Length error interrupt
	INT[20]	TX FIFO access error interrupt
	INT[21]	Reserved
	INT[22]	General purpose timer 1 interrupt
	INT[23]	General purpose timer 2 interrupt

(2) Interrupt generation timing

In each interrupt generation, timing from reference point to interrupt generation (notification) is described in the following table. Timeout procedure for interrupt notification waiting is also described below.

[Note]
(1) The following table shows values at 100 kbps. For any symbol rate, replace the value described as symbol time with the symbol period in the following table.
(2) The following table uses the following format for TX/RX data.

10 byte	2 byte	1 byte	24 byte	2 byte
Preamble	SyncWord	Length	User data	CRC

(3) Even when an interrupt notification is set to OFF, ML7456N RF part internally holds the interrupt. When the interrupt notification setting is then changed from OFF to ON without clearing the interrupt, it will be notified. When the interrupt occurs, it is recommended that interrupt should be cleared after turning off the interrupt notification.

Interrupt notification			Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[0]	Clock stabilization completion	In case of crystal oscillator circuits	RESETN release (upon power-up)	300 to 500 µs
			Exit from SLEEP (recovered from SLEEP)	300 to 500 µs
		TCXO used	TCXO_EN setting (upon power-up)	10 to 500 µs
			Exit from SLEEP (recovered from SLEEP)	10 to 500 µs
INT[1]	VCO calibration completed		VCO calibration start	9ms
INT[2]	PLL unlock detection		-	(TX) during TX after PA_ON (RX) during RX after RX enable.
	Out of VCO adjusting voltage range detected		-	(TX) PA_ON rise (RX) RX enable rise
INT[3]	RF state transition completion		TX_ON command	(IDLE) 143 µs (RX) 24 µs
			RX_ON command	(At IDLE) 118µs (TX) 25µs
			TRX_OFF command	(TX) 24µs (RX) 5 µs
			Force_TRX_OFF command	(TX) 24µs (RX) 5 µs
INT[4]	FIFO-EMPTY		TX_ON command (TX) (*1)	Empty trigger level is set to 0x02. (NRZ encoding) RF wake-up (210 µs)+(preamble to 22nd Data byte)x10(bit time) = 3010 µs)
			-(RX)	By FIFO read, FIFO usage is under trigger level
INT[5]	FIFO-FULL		-(TX)	By FIFO write, FIFO usage exceed trigger level
			SyncWord detection (RX)	Full trigger level is set to 0x05. (NRZ encoding) 500 µs (5-byte data x 10 µs (bit time))
INT[6]	Wake-up timer completion		SLEEP setting	Wake-up timer is completed. For details, please refer to the “Wake-up timer”.
INT[7]	Clock calibration completion		Calibration start	Calibration timer is completed. For details, please refer to ““Low Speed Clock Shift Detection Function””.
INT[8]	Data reception completion		SyncWord detection	When the length of L-field is 1 byte, and NRZ encoding is used, after 2160 µs (L-field length (8 bit)x10(symbol time)=80 µs, data length ((Data to CRC: bit)x10(symbol time)=2080 µs))
INT[9]	CRC error		SyncWord detection	(Format A/B) each RX CRC block calculation completion (Format C) RX completion
INT[10]	Diversity search completion		-	SyncWord detection during diversity enable setting

Interrupt notification		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[11]	RX Length error	SyncWord detection	80 μs(L-field 1 byte) 160 μs(L-field 2 byte)
INT[12]	Reserved	-	-
INT[13]	SyncWord detection	-	SyncWord detection
INT[14]	Field check	-	Match or mismatch detected in Field check
INT[15]	Sync error	-	During RX after SyncWord detection, out-of-sync detected. (When RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)]) is set to 0b00 or 0b11)
INT[16]	Data transmission completion	TX_ON command (*1)	RF wake-up+[TX data+3](bit) =210μs+315 bit x 10μs (bit time)=3360μs
INT[17]	TX Data request accept completion	-	After full length data is written to the TX_FIFO. (It is considered as transmitting when using FIFO trigger to write additional data in FAST_TX mode)
INT[18]	CCA completion	CCA execution start	(1)Normal mode (ED value average times + IDLE_WAIT setting) x Average period (2) IDLE detection mode ○ IDLE detection (ED value average times + IDLE_WAIT setting) x Average period ○ BUSY detection ED value average times x Average interval Average interval is 16 μs.
INT[19]	TX Length error	-	When setting Length for [TX_PKT_LEN_H/L: B0 0x7A/0x7B]
INT[20]	TX FIFO access error	-	(1) When data was written when there was no free space on FIFO (2) When additional data was written to FIFO, overflow occurred (3) When there was no more data to transmit during transmission
INT[21]	Reserved	-	-
INT[22]	General purpose timer 1	Timer start	General purpose timer 1 completion General purpose timer clock cycle * Division setting [GT_CLK_SET: B0 0x33] * B0 0x33]) * After general purpose timer interval setting ([GT1_TIMER: B0 0x34])
INT[23]	General purpose timer 2 completion	Timer start	General purpose timer 2 completion General purpose timer clock cycle * Division setting [GT_CLK_SET: B0 0x33] * B0 0x33]) * After general purpose timer interval setting ([GT2_TIMER: B0 0x35])

(*1) Before issuing TX_ON, writing full-length TX data to the TX_FIFO.

(2) Clearing interrupt conditions

Interrupt notification		Recommended clearing timing for interrupts
INT[0]	CLK stabilization completion	
INT[1]	VCO calibration completion Out of VCO adjusting voltage range detected	
INT[2]	PLL unlock detection	
INT[3]	RF state transition completion	
INT[4]	FIFO-EMPTY	Clear before the next EMPTY trigger generation timing
INT[5]	FIFO-FULL	Clear before the next FULL trigger generation timing
INT[6]	Wake-up timer completion	
INT[7]	Clock calibration	
INT[8]	Data reception completion	Clear before the next packet reception
INT[9]	CRC error	Clear before the next packet reception
INT[10]	Diversity search completion	After interrupt generated
INT[11]	RX Length error	
INT[12]	Reserved	
INT[13]	SyncWord detection	
INT[14]	Field check	
INT[15]	Sync error	
INT[16/]	Data transmission completion	Clear before the next packet transmission
INT[17]	TX Data request accept completion	Clear before the next packet reception
INT[18]	CCA completion	Clear before the next CCA execution (Note) clearing interrupt erase CCA result as well.
INT[19]	TX Length error	
INT[20]	TX FIFO access error	Clear before the next packet transmission
INT[21]	Reserved	
INT[22]	General purpose timer 1	
INT[23]	General purpose timer 2 completion	

○Low Speed Clock Shift Detection Function

This LSI has low speed shift detection function to compensate inaccurate clock generated by RC oscillator (external clock or internal RC oscillation circuits). By detecting frequency shift of the wake up timer, host can set wake-up timer parameters which taking frequency shift into consideration. More accurate timer operation is possible by considering the offset of wake-up timer clock frequency detected by this function and adjusting the wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) or continuous operation timer interval setting ([WU_DURATION: B0 0x31]).

Setting	Register
Frequency shift detection clock frequency setting	[CLK_CAL_SET: B0 0x70]
Calibration time	[CLK_CAL_TIME: B0 0x71]
Clock calibration result value	[CLK_CAL_H: B0 0x72] and [CLK_CAL_L: B0 0x73]

This function counts the low speed clock cycle for wake-up timer using the accurate and high speed internal clock, and the count result is displayed in the [CLK_CAL_H/L: B0 0x72/0x73] register. Above setting and count numbers are as follows:

High speed clock counter = {Wakeup timer clock cycle[SLEEP/WU_SET:B0 0x2D(2)] *
Clock calibration time setting ([CLK_CAL_TIME:B0 0x71(5-0)]) /
{Master clock cycle (36 MHz) / Clock division setting ([CLK_CAL_SET: B0 0x70(7-4)])}

Clock calibration time is as follows:

Clock calibration time[sec] = Wakeup timer clock cycle * Clock calibration time setting

[Wake-up timer correction example]
Assuming no division in the internal high speed clock, calibration time set to 10 cycles, wake-up timer set to 1000(0x3E8)
Condition: Wake-up timer clock frequency = 32.768 kHz
Detection clock division setting CLK_CAL_DIV[3:0] ([CLK_CAL_SET: B0 0x70(7-4)])= 0b0000
Calibration time setting [CLK_CAL_TIME] = 0x0A
Wake-up timer setting [WUT_INTERVAL:B0 0x2F,30] = 0x03E8(1000)

Ideal high speed clock count is as follows:

High speed clock count = (1/32.768 kHz) * 10 / (1/36 MHz)
= 10986(0x2AEA)

If getting [CLK_CAL_H/L:B0 0x72,73] = 0x2A03 (10755)
Counter difference = 10755 - 10986 = -231
Frequency shift = 1/[{1/32.768 kHz + (-231) / 10 * 1/36 MHz}] - 32.768 kHz = 703.78 Hz
Then finding wake-up timer clock frequency accuracy is +2.18% higher. And the compensation vale (C) is calculated as below:

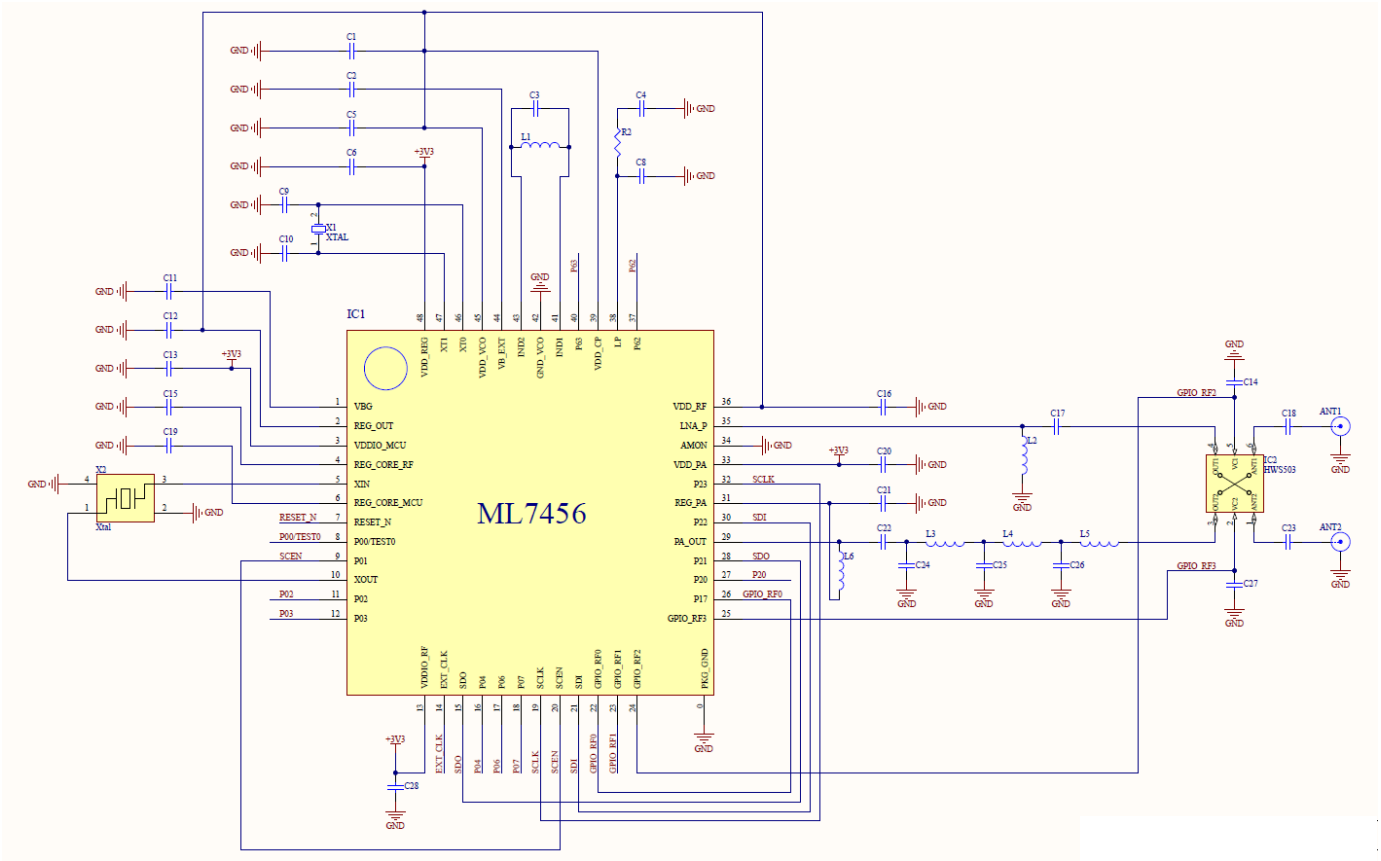
C= Wake-up timer interval([WUT_INTERVAL_H/L:B0 0x2F,30]) * frequency shift / 32.768
= 1000 * 703.78Hz / 32.768kHz
= 21

Therefore, setting wale-up timer setting value = 1000 +21 = 1021 = 0x03FD enables to achieve more accurate timer interval timing that was supposed to be set at 32.768 kHz.

[Note]

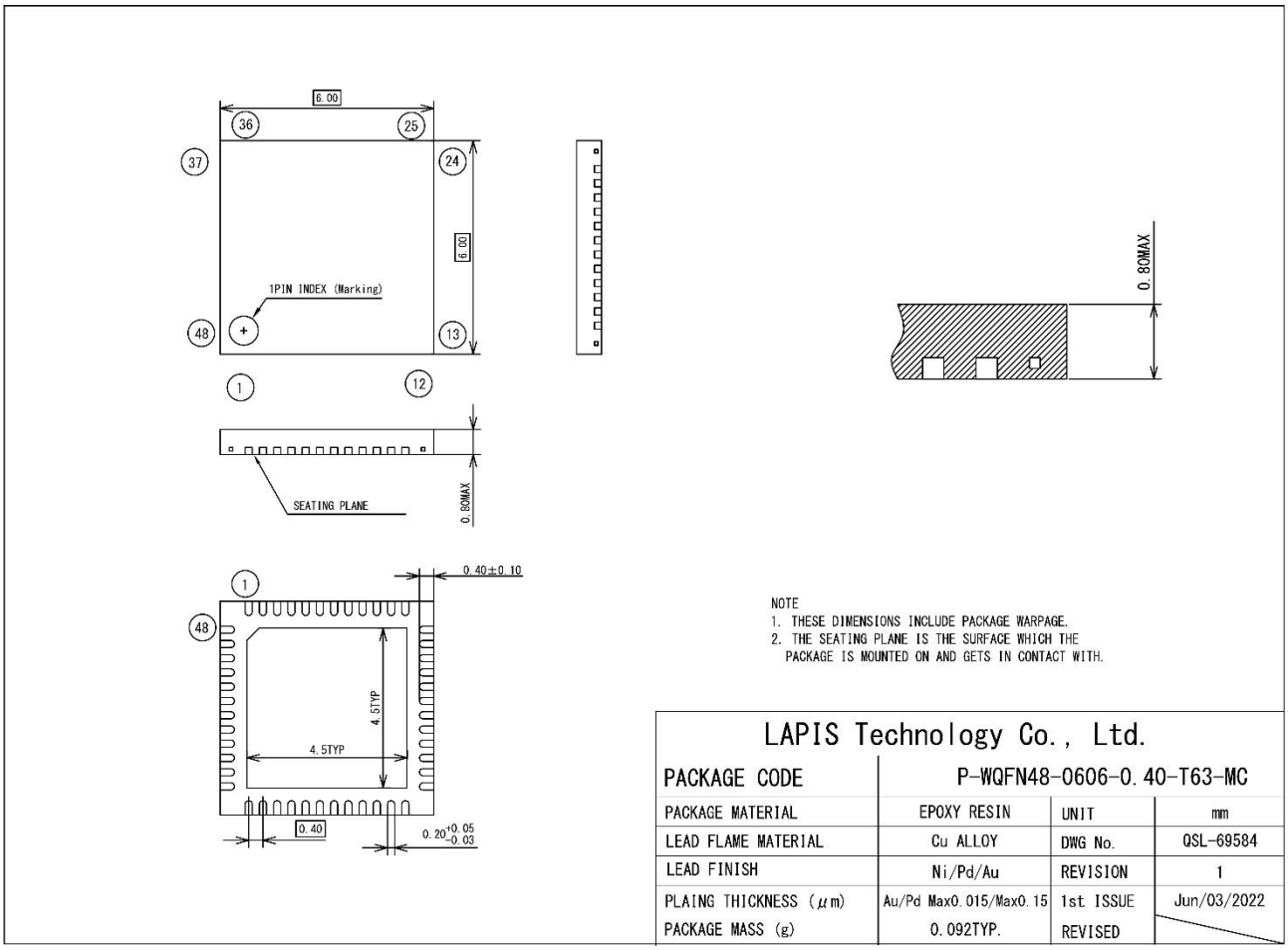
1. If calibration time is too short or if high speed counter is divided into low speed clock, calibration may not be accurate.
2. When the master clock is 36 MHz, setting [CLK_CAL_TIME: B0 0x71] = 0x3F exceeds the upper limit of clock calibration result display value ([CLK_CAL_H/L: B0 0x72/73]). Set a value of 0x3E or smaller.

■Application Circuits Example



Please refer to the Design Guide in details.

■Package Dimensions



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN48-0606-0.40-T63-MC		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69584
LEAD FINISH	Ni/Pd/Au	REVISION	1
PLAING THICKNESS (μm)	Au/Pd Max0.015/Max0.15	1st ISSUE	Jun/03/2022
PACKAGE MASS (g)	0.092TYP.	REVISED	

Remarks for surface mount type package

The surface mount type package is very sensitive to heat generated in the reflow process, moisture absorption during storage, etc. Therefore, when considering the reflow mounting process, please contact our sales office about the product name, package name, number of pins, package code, desired mounting conditions (reflow method, temperature, number of processes), storage conditions, etc.

■Revision History

Document No.	Release date	Page		Revision description
		Before revision	After revision	
FEDL7456N-01	2022.07.04	-	-	Initial release
FEDL7456N-02	2022.09.12	46	46	[Electrical Characteristics]-[RF]-[RF Characteristics] modified sensitivity
FEDL7456N-03	2022.10.26	5	5	[Features] modified channel number of Functional timer and 16bit General timers
		7	7	[Features] modified RX currnet cunsumption
		40	40	[Electrical Characteristics]-[MCU]-[Analog Comparator Characteristics] changed condition of input offset
		41	41	[Electrical Characteristics]-[MCU]-[Successive Approximation Type A/D Converter] modified condition
		43	43	[Electrical Characteristics]-[RF]-[Power Consumption] modified RX state
FEDL7456N-04	2023.11.1	1	1	Add application
		1	1	Add Product Name
		218	218	The description of [Note] has been updated.
FEDL7456N-05	2024.1.10	218	218	The description of [Note] has been updated.

(Note) Changes and corrections of writing errors/expressions are not included.

Notes

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