Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML86V7675

Digital Video Decoder

General Description

The ML86V7675 is a digital video decoder LSI that converts NTSC, PAL analog video signals, 480i/576i/480p/576p analog video signals, analog EGA(400 x 234, 480 x 234), analog RGB WVGA(800 x 480) signals into the YCbCr standard digital format defined by ITU-R recommendations BT.601/BT.656.
The device has built-in 10-bit A/D converters and can accept only composite video signal, S-video signal, or Component video signal as an analog input.
An input composite video signal is separated into a luminance signal and a chrominance signal with a 2-dimensional Y/C separation filter. These two signals are then output as digital video signals.
In addition to the asynchronous sampling method, which is a special feature of LAPIS Semiconductor's video decoders, video signals can also be sampled with a line lock clock sampling method using the built-in PLL.
Further, the pixel position compensation function provided makes it possible to eliminate video jitter even with the asynchronous sampling method, ensuring the output of jitter-free video data.

Features

- Analog video input - input format
  - Composite video : NTSC/PAL/SECAM (ITU-R BT.470)
  - S vide : NTSC/PAL/SECAM (ITU-R BT.470)
  - Component video input : (YPbPr/RGB) 480i/576i/480p/576p, EGA, WVGA (Sync on Y/G. CSYNC input supported only at RGB input)
- Analog input port : Composite video input 4ch; Component video input (YPbPr/RGB) 1ch; Component video input (YPbPr/RGB) or S video input 1ch
- A/D converter : 10bit ADC
- Supported sampling frequency
  - NTSC/ PAL/ SECAM : (ITU-R BT.601) 27.0000MHz
  - NTSC 28.6363 MHz
  - D1 (480i/576i) : 27.0000 MHz
  - D2 (480p/576p) : 27.0000 MHz
  - EGA (400×234) : 7.993006 MHz
  - EGA (480×234) : 9.582167 MHz
  - WVGA (800×480) : 33.231, 33.333MHz
- Sampling method : Asynchronous sampling method / Line lock clock sampling method
- Y/C separation : Adaptive two-dimensional Y/C separation filter
- Luminance level adjustment : AGC (automatic luminance adjustment) / MGC (manual luminance adjustment) / Peak AGC
- Color level adjustment : ACC (automatic color adjustment) / MCC (manual color adjustment)
- Contrast adjustment: Adjustable around 128 with a slope ranging from 1/32 to 63/32
- Luminance offset adjustment : Adjustable between -7IRE to 7IRE(except analog RGB inputs), -128LSB to 127LSB
- Contour correction: Emphasizes higher frequencies
- Hue adjustment: Adjustable between -178.6° to 180°(NTSC,PAL only), -45° to 44.6°

ROHM SEMICONDUCTOR

● Automatic judgment of input video signal method :	NTSC / PAL / SECAM automatic recognition	
● VBI data detection :	Closed caption	Supports only NTSC (480i)
	CGMS	Supports only NTSC (480i, 480p)
	WSS	Supports only PAL (576i)
● Output format :	YCbCr 4:2:2 (8bit duplex data + sync signal), ITU-R BT.656 (YCbCr 4:2:2 8-bit multiplexed data including synchronization information) SDR, DDR output selectable	
● Host interface :	I^2C (Slave) Slave address selectable from 80h (1000_000x) or 82h (1000_001x).	
● Clock Sampling clock :	Line lock PLL method An external crystal oscillator (32.00 MHz or 25.00MHz) is attached as a reference clock	
● Power supply voltage :	I/O	3.3V ± 0.3V
	Analog section (AFE / ADC)	3.3V ± 0.3V
	Analog section (PLL)	1.5V ± 0.15V
	Logic section	1.5V ± 0.15V
● Operating frequency :	Maximum input 28.63MHz, maximum output 57.26MHz	
● Operating temperature (ambient temperature) :	-40°C to +85°C	
● Package :	64 pin plastic TQFP	

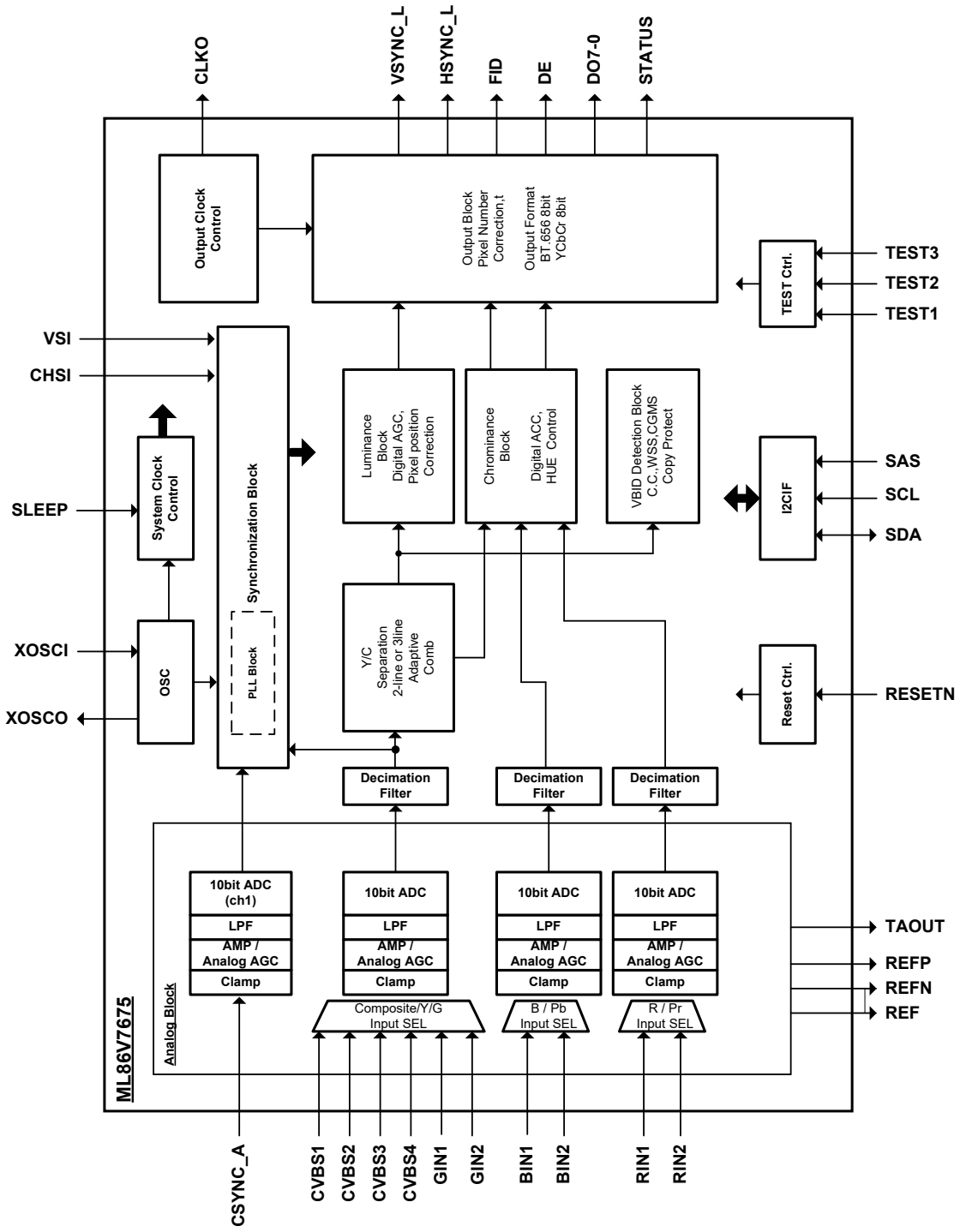
Application

- Car navigation
- Display audio
- RSE (Rear Seat Entertainment)

Line up

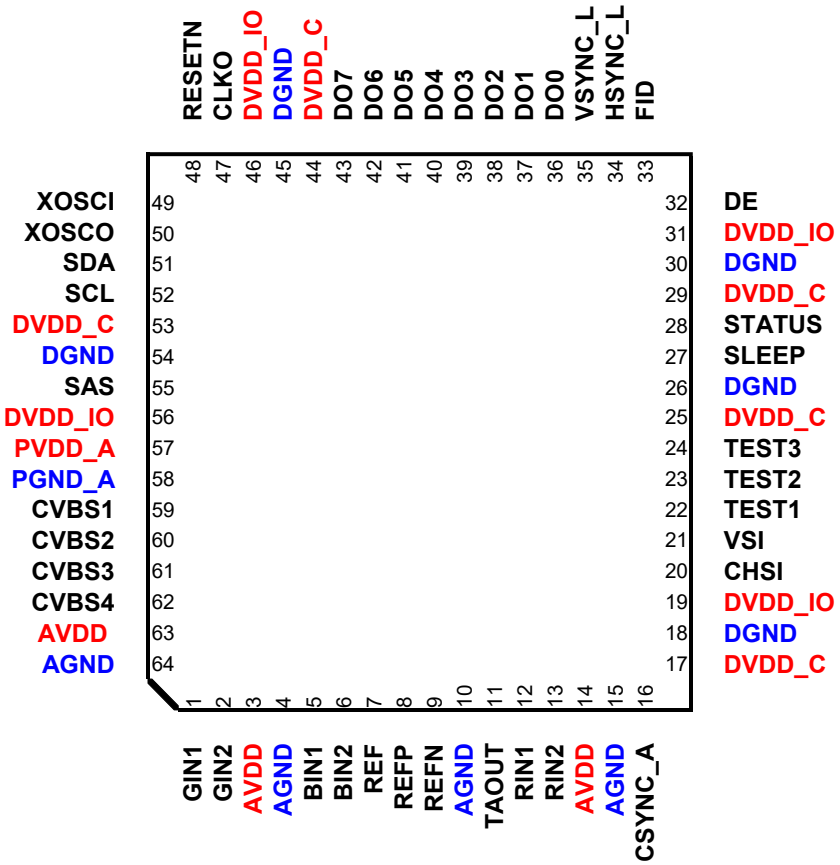
Part Number	Shipping form
ML86V7675TPZ0AX	Tray

Block Diagram



Pin Connections (Top View)

64-pin Plastic TQFP, Cu Lead
(P-TQFP64-1010-0.50)



Note: Apply the same power supply voltage to the power supply pins of the same pin name.
Fix the unused input pins to the “L” level or the “H” level.
However, if the unused input pin is a pull-up resistor pin, fix it to the “H” level, and if it is a pull-down pin, fix it to the “L” level.

List of Pins

Pin number	Pin name	I/O	Type		Type
			Input	Output	
1	GIN1	I	Analog	—	Analog video input (G/Y)
2	GIN2	I	Analog	—	Analog video input (G/Y/SY)
3	AVDD	—	Power supply	—	Power supply for analog (3.3V)
4	AGND	—	Power supply	—	Ground for analog
5	BIN1	I	Analog	—	Analog video input (B/Pb)
6	BIN2	I	Analog	—	Analog video input (B/Pb/SC)
7	REF	O	—	Analog	Reference voltage for ADC (external grounding through 0.01uF)
8	REFP	O	—	Analog	Reference voltage for ADC (external grounding through 0.22uF)
9	REFN	O	—	Analog	Reference voltage for ADC (external grounding through 0.22uF)
10	AGND	—	Power supply	—	Ground for analog
11	TAOUT	O	—	Analog	Output for testing (open)
12	RIN1	I	Analog	—	Analog video input (R/Pr)
13	RIN2	I	Analog	—	Analog video input (R/Pr)
14	AVDD	—	Power supply	—	Power supply for analog (3.3V)
15	AGND	—	Power supply	—	Ground for analog
16	CSYNC_A	I	Analog	—	Analog composite synchronous input
17	DVDD_C	—	Power supply	—	Power supply for digital core (1.5V)
18	DGND	—	Power supply	—	Ground for digital
19	DVDD_IO	—	Power supply	—	Power supply for digital input/output (3.3V)
20	CHSI	I	LVTTL,ST 5V-tolerant	—	Digital composite synchronous input or Digital horizontal synchronous input (For analog RGB input)
21	VSI	I	LVTTL,ST 5V-tolerant	—	Digital vertical synchronous input (for analog RGB input)
22	TEST1	I	LVTTL,PD	—	Test mode selection
23	TEST2	I	LVTTL,PD	—	Test mode selection
24	TEST3	I	LVTTL,PD	—	Test mode selection
25	DVDD_C	—	Power supply	—	Power supply for digital core (1.5V)
26	DGND	—	Power supply	—	Ground for digital
27	SLEEP	I	LVTTL,PD	—	Sleep enable input
28	STATUS	O	—	4-mA drive	Status output
29	DVDD_C	—	Power supply	—	Power supply for digital core (1.5V)
30	DGND	—	Power supply	—	Ground for digital
31	DVDD_IO	—	Power supply	—	Power supply for digital input/output (3.3V)
32	DE	O	—	2-/4-mA drive	Data enable output

PD = pull-down. ST = Schmitt Trigger.
Note: The pull-up or pull-down resistance is 40kΩ.

Pin number	Pin name	I/O	Type		Type
			Input	Output	
33	FID	O	—	2-/4-mA drive	Field output
34	HSYNC_L	O	—	2-/4-mA drive	Vertical synchronous output
35	VSYNC_L	O	—	2-/4-mA drive	Horizontal synchronous output
36	DO0	O	—	2-/4-mA drive	Output data 0
37	DO1	O	—	2-/4-mA drive	Output data 1
38	DO2	O	—	2-/4-mA drive	Output data 2
39	DO3	O	—	2-/4-mA drive	Output data 3
40	DO4	O	—	2-/4-mA drive	Output data 4
41	DO5	O	—	2-/4-mA drive	Output data 5
42	DO6	O	—	2-/4-mA drive	Output data 6
43	DO7	O	—	2-/4-mA drive	Output data 7
44	DVDD_C	—	Power supply	—	Power supply for digital core (1.5V)
45	DGND	—	Power supply	—	Ground for digital
46	DVDD_IO	—	Power supply	—	Power supply for digital input/output (3.3V)
47	CLKO	O	—	2-/4-mA drive	Output clock
48	RESETN	I	LVTTL,ST	—	System reset input (active “L”)
49	XOSCI	I	LVTTL	—	Clock oscillation input (HPLL reference clock input)
50	XOSCO	O	—	6 mA drive	Clock oscillation output
51	SDA	I/O	LVTTL,ST	4 mA drive open-drain	I^2C bus serial data
52	SCL	I	LVTTL,ST	—	I^2C bus serial clock
53	DVDD_C	—	Power supply	—	Power supply for digital core (1.5V)
54	DGND	—	Power supply	—	Ground for digital
55	SAS	I	LVTTL,PD	—	I^2C bus slave address selection
56	DVDD_IO	—	Power supply	—	Power supply for digital input/output (3.3V)
57	PVDD_A	—	Power supply	—	Power supply for HPLL (1.5V)
58	PGND_A	—	Power supply	—	Ground for HPLL
59	CVBS1	I	Analog	—	Analog video input (CVBS)
60	CVBS2	I	Analog	—	Analog video input (CVBS)
61	CVBS3	I	Analog	—	Analog video input (CVBS)
62	CVBS4	I	Analog	—	Analog video input (CVBS)
63	AVDD	—	Power supply	—	Power supply for analog (3.3V)
64	AGND	—	Power supply	—	Ground for analog

PD = pull-down. ST = Schmitt Trigger.
Note: The pull-up or pull-down resistance is 40kΩ.

Pin Descriptions

Pin name	Primary function		Secondary function		Initial Status
	I/O	Description	I/O	Description	
Analog video input					
RIN1, GIN1, BIN1	I	Analog component video signal input 1 (RGB1) RIN1: For R/Pr GIN1: For G/Y BIN1: For B/Pb			
RIN2, GIN2, BIN2	I	Analog component video signal input 2 (RGB2) RIN2: For R/Pr GIN2: For G/Y BIN2: For B/Pb	I	Analog video S signal input BIN2: For SC GIN2: For SY	
CVBS1-4	I	Analog composite video signal input			
CSYNC_A	I	Analog composite sync input (for analog RGB input)			
CHSI	I	Digital composite sync input, digital horizontal synchronous input (For analog RGB input)			
VSI	I	Digital vertical synchronous input(For analog RGB input)			
REF	O	Reference voltage for ADC (external grounding through 0.01uF)			
REFN	O	Reference voltage for ADC (external grounding through 0.22uF)			
REFP	O	Reference voltage for ADC (external grounding through 0.22uF)			
TAOUT	O	Output for testing (open)			
External CLK					
XOSCI	I	Clock oscillation input (HPLL reference clock input)			Input
XOSCO	O	Clock oscillation output			“X”

Note: The initial state is the primary function.

Pin name	Primary function		Secondary function		Initial Status
	I/O	Description	I/O	Description	
Host interface					
SDA	I/O	I^2C bus serial data			Input
SCL	I	I^2C bus serial clock			Input
SAS	I	I^2C bus address selection “L”: 80h (1000_000x)／”H”: 82h (1000_001x)			Input PD
STATUS	O	Status or interrupt (“L” active) output			“H”
System					
RESETN	I	System reset input (active “L”)			Input
SLEEP	I	Sleep enable, “L”: Normal operation / “H”: Sleep			Input PD
TEST1-3	I	Test mode selection, “L”: Normal operation / “H”: Test mode			Input PD
Power supply					
AVDD AGND	—	Power supply and ground for analog			
PVDD_A PGND_A	—	Power supply and ground for HPLL (analog sampling clock generation)			
DVDD_C	—	Power supply for digital core			
DVDD_IO	—	Power supply for digital input/output			
DGND	—	Ground for digital			

Note: The initial state is the primary function. PD = pull-down.
Note: The output at power down is the same as for the initial state.
Note: The pull-up or pull-down internal resistance is 40kΩ.

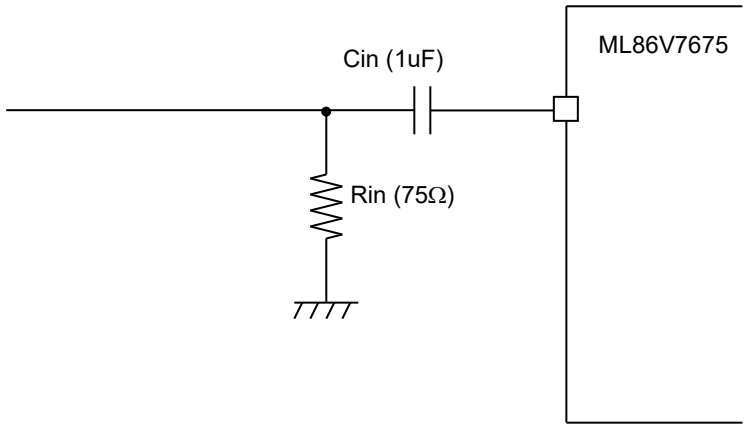
Description

1. Analog Video Input

The ML86V7675 offers component video input, S video input, and composite video input for analog video input.
The analog input supports the composite video defined in ITU-R BT.470 and the component signal (interlace/progressive) defined in SMPTE 293M / ITU-R BT.601、1358.
For the component video YPbPr input, superimpose the composite synchronization signal (Sync-On-Y) on the Y signal.
For the component video RGB input, select from superimposition of the composite synchronization signal on the G signal (Sync-On-G), analog input composite sync (CSYNC_A), digital input composite sync (CHSI), and operation with vertical/horizontal synchronous signals (VSI, CHSI).

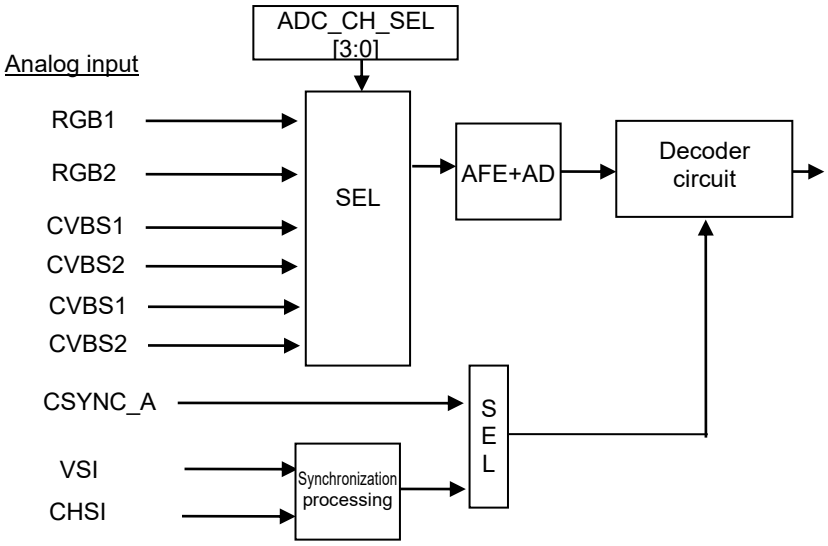
Analog video signal is input using capacitance coupling. Level of the synchronization signal is detected through the internal clamp circuit to reproduce in DC. (Sync-chip clamp)
The internal ADC performs sampling on the analog signals that are clamped. Unused A/D converter enters sleep mode to reduce power consumption.

When inputting a signal to the decoder, the analog video input terminal must compose an external-circuit by figure described below.
The input-resistance which was loaded from the decoder must be about 75 Ω.
When it isn't possible to terminate by 75 Ω in the influence of the selector, the amplifier of the input stage and so on, connect equal to or less than 300 Ω even if maximum.



Cin: Laminated ceramic capacitor (electrostatic capacity allowance ±10%, temperature characteristics ±10%)
Rin: Resistor (accuracy of ±5%)

The ML86V7675 selects and uses one analog video input system to convert to digital video.



Input selection of internal processing circuit (#50h ADC_CH_SEL[3:0])

Input selection	Port for input					
	RGB1	RGB 2	CVBS1	CVBS2	CVBS3	CVBS4
0000	○ (YPbPr)	–	–	–	–	–
0001	–	○ (YPbPr)	–	–	–	–
1000	○ (RGB)	–	–	–	–	–
1001	–	○ (RGB)	–	–	–	–
1011	–	○ (SY/SC)	–	–	–	–
0100	–	–	○	–	–	–
0101	–	–	–	○	–	–
0110	–	–	–	–	○	–
0111	–	–	–	–	–	○
Others	Analog sleep					

Note: CVBS = Composite video signal, SY/SC = S video signal, Other = Component signal

Synchronous input at component input（#01h　SEP_S_MD[1:0]）

Input format	Synchronous input	Pin
Component YPbPr	Sync on Y	GIN1, GIN2
Component RGB	Sync on G	GIN1, GIN2
	Analog composite sync	CSYNC_A
	Digital composite sync	CHSI
	Digital separate sync	VSI, CHSI

2. Sampling Clock

2.1 Sampling Clock Method

As a sampling clock of analog video input, the following two types can be selected.
The related control registers are #5Ch to #5Dh.

(1) Asynchronous sampling method
This sampling method is based on the fixed clock. The sampling clock is selectable from following two operation types:

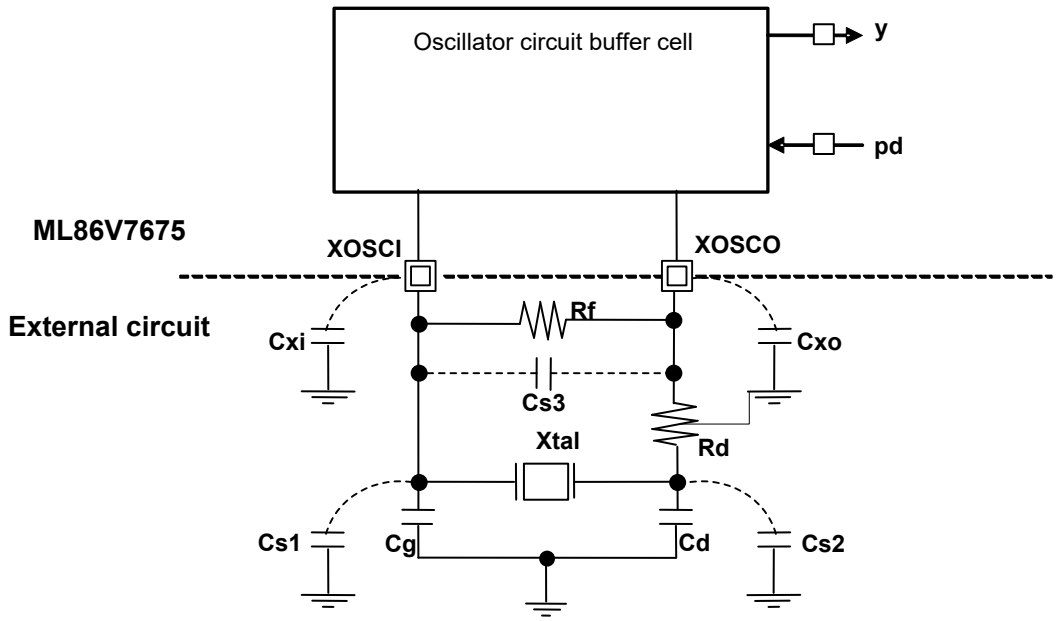
•Directly input from an external pin (enabled only for interlace input, 27MHz sampling operation without HPLL)
•Generated by the built-in HPLL using an external reference clock
When using the built-in HPLL, the clock is generated using a 32MH or 25MHz external reference clock at a fixed dividing ratio(#8Fh/bit[0] OSC_SEL). Since the clock is asynchronous with the video input signal in any case, clock phase is adjusted internally by each line.
There is an advantage with high synchronous traceability for disordered synchronization signal such as a nonstandard video signal or others. However, for composite and S video inputs, a performance of color separation is somewhat influenced if the deflection from a specified clock frequency is large.

(2) Line lock method (HPLL)
Sampling method by line lock PLL.
Because a sampling clock is adjusted to divide a time of one line by a specified number of clocks, this method has an advantage that the number of clocks of one line and one frame (field) always obtain a constant output. However, since traceability is poor for a nonstandard video signal input, a normal output image may not be obtained in some cases.

When the line lock method is selected, the line lock operation mode can be selected by the control register (#5Ch bit[3] PLL_LK_TM). When the #5Ch bit[3] PLL_LK_TM is set to “1” (Fast-lock mode), the trace rate of PLL can be faster while the traceability may be deteriorated if a nonstandard signal is input.
Moreover, the trace rate of the line lock operation can be adjusted by the control register (#5Dh). Stability may be deteriorated when the trace rate is made faster.

2.2 External Reference Clock

The following figure shows the external circuit configuration chart of the external clock to which the internal PLL refers, and an example of the component layout.
Use the 32MHz or 25MHz for the external crystal frequency.
To ensure the line clock stability, use an external crystal with the frequency accuracy of 100 ppm or less.



Circuit constants

As a reference, the following table shows an example of circuit constants.

Rf	Rd	Cg(*)	Cd(*)	Load capacity of available oscillator
1MΩ	100Ω	8pF	8pF	8pF

(*)These values are excluding the input-capacitance Cxi, Cxo and stray-capacitance Cs1, Cs2 and Cs3.
The stray-capacitance values are varied by mounting conditions on Print circuit board and so on.
The experimental examination and evaluation of these values are strongly recommended.
Please refer the details to the vender of the crystal oscillator.

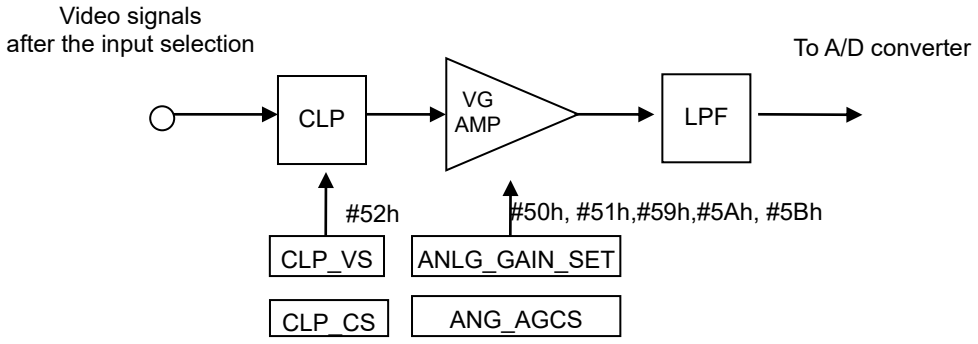
$$CL \fallingdotseq (Cg + Cs1 + Cxi) // (Cd + Cs2 + Cxo) + Cs3$$
$$= ((Cg + Cs1 + Cxi)*(Cd + Cs2 + Cxo)) / ((Cg + Cs1 + Cxi) + (Cd + Cs2 + Cxo)) + Cs3$$

3. Analog Front End Section (Clamp, LPF, Amplifier)

The analog front end (AFE) performs the following processes:

- Detection of the analog video signal sync chip
- Clamp operation for converting to the built-in ADC input range
- Anti-aliasing using the LPF
- Level adjustment using the analog AGC (Auto Gain Control) function

AGC function has the output level adjustment function of the digital section (luminance block) as well as the input adjustment function by the internal amplifier. Manual gain setting is also available for the internal amplifier.
ML86V7675 has individual gain coefficient for each 4ch internal amplifier.



4. CVBS Video Decoder Section

The CVBS video decoder section has the Y/C separation, luminance processing, chrome processing, synchronization processing, and VBID detection functions.

4.1 Y/C Separation

Y/C separation function separates the composite video data into Y (luminance) component and C (composite color difference) component.
The Y/C separation method is two-dimensional separation method without inter-field calculation. The format of Y/C separation filter used differs depending on the input video signal method. You can specify the mode to select the Y/C separation filter for each signal type.

Mode selection	Y/C separation method		
	NTSC	PAL	SECAM
Mode 0	Adaptive filter	Adaptive filter	Trap filter
Mode 1	Three-line comb filter	Two-line comb filter	
Mode 2	Trap filter	Trap filter	
Mode 3	Three-line comb/trap Adaptive filter	Not defined	

4.2 CVBS Input Signal System

The CVBS input signal system is discriminated based on the following specifications.

Signal system	Number of lines (frames)	Field frequency (Hz)	Sub-carrier frequency (MHz)	Black level (IRE)
NTSC-M	525	59.94	3.58	7.5
NTSC-Japan	525	59.94	3.58	0
PAL-B, B1, D, D1, G, H, I, K	625	50	4.43	0
NTSC-443	525	59.94	4.43	0
PAL-M	525	59.94	3.576	7.5
PAL-N	625	50	4.43	7.5
PAL-Nc	625	50	3.582	0
PAL-60	525	59.94	4.43	0
SECAM	625	50	-	0

For input signal systems, you choose to automatically detect from the cycle of horizontal and vertical synchronization signals reproducing from synchronizing separation and the color burst signal or to fix to use the specified system.
Among the input signal systems, automatic discrimination is available to the NTSC system (including -M / -Japan) defined in the ITU-R BT.470 recommendation, to the PAL system (B, B1, D, D1, G, H, I, K, M, N, and Nc, and to the SECAM system. For other systems such as NTSC-443 and PAL-60, NTSC-M and NTSC-J, you have to explicitly select by using the control register.

4.3 Luminance Processing

Level adjustment (AGC) processing is available for Y (luminance) data after Y/C separation. As the level adjustment, there are digital AGC (Automatic Gain Control) and analog amplifier AGC. Analog amplifier AGC is adjusted by the control register #51h.
The upper limit of the digital AGC scaling factor is about four times. If the amplitude of input signal is small, analog amplifier AGC adjusts it. The analog amplifier AGC scaling factor is from about 0.507 times to 4.5 times.

Digital AGC refers the depth of SYNC of Y (luminance) data after Y/C separation, and then adjusts the scaling factor of the luminance processing. The control register #21h enables fine adjustment of the luminance level.
In addition, digital MGC (Manual Gain Control) mode which determines luminance scaling factor by the register is available, regardless of depth of SYNC.

Digital AGC/MGC mode is divided into the following combinations, depending on the combination of settings of control registers #20h[7:6] and #20h[4]:

#20h[7:6]	#20h[4]	Operation
00	0	AGC slow
01	0	AGC medium
10	0	AGC fast
11	0	Inhibit
XX	1	MGC

4.4 Color Difference Processing Section

C (composite color difference) data after Y/C separation is separated into two components of Cb and Cr by the color difference processing section. Color difference processing section adjusts the level of the data based on the color burst signals (digital ACC: Automatic Color Control), demodulates them by reproducing color sub-carriers based on each video signal format, and then separates them into Cb data and Cr data. The hue of Cb and Cr data can be adjusted.
Color difference processing is adjusted by the control registers #30h to #39h.

#30h[7:6]	Operation
00	ACC fast
01	ACC slow
10	ACC medium
11	MCC

If the color demodulation is determined not to be performed correctly, the color killer processing (erases colors) is performed.
Color killer processing is adjusted by the control registers #33h to #34h.

4.5 Synchronization Processing Section

Separates into the vertical synchronization signals and the horizontal synchronization signals using Y (luminance) data of composite video data.
Synchronization processing section generates synchronizing separation threshold from input signals automatically, and then generates vertical valid range/horizontal valid range.
Synchronizing separation is adjusted by the control registers #14h to #16h. The following settings are available:

- •Selection of synchronizing separation threshold between automatic and manual
- •Adjustment of synchronizing separation threshold
- •Method of automatic generation of the synchronizing separation threshold
  You can select from the method to generate based on the digital AGC gain value and the method to generate based on the depth of SYNC.
- •Filter selection for Y (luminance) data at synchronous detection
  Anti-noise filter can be selected in case of the light electric field signal.
- •[Horizontal synchronization signal detection] Window
  After detecting horizontal synchronization signals, you can set the range to detect the next horizontal synchronization signals.
- •[Vertical synchronization signal detection] Window
  After detecting vertical synchronization signals, you can set the range to detect the next vertical synchronization signals.

Because the detection of vertical synchronization signal detection supports light electric field signals, it can be reflected to the internal operations after checking validity of the result of the vertical synchronization detection.
Vertical synchronization signal detection is adjusted by the control registers #1Ah.

Because the detection of horizontal synchronization signals supports light electric field signals, it can be reflected to the internal operations after correcting the shift in the result of the horizontal synchronization detection by using horizontal AFC (Automatic Frequency Control) circuit.
Horizontal AFC is adjusted by the control register #18h.

The horizontal AFC includes the PLL-AFC using line lock PLL, and the digital AFC that corrects pixel errors in horizontal synchronization detection. PLL-AFC operates in the line lock state and generates a horizontal synchronization signal per one line with the line lock clock. Digital AFC operates in the states other than line lock. It multiplies the result of horizontal synchronization detected by the specified gain (DAFC_GAIN #2Ah), and then generates horizontal synchronization signals that have been applied error correction. Operation status of the horizontal AFC can be monitored by status register #71h bit[2].

Based on the results of horizontal synchronization signals detection and vertical synchronization signal detection, blue-back processing is performed to display blue on the full screen. Blue-back processing is adjusted by the control registers #40h to #44h. Results of the blue-back detection can be monitored by status register #71h bit[1].

There is a built-in judgment circuit that judges the current state as light electric field signal state based on the pixel errors at horizontal synchronization detection and the number of lines that contain these errors. Additionally, there is a built-in circuit that detects the VTR signal input status based on the pixel errors at horizontal synchronization detection and the line errors of horizontal synchronization detection.
Each detection result can be monitored by the status register #71h.

The process to make the length of lines constant is performed since the number of clocks in one line may increase/decrease due to the disorder of the input synchronization signals in the case of asynchronous sampling method.
Detects errors in accuracy of 1/16 pixel based on the luminance data between pixels before and after synchronizing separation threshold in the horizontal synchronization detection, and then corrects the pixel position of luminance data and color difference data.

4.6 VBI Data Slicer, Detection of Copy Protection

Copy protect information and various data superimposed to the vertical blanking interval (VBI: Vertical Blanking Interval) of input video signals can be extracted and read from the control register.
The following data can be read:

(1) Copy protection
    VBI nonstandard signal (NTSC/PAL), nonstandard color burst signal (NTSC only)
(2) Closed caption
    Keeps characters information such as caption, odd number line/even number line (NTSC/PAL)
(3) WSS (Wide Screen Signaling)
    Wide video identification signal defined by ETS 300 294 (PAL only)
(4) CGMS-A (Copy Generation Management System - Analog)
    Copy generation management information defined by IEC61880 (NTSC)

5. COMPONENT Video Decoder Section

The COMPONENT video decoder section has the luminance/color difference processing, synchronization processing, and VBID detection functions.

5.1 COMPONENT Input Signal Format

The component input signal format is discriminated based on the following specifications.

D1 setup (#00h/bit[2:1] ISPMD[1:0]=00)

Signal system	Number of lines(frame)	Field frequency [Hz]	Line frequency	Correspondence standard
480i	525	59.94	15734	ITU-R BT.601
576i	625	50	15625	ITU-R BT.601

D2 setup (#00h/bit[2:1] ISPMD[1:0]=00)

Signal system	Number of lines(frame)	Field frequency [Hz]	Line frequency	Correspondence standard
480p	525	59.94	31468	SMPTE 293M
576p	625	50	31250	ITU-R BT.1358

For input signal formats, you can choose to automatically detect from the cycle of the horizontal and vertical synchronization signals reproducing from synchronizing separation or to fix to use the specified format.

WVGA setup (#00h/bit[2:1] ISPMD[1:0]=01, sampling frequency 33.231MHz)

Signal system	Number of lines(frame)	Field frequency [Hz]	Line frequency	Correspondence standard
480p	525	59.94	31468	SMPTE293M

WVGA setup (#00h/bit[2:1] ISPMD[1:0]=10, sampling frequency 33.333MHz)

Signal system	Number of lines(frame)	Field frequency [Hz]	Line frequency	Correspondence standard
480p	525	60.57	31800	-

EGA setup (#00h/bit[2:1] ISPMD[1:0]=11)

Signal system	Number of lines(frame)	Field frequency [Hz]	Line frequency	Correspondence standard
262p	262	60	15734	-

Automatic detection of an EGA input signal system cannot be performed.

The automatic judgment at component input has the following operation restriction:

- At component input, “SYNC depth” and “Blank Level (7.5IRE setup)” cannot be automatically judged. The “SYNC depth” and “Blank Level” at component input can be set using the control register #01h bit[5] and bit[4].
- EGA(400x234 or 480x234), WVGA cannot be automatically judged.

5.2 COMPONENT Luminance/Color Difference Processing

The gain coefficient is automatically calculated from the synchronous signal on Y or G signal. Level adjustment (AGC) processing is available for all Y/PbPr or RGB input signals.
The operation that inputs synchronization signals via CHSI , VSI and CSYNC_A at the LVTTL level supports only the MGC mode.

5.3 Synchronization Processing Section

For the component YPbPr and RGB inputs, superimpose the composite synchronization signal on the Y or G signal. The synchronization signal input from CSYNC_A, CHSI and VSI can be supported only for the component RGB input. Processings such as synchronous detection are equivalent to those for composite video input.

5.4 VBI Data Slicer, Detection of Copy Protection

Copy protect information and various data superimposed to the vertical blanking interval (VBI: Vertical Blanking Interval) of input video signals can be extracted and read from the control register.
The following data can be read:

(1) Copy protection
VBI nonstandard signal (480i/576i/480p/576p)

(2) CGMS-A (Copy Generation Management System - Analog)
Copy generation management information defined by IEC61880 (480i/480p)

5.5 Sampling frequency set mode

In sampling frequency set mode, sampling processing is done by the clock corresponding to the dot clock of YPbPr or RGB progressive 525 line video signals except TV signals defined in the ITU-R BT.601 or SMPTE293M.

To select sampling frequency set mode as input video format, then related registers are available.
Sampling frequency variable mode processing is controlled by the control registers #00h and #84h to #8Eh.

- Set the input video format to sampling frequency set mode (#00h)
- Set the sampling frequency corresponding to the dot clock of input video signal (#84h to #87h)
- Set the total pixels (#88h,#89h), the horizontal valid start position and horizontal valid width (#8Ah to #8Ch) according to horizontal timing of input signal.
- For Sync on Y/G input, AGC processing is enabled by adjusting sync tip position and pedestal position (#8Dh, #8Eh)

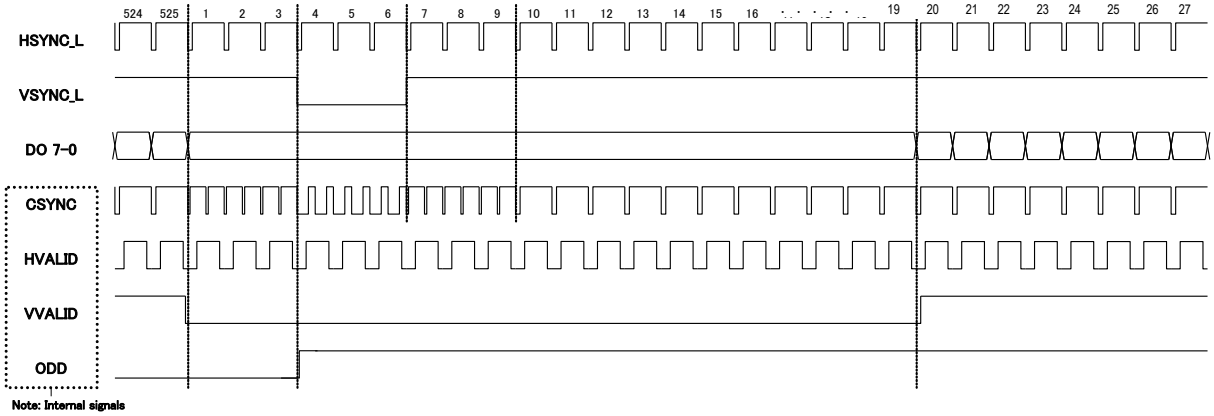
The sampling frequency set mode has the following restriction:

- Only available when fixed mode for video mode setting is set(#00h/bit[0] AVMD)
- Only available when D1/D2 for sampling clock setting is selected(#00h/bit[2:1] ISPMD)
- Horizontal total pixels can be set 576 to 1280 pixels
- Horizontal total pixels, valid start position and valid width registers can be set even number.
- Only available for vertical line number is 525(Vertical timing is same as 480P)

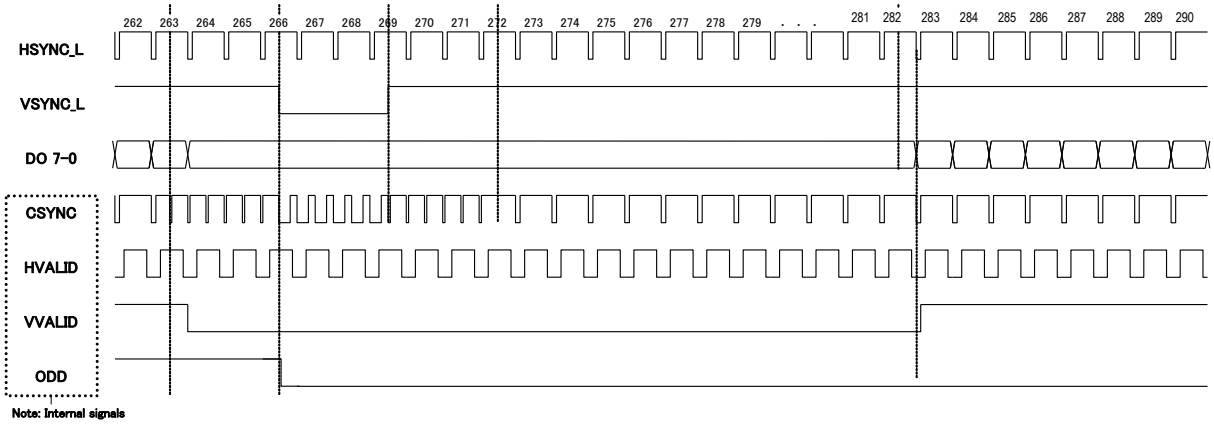
6. Synchronization Signal internal Timing

6.1 Vertical Timing

◆ NTSC Vertical Timing

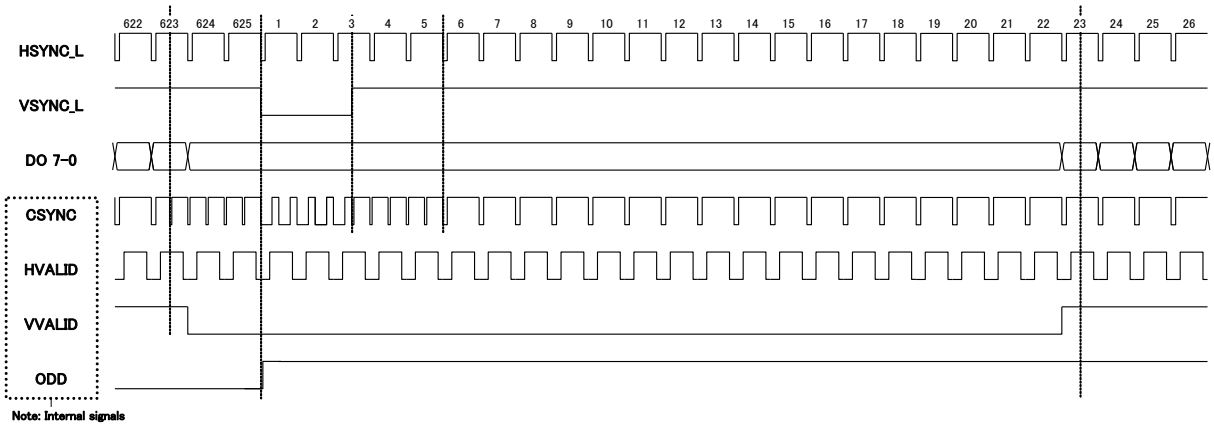


ODD Field Internal Timing

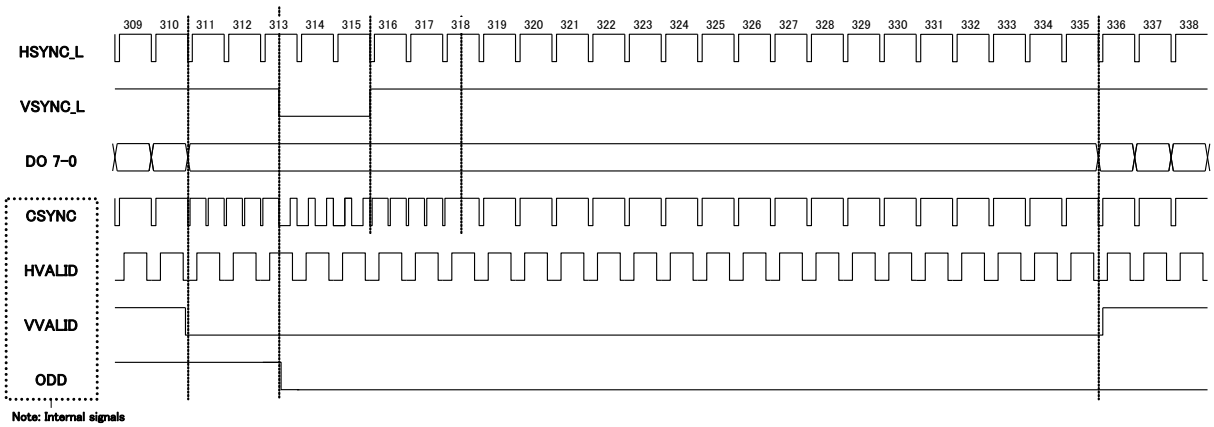


EVEN Field Internal Timing

◆ PAL Vertical Timing



ODD Field Internal Timing



EVEN Field Internal Timing

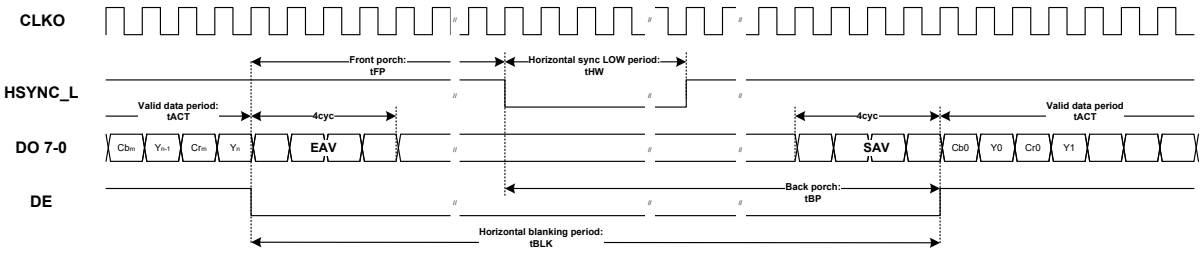
6.2 Horizontal Timing

ML86V7675 output format offers ITU-R BT.656 style or YCbCr 8bit.

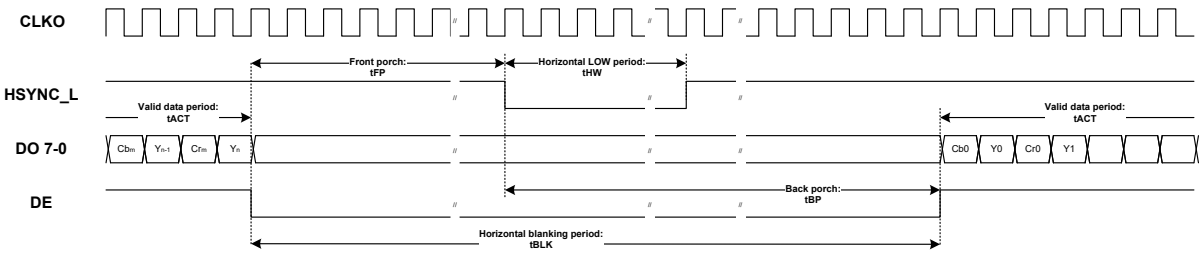
#04[2:0]	Data format	Output pin
000	ITU-R BT.656 style	DO7-0
001	8bit YCbCr	DO7-0

Following figures describe digital video, sync signal output timing.

6.2.1 Horizontal Timing in ITU-R BT.656 Mode



6.2.2 Horizontal Timing in "8-Bit Multiplexed + Sync Signal" Mode



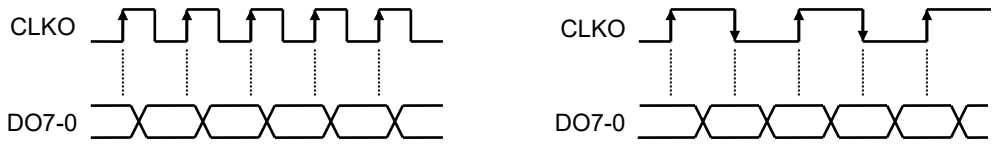
Video format	Sampling frequency	Horizontal(number of pixels)					Vertical(number of lines)		
		1H total	Front porch	Sync Width	Back porch	Valid period	Blank period	Valid period	1V total
			tFP	tHW	tBP	tACT			
NTSC (ITU-R BT.601) D1(480I)	27.000MHz	1716	32	120	244	1440	Odd/19 Even/19	Odd/244 Even/243	Odd/262.5 Even/262.5
NTSC (4fsc)	28.636MHz	1820	32	120	252	1536	Odd/19 Even/19	Odd/244 Even/243	Odd/262.5 Even/262.5
PAL / SECAM D1(576I)	27.000MHz	1728	24	120	264	1440	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5
D2(480P)	27.000MHz	1716	32	120	244	1440	42	483	525
D2(576P)	27.000MHz	1728	24	120	264	1440	49	576	625
EGA 400 x 234	7.9930MHz	1016	44	80	172	800	28	234	262
EGA 480 x 234	9.58216MHz	1218	54	80	204	960	28	234	262
WVGA 800 x 480	33.333MHz	2120	144	120	376	1600	42	483	525
	33.231MHz	2112	40	120	300	1772	42	483	525

Note: Where the FIFO mode is used in asynchronous sampling operations with fixed clock, the 1-field sampling error accumulated in the line immediately following the fall of VVALID is reset. Therefore, the pixel count for the line that was reset will change. In addition, where the condition of VTR and other signals is poor in the FIFO-2 mode, the FIFO reset line might break in before the fall of VVALID.

"V blank", "Active lines", and "Total lines" in the table above indicate the period
The digital lines 1716T (NTSC, 525) and 1728T (PAL, 625) varies due to the sampling error when this LSI is operated in the asynchronous sampling mode.
When used in the FIFO mode, although there is no variation in the number of pixels between valid lines due to the pixel count compensation function, the line immediately after VVALID has fallen varies due to FIFO reset. In particular, when non-standard signals such as of a VTR are input, the line immediately after VVALID falls varies widely depending on the degree of the instability of that input signal, and when the error is large the change occurs immediately before the fall of VVALID.
Further, EAV or SAV may not be guaranteed in the case of non-standard signals in which the number of lines increases or decreases with respect to the reference value.

6.2.3 Data Clock Output

Data clock (CLKO) selectable single data rate mode(SDR) or dual data rate mode(DDR). In SDR mode output data is synchronous to positive edge or negative edge of CLKO. In DDR mode output data is synchronous to both positive edge and negative edge.



(a) SDR mode（positive edge） (b) DDR mode

#05h/bit[1:0]	Data clock format
10	SDR mode
01	DDR mode
00/11	Inhibit

7. Image Quality Adjustment

There are the following control registers for image quality adjustment in video decoder section and scaler section. The registers in the video decoder section are effective for analog video input, while the registers in scaler section are effective for both analog and digital video input.

Registers for image quality adjustment in video decoder section

- •Luminance level adjustment : Adjusts luminance level of analog video input. Capable of setting AGC (automatic luminance adjustment) / MGC (manual luminance adjustment) / Peak AGC.
- •Color level adjustment : Adjusts color difference level of analog video input. Capable of setting ACC (automatic color adjustment) / MCC (manual color adjustment).
- •Contour correction and coring : Corrects contour correction of analog video input.
- •Contrast adjustment : Adjustable around 128 with a slope ranging from 1/32 to 63/32.
- •Luminance offset adjustment : Capable of adjusting the analog video input luminance between -7 and +7 IRE(for Composite, YPbPr inputs). Capable of adjusting the analog video input luminance between -128 and +127 LSB(for Composite, YPbPr RGB inputs).
- •Hue control : Capable of adjusting the analog video input color phase at an adjustment angle ranging from -178.6° to +180°.
  (Setting disabled for the SECAM or component video input.)
  Capable of adjusting the analog video input color phase at an adjustment angle ranging from -45° to +44.6°.

8. STATUS and Interruption Outputs

The status detection result is output as the STATUS or interrupt signal.
The STAUS output outputs the current status detection result on the video decoder section (e.g., HPLL lock detection, NTSC/PAL automatic discrimination, VBID detection status). The internal register selects the status detection result to output.
The interruption output outputs an interrupt when there is a change to any of the video decoder section status detection results. Each status detection result is maskable.
(The status retention until the interrupt is cleared is not performed.)

- •Discrimination result of input format
- •Detection/non-detection of VBID
- •Detection/non-detection of light electric field state and VTR input (interrupt output only, not output from a STATUS terminal)
- •Monitoring of AFC operation status
- •Monitoring of input synchronization detection status
- •Monitoring of line lock state by internal PLL

9. Sleep Function

The ML86V7675 has the sleep function for suppressing the power consumption by using SLEEP input or a control register.

Sleep control	Internal clock	Analog operation	Output port
Control register (#FFh)	Stops except the I2C control clock	AFE, ADC, HPLL, Sleep	VSYNC_L, HSYNC_L, FID, DE, CLKO, DO7-0 : “L” output
SLEEP input	Stops oscillation		VSYNC_L, HSYNC_L, FID, DE, CLKO, DO7-0 : “HiZ”

10. I²C Bus Interface

Each function block of the ML86V7675 controls the operation by writing data to the control register.
The control register is accessible via the I²C bus interface.
The I²C bus slave address is selectable from the following two addresses according to the pin setting.

Slave address	SAS
80h (1000_000x)	0
82h (1000_001x)	1

In the I²C bus communication, the 1-byte data following the slave address is used as the register address (beginning address).
The 2 types of addressing modes are available for accessing a control register.

(1) Address increment mode

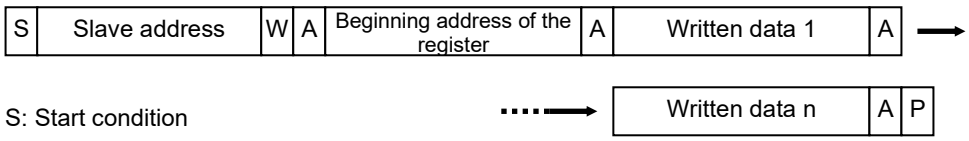
This mode is selected in the default state. When two or more data are sequentially accessed, the register address is incremented starting from the specified beginning address. This is useful to access a contiguous register address area.

(2) Address circulating mode

One to four addresses from the beginning address of the register can be accessed in a circular fashion. It is useful to access the same address for multiple times (the number of circulating is 1) or access 2 - 4 addresses in a circular fashion.

(a) Register Write Format

Write data to the specified register address.

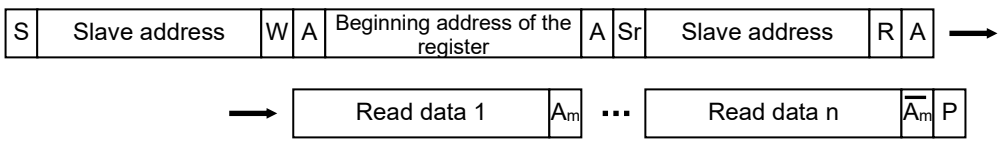


S: Start condition

A: Acknowledge (slave)
P: Stop condition
W = “0” (write)

(b) Register Read Format

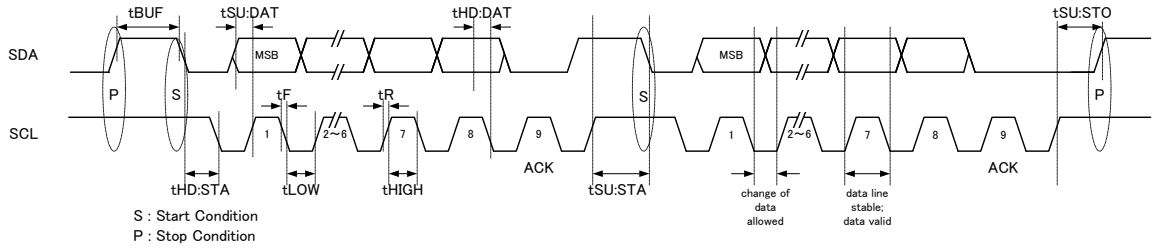
Read data from the specified register address.



S: Start
Sr: Restart
A: Acknowledge (slave)
A_m: Acknowledge (master)
P: Stop
W = “0” (write)
R = “1” (Read)

I²C Bus Interface Basic Timing

The SDA value should not be changed while SCL is “H” except for the start condition/stop condition (S/P). Communicate in the I²C bus. after all the power supplies have reached the specified values and a stable clock has been input.



I²C Standard Table (Standard Mode)

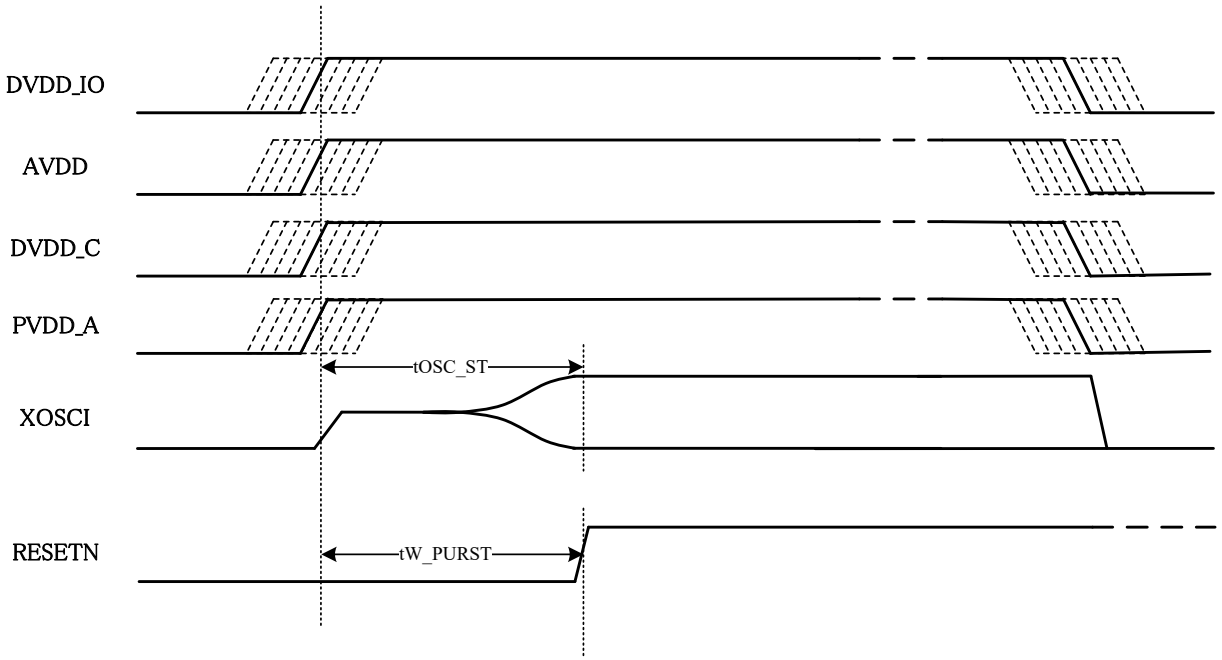
Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL Frequency	0	-	100	KHz
tBUF	Bus Open Time	4.7	-	-	µs
tHD:STA	Start Condition Hold Time	4.0	-	-	µs
tLOW	Clock LOW Period	4.7	-	-	µs
tHIGH	Clock HIGH Period	4.0	-	-	µs
tSU:STA	Start Condition Setup Time	4.7	-	-	µs
tHD:DAT	Data Hold Time	0(300)	-	-	ns
tSU:DAT	Data Setup Time	250	-	-	ns
tR	Line Rise Time	-	-	1000	ns
tF	Line Fall Time	-	-	300	ns
tSU:STO	Stop Condition Setup Time	4.0	-	-	µs

I²C Standard Table (Fast Mode)

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL Frequency	0	-	400	KHz
tBUF	Bus Open Time	1.3	-	-	µs
tHD:STA	Start Condition Hold Time	0.6	-	-	µs
tLOW	Clock LOW Period	1.3	-	-	µs
tHIGH	Clock HIGH Period	0.6	-	-	µs
tSU:STA	Start Condition Setup Time	0.6	-	-	µs
tHD:DAT	Data Hold Time	0(300)	-	-	ns
tSU:DAT	Data Setup Time	100	-	-	ns
tR	Line Rise Time	-	-	300	ns
tF	Line Fall Time	-	-	300	ns
tSU:STO	Stop Condition Setup Time	0.6	-	-	µs

11. Power on Sequence

When turning on the power, follow the sequence shown in the figure below:



Power On/Off Sequence

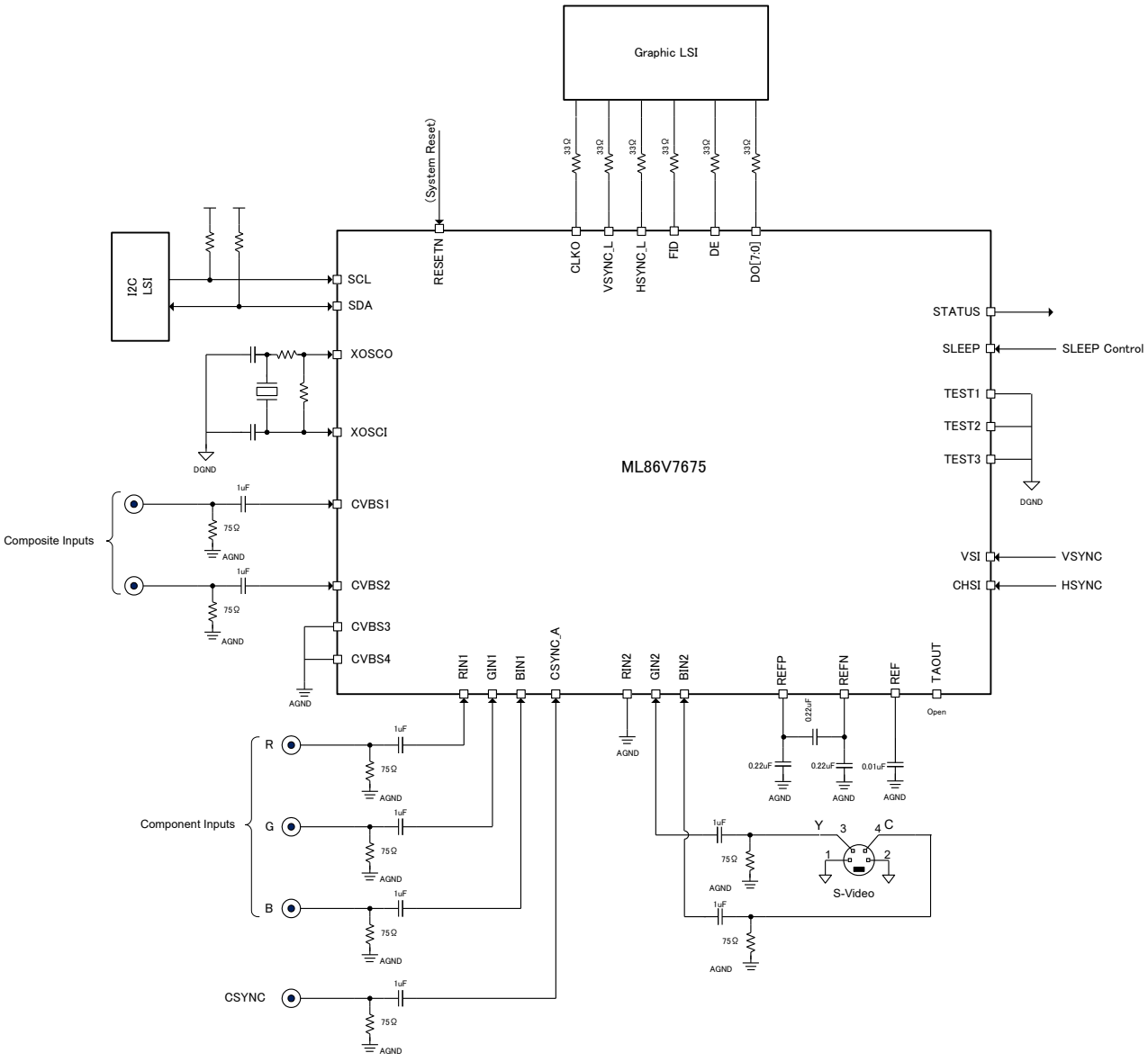
There are no restrictions on the power-on sequence between the above four power supplies (DVDD_IO, AVDD, DVDD_C, PVDD_A,): Those power supplies can be turned on starting from any of them.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
The Oscillator activation time	tOSC_ST	—	—	10	ms	
Reset time after power on	tW_PURST	10	—	—	ms	

This LSI should be used after the specified voltages have been applied to all the power supplies.
When applying a voltage to any input pin, do so after making sure that the power supply voltages have stabilized in the specified levels.
Apply reset after all the power supplies have reached the specified values and a stable clock has been input.

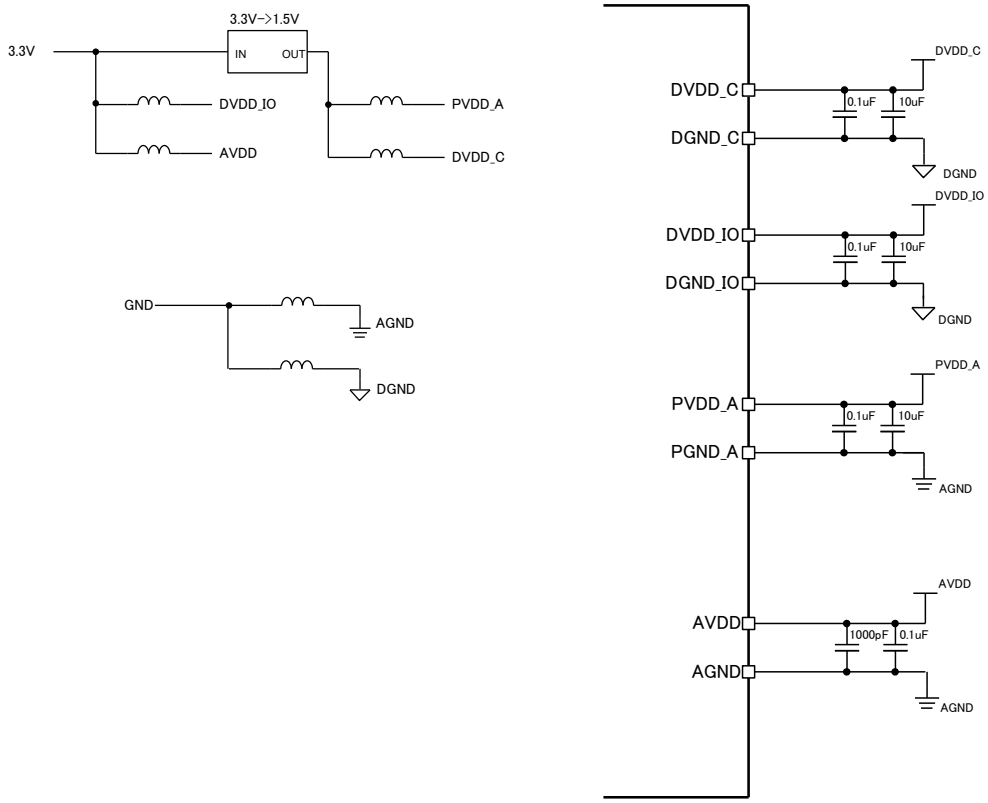
12. Example of Application Circuit

○Example of Generic Application Circuit



The example of the circuit appears here just for the purpose to show the application example, and then does not guarantee its characteristics. When using this LSI,
verify the operation with the best suited circuit elements and circuit configurations for your system.

○Example of Power Supply/Ground Separation



[Notes on Board Layout]

1. It is recommended to add a damping resistor for digital output signal connection to reduce any digital noise.
2. Connection with ceramic capacitors of about 0.1µF and 10µF is recommended between each of digital power supply (DVDD_IO, DVDD_C) and digital ground (DGND).
3. Connection with ceramic capacitors of about 1000pF and 0.1µF is recommended between analog power supply (AVDD) and analog ground (AGND). Connection with ceramic capacitors of about 0.1µF and 10µF is recommended between analog power supply (PVDD_A) and analog ground (AGND).
4. Avoid placing any noise source around TAOUT.
5. Avoid placing any noise source around REF, REFP and REFP. Wire as short as possible.
6. For the analog video signals, shorten the distance from the coupling capacitor to the input pin of the device as much as possible to avoid inducement interference.
7. It is recommended to assign large area for the analog power supply (AVDD) and the analog ground (AGND) for good separation from the digital power supply and the ground.

The example of the circuit appears here just for the purpose to show the application example, and then does not guarantee its characteristics. When using this LSI, verify the operation with the best suited circuit elements and circuit configurations for your system.

13. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (for analog)	AVDD	AGND = 0 V PGND_A = 0 V DGND = 0 V Ta = 25°C	–0.3 to +4.6	V
Power supply voltage (for HPLL)	PVDD_A		–0.3 to +2.0	
Power supply voltage (for logic core)	DVDD_C		–0.3 to +2.0	
Power supply voltage (for I/O)	DVDD_IO		–0.3 to +4.6	
Analog input voltage	VAI		–0.3 to AVDD+0.3	
Logic input voltage	VDI1		–0.3 to DVDD_IO+0.3	
Logic input voltage (5 V tolerant)	VDI2		-0.3 to +6.0*1	
Logic output voltage	VO		–0.3 to DVDD_IO+0.3	
Output short-circuit current	IOS	—	16	mA
Power dissipation	PD	Ta = 85°C	1.0	W
Storage temperature	Tstg	—	–55 to +125	°C

Note: Absolute maximum ratings are the marginal values that do not cause physical damage to the device. The device quality might be damaged if the rating of any one of these items is exceeded even for a moment. Be sure to use within this rating.

*1: Specified when power is supplied.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (for analog)	AVDD	AGND = 0 V	3.0	3.3	3.6	V
Power supply voltage (for HPLL)	PVDD_A	PGND_A = 0 V	1.35	1.5	1.65	
Power supply voltage (for logic core)	DVDD_C	DGND = 0 V	1.35	1.5	1.65	
Power supply voltage (for I/O)	DVDD_IO	DGND = 0 V	3.0	3.3	3.6	
Ambient temperature	Ta	—	–40	25	+85	°C

Note: Also avoid the situation where only some power supplies are powered on/off. All power supplies must be on or off.

■ Electrical Characteristics

● DC Characteristics

DVDD_IO, AVDD = 3.3V±0.3V, PVDD_A, DVDD_C = 1.5V±0.15V
DGND, AGND, PGND_A = 0 V , Ta = -40 to +85°C

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Analog input voltage		VVIN	Capacitance coupling	—	1.3	—	Vp-p
"H" level input voltage 1		VIH1	LVTTL input pins	2.0	—	VDDIO+0.3	V
"H" level input voltage 2		VIH2*1	5 V tolerant, Schmitt input pins	2.1	—	5.5	V
"H" level input voltage 3		VIH3*2	Schmitt input pins	2.1	—	VDDIO+0.3	V
"L" level input voltage		VIL	LVTTL input pins	-0.3	—	0.8	V
"L" level input voltage 2		VIL2*3	Schmitt input pins	-0.3	—	0.7	V
"H" level output voltage 1		VOH1	IOH = -2, -4 mA	2.4	—	—	V
"L" level output voltage 1		VOL1	IOL = 2, 4 mA	—	—	0.4	V
"H" level output voltage 2		VOH2*4	IOH = -6 mA	2.4	—	—	V
"L" level output voltage 2		VOL2*4	IOL = 6 mA	—	—	0.4	V
Input leakage current 1		IIL1	VIN = DVDD_IO or DGND	-10	—	+10	µA
Input leakage current 2		IIL2*5	XOSCI=DVDD_IO or DGND	-1.0	—	+1.0	µA
Output leakage current		IOL	VIN = DVDD_IO or DGND	-10	—	+10	µA
"H" level input current (pull-down)		IIHd	VIN = DVDD_IO	20	—	200	µA
Current during operation	Analog video section	IDDA	Component video input Sampling 33 MHz	—	70	95	mA
	HPLL section	IDDPA	At 33 MHz oscillation	—	1	2	mA
	Logic section	IDDC	Component video input Sampling 33 MHz CLKO = 66MHz	—	50	70	mA
	IO+ oscillation section	IDDIO	CLKO = 66MHz CL = 15 pF	—	20	26	mA
Current during power down	Analog video section	IDDA	SLEEP="H"	—	0.5	2	mA
	HPLL section	IDDPA		—	0.05	0.5	mA
	Logic section	IDDC		—	1.0	5	mA
	IO+ oscillation section	IDDIO		—	0.5	2	mA

*1: VIH2 is applied to the CHSI and VSI pins.
*2: VIH3 is applied to the SCL, SDA, and RESETN pins.
*3: VIL2 is applied to the RESETN, SCL, SDA, CHSI, and VSI pins.
*4: VOH2 and VOL2 are applied to XOSCO pins.
*5: IIL2 is applied to XOSCI pins.

- ADC Characteristics

DVDD_IO, AVDD = 3.3V±0.3V, PVDD_A, DVDD_C = 1.5V±0.15V
DGND, AGND, PGND_A = 0 V , Ta = -40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SN ratio	SNR	fin=1 MHz, fck=27MHz	—	50	—	dB
Differentiation linearity error margin	DLE	Lamp wave, fck=1MHz	—	0.5	—	LSB
Integration linearity error margin	ILE	Lamp wave, fck=1MHz	—	0.75	—	LSB

- AFE Characteristics

DVDD_IO, AVDD = 3.3V±0.3V, PVDD_A, DVDD_C = 1.5V±0.15V
DGND, AGND, PGND_A = 0 V , Ta = -40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain setting value deviation	ΔG	—	-3.0	—	3.0	dB
Clamp voltage	Vclp	—	—	1.088	—	V
Clamp current	Iclp	CLP_CS = “4”	140	280	420	μA
		When clamp is stopped	-3	-7	-15	μA

Note: “CLP_CS” is the name of the control register for clamp current selection.
The clamp section is 10% or less in one line. Other sections are treated equally as when the clamp is stopped.

- AFE + ADC general characteristic

DVDD_IO, AVDD = 3.3V±0.3V, PVDD_A, DVDD_C = 1.5V±0.15V
DGND, AGND, PGND_A = 0 V , Ta = -40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differentiation gain	DG	Input 3.58 MHz	—	3.0	—	%
Differentiation phase	DP	Input 3.58 MHz	—	3.0	—	deg.
Input bandwidth	FC	Gain at 4 MHz for DC 0dB when the set to 10 MHz	-1.5	—	1.0	dB
		Gain at 8 MHz for DC 0dB when the set to 20 MHz	-2.0	—	2.0	dB

- Line lock PLL characteristics

DVDD_IO, AVDD = 3.3V±0.3V, PVDD_A, DVDD_C = 1.5V±0.15V
DGND, AGND, PGND_A = 0 V , Ta = -40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VCO output frequency	Fvco	27.0000 MHz	—	27.000	—	MHz
		28.6363 MHz	—	28.636	—	MHz
		7.993006 MHz	—	7.993	—	MHz
		9.582167 MHz	—	9.582	—	MHz
		33.231 MHz	—	33.231	—	MHz
		33.333 MHz	—	33.333	—	MHz

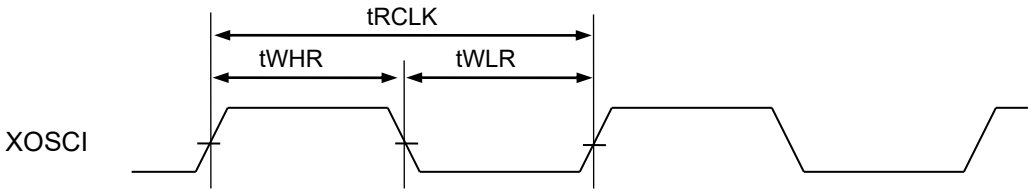
- AC Characteristics

DVDD_IO, AVDD = 3.3V±0.3V, PVDD_A, DVDD_C = 1.5V±0.15V
DGND, AGND, PGND_A = 0 V , Ta = -40 to +85°C

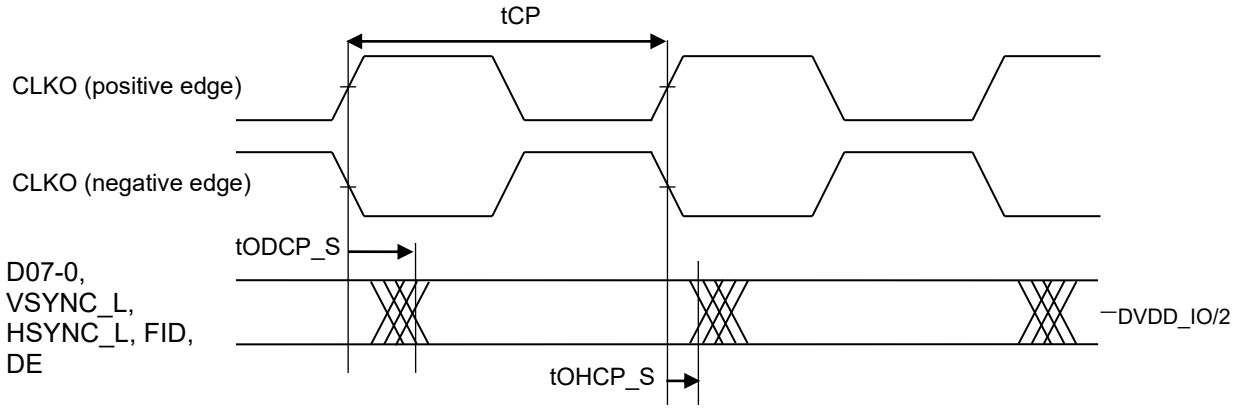
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference clock frequency	fREFCLK	—	—	32	—	MHz
ADC sampling frequency	fADC	—	—	27	—	MHz
CLKO output clock frequency (SDR)	fCP_S	—	—	—	66.67	MHz
CLKO output clock frequency (DDR)	fCP_D	—	—	—	33.34	MHz
XOSCI clock cycle	tRCLK	—	30.0	—	—	ns
XOSCI H level pulse width*1	tWHR	—	12.0	—	—	ns
XOSCI L level pulse width*1	tWLR	—	12.0	—	—	ns
CLKO output clock(SDR) cycle	tCP_S	—	14.9	—	—	ns
CLKO output clock(DDR) cycle	tCP_D	—	29.9	—	—	ns
Output delay(SDR) time (CLKO →)	tODCP_S	CL=15pF	—	—	2.0	ns
Output hold(SDR) time (CLKO →)	tOHCP_S	CL=15pF	-1.0	—	-	ns
Output delay(DDR) time (CLKO →)	tODCP_D	CL=15pF	—	—	tCP_S/2+2.0	ns
Output hold(DDR) time (CLKO →)	tOHCP_D	CL=15pF	tCP_S/2-1.0	—	-	ns
Output clock duty ratio	dtCP	CL=15pF	45	—	55	%
Reset L level pulse width (except power on)	tWRST	—	200	—	—	ns

The characteristics value of the input signal is prescribed using the input voltage DVDD_IO or 0 V. The output signal characteristics value is measured at the point where the output voltage is DVDD_IO/2.

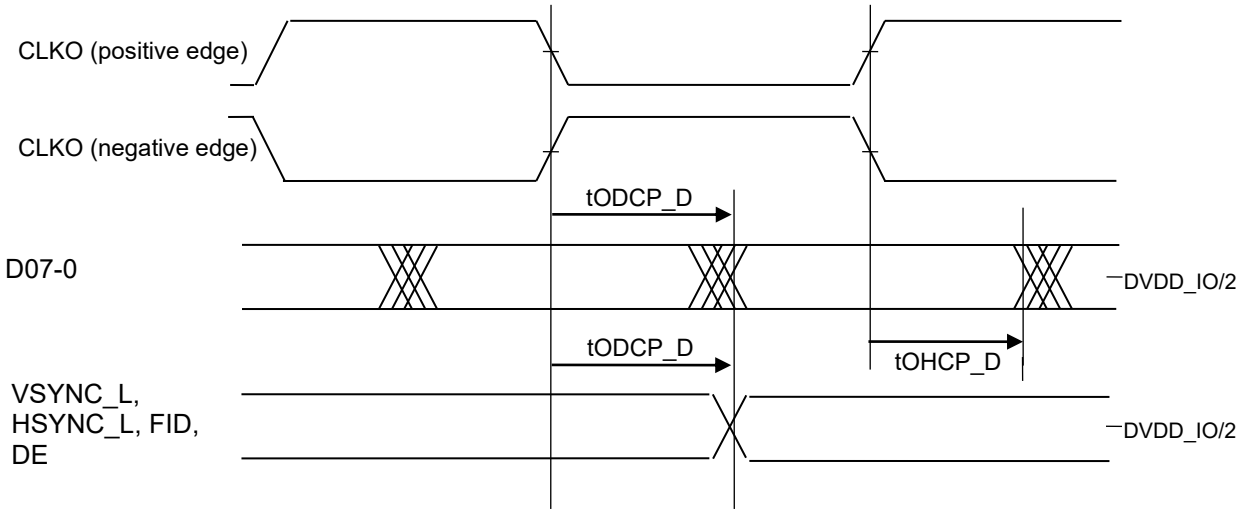
* 1: This is a specification when there is a clock input including the external oscillator. Maximum of 5 ns or lower is recommended as the tr/tf of the input clock.



AC Characteristics External Clock System



AC Characteristics Video Output System (SDR Outpu)



AC Characteristics Video Output System (DDR Outpu)

14. Control Register

14.1 Description of Control Registers

The control register of ML86V7675 is operated from I^2C bus.
The register address is assigned to the sub address #00h-#FFh of I2C bus.

The sub-addresses that are not described in Control Register List do not implement any register. Note that the acknowledge is not returned when these sub-addresses are accessed.
Various operations such as the image quality adjustment and the mode switching can be set by register control.
Data detected by VBI data detection function can be read sequentially from the control register via the internal registers.

The following section describes each register in the order of each address.
The register value with "*" or "(default)" is an initial value.

14.2 Control Register List

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#00h	W/R	VIF[4:0]					ISPMD[1:0]		AVMD	09h	Input signal format setting
#01h	W/R	(res)	(res)	SETUP_IRE	SYNC_IRE	HS_INV	VS_INV	SEP_S_MD[1:0]		10h	Component setting
#02h	W/R	(res)	VMSK-NTSC-443	(res)	VMSK-PAL-M	VMSK-PAL-N	VMSK-PAL-Nc	VMSK-PAL-60	VMSK-SECAM	5Fh	Input mode automatic judgment mask setting
#03h	W/R	(res)								00h	—
#04h	W/R	CLK_INV	C2_SEL	YC_INV	DO_DRV	(res)	OUT_MODE[2:0]			08h	Output format selection 1
#05h	W/R	LIMIT	BLANK_MASK	(res)	FIELD_INV	CbCr_EDGE	CbCr_tim	CLK_SEL	DDR_MODE	02h	Output format selection 2
#06h	W/R	(res)								00h	—
#07h	W/R	(res)								E4h	—
#08h	W/R	(res)	(res)	FIFOMD[1:0]		(res)				00h	Internal operation mode setting
#09h	W/R	(res)								00h	I—
#0Ah	W/R	(res)								00h	—
#0Bh	—	(res)								—	—
#0Ch	W/R	(res)	YC_SFM[2:0]			(res)	COMBF_TH[2:0]			00h	Y/C separation setting 1
#0Dh	W/R	(res)			LUMED	(res)				00h	Y/C separation setting 2
#0Eh	W/R	(res)	ADP_TH[1:0]		(res)					00h	Y/C separation setting 3
#0Fh	W/R	YCSEP_SEL	COMBF_TH2[2:0]			COMBF_TH3[1:0]	ADP_TH2[1:0]			80h	Y/C separation setting 4
#10h	W/R	(res)								00h	—
#11h	W/R	(res)								00h	—
#12h	—	(res)								—	—
#13h	—	(res)								—	—
#14h	W/R	VSMSEL[1:0]		VSDSEL[1:0]		VSI SEL	HSW SEL	ANF SEL	STD SEL	C2h	Synchronous detection setting 1
#15h	W/R	VSO SEL	(res)		VS DWD	VS DET1	VSDET2[2:0]			0Ah	Synchronous detection setting 2
#16h	W/R	SYNC TH	FID AINV	(res)	PXALM	(res)				0Fh	Synchronous detection setting 3
#17h	W/R	(res)								0Dh	—
#18h	W/R	DAFC_GAIN [1:0]		DAFC_VTR	AFC_PLL	LD_DT	AFC_IP	AFC_MODE[1:0]		D4h	AFC setting
#19h	W/R	ATSYC	SYCTH[6:0]							9Fh	Horizontal synchronization detection setting
#1Ah	W/R	(res)		VSYCTH[5:0]						00h	Vertical synchronization detection setting
#1Bh	W/R	HSDLY[7:0]								00h	HSYNC position setting
#1Ch	W/R	HVLDST[3:0]				HVLDSP[3:0]				00h	HVALID position setting
#1Dh	W/R	VVLDST[3:0]				VVLDSP[3:0]				00h	VVALID position setting 1
#1Eh	W/R	VVLD_BO[1:0]		VVLD_SO[1:0]		VVLD_BE[1:0]		VVLD_SE[1:0]		00h	VVALID position setting 2
#1Fh	W/R	(res)	SEP_S_DLY[6:0]							00h	Separate SYNC position adjustment

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#20h	W/R	AGC_FT [1:0]		(res)	LOSET_ E	(res)				41h	AGC setting
#21h	W/R	AGC_REF[7:0]								00h	AGC reference
#22h	W/R	(res)								00h	—
#23h	W/R	LGAIN_ WTPK	LGAIN_ CG	(res)						84h	Luminance output level adjustment 1
#24h	W/R	(res)			WTPKC_SEL [1:0]	PED_LV_LMT [2:0]				00h	Luminance output level adjustment 2
#25h	W/R	PRE_ FIL	APTR_FIL [1:0]		CORING_SEL [1:0]	APTR_FIL_WT [2:0]				00h	Luminance output level adjustment 3
#26h	W/R	(res)	CTCNT[5:0]						(res)	00h	Contrast adjustment
#27h	W/R	(res)	LOSET_LV[6:0]							00h	Luminance offset adjustment 1
#28h	W/R	BRIGHT_LV[7:0]								00h	Luminance offset adjustment 2
#29h	—	(res)								—	—
#2Ah	—	(res)								—	—
#2Bh	—	(res)								—	—
#2Ch	—	(res)								—	—
#2Dh	—	(res)								—	—
#2Eh	—	(res)								—	—
#2Fh	—	(res)								—	—
#30h	W/R	ACC_LF_TM [1:0]		SUB_CRR_OFT [1:0]		PAL_ UVF	UVF_TH[2:0]			00h	ACC, chroma setting
#31h	W/R	ACC_REF[7:0]								00h	ACC reference level
#32h	W/R	(res)	CKIL_ COMP	CKIL_COMP_FLD [1:0]		(res)				60h	Color kill setting 1
#33h	W/R	CKIL_ MD	CKIL TH[1:0]		CKIL_ PHS	CKIL_ TV	CKIL_ YCS1	CKIL_ YCS2	CKIL_ YCS3	60h	Color kill setting 2
#34h	W/R	(res)	CKIL_ PHL	CKIL_TH1[1:0]		CKIL_TH2[1:0]		CKIL_TH3[1:0]		94h	Color kill setting 3
#35h	W/R	HUE_CNT[7:0]								00h	HUE setting 1
#36h	W/R	U_LV_CNT[6:0]							(res)	00h	U level setting
#37h	W/R	V_LV_CNT[6:0]							(res)	00h	V level setting
#38h	W/R	BST_FBG_STA[3:0]				BST_FBG_END[3:0]				80h	Burst period adjustment
#39h	W/R	BST_ FBG	(res)	BST_LCK_RG [1:0]		BST_UNLCK [1:0]		BST_LCK [1:0]		00h	Burst lock adjustment
#3Ah	W/R	HUE_ CNT2	(res)							00h	HUE setting 2
#3Bh	W/R	HUE_CNT3								00h	HUE setting 3
#3Ch	—	(res)								—	—
#3Dh	—	(res)								—	—
#3Eh	—	(res)								—	—
#3Fh	—	(res)								—	—

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#40h	W/R	BB_GDSEL	BB_FMODE	BB_CSEL	HLCK_DET1 [1:0]		(res)	HLCK_DET2 [1:0]		89h	Free-running synchronization output setting 1
#41h	W/R	BB_DSEL[1:0]		(res)						00h	Free-running synchronization output setting 2
#42h	W/R	BB_Y[7:0]								26h	Free-running synchronization output setting 3
#43h	W/R	BB_Cb[7:0]								5Ah	Free-running synchronization output setting 4
#44h	W/R	BB_Cr[7:0]								ECh	Free-running synchronization output setting 5
#45h	—	(res)								—	—
#46h	—	(res)								—	—
#47h	—	(res)								—	—
#48h	W/R	STATUS_SEL[3:0]				(res)				00h	STATUS output setting
#49h	—	(res)								—	—
#4Ah	—	(res)								—	—
#4Bh	—	(res)								—	—
#4Ch	W/R	(res)								00h	—
#4Dh	—	(res)								—	—
#4Eh	—	(res)								—	—
#4Fh	—	(res)								—	—
#50h	W/R	ANG_AMPE	ANG_AGCS	ANG_GAIN	(res)	ADC_CH_SEL[3:0]				A4h	Analog setting 1
#51h	W/R	(res)	AGC_OVF	ANG_GAIN_SET1[5:0]						7Fh	Analog setting 2
#52h	W/R	(res)	CLP_CS[2:0]			(res)		CLP_VS[1:0]		44h	Analog setting 3
#53h	W/R	(res)								00h	—
#54h	W/R	(res)								04h	—
#55h	W/R	(res)								F3h	—
#56h	W/R	(res)								00h	—
#57h	W/R	(res)								00h	—
#58h	W/R	(res)								00h	—
#59h	W/R	(res)		ANG_GAIN_SET2[5:0]						3Fh	Analog setting 4
#5Ah	W/R	(res)		ANG_GAIN_SET3[5:0]						3Fh	Analog setting 5
#5Bh	W/R	(res)		ANG_GAIN_SET4[5:0]						3Fh	Analog setting 6
#5Ch	W/R	PLL_EN	PLL_LKSEL	SCFB_SEL	PLL_LL_SEL	PLL_LK_TM	PLL_PH_LMT	PLL_LK_PRCT[1:0]		A0h	HPLL setting 1
#5Dh	W/R	(res)	PLL_GAIN_S1[2:0]			(res)	PLL_GAIN_S2[2:0]			00h	HPLL setting 2
#5Eh	—	(res)								—	—
#5Fh	—	(res)								—	—

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#60h	W/R	VBID_DT	(res)							00h	VBID detection setting
#61h	W/R	(res)								86h	—
#62h	W/R	C.C_DT_LV[2:0]			C.C_ODT_LSET[4:0]					00h	C.C. detection 1
#63h	W/R	(res)			C.C_EDT_LSET[4:0]					00h	C.C. detection 2
#64h	W/R	(res)			CGMS_DT_LV[2:0]			CGMS_ODT_LSET[1:0]		00h	CGMS detection 1
#65h	W/R	(res)						CGMS_EDT_LSET[1:0]		00h	CGMS detection 2
#66h	W/R	VBNS_DT_LV[2:0]			(res)					00h	VBNS detection
#67h	W/R	(res)								00h	—
#68h	W/R	(res)			WSS_DT_LV[2:0]			WSS_ODT_LSET[1:0]		00h	WSS data detection
#69h	W	(res)	RST_C.C_O	RST_C.C_E	RST_CGMS_O	RST_CGMS_E	(res)		RST_WSS	00h	VBID detection reset setting
#6Ah	—	(res)								—	—
#6Bh	—	(res)								—	—
#6Ch	—	(res)								—	—
#6Dh	—	(res)								—	—
#6Eh	—	(res)								—	—
#6Fh	R	(res)								01h	—
#70h	R	(res)			ST_IFM_DET[4:0]					00h	Status 1
#71h	R	ST_NSCB_M2	ST_NSCB_M1	ST_SD_DT	ST_VBID_DT	ST_VTR_DT	ST_AFC_MT	ST_HLCK_DT	ST_PLL_MD	00h	Status 2
#72h	R	VF_NSCB	VF_C.C_O	VF_C.C_E	VF_CGMS_O	VF_CGMS_E	VF_AGC_O	VF_AGC_E	VF_WSS	00h	VBID flag
#73h	R	C.C_O_DT2[7:0]								00h	C.C ODD data 2
#74h	R	C.C_O_DT1[7:0]								00h	C.C ODD data 1
#75h	R	C.C_E_DT2[7:0]								00h	C.C EVEN data 2
#76h	R	C.C_E_DT1[7:0]								00h	C.C EVEN data 1
#77h	R	CGMS_O_DT3[7:0]								00h	CGMS ODD data 3
#78h	R	CGMS_O_DT2[7:0]								00h	CGMS ODD data 2
#79h	R	C.C_O_P1_ER	C.C_O_P2_ER	(res)	CGMS_O_CRC_ER	CGMS_O_DT1[3:0]				00h	CGMS ODD data 1
#7Ah	R	CGMS_E_DT3[7:0]								00h	CGMS EVEN data 3
#7Bh	R	CGMS_E_DT2[7:0]								00h	CGMS EVEN data 2
#7Ch	R	C.C_O_P1_ER	C.C_O_P2_ER	(res)	CGMS_O_CRC_ER	CGMS_E_DT1[3:0]				00h	CGMS EVEN data 1
#7Dh	R	WSS_DG2[1:0]		WSS_DG3[2:0]			WSS_DG4[2:0]			00h	WSS data
#7Eh	R	WSS_P_ER	(res)	WSS_DG1[3:0]				WSS_DG2[1:0]		00h	WSS data
#7Fh	R	NSS_D	VBNS_D	VBNS_OP	NSCB_OP	NSCB_MOD	(res)	CCOP[1:0]		00h	Copy guard status

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#80h	W/R	(res)	SD_MSK	TV_MSK	VBID_MSK	VTR_MSK	AFC_MSK	HLOCK_MSK	PLLMD_MSK	FFh	Interruption mask setting 1
#81h	W/R	(res)	SD_INT	TV_INT	VBID_INT	VTR_INT	AFC_INT	HLOCK_INT	PLLMD_INT	00h	Interrupt status 1
#82h	W/R	(res)								FFh	—
#83h	W/R	(res)								00h	—
#84h	W/R	PLL_FREQ[7:0]								AAh	HPLL setting 3
#85h	W/R	PLL_FREQ[15:8]								AAh	HPLL setting 4
#86h	W/R	PLL_FREQ[23:16]								AAh	HPLL setting 5
#87h	W/R	PLL_FREQ[31:24]								42h	HPLL setting 6
#88h	W/R	SAMPLE_PIXEL[7:0]								00h	Sampling frequency setting 1
#89h	W/R	(res)					SAMPLE_PIXEL[10:8]			00h	Sampling frequency setting 2
#8Ah	W/R	DEHST[7:0]								00h	Sampling frequency setting 3
#8Bh	W/R	DEHWD[7:0]								00h	Sampling frequency setting 4
#8Ch	W/R	(res)					DEHWD[10:8]			00h	Sampling frequency setting 5
#8Dh	W/R	SYNCTIP[7:0]								00h	Sampling frequency setting 6
#8Eh	W/R	PEDESTAL[7:0]								00h	Sampling frequency setting 7
#8Fh	W/R	(res)							OSC_SEL	00h	Reference clock setting
#90h	W/R	(res)								—	—
#91h	W/R	(res)								—	—
#92h	W/R	(res)								—	—
#93h	W/R	(res)								—	—
#94h	W/R	(res)								—	—
#95h	W/R	(res)								—	—
#96h	W/R	(res)								—	—
#97h	W/R	(res)								—	—
#98h	W/R	(res)								—	—
#99h	R	(res)								—	—
#9Ah	R	(res)								—	—
#9Bh	R	(res)								—	—
#9Ch	R	(res)								—	—
#9Dh	—	(res)								—	—
#9Eh	—	(res)								—	—
#9Fh	—	(res)								—	—

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#A0h	W/R	(res)								00h	–
#A1h	W/R	(res)								00h	–
#A2h	W/R	(res)								00h	–
#A3h	W/R	(res)								00h	–
#A4h	W/R	(res)								00h	–
#A5h	–	(res)								–	–
#A6h	–	(res)								–	–
#A7h	–	(res)								–	–
#A8h	W/R	(res)								00h	–
#A9h	–	(res)								–	–
#AAh	–	(res)								–	–
#ABh	–	(res)								–	–
#ACh	–	(res)								–	–
#ADh	–	(res)								–	–
#AEh	–	(res)								–	–
#AFh	W/R	(res)								00h	–
#B0h	W/R	(res)								39h	–
#B1h	W/R	(res)								F0h	–
#B2h	W/R	(res)								DCh	–
#B3h	W/R	(res)								C8h	–
#B4h	W/R	(res)								B4h	–
#B5h	W/R	(res)								13h	–
#B6h	W/R	(res)								15h	–
#B7h	W/R	(res)								1Fh	–
#B8h	W/R	(res)								21h	–
#B9h	W/R	(res)								00h	–
#BAh	–	(res)								–	–
#BBh	–	(res)								–	–
#BCh	–	(res)								–	–
#BDh	–	(res)								–	–
#BEh	–	(res)								–	–
#BFh	–	(res)								–	–

* Addresses from #C0h to #FEh are reserved registers.

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#E0h	–	(res)								–	–
#E1h	–	(res)								–	–
#E2h	–	(res)								–	–
#E3h	–	(res)								–	–
#E4h	–	(res)								–	–
#E5h	–	(res)								–	–
#E6h	–	(res)								–	–
#E7h	–	(res)								–	–
#E8h	–	(res)								–	–
#E9h	–	(res)								–	–
#EAh	–	(res)								–	–
#EBh	–	(res)								–	–
#ECh	–	(res)								–	–
#EDh	–	(res)								–	–
#EEh	–	(res)								–	–
#EFh	–	(res)								–	–
#F0h	–	(res)								–	–
#F1h	–	(res)								–	–
#F2h	–	(res)								–	–
#F3h	–	(res)								–	–
#F4h	–	(res)								–	–
#F5h	–	(res)								–	–
#F6h	–	(res)								–	–
#F7h	–	(res)								–	–
#F8h	–	(res)								–	–
#F9h	–	(res)								–	–
#FAh	–	(res)								–	–
#FBh	–	(res)								–	–
#FCh	–	(res)								–	–
#FDh	–	(res)								–	–
#FEh	–	(res)								–	–
#FFh	W/R	(res)			PDEN	(res)	ISAM	ICYC[1:0]		00h	Register operation setting

14.3 Details of Decoder Section Control Register

14.3.1 Sub Address #00h/Input Signal Format Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#00h	VIF[4:0]					ISPMD[1:0]		AVMD	09h

#00h/bit[7:3] VIF[4:0], video format specification of video input signals

This is valid when the bit[0] AVMD is set to "0". Even when the bit[0] AVMD is set to "1" (automatic discrimination), this setting value is also valid for selecting NTSC-M or NTSC-J.

"00000" : NTSC-M
"00001" : NTSC-J (default)
"00010" : NTSC 443
"00011" : PAL
"00100" : PAL-M
"00101" : PAL-N
"00110" : PAL-Nc
"00111" : PAL-60
"01000" : SECAM
"10000" : 525i
"10001" : 625i
"10010" : 525p
"10011" : 625p
"10100" : WVGA-33.231MHz
"10101" : WVGA-33.333MHz
"10110" : EGA-480
"10111" : EGA-400
"11000" : 525p (Sampling frequency setting mode)
In other than above : Setting prohibited

[Note] In case of using WVGA-33.333MHz sampling when reference clock frequency is 25MHz(#8Fh[0]=1), write 55h to control register #84h to #87h.

525p (Sampling frequency setting mode) can not be discriminated automatically.
Set bit[2:1] ISPMD to "00" and bit[0] AVMD to "0".

#00h/bit[2:1] ISPMD[1:0], Input sampling clock setting

Set the operation mode that is appropriate for the input signal and the sampling clock used.

For COMPOSITE input

"00": NTSC/PAL/SECAM ITU-R BT.601 27 MHz pixel operation (default)

"01": Setting prohibited

"10": NTSC 8fsc 28.6363MHz operation
PAL/SECAM ITU-R BT.601 27MHz operation

"11": Setting prohibited

[Note] When "10" is set, the clock operates on NTSC 8FSC only when the automatic judgment result is NTSC-M/J.

For COMPONENT input

"00": 27MHz pixel operation (default)

"01": WVGA(analog RGB) 33.231MHz pixel operation

"10": WVGA(analog RGB) 33.333MHz pixel operation

"11": EGA(analog RGB) 9.582167/7.993006MHz pixel operation

[Note] Automatic judgment is available only when "00" is set.

#00h/bit[0] AVMD, Automatic video mode setting

When the sampling frequency of an input signal is ITU-R BT.601, automatic judgment is executed.

"0": fixed mode (bit[7:3] VIF[4:0] register is effective)

"1": automatic discrimination mode (default)

For COMPOSITE/S-VIDEO input

Automatic judgment is available only when the bit[2:1] ISPMD is "00".

Discrimination between NTSC-M and NTSC-J is based on the bit[7:4] VIF[4:0] register.

For COMPONENT input

Automatic judgment is available only when the bit[2:1] ISPMD is "00".

For EGA(400x234 or 480x234), WVGA inputs, set input format (bit[7:3] VIF[4:0]) and sampling clock frequency(bit[2:1] ISPMD[1:0]) registers.

14.3.2 Sub Address #01h/ Component Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#01h	(res)	(res)	SETUP_IRE	SYNC_IRE	HS_INV	VS_INV	SEP_S_MD[1:0]		10h

#01h/bit[7] Not defined
Set “0” (initial value).

#01h/bit[6] Not defined
Set “0” (initial value).

#01h/bit[5] SETUP_IRE, 7.5IRE Setup selection
Setup selection for component input.
Valid only for YPbPr input.
“0” : No setup (default) / “1” : 7.5 IRE setup

#01h/bit[4] SYNC_IRE, 40/43IRE selection
SYNC depth selection for component input.
“0” : 40 IRE / “1” : 43 IRE (300mV) (default)

#01h/bit[3] HS_INV, Separate CHSI polarity selection
Polarity selection of CHSI for digital separate SYNC or composite SYNC.
“0” : Negative logic (default) / “1” : Positive logic

#01h/bit[2] VS_INV, Separate VSI polarity selection
Polarity selection of VSI for separate SYNC.
“0” : Negative logic (default) / “1” : Positive logic

#01h/bit[1:0] SEP_S_MD, Separate SYNC selection
Selection of the SYNC input method for RGB input.
“00”: Sync on Green (default)
“01”: Analog Composite Sync
“10”: Digital Separate Sync
“11”: Digital Composite Sync

14.3.3 Sub Address #02h/ Input Mode Automatic Judgment Mask Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#02h	(res)	VMSK-NTSC-443	(res)	VMSK-PAL-M	VMSK-PAL-N	VMSK-PAL-Nc	VMSK-PAL-60	VMSK-SECAM	5Fh

#02h/bit[7] Not defined
Set "0" (initial value).

#02h/bit[6] VMSK-NTSC-443
Used to mask unnecessary modes when an input video signal mode should be automatically selected. This register is for NTSC-443.

"0": Perform judgment/ 1: Mask (default)

#02h/bit[5] Not defined
Set "0" (initial value).

#02h/bit[4] VMSK-PAL-M
Used to mask unnecessary modes when an input video signal mode should be automatically selected. This register is for PAL-M.

"0": Perform judgment / "1": Mask (default)

#02h/bit[3] VMSK-PAL-N
Used to mask unnecessary modes when an input video signal mode should be automatically selected. This register is for PAL-N.

"0": Perform judgment / "1": Mask (default)

#02h/bit[2] VMSK-PAL-Nc
Used to mask unnecessary modes when an input video signal mode should be automatically selected. This register is for PAL-Nc.

"0": Perform judgment / "1": Mask (default)

#02h/bit[1] VMSK-PAL-60
Used to mask unnecessary modes when an input video signal mode should be automatically selected. This register is for PAL-60.

"0": Perform judgment / "1": Mask (default)

#02h/bit[0] VMSK-SECAM
Used to mask unnecessary modes when an input video signal mode should be automatically selected. This register is for SECAM.

"0": Perform judgment / "1": Mask (default)

[Note] Since trying to perform automatic judgment for both NTSC-443 and PAL-60 makes correct judgment impossible, mask either of them.

14.3.4 Sub Address #03h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#03h	(res)								00h

#03h/bit[7:0] Not defined
Set "0" (initial value).

14.3.5 Sub Address #04h/ Output format selection 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#04h	CLK_INV	C2_SEL	YC_INV	DO_DRV	(res)	OUT_MODE[2:0]			08h

#04h/bit[7] CLK_INV, Output clock setting
Inverts the clock output logic.

"0": Negative logic (data synchronizes to the clock fall)(default)
"1": Positive logic (data synchronizes to the clock rise)

#04h/bit[6] C2_SEL, Chroma output format setting
This register sets the chroma data output format.

"0": offset binary (default) /"1": 2's complement

#04h/bit[5] YC_INV, Output data bit inversion setting
Inverts the Y and C data order.

"0": Cb, Y, Cr, Y, …… (default) / "1": Y, Cb, Y, Cr, ……

#04h/bit[4] DO_DRV, Data output driver selection
Selects the driving capacity of the output driver.

"0": 4mA drive (default) /"1": 2mA drive

#04h/bit[3] Not defined
Set to "1".

#04h/bit[2:0] OUT_MODE[2:0], Output format setting
Sets the data output format.

#04h[2:0]	Output mode
000	BT.656 8bit
001	BT.601 8bit
010	Not defined
100	Not defined
101	Not defined
110	Not defined
etc.	BT.656 8bit

14.3.6 Sub Address #05h/ Output format selection 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#05h	LIMIT	BLANK_ MASK	(res)	FIELD_ INV	CbCr_ EDG	CbCr_ TIM	CLK_SEL	DDR_ MODE	02h

#05h/bit[7] LIMIT, Output data limiter setting

Selects the output data limit range.

For the BT.656 output, “0” and “255” are not output other than at EAV and SAV even when unrestricted.

“0”: OFF Unrestricted. Luminance data: 0...255 / Color difference data: 0...255 (default)

“1”: ON Restricted. Luminance data: 16...235 / Color difference data: 16...240

#05h/bit[6] BLANK_MASK, Blank interval mask setting

Masks (black level) the blank interval data.

“0”: Through (default)

“1”: Mask

#05h/bit[5] Not defined

Set to “0”.

#05h/ bit[4] FIELD_INV, Output field selection

For the BT.656 output, selects the output field signal logic.

“0”: ODD=“L”, EVEN=“H” (default)

“1”: EVEN=“L”, ODD=“H

#05h/ bit[3] CbCr_EDGE, CbCr reference selection

For the BT.656 output, selects either EAV or SAV as the reference of color difference data Cb/Cr.

“0”: SAV as the reference (default) / “1”: EAV as the reference

#05h/ bit[2] CbCr_TIM, CbCr output phase selection

Selects the phase of color difference data Cb/Cr.

“0”: Cb, Cr, Cb, Cr, … (default) /”1”: Cr, Cb, Cr, Cb, …

#05h/ bit[1] CLK_SEL, Output clock frequency selection

Selects the clock frequency.

“0”: 1x speed clock output / “1”: 2x speed clock output (default)

#05h/bit[0] DDR_MODE, DDR output enable

DDR mode enable setting for output data.

“0”: DDR mode off (default) / “1”: DDR mode on

14.3.7 Sub Address #06h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#06h	(res)								00h

#06h/bit[7:0] Not defined

Set “00h” (initial value).

14.3.8 Sub Address #07h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#07h	(res)								E4h

#07h/bit[7:0] Not defined

Set “E4h” (initial value).

Sub Address #08h/Internal Operation Mode Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#08h	(res)	(res)	FIFOMD[1:0]		(res)	(res)			00h

#08h bit[7] Not defined
Set "0" (initial value).

#08h/bit[6] Not defined
Set "0" (initial value).

#08h/bit[5:4] FIFOMD[1:0], FIFO mode to correct the number of pixels
In FIFO mode, the number of pixels for each 1H is output based on the standard value even in the asynchronous sampling mode. In that case, FIFO is reset at the latter part of every field where the positions of the memory reset are different between FIFO1 mode and FIFO2 mode. In FM mode, the result of decode is output as the original following the SYNC signal.

"00": Use FIFO1 internal memory: with correction of the number of pixels
FIFO reset position is immediately after the falling of VVALID (default)
"01": Use FIFO2 internal memory: with correction of the number of pixels
FIFO reset position is automatically adjusted based on the error of the number of pixels
"10": FM FIFO through mode: without correction of the number of pixels
"11": Setting prohibited

#08h/bit [3:0] Not defined
Set "0" (initial value).

14.3.9 Sub Address #09h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#09h	(res)								00h

#09h/bit[7:0] Not defined
Set “00h” (initial value).

14.3.10 Sub Address #0Ah/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Ah	(res)								00h

#0Ah/bit[7:0] Not defined
Set “00h” (initial value).

14.3.11 Sub Address #0Ch/ Y/C Separation Setting 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Ch	(res)	YC_SFM[2:0]			(res)	COMBF_TH[2:0]			00h

#0Ch/bit[7] Not defined
Set "0" (initial value).

#0Ch/bit[6:4] YC_SFM[2:0], Y/C separation filter setting
Filter that separates the composite video data into the luminance data (Y) and the color difference data (C).

"000": [NTSC] adaptive filter/[PAL] adaptive filter (default)
Filter that adaptively selects the two-line comb, the three-line comb (two-line in PAL), or the trap filter based on the line-to-line correlation. Y/C separation characteristics will be improved in both the horizontal and vertical directions.

"001": [NTSC] three-line comb filter/[PAL] two-line comb filter
Filter with high-quality Y/C separation characteristics in the vertical direction.

"010": [NTSC] trap filter/[PAL] trap filter
Filter with high-quality Y/C separation characteristics in the horizontal direction.

"011": [NTSC] three-line comb or trap adaptive filter/[PAL] setting prohibited
Filter that adaptively selects a filter based on the line-to-line correlation.
Y/C separation characteristics will be improved in both the horizontal and vertical directions.

"100": Setting prohibited

"101": Setting prohibited

"110": Setting prohibited

"111": Setting prohibited

[Note] Operates with a trap filter fixed when the input is SECAM.

YC_SFM [6:4]	NTSC Y/C separation method	PAL Y/C separation method
*000	Adaptive filter	Adaptive filter
001	Three-line comb filter	Two-line comb filter
010	Trap filter	Trap filter
011	Three-line comb or trap adaptive filter	Setting prohibited
100	Setting prohibited	Setting prohibited
101	Setting prohibited	Setting prohibited
110	Setting prohibited	Setting prohibited
111	Setting prohibited	Setting prohibited

#0Ch/bit[3] Not defined
Set "0" (initial value).

#0Ch/bit[2:0] COMBF_TH[2:0], PAL adaptive transition filter threshold setting

This register is enabled when the PAL adaptive transition filter or comb filter is selected.
The adaptive type filter works more like a comb filter in the plus direction and more like a trap filter in the minus direction, regardless of the line-to-line correlation.
The non-adaptive type filter always works as a comb filter in the plus direction, as a trap filter in the minus direction, and as the filter with their average characteristics in the middle.

"011": +3 (advantage comb filter)
|
"000": 0 (default)
|
"100": -4 (advantage trap filter)

14.3.12 Sub Address #0Dh/ Y/C Separation Setting 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Dh	(res)			LUMED	(res)	(res)			00h

#0Dh/bit[7:5] Not defined
Set "0" (initial value).

#0Dh/bit[4] LUMED, Luminance edge detection
Selects the Y/C separation method (initial value) at the start of the valid horizontal period.
This setting is enabled when the #0Ch YC_SFM[2:0] is set to "000".

"0": Comb filter (default) / "1": Trap filter

#0Dh/bit [3:0] Not defined
Set "0" (initial value).

14.3.13 Sub Address #0Eh/ Y/C Separation Setting 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Eh	(res)	ADP_TH[1:0]		(res)					00h

#0Eh/bit[7] Not defined
Set "0" (initial value).

#0Eh/bit[6:5] ADP_TH, Y/C separation correlation judgment threshold
Threshold value of correlation judgment.
The larger the value of judgment threshold, the easier there is correlation.

"01": 3 Easy to judge to be in correlation
"00": 2
"10": 1 (default)
"11": 0 Easy to judge not to be in correlation

#0Eh/bit[4:0] Not defined
Set "0" (initial value).

14.3.14 Sub Address #0Eh/ Y/C Separation Setting 4 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Fh	YCSEP_SEL		COMBF_TH2[2:0]		COMBF_TH3[1:0]		ADP_TH2[1:0]		80h

#0Fh/bit[7] YCSEP_SEL, Y/C separation method selection.

"0" : Select filter by correlation between composite signal and signal through after comb filter and trap filter processing.
This is adopted only when #0Ch/bit[6:4] YC_SMF[2:0]="000" for NTSC.

"1" : Select filter by correlation between chrominance signal and signal through after comb filter and trap filter processing. (default)

#0Fh/bit[6:4] COMBF_TH2[2:0], Y/C separation correlation judgment threshold 2

Threshold value of correlation judgment when YCSEP_SEL is set to "0".
Judge correlation of chrominance signal
Switches comb filter, trap filter select region based on setting value.

"011": +3 (advantage comb filter)
|
"000": 0 (default)
|
"100": -4 (advantage trap filter)

#0Fh/bit[3:2] COMBF_TH3[1:0], Y/C separation correlation judgment threshold 3

Threshold value of correlation judgment when YCSEP_SEL is set to "0".
Judge correlation of subcarrier amplitude.
Switches comb filter, trap filter select region based on setting value.

"00": 0 (advantage comb filter) (default)
"01": 1
"10": 2
"11": 3 (advantage trap filter)

#0Fh/bit[1:0] ADP_TH2[1:0], Y/C separation correlation judgment threshold 4

Threshold value of correlation judgment when YCSEP_SEL is set to "0".
Judge correlation of luminance signal of vertical direction.
Switches comb filter, trap filter select region based on setting value.

"01": 3 (advantage comb filter)
"10": 2
"00": 1 (default)
"11": 0 (advantage trap filter)

14.3.15 Sub Address #10h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#10h	(res)								00h

#10h/bit[7:0] Not defined
Set “00h” (initial value).

14.3.16 Sub Address #11h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#11h	(res)								00h

#11h/bit[7:0] Not defined
Set “00h” (initial value).

14.3.17 Sub Address #14h/ Synchronization Detection Setting 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#14h	VSMSEL[1:0]		VSDSEL[1:0]		VSISEL	HSWSEL	ANFSEL	STDSEL	C2h

#14h/bit[7:6] VSMSEL[1:0], Selection of the VSYNC internal processing mode

[Recommended] The setting VSMSEL="11" is recommended when the light electric field state need not be considered.

"00" : Free-running VSYNC output when the light electric field detection is enabled, otherwise input VSYNC output

"01" : Input VSYNC output when VTR detection is enabled, otherwise free-running VSYNC output

"10" : Input VSYNC output when VTR, unilateral field detection is enabled, otherwise free-running VSYNC output

"11" : Input VSYNC output (default)

#14h/bit[5:4] VSDSEL[1:0], Selection of the number of VSYNC update continuous detection

Under the setting of #41h bit[7:6] BB_DSEL="10" "11" when in the free-running synchronization output, sets the sensitivity for the VSYNC output signal to follow the input signal. The smaller the detection sensitivity value (field number) is, the more easily the VSYNC output signal follows the input signal.

"00" : 2 fields (default)
"01" : 1 field
"10" : 4 fields
"11" : 3 fields

[Note] Sufficient evaluation need to be taken into account when using in the light electric field. The smaller the detection sensitivity value (number of fields) is, the more easily the VSYNC output signal follows the input signal. However, the video stability may be lost when the VSYNC is erroneously detected in the noisy situation or light electric field.

#14h/bit[3] VSISEL, VSYNC forced insertion switching

When the input VSYNC signal cannot be detected, the VSYNC is automatically generated internally. When the free-running VSYNC output condition is not met under the #14h bit[7:6] VSMSEL condition, the free-running VSYNC is forcibly output if this setting is ON. (Free-running VSYNC: VSYNC signal being generated at the internal counter)

"0": Forced insertion ON (default)/"1": Forced insertion OFF

#14h/bit[2] HSWSEL, HSYNC detection window setting

Setting related to the HSYNC detection. Sets to "1" when the signal condition is bad such as in the light electric field.

Sets the detection range when the following HSYNC is detected:

"0": ±80cycle (default) / "1": ±20cycle

#14h/bit[1] ANFSEL, Setting of anti-noise filter automatic switching

Sets the anti-noise filter automatic switching. Turning it to ON is effective when the light electric field signal is input. Detects the noise and switches the filter automatically.

"0": Automatic switching ON / "1": Automatic switching OFF (default)

#14h/bit[0] STDSEL, Switching of sync-chip detection method

Sets the sync-chip level detection cycle.

"Automated switching" is effective for the signal whose line cycle is not shifted, such as a standard signal "Fixed switching" is effective for the signal whose line cycle is shifted, such as VTR.

"0": Automatic switching (default) / "1" : Fixed switching (2048)

14.3.18 Sub Address #15h/ Synchronization Detection Setting 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#15h	VSOSEL	(res)		VSDWD	VSDET1	VSDET2[2:0]			0Ah

#15h/bit[7] VSOSEL, VSYNC output timing setting
Setting to “1” is more stable when decoding the nonstandard signal.

“0”: VSYNC_L is output in synchronous with HSYNC_L.(default)
“1”: VSYNC_L is output at the point when the input signal's VSYNC is detected.

#15h/bit[6:5] Not defined
Set “0” (initial value).

#15h/bit[4] VSDWD, VSYNC detection window setting
Setting related to the VSYNC detection.
Sets the presence/absence of the detection range when the following VSYNC is detected:

“0”: Mode that is resistant to nonstandard signal since the VSYNC prediction is performed.(default)
“1”: Operate assuming the point when VSYNC is detected as the VSYNC.

#15h/bit[3] VSDET1, VSYNC detection mode setting 1
Sets the VSYNC detection mode in the PLL, AFC (Auto Frequency Control) operation status.
[Recommended] The setting VSDET1=“1” is recommended when the light electric field state need not be considered.

“0”: Generate VSYNC by the internal counter even when the VSYNC is not detected for the certain protection period.
“1”: Operate assuming the point when VSYNC is detected as the VSYNC. (default)

#15h/bit[2:0] VSDET2[2:0], VSYNC detection mode setting 2
Sets the VSYNC detection condition.
Adjust the setting when the VSYNC is erroneously detected because of the light electric field or other reasons.

“111”: 7 Detection sensitivity is strong (easy to detect VSYNC signal)
|
“010”: 2 (default)
|
“000”: 0 Detection sensitivity is weak (hard to detect VSYNC signal)

14.3.19 Sub Address #16h/ Synchronization Detection Setting 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#16h	SYNCTH	FIDAINV	(res)	PXALM	(res)				0Fh

#16h/bit[7] SYNCTH, selection of the SYNC threshold criteria
Switches threshold generation for SYNC detection.

"0": Refer to the SYNC depth (default) / "1": Refer to the AGC gain

#16h/bit[6] FIDAINV, field signal automatic toggle mode
Mode in which a field signal is automatically toggled when a unilateral field signal is input.
A field signal is inverted for every field when fields are continuous.

"0": OFF (default) / "1": ON

#16h/bit[5] Not defined
Set "0" (initial value).

#16h/bit[4] PXALM, setting of the pixel position correction
Corrects the line-to-line sampling phase shift which occurs in the asynchronous sampling.

"0": Pixel position correction is performed.(default)

"1": Pixel position correction is not performed.

#16h/bit [3:0] Not defined
Set "1111" (initial value).

14.3.20 Sub Address #17h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#17h	(res)								0Dh

#17h/bit[7:0] Not defined
Set "0Dh" (initial value).

14.3.21 Sub Address #18h/ AFC Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#18h	DAFC_GAIN[1:0]		DAFC_ VTR	AFC_ PLL	LD_DT	AFC_IP	AFC_MODE[1:0]		D4h

#18h/bit[7:6] DAFC_GAIN[1:0], DAFC feedback gain adjustment

Sets the following gain of the digital AFC (Digital Auto Frequency Control).
The greater the setting value is, the more easily the follow can be performed for the horizontal synchronization shift at the light electric field.

"00": 1 time

"01": 2 times

"10": 4 times

"11": 6 times (default)

#18h/bit[5] DAFC_VTR, AFC operation selection at VTR detection

Input with great volatility such as VTR signal may not be followed by the AFC (Auto Frequency Control). In that case, turn off the AFC.

"0": Turn OFF the digital AFC (default) / "1": Do not turn OFF the digital AFC

[Note] The video may be disturbed horizontally when the VTR signal is input with the setting of "1".

#18h/bit[4] AFC_PLL, Selection of the AFC operation

This register switches the AFC operation mode.
When "0" is set, the digital AFC always operates if the analog AFC is not operating.
When "1" is set, the digital AFC operates if the analog AFC is not operating and the number of pixels per line changes frequently.

"0": AFC always operates

"1": ON when the number of pixels per line changes frequently (default)

#18h/bit[3] LD_DT, Selection of the Laser Disk device pause detection

This register turns off the analog/digital AFC when the LD player pause is detected.

"0": Do not turn off the AFC (default) / "1": Turn off the AFC

#18h/bit[2] AFC_IP, Selection of the pixel position correction when AFC is functioning

Selects whether the pixel position correction is performed at AFC (Auto Frequency Control) operation.
[Recommended] The recommended setting value of this register is "1".

"0": OFF / "1": ON (correction is performed)(default)

#18h/bit[1:0] AFC_MODE, Selection of the AFC operation mode

Selects the AFC (Auto Frequency Control) automatic on/off.
Operates the AFC when the number of pixels per line in the input signal changes frequently or when the input signal is judged to be a standard signal.

"00": AFC OFF (default)

"01": Analog AFC off, digital AFC automatic on/off

"10": Analog AFC automatic on/off, digital AFC off

"11": Analog AFC automatic on/off, digital AFC automatic on/off

14.3.22 Sub Address #19h/ Horizontal Synchronization Detection Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#19h	ATSYC	SYCTH[6:0]							9Fh

#19h/bit[7] ATSYC, SYNC detection level method setting

When in the register control, sets the SYNC detection level based on bit[6:0] SYCTH[6:0].
When in the automatic control, automatically sets the area around the center of SYNC level to the threshold.

"0": Register control

"1": Automated control (default)

#19h/bit[6:0] SYCTH[6:0], SYNC detection level setting

Sets SYNC detection level.
Adjusts when synchronization is disturbed due to noise or when the signal level changes.
The IRE notation below shows the case when the standard signal is input whose synchronization signal is 40IRE.

At bit[7] ATSYC="0"

"111_1111": 127 Approximately 48 IRE

|

"001_1111": 31 Approximately 12 IRE (default)

|

"000_0000": 0 0 IRE

At bit[7] ATSYC="1"

"111_1xxx": 15 Approximately 31 IRE

|

"001_1xxx": 3 Approximately 25 IRE (default)

|

"000_0xxx": 0 Approximately 23 IRE

14.3.23 Sub Address #1Ah/ Vertical Synchronization Detection Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Ah	(res)		VSYCTH[5:0]						00h

#1Ah/ bit[7:6] Not defined

Set "0" (initial value).

#1Ah/bit[5:0] VSYCTH[5:0], VSYNC detection level setting

Sets VSYNC detection level to the #19h bit[6:0] SYCTH [6:0] register setting.
Used when the signal condition is bad such as in the light electric field. The level does not drop below the SYNC-chip level.

"11_1111" : -63 -25IRE

|

"00_ 0000" : 0 0IRE (default)

14.3.24 Sub Address #1Bh/Horizontal Synchronization Signal Output Position Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Bh	HSDLY[7:0]								00h

#1Bh/bit[7:0] HSDLY[7:0], HSYNC output position adjustment

This register adjusts the position of the horizontal synchronization signal HSYNC (internal signal), which is detected in the analog video input.
Normally, it can be used with the default state.

"0111_1111": +127 pixel
|
"0000_0000": 0 pixel (default)
|
"1000_0000": -128 pixel

14.3.25 Sub Address #1Ch/ Horizontal Valid Data Area (HVALID) Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Ch	HVLDST[3:0]				HVLDSP[3:0]				00h

#1Ch/ bit[7:4] HVLDST[3:0], HVALID Start position adjustment

This register is used to adjust the rise position of the horizontal valid data period HVALID (internal signal), detected in the analog video input.
Normally, it can be used with the default state.

"0111" : +7 pixel
|
"0000" : 0 pixel (default)
|
"1000" : -8 pixel

#1Ch/ bit[3:0] HVLDSP[3:0], HVALID Stop position adjustment

This register is used to adjust the fall position of the horizontal valid data period HVALID (internal signal), detected in the analog video input.
Normally, it can be used with the default state.

"0111": +7 pixel
|
"0000": 0 pixel (default)
|
"1000": -8 pixel

14.3.26 Sub Address #1Dh/ Vertical Valid Data Area (VVALID) Adjustment 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Dh	VVLDST[3:0]				VVLDSP[3:0]				00h

#1Dh/ bit[7:4] VVLDST[3:0], VVALID Start position adjustment

This register is used to adjust the rise position of the vertical valid data period VVALID (internal signal) detected in the analog video input. Normally, it can be used with the default state.

"0111": +7 line
|
"0000": 0 line (default)
|
"1000": -8 line

#1Dh/ bit[3:0] VVLDSP[3:0], VVALID Stop position adjustment

This register is used to adjust the fall position of the vertical valid data period VVALID (internal signal) detected in the analog video input. Normally, it can be used with the default state.

"0111": +7 line
|
"0000": 0 line (default)
|
"1000": -8 line

14.3.27 Sub Address #1Eh/ Vertical Valid Data Area (VVALID) Adjustment 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Eh	VVLD_BO[1:0]		VVLD_SO[1:0]		VVLD_BE[1:0]		VVLD_SE[1:0]		00h

#1Eh/ bit[7:6] VVLD_BO[1:0], VVALID ODD Field start position adjustment
This register is used to adjust the VVALID rise position in the ODD field.

"00": 0 line (default)
"01": Rise slower by one line
"10": Rise earlier by one line
"11": Not defined

#1Eh/ bit[5:4] VVLD_SO[1:0], VVALID ODD Field stop position adjustment
This register is used to adjust the VVALID fall position in the ODD field.

"00": 0 line (default)
"01": Fall slower by one line
"10": Fall earlier by one line
"11": Not defined

#1Eh/ bit[3:2] VVLD_BE[1:0], VVALID EVEN Field start position adjustment
This register is used to adjust the VVALID rise position in the EVEN field.

"00": 0 line (default)
"01": Rise slower by one line
"10": Rise earlier by one line
"11": Not defined

#1Eh/ bit[1:0] VVLD_SE[1:0], VVALID EVEN Field stop position adjustment
This register is used to adjust the VVALID fall position in the EVEN field.

"00": 0 line (default)
"01": Fall slower by one line
"10": Fall earlier by one line
"11": Not defined

14.3.28 Sub Address #1Fh/ Separate SYNC Position Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Fh	(res)	SEP_S_DLY[6:0]							00h

#1Fh/bit[7] Not defined
Set “0” (initial value).

#1Fh/ bit[6:0] SEP_SYNC_DLY[6:0], Separate SYNC synchronization signal position adjustment
Adjusts the synchronization signal position for the digital composite SYNC or digital separate SYNC. Normally, it can be used with the default state.

“111_1111”: +127 pixel
|
“000_0000”: 0 pixel (default)

14.3.29 Sub Address #20h/ AGC Control Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#20h	AGC_FT[1:0]		(res)	LOSET_E	(res)				41h

#20h/bit[7:6] AGC_FT[1:0], Luminance digital AGC function convergence time setting

Sets the luminance digital AGC or MGC mode, and the AGC function convergence time.
Digital AGC is the function to set a coefficient automatically as depth of detected SYNC is 40IRE, and to adjust a luminance level automatically. This allows the video to always get the constant luminance data level regardless of the different input level.
The convergence time changes by approximately 4 times for each step from slow through medium to fast.

"00": Slow AGC mode
"01": Medium AGC mode (default)
"10": Fast AGC mode
"11": Setting prohibited

#20h/bit[5] Not defined

Set "0" (initial value).

#20h/bit[4] LOSET_E, Luminance data offset enable

Sets the MGC mode.
The MGC mode is the mode to fix the luminance level with the register regardless of SYNC depth.

"0": MGC OFF (default)
"1": MGC ON

AGC/MGC mode can be categorized as follows based on the combination of bit[7:6] AGC_FT[1:0] and bit[4] LOSET_E:

AGC_FT[1:0]	LOSET_E	Operation
00	0	AGC slow
01	0	AGC medium
10	0	AGC fast
11	0	Inhibit
XX	1	MGC

#20h/bit [3:1] Not defined

Set "0" (initial value).

#20h/bit[0] Not defined

Set "1" (initial value).

14.3.30 Sub Address #21h/ AGC Reference Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#21h	AGC_REF[7:0]								00h

#21h/bit[7:0] AGC_RC[7:0] AGC reference level (two's complement format)

Function to adjust the slope of luminance.
This function adjusts slope with a pedestal level as the starting point.
This setting is enabled in either of the digital AGC mod or MGC mode.
Gain coefficient at AGC mode is approximately (350 + AGC_REF value)/350 times.
Gain coefficient at MGC mode is approximately (227 + AGC_REF value)/227 times.

"0111_1111": Approx. 1.36 times (at AGC), approx. 1.56 times (at MGC)
|
"0000_0000": Approx. 1 time (at AGC), approx. 1.0 times (at MGC) (default)
|
"1000_0000": Approx. 0.63 times (at AGC), approx. 0.44 times (at MGC)

14.3.31 Sub Address #22h/ Reserve Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#22h	(res)								00h

#22h/bit[7:0] Not defined

Set to "00h" (initial value).

14.3.32 Sub Address #23h/ Luminance Output Level Adjustment 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#23h	LGAIN_ WTPK	LGAIN_ CG	(res)						84h

#23h/bit[7] LGAIN_WTPK, Gain adjustment when the luminance level peak detection is performed

Sets the gain adjustment when the luminance level peak detection.

Adjusts the luminance data gain when the luminance level peak detection is performed to prevent saturation of luminance level.

This setting is enabled in AGC mode.

"0": Perform gain adjustment / "1": Do not perform gain adjustment (default)

#23h/bit[6] LGAIN_CG, Gain adjustment when the copy guard signal detection is performed

Sets the luminance level peak detection of the signal to which the analog copy guard signal is added. Adjusts the luminance data gain when the luminance level peak detection is performed to prevent saturation of luminance level.

"0": ON (default) / "1": OFF

#23h/bit[5:0] Not defined

Set to "04h" (initial value).

14.3.33 Sub Address #24h/ Luminance Output Level Adjustment 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#24h	(res)			WTPKC_SEL[1:0]		PED_LV_LMT[2:0]			00h

#24h/bit[7:5] Not defined

Set to "0" (initial value).

#24h/bit[4:3] WTPKC_SEL[1:0], Selection of the white peak convergence time

This register sets the convergence speed when the luminance peak level detection is performed. The convergence speed changes by 2 times for each step from Slow through Medium and Fast to VeryFast. This setting is enabled when Gain adjustment when the luminance level peak detection is performed (#23h bit[7]="0").

This setting is suitable for the signal whose SYNC depth does not reach the reference value (40/43IRE) and for the signal whose luminance exceeds the 100IRE.

"00": Medium (default)

"01": Fast

"10": Very Fast

"11": Slow

#24h/bit[2:0] PED_LV_LMT[2:0], Pedestal level update control

This register sets the pedestal level update threshold. The greater this setting value is, the less susceptible to noise. Enabled when the MGC mode (#20h bit[4]="1").

"000": 0IRE (unrestricted) (default)

"001": 0.5IRE

"010": 1IRE

"011": 2IRE

"100": 3IRE

"101": 3.6IRE

"110": 5.4IRE

"111": 7.2IRE

14.3.34 Sub Address #25h/ Luminance Output Level Adjustment 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#25h	PRE_FIL	APTR_FIL[1:0]		CORING_SEL[1:0]		APTR_FIL_WT[2:0]			00h

#25h/bit[7] PRE_FIL, Sharp filter.

Using the sharp filter emphasizes the luminance frequencies near 3 MHz.

It may be that the peak of the luminance level will be detected in the portion where the luminance level has been raised by emphasis, resulting in lowering the luminance level of the entire image.

"0": OFF (default) / "1": ON

#25h/bit[6:5] APTR_FIL[1:0], Filter for contour correction

Sets the characteristics of the filter for contour correction. Used in combination with the lower bit [4:0] (CORING_SEL[1:0], APTR_FIL_WT[2:0]).

This register chooses the frequency band to emphasize. The frequency of the high area is emphasized as much as the hige range.

"00": range0 (middle) (default)

"01": range1

"10": range2

"11": range3 (high)

#25h/bit[4:3] CORING_SEL[1:0], Level setting for the contour correction

Sets the sensitivity level of the contour correction. Used in combination with the upper bit [6:5] (APTR_FIL[1:0]) and lower bit[2:0](APTR_FIL_WT[2:0]).

By the data finite difference quantity of the next to each other pixel, the register chooses whether or not to emphasize the contour component.

"00": Always emphasized (default)

"01": Emphasis sensitivity is strong

"10": Emphasis sensitivity is medium

"11": Emphasis sensitivity is weak

#25h/bit [2:0] APTR_FIL_WT[2:0], Coefficient setting of filter for contour correction

Sets the emphasis level of the filter for contour correction. Used in combination with the upper bit [6:3] (APTR_FIL [1:0], CORING_SEL[1:0]).

High frequency is emphasized.

"000": Emphasis level 0 (contour correction OFF) (default)

"001": Emphasis level 1

"010": Emphasis level 2

"011": Emphasis level 3

"100": Emphasis level 4

"101": Emphasis level 5

"110": Emphasis level 6

"111": Emphasis level 7 (emphasis level high)

14.3.35 Sub Address #26h/ Contrast Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#26h	(res)	CTCNT[5:0]						(res)	00h

#26h/bit[7] Not defined
Set to "0" (initial value).

#26h/bit[6:1] CTCNT[5:0], Contrast level adjustment function
Adjusts the contrast level. Adjusts the slope with reference to around luminance digital level 128.

"01 1111": 63/32 times
|
"00 0000": 32/32 times (default)
|
"10 0001": 1/32 times
"10 0000": Setting prohibited

#26h/bit[0] Not defined
Set to "0" (initial value).

14.3.36 Sub Address #27/ Luminance Offset Adjustment 1(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#27h	(res)	LOSET_LV[6:0]							00h

#27h/bit[7] Not defined
Set to "0" (initial value).

#27h/bit[6:0] LOSET_LV[6:0], Luminance offset adjustment 1
This register sets the offset value which is added to the luminance level to the pedestal-level.

"011_1111": -7IRE (The luminance level becomes low.)
|
"000_0000": 0IRE (default)
|
"100_0000": +7IRE (The luminance level becomes high.)

[Note] When input is analog RGB, this setting is disabled (set to 0.).

14.3.37 Sub Address #28/ Luminance Offset Adjustment 2(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#28h	BRIGHT_LV[7:0]								00h

#28h/bit[7:0] BRIGHT_LV[7:0], Luminance offset adjustment 2
Adjusts luminance offset level. 1LSB of Luminance (Y) data is adjusted by BRIGHT_LV value.
BRIGHT_LV is set by 2's complement value.

14.3.38 Sub Address #30h/ ACC Loop Filter & Chroma Control (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#30h	ACC_LF_TM[1:0]		SUB_CRR_OFT[1:0]		PAL_UVF	UVF_TH[2:0]			40h

#30h/bit[7:6] ACC_LF_TM[1:0], Chroma digital ACC function convergence characteristics setting

Sets the ACC function convergence time in the chroma digital ACC or MCC mode
Digital ACC is the function to set a coefficient automatically as amplitude of detected burst signal is 40IRE, and to adjust a chroma level automatically. This allows the video to always get the constant chroma data level regardless of the different input level.
The convergence time is 4 times faster when comparing between slow and medium, and 64 times between slow and fast.
In MCC mode, the chroma scaling factor is determined based on the register #31h ACC_REF[7:0] regardless of the burst signal amplitude of the input signal. This operates only CVBS input.

"00": Fast ACC mode
"01": Slow ACC mode (default)
"10": Medium ACC mode
"11": MCC mode

#30h/bit [5:4] SUB_CRR_OFT[1:0], Sub-carrier offset value setting

Function to add an offset value to the sub-carrier.
This prevents the output color from fading when the chroma level is small.

"00": 0 (default)
"01": +2
"10": +4
"11": +8

#30h/bit[3] PAL_UVF, Selecting the usage of UV filter in PAL

Set the usage of UV filter in PAL.

"0": Use (default) Averaging processing is always performed with the previous line in PAL.
"1": Not used Averaging processing is performed according to the setting of bit[2:0] UVF_TH[2:0].

#30h/bit[2:0] UVF_TH[2:0], UV filter threshold setting

Set the threshold of the averaging processing for the U and V data with the previous line.

"000": No averaging (default)
"001": Level difference 4
"010": Level difference 8
"011": Level difference 12
"100": Level difference 16
"101": Level difference 20
"110": Level difference 24
"111": Always performs averaging

14.3.39 Sub Address #31h/ ACC Reference Level Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#31h	ACC_REF[7:0]								00h

#31h/bit[7:0] ACC_REF[7:0], Chroma level adjustment(two's complement format)

Adjusts the chroma level (color level).
Gain coefficient at ACC mode is approximately (44 + ACC_REF value /4) / 44 times.
Gain coefficient at MCC mode is approximately (32 + ACC_REF value /4) / 32 times.

"0111_1111": Approx. 1.7 times (at ACC), approx. 1.97 times (at MCC)
|
"0000_0000": Approx. 1 time (at ACC), approx. 1 time (at MCC) (default)
|
"1000_0000": Approx. 0.27 times (at ACC), approx. 0 times (at MCC)

[Note] In SECAM, all of the 8 bits are significant while in NTSC/PAL, upper 6 bits are significant.

In addition to the above, the level of U and V signals can be adjusted independently using the #36h/bit[7:1] U_LV_CNT[6:0] and #37h/bit[7:1] V_LV_CNT[6:0].

14.3.40 Sub Address #32h/ Color Killer Control 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#32h	(res)	CKIL_ COMP	CKIL_COMP_FLD [1:0]		(res)				60h

#32h/bit[7] Not defined

Set to "0" (initial value).

#32h/bit[6] CKIL_COMP, Color killer enable when component input selected

Enables color killer on switching input signal.
Color killer is available during the period set by CKIL_COMP_FLD after switching input signal.
Color killer operation is enabled only for YPbPr or RGB signals as inputs.

"0":.Output decoded result on switching input signal

"1":.Color killer operation on switching input signal (default)

#32h/bit [5:4] CKIL_COMP_FLD[1:0], Color killer period setting when component input selected

Sets the color killer period on switching input. This is enabled when CKIL_COMP is set to 1.

"00": 8 fields for interlace signal, 8 frames for progressive signal

"01": 16 fields for interlace signal, 16 frames for progressive signal

"10": 20 fields for interlace signal, 20 frames for progressive signal (default)

"11": 24 fields for interlace signal, 24 frames for progressive signal

#32h/bit[3:0] Not defined

Set to "0" (initial value).

14.3.41 Sub Address #33h/ Color Killer Control 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#33h	CKIL_MD	CKIL TH[1:0]		CKIL_ PHS	CKIL_ TV	CKIL_ YCS1	CKIL_ YCS2	CKIL_ YCS3	60h

#33h/bit[7] CKIL_MD, Color killer mode setting

"0" : Automatic color killer mode (default)
Using the setting of the color killer threshold, bit[6:5] CKIL_TH[1:0], output in automatically performed in monochrome based on the color burst signal amplitude level, sub-carrier phase, and TV system automatic judgment.

"1" : Forced color killer mode
Outputs in monochrome by forcibly minimizing the value of the color difference data.

#33h/bit[6:5] CKIL TH[1:0], Color killer threshold

Detection setting in the automated color killer mode, bit[7] CKIL_MD ="0".
When input is NTSC or PAL, the color killer judge level is set as the ratio to the reference color burst signal amplitude level (40IRE). When input is SECAM, the color killer judge level is set as the number of continuous lines.

•In NTSC/PAL input

"00": 12% Color burst level

"01": 6% Color burst level

"10": 3% Color burst level

"11": Color killer off (default)

•In SECAM input

"00": 1-line

"01": 32-line

"10": 64-line (default)

"11": Color killer off (default)

#33h/bit[4] CKIL_PHS, Color killer sub-carrier phase lock judgment

Judges if the sub-carrier phase is locked, and performs the color killer if it is not locked.

"0": OFF (default) / "1": ON [Recommended] Recommended setting value is "0".

#33h/bit[3] CKIL_TV, Color killer TV system judgment

Performs color killer if the TV system automatic judgment cannot make a judgment or during judgment.

"0": OFF (default) / "1": ON [Recommended] Recommended setting value is "0".

#33h/bit[2] CKIL_YCS1, Y/C separation setting 1 during color killer

When the color killer is performed based on the sub-carrier amplitude, Y/C separation is not made. (When Y/C separation is set to OFF)

"0": Y/C separation ON (default) / "1": Y/C separation OFF

[Recommended] Recommended setting value is "0".

#33h/bit[1] CKIL_YCS2, Y/C separation setting 2 during color killer

When the color killer is performed based on the sub-carrier phase, Y/C separation is not made. (When Y/C separation is set to OFF)

"0": Y/C separation ON (default) / "1": Y/C separation OFF

[Recommended] Recommended setting value is "0".

#33h/bit[0] CKIL_YCS3, Y/C separation setting 3 during color killer

When the color killer is performed based on the TV system automatic judgment, Y/C separation is not made. (When Y/C separation is set to OFF)

"0": Y/C separation ON (default) / "1": Y/C separation OFF

[Recommended] Recommended setting value is "0".

Setting to the recommended setting value may stabilize the operation when using in the environment where the electric field intensity changes significantly such as a light electric field.

[Note] When input is a color video, set #33h bit[2:0]="000". When input is a monochrome video, set #33h bit[2:0]="111".

14.3.42 Sub Address #34h/ Color Killer Control 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#34h	(res)	CKIL_PHL	CKIL_TH1[1:0]		CKIL_TH2[1:0]		CKIL_TH3[1:0]		94h

#34h/bit[7] Not defined
Set to “1” (initial value).

#34h/bit[6] CKIL_PHL, Color killer detection threshold level
“0”: Color is easy to disappear (default) / “1”: Color is hard to disappear

#34h/bit[5:4] CKIL_TH1[1:0], Color killer detection threshold 1
Detection sensitivity setting of the color killer using the sub-carrier phase when #33h CKIL_PHS=“1”.
Sets the detection sensitivity according to the number of lines in one field.
The greater the detection sensitivity value is, the easier the transiting to the color killer mode becomes.
When #33h CKIL_PHS=“0”, the detection sensitivity setting is disabled.

“00”: Detection sensitivity 0
“01”: Detection sensitivity 1 (default)
“10”: Detection sensitivity 2
“11”: Detection sensitivity 3

#34h/bit[3:2] CKIL_TH2[1:0], Color killer detection threshold 2
Detection sensitivity setting of the color killer using the sub-carrier phase when #33h CKIL_PHS=“1”.
Sets the detection sensitivity by counting the number of fields in addition to the setting of number of lines in bit[5:4] CKIL_TH1[1:0].
The greater the detection sensitivity value is, the easier the transiting to the color killer mode becomes.
When #33h CKIL_PHS=“0”, the detection sensitivity setting is disabled.

“00”: Detection sensitivity 3
“01”: Detection sensitivity 2 (default)
“10”: Detection sensitivity 1
“11”: Detection sensitivity 0

#34h/bit[1:0] CKIL_TH3[1:0], Color killer detection threshold 3
Detection sensitivity setting of the color killer using the sub-carrier phase when #33h CKIL_PHS=“1”.
(Returning from the color killer state to the color output state)
Condition to return to the color output state based on the result of counting the number of lines locked by the sub-carrier phase.
The smaller the detection sensitivity value is, the easier returning to the color output state becomes.
When #33h CKIL_PHS=“0”, the detection sensitivity setting is disabled.

“00”: Detection sensitivity 0 (default)
“01”: Detection sensitivity 1
“10”: Detection sensitivity 2
“11”: Detection sensitivity 3

14.3.43 Sub Address #35h/ Hue Control 1(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#35h	HUE_CNT[7:0]								00h

#35h/bit[7:0] HUE_CNT[7:0], Hue adjustment

Adjusts the color phase. The degree changes by approximately 1.4 per 1 bit. (+180° to -178.6°)
[Note] In SECAM or component inputs, setting is prohibited.

"0111_1111": -178.6°
|
"0000_0000": 0° (default)
|
"1000_0000": +180°

14.3.44 Sub Address #36h/ Chroma U(Cb) Level setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#36h	U_LV_CNT[6:0]							(res)	00h

#36h/bit[7:1] U_LV_CNT[6:0], Chroma data U level adjustment
This register is for adjusting the U(Cb) level of a chrominance signal.

"011_1111": 95/32 times
|
"000_0000": 32/32 times (default)
|
"110_0001": 1/32 times
"110_0000": Setting prohibited
|
"100_0000": Setting prohibited

#36h/bit[0] Not defined
Set to "0" (initial value).

14.3.45 Sub Address #37h/ Chroma V(Cr) Level setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#37h	V_LV_CNT[6:0]							(res)	00h

#37h/bit[7:1] V_LV_CNT[6:0], Chroma data V level adjustment
This register is for adjusting the V(Cr) level of a chrominance signal.

"011_1111": 95/32 times
|
"000_0000": 32/32 times (default)
|
"110_0001": 1/32 times
"110_0000": Setting prohibited
|
"100_0000": Setting prohibited

#37h/bit[0] Not defined
Set to "0" (initial value).

14.3.46 Sub Address #38h/ Color Burst Period Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#38h	BST_FBG_STA[3:0]				BST_FBG_END[3:0]				80h

#38h/bit[7:4] BST_FBG_STA[3:0], Color burst starting position adjustment

This register adjusts the starting position of the color burst signal detection.
Adjusts the detection starting position by two pixels at a time. The starting position becomes earlier in the minus direction and slower in the plus direction.
"0-pixel" is a standard starting position. Adjust when the color burst position is different from the reference.

"0111": +14-pixel
|
"0000": 0-pixel
|
"1000": -16-pixel (default)

#38h/bit[7:4] BST_FBG_END[3:0], Color burst ending position adjustment

This register adjusts the ending position of the color burst signal detection.
Adjusts the detection ending position by two pixels at a time. The ending position becomes earlier in the minus direction and slower in the plus direction.
"0-pixel" is a standard ending position. Adjust when the color burst position is different from the reference.

"0111": +14-pixel
|
"0000": 0-pixel (default)
|
"1000": -16-pixel

14.3.47 Sub Address #39h/ Color Burst Lock Adjustment (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#39h	BST_FBG	(res)	BST_LCK_RG [1:0]		BST_UNLCK [1:0]		BST_LCK [1:0]		00h

#39h/bit[7] BST_FBG, Color burst feedback gain selection

This register switches the feedback gain of the color burst signal.
When set to "0", the feedback gain is decreased if the signal is locked, resulting in smaller color mismatch per line.
When set to "1", a certain amount of feedback gain is always applied.
[Recommended] The recommended setting value of this register is "0".

"0": Small gain when locked (default)

"1": Gain constant

#39h/ bit[6] Not defined

Set to "0" (initial value).

#39h/bit[5:4] BST_LCK_RG[1:0], Color burst lock judge condition selection

This register selects the condition for judging whether or not the color burst signal is locked.
The larger the phase angle is, the more likely the signal is judged to be in a locked state.

"00": 180 degrees (default)

"01": 135 degrees

"10": 90 degrees

"11": 45 degrees

#39h/bit[3:2] BST_UNLCK[1:0], Adjustment of color burst lock feedback gain when unlocked

This register adjusts the color burst lock feedback gain when the signal is unlocked.

"00": 1/1 (default)

"01": 1/2

"10": 1/4

"11": 1/8

#39h/bit[1:0] BST_LCK[1:0], Adjustment of color burst lock feedback gain when locked

This register adjusts the color burst lock feedback gain when the signal is locked.
Enabled when the #39h bit[7] is set to "0".

"00": 1/16 (default)

"01": 1/32

"10": 1/64

"11": 1/128

14.3.48 Sub Address #3Ah/ Hue Control 2(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#3Ah	HUE_ CNT2	(res)							00h

#3Ah/ bit[7] HUE_CNT2, Hue adjustment enable
"0": Do not adjust (default) / "1": Adjust

#3Ah/bit [6:0] Not defined
Set to "00h" (initial value).

14.3.49 Sub Address #3Bh/ Hue Control 3(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#3Bh	HUE_CNT3[7:0]								00h

#3Bh/bit[7:0] HUE_CNT3[7:0], Hue setting
Sets the hue by rotating the Cb/Cr signal component. The hue is adjusted between -45° and 45°. The degree changes by approximately 0.35 per 1-bit.

"0111_1111": 44.6°
|
"0000_0000": 0° (default)
|
"1000_0000": -45°

14.3.50 Sub Address #40h/ Free-running Synchronization Output Control 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#40h	BB_ GDSEL	BB_ FMODE	BB_ CSEL	HLCK_DET1[1:0]		(res)	HLCK_DET2[1:0]		89h

#40h/bit[7] BB_GDSEL, Free-running synchronization protect time setting

This register sets the protection time of the synchronous detection (#71h bit[1] ST_HLCK_DT signal).
When set to “Not protected”, the ST_HLCK_DT signal switches quickly.
“Not protected” setting is effective for the video signal that has no noise.

“0”: Not protected / “1”: Protected (default)

#40h/bit[6] BB_FMODE, Forced free-running synchronization output mode setting

Regardless of the input signal, forces the free-running output of the synchronization signal, and outputs the video selected by #41h bit[7:6] BB_DSEL[1:0].
Even when the free-running synchronization output is forced, #71h bit[1] ST_HLCK_DT is detected by the input signal.

“0”: OFF (default) / “1”: ON

#40h/bit[5] BB_CSEL, Free-running synchronization output mode release setting

This register changes the switch speed from “0” to “1” of the ST_HLCK_DT signal.
When set to “0”, the ST_HLCK_DT signal is switched to the lock state more rapidly than when set to “1”.

“0”: 7 fields (default)/ “1”: 64 fields

#40h/bit[4:3] HLCK_DET1[1:0], H-lock detection sensitivity setting 1

Sets the detection sensitivity of #71h bit[1] ST_HLCK_DT.
Detects the number of edges (noise) within one line that does not include HSYNC, and if the value exceeds the setting value, #71h bit[1] ST_HLCK_DT is switched to “0”.
The larger the value of detection sensitivity, the easier the free-running synchronization output mode is enabled.
[Recommended] In a light electric field state, the recommended setting value is “11”.

“00”: Detection sensitivity 3

“01”: Detection sensitivity 2 (default)

“10”: Detection sensitivity 1

“11”: Detection sensitivity 0

#40h/bit [2] Not defined

Set to “0” (initial value).

#40h/bit [1:0] HLCK_DET2[1:0], H-lock detection sensitivity setting 2

Sets the detection sensitivity of #71h bit[1] ST_HLCK_DT.
Detects “the number of lines including the number of edges set by bit[4:3] HLCK_DET1[1:0]” within one field, and if the value exceeds the setting value, #71h bit[1] ST_HCLK_DT is switched to “0”.
The larger the value of detection sensitivity, the easier the free-running synchronization output mode is enabled.

“00”: Detection sensitivity 3

“01”: Detection sensitivity 2 (default)

“10”: Detection sensitivity 1

“11”: Detection sensitivity 0

14.3.51 Sub Address #41h/ Free-running Synchronization Output Control 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#41h	BB_DSEL[1:0]		(res)						00h

#41h/bit[7:6] BB_DSEL[1:0], Output data selection during free-running synchronization output
[Recommended] In a light electric field state, the recommended setting value is “11”.

“00”: Blue (default)
“01”: Black
“10”: Input signal
“11”: Input signal (luminance only, no color difference)

[Note] When in the forced blue-back mode (#40h bit[6] BB_FMODE = “1”), set this register to blue or black (“00” or “01”).

#41h/bit[5:0] Not defined
Set to “0” (initial value).

14.3.52 Sub Address #42h/ Free-running Synchronization Output Control 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#42h	BB_Y[7:0]								26h

#42h/bit[7:0] BB_Y[7:0], Output data setting during free-running synchronization output
Sets the level of luminance when the #41h bit[7:6] BB_DSEL is set to “00” (blue).
The value with luminance level to want to make output can be directly set.

14.3.53 Sub Address #43h/ Free-running Synchronization Output Control 4 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#43h	BB_CB[7:0]								5Ah

#43h/bit[7:0] BB_CB[7:0], Output data setting during free-running synchronization output
Sets the level of color difference (Cb) when the #41h bit[7:6] BB_DSEL is set to “00” (blue).
Set the value in two’s complement format.
The value with Cb level to want to make output can be directly set.

14.3.54 Sub Address #44h/ Free-running Synchronization Output Control 5 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#44h	BB_CR[7:0]								ECh

#44h/bit[7:0] BB_CR[7:0], Output data setting during free-running synchronization output
Sets the level of color difference (Cr) when the #41h bit[7:6] BB_DSEL is set to “00” (blue).
Set the value in two's complement format.
The value with Cr level to want to make output can be directly set.

14.3.55 Sub Address #48h/ STATUS Output Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#48h	STATUS_SEL[3:0]				(res)				00h

#48h/ bit[7:4] STATUS_SEL[3:0], STATUS output information selection

"0000": Interruption notification (default)
"0001": Not defined
"0010" :Not defined
"0011": Not defined
"0100": Not defined
"0101": Not defined
"0110": Input format detection (L:60Hz, H:50Hz)
"0111": Synchronous signal detection (L: Not detected, H: Detected)
"1000": Not defined
"1001": PLL synchronous detection (L: Not detected, H: Detected)
"1010": VBID detection (L: Not detected, H: Detected)
"1011": AFC operation detection (L: Not detected, H: Detected)
"1100": SYNC depth detection (L: Not detected, H: Detected)
"1101": Not defined
"1110": Not defined
"1111": Not defined

#48h/bit [3:0] Not defined
Set to "0" (initial value).

14.3.56 Sub Address #4Ch/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#4Ch	(res)								00h

#4Ch/bit[7:0] Not defined
Set to "00h" (initial value).

14.3.57 Sub Address #50h/ Analog setting 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#50h	ANG_ AMPE	ANG_ AGCS	ANG_ GAIN	(res)	ADC_CH_SEL[3:0]				A4h

#50h/bit[7] ANG_AMPE, Analog input amplifier operation setting

Sets the analog amplifier operation.

"0": Amplifier sleep

"1": Amplifier active (default)

#50h/bit[6] ANG_AGCS, Analog AGC function setting

Detects the SYNC level, and automatically adjusts the amplifier gain.

In the manual mode, #51h bit[5:0] ANG_GAIN_SET1[5:0], #59h bit[5:0] ANG_GAIN_SET2[5:0], #5Ah bit[5:0] ANG_GAIN_SET3[5:0] and #5Bh bit[5:0] ANG_GAIN_SET4[5:0] are used to set the amplifier gain individually.

"0": Manual setting (default)

"1": Automatic setting

#50h/bit[5] ANG_GAIN, Analog amplifier gain initial value setting

When the amplitude of the input analog signal is very small, setting this register to "0" allows the synchronization detection.

[Recommended] Set to "0" when the #50h[6] is set to 1 (automatic setting).

"0": 5.4

"1": 0.608 (default)

#50h/ bit[4] Not defined

Set to "0" (initial value).

#50h/bit[3:0] ADC_CH_SEL[3:0], Analog video input channel setting

ADC_CH_SEL [3:0]	Input Mode	Port for input									
		GIN1	GIN2	BIN1	BIN2	RIN1	RIN2	CVBS1	CVBS2	CVBS3	CVBS4
0000	YPbPr1	Y	-	Pb	-	Pr	-	-	-	-	-
0001	YPbPr2	-	Y	-	Pb	-	Pr	-	-	-	-
1000	RGB1	G	-	B	-	R	-	-	-	-	-
1001	RGB2	-	G	-	B	-	R	-	-	-	-
1011	S-Video	-	Y	-	C	-	-	-	-	-	-
0100	CVBS1	-	-	-	-	-	-	CVBS	-	-	-
0101	CVBS2	-	-	-	-	-	-	-	CVBS	-	-
0110	CVBS3	-	-	-	-	-	-	-	-	CVBS	-
0111	CVBS4	-	-	-	-	-	-	-	-	-	CVBS
Other than above	SLEEP	-	-	-	-	-	-	-	-	-	-

14.3.58 Sub Address #51h/ Analog setting 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#51h	(res)	AGC_OVF	ANG_GAIN_SET[5:0]						7Fh

#51h/bit[7] Not defined
Set to "0" (initial value).

#51h/bit[6] AGC_OVF, ADC overflow detection
This register sets the overflow detection of ADC when the amplifier gain is automatically set.
When set to "1", the amplifier gain is reduced if the overflow is detected.
Setting of "0" is effective for the video signal of which only the synchronization signal does not satisfy the standard value.

"0": Do not detect
"1": Detect (default)

#51h/bit[5:0] ANLG_GAIN_SET1[5:0], Analog amplifier gain manual setting 1
Gain setting when the analog amplifier gain is set in manual mode for AMP1(CVBS1-4, GIN1-2).

"11_1111": 63 Minimum gain (default)
|
"00_0000": 0 Maximum gain

Register #51/ANLG_GAIN_SET 1 [5:0]	Scaling factor
11_1111	0.608
11_0001	0.758
10_0110	0.939
01_1101	1.168
01_0110	1.440
01_0000	1.800
00_1011	2.274
00_0111	2.880
00_0100	3.600
00_0010	4.320
00_0000	5.400

[Note] (Scaling factor of analog amplifier gain) = 504/ (7 x ANLG_GAIN_SET1 + 56) x 0.6
The gain value is a design value.

14.3.59 Sub Address #52h/ Analog setting 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#52h	(res)	CLP_CS[2:0]			(res)		CLP_VS[1:0]		44h

#52h/bit[7] Not defined
Set to “0” (initial value).

#52h/bit[6:4] CLP_CS[2:0], Fine adjustment of clamp current (UP)
The clamp current : Iclp setting that is described in the amplifier characteristic table of the data sheet.
CLP_CS can be adjusted between “000”(0) and “111”(7).The initial value is “100”(4).
Normally, it can be used with the default state.

#52h/bit[3:2] Not defined
Set to “01” (initial value).

#52h/bit[1:0] CLP_VS[1:0], Fine adjustment of clamp voltage
The clamp voltage : Vclp setting that is described in the amplifier characteristic table of the data sheet.
CLP_VS can be adjusted between “00”(0) and “11”(3).The initial value is “00”(0).
Normally, it can be used with the default state.

14.3.60 Sub Address #53h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#53h	(res)								00h

#53h/bit[7:0] Not defined
Set to "00h" (initial value).

14.3.61 Sub Address #54h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#54h	(res)								04h

#54h/bit[7:0] Not defined
Set to "04h" (initial value).

14.3.62 Sub Address #55h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#55h	(res)								F3h

#55h/bit[7:0] Not defined
Set to "F3h" (initial value).

14.3.63 Sub Address #56h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#56h	(res)								00h

#56h/bit[7:0] Not defined
Set to "00h" (initial value).

14.3.64 Sub Address #57h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#57h	(res)								00h

#57h/bit[7:0] Not defined
Set to "00h" (initial value).

14.3.65 Sub Address #58h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#58h	(res)								00h

#58h/bit[7:0] Not defined
Set to "00h" (initial value).

14.3.66 Sub Address #59h/ Analog setting 4 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#59h	(res)		ANG_GAIN_SET2[5:0]						3Fh

#59h/bit[7:6] Not defined
Set to "0" (initial value).

#59h/bit[5:0] ANLG_GAIN_SET2[5:0], Analog amplifier gain manual setting 2
Gain setting when the analog amplifier gain is set in manual mode for AMP2(CSYNC_A).

"11_1111": 63 Minimum gain (default)
|
"00_0000": 0 Maximum gain

Register #59/ANLG_GAIN_SET 2 [5:0]	Scaling factor
11_1111	0.608
11_0001	0.758
10_0110	0.939
01_1101	1.168
01_0110	1.440
01_0000	1.800
00_1011	2.274
00_0111	2.880
00_0100	3.600
00_0010	4.320
00_0000	5.400

[Note] (Scaling factor of analog amplifier gain) = 504/ (7 x ANLG_GAIN_SET2 + 56) x 0.6
The gain value is a design value.

14.3.67 Sub Address #5Ah/ Analog setting 5 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#5Ah	(res)		ANG_GAIN_SET3[5:0]						3Fh

#5Ah/bit[7:6] Not defined
Set to “0” (initial value).

#5Ah/bit[5:0] ANLG_GAIN_SET3[5:0], Analog amplifier gain manual setting 3
Gain setting when the analog amplifier gain is set in manual mode for AMP3(BIN1-2).

“11_1111”: 63 Minimum gain (default)
|
“00_0000”: 0 Maximum gain

Register #5A/ANLG_GAIN_SET 3 [5:0]	Scaling factor
11_1111	0.608
11_0001	0.758
10_0110	0.939
01_1101	1.168
01_0110	1.440
01_0000	1.800
00_1011	2.274
00_0111	2.880
00_0100	3.600
00_0010	4.320
00_0000	5.400

[Note] (Scaling factor of analog amplifier gain) = 504/ (7 x ANLG_GAIN_SET3 + 56) x 0.6
The gain value is a design value.

14.3.68 Sub Address #5Bh/ Analog setting 6 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#5Bh	(res)		ANG_GAIN_SET4[5:0]						3Fh

#5Bh/bit[7:6] Not defined
Set to “0” (initial value).

#5Bh/bit[5:0] ANLG_GAIN_SET4[5:0], Analog amplifier gain manual setting 4
Gain setting when the analog amplifier gain is set in manual mode for AMP4(RIN1-2).

“11_1111”: 63 Minimum gain (default)
|
“00_0000”: 0 Maximum gain

Register #5B/ANLG_GAIN_SET 4 [5:0]	Scaling factor
11_1111	0.608
11_0001	0.758
10_0110	0.939
01_1101	1.168
01_0110	1.440
01_0000	1.800
00_1011	2.274
00_0111	2.880
00_0100	3.600
00_0010	4.320
00_0000	5.400

[Note] (Scaling factor of analog amplifier gain) = 504/ (7 x ANLG_GAIN_SET1 + 56) x 0.6
The gain value is a design value.

14.3.69 Sub Address #5Ch/ HPLL Control 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#5Ch	PLL_EN	PLL_ LKEN	SCFB_ SEL	PLL_LL_ SEL	PLL_ LK_TM	PLL_ PH_LMT	PLL_ LK_PRCT[1:0]		A0h

#5Ch/bit[7] PLL_EN, PLL operation selection

This register sets whether PLL is used or not.

"0": External clock / "1": PLL clock (default)

[Note] External clock mode is only available at 27MHz sampling operation.

#5Ch/bit[6] PLL_LKEN, PLL clock selection

This register sets the PLL operation mode.

"0": Line lock clock (default) / "1": PLL fixed clock

#5Ch/bit[5] SCFB_SEL, Sub-carrier feedback selection

This register provides the feedback of color sub-carrier depending on the PLL oscillation frequency. The "Feedback" setting is valid when the color sub-carrier frequency is standard value while the line cycle is not.

This register is enabled when line lock clock selected (#5C[7]="1" and #5C[6]=1)

"0": No feedback / "1": Feedback (default)

#5Ch/bit[4] PLL_LL_SEL, PLL line lock control selection in the light electric field state

This register controls the PLL line lock from OFF to ON.

This register is enabled when line lock clock selected (#5C[7]="1" and #5C[6]=1)

"0": Line lock OFF when the number of pixels per line changes frequently (default)

"1": Always line lock ON

#5Ch/bit[3] PLL_LK_TM, PLL lock time selection

In the Fast-lock mode, the trace rate of PLL can be faster while the traceability may be deteriorated if a nonstandard signal is input.

"0": Normal mode (default) / "1": Fast-lock mode

#5Ch/bit[2] PLL_PS_LMT, PLL phase difference limiter selection

This register selects the PLL phase difference limiter. Normally use the default setting.

"0": No limiter (default) / "1": Use limiter

#5Ch/bit[1:0] PLL_LK_PRCT[1:0], PLL lock protect time selection

Sets the maximum length of time until the PLL is locked. If the PLL is not locked within the specified field count, operates with a PLL fixed clock.

"00": 32 fields (default)

"01": 64 fields

"10": 128 fields

"11": 256 fields

14.3.70 Sub Address #5Dh/ HPLL Control 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#5Dh	(res)	PLL_GAIN_S1[2:0]			(res)	PLL_GAIN_S2[2:0]			00h

#5Dh/bit[7] Not defined
Set to "0" (initial value).

#5Dh/bit[6:4] PLL_GAIN_S1[2:0], Gain rough adjustment at lock start
Adjusts the feedback gain factor of PLL at lock start.
This setting is effective in stabilizing the PLL operation.

"011": 8 times
"010": 4 times
"001": 2 times
"000": 1 time (default)
"111": 1/2 times
"110": 1/4 times
"101": 1/8 times
"100": Not defined

#5Dh/bit[3] Not defined
Set to "0" (initial value).

#5Dh/bit[2:0] PLL_GAIN_S2[2:0], Gain fine adjustment at lock start
Adjusts finely the feedback gain factor of PLL at lock start.
This setting is effective in stabilizing the PLL operation.

"011": 1/8 times
"010": 1/16 times
"001": 1/32 times
"000": 1/64 times (default)
"111": 1/128 times
"110": 1/256 times
"101": 1/512 times
"100": Not defined

14.3.71 Sub Address #60h/ VBID Detection Control (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#60h	VBID_DT	(res)							00h

#60h/bit[7] VBID_DT, Data detection mode during VBI period

Sets the data detection during VBI period. To detect the VBI data, set this register to "1".

"0": Not detected (default) / "1": Detected

#60h/bit[6:0] Not defined

Set to "0".

14.3.72 Sub Address #61h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#61h	(res)								86h

#61h/bit[7:0] Not defined

Set "86h" (initial value).

14.3.73 Sub Address #62h/ Closed Caption Detection Setting 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#62h	C.C_DT_LV[2:0]			C.C_ODT_LSET[4:0]					00h

#62h/bit[7:5] C.C_DT_LV[2:0], C.C. data detection level

Sets the level for detecting the closed caption data that is written into a specific line of the VBI period of NTSC signal. Adjust this setting when you want to improve the detection sensitivity.

"011": 79IRE

"010": 65IRE

"001": 50IRE

"000": 36IRE (default)

"111": 22IRE

"110": 0IRE

"101": 0IRE

"100": 0IRE

#62h/bit[4:0] C.C_ODT_LSET[4:0], C.C. data ODD detection line setting

Sets the detection line of the closed caption data in the ODD field.
Normally, this is written into the default line.

"0_1111": +15 NTSC: 36 line / PAL: 37 line

|

"0_0001": +1 NTSC: 22 line / PAL: 23 line

"0_0000": 0 NTSC: 21 line / PAL: 22 line (default)

"1_1111": -1 NTSC: 20 line / PAL: 21 line

|

"1_0000": -16 NTSC: 5 line / PAL: 6 line

14.3.74 Sub Address #63h/ Closed Caption Detection Setting 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#63h	(res)			C.C_EDT_LSET[4:0]					00h

#63h/bit[7:5] Not defined

Set to "0" (initial value).

#63h/bit[4:0] C.C_EDT_LSET[4:0], C.C. data EVEN detection line setting

Sets the detection line of the closed caption data in the EVEN field.
Normally, this is written into the default line.

"0_1111": +15 NTSC: 36(299) line / PAL: 37(350) line

|

"0_0001": +1 NTSC: 22(285) line / PAL: 23(336) line

"0_0000": 0 NTSC: 21(284) line / PAL: 22(335) line (default)

"1_1111": -1 NTSC: 20(283) line / PAL: 21(334) line

|

"1_0000": -16 NTSC: 5(268) line / PAL: 6(319) line

14.3.75 Sub Address #64h/ CGMS Detection Setting 1 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#64h	(res)			CGMS_DT_LV[2:0]			CGMS_ODT_LSET[1:0]		00h

[Note] NTSC only

#64h/bit[7:5] Not defined
Set to "0" (initial value).

#64h/bit[4:2] CGMS_DT_LV[2:0], CGMS data detection level
Set the level of detecting the CGMS data written into a specific line of the VBI period.
Adjust this setting when you want to improve the detection sensitivity.

"011": 79IRE
"010": 65IRE
"001": 50IRE
"000": 36IRE (default)
"111": 22IRE
"110": 0IRE
"101": 0IRE
"100": 0IRE

#64h/bit [1:0] CGMS_ODT_LSET[1:0], CGMS data ODD detection line setting
Sets the detection line of the CGMS data in the ODD field.
Normally, this is written into the default line.

"01": +1 NTSC: 21 line
"00": 0 NTSC: 20 line (default)
"11" : -1 NTSC: 19 line
"10": -2 NTSC: 18 line

14.3.76 Sub Address #65h/ CGMS Detection Setting 2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#65h	(res)						CGMS_EDT_LSET[1:0]		00h

[Note] NTSC only

#65h/bit[7:2] Not defined
Set to "0" (initial value).

#65h/bit[1:0] CGMS_EDT_LSET[1:0], CGMS data EVEN detection line setting
Sets the detection line of the CGMS data in the EVEN field.
Normally, this is written into the default line.

"01": +1 NTSC: 284 line
"00": 0 NTSC: 283 line (default)
"11": -1 NTSC: 282 line
"10": -2 NTSC: 281 line

14.3.77 Sub Address #66h/ VBI Non Standard Signal Detection Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#66h	VBNS_DT_LV[2:0]			(res)					00h

#66h/bit[7:5] VBNS_DT_LV[2:0], VBI non standard signal level setting

Set the level of detecting the non standard signal written into a specific line of the VBI period.
Adjust this setting when you want to improve the detection sensitivity.

"011": 100IRE
"010": 100IRE
"001": 100IRE
"000": 92IRE (default)
"111": 74IRE
"110": 57IRE
"101": 39IRE
"100": 22IRE

#66/bit[4:0] Not defined

Set "0" (initial value).

14.3.78 Sub Address #67h/ Reserved Register (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#67h	(res)								00h

#67/bit[7:0] Not defined

Set "00h" (initial value).

14.3.79 Sub Address #68h/ WSS Data Detection Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#68h	(res)			WSS_DT_LV[2:0]			WSS_ODT_LSET [1:0]		00h

[Note] PAL only

#68h/bit[7:5] Not defined
Set to "0" (initial value).

#68h/bit[4:2] WSS_DT_LV[2:0], WSS data detection level setting
Set the level of detecting the WSS data written into a specific line of the VBI period of PAL signal.
Adjust this setting when you want to improve the detection sensitivity.

"011": 79IRE
"010": 65IRE
"001": 50IRE
"000": 36IRE (default)
"111": 22IRE
"110": 0IRE
"101": 0IRE
"100": 0IRE

#68h/bit[1:0] WSS_ODT_LSET[1:0], WSS data ODD detection line setting
Sets the detection line of the WSS data in the ODD field.
Normally, this is written into the default line.

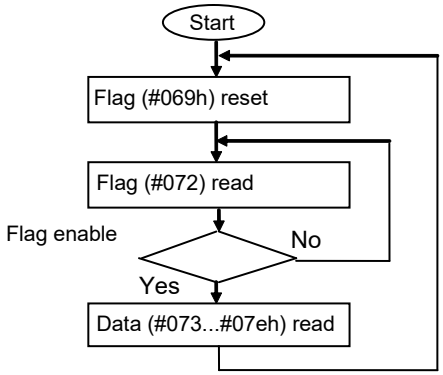
"01": +1 NTSC: 24 line
"00": 0 NTSC: 23 line (default)
"11": -1 NTSC: 22 line
"10": -2 NTSC: 21 line

14.3.80 Sub Address #69h/ VBID Detection Reset Control (W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#69h	(res)	RST_ C.C_O	RST_ C.C_E	RST_ CGMS_O	RST_ CGMS_E	(res)	(res)	RST_ WSS	00h

Whether each data was present or not is stored within the decoder.
Those results can be read out from the sub address #72h of the I^2C bus.
The contents that have been stored once will not be erased unless this register instructs it.
However, the information may not be detected depending on the condition or contents of the signal.
An example of the VBID module read sequence is shown below.

[Note] When this detection function is used, the information of the presence of a VBID signal or contents may be output incorrectly depending on the input signal state.
To ensure the stable operation of this function, read the signal over several fields, and confirm that the read contents are stable, before using the detected data.



Example of VBID Module Read Sequence

#69h/bit[7] Not defined.

Set to “0”.

#69h/bit[6] RST_C.C_O, C.C. data (odd field) reset request

“1”: Flag reset

#69h/bit[5] RST_C.C_E, C.C. data (even field) reset request

“1”: Flag reset

#69h/bit[4] RST_CGMS_O, CGMS data (odd field) reset request

“1”: Flag reset

#69h/bit[3] RST_CGMS_E, CGMS data (even field) reset request

“1”: Flag reset

#69h/bit[2] Not defined.

Set to “0”.

#69h/bit[1] Not defined.

Set to “0”.

#69h/bit[0] RST_WSS, WSS data reset request

“1”: Flag reset

14.3.81 Sub Address #70h/ Status Register 1 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#70h	(res)	(res)		ST_IFM_DET[4:0]					00h

#70h/ bit[7] Not defined

This register reads “X”(unknown) when read.

#70h/ bit[5:4] Not defined

This register reads “00” when read.

#70h/bit[4:0] ST_IFM_DET[4:0], Reading the input format automatic judgment result

Stores the results of the automatic judgment of the input video signal.

“00000” : NTSC-M
“00001” : NTSC-J
“00010” : NTSC 443
“00011” : PAL
“00100” : PAL-M
“00101” : PAL-N
“00110” : PAL-Nc
“00111” : PAL-60
“01000” : SECAM
“10000” : 525i
“10001” : 625i
“10010” : 525p
“10011” : 625p
“10100” : WVGA-33.231MHz
“10101” : WVGA-33.333MHz
“10110” : EGA-480
“10111” : EGA-400
“11000” : 525p (Sampling frequency setting mode)
Other than above : Not defined

14.3.82 Sub Address #71h/ Status Register 2 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#71h	ST_ NSCB_M2	ST_ NSCB_M1	ST_ SD_DT	ST_ VBID_DT	ST_ VTR_DT	ST_ AFC_MT	ST_ HLCK_DT	ST_ PLL_MD	00h

#71h/bit[7] ST_NSCB_M2, Non standard color burst (mode 2) judgment result readout

"0": Not detected / "1": Detected

#71h/bit[6] ST_NSCB_M1, Non standard color burst (mode 1) judgment result readout

"0": Not detected / "1": Detected

#71h/bit[5] ST_SD_DT, SYNC depth detection
Able to monitor whether there is a difference between the SYNC depth during the vertical blank period and the SYNC depth during the vertical valid period.

"0": Not detected / "1": Detected

#71h/bit[4] ST_VBID_DT, VBID data detection
Able to monitor whether each VBID flag of #72[7:0] is detected or not.

"0": Not detected / "1": Detected

#71h/bit[3] ST_VTR_DT, VTR detection monitor
Able to monitor whether the VTR signal is detected or not.

"0": Not detected / "1": Detected

#71h/bit[2] ST_AFC_MT, AFC operation mode monitor
Able to monitor whether AFC is operating or not.

"0": No operation / "1": Operation

#71h/bit[1] ST_HLCK_DT, Synchronization signal detection
Able to monitor HLOCK detection result described in section 4.5.

"0": Not detected / "1": Detected

#71h/bit[0] ST_PLL_MD, Internal HPLL operation mode
Able to monitor whether the internal HPLL operates in the line lock mode or in the asynchronous sampling mode.

"0": Asynchronous sampling / "1": Line lock

14.3.83 Sub Address #72h/ VBID Flag Register (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#72h	VF_ NSCB	VF_ C.C_O	VF_ C.C_E	VF_ CGMS_O	VF_ CGMS_E	VF_ VBNS_O	VF_ VBNS_E	VF_ WSS	00h

This register holds the detection results of the VBID flags.

When any VBID flag is set to "1", C.C, CGMS, WSS data can be read from register #73h to #7Eh.

#72h/ bit[7] VF_NSCB, Non standard color burst detect
#72h/ bit[6] VF_C.C_O, C.C. data ready(odd field)
#72h/ bit[5] VF_C.C_E, C.C. data ready(even field)
#72h/ bit[4] VF_CGMS_O, CGMS data ready(odd field)
#72h/ bit[3] VF_CGMS_E, CGMS data ready(even field)
#72h/ bit[2] VF_VBNS_O, VBI non standard signal detect(odd field)
#72h/ bit[1] VF_VBNS_E, VBI non standard signal detect(even field)
#72h/ bit[0] VF_WSS, WSS data ready

14.3.84 Sub Address #73h/ C.C Data Buffer Register in ODD Field 0 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#73h	C.C_O_DT2[7:0]								00h

#73h/ bit[7:0] C.C_O_DT2[7:0], character Two b0..b6,p2
Able to read out the value of the character 2 of the ODD closed caption data.

14.3.85 Sub Address #74h/ C.C Data Buffer Register in ODD Field 1 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#74h	C.C_O_DT1[7:0]								00h

#74h/ bit[7:0] C.C_O_DT1[7:0], character One b0..b6,p1
Able to read out the value of the character 1 of the ODD closed caption data.

14.3.86 Sub Address #75h/ C.C Data Buffer Register in EVEN Field 0 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#75h	C.C_E_DT2[7:0]								00h

#75h/ bit[7:0] C.C_E_DT2[7:0], character Two b0..b6,p2
Able to read out the value of the character 2 of the EVEN closed caption data.

14.3.87 Sub Address #76h/ C.C Data Buffer Register in EVEN Field 1 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#76h	C.C_E_DT1[7:0]								00h

#76h/ bit[7:0] C.C_E_DT1[7:0], character One b0..b6,p1
Able to read out the value of the character 1 of the EVEN closed caption data.

14.3.88 Sub Address #77h/ CGMS Data Buffer Register in ODD Field 0 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#77h	CGMS_O_DT3[7:0]								00h

#77h/ bit[7:0] CGMS_O_DT3[7:0], Bit 13..20
Able to read the value of bit 13 to bit 20 of the ODD CGMS data.

14.3.89 Sub Address #78h/ CGMS Data Buffer Register in ODD Field 1 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#78h	CGMS_O_DT2[7:0]								00h

#78h/ bit[7:0] CGMS_O_DT2[7:0], Bit 5..12
Able to read the value of bit 5 to bit 12 of the ODD CGMS data.

14.3.90 Sub Address #79h/ CGMS Data Buffer Register in ODD Field 2 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#79h	CC_O_P1_ER	CC_O_P2_ER	(res)	CGMS_O_CRC_ER	CGMS_O_DT1[3:0]				00h

#79h/ bit[7] CC_O_P1_ER, C.C. ODD PTY1 error detection
Able to read out the parity error judgment results of the ODD C.C. data PTY1.

"0": No error / "1": Error

#79h/ bit[6] C.C_O_P2_ER, C.C. ODD PTY2 error detection
Able to read out the parity error judgment results of the ODD C.C. data PTY2.

"0": No error / "1": Error

#79h/bit[5] Not defined
No setting. This register reads "0" when read.

#79h/bit[4] CGMS_O_CRC_ER, CGMS ODD CRC error detection
Able to read the value of the CRC error judgment result of the ODD CGMS data.

"0": No error / "1": Error

#79h/ bit[3:0] CGMS_O_DT1[3:0], Bit 1..4
Able to read the value of bit 1 to bit 4 of the ODD CGMS data.

14.3.91 Sub Address #7Ah/ CGMS Data Buffer Register in EVEN Field 0 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Ah	CGMS_E_DT3[7:0]								00h

#7Ah/ bit[7:0] CGMS_E_DT3[7:0], Bit 13..20
Able to read the value of bit 13 to bit 20 of the EVEN CGMS data.

14.3.92 Sub Address #7Bh/ CGMS Data Buffer Register in EVEN Field 1 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Bh	CGMS_E_DT2[7:0]								00h

#7Bh/ bit[7:0] CGMS_E_DT2[7:0], Bit 5..12
Able to read the value of bit 5 to bit 12 of the EVEN CGMS data.

14.3.93 Sub Address #7Ch/ CGMS Data Buffer Register in EVEN Field 2 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Ch	CC_E_P1_ER	CC_E_P2_ER	(res)	CGMS_E_CRC_ER	CGMS_E_DT1[3:0]				00h

#7Ch/ bit[7] C.C_E_P1_ER, C.C. EVEN PTY1 error detection
Able to read out the parity error judgment results of the EVEN C.C. data PTY1.

"0": No error / "1": Error

#7Ch/ bit[6] C.C_E_P2_ER, C.C. EVEN PTY2 error detection
Able to read out the parity error judgment results of the EVEN C.C. data PTY2.

"0": No error / "1": Error

#7Ch/bit[5] Not defined
No setting. This register reads "0" when read.

#7Ch/bit[4] CGMS_E_CRC_ER, CGMS EVEN CRC error detection
Able to read out the CRC error judgment results of the EVEN CGMS data.

"0": No error / "1": Error

#7Ch/ bit[3:0] CGMS_E_DT1[7:0], Bit 1..4
Able to read the value of bit 1 to bit 4 of the EVEN CGMS data.

14.3.94 Sub Address #7Dh/ WSS Data Buffer Register 0 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Dh	WSS_DG2[1:0]		WSS_DG3[2:0]			WSS_DG4[2:0]			00h

#7Dh/ bit[7:6] WSS_DG2[1:0], Group2 Bit 6, 7
#7Dh/ bit[5:3] WSS_DG3[2:0], Group3 Bit 8, 9, 10
#7Dh/ bit[2:0] WSS_DG4[2:0], Group4 Bit 11, 12, 13
Able to read the value of bit 13 to bit 6 of the WSS data.

14.3.95 Sub Address #7Eh/ WSS Data Buffer Register 1 (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Eh	WSS_P_ER	(res)	WSS_DG1[3:0]			WSS_DG2[3:2]			00h

#7Eh/bit[7] WSS_P_ER, WSS PTY error detection
Able to read out the parity error judgment results of the WSS data.
"0": No error / "1": Error

#7Eh/ bit[6] Not defined
The read value is undefined.

#7Eh/ bit[5:2] WSS_DG1[3:0], Group1 Bit 0, 1, 2, 3
#7Eh/ bit[1:0] WSS_DG2[3:2] Group2 Bit 4, 5
Able to read the value of bit 5 to bit 0 of the WSS data.

14.3.96 Sub Address #7Fh/ Copy Guard Status Register (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Fh	NSS_D	VBNS_D	VBNS_OP	NSCB_OP	NSCB_MOD	(res)	CCOP[1:0]		00h

#7Fh/bit[7] NSS_D, Non standard sync signal detection
Able to be read non standard sync signal detection result.

"0": Not detected / "1": Detected

#7Fh/bit[6] VBNS_D, VBI non standard signal detection
Able to be read VBI non standard signal detection result.

"0": Not detected / "1": Detected

#7Fh/bit[5] VBNS_OP, VBI non standard operation detection
Able to be read VBI non standard operation detection result.

"0": Not detected / "1": Detected

#7Fh/bit[4] NSCB_OP, Non standard color burst operation detection
Able to be read non standard color burst operation detection result.

"0": Not detected / "1": Detected

#7Fh/bit[3] NSCB_MOD, Non standard color burst operation mode detection
Able to be read non standard color burst operation mode detection result.

"0": Mode 1 / "1": Mode 2

#7Fh/bit[2] Not defined
No setting. This register reads "0" when read.

#7Fh/bit[1:0] CCOP, Copy control operation detection
Able to be read copy control data (copy guard detection result).

"00": VBI non standard operation detection, non standard color burst operation no detection
"01": VBI non standard operation detection, non standard color burst operation no detection
"10": VBI non standard operation detection, non standard color burst operation mode1 detection
"11": VBI non standard operation detection, non standard color burst operation mode2 detection

14.3.97 Sub Address #80h/ Interruption Mask Setting 1(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#80h	(res)	SD_MSK	TVSYS_MSK	VBID_MSK	VTR_MSK	AFC_MSK	HLCK_MSK	PLLMD_MSK	FFh

#80h/bit[7] Not defined.
Set to “1”.

#80h/bit[6] SD_MSK, SYNC depth detection interruption mask
Sets the masking of the notification of the SYNC depth detection interruption.
“0” : No mask / “1” : Mask

#80h/bit[5] TVSYS_MSK, Input video format change interruption mask
Sets the masking of the notification of the input video format change detection interruption.
“0” : No mask / “1” : Mask

#80h/bit[4] VBID_MSK, VBID detection interruption mask
Sets the masking of the notification of the VBID detection interruption.
“0” : No mask / “1” : Mask

#80h/bit[3] VTR_MSK, VTR detection interruption mask
Sets the masking of the notification of the VTR detection interruption.
“0” : No mask / “1” : Mask

#80h/bit[2] AFC_MSK, AFC operation status change interruption mask
Sets the masking of the notification of the AFC operation status change interruption.
“0” : No mask / “1” : Mask

#80h/bit[1] HLCK_MSK, Synchronization signal detection interruption mask
Sets the masking of the notification of the synchronization detection interruption.
“0” : No mask / “1” : Mask

#80h/ bit[0] PLLMD_MSK, PLL line lock operation status change interruption mask
Sets the masking of the notification of the PLL line lock operation status change interruption.
“0” : No mask / “1” : Mask

14.3.98 Sub Address #81h/ Interrupt Status 1(R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#81h	(res)	SD_INT	TVSYS_INT	VBID_INT	VTR_INT	AFC_INT	HLCK_INT	PLLMD_INT	00h

#81h/bit[7] Not defined

Read out unknown status.

#81h/bit[6] SD_INT, SYNC depth detection interruption status

Able to read out the information of SYNC depth detection interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

#81h/bit[5] TVSYS_INT, Input video format change interruption status

Able to read out the information of the input video format change detection interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

#81h/bit[4] VBID_INT, VBID detection interruption status

Able to read out the information of VBID detection interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

#81h/bit[3] VTR_INT, VTR detection interruption status

Able to read out the information of VTR detection interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

#81h/bit[2] AFC_INT, AFC operation status change interruption status

Able to read out the information of AFC operation status change interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

#81h/bit[1] HLCK_INT, Synchronization signal detection interruption status

Able to read out the information of synchronization detection interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

#81h/bit[0] PLLMD_INT, PLL line lock operation status change interruption status

Able to read out the information of PLL line lock operation status change interruption. When writing, clears the interrupt.

"0" : No interruption / "1" : Interruption (cleared when writing)

14.3.99 Sub Address #84h,#85h,#86h,#87h/ HPLL setting 3,4,5,6 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#84h	PLL_FREQ[7:0]								AAh
#85h	PLL_FREQ[15:8]								AAh
#86h	PLL_FREQ[23:16]								AAh
#87h	PLL_FREQ[31:24]								42h

#84h/bit[7:0],#85h/bit[7:0],#86h/bit[7:0],#87h/bit[7:0] PLL_FREQ[31:0]、PLL sampling frequency setting

Sets the sampling (operating) clock frequency.

This register is available in WVGA2 mode (#00h[7:1]=1010110) or sampling frequency setting mode (#00h[7:1]=1100000).

Set the sampling frequency by expression described below.

Setting value = 2^32 x sampling clock frequency / (4 x reference clock frequency)

Reference clock frequency :Clock frequency input from XOSCI pin

Example 1:Sampling clock frequency=33.33333333MHz,reference clock frequency=32MHz

2^32 x 33.33333333MHz／(4 x 32MHz)≒1118481066＝42AAAAAAh

Example 2:Sampling clock frequency =25.175MHz,reference clock frequency =32MHz

2^32 x 25.175MHz／(4 x 32MHz)≒844732825＝32599999h

14.3.100 Sub Address #88h,#89h/ Sampling frequency setting control 1,2 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#88h	SAMPLE_PIXEL[7:0]								00h
#89h	(res)					SAMPLE_PIXEL[10:8]			00h

#88h/ bit[7:0],#89h/ bit[2:0] SAMPLE_PIXEL[10:0] pixel number of 1 line setting

Total pixel number of sampling frequency setting mode.

Actual total pixel number is “setting value+1”.

Total pixel number can operate when total pixel number is even number. Set odd number to this register.

Also set the register sub address #84h to #87h and #8Ah to #8Eh.

Total pixel of one line covers from 576 to 1280 pixels.

[Note] Only available for progressive 525 line input.

VVALID period follows 525P operation.

(VVALID position can be adjusted by control register #1Dh[7:0])

14.3.101 Sub Address #8Ah/ Sampling frequency setting control 3 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#8Ah	DEHST[7:0]								00h

#8Ah/ bit[7:0] DEHST[7:0] Horizontal valid start position setting

Horizontal valid start position from negative edge of horizontal synchronization in sampling frequency setting mode.

Actual horizontal valid start position is “setting value+1”.

S Horizontal valid start position can operate when total pixel number is even number. Set odd number to this register.

14.3.102 Sub Address #8B,#8Ch/ Sampling frequency setting control 4,5 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#8Bh	DEHWD[7:0]								00h
#8Ch	(res)					DEHWD[10:8]			00h

#8Bh/ bit[7:0], #8Ch/ bit[2:0] DEHWD[10:0] Horizontal valid period setting

Horizontal valid period in sampling frequency setting mode.

Actual horizontal valid period is "setting value+1".

Horizontal valid period can operate when total pixel number is even number. Set odd number to this register.

Set this register within (DEHST+1) + (DEHWD+1) < (SAMPLE_PIXEL+1)

14.3.103 Sub Address #8Dh/ Sampling frequency setting control 6 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#8Dh	SYNCTIP[7:0]								00h

#8Dh/ bit[7:0] SYNCTIP[7:0] Synctip position setting

Synctip position from negative edge of horizontal synchronization in sampling frequency setting mode.

Actual horizontal valid period is "setting value+1".

[Note] This register is available only for Sync on Y/G input with AGC processing.

14.3.104 Sub Address #8Eh/ Sampling frequency setting control 7 (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#8Eh	PEDESTAL[7:0]								00h

#8Eh/ bit[7:0] PEDESTAL[7:0] Pedestal position setting

Pedestal position in sampling frequency setting mode.

Actual pedestal position is "setting value+1".

Detect black level of input signal using 16 pixels from pedestal position, adjust AGC gain or pedestal level.

Set not to overlap with valid period or horizontal synchronization period.

[Note] This register is available only for Sync on Y/G input with AGC processing.

14.3.105 Sub Address #8Fh/ Reference Clock Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#8Fh	(res)							OSC_SEL	00h

#8Fh/bit[7:1] Not defined.

Set to "1".

#8Fh/bit[0] OSC_SEL, Reference clock selection

Sets the reference clock when HPLL is used.

"0" : 32.000MHz (default)

"1" : 25.000MHz

14.3.106 Sub Address #FFh/ Power Down, Internal Operation Mode Setting (R/W)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#FFh	(res)			PDEN	(res)	ISAM	ICYC[1:0]		00h

#FFh/bit[7:5] Not defined
Set “000” (initial value).

#FFh/ bit[4] PDEN, Power down setting
Minimizes the internal operation to go to the power down mode. When PDEN = “1”, the synchronization signal and data output are also stopped.
“0”: Normal operation (default) / “1”: Power down mode

#FFh/bit[3] Not defined
Set “0” (initial value).

#FFh/ bit[2] ISAM, I2C bus addressing mode selection
ISAM = “0” sets the address increment mode, which is the default state. If two or more data are successively accessed, the register address is incremented starting from the specified beginning address. This is useful to access a contiguous register address area.

ISAM = “1” sets the address circulating mode. By setting the ICYC register, one to four addresses from the beginning address of the register can be accessed in a circular fashion. It is useful to access the same address successively (ICYC = “00”) or to access two to four addresses repeatedly.
“0”: Address increment mode (default) / “1”: Address circulating mode

#FFh/ bit[1:0] ICYC, Circulating range in address circulating mode
Sets the range of the address circulation when bit[2] ISAM = “1”.

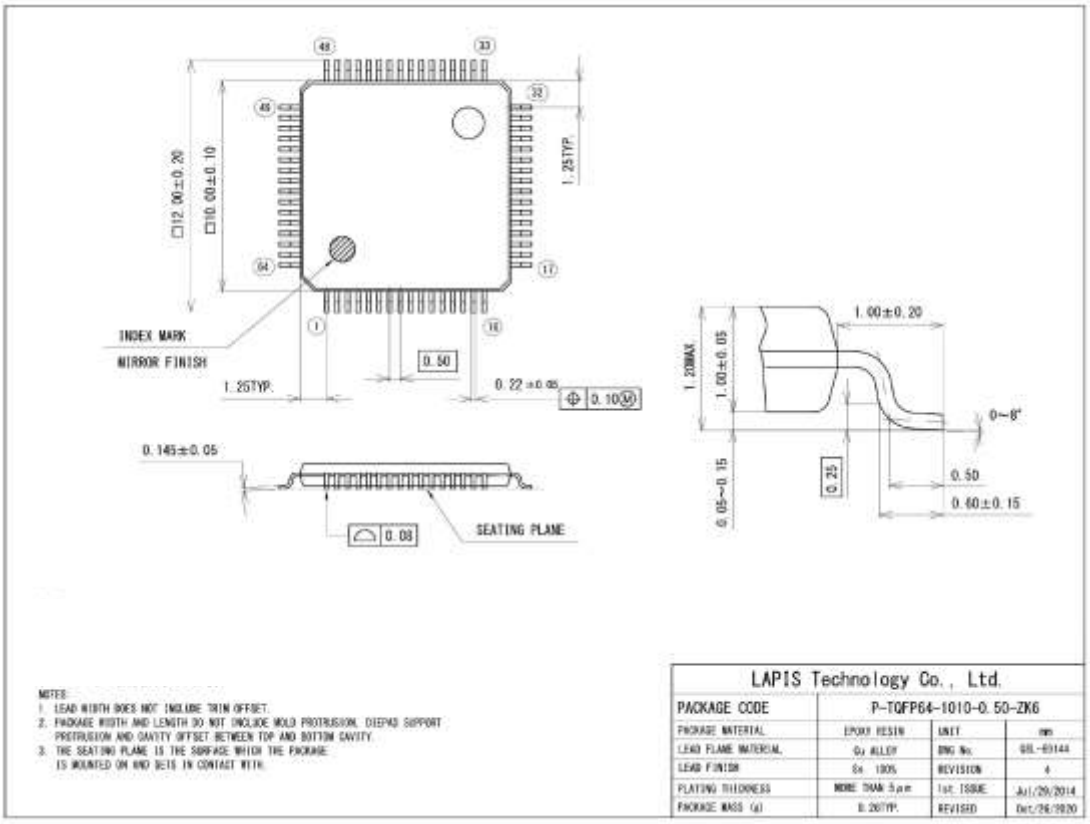
“00”: Only the beginning address (default)
“01”: From the beginning address to (the beginning address + 1)
“10”: From the beginning address to (the beginning address + 2)
“11”: From the beginning address to (the beginning address + 3)

[Circulating mode example] When writing #02h to the sub address to operate in the address circulating mode (ISAM = 1)

Start Condition	Slave address	Sub address	DATA 1	DATA 2	DATA 3	DATA 4	DATA 5	----------
At ICYC="00"		02h	(02h)	(02h)	(02h)	(02h)	(02h)	----------
At ICYC="01"		02h	(02h)	(03h)	(02h)	(03h)	(02h)	----------
At ICYC="10"		02h	(02h)	(03h)	(04h)	(02h)	(03h)	----------
At ICYC="11"		02h	(02h)	(03h)	(04h)	(05h)	(02h)	----------

■ PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

[Notes in Use]

The analog input section of ML86V7675 is developed based on the standard video signal. We have improved it to obtain a stable behavior for nonstandard video signals as well. However, a stable behavior for every signal is not guaranteed, since there are various situations in the signal condition and usage environment such as airwave signals received in light electric field areas, VTR playback signals, video signals with switching signal sources, noise contamination signals, and simplified video signals of various cameras and game machines.
Please thoroughly evaluate and examine the product in assumed signal conditions and usage environments before you adopt it.

■ Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL86V7675-01	2013.02.13	—	113	First edition issued
FEDL86V7675-02	2013.06.07	113	115	Add description of sampling setting mode (section 5.5, register #00h,#70h,#84h-#8Eh)
FEDL86V7675-03	2022.05.13	115	115	P20.revice line number
FEDL86V7675-04	2024.02.29	115	115	p.2 : Added applications and “Line up” p.115 : Updeted “Notice”

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