Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL-7650-03
Issue Date: Jan. 5, 2024

ML7650

13.56MHz wireless charging receiver LSI

1. Overview

ML7650 is a 13.56MHz wireless power receiver LSI. ML7650 realizes a wireless power transfer system by combining with the wireless power transmitter LSI ML7651, and can output 3W to a charging device.
ML7650 is equipped with a 10-bit SA-ADC for measuring the power charging status and a wireless power charging control function in a 2.28 mm x 2.61 mm (equivalent to 2.44 mm square) WL-CSP chip or a 5 mm square 32-pin WQFN package. This LSI is ideal for wireless power transfer of small devices. Furthermore, ML7650 is equipped with a host interface (SPI / I^2C slave) function, and it is possible to update configuration data from an external MCU.

2. Features

- Charging control
  - Built-in Charging control circuit
    Built-in setting of output voltage by shunt regulator
    Voltage/Current supply ON/OFF function to external charging IC
    3W receiving available
  - Abnormally detection function by software and hardware control
  - Abnormally notification function to the power transmission side

- Communication control
  - Communication speed: 212kbps, 424kbps
  - 2Kbyte data flash for storing user data

- Host interface
  - 1ch Serial interface (Slave), and selectable from SPI or I^2C

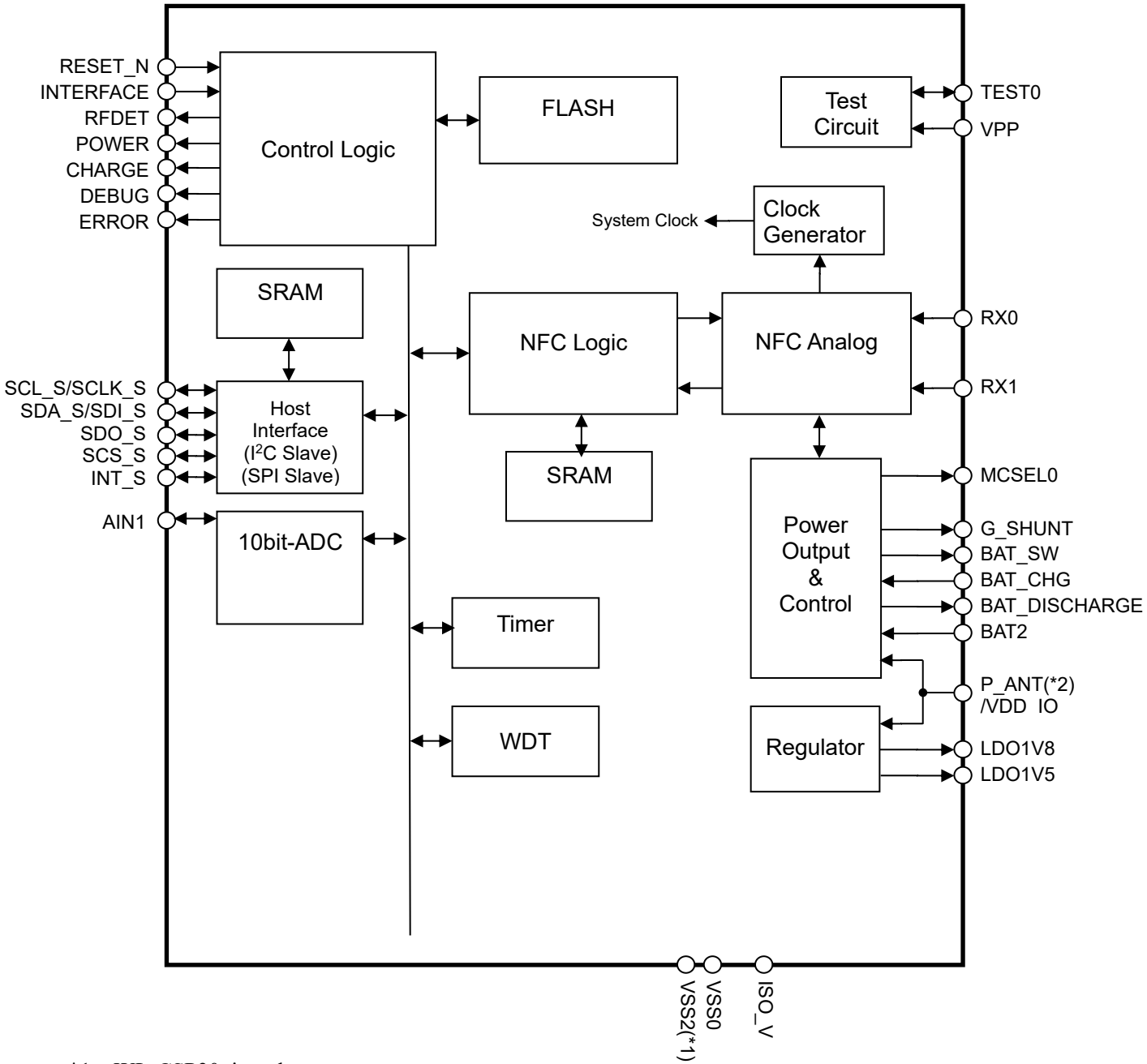
- Package
  - WL-CSP30pin (S-UFLGA30-2.28x2.61-0.40-W)
  - WQFN32pin (P-WQFN32-0505-0.50-A63)

- Product name
  ML7650-F00GD (WQFN)
  ML7650-F00HB (WL-CSP)

- Applications
  NFC charging devices, e.g.
  ・smart wathes, fitness Trackers and smart wristbands
  ・smart rings
  ・smart glasses
  ・true wireless stereos and hearing aids
  ・stylus pens, wireless mouses and wireless keyboads
  ・electric toothbrushes
  ・beauty home appliances
  ・personal health care devices
  ・battery packs

ROHM SEMICONDUCTOR

3. Block Diagram



*1 WL-CSP30pin only
*2 WQFN32pin only

4. Pin Assignment

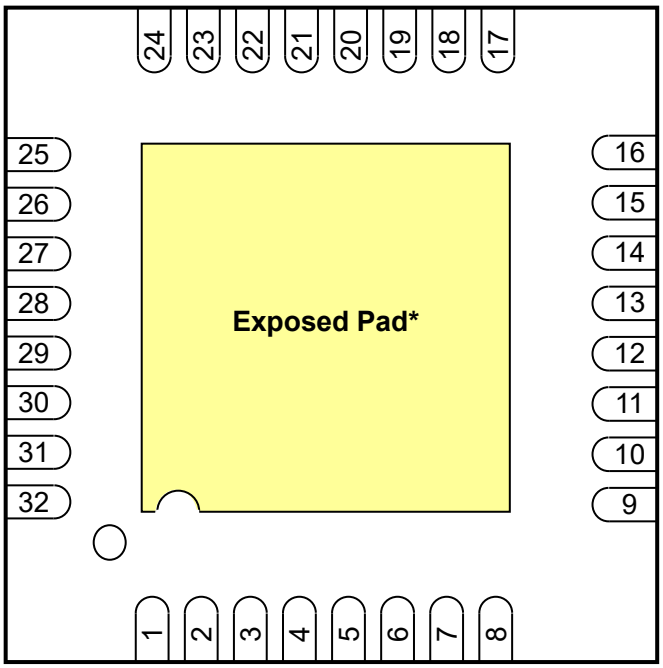
WL-CSP 30pin

BOTTOM VIEW

E6	D6	C6	B6	A6	6
E5	D5	C5	B5	A5	5
E4	D4	C4	B4	A4	4
E3	D3	C3	B3	A3	3
E2	D2	C2	B2	A2	2
E1	D1	C1	B1	A1	1
E	D	C	B	A	

WQFN 32pin

TOP VIEW



*Solder the exposed pad to GND on the PCB

5. Pin Description

5.1 Power, GND, Reference Voltage Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
C4/14	VSS0	—	—	—	Ground (VSS0 to VSS2 are connected inside the LSI, respectively)	—
C3	VSS2					
D6/15	VDD_IO	—	—	—	Logic IO voltage supply pin	—
E1/25	LDO1V5	H(A)	O_A	—	This pin for connecting decoupling capacitor of internal LDO (Core 1.5V)	—
D1/26	LDO1V8	H(A)	O_A	—	This pin for connecting decoupling capacitor of internal LDO (ADC 1.8V)	—
31	P_ANT	—	—	—	Input pin of the output of a rectifier circuit. (In WL-CSP Package, the output of a rectifier circuit should be input to VDD_IO)	—
E2/24	ISO_V	—	—	—	Logic IO voltage supply pin (for host communication)	—
C1/27	BAT2	—	I_A	—	Battery voltage monitor pin	—

5.2 Analog Signal Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
B1/29	RX0	—	I_A	—	Antenna (Plus)	—
B2/28	RX1	—	I_A	—	Antenna (Minus)	—

5.3 Other Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
D2/4	RESET_N	PU	I	VDD_IO	L	Reset input pin	Open
E3/23	SDA_S / SDI_S	Z	I/O	ISO_V	—	I^2C slave data input/output pin SPI slave data input pin	Open
D3/22	SCL_S / SCLK_S	Z	I/O	ISO_V	—	I^2C slave clock input pin SPI slave clock input pin	Open
B4/6	Not Used	Z	I/O	ISO_V	—	Not used	Open
A4/5	INTERFACE	Z	I/O	ISO_V	L: SPI H or Open: I^2C	Host communication interface select input pin	Open
E4/21	INT_S	Z	I/O	ISO_V	L	Interrupt output pin	Open
D4/20	SDO_S	Z	I/O	ISO_V	—	SPI slave data output pin	Open
E5/19	SCS_S	Z	I/O	ISO_V	—	SPI slave chip select input pin	Open
10	Not Used	Z	I_A	VDD_IO	—	Not used	Open
B6/11	AIN1	Z	I_A	VDD_IO	—	ADC input pin for current measurement	Open
A2/32	BAT_SW	PU	I/O	VDD_IO	L	Power supply ON/OFF output pin for charging IC	Open
D5/18	RFDET	Z	I_{DA}/O	ISO_V	Selectable	Magnetic field detection signal output pin It becomes active by detecting the magnetic field.	Open

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
A5/7	POWER	Z	I/O	ISO_V	—	LED0 (Power) Turns on after initialization is completed.	Open
E6/17	BAT_CHG	Z	I_{DA}/O	VDD_IO	Selectable	Full charge status input pin Connect to the full charge status signal of charging IC	Open
A6/9	CHARGE	Z	I/O	ISO_V	—	LED1 (Charging) Turns on during charging	Open
B3/3	DEBUG	Z	I/O	VDD_IO	—	Debug pin	Open
A3/2	BAT_DISCHARGE	Z	I/O_{DA}	VDD_IO	L	Discharge control pin for charging capacitor	Open
B5/8	ERROR	Z	I/O	ISO_V	—	LED2 (Error) Turns on when an abnormality is notified.	Open
C6/13	MCSEL0	PU	O	VDD_IO	Selectable	Matching circuit configuration signal output pin #1	Open
12	Not Used	PU	O	VDD_IO	—	Not used	Open
A1/30	G_SHUNT	L(A)	O	P_ANT	—	Shunt transistor control signal output pin	Open

5.4 Test Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
C2/1	TEST0	Z	I/O	VDD_IO	L	Input/Output pin for debugger	Pull-Up
C5/16	VPP	—	I_A	—	—	Power supply pin for test	Open

(*1) In reset state :

Pin state definition in reset state	L(O)	:	“L” level output
	H(O)	:	“H” level output
	L(A)	:	Analog “L” level output
	H(A)	:	Analog “H” level output
	PU	:	Pull-Up
	PD	:	Pull-Down
	Z	:	Floating state

(*2) I/O : I/O definitions use abbreviations

I/O definition	I_A	:	Analog input pin
	O_A	:	Analog output pin
	I	:	Digital input pin
	I/O	:	Bi-directional pin
	I_{DA}/O	:	Bi-directional pin, Input are digital and analog shared
	I/O_{DA}	:	Bi-directional pin, Output are digital and analog shared
	O	:	Digital output pin

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power voltage	VDD_IO	Ta=25°C	-0.3 to +6.5	V
	ISO_V	Ta=25°C	-0.3 to +6.5	V
	P_ANT	Ta=25°C	-0.3 to +6.5	V
	BAT2	Ta=25°C	-0.3 to +6.5	V
Core power voltage	LDO1V5	Ta=25°C	-0.3 to +2.0	V
Analog power voltage	LDO1V8	Ta=25°C	-0.3 to +6.5	V
Input voltage	V_{DIN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
		Ta=25°C, RX0/RX1	12	V
Input current	Ii	Ta=25°C	-10 to +10	mA
	I_{P_ANT}	Ta=25°C	100	mA
Output voltage	V_{DO}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Digital output current	I_{DO}	Ta=25°C	-12 to +20	mA
Power dissipation (QFN)	PD	Ta=25°C	1	W
Power dissipation (CSP)	PD	Ta=25°C	0.5	W
Storage temperature	T_{stg}	—	-55 to +150	°C

V_{DD} : In the Pin Description table, VDD for pins indicated by VDD_IO in the "Supply power" column will be the VDD_IO voltage, and VDD for pins indicated by ISO_V will be the ISO_V voltage.e.

6.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD_IO	—	1.8	—	5.5	V
	ISO_V	—	1.8	—	5.5	V
	P_ANT	During communication	2.0	5.0	5.5	V
		During charging	—	—	5.5	V
Operating temperature	Ta	—	-40	+25	+85	°C
LDO1V5 outside Capacitor	C_{LDO1V5}	—	Typ. -10%	2.2	Typ. +10%	µF
P_ANT outside Capacitor	C_{PANT}	—	Typ. -10%	2.2	Typ. +10%	µF
LDO1V8 outside Capacitor	C_{LDO1V8}	—	Typ. -10%	0.47	Typ. +10%	µF
VDD_IO outside Capacitor	C_{VDDIO}	—	Typ. -10%	0.1	Typ. +10%	µF
ISO_V outside Capacitor	C_{ISOV}	—	Typ. -10%	0.1	Typ. +10%	µF
Antenna input frequency	F_{ANT}	—	Typ. -0.05%	13.56	Typ. +0.05%	MHz

6.3 Flash Memory Operating Conditions

(VDD_IO=2.7 to 5.5V, P_ANT=2.7 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Range	Unit
Rewrite count	C_{EPD}	Data Flash	10,000	Times

6.4 RF Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Level	V_{RX1}	RX0/RX1	2.0	–	5.9	V
Input data amplitude	V_{RX2}	RX0/RX1	50	–	–	mV
Communication speed	F_{RX}	RX0/RX1		212		kbps
				424		kbps

6.5 Notification Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
P_ANT limiter	V_{PANT1}	Normal	–	–	5.5	V
	V_{PANT2}	In case of abnormality notice	–	3.0	–	V

6.6 AC Characteristics (I^2C Bus Interface)

● Standard Mode 100kHz

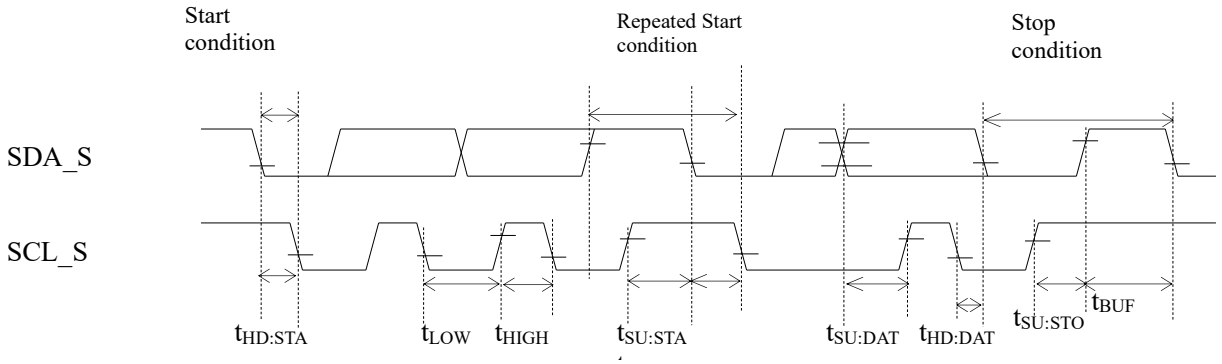
(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	100	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL_S "L" level time	t_{LOW}	–	4.7	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus free time	t_{BUF}	–	4.7	–	–	µs

● Fast Mode 400kHz

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	400	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL_S "L" level time	t_{LOW}	–	1.3	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus free time	t_{BUF}	–	1.3	–	–	µs

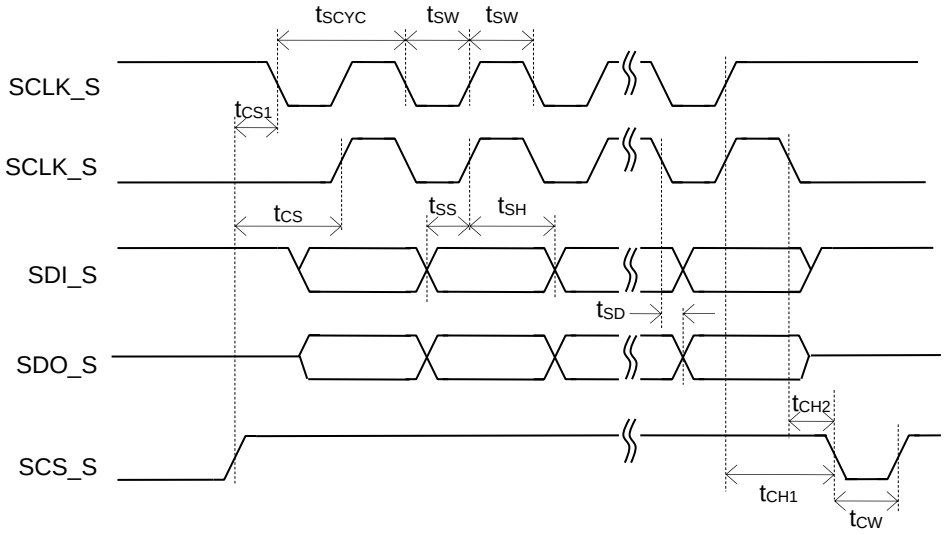


If powering off ISO_V of this LSI, it disables communications of other devices on the I^2C bus.
Even when there is no receiving power from the P_ANT pin, the SDA_S/SCL_S pin will maintain the Hi-Z state when there is a power input on the ISO_V pin of this LSI.

6.7 AC Characteristics (Host Interface: SPI slave)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S input cycle	t_{SCYC}	–	500	–	–	ns
SCLK_S input pulse width	t_{SW}	–	200	–	–	ns
SCS_S setup time	t_{CS1}	–	80	–	–	ns
	t_{CS2}	–	80	–	–	ns
SCS_S hold time	t_{CH1}	–	80	–	–	ns
	t_{CH2}	–	80	–	–	ns
SCS_S input pulse width	t_{CW}	–	80	–	–	ns
SDO_S output delay time	t_{SD}	–	–	–	240	ns
SDI_S input setup time	t_{SS}	–	80	–	–	ns
SDI_S input hold time	t_{SH}	–	80	–	–	ns



6.8 IO Characteristics

(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1	VOH1	IOH=-1.0mA	V_{DD}-0.5	–	–	V
	VOL1	IOL=+0.5mA	–	–	0.4	V
Output voltage 2 (LED mode selected)	VOL2	2.7V ≤ V_{DD} ≤ 5.5V IOL=+5.0mA	–	–	0.6	V
		IOL=+2.0mA	–	–	0.4	V
Output voltage 3 (I^2C mode selected)	VOL3	IOL3= +3mA (I^2C spec) (VDD_IO ≥ 2V、ISO_V ≥ 2V)	–	–	0.4	V
Output voltage 4 (I^2C mode selected)	VOL4	IOL4= +2mA (I^2C spec) (VDD_IO < 2V、ISO_V < 2V)	–	–	V_{DD}×0.2	V
Output leakage 1	IOOH1	VOH=V_{DD} (at high impedance)	–	–	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	–	–	μA
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	–	–	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	–	–	1	μA
	IIL2	VIL2=VSS	-200	-15	-1	μA
Input current 3	IIH3	VIH3=V_{DD} (when pull-down)	1	15	200	μA
	IIL3	VIL3=VSS (when pull-down)	-200	-15	-1	μA
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	–	–	μA
Input voltage 1	VIH1	–	0.75×V_{DD}	–	V_{DD}	V
	VIL1	–	0	–	0.3×V_{DD}	V
Input pin capacitance	CIN	f=10kHz Vrms=50mV Ta=25°C	–	10	–	pF
Leak current	I_{ISOV}	Voltage supply to the ISO_V terminal, no magnetic field input	–	100	–	nA

V_{DD} : Refer to Pin Description table, in case “Supply Power” column equals “VDD_IO”, VDD is VDD_IO voltage and column equals “ISO_V”, VDD is ISO_V voltage.
Typ. : Standard is at Ta=25°C, VDD_IO=3.0V

6.9 Current Consumption

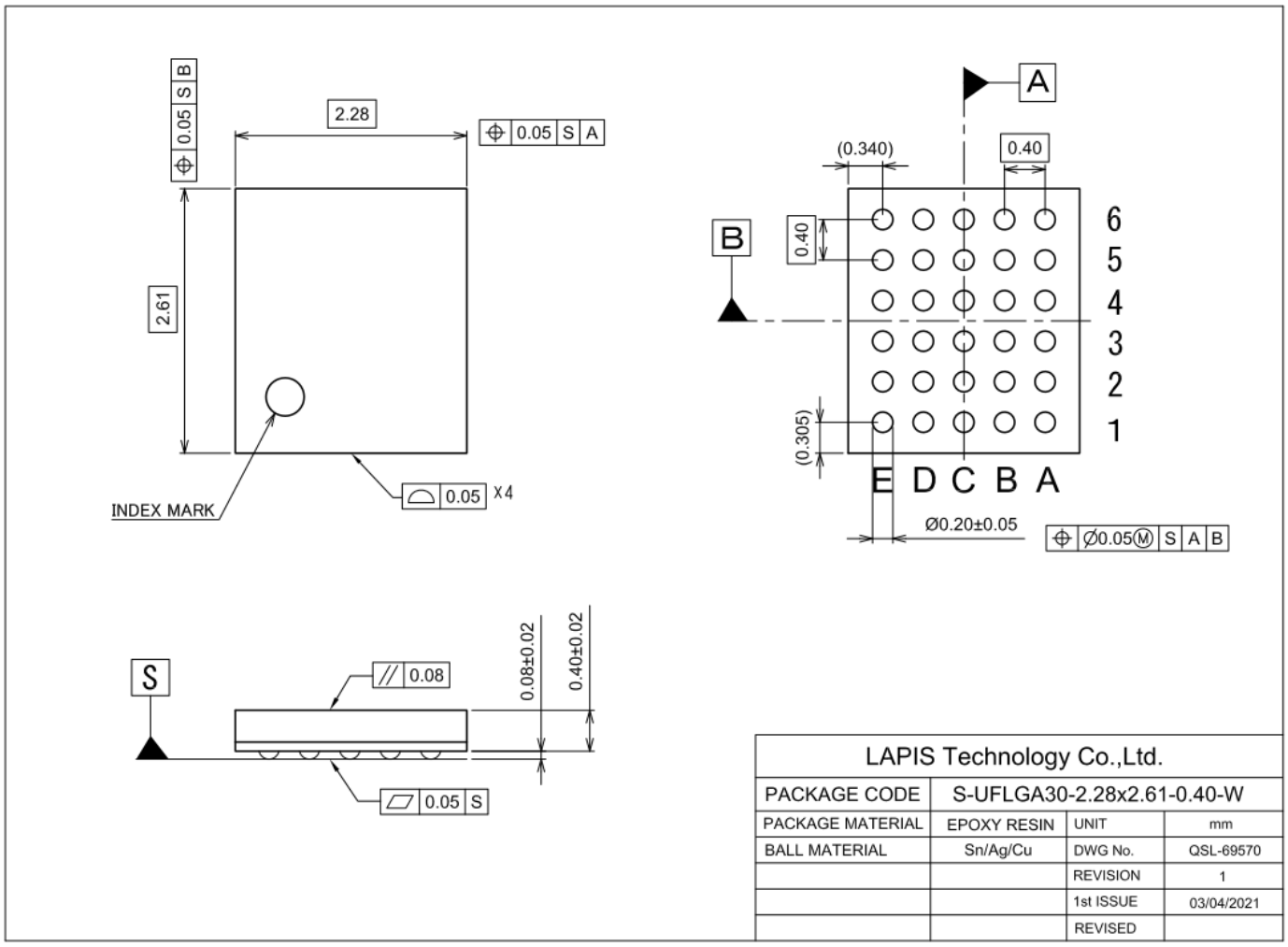
(VDD_IO=1.8 to 5.5V, P_ANT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	P_ANT	During Communication	0.5	—	—	mA
		During Charging	—	—	10	mA

* Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External transistor current is not included.

7. Package Dimensions

WL-CSP30pin

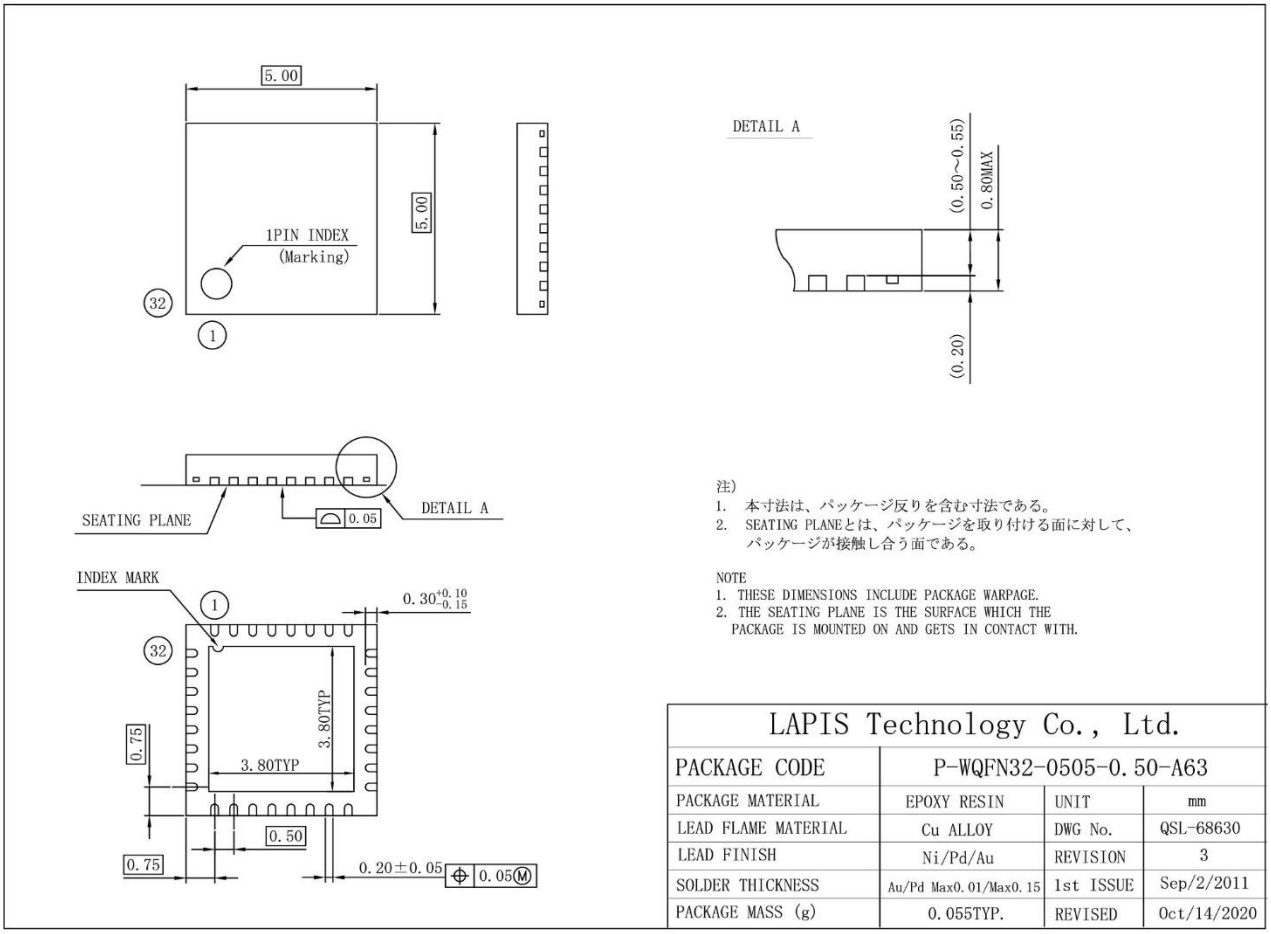


LAPIS Technology Co.,Ltd.			
PACKAGE CODE	S-UFLGA30-2.28x2.61-0.40-W		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
BALL MATERIAL	Sn/Ag/Cu	DWG No.	QSL-69570
		REVISION	1
		1st ISSUE	03/04/2021
		REVISED	

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

WQFN32pin



注)
1. 本寸法は、パッケージ反りを含む寸法である。
2. SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。

NOTE
1. THESE DIMENSIONS INCLUDE PACKAGE WARPAGE.
2. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN32-0505-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68630
LEAD FINISH	Ni/Pd/Au	REVISION	3
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/2/2011
PACKAGE MASS (g)	0.055TYP.	REVISED	Oct/14/2020

Notes for Mounting the Surface Mount Type Package
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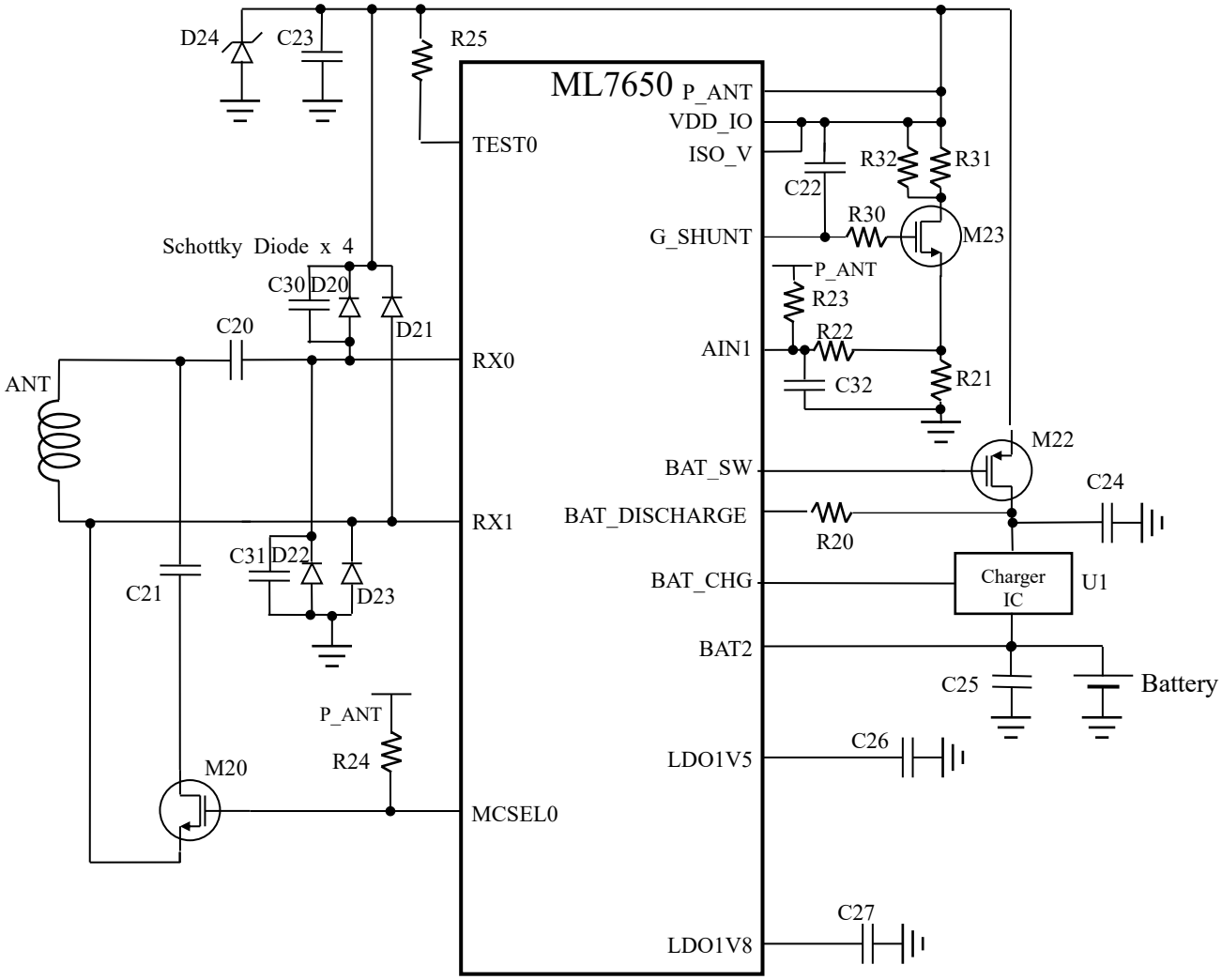
8. Application Circuit Example



Revision History

Document No.	Issue Date	Page		Change Contents
		Previous Edition	Current Edition	
FEDL7650-01	2023.6.7	-	-	First edition
FEDL7650-02	2023.12.15	1	1	Added product name and appications
		14	14	Modified Application Circuit Example
FEDL7650-03	2024.1.5	16	16	Modified Notes

Notes

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2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
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