



Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML7651

13.56MHz wireless charging transmitter LSI

1. Overview

ML7651 is a 13.56MHz wireless power transmitter LSI. ML7651 realizes a wireless power transfer system by combining with the wireless power receiver LSI ML7650, and can output 3W to ML7650.

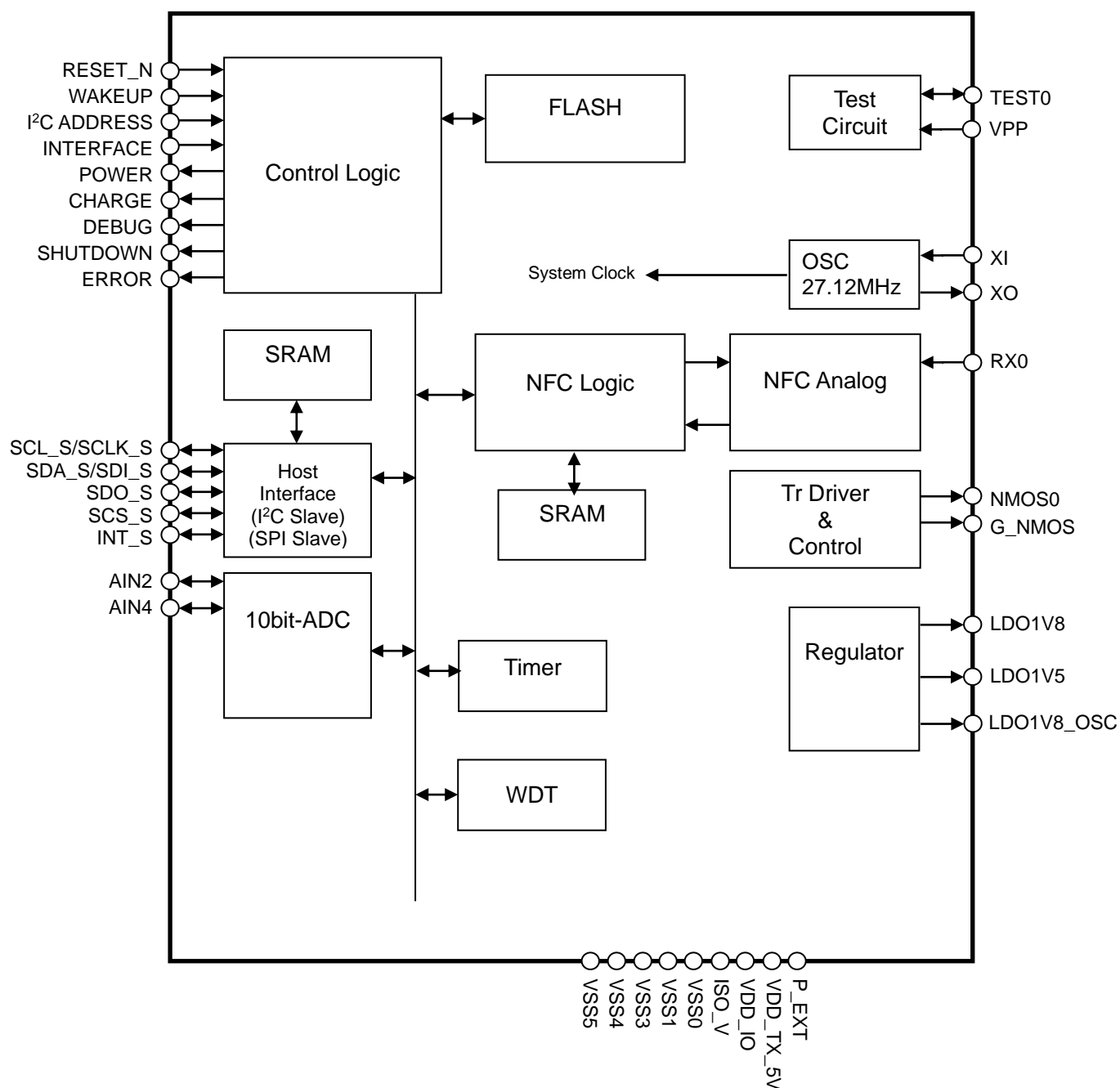
ML7651 has a communication command generation function for communicating with ML7650, an external transistor control function for supplying 1W, a function for variably controlling the transmission amount to optimize the transmission power, and a function to detect abnormalities when ML7650 is attached/detached or power is transmitted. All of these functions are included in the 40-pin WQFN package (6.0 mm square), and ML7651 is ideal for wireless power transfer of small devices. In addition, the operating voltage is 5V, and it can be driven from a USB power source such as a mobile battery. Furthermore, ML7651 is equipped with a host interface (SPI / I²C slave) function, and it is possible to update configuration data from an external MCU.

2. Features

- Charging control
 - Built-in 13.56MHz power transmission control circuit
 - 3W power transmission transistor control output
 - Abnormally detection function by software and hardware control
- Communication control
 - Equipped with a command generation function for communication with ML7650
 - Communication speed: 212kbps, 424kbps
 - 2Kbyte data flash for storing user data
- Host interface
 - 1ch Serial interface (Slave), and selectable from SPI or I²C
- Package
 - WQFN40pin (P-WQFN40-0606-0.50-63)
- Product name
ML7651-F00GD (WQFN)
- Applications
NFC charging devices, e.g.
 - smart wathes, fitness Trackers and smart wristbands
 - smart rings
 - smart glasses
 - true wireless stereos and hearing aids
 - stylus pens, wireless mouses and wireless keyboards
 - electric toothbrushes
 - beauty home appliances
 - personal health care devices
 - battery packs



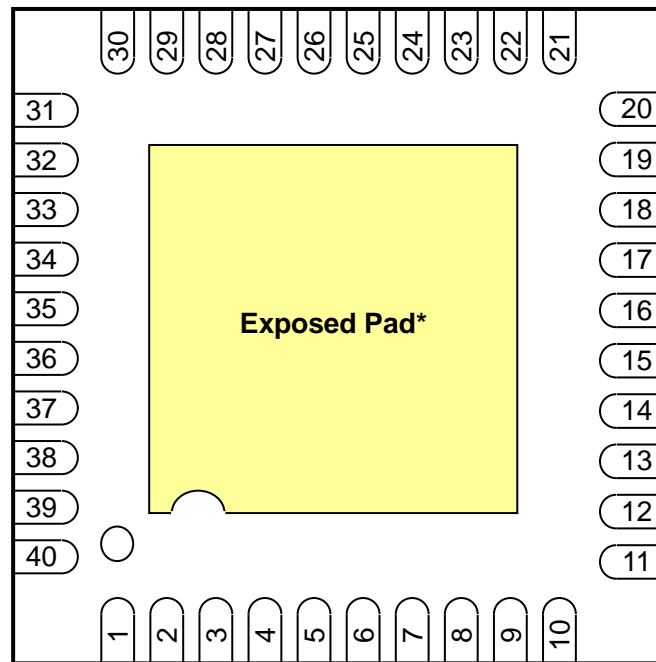
3. Block Diagram



4. Pin Assignment

WQFN 40pin

TOP VIEW



*Solder the exposed pad onto the PCB

5. Pin Description

5.1 Power, GND, Reference Voltage Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
15	VSS0	—	—	—	Ground (VSS0 to VSS5 are connected inside the LSI, respectively)	—
16	VSS1					
29	VSS3					
36	VSS4					
12	VSS5					
17	VDD_IO	—	—	—	Logic IO voltage supply pin	—
34	LDO1V5	H(A)	OA	—	This pin for connecting decoupling capacitor of internal LDO (Core 1.5V)	—
35	LDO1V8	H(A)	OA	—	This pin for connecting decoupling capacitor of internal LDO (ADC 1.8V)	—
31	LDO1V8_OSC	H(A)	OA	—	This pin for connecting decoupling capacitor of internal LDO (Oscillator 1.8V)	—
40	P_EXT	—	—	—	Main power supply pin of this LSI (5V)	—
26	ISO_V	—	—	—	Logic IO voltage supply pin (for host communication)	—
27	VDD_TX_5V	—	—	—	Power supply pin for driver (5V)	—

* Connect ISO_V to VDD_IO on the board

5.2 Analog Signal Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
37	RX0	—	IA	—	—	RF data receiving	—
30	G_NMOS	PD	OA	VDD_TX_5V	—	NMOS transistor bias output pin for power transmission	—
28	NMOS0	Z	OA	VDD_TX_5V	—	NMOS transistor driver output pin for power transmission	—

5.3 Clock Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
32	XI	I	I	LDO1V8_OSC	—	27.12MHz oscillation input pin	—
33	XO	O	O	LDO1V8_OSC	—	27.12MHz oscillation output pin	—

5.4 Other Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
5	RESET_N	PU	I	VDD_IO	L	Reset input pin	Open
25	SDA_S / SDI_S	Z	I/O	ISO_V	—	I ² C slave data input/output pin SPI slave data input pin	Open
24	SCL_S / SCLK_S	Z	I/O	ISO_V	—	I ² C slave clock input pin SPI slave clock input pin	Open
7	P02	Z	I/O	ISO_V	—	DCDC Converter control pin1	Open
6	WAKEUP	Z	I/O	ISO_V	—	WAKEUP request input pin from the host	Open
23	INT_S	Z	I/O	ISO_V	—	Interrupt output pin	Open

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
22	SDO_S	Z	I/O	ISO_V	—	SPI slave data output pin	Open
21	SCS_S	Z	I/O	ISO_V	—	SPI slave chip select input pin	Open
11	Not Used	Z	I _A	VDD_IO	—	Not used	Open
13	Not Used	Z	I _A	VDD_IO	—	Not used	Open
39	AIN2	Z	I _A	P_EXT	—	ADC input pin for current measurement	Open
38	AIN4	Z	I _A	P_EXT	—	Receiver notification signal detection pin	Open
1	I ² C ADDRESS	PU	I/O	VDD_IO	—	I ² C slave address select input pin	Open
20	INTERFACE	Z	I _{DA} /O	ISO_V	L: SPI H or Open: I ² C	Host communication interface select input pin	Open
8	POWER	Z	I/O	ISO_V	—	LED0 (Power) Turns on after initialization is completed.	Open
19	P13	Z	I _{DA} /O	VDD_IO	—	DCDC Converter control pin2	Open
10	CHARGE	Z	I/O	ISO_V	—	LED1 (Charging) Turns on during charging	Open
4	DEBUG	Z	I/O	VDD_IO	—	Debug pin	Open
3	SHUTDOWN	Z	I/O _{DA}	VDD_IO	—	Shutdown request signal output pin to the host.	Open
9	ERROR	Z	I/O	ISO_V	—	LED2 (Error) Turns on when an abnormality is notified.	Open
14	Not Used	PU	O	VDD_IO	—	Not used	Open

5.5 Test Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
2	TEST0	Z	I/O	VDD_IO	L	Input/Output pin for debugger	Pull-Up
18	VPP	—	I _A	—	—	Power supply pin for test	Open

(*1) In reset state :

Pin state definition in reset state	L(O)	: "L" level output
	H(O)	: "H" level output
	L(A)	: Analog "L" level output
	H(A)	: Analog "H" level output
	PU	: Pull-Up
	PD	: Pull-Down
	Z	: Floating state

(*2) I/O : I/O definitions use abbreviations

I/O definition	I _A	: Analog input pin
	O _A	: Analog output pin
	I	: Digital input pin
	I/O	: Bi-directional pin
	I _{DA} /O	: Bi-directional pin, Input are digital and analog shared
	I/O _{DA}	: Bi-directional pin, Output are digital and analog shared
	O	: Digital output pin

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power voltage (Digital IO)	VDD_IO	Ta=25°C	-0.3 to +6.5	V
	ISO_V	Ta=25°C	-0.3 to +6.5	V
Regulator Input voltage	P_EXT	Ta=25°C	-0.3 to +6.5	V
Power voltage (Power transmission)	VDD_TX_5V	Ta=25°C	-0.3 to +6.5	V
Core power voltage / Crystal oscillator voltage	LDO1V5	Ta=25°C	-0.3 to +2.0	V
Analog power voltage	LDO1V8	Ta=25°C	-0.3 to +6.5	V
27.12MHz oscillator power voltage	LDO1V8_OSC	Ta=25°C	-0.3 to +6.5	V
Input voltage	VDIN	Ta=25°C	-0.3 to VDD_IO+0.3	V
		Ta=25°C, RX0	-0.3 to +6.5	V
Input current	Ii	Ta=25°C	-10 to +10	mA
Output voltage	VDO	Ta=25°C	-0.3 to VDD_IO+0.3	V
Digital output current	IDO	Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	1	W
Storage temperature	Tstg	—	-55 to +150	°C

6.2 Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD_IO	—	1.8	—	5.5	V
	ISO_V	Connect with VDD_IO on the board	1.8	—	5.5	V
	P_EXT	—	4.5	5.0	5.5	V
	VDD_TX_5V	—	4.5	5.0	5.5	V
Operating temperature	Ta	—	-40	+25	+85	°C
Crystal oscillator frequency	f _{XTL}	—	Typ. -0.05%	27.12	Typ. +0.05%	MHz
Crystal oscillator load capacitance	C _{DL} C _G L	NIHON DEMPA KOGYO Co., Ltd. NX2016SA (CL=6pF)	Typ. -1%	8	Typ. +1%	pF
	C _{DL} C _G L	NIHON DEMPA KOGYO Co., Ltd. NX2016SA (CL=8pF)	Typ. -1%	12	Typ. +1%	pF
	C _{DL} C _G L	KYOCERA Corporation CX1210SB (CL=6pF)	Typ. -1%	8	Typ. +1%	pF
	C _{DL} C _G L	KYOCERA Corporation CX2016DB (CL=8pF)	Typ. -1%	12	Typ. +1%	pF
	C _{DL} C _G L	TXC SMD SEAM SEALING XTAL 2.0 x 1.6 (CL=8pF)	Typ. -1%	12	Typ. +1%	pF
LDO1V5 outside Capacitor	C _{LDO1V5}	—	Typ. -10%	2.2	Typ. +10%	μF
P_EXT outside Capacitor	C _{PEXT}	—	Typ. -10%	2.2	Typ. +10%	μF
LDO1V8 outside Capacitor	C _{LDO1V8}	—	Typ. -10%	0.47	Typ. +10%	μF
LDO1V8_OSC outside Capacitor	C _{LDO1V8OSC}	—	Typ. -10%	0.47	Typ. +10%	μF
VDD_IO outside Capacitor	C _{VDDIO}	—	Typ. -10%	0.1	Typ. +10%	μF
VDD_TX_5V outside Capacitor	C _{TX5V}	—	Typ. -10%	2.2	Typ. +10%	μF

6.3 Flash Memory Operating Conditions

(VDD_IO=2.7 to 5.5V, P_EXT=2.7 to 5.5V, VSS=0V, Ta=-40 to +85°C)

項目	記号	条件	範囲	単位
Rewrite count	C _{EPD}	Data Flash	10,000	times

6.4 Power Transmission Characteristics

(VDD_IO=1.8 to 5.5V, VDD_TX_5V=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
nmos0 output frequency	F _{TX}	—	—	13.56	—	MHz

6.5 AC Characteristics (I²C Bus Interface)

● Standard Mode 100kHz

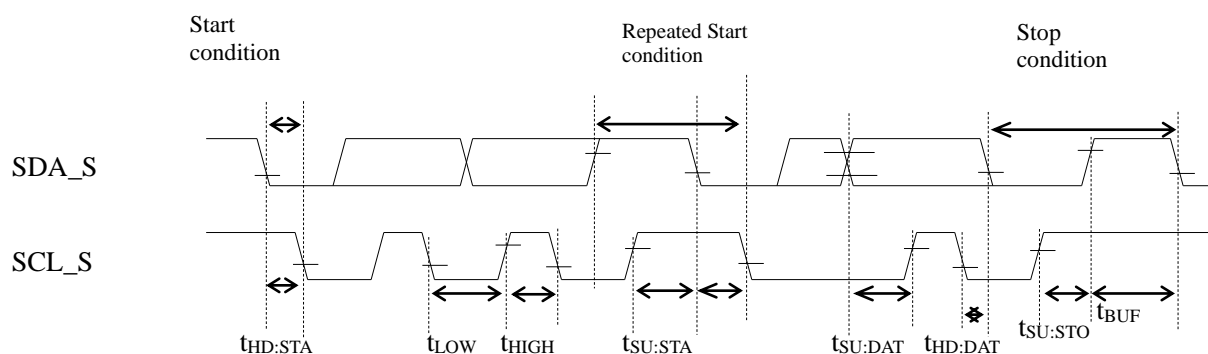
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f _{SCL}	—	—	—	100	kHz
SCL_S hold time (start/repeated start condition)	t _{HD:STA}	—	4.0	—	—	μs
SCL_S "L" level time	t _{LOW}	—	4.7	—	—	μs
SCL_S "H" level time	t _{HIGH}	—	4.0	—	—	μs
SCL_S setup time (repeated start condition)	t _{SU:STA}	—	4.7	—	—	μs
SDA_S hold time	t _{HD:DAT}	—	0	—	—	μs
SDA_S setup time	t _{SU:DAT}	—	0.25	—	—	μs
SDA_S setup time (P: Stop condition)	t _{SU:STO}	—	4.0	—	—	μs
Bus free time	t _{BUF}	—	4.7	—	—	μs

● Fast Mode 400kHz

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f _{SCL}	—	—	—	400	kHz
SCL_S hold time (start/repeated start condition)	t _{HD:STA}	—	0.6	—	—	μs
SCL_S "L" level time	t _{LOW}	—	1.3	—	—	μs
SCL_S "H" level time	t _{HIGH}	—	0.6	—	—	μs
SCL_S setup time (repeated start condition)	t _{SU:STA}	—	0.6	—	—	μs
SDA_S hold time	t _{HD:DAT}	—	0	—	—	μs
SDA_S setup time	t _{SU:DAT}	—	0.1	—	—	μs
SDA_S setup time (P: Stop condition)	t _{SU:STO}	—	0.6	—	—	μs
Bus free time	t _{BUF}	—	1.3	—	—	μs

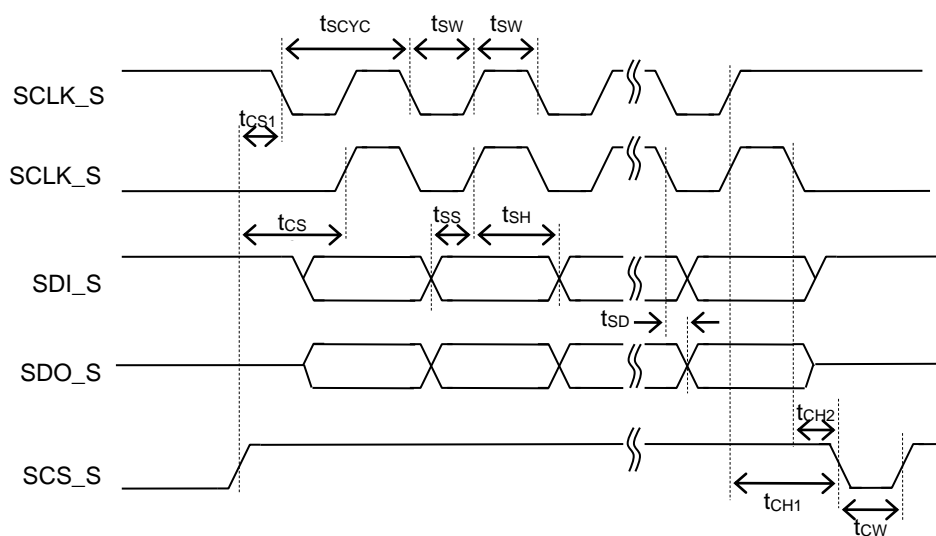


If powering off this LSI, it disables communications of other devices on the I²C bus.

6.6 AC Characteristics (Host Interface : SPI slave)

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S input cycle	t _{SCYC}	—	500	—	—	ns
SCLK_S input pulse width	t _{SW}	—	200	—	—	ns
SCS_S setup time	t _{CS1}	—	80	—	—	ns
	t _{CS2}	—	80	—	—	ns
SCS_S hold time	t _{CH1}	—	80	—	—	ns
	t _{CH2}	—	80	—	—	ns
SCS_S input pulse width	t _{CW}	—	80	—	—	ns
SDO_S output delay time	t _{SD}	—	—	—	240	ns
SDI_S input setup time	t _{SS}	—	80	—	—	ns
SDI_S input hold time	t _{SH}	—	80	—	—	ns



6.7 IO Characteristics

(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1	VOH1	IOH=-1.0mA	VDD_IO -0.5	—	—	V
	VOL1	IOL=+0.5mA	—	—	0.4	V
Output voltage 2 (LED mode selected)	VOL2	2.7V ≤ VDD_IO ≤ 5.5V IOL=+5.0mA	—	—	0.6	V
		IOL=+2.0mA	—	—	0.4	V
Output voltage 3 (I ² C mode selected)	VOL3	IOL3= +3mA (I ² C spec) (VDD_IO ≥ 2V)	—	—	0.4	V
Output voltage 4 (I ² C mode selected)	VOL4	IOL4= +2mA (I ² C spec) (VDD_IO < 2V)	—	—	VDD_IO ×0.2	V
Output leakage 1	IOOH1	VOH=VDD_IO (at high impedance)	—	—	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	—	—	μA
Input current 1 (RESET_N)	IIH1	VIH1=VDD_IO	—	—	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=VDD_IO	—	—	1	μA
	IIL2	VIL2=VSS	-200	-15	-1	μA
Input current 3	IIH3	VIH3=VDD_IO (when pull down)	1	15	200	μA
	IIL3	VIL3=VSS (when pull down)	-200	-15	-1	μA
	IIH3Z	VIH3=VDD_IO (at high impedance)	—	—	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	—	—	μA
Input voltage 1	VIH1	—	0.75× VDD_IO	—	VDD_IO	V
	VIL1	—	0	—	0.3× VDD_IO	V
Input pin capacitance	CIN	f=10kHz Vrms=50mV Ta=25°C	—	10	—	pF

Typ.: standard is at Ta=25°C, VDD_IO=3.0V

6.8 Current Consumption

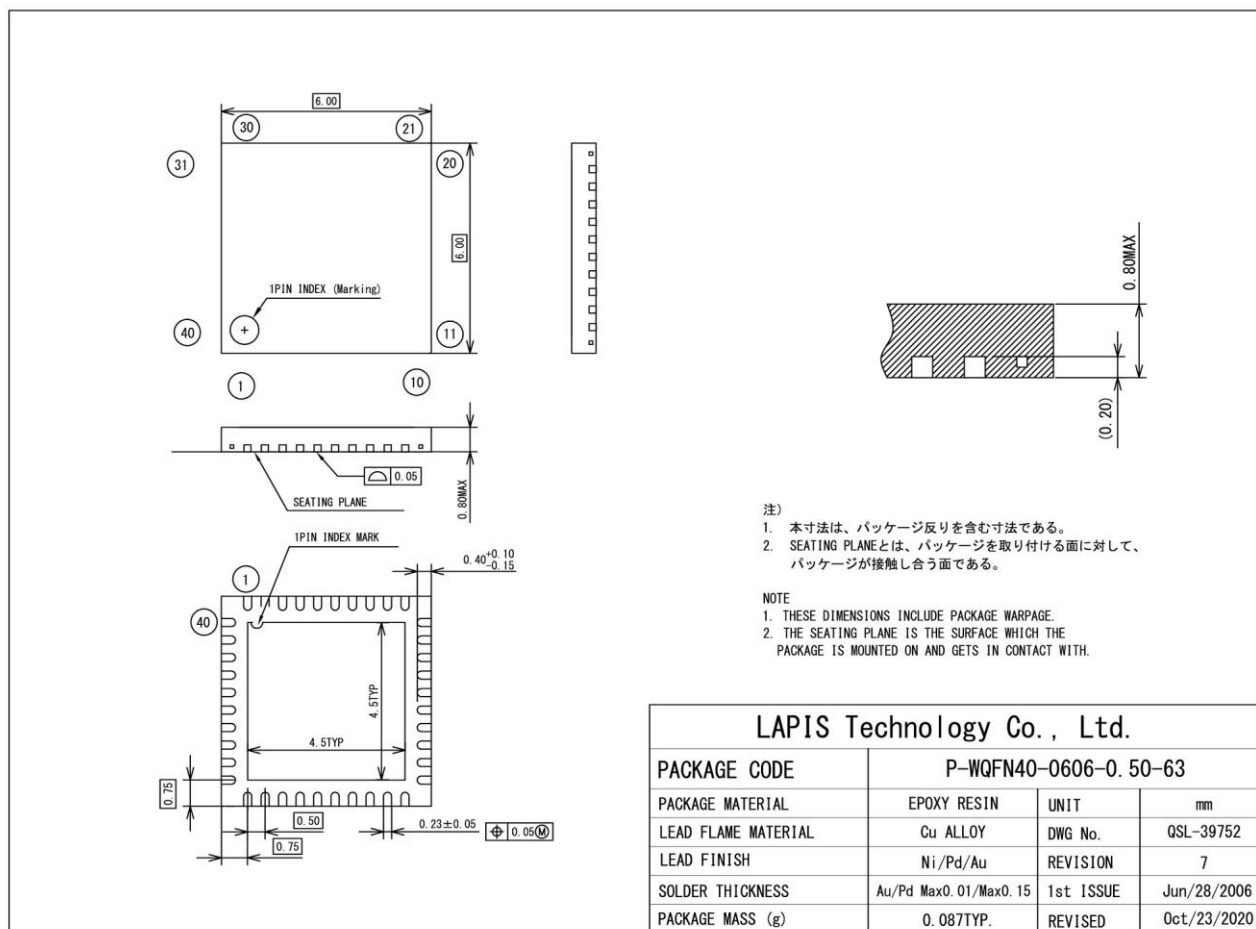
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	IDD1	HALT-H High speed clock stop	—	7	23.6	μA
	IDD2	HALT	—	1.3	2.0	mA
	IDD3	CPU 6.78MHz operation Peripherals stop	—	2.2	3.0	mA
	IDD4	CPU 6.78MHz operation During communication*	—	15	—	mA
	IDD5	CPU 6.78MHz operation During power transmission*	—	20	—	mA

* Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External transistor current is not included.

7. Package Dimensions

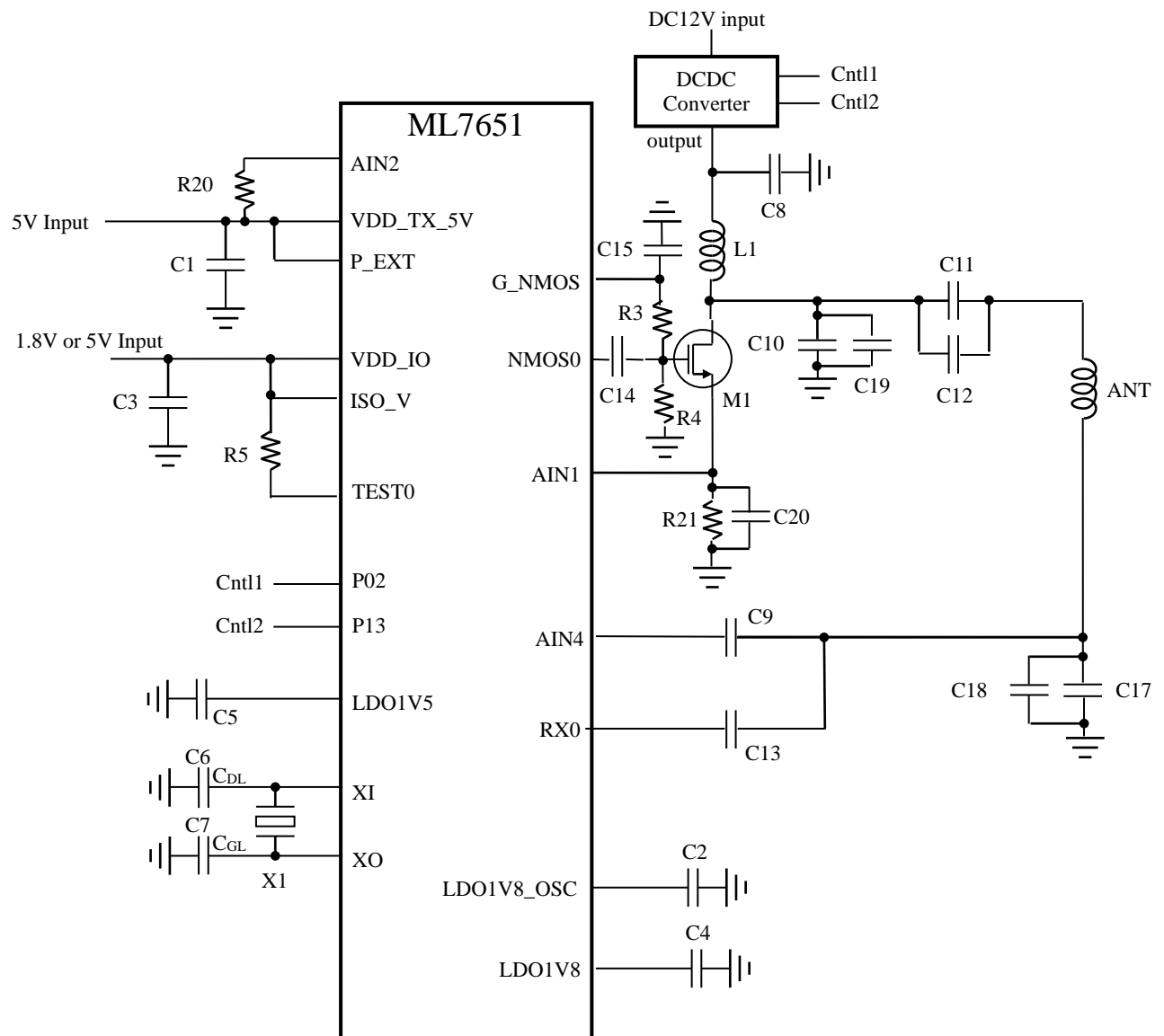
WQFN40 pin



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

8. Application Circuit Example



Revision History

Document No.	Issue Date	Page		Change contents
		Previous Edition	Current Edition	
FEDL7651-01	2023.6.7	-	-	First edition
FEDL7651-02	2023.12.15	1	1	Added product name and applications
		12	12	Modified Application Circuit Example
FEDL7651-03	2024.1.5	14	14	Modified Notes

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