ML7662

13.56MHz Wireless charging receiver LSI

■Overview

ML7662 is a 13.56MHz wireless power receiver LSI. ML7662 realizes a wireless power transfer system by combining with the wireless power transmitter LSI ML7663, and can output 1W to a charging device.

ML7662 is NFC Forum WLC* compliant. ML7662 can output power by combining with the NFC Forum WLC* compliant transmission device.

ML7662 is equipped with a 10-bit SA-ADC for measuring the power charging status and a wireless power charging control function in a 2.28 mm x 2.61 mm (equivalent to 2.44 mm square) WL-CSP chip or a 5 mm square 32-pin WQFN package. This LSI is ideal for wireless power transfer of small devices. In addition, since it is equipped with the NFC Forum Type 3 Tag function, it is possible to realize NFC functions such as Bluetooth® pairing by touch. Furthermore, ML7662 is equipped with a host interface (SPI / I2C Target) function, and it is possible to update configuration data from an external MCU.

*Note: NFC Forum WLC 2.0.

■Features

- Charging control
  - Built-in Charging control circuit
    Built-in setting of output voltage by shunt regulator
    Voltage/Current supply ON/OFF function to external charging IC
    1W receiving available
  - Abnormally detection function by software and hardware control
  - Abnormally notification function to the power transmission side

- Communication control
  - Communication speed: 212kbps, 424kbps
  - 2Kbyte data flash for storing user data

- Host interface
  - 1ch Serial interface (Target), and selectable from SPI or I2C

- Package
  - WL-CSP30pin (S-UFLGA30-2.28x2.61-0.40-W)
  - WQFN32pin (P-WQFN32-0505-0.50-A63)

- Applications
  - NFC charging devices, e.g.
  - smart watches, fitness trackers and smart wristbands
  - smart rings
  - smart glasses
  - true wireless stereos and hearing aids
  - stylus pens, wireless mouses and wireless keyboads
  - electric toothbrushes
  - beauty home appliances
  - personal health care devices
  - battery packs

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●Product name

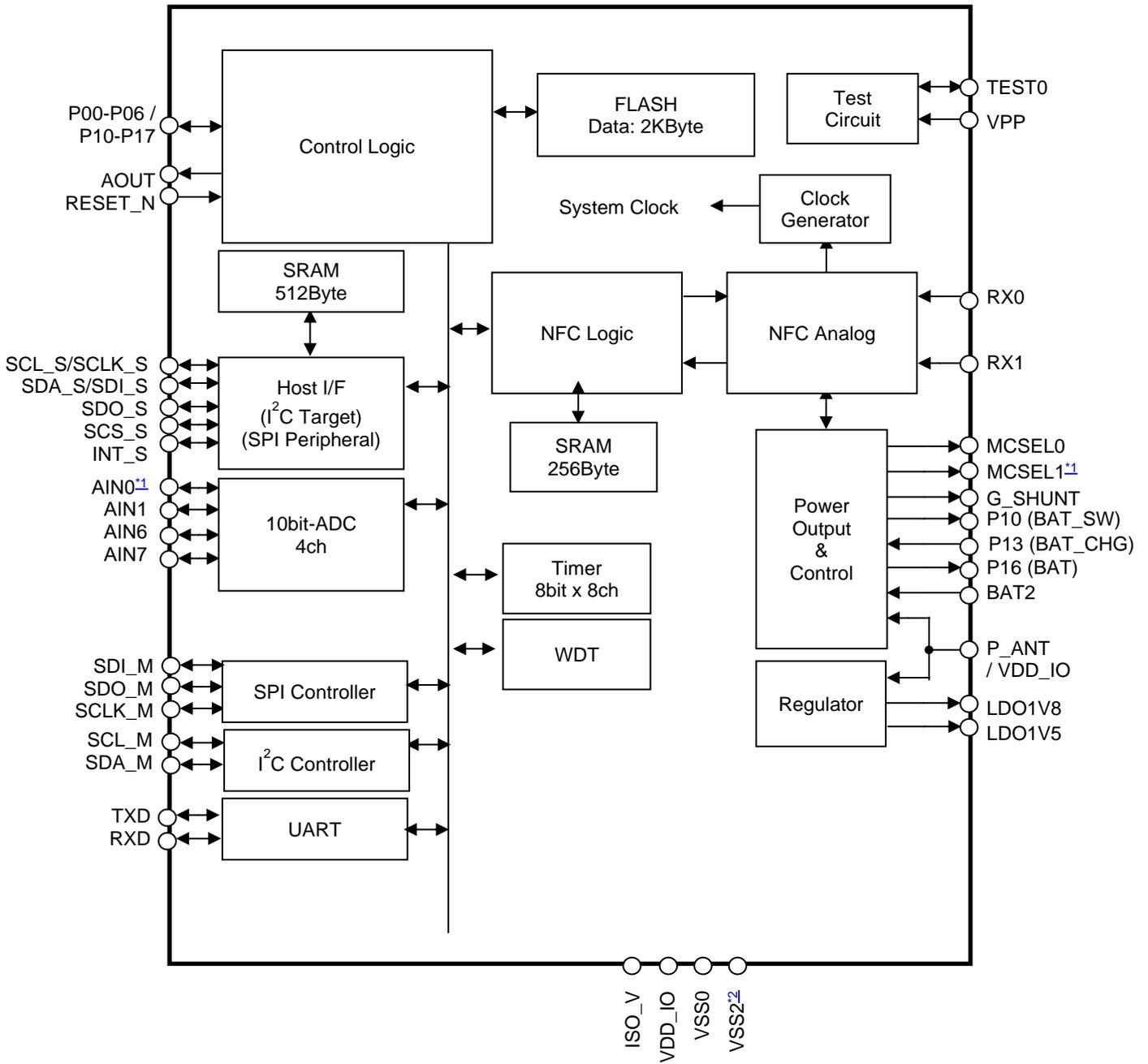　　　ML7662-J01GD(WQFN Packages)
　　　ML7662-J01HB(WLCSP Packages)

■Related Documents

In addition to this document, the following documents should also be read together as necessary.

・ML7663 Data Sheet
・ML7662 / ML7663 Application Note

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■Block Diagram

[*1] only WLCSP 30pin
[*2] only WQFN 32 pin

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■Pin Assignment

●WLCSP 30pin

BOTTOM VIEW

P13 / AIN7	VDD_IO	MCSEL0	AIN1	P14 / SCLK_M	6
P06 / SCS_S	P11 / AIN6	VPP	P17 / SDO_M	P12 / SDI_M	5
P04 / INT_S	P05 / SDO_S	VSS0	P02 / SCL_M	P03 / SDA_M	4
P00 / SDA_S / SDI_S	P01 / SCL_S / SCLK_S	VSS2	P15 / TXD	P16 / AOUT	3
ISO_V	RESET_N	TEST0	RX1	P10 / RXD	2
LDO1V5	LDO1V8	BAT2	RX0	G_SHUNT	1
E	D	C	B	A	

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● WQFN 32pin

TOP VIEW

Pins (top, left to right):
- 24 ISO_V
- 23 P00 /SDA_S/ SDI_S
- 22 P01 / SCL_S / SCLK_S
- 21 P04 / INT_S
- 20 P05 / SDO_S
- 19 P06 / SCS_S
- 18 P11 / AIN6
- 17 P13 / AIN7

Pins (left side, top to bottom):
- LDO1V5 25
- LDO1V8 26
- BAT2 27
- RX1 28
- RX0 29
- G_SHUNT 30
- P_ANT 31
- P10 /RXD 32

Center: **Exposed PAD**

Pins (right side, top to bottom):
- 16 VPP
- 15 VDD_IO
- 14 VSS0
- 13 MCSEL0
- 12 MCSEL1
- 11 AIN1
- 10 AIN0
- 9 P14 /SCLK_M

Pins (bottom, left to right):
- 1 TEST0
- 2 P16 / AOUT
- 3 P15 / TXD
- 4 RESET_N
- 5 P03 / SDA_M
- 6 P02 / SCL_M
- 7 P12 / SDI_M
- 8 P17 / SDO_M

Note： **The center square is the PAD on the back side of the package (exposed PAD).**
The exposed PAD should be connected to the GND of the board.

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■Pin list

Table 1   Pin list

PIN No. (WLCSP)	PIN No (WQFN)	Pin name (Function name) [*3]	1st function	2nd function	3rd function
C2	1	TEST0	Debug port	-	-
A3	2	P16/AOUT (BAT_DISCHARGE)	General purpose port	Analog monitor output	-
B3	3	P15/TXD (DEBUG)	General purpose port	UART data output	-
D2	4	RESET_N	Reset pin	-	-
A4	5	P03/SDA_M (INTERFACE)	General purpose port	I^{2}C Controller data I/O	-
B4	6	P02/SCL_M	General purpose port	I^{2}C Controller clock output	-
A5	7	P12/SDI_M (POWER)	General purpose port	SPI Controller data input	-
B5	8	P17/SDO_M (ERROR)	General purpose port	SPI Controller data output	-
A6	9	P14/SCLK_M (CHARGE)	General purpose port	SPI Controller clock output	-
-	10	AIN0	General-purpose port 0 (for AD input)	-	-
B6	11	AIN1	General-purpose port 1 (for current measurement)	-	-
-	12	MCSEL1	Capacitor selection signal (for impedance matching)	-	-
C6	13	MCSEL0	Capacitor selection signal (for impedance matching)	-	-
C4	14	VSS0	GND	-	-
D6	15	VDD_IO	Power supply for logic IO	-	-
C5	16	VPP	Power supply pin for test	-	-
E6	17	P13/AIN7 (BAT_CHG)	General purpose port	General-purpose port 7 for AD input	-
D5	18	P11/AIN6 (RFDET)	General purpose port	General-purpose port 6 for AD input	-
E5	19	P06/SCS_S (SCS_S)	General purpose port	SPI Peripheral chip select input	-
D4	20	P05/SDO_S (SDO_S)	General purpose port	SPI Peripheral data output	-
E4	21	P04/INT_S (INT_S)	General purpose port	Host IF INT output	-
D3	22	P01/SCL_S/SCLK_S (SCL_S / SCLK_S)	General purpose port	I^{2}C Target clock input	SPI Peripheral clock input
E3	23	P00/SDA_S/SDI_S (SDA_S / SDI_S)	General purpose port	I^{2}C Target data I/O	SPI Peripheral data input
E2	24	ISO_V	Power supply for logic IO (for Host IF)	-	-
E1	25	LDO1V5	Internal power supply	-	-

[*3] Function name assigned by firmware.

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PIN No. (WLCSP)	PIN No (WQFN)	Pin name (Function name) [*3]	1st function	2nd function	3rd function
			(1.5V)		
D1	26	LDO1V8	Internal power supply (1.8V)	-	-
C1	27	BAT2	Battery voltage monitor pin	-	-
B2	28	RX1	RF data receiving pin	-	-
B1	29	RX0	RF data receiving pin	-	-
A1	30	G_SHUNT	Shunt transistor control signal	-	-
-	31	P_ANT[*4]	Rectifier input voltage	-	-
A2	32	P10/RXD (BAT_SW)	General purpose port	UART data input	-
C3	-	VSS2	GND	-	-

[*4] If the package is WLCSP, connect to VDD_IO power supply.

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■Pin Description

Notation Definition: Pin state in reset

Index	Notation	Description
In reset	L	"L" level output
	H	"H" level output
	PU	Pull-Up
	PD	Pull-Down
	Z	Floating state

Notation Definition: input/output direction

Index	Notation	Description
I/O	I	Input pin
	O	Output pin
	I/O	Bi-directional pin

●Power, GND, and reference voltage pins

PIN No. (WLCSP)	PIN NO. (WQFN)	Pin name	I/O	Pin description
C4	14	VSS0	-	GND
D6	15	VDD_IO	-	Power supply (for Logic IO)
C5	16	VPP	I	Power supply (for Test)
E2	24	ISO_V	-	Power supply (for Host IF)
E1	25	LDO1V5	-	Power supply for internal use (1.5V)
D1	26	LDO1V8	-	Power supply for internal use (1.8V)
C1	27	BAT2	I	Battery voltage monitor pin
-	31	P_ANT	-	Rectifier input voltage
C3	-	VSS2	-	GND

●Analog signal pin

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	I/O	Pin description
B2	28	RX1	I	Pins Connected to LSI internal circuits that demodulate communications.
B1	29	RX0	I	

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●General purpose port terminal (VDD_IO system)

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	In reset	I/O	Active Level	Pin description
C2	1	TEST0	Z	I/O	L	Debug port
A3	2	P16 / AOUT	Z	I/O	-	General purpose port Analog monitor output
B3	3	P15 / TXD	Z	I/O	-	General purpose port UART data output
D2	4	RESET_N	PU	I	L	Reset Input Pin L：System reset mode H：Program operation mode
-	10	AIN0	Z	I	-	General-purpose port 0 (for AD input)
B6	11	AIN1	Z	I	-	General-purpose port 1 (for current measurement)
-	12	MCSEL1	PU	O	-	Capacitor selection signal (for impedance matching)
C6	13	MCSEL0	PU	O	-	Capacitor selection signal (for impedance matching)
E6	17	P13 / AIN7	Z	I/O	-	General purpose port General-purpose port 7 (for AD input)
A2	32	P10 / RXD	PU	I/O	-	General purpose port UART data input

●General purpose port terminal (ISO_V system) [*5]

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	In reset	I/O	Pin description
A4	5	P03 / SDA_M	Z	I/O	General purpose port I^{2}C Controller data I/O
B4	6	P02 / SCL_M	Z	I/O	General purpose port I^{2}C Controller Clock output
A5	7	P12 / SDI_M	Z	I/O	General purpose port SPI Controller Data input
B5	8	P17 / SDO_M	Z	I/O	General purpose port SPI Controller Data output
A6	9	P14 / SCLK_M	Z	I/O	General purpose port SPI Controller Clock output
D5	18	P11 / AIN6	Z	I/O	General purpose port General-purpose port 6 (for AD input)
E5	19	P06 / SCS_S	Z	I/O	General purpose port SPI Peripheral Chip Select input
D4	20	P05 / SDO_S	Z	I/O	General purpose port SPI Peripheral Data output
E4	21	P04 / INT_S	Z	I/O	General purpose port Host IF INT output
D3	22	P01 / SCL_S / SCLK_S	Z	I/O	General purpose port I^{2}C Target Clock input SPI Peripheral Clock input
E3	23	P00 / SDA_S / SDI_S	Z	I/O	General purpose port I^{2}C Target Data I/O SPI Peripheral Data input

[*5] When controlled by an MCU or other device, the voltage should be the same as the interface voltage of the MCU.

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●General-purpose port pins (P_ANT system)

PIN No. (WLCSP)	PIN No. (WQFN)	Pin name	In reset	I/O	Pin description
A1	30	G_SHUNT	L	O	Shunt transistor control signal

■Unused pin processing

Pin name	Pin processing
TEST0	Pull-Up
P00~P6、P10~P17 RESET_N AIN0 AIN1 MCSEL0 MCSEL1 G_SHUNT	Open

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■Electrical Characteristics

●Absolute Maximum Ratings

Index		Symbol	Condition	Rated value	Unit
Supply voltage	Power supply for logic IO	VDD_IO	-	-0.3～+6.5	V
	Power supply for logic IO (for Host IF)	ISO_V	-	-0.3～+6.5	V
	Rectifier input voltage	P_ANT	-	-0.3～+6.5	V
	Battery voltage monitor	BAT2	-	-0.3～+6.5	V
	Internal power supply	LDO1V5	-	-0.3～+2.0	V
		LDO1V8	-	-0.3～+6.5	V
Input voltage		VDIN	-	-0.3～VDD_IO+0.3	V
		$VDIN_{DIFF}$	RX0-RX1 (differential)	14	V
Input current		Ii	-	-10～+10	mA
		I_{P_ANT}	-	100	mA
Output voltage		VDO	-	-0.3～VDD_IO+0.3	V
Digital output current		IDO	-	-12～+20	mA
Power dissipation(WQFN)		PD	-	1	W
Power dissipation (CSP)		PD	-	0.5	W
Storage temperature		Tstg	-	-55～+150	°C

●Recommended Operating Conditions

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage range	VDD_IO	-	1.8	-	5.5	V
	ISO_V	-	1.8	-	5.5	V
	P_ANT	During communication	2.0	5.0	5.5	V
	P_ANT	During power transmission	-	-	5.5	V
Operating temperature	Ta	-	-40	+25	+85	°C
Antenna input frequency	F_{ANT}	-	Typ. -0.05%	13.56	Typ. +0.05%	MHz

●Flash Memory Operating Conditions

(VDD_IO=2.7 to 5.5V, P_ANT=2.7 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Range	Unit
Rewrite count	C_{EPD}	Data Flash	10,000	times

●RF Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage level	V_{RX1}	RX0/RX1	2.0	-	5.9	V
Input data amplitude	V_{RX2}	RX0/RX1	50	-	-	mV
Communication speed	F_{RX}	RX0/RX1	-	212	-	kbps
			-	424	-	kbps

●Notification Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
P_ANT limiter	V_{PANT1}	Normal	-	-	5.5	V
	V_{PANT2}	In case of abnormality notice	-	3.0	-	V

●AD Characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	AD_{res}	-	-	10	-	bit
Zero-Scale Error	ZSE	-	-6	-	+6	LSB
Full-Scale Error	FSE	-	-6	-	+6	LSB

● AC Characteristics (I²C Bus Interface)

● Standard Mode 100 kHz

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S	Clock frequency	f_{SCL}	-	-	-	100	kHz
	Hold time (start/repeated start condition)	$t_{HD:STA}$	-	4.0	-	-	µs
	"L" level time	t_{LOW}	-	4.7	-	-	µs
	"H" level time	t_{HIGH}	-	4.0	-	-	µs
	Setup time (start/repeated start condition)	$t_{SU:STA}$	-	4.7	-	-	µs
SDA_S	Hold time	$t_{HD:DAT}$	-	0	-	-	µs
	Setup time	$t_{SU:DAT}$	-	0.25	-	-	µs
	Setup time (Stop condition)	$t_{SU:STO}$	-	4.0	-	-	µs
Bus free time		t_{BUF}	-	4.7	-	-	µs

● Fast Mode 400 kHz

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

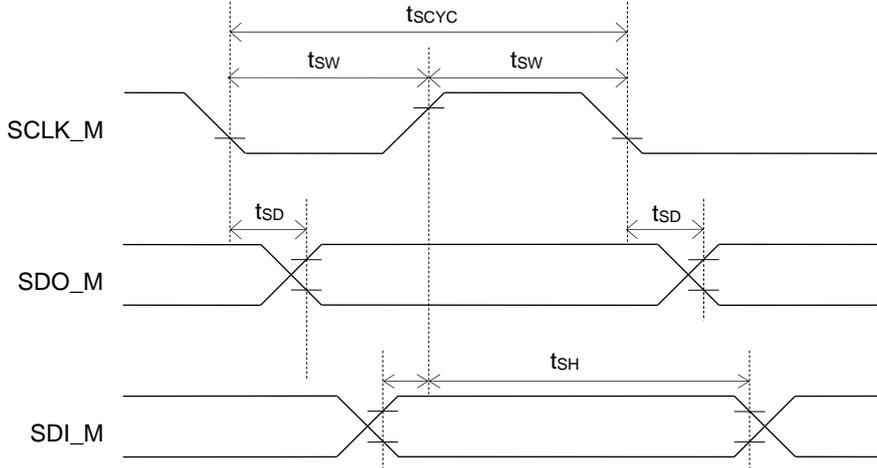| Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S	Clock frequency	f_{SCL}	-	-	-	400	kHz
	Hold time (start/repeated start condition)	$t_{HD:STA}$	-	0.6	-	-	µs
	"L" level time	t_{LOW}	-	1.3	-	-	µs
	"H" level time	t_{HIGH}	-	0.6	-	-	µs
	Setup time (repeated start condition)	$t_{SU:STA}$	-	0.6	-	-	µs
SDA_S	Hold time	$t_{HD:DAT}$	-	0	-	-	µs
	Setup time	$t_{SU:DAT}$	-	0.1	-	-	µs
	Setup time (Stop condition)	$t_{SU:STO}$	-	0.6	-	-	µs
Bus free time		t_{BUF}	-	1.3	-	-	µs
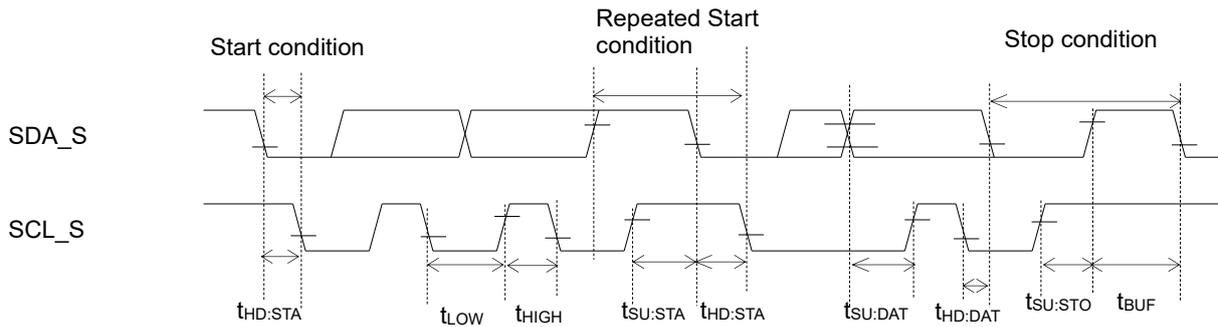
Note : If powering off this LSI, it disables communications of other devices on the I²C bus
When power is not received from the P_ANT pin and there is a power input to the ISO_V pin of this LSI,
the SDA_S/SCL_S pins maintain the Hi-Z state.

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●AC Characteristics (Host Interface：SPI Controller)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_M	Output cycle	t_{SCYC}	-	250	SCLK[*6]	-	ns
	Output pulse width	t_{SW}	-	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	ns
SDO_M	Output delay time	t_{SD}	-	-	-	100	ns
SDI_M	Input setup time	t_{SS}	-	100	-	-	ns
	Input hold time	t_{SH}	-	60	-	-	ns

●AC Characteristics (Host Interface：SPI Peripheral)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

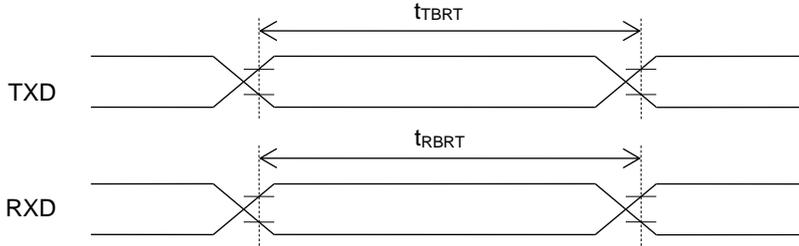| Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S	Input cycle	t_{SCYC}	-	500	-	-	ns
	Input pulse width	t_{SW}	-	200	-	-	ns
SCS_S[*7]	Setup time	t_{CS1}	-	80	-	-	ns
		t_{CS2}	-	80	-	-	ns
	Hold time	t_{CH1}	-	80	-	-	ns
		t_{CH2}	-	80	-	-	ns
	Input pulse width	t_{CW}	-	80	-	-	ns
SDO_S	Output delay time	t_{SD}	-	-	-	240	ns
SDI_S	Input setup time	t_{SS}	-	80	-	-	ns
	Input hold time	t_{SH}	-	80	-	-	ns
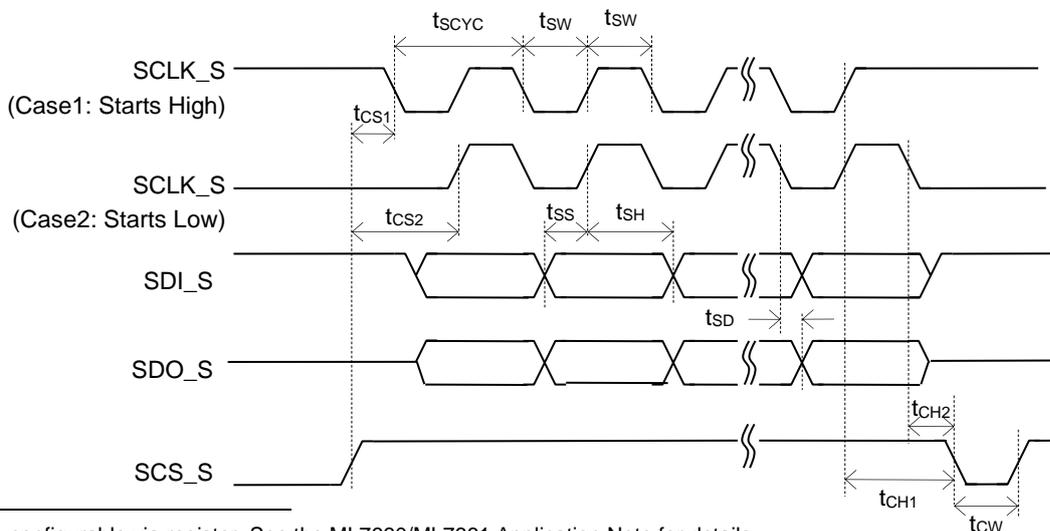
[*6] SCLK is configurable via register. See the ML7660/ML7661 Application Note for details.
[*7] SCS_S polarity (active-high or active-low) is switchable.
   See the ML7660/ML7661 Application Note for details.

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●AC Characteristics (UART)

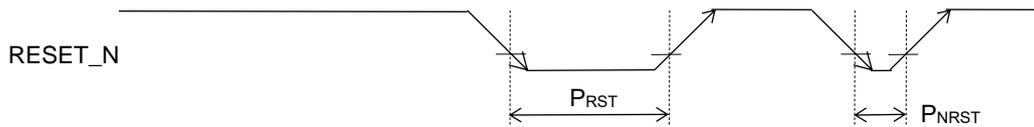(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Tx Baud Rate	t_{TBRT}	-	-	-	115.2	kbps
Rx Baud Rate	t_{RBRT}	-	-	-	115.2	kbps

TXD

RXD

●AC Characteristics (Reset)

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Pulse Width	P_{RST}	-	2	-	-	ms
Non-reset Pulse Width	P_{NRST}	-	-	-	0.3	µs

RESET_N

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●IO Characteristics

(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.[*8]	Max.	Unit
Output voltage 1	VOH1	IOH=-1.0mA	VDD_IO -0.5	-	-	V
	VOL1	IOL=+0.5mA	-	-	0.4	V
Output voltage 2 (LED mode selected)	VOL2	$2.7V \leqq V_{DD} \leqq 5.5V$ IOL=+5.0mA	-	-	0.6	V
		IOL=+2.0mA	-	-	0.4	V
Output voltage 3 (I²C mode selected)	VOL3	IOL3= +3mA (I²C spec.) (VDD_IO ≥2V、ISO_V≥2V)	-	-	0.4	V
Output voltage 4 (I²C mode selected)	VOL4	IOL4= +2mA (I²C spec.) (VDD_IO <2V、ISO_V<2V)	-	-	VDD_IO ×0.2	V
Output leakage1	IOOH1	VOH=V_{DD} (at high impedance)	-	-	1	µA
	IOOL1	VOL=VSS (at high impedance)	-1	-	-	µA
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	-	-	1	µA
	IIL1	VIL1=VSS	-900	-300	-20	µA
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	-	-	1	µA
	IIL2	VIL2=VSS	-200	-15	-1	µA
Input current 3	IIH3	VIH3=V_{DD} (when pull-down)	1	15	200	µA
	IIL3	VIL3=VSS (when pull-up)	-200	-15	-1	µA
	IIH3Z	VIH3=V_{DD} (at high impedance)	-	-	1	µA
	IIL3Z	VIL3=VSS (at high impedance)	-1	-	-	µA
Input voltage 1	VIH1	-	0.75× VDD_IO	-	VDD_IO	V
	VIL1	-	0	-	0.3× VDD_IO	V
Input pin capacitance	CIN	f=10kHz Vrms=50mV Ta=25°C	-	10	-	pF
Leak current	I_ISOV	Voltage supply to the ISO_V pin, no magnetic field input	-	100	-	nA

●Current Consumption

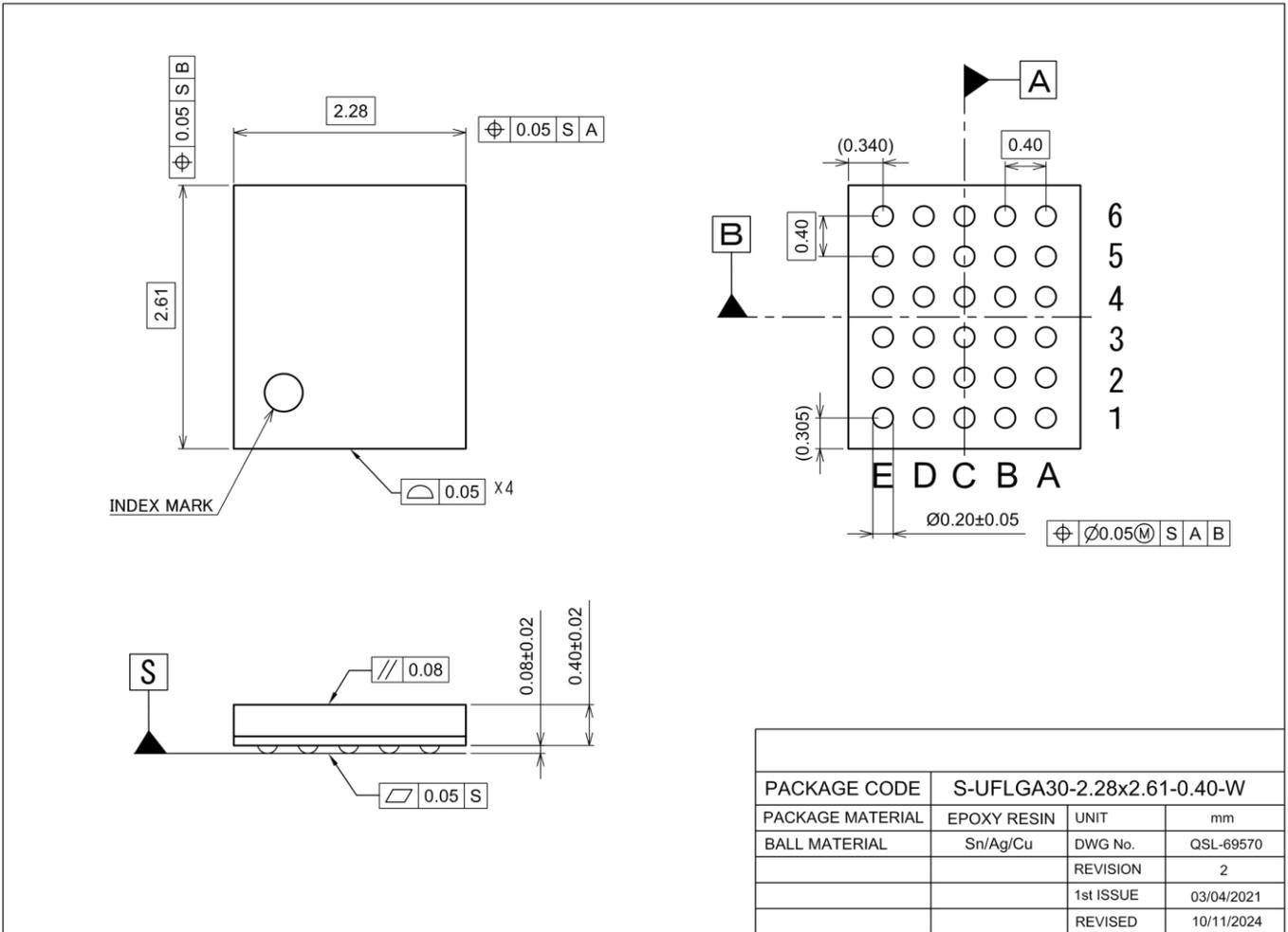(VDD_IO=1.8 to 5.5V, P_ANT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption[9]	P_ANT	During communication	0.5	-	-	mA
	P_ANT	During power transmission	-	-	10	mA

[*8] Typical values are listed for Ta=25°C and VDD_IO=3.0V.
[*9] Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External transistor current is not included.

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■Package Dimensions

WLCSP30pin

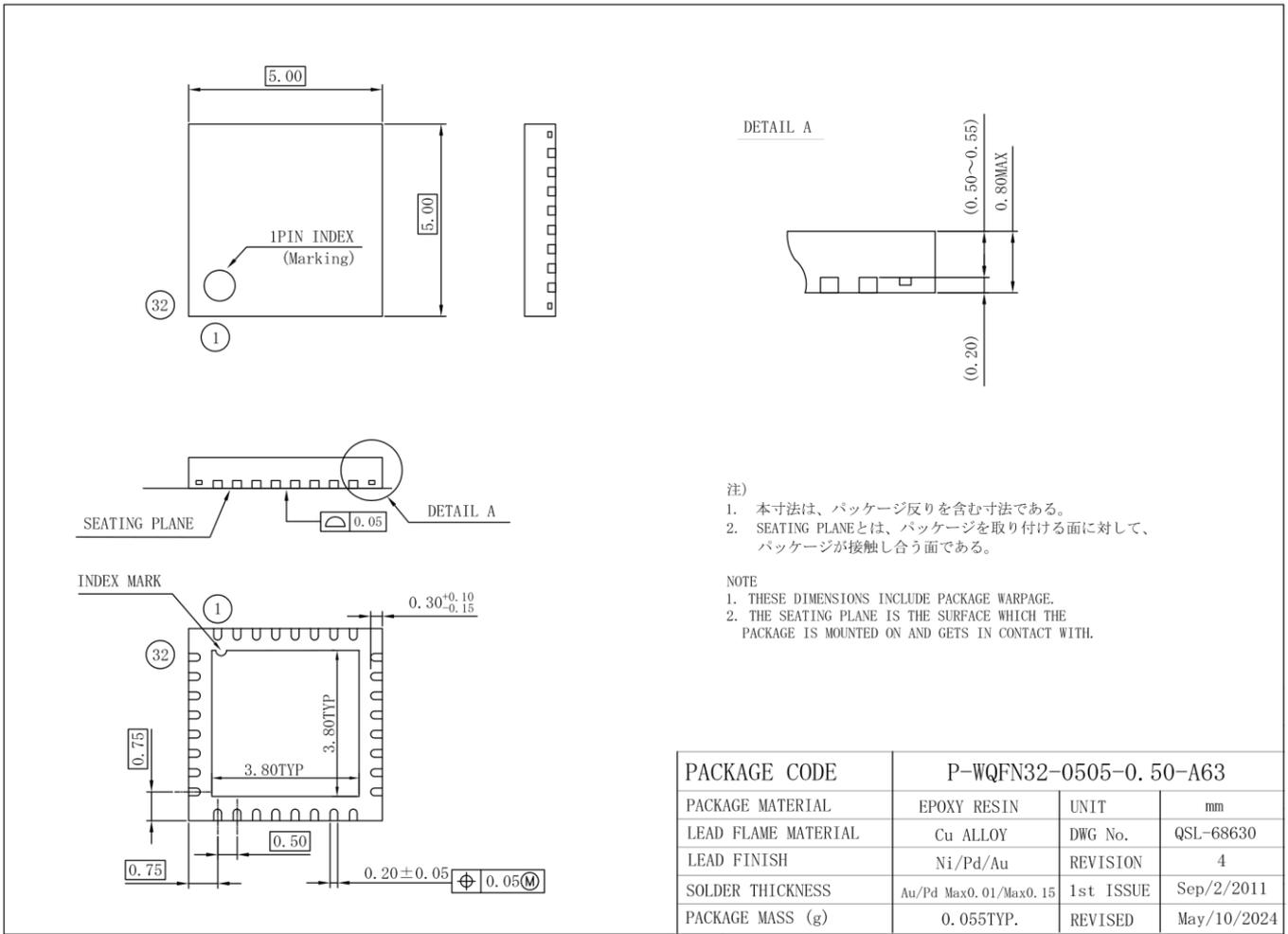| PACKAGE CODE	S-UFLGA30-2.28x2.61-0.40-W		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
BALL MATERIAL	Sn/Ag/Cu	DWG No.	QSL-69570
		REVISION	2
		1st ISSUE	03/04/2021
		REVISED	10/11/2024

Notes for Mounting the Surface Mount Type Package
> The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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WQFN32pin

PACKAGE CODE	P-WQFN32-0505-0.50-A63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68630
LEAD FINISH	Ni/Pd/Au	REVISION	4
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Sep/2/2011
PACKAGE MASS (g)	0.055TYP.	REVISED	May/10/2024

注)
1. 本寸法は、パッケージ反りを含む寸法である。
2. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTE
1. THESE DIMENSIONS INCLUDE PACKAGE WARPAGE.
2. THE SEATING PLANE IS THE SURFACE WHICH THE
PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

Notes for Mounting the Surface Mount Type Package
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin
number, package code and desired mounting conditions (reflow method, temperature and times).

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■Application Circuit Example

Please refer to the ML7662 / ML7663 Application Note for details.

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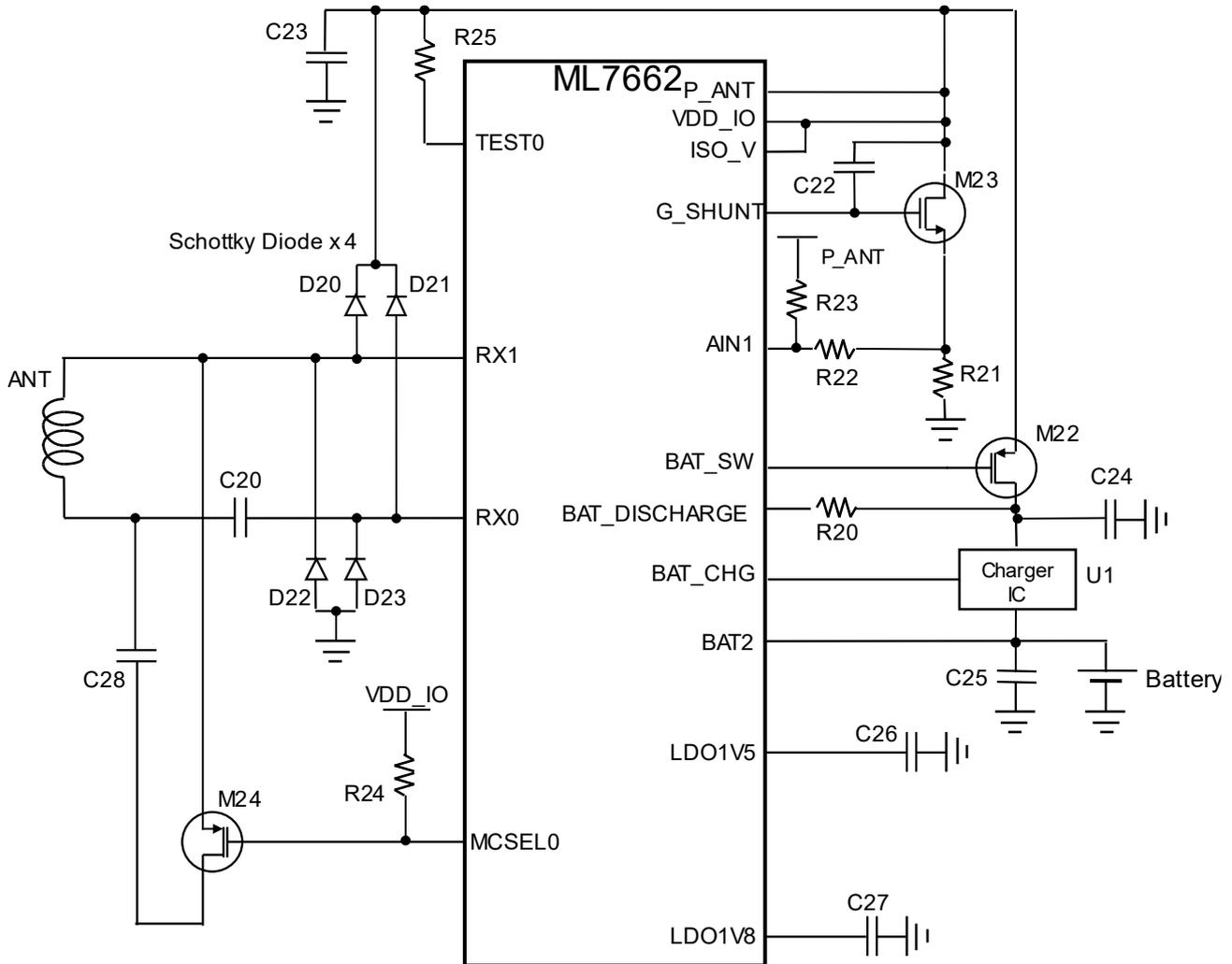
■Revision History

| Document No. | Issue Date | Page | | Change Contents |
		Previous Edition	Current Edition	
FEDL7662-01	2024.6.9	-	-	First edition
FEDL7662-02	2023.12.12	-	1	Add product name and appications description
FEDL7662-03	2024.1.9	16	16	Modified Notes
FEDL7662-04	2025.12.30	16	16	Revise the contents of the notice
FEDL7662-05	2026.1.30	all	all	Revise the datasheet layout Added: AC Characteristics (UART) Added: AC Characteristics (Reset)
		17	17	Delet: Note for the package with exposed die pad

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