FEDL7663-05
Issue Date：January 30, 2026

ML7663

13.56MHz Wireless charging transmitter LSI

■Overview

ML7663 is a 13.56MHz wireless power transmitter LSI.
ML7663 realizes a wireless power transfer system by combining with the wireless power receiver LSI ML7662, and can output power for ML7662 to supply 1W to charging device.
ML7663 has a communication command generation function based on NFC Forum Type F technology for communicating with ML7662, a function for variably controlling the transmission amount to optimize the transmission power, and a function to detect abnormalities when ML7662 is attached/detached or power is transmitted. All of these functions are included in the 40-pin WQFN package (6.0 mm square), and ML7663 is ideal for wireless power transfer of small devices.
In addition, the operating voltage is 5V, and it can be driven from a USB power source such as a mobile battery.
Furthermore, ML7663 is equipped with a host interface (SPI / I^2C Target) function, and it is possible to update configuration data from an external MCU.

■Features

- Charging control
  - Built-in 13.56MHz power transmission control circuit
    power transmission transistor control output
  - Abnormally detection function by software and hardware control

- Communication control
  - Equipped with a command generation function for communication with ML7662
  - Communication speed: 212kbps, 424kbps
  - 2Kbyte data flash for storing user data

- Host interface
  - 1ch Serial interface (Target), and selectable from SPI or I^2C

- Package
  - WQFN40pin (P-WQFN40-0606-0.50-63)

- Applications
  - NFC charging devices, e.g.
  - smart wathes, fitness trackers and smart wristbands
  - smart rings
  - smart glasses
  - true wireless stereos and hearing aids
  - stylus pens, wireless mouses and wireless keyboads
  - electric toothbrushes
  - beauty home appliances
  - personal health care devices
  - battery packs

●Product Name

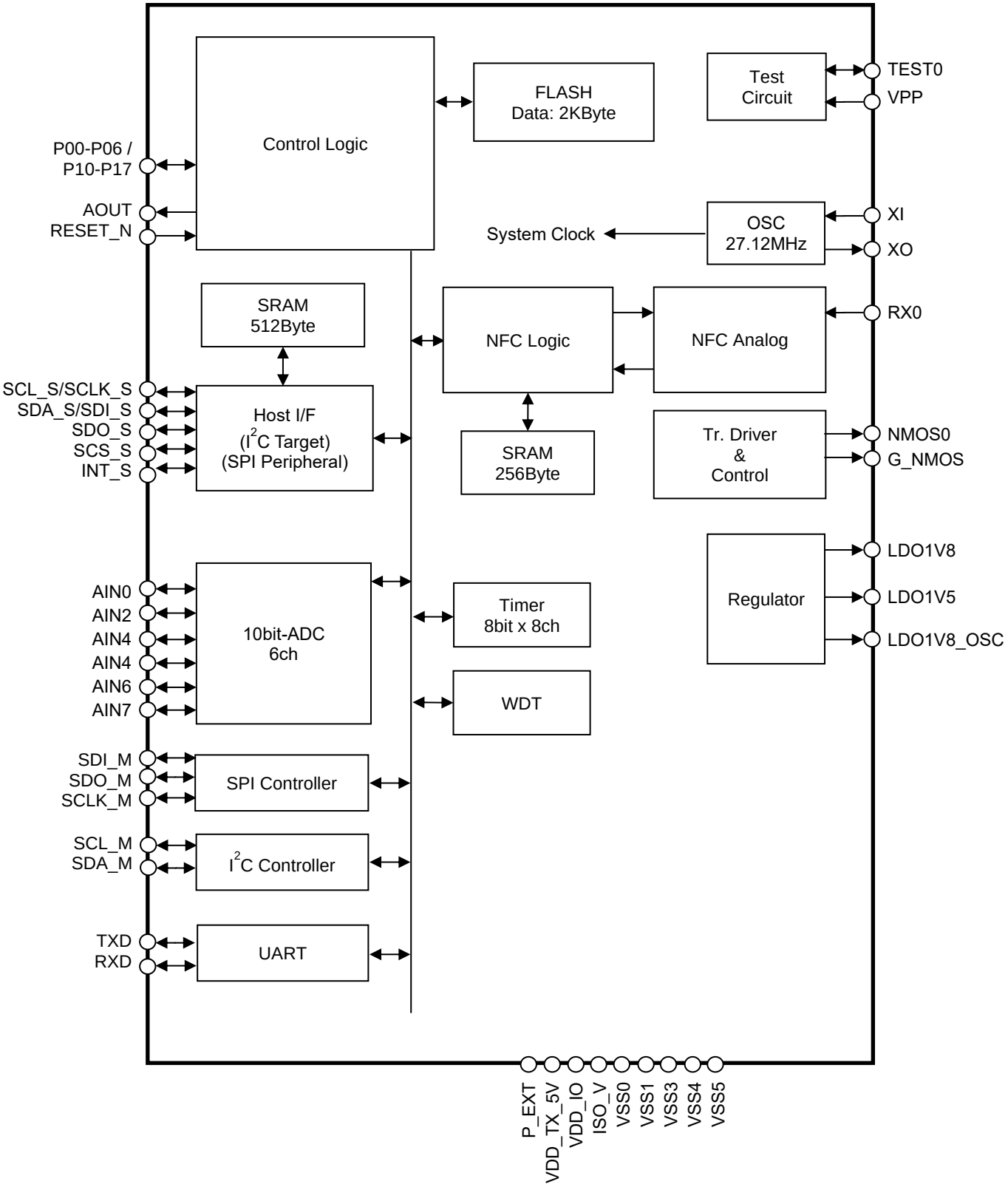
ML7663-J01GD (WQFN Package)

■Related Documents

In addition to this document, the following documents should also be read together as necessary.

・ML7662 Data Sheet
・ML7662 / ML7663 Application Note

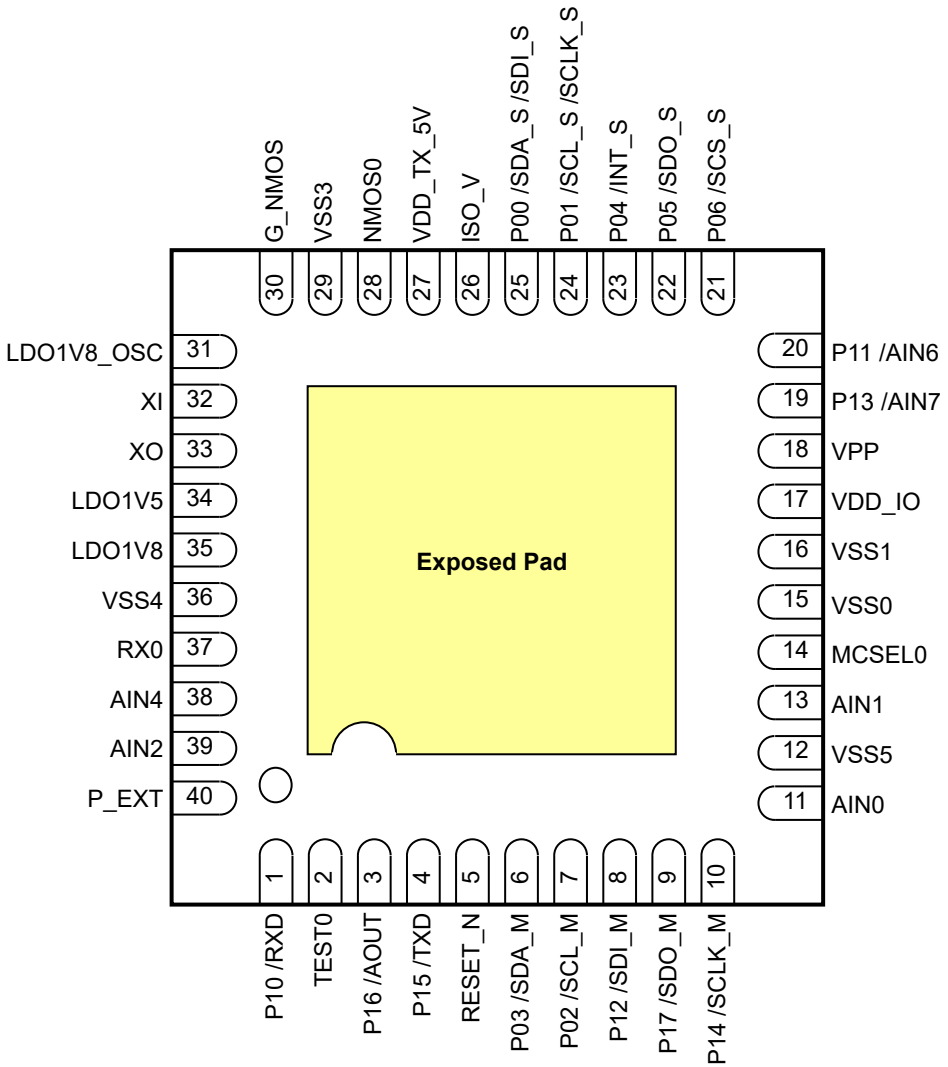
■Block Diagram



■Pin Assignment

WQFN 40pin

TOP VIEW



note: The center square is the PAD on the back side of the package (exposed PAD).
The exposed PAD should be connected to the GND of the board.

■Pin list

PIN No.	Pin name (Function name)[1]	1st function	2nd function	3rd function
1	P10/RXD (I^2C ADDRESS)	General purpose port	UART data input	-
2	TEST0	Debug port	-	-
3	P16/AOUT (SHUTDOWN)	General purpose port	Analog monitor output	-
4	P15/TXD	General purpose port	UART data output	-
5	RESET_N	Reset pin	Debug port	-
6	P03/SDA_M (WAKEUP)	General purpose port	I^2C Controller data I/O	-
7	P02/SCL_M	General purpose port	I^2C Controller clock output	-
8	P12/SDI_M (POWER)	General purpose port	SPI Controller data input	-
9	P17/SDO_M (ERROR)	General purpose port	SPI Controller data output	-
10	P14/SCLK_M (CHARGE)	General purpose port	SPI Controller clock output	-
11	AIN0	General-purpose port 0 (for AD input)	-	-
12	VSS5	GND	-	-
13	AIN1	General-purpose port 1 (for current measurement)	-	-
14	MCSEL0	Capacitor selection signal (for impedance matching)	-	-
15	VSS0	GND	-	-
16	VSS1	GND	-	-
17	VDD_IO	Power supply (for logic IO)	-	-
18	VPP	Test pin	-	-
19	P13/AIN7	General purpose port	General-purpose port 7 for AD input	-
20	P11/AIN6 (INTERFACE)	General purpose port	General-purpose port 6 for AD input	-
21	P06/SCS_S (SCS_S)	General purpose port	SPI Peripheral chip select input	-
22	P05/SDO_S (SDO_S)	General purpose port	SPI Peripheral data output	-
23	P04/INT_S (INT_S)	General purpose port	Host IF INT output	-
24	P01/SCL_S/SCLK_S (SCL_S / SCLK_S)	General purpose port	I^2C Target clock input	SPI Peripheral clock input
25	P00/SDA_S/SDI_S (SDA_S / SDI_S)	General purpose port	I^2C Target data I/O	SPI Peripheral data input
26	ISO_V	Power supply for logic IO (for Host IF) [*2]	-	-
27	VDD_TX_5V	Power source for driving	-	-

[*1] Function name assigned by firmware.
[*2] ISO_V should be connected to VDD_IO on the board.

PIN No.	Pin name (Function name)[1]	1st function	2nd function	3rd function
28	NMOS0	Nch transistor driver (for power feed)	-	-
29	VSS3	GND	-	-
30	G_NMOS	Nch transistor bias output (for power feed)	-	-
31	LDO1V8_OSC	1.8V power supply output for 27.12MHz oscillator circuit	-	-
32	XI	27.12MHz oscillation terminal	-	-
33	XO	27.12MHz oscillation terminal	-	-
34	LDO1V5	Internal power supply (1.5V)	-	-
35	LDO1V8	Internal power supply (1.8V)	-	-
36	VSS4	GND	-	-
37	RX0	RF data receiving terminal	-	-
38	AIN4	General-purpose input port 4 for high frequency current measurement	-	-
39	AIN2	General-purpose input port 2 for measuring transmission current	-	-
40	P_EXT	External power supply (5V)	-	-

■Pin Description

Notation Definition: Pin state in reset

Index	Notation	Description
In reset	L	“L” level output
	H	“H” level output
	PU	Pull-Up
	PD	Pull-Down
	Z	Floating state

Notation Definition: input/output direction

index	Notation	Description
I/O	I	Input pin
	O	Output pin
	I/O	Bi-directional pin

●Power, GND, and reference voltage pins

PIN No.	Pin name	I/O	Pin description
12	VSS5	-	GND
15	VSS0	-	GND
16	VSS1	-	GND
17	VDD_IO	-	Power supply (for Logic IO)
18	VPP	I	Power supply (for Test)
26	ISO_V	-	Power supply (for Host Interface control)
27	VDD_TX_5V	-	Power supply (for magnetic field generation transistor)
29	VSS3	-	GND
31	LDO1V8_OSC	-	Power supply for crystal oscillator (1.8V)
34	LDO1V5	-	Power supply for internal use (1.5V)
35	LDO1V8	-	Power supply for internal use (1.8V)
36	VSS4	-	GND
40	P_EXT	-	Power supply (5V)

●Analog signal pin

PIN No.	Pin name	In reset	I/O	Pin description
28	NMOS0	Z	O	Pin that generates a 13.56 MHz sine wave to generate a magnetic field in a later stage Nch MOSFET.
30	G_NMOS	PD	O	Pin for adjusting the gain of the Nch MOSFET in the subsequent stage. G_NMOS makes modulation degree changeable.
37	RX0	-	I	Pins Connected to LSI internal circuits that demodulate communications.

●Clock pin

PIN No.	Pin name	I/O	Pin description
32	XI	I	Pins to generate clock by connecting to 27.12MHz crystal oscillator
33	XO	O	

●General purpose port pin (P_EXT system)

PIN No.	Pin name	in reset	I/O	Pin Description
38	AIN4	Z	I	Pins connected to the internal circuitry of the LSI that demodulates the notification.*3
39	AIN2	Z	I	Pins that can measure the current flowing through the antenna with AD.

●General purpose port terminal (ISO_V system) *4

PIN No.	Pin name	in reset	I/O	Pin Description
6	P03/SDA_M	Z	I/O	General purpose port I^2C Controller data I/O
7	P02/SCL_M	Z	I/O	General purpose port I^2C Controller Clock output
8	P12/SDI_M	Z	I/O	General purpose port SPI Controller Data input
9	P17/SDO_M	Z	I/O	General purpose port SPI Controller Data output
10	P14/SCLK_M	Z	I/O	General purpose port SPI Controller Clock output
20	P11/AIN6	Z	I/O	General purpose port General-purpose port 6 (for AD input)
21	P06/SCS_S	Z	I/O	General purpose port SPI Peripheral Chip Select input
22	P05/SDO_S	Z	I/O	General purpose port SPI Peripheral Data output
23	P04/INT_S	Z	I/O	General purpose port Host IF INT output
24	P01/SCL_S/SCLK_S	Z	I/O	General purpose port I^2C Target Clock input SPI Peripheral Clock input
25	P00/SDA_S/SDI_S	Z	I/O	General purpose port I^2C Target Data I/O SPI Peripheral Data input

*3 A communication that originates from the power receiver as defined in the NFC standard.
*4 When controlled by an MCU or other device, the voltage should be the same as the interface voltage of the MCU.

●General-purpose port pins (VDD_IO system)

PIN No.	Pin name	In reset	I/O	Active Level	Pin Description
1	P10/RXD	PU	I/O	-	General purpose port UART data input
2	TEST0	Z	I/O	L	Debug port
3	P16/AOUT	Z	I/O	-	General purpose port Analog Monitor Outputs
4	P15/TXD	Z	I/O	-	General purpose port UART data output
5	RESET_N	PU	I	L	Reset Input Pin L：System reset mode H：Program operation mode
11	AIN0	Z	I	-	General-purpose port 0 (for AD input)
13	AIN1	Z	I	-	General-purpose port 1 (for AD input)
14	MCSEL0	PU	O	-	Selection signal for impedance matching capacitor
19	P13/AIN7	Z	I/O	-	General purpose port General-purpose port 7 (for AD input)

■Unused pin processing

Pin name	Pin processing
TEST0	Pull-Up
P00~P06, P10~P17 RESET_N AIN0 AIN1 MCSEL0 AIN4 AIN2	Open

■Electrical Characteristics

●Absolute Maximum Ratings

Index		Symbol	Rated value	Unit
Supply voltage	Power supply for logic IO	VDD_IO	-0.3～+6.5	V
	Power supply for logic IO (for Host IF)	ISO_V		
	Regulator input voltage	P_EXT	-0.3～+6.5	V
	Power supply voltage for power transmission	VDD_TX_5V	-0.3～+6.5	V
	Internal power supply / Crystal oscillation voltage	LDO1V5	-0.3～+2.0	V
	Internal power supply	LDO1V8	-0.3～+6.5	V
	27.12MHz oscillator	LSO1V8_OSC	-0.3～+6.5	V
Input voltage		V_{DIN_IO}	-0.3～VDD_IO+0.3	V
		V_{DINmax}	-0.3～+6.5	V
Input current		Ii	-10～+10	mA
Output voltage		V_{DO}	-0.3～VDD_IO+0.3	V
Digital output current		I_{DO}	-12～+20	mA
Allowable Loss		PD	1	W
Storage Temperature		T_{stg}	-55～+150	℃

●Recommended Operating Conditions

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage range	VDD_IO	-	1.8	-	5.5	V
	ISO_V	Connect with VDD_IO on the board	1.8	-	5.5	V
	P_EXT	-	4.5	5.0	5.5	V
	VDD_TX_5V	-	4.5	5.0	5.5	V
Operating temperature	Ta	-	-40	+25	+85	℃
Crystal oscillator frequency	f_{XTL}	-	Typ. -0.05%	27.12	Typ. +0.05%	MHz

●Flash Memory Operating Conditions

(VDD_IO=2.7 to 5.5V, P_EXT=2.7 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index	Symbol	Condition	Range	Unit
Rewrite count	C_{EPD}	Data Flash	10,000	times

●Power Transmission Characteristics

(VDD_IO=1.8 to 5.5V, VDD_TX_5V=4.5 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
nmos0 output frequency	F_{TX}	-	-	13.56	-	MHz

●AC Characteristics (I^2C Bus Interface)

- Standard Mode 100 kHz

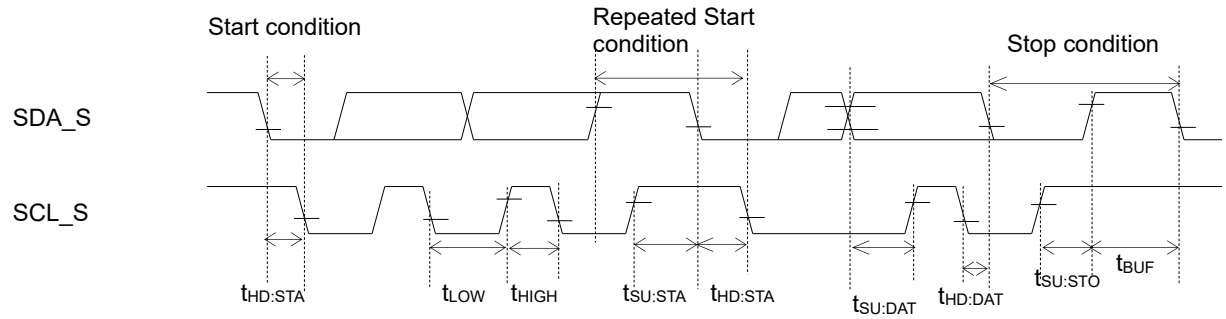
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S	Clock frequency	f_{SCL}	-	-	-	100	kHz
	Hold time (start/repeated start condition)	$t_{HD:STA}$	-	4.0	-	-	μs
	"L" level time	t_{LOW}	-	4.7	-	-	μs
	"H" level time	t_{HIGH}	-	4.0	-	-	μs
	Setup time (repeated start condition)	$t_{SU:STA}$	-	4.7	-	-	μs
SDA_S	Hold time	$t_{HD:DAT}$	-	0	-	-	μs
	Setup time	$t_{SU:DAT}$	-	0.25	-	-	μs
	Setup time (Stop condition)	$t_{SU:STO}$	-	4.0	-	-	μs
Bus free time		t_{BUF}	-	4.7	-	-	μs

- Fast Mode 400 kHz

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Index		symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S	Clock frequency	f_{SCL}	-	-	-	400	kHz
	Hold time (start/repeated start condition)	$t_{HD:STA}$	-	0.6	-	-	μs
	"L" level time	t_{LOW}	-	1.3	-	-	μs
	"H" level time	t_{HIGH}	-	0.6	-	-	μs
	Setup time (repeated start condition)	$t_{SU:STA}$	-	0.6	-	-	μs
SDA_S	Hold time	$t_{HD:DAT}$	-	0	-	-	μs
	Setup time	$t_{SU:DAT}$	-	0.1	-	-	μs
	Setup time (Stop condition)	$t_{SU:STO}$	-	0.6	-	-	μs
Bus free time		t_{BUF}	-	1.3	-	-	μs

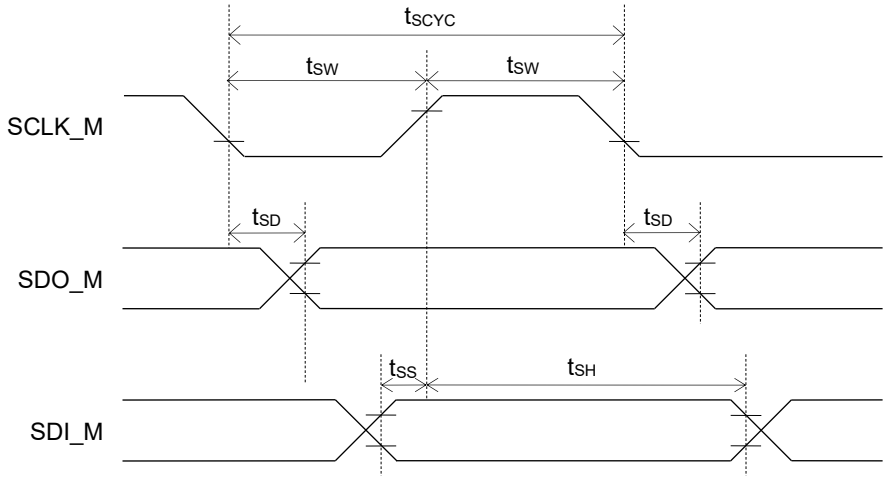


Note：If powering off this LSI, it disables communications of other devices on the I^2C bus

●AC Characteristics (Host Interface：SPI Controller)

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_M	Output cycle	t_{SCYC}	-	250	SCLK[*5]	-	ns
	Output pulse width	t_{SW}	-	tSCYC ×0.4	tSCYC ×0.5	tSCYC ×0.6	ns
SDO_M	Output delay time	t_{SD}	-	-	-	100	ns
SDI_M	Input setup time	t_{SS}	-	100	-	-	ns
	Input hold time	t_{SH}	-	60	-	-	ns

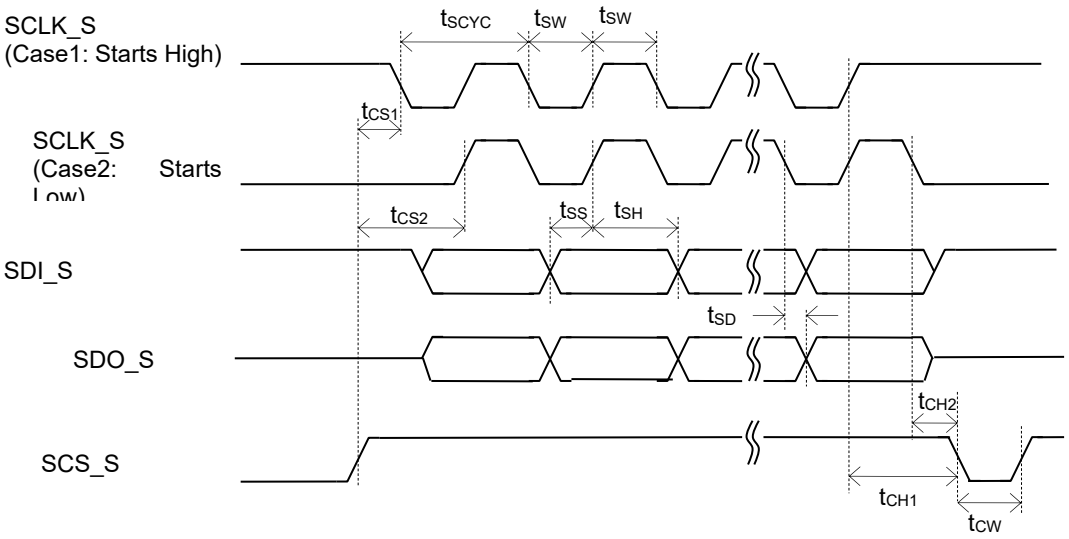


[*5] SCLK is configurable via register. See the ML7662/ML7663 Application Note for details.

●AC Characteristics (Host Interface：SPI Peripheral)

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index		Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S	Input cycle	t_{SCYC}	-	500	-	-	ns
	Input pulse width	t_{SW}	-	200	-	-	ns
SCS_S*6	Setup time	t_{CS1}	-	80	-	-	ns
		t_{CS2}	-	80	-	-	ns
	Hold time	t_{CH1}	-	80	-	-	ns
		t_{CH2}	-	80	-	-	ns
	Input pulse width	t_{CW}	-	80	-	-	ns
SDO_S	Output delay time	t_{SD}	-	-	-	240	ns
SDI_S	Input setup time	t_{SS}	-	80	-	-	ns
	Input hold time	t_{SH}	-	80	-	-	ns

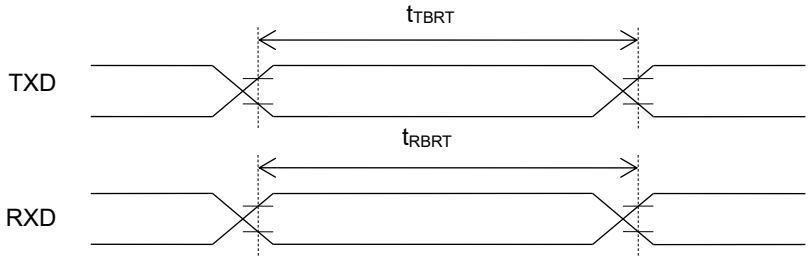


*6 SCS_S polarity (active-high or active-low) is switchable.
See the ML7662/ML7663 Application Note for details.

●AC Characteristics (UART)

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

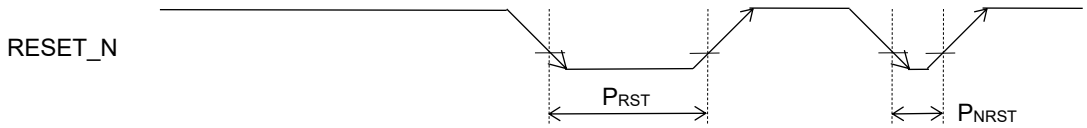
Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Tx Baud Rate	t_{TBRT}	-	-	-	115.2	kbps
Rx Baud Rate	t_{RBRT}	-	-	-	115.2	kbps



●AC Characteristics (Reset)

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset Pulse Width	P_{RST}	-	2	-	-	ms
Non-reset Pulse Width	P_{NRST}	-	-	-	0.3	μs



●IO Characteristics

(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index	Symbol	Condition	Min.	Typ.[*7]	Max.	Unit
Output voltage 1	VOH1	IOH=-1.0mA	VDD_IO -0.5	-	-	V
	VOL1	IOL=+0.5mA	-	-	0.4	V
Output voltage 2 (LED mode selected)	VOL2	2.7V≦VDD_IO≦5.5V IOL=+5.0mA	-	-	0.6	V
		IOL=+2.0mA	-	-	0.4	V
Output voltage 3 (I^2C mode selected)	VOL3	IOL3= +3mA (I^2C Spec.) (VDD_IO ≧2V)	-	-	0.4	V
Output voltage 4 (I^2C mode selected)	VOL4	IOL4= +2mA (I^2C Spec.) (VDD_IO ＜2V)	-	-	VDD_IO ×0.2	V
Output leakage 1	IOOH1	VOH=VDD_IO (at high impedance)	-	-	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	-	-	μA
Input current 1 (RESET_N)	IIH1	VIH1=VDD_IO	-	-	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=VDD_IO	-	-	1	μA
	IIL2	VIL2=VSS	-200	-15	-1	μA
Input current 3	IIH3	VIH3=VDD_IO (when pull down)	1	15	200	μA
	IIL3	VIL3=VSS (when pull down)	-200	-15	-1	μA
	IIH3Z	VIH3=VDD_IO (at high impedance)	-	-	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	-	-	μA
Input voltage1	VIH1	-	0.75× VDD_IO	-	VDD_IO	V
	VIL1	-	0	-	0.3× VDD_IO	V
Input pin capacitance	CIN	f=10kHz Vrms=50mV Ta=25℃	-	10	-	pF

[*7] Typical values are listed for Ta=25°C and VDD_IO=3.0V.

●Current Consumption

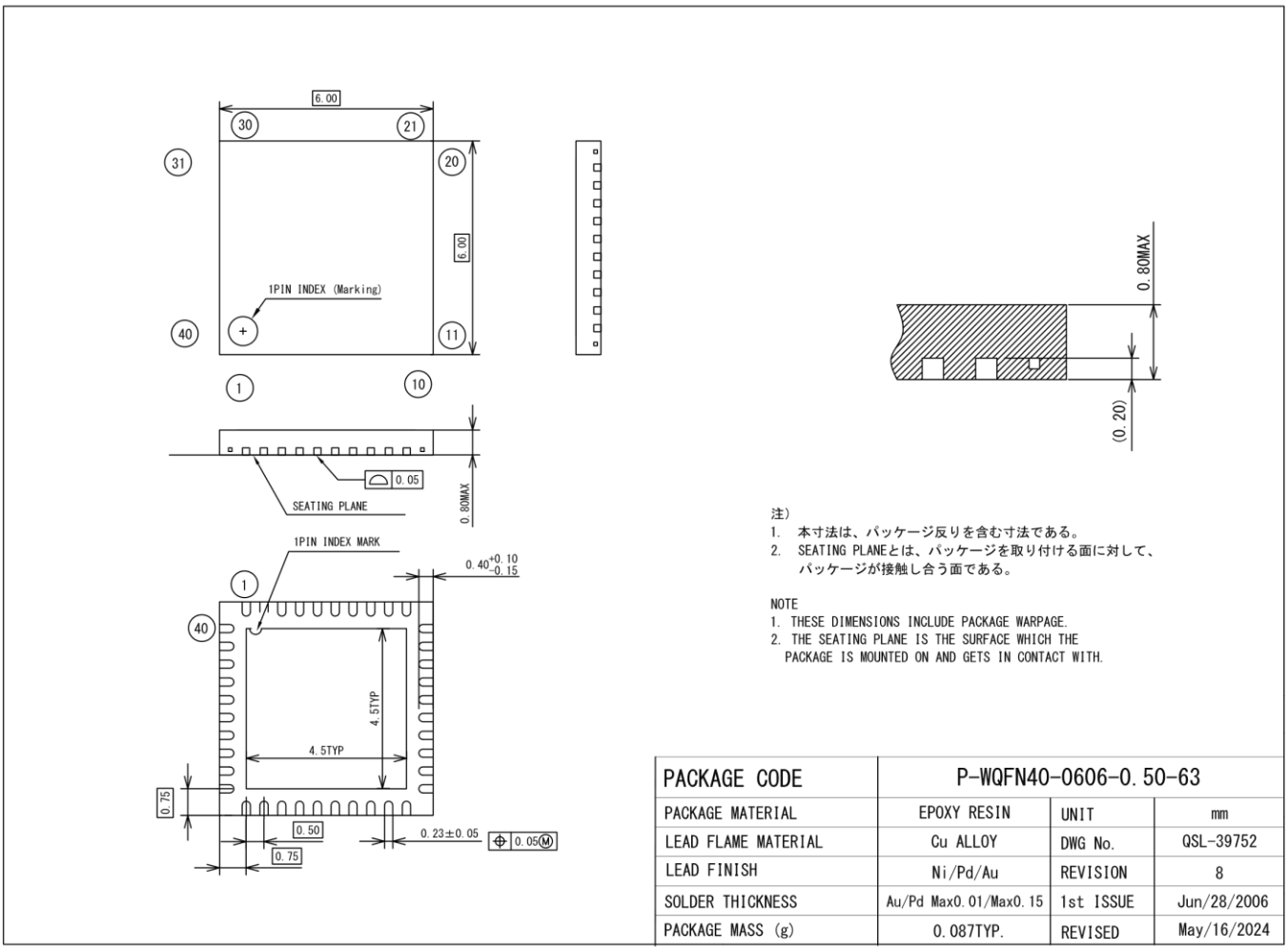
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85℃)

Index	Symbol	Condition	Min.	Typ.	Max.	Unit
Current Consumption	IDD1	HALT-H High speed clock stops	-	7	23.6	μA
	IDD2	HALT	-	1.3	2.0	mA
	IDD3	CPU 6.78MHz operation Peripherals stop	-	2.2	3.0	mA
	IDD4	CPU 6.78MHz operation During communication*8	-	15	-	mA
	IDD5	CPU 6.78MHz operation During power transmission*8	-	20	-	mA

*8 Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External transistor current is not included.

■Package Dimensions

WQFN40 pin



注）
1. 本寸法は、パッケージ反りを含む寸法である。
2. SEATING PLANEとは、パッケージを取り付ける面に対して、パッケージが接触し合う面である。

NOTE
1. THESE DIMENSIONS INCLUDE PACKAGE WARPAGE.
2. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

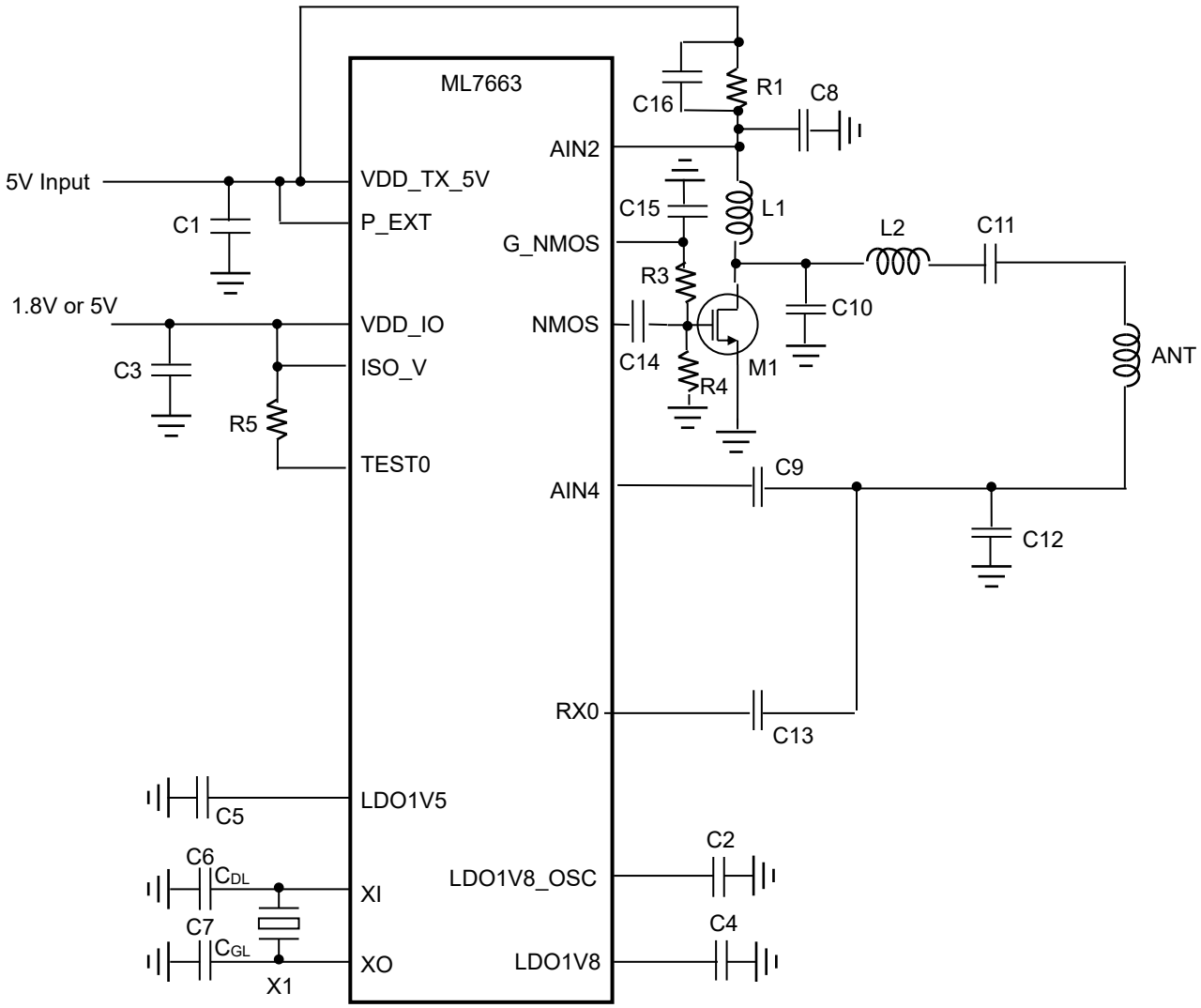
PACKAGE CODE	P-WQFN40-0606-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39752
LEAD FINISH	Ni/Pd/Au	REVISION	8
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Jun/28/2006
PACKAGE MASS (g)	0.087TYP.	REVISED	May/16/2024

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■Application Circuit Example

Please refer to the ML7662 / ML7663 Application Note for details.



■Revision History

Document No.	Issue Date	Page		Change contents
		Previous Edition	Current Edition	
FEDL7663-01	2023.6.9	-	-	First edition
FEDL7663-02	2023.12.12	-	1	Add product name and appications description
FEDL7663-03	2024.1.9	14	14	Modified Notes
FEDL7663-04	2025.12.30	14	14	Revise the contents of the notice
FEDL7663-05	2026.1.30	all	all	Revise the datasheet layout Added: AC Characteristics (UART) Added: AC Characteristics (Reset)
		17	17	Delete:Note for the package with exposed die pad
		4	4	Added note：exposed PAD

Notice

Precaution on using ROHM Products

1) When using ROHM Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings[*1], recommended operating conditions, etc.) are within the ranges specified. ROHM disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of ROHM Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of ROHM Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

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