Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ROHM GROUP
LAPIS
SEMICONDUCTOR

16LD-0725-02E

LAPIS Semiconductor Errata

ML620Q500H Series

Issue date: May. 19th 2016

ROHM
SEMICONDUCTOR

Notes

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1. Introduction

A part of functions on ML620Q500H Series (ML620Q503H/504H) has a bug. And User's manual has defective descriptions.This document describes the details and the workaround.

Target User's manual : FEUL620Q504H-01

1.1 Issue List

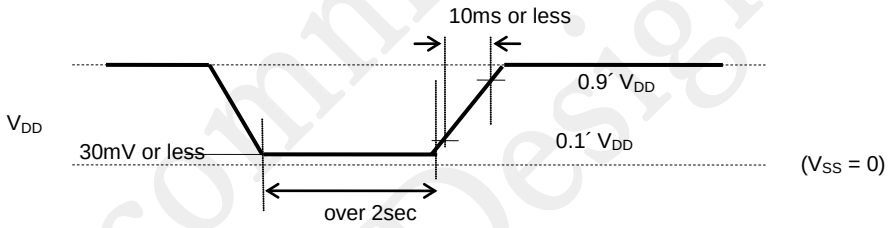
No.	Issue Date	Update	Subject
1	2015.10.16	-	Power-down/on Procedures
2	2015.10.16	-	Memory mapping of ML620Q503H
3	2016.05.19	-	Use of timer

2. Detail Description

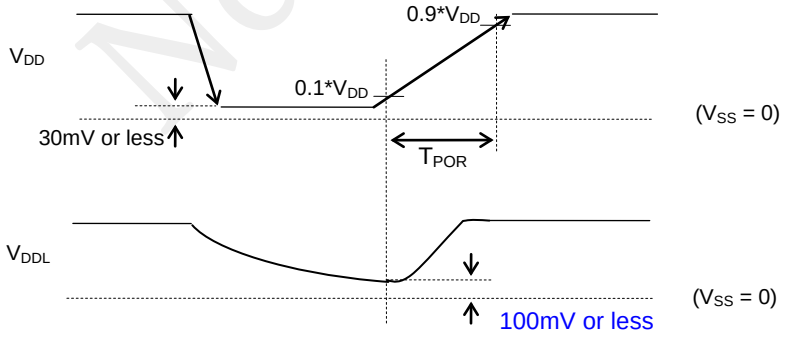
2.1 Power-down/on Procedures

A Power-on procedures and constraints are modified (in Appendix C. of the User's manual).

(Previous procedures and consraints)



(Modified procedures and consraints)

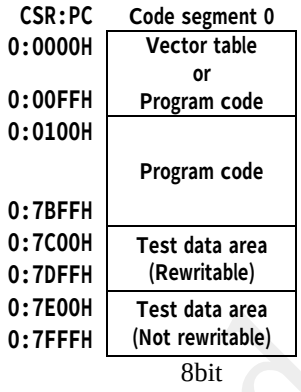


Note:
If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.

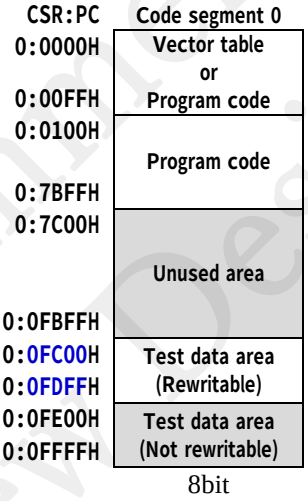
2.2 Memory mapping of ML620Q503H

Memory mapping of ML620Q503H is modified (in section 2. CPU and Memory Space of the User's manual).

(Previous mapping) :



(Modified mapping) :



2.3 Use of timer

When using a 16bit timer configured by two 8bit timers, there are following two restrictions.
The restrictions are resident in 8bit timer. It is not applicable to FTM.

2.3.1 Restriction 1

When using the 16bit timer configured by two 8bit timers, do not set “0FEh” to the lower byte of timer data register(TMnD). Set data except for “0FEh”(“00h to 0FDh” or “0FFh”). There is no restriction for the higher byte of timer data register(TMmD).
If the “0FEh” is set to the lower byte of timer data register, it works normally for the first interrupt cycle but shortens the cycle by 256 clocks for the second or later interrupt because the timer counter is not reset to “0000h” and restart counting up from “0100h”.

2.3.2 Restriction 2

When using the 16bit timer configured by two 8bit timers and also if you restart the timer after the timer is stopped by the software or automatically stopped in one shot timer mode, always reset the timer counter register(TMmC, TMnC) to “0000h” by making a write operaton to the register even the data is “0000h”. The write operation to one of the higher byte register(TMmC) or lower byte register(TMnC) resets both registers. If not reset the timer counter registers, the first interrupt cycle after restarting the timer may be incorrect.

2.3.3 Workaround

Example for programming code when using 16bit timer mode with Timer0 and Timer1 in order to avoid the aforementioned restriction 1 and restriction 2 :

```
if ( TM0D == 0xfe ) TM0D = 0xfd;    //  Check the data of timer register (for restriction 1)
TM0C = 0x00;                        //  Initialize the timer counter register (for restriction 2)
T0RUN = 1;                          // Start timer
```

The example shows that it checks the lower byte of timer data register(TM0D) and changes it to 0FDh if it is 0FEh, and starts the timer after initializing the timer counter register (TM1C, TM0C).

2.3.4 Improvement plan

No plan to fix the hardware.
[Note] will be added in the next revision of User’s Manual.

Revision History

Document No.	Issue date	Page		Description
		Before revised	After revised	
15LD-1070-01E	2015.10.16	–	–	First revision
16LD-0725-02E	2016.05.19	–	4	Add Issue No. 3