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April 1, 2024

FEXL7436NDG-06

ML7436N LSI

Hardware Design Manual

Issue Date: Apr. 13th 2021

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Introduction

This hardware design manual contains hardware information that should be referenced when designing ML7436N devices (Hereafter ML7436N). And also contains the measurement conditions and example of measurement results of RF characteristics.

Target product：

ML7436N

The following related manual is available and should be referenced as needed

- ML7436N data sheet

Notation

Classification	Notation	Description
● Numeric value	0x*nn*	Represents a hexadecimal number.
	0b*nnnn*	Represents a binary number.
● Address	0x*nnnn_nnnn*	Represents a hexadecimal number. (indicates 0xnnnnnnnn)
● Unit	word, W	1 word = 32 bits
	byte, B	1 byte = 8 bits
	Mega, M	10^6
	Kilo, K (uppercase)	2^{10}=1024
	Kilo, k (lowercase)	10^3=1000
	Milli, m	10^{-3}
	Micro, μ	10^{-6}
	Nano, n	10^{-9}
	Second, s (lowercase)	Second
● Terminology	"H" level	Signal level on the high voltage side; indicates the voltage level of V_{IH} and V_{OH} as defined in electrical characteristics.
	"L" level	Signal level on the low voltage side; indicates the voltage level of V_{IL} and V_{OL} as defined in electrical characteristics.

● Register description

Read/write attribute: R indicates read-enabled; W indicates write-enabled.

MSB: Most significant bit in an 8-bit register (memory)

LSB: Least significant bit in an 8-bit register (memory)

Table of Contents

1. Bypass capacitors

Notes the following when placing bypass capacitors.

- The VDD and GND traces should be wider than other signal line traces to reduce the resister element.
- Bypass capacitor should be placed as close to an LSI pin as possible. The recommended distance between ML7436N pin and the capacitor is less than 2mm. The smaller capacitor should be closer to an LSI pin than other capacitors.
- The RF_VBG (#28) pin is a reference voltage output pin of band-gap reference circuit. Placing a 0.1μF multilayer ceramic capacitor to the RF_VBG (#28) pin to reduce the noise from the band-gap reference circuit.

2. Crystal Oscillator circuit

Figure 2.1 shows a configuration example of the crystal oscillator circuit. Capacitors should be connected to RF_XIN (#1), RF_XOUT (#48), CXIN(#19) and CXOUT(#18) pins to stabilize crystal oscillator circuit. To determine the component values, the oscillator circuit evaluation on your designing board is required, since the stray capacitor of the board will be influenced. Amplitude level, oscillation margin, frequency deviation and oscillator circuit start-up time should be considered and evaluated.

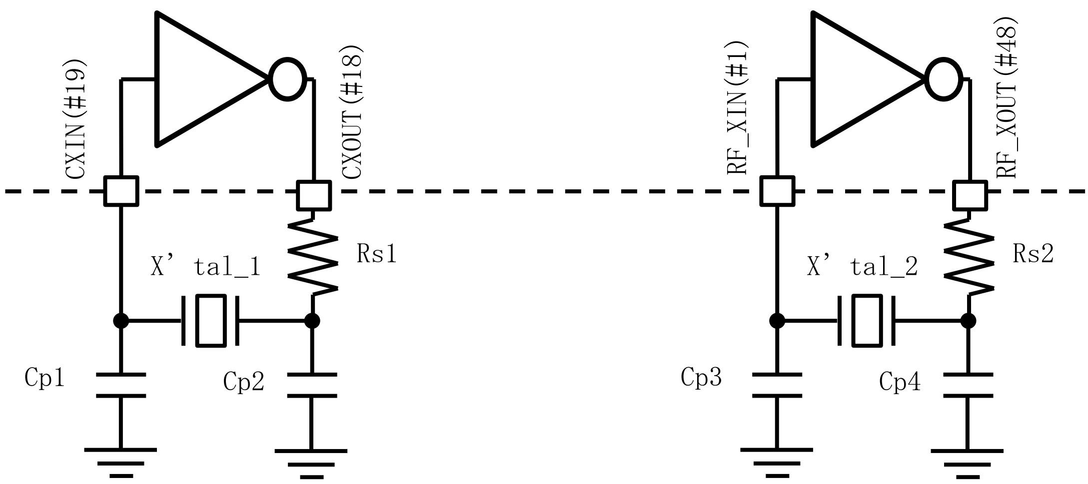


Figure 2.1 Crystal Oscillator circuit configurations

2.1. Circuit component values for crystal oscillator circuit

It is recommended to ask your oscillator manufacturer to evaluate the matching component values on the assembled board. The following Table 2.1 shows the matching component values with LAPIS Technology RF board configured by Figure 2.1 as reference.

Table 2.1 Representative matching component values

Manufacturer	Cristal oscillator X'tal_1 Type	Frequency (kHz)	Equivalent series resister max(Ω)	Load capacitor (pF)	Component values		
					Cp1 (pF)	Cp2 (pF)	Rs1 (Ω)
NDK	NX2012SE	32.768	50k.	9	18	18	0

Manufacturer	Cristal oscillator X'tal_2 Type	Frequency (MHz)	Equivalent series resister max(Ω)	Load capacitor (pF)	Component values		
					Cp3 (pF)	Cp4 (pF)	Rs2 (Ω)
Kyocera	CX2016DB	48	50	6	OPEN	OPEN	0

[Note] These component values appropriate for use on the LAPIS Semiconductor's RF board. It is not guaranteed to obtain same result on your specific board.

2.2. Notes on the crystal oscillator circuit configuration

Note the following when designing the crystal oscillator circuit.

- The capacitor's value of C1, C2, C3 and C4 depends on the crystal oscillator specification.
- C1, C2, C3 and C4 should be placed as close as possible to the RF_XIN (#1), the RF_XOUT (#48), the CNIN(#19), CXOUT(#18) pins to suppress parasitic LCR and stabilize the oscillator. The recommended distance between ML7436N pin and the capacitor is less than 2mm.
- Do not place the crystal oscillator circuit across other signal lines.
- Do not trace signal lines where large current flow around the crystal oscillator circuit.
- For the oscillator circuit capacitors, make sure the potential of the ground points is always equal to that of the GND. Do not connect the capacitors to GNDs where large current flow.
- Connect the crystal oscillator circuit to only ML7436N. Do not take oscillation signals from the oscillator circuit.
- Table 2.2 shows the tolerance of the frequency accuracy. Adopt the frequency accuracy as followed by Table 2.2 to confirm to the standards.

Table 2.2 Frequency accuracy to confirm to the standards.

Standard	Frequency accuracy
RCR STD-30 type III (Japan)	±10 ppm
RCR STD-30 type IV (Japan)	±4 ppm
ARIB STD-T108（Japan）	±20 ppm
Wireless M-Bus N mode	±1.5kHz(8.852ppm , 4.8kbps) ±2.0kHz(11.803ppm, 2.4kbps)
Wireless M-Bus F mode	±16 ppm

3. TCXO circuit

Please use a TCXO that satisfy the following specification.

- Output load: 10kΩ//10pF
- Output level: 0.8Vpp to 1.5Vpp
- Frequency accuracy: Refer to Table 2.2

The ML7436N integrates bias circuit and the DC bias is applied to the RF_XOUT (#48) pin. A 100pF capacitor should be placed on the TCXO line as followingFigure 3.1.
In ML7436N, RF_XIN(#1) pins is N.C. pin, then it should be open.
It is necessary to turn TCXO off to reduce electric comsumption, when Sleep mode set. Configure pull-up/pull-down on the board to enable TCXO automatically that ML7436N does not need to control the waking up.

Table 3.1 Recommended TCXO

Manufacturer	Type	Frequency (MHz)
KYOCERA	KT2016K	48
NDK	NT2016SB	48

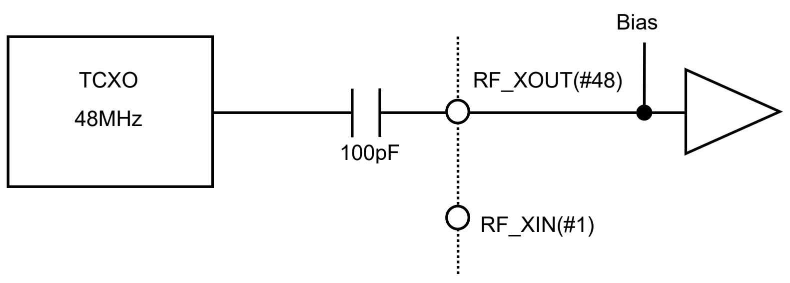


Figure 3.1 External oscillator circuit (TCXO) configurations

4. Debugger interface

ML7436N supports the serial debug ports as a debug interface. Figure 4.1 shows the connection between the debug connectors and ML7436N. Please refer to the debugger manual in detail.

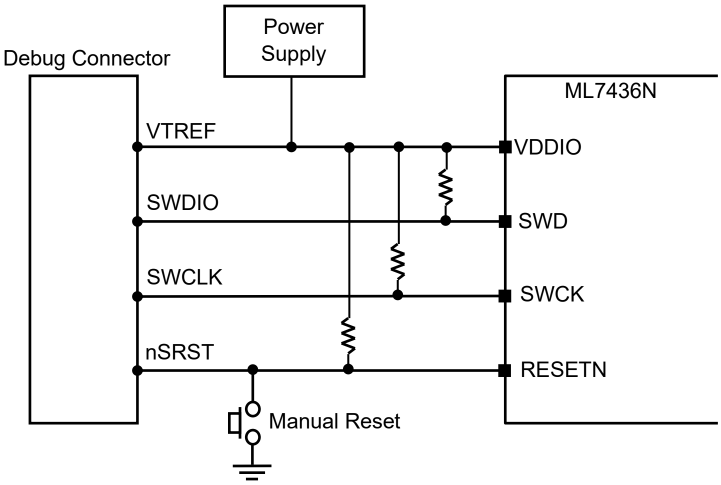


Figure 4.1 Debug connectors configurations

5. Internal ADC

ML7436N integrates a internal capacitor (20pF(Typ)) that holds electric charge by ADC0 input voltage. Connect more than 0.22uF capacitor when DC voltage level is measured with AD convertor, the internal capacitor can hold the voltage level that is independent of the input inpedance.

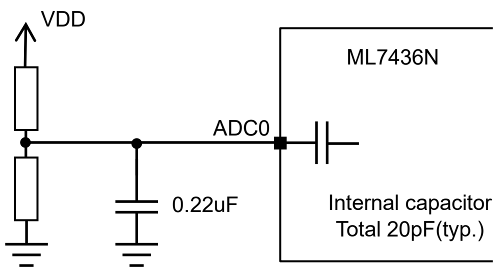


Figure 5.1 Internal ADC configurations

6. Hard Reset

Please adopt a reset IC to execute hard reset of ML7436N. The reset IC needs to control RESETN(#13) pin.

7. RF matching circuit

This chapter explains the development method of RF matching circuit. The ordinary antenna impedance is 50Ω. The input impedance at the antenna edge is needed to convert into 50Ω. The misalignment of impedance causes the deterioration of the reception sensitivity. The adjustment of antenna impedance having transmission circuit as reference can maximize the power efficiency of transmission circuit. Table 7.1 is the Measured RF impedance of each RF pins.

Table 7.1 Measured RF impedance of each RF pins

	R + jX [Ω]			
	TX [RF_PA_OUT1(#33) pin]			RX [RF_LNA_IN1(#35) pin]
Measured frequency	13dBm	10dBm	0dBm	-
433MHz	44.4-j29.4	41.0-j23.7	28.3 -j7.7	63.4-j225.7
868MHz	23.0-j14.9	22.0-j11.0	17.1+j2.0	24.6-j114.1
920MHz	21.2-j13.6	21.4-j10.1	17.1+j3.3	22.0-j106.6

	R + jX [Ω]	
	TX [RF_PA_OUT2(#38) pin]	RX [RF_LNA_IN2(#37) pin]
Measured frequency	0dBm	-
2.402GHz	19.5+j9.0	7.5-j14.2

[Note] These component values appropriate for use on the LAPIS Technology's RF board. It is not guaranteed to obtain same result on your specific board.

Figure 7.1 shows the RF matching circuit configurations. The reception circuit is T-type configuration and composed of two chip capacitors and a chip coil. SAW(Surface Acoustic wave) filter is adopted to remove the interfering wave. At the transmission circuit, DC voltage is biased at RF_REG_PA(#32) pin through the choke coil of RF_PA_OUT1(#33) pin. It composes LPF（Low Pass Filter）and the trap filter to suppress the higher harmonics. The transmission and reception lines connect antenna through the antenna switch IC to switch the transmission and reception.

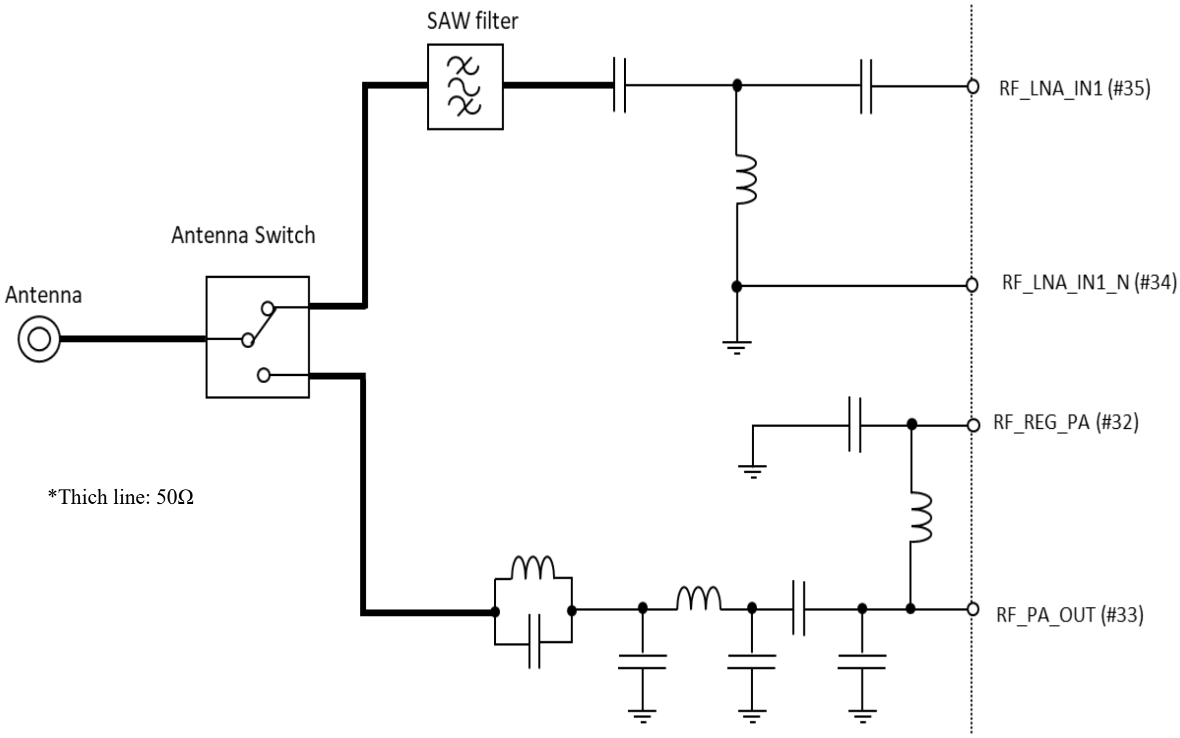


Figure 7.1 RF matching circuit configurations

7.1. SubGHz reception circuit matching development procedure

Figure 7.2 is the measured value of the input impedance at RF_LNA_IN1(#35) pin.

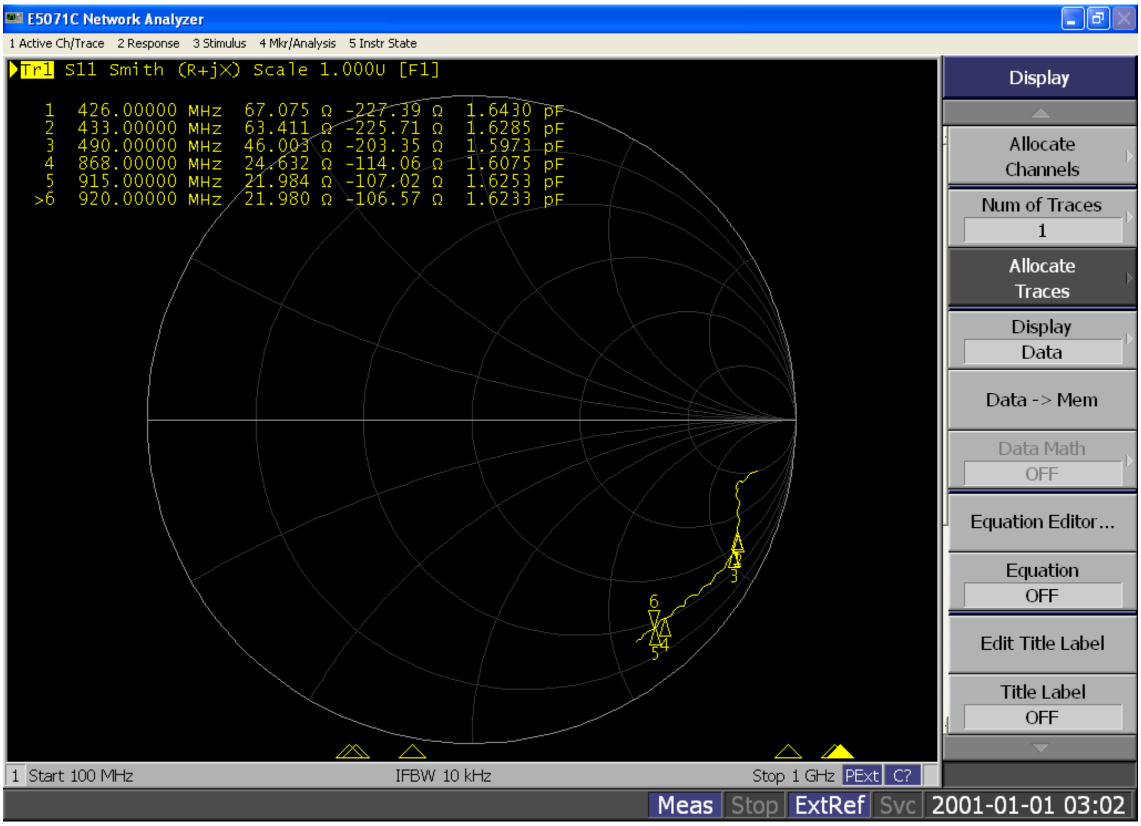


Figure 7.2 Measured input impedance

The input impedance at the RF_LNA_IN1(#35) can be expressed by the equivalent circuit that is the parallel connection of a resister and a capacitor.

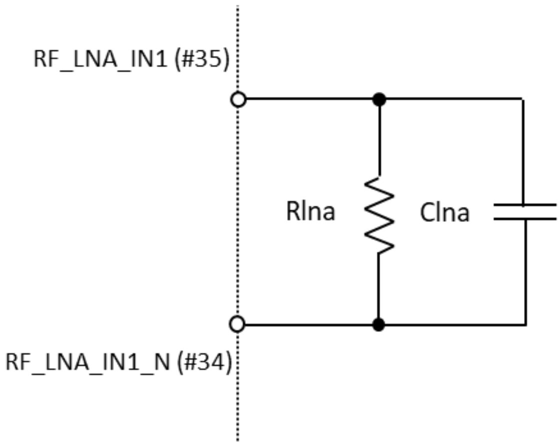


Figure 7.3 Equivalent circuit of RF_LNA_IN1(#35) pin

Table 7.2 shows the resister and capacitor values of the equivalent circuit on the typical frequency.

Table 7.2 Resister and capacitor values of the equivalent circuit

Frequency[MHz]	Rlna[Ω]	Clna[pF]
433	881	1.51
868	563	1.53
920	549	1.55

7.1.1. Connection of coupling capacitor

Figure 7.4 shows that the connection of enough AC coupling capacitor Cac(100pF) is connected to RF_LNA_IN1 pin. RF_LNA_IN1 pin is biased to the stable DC voltage by the internal circuit when the IC is the reception state. Cac causes that RF_LNA_IN1 pin is open state on DC. The DC voltage is not influenced by the matching calculation. Cac does not influence the matching value on the high frequency range, because of enough Cac capacitor.

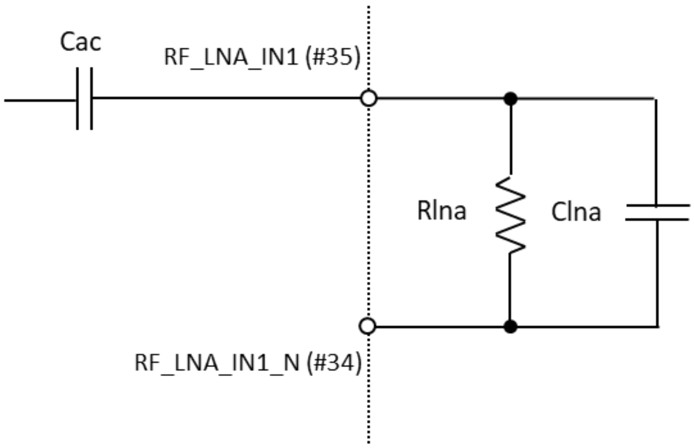


Figure 7.4 Addition of AC coupling capacitor Cac

7.1.2. Adjustment of LNA input impedance real part to 50Ω

Figure 7.5 shows the inductor Lmatch parallel connection. It adjusts the LNA input impedance real part to 50Ω.

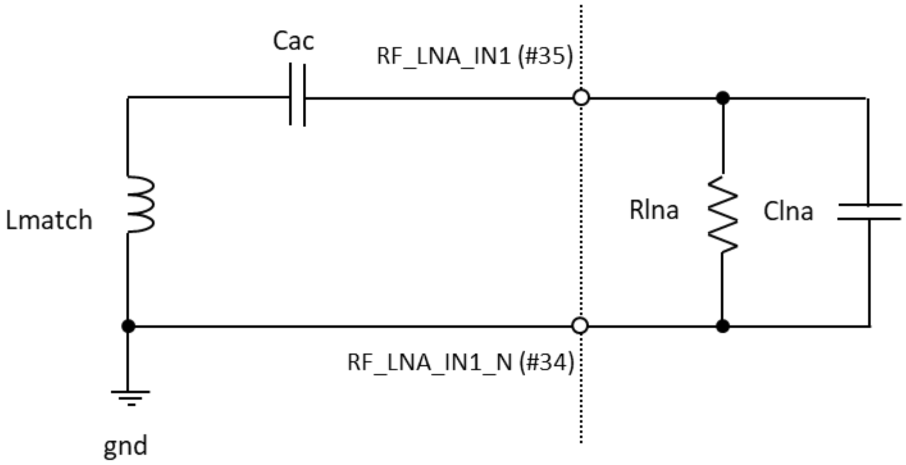


Figure 7.5 Addition of Lmatch

The required inductance is calculated by the formula (1).

$$\mathrm{L_{match}} = \frac{1}{\omega_{\mathrm{RF}}} \cdot \frac{1}{\omega_{\mathrm{RF}} \cdot C_{\mathrm{lna}} + \sqrt{\frac{1}{50 \cdot R_{\mathrm{lna}}} - \frac{1}{R_{\mathrm{lna}}^{2}}}} \cdots (1)$$

The impedance moves to 50+jX when the inductor Lmatch is connected on the Smith chart as following Figure 7.6.

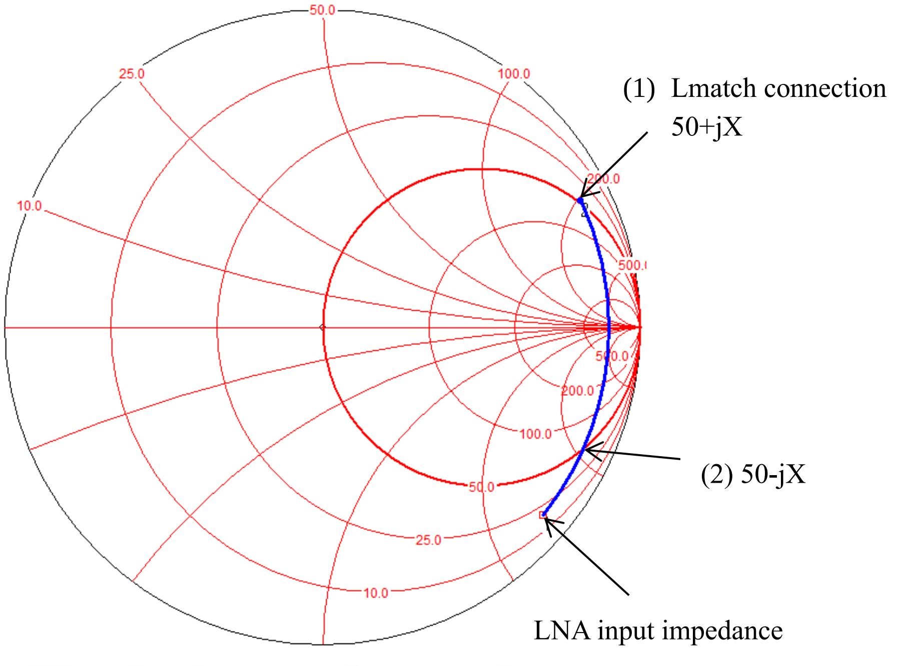


Figure 7.6 Impedance conversion with Lmatch addition

In fact, there are two Lmatch values whose real part is 50Ω. Each Lmatch values convert input impedances to (1)50+jX, (2)50-jX. In case of (2)50-jX, Lmatch is too large value, it is difficult to adjust Lmatch value. LAPIS technology recommends adopting (1)50+jX.

7.1.3. Adjustment of LNA input impedance imaginary part to 0Ω

Figure 7.7 shows the capacitor Cmatch series connection. It adjusts the LNA input impedance imaginary part to 0Ω.

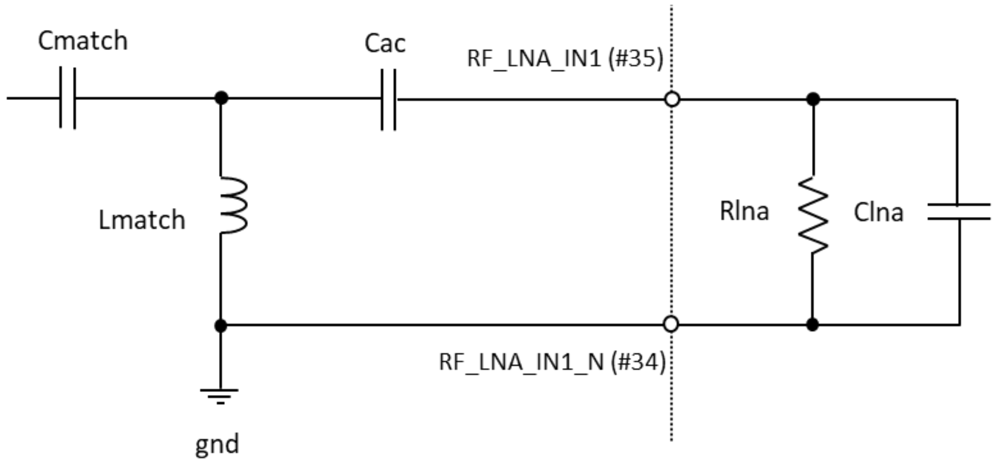


Figure 7.7 Addition of Cmatch

The required capacitance is calculated by the formula (2).

$$C_{match} = \frac{1}{50 \cdot \omega_{RF} \cdot \sqrt{\frac{R_{lna}}{50} - 1}} \cdots (2)$$

The impedance moves to 50+j0Ω when the capacitor Cmatch is connected on the Smith chart as following Figure 7.8.

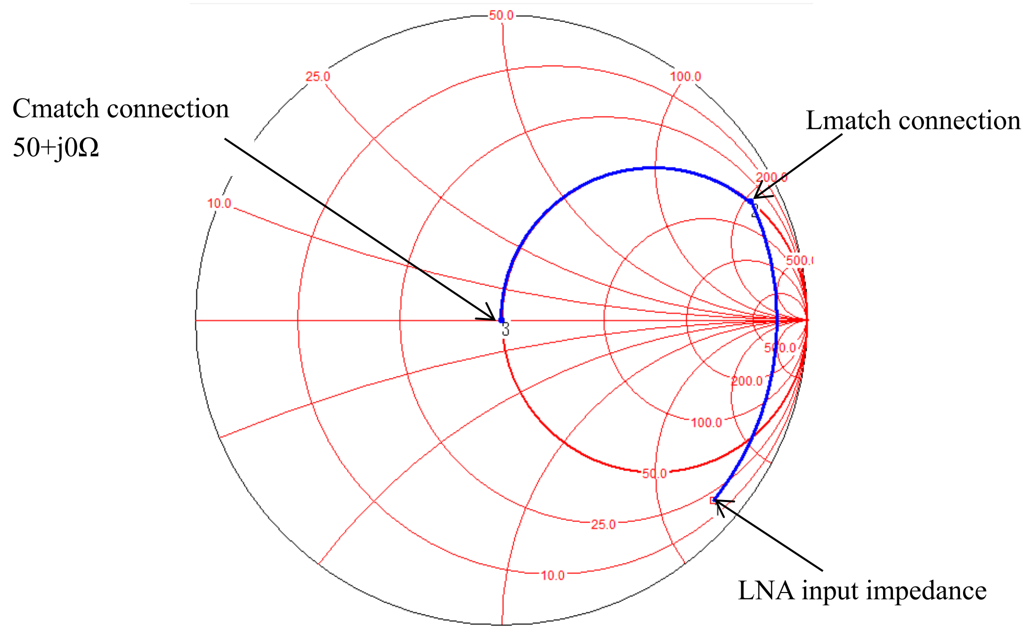


Figure 7.8 Impedance conversion with Cmatch addition

7.1.4. Connection to antenna

Figure 7.9 shows the connection between antenna and the matching circuit. The characteristic impedance is 50Ω.

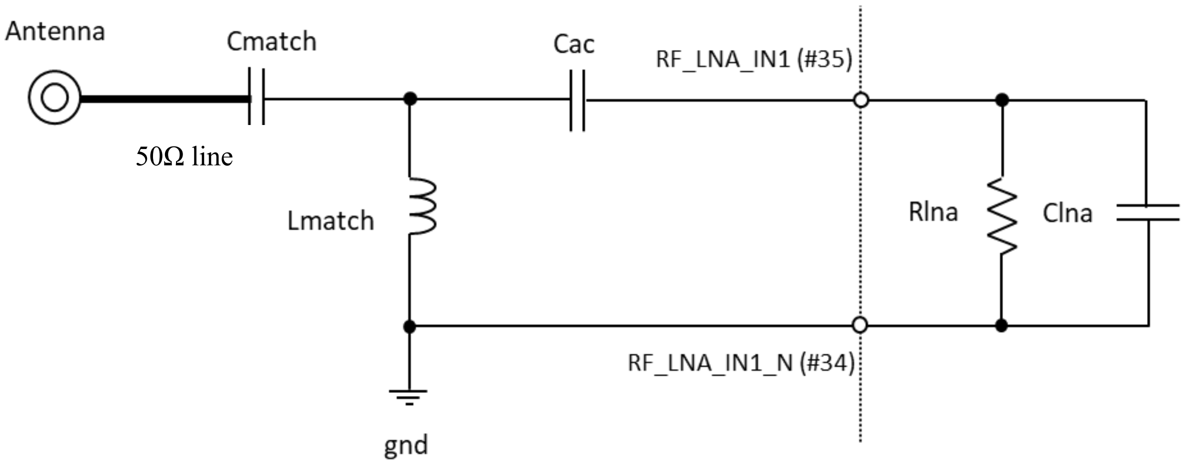


Figure 7.9 Addition of the characteristic impedance 50Ω line

7.1.5. Reception matching value

Table 7.3 shows the matching value that LAPIS technology adjusts it. In fact, it is necessary to make fine adjustment for each different board.

Table 7.3 Reception matching value of each frequency bands

Frequency[MHz]	Lmatch[nH]	Cmatch[pF]	Cac[pF]
433	36	1.5	100
860	12.5	1.1	100
920	10	0.8	100

7.2. SubGHz transmission circuit matching development procedure

This chapter explains an example of the transmission matching circuit development. The development procedure is as following.

1. Adjust Lch,Cp,Cs to Chapter10 application circuit.
2. Cut the higher harmonics with T or π-type Chebyshev LPF(Cz,Lz,Cz) (Figure 7.10).
   The cutoff frequency is approximately 1.5 times of the transmission frequency, the ripple of passband is approximately 0.5dB, the order is approximately 3.
3. Cut the second harmonic with the Notch filter Ln//Cn (Figure 7.11)

In case of the higher harmonics spurious of even number can not satisfy the standard, adjust the notch filter values (Ln,Cn), cut the second harmonics. f0 is the transmission frequency. The notch filter values (Ln,Cn) is calculated as the following formula.

$$2f_0 = \frac{1}{2\pi\sqrt{L_n C_n}}$$

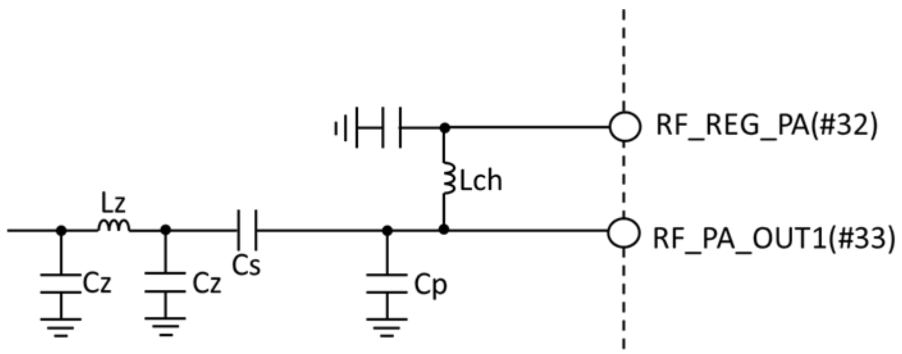


Figure 7.10 π-type LPF(Cz,Lz,Cz) configuration

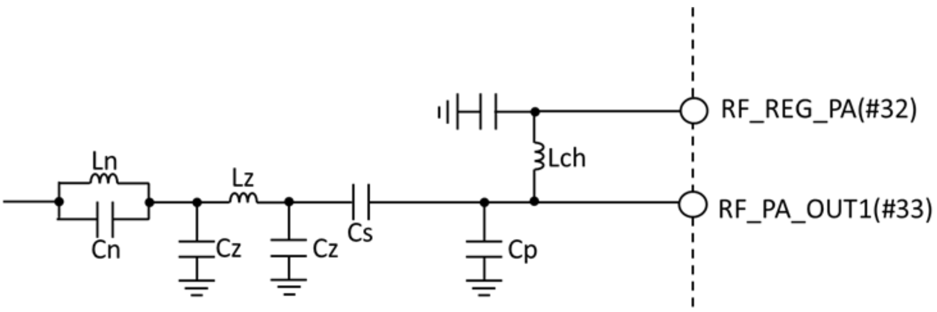


Figure 7.11 Second harmonics suppression with notch filter(Ln//Cn)

Table 7.4 shows the transmission matching value of each frequency bands.

Table 7.4 Transmission matching value of each frequency bands

Frequency[MHz]	Lch[nH]	Cp[pF]	Cs[pF]	Cz[pF]	Lz[nH]	Cn[pF]	Ln[nH]
433	15.5	-	100	8.2	15.5	4.7	6.8
868	3.9	3.9	100	4.3	6.8	2.7	2.7
920	3.9	3.9	100	4.3	6.8	2.7	2.7

7.3. 2.4GHz RF matching development procedure

Figure 7.12 shows the example of the 2.4GHz RF matching circuit configuration. The trap filter is configured to suppress the higher harmonics close to antenna.

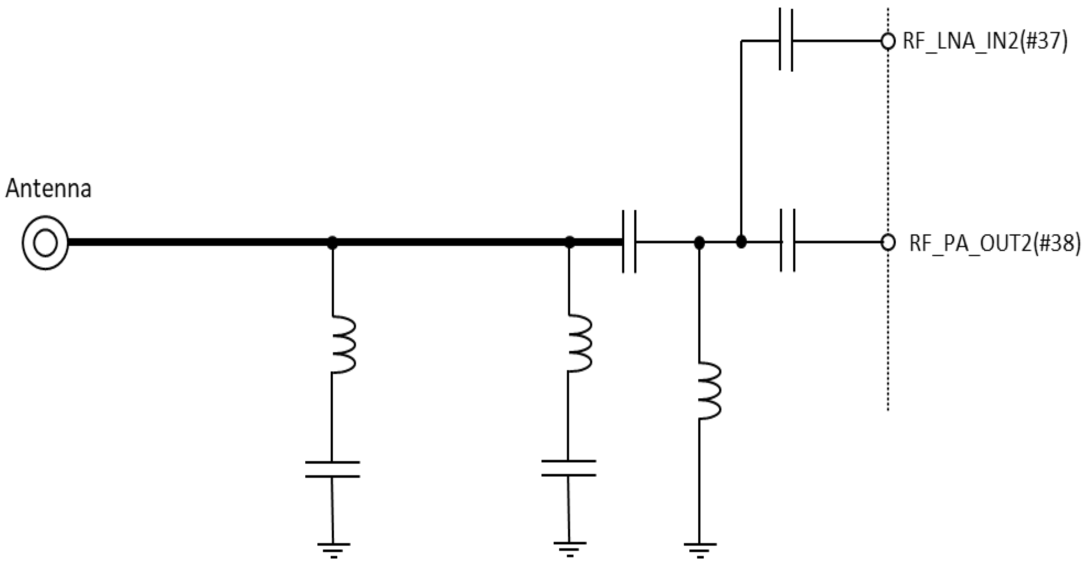


Figure 7.12 Example of 2.4GHz RF matching circuit configuration

This chapter explains 2.4GHz band transmission, reception circuit matching development procedure. 2.4GHz transmission PA corresponds to 0dBm(1mW) output. The PA is designed to output 0dBm at the 50Ω load impedance antenna.

7.3.1. Addition of higher harmonics trap filter

Figure 7.13 shows the addition of the trap filter to suppress higher harmonics of transmission signal. The trap filter impedance is small value at the resonance frequency of the inductor and the capacitor. It is possible to propagate the signal to GND at the resonance frequency. The transmission line (Thick line) between antenna and RF_PA_OUT2(#38) has 50Ω characteristic impedance.

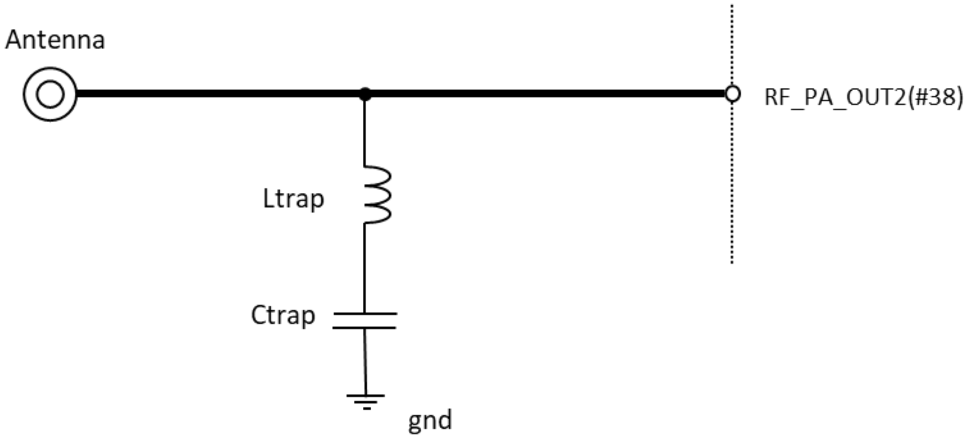


Figure 7.13 Higher harmonics trap filter configuration

The inductor and capacitor values configuring the trap filter is calculated as the following formula.

$$\omega_{\mathrm{RF}} \cdot N = \frac{1}{\sqrt{L_{\mathrm{trap}} \cdot C_{\mathrm{trap}}}}$$

ω_{RF} is the transmission frequency. N is the multiple number of higher harmonics. It is required to decide the maximum value of the higher harmonics and adjust the values meeting standards. If necessary, the trap filters are added to suppress every higher harmonic.

7.3.2. Addition of impedance conversion circuit (if necessary)

Addition of the trap filter may cause that the load impedance becomes lower and the transmission power becomes less than 0dBm. It is necessary to add the impedance conversion circuit and convert the antenna load impedance to higher value and adjust the transmission power to 0dBm. LAPIS technology recommends the high pass filter type impedance conversion circuit. It is possible to protect mixing the frequency elements of switching regulator and clock signal. If it is necessary to adopt high pass filter type conversion circuit, add enough AC coupling capacitor(100pF). DC voltage of RF_PA_OUT2 pin is decided by the internal circuit. It is not influenced by the matching circuit.

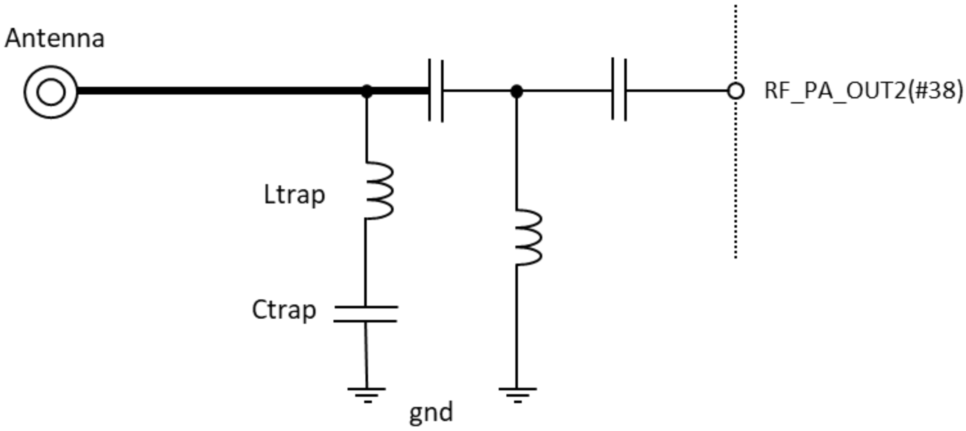


Figure 7.14 Addition of impedance conversion circuit

7.3.3. Connection to reception line

The reception line is connected through 1.5pF capacitance to antenna as following Figure 7.15. This configuration impedance is not 50Ω because the transmission character is prioritized over the reception character. LAPIS technology tests the circuit with this impedance on the mass production process and confirm the minimum reception sensitivity is -97dBm (BER<0.1%, Center frequency 2450MHz, GFSK100kbps, fdev=50kHz). If the addition of reception line causes the reduction of transmission power, increase the inductance of the matching circuit.

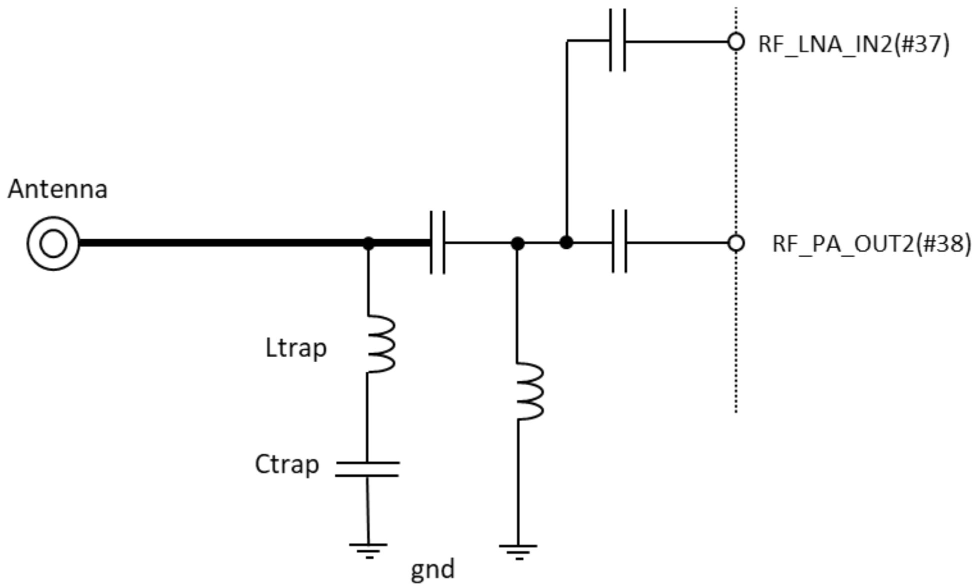


Figure 7.15 Connection to reception line

7.3.4. Matching circuit value

Figure 7.16 shows the circuit that LAPIS technology adjusts it. The circuit is configured with the trap filter suppressing the second, the third harmonics and the matching circuit converting antenna load impedance to 50Ω. Table 7.5 shows the matching circuit value.

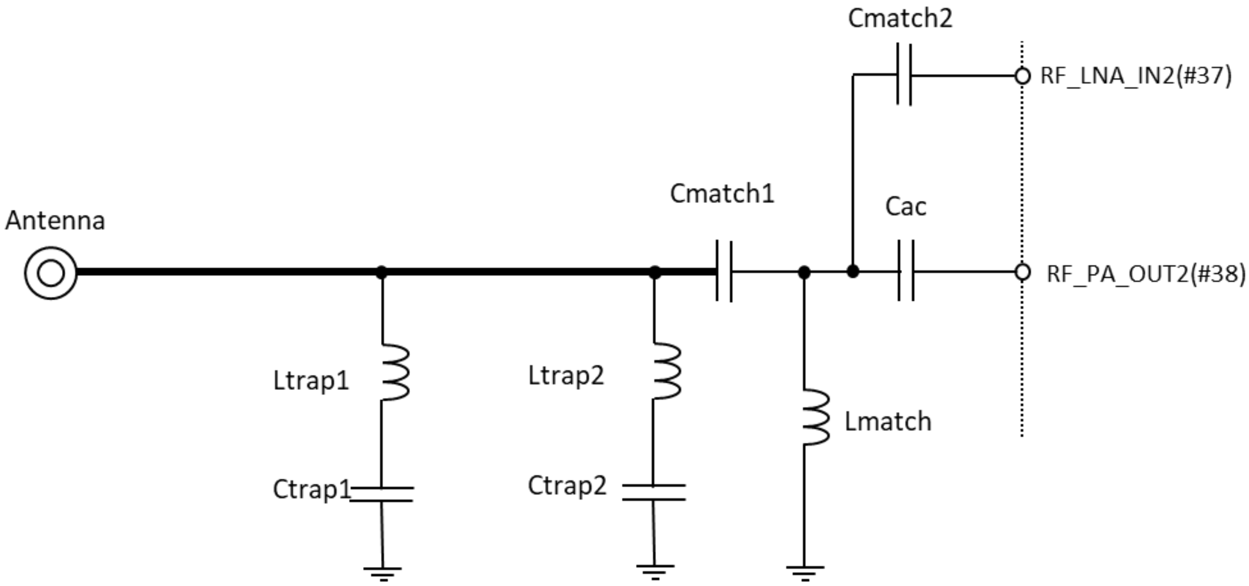


Figure 7.16 2.4GHz RF matching circuit

Table 7.5 2.4GHz RF matching circuit value

Parts	Value
Ltrap1	1.3nH
Ltrap2	1.3nH
Lmatch	3.3nH
Ctrap1	0.5pF
Ctrap2	0.2pF
Cmatch1	2.4pF
Cac	100pF
Cmatch2	1.5pF

8. Parts selection

8.1. Antenna

It is recommended to use an antenna with the specifications shown in Table 8.1. Select an antenna with the best directive characteristics for your specific operating, environmental and installation condition. Since antennas are affected by installation conditions such as GND, external factors should always be taken into account. It is recommended to ask the manufacturer of the selected antenna for installation details in relation to various factors, including the shape and stray capacitance of the board to be used.

Table 8.1 Recommended antenna character

Frequency band	430MH z /860MHz/ 920MHz/2.4GHz band
VSWR	2.0MAX
Nominal impedance	50Ω

8.2. Inductors

Use inductors with high Q. It is recommended to use LQW03AW series (manufactured by Murata Manufacturing Co. Ltd) or equivalent. Use inductors for the switching regulators that DC resistance is less than 0.4Ω, the rated current is more than 800mA Max.

8.3. Capacitors

Take the working voltage and temparature into account, because ordinary seramic capacitor has the temparature character and the voltage character. Use capacitors with a CH or a B of temperature characteristics. It is recommended to use capacitors of 0 ± 60 ppm/°C or less for areas that affect wireless characteristics. ML7436N equipes low power consumption mode (SLEEP mode). SLEEP mode can not ignore the leak current of the external capacitors. It is recommended to use the low leak current parts to design low power consumption.

8.4. Resisters

Use resistors for which the resistance variation are small when the temperature changes.

9. Notes on board artworks

9.1. GND

About IC's back side GND pad, the number of through-hole to board GND plane should be placed more than 12. And drawing GND line width should be more wide as much as possible to reduce GND impedance. Almost of L2 layer should be GND plane for double-layerd board.

Figure 9.1 shows the ML7436N package figure. The IC's back side GND PAD floats on the board. The distance is 0.25mm. Adjust the amount of solder to avoid poor soldering between IC and PCB GND.

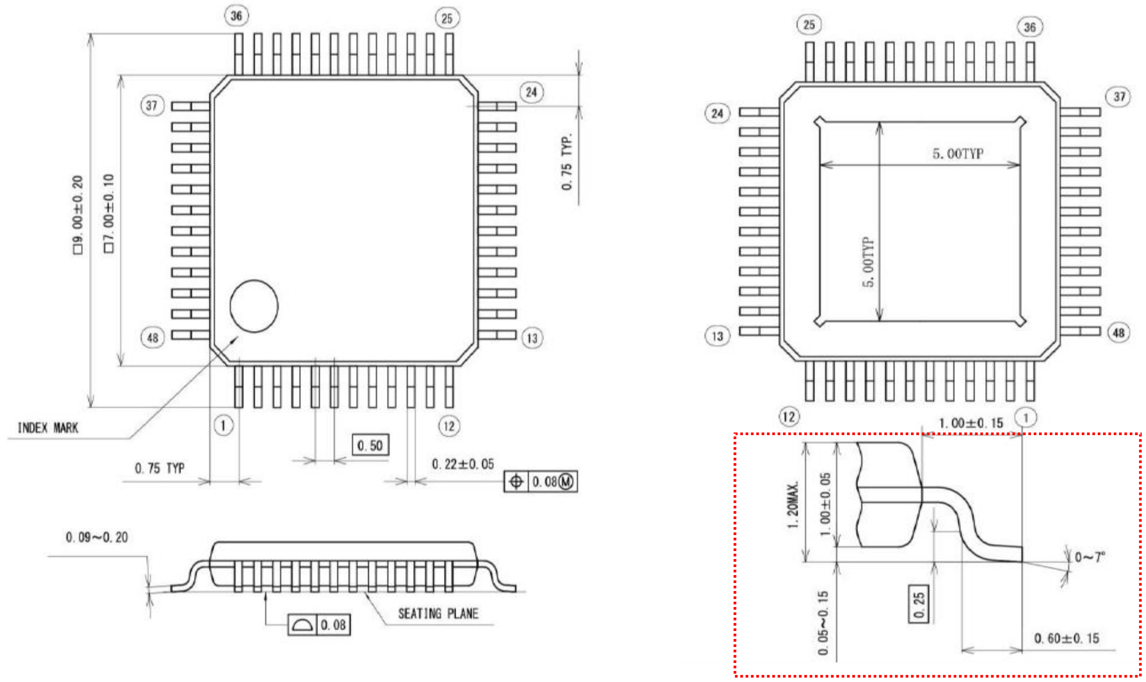


Figure 9.1 ML7436N package figure

RF_LNA_IN1_N(#34) is GND dedicated to RF input circuit 1st amplifier. Connect it to input matching circuit GND in the shortest and separate it from other GND not to mix noises.

9.2. Switching regulator

Switching regulator operation causes large pulse current alternately, whose lines are blue/orange. Take the following items into account.

- Draw current lines to minimize the large current loop.
- Mount inductor and capacitor close to IC and connect them with low impedance.
- Mount the inductor L1 of the switching regulator and the transmission choke inductor L4 at an angle of 90°. It influences the transmission spurious emission.
- Implement the branching of GND and lines close to capacitors.

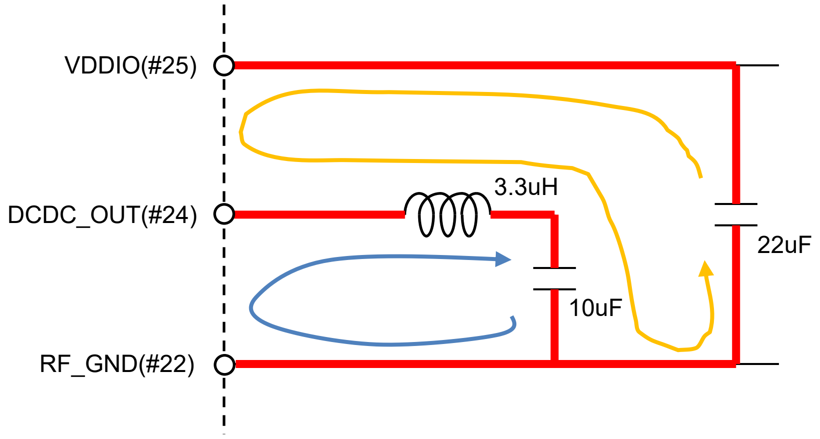
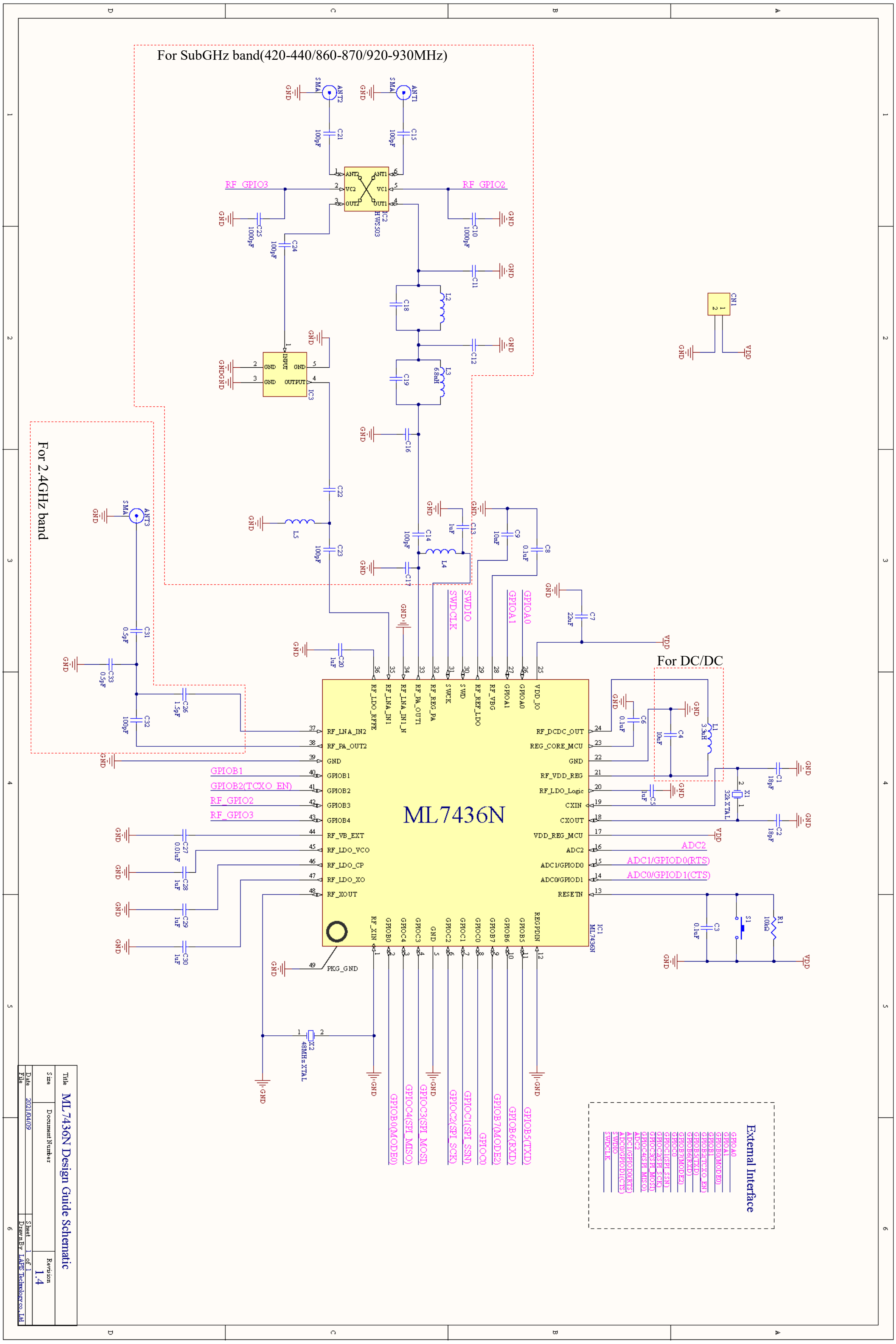


Figure 9.2 Current lines of switching regulator operation

10. Schematic example

This chapter explains circuit examples of each frequency bands. It is necessary to adjust values depending on customers' board pattern and parts. Please note the following for board design.

- Fix REGPDIN(#12) pin and TEST(#39) pin to GND at the normal operation.
- Fix RF_AMON(#5) pin to GND.
- When using TCXO, fix RF_XIN(#1) pin to OPEN. Refer section 3.TCXO circuit.
- When not using 2.4GHz band, fix RF_LNA_IN2(#37), RF_PA_OUT2(#38) to OPEN. Parts connecting above 2 pins are unnecessary.
- When not using SubGHz band, fix RF_REG_PA(#32), RF_PA_OUT1(#33),RF_LNA_IN1_N(#34), RF_LNA_IN1(#35) to open. Parts connecting to above 4 pins are unnecessary.
- When not using DCDC, change L1 to 0Ω.


For SubGHz band(420-440/860-870/920-930MHz)
For 2.4GHz band
For DC/DC
ML7436N
External Interface
ML7436N Design Guide Schematic

11. Bill of materials

This chapter shows the bill of materials corresponding to the chapter 10 schematic examples.
* Yellow cells' values are depending on frequency band.

Designator	420-440MHz		860-870MHz		920-930MHz		Manufacturer	Remarks
	Value	Type	Value	Type	Value	Type		
ANT1	-	SMAJ103HL-T16	←	←	←	←	JC ELECTRONICS	SMA Connector
ANT2	-	SMAJ103HL-T16	←	←	←	←	JC ELECTRONICS	SMA Connector
ANT3	-	SMAJ103HL-T16	←	←	←	←	JC ELECTRONICS	SMA Connector
C1	18pF	GJM0335C1H180G00	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C2	18pF	GJM0335C1H180G00	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C3	0.1uF	GRM033C71C104KE14	←	←	←	←	Murata Manufacturing	GRM033 series (0604mm)
C4	10uF	C1608JB1A106K	←	←	←	←	TDK	TDK MLCC (1608mm)
C5	1uF	GRM033R61A105ME15E	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C6	0.1uF	GRM033R6YA104KE14D	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C7	22uF	'GRM21BC81C226ME44L	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C8	0.1uF	GRM0335C1C104JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C9	10nF	GRM033R71C103KE14D	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C10	1000pF	GRM0335C1E102JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C11	8.2pF	GJM0335C1H8R2WB01	N.M.	-	←	←	Murata Manufacturing	GRM033 series (0603mm)
C12	8.2pF	GJM0335C1H8R2WB01	4.3pF	GJM0335C1H4R3B01	←	←	Murata Manufacturing	GRM033 series (0603mm)
C13	1uF	GRM033R61A105ME15E	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C14	100pF	GRM0335C1H101JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C15	100pF	GRM0335C1H101JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C16	N.M.	-	4.3pF	GJM0335C1H4R3B01	←	←	Murata Manufacturing	GRM033 series (0603mm)
C17	N.M.	-	3.9pF	GJM0335C1H3R9B01	←	←	Murata Manufacturing	GRM033 series (0603mm)
C18	N.M.	-	2.7pF	GJM0335C1H2R7B	←	←	Murata Manufacturing	GRM033 series (0603mm)
C19	4.7pF	GJM0335C1H4R7WB01	N.M.	-	←	←	Murata Manufacturing	GRM033 series (0603mm)
C20	1uF	GRM033R61A105ME15E	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C21	100pF	GRM0335C1H101JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C22	1.5pF	GJM0335C1H1R5WB01	1.1pF	GJM0335C1H1R1WA01	0.9pF	GJM0335C1HR90W	Murata Manufacturing	GRM033 series (0603mm)
C23	100pF	GRM0335C1H101JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C24	100pF	GRM0335C1H101JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C25	1000pF	GRM0335C1E102JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C26	1.5pF	GJM1555C1H1R5B	←	←	←	←	Murata Manufacturing	GRM033 series (0604mm)
C27	0.01uF	GRM033C81E103KE14	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C28	1uF	GRM033R61A105ME15E	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C29	1uF	GRM033R61A105ME15E	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C30	1uF	GRM033R61A105ME15E	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C31	0.5pF	GJM0335C1HR50W	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C32	100pF	GRM0335C1H101JA01	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
C33	0.5pF	GJM0335C1HR50W	←	←	←	←	Murata Manufacturing	GRM033 series (0603mm)
CN	-	XJ8C-0211	←	←	←	←	OMRON	Power terminal
IC1	-	ML7436N	←	←	←	←	LAPIS Technology	LSI TQFP48
IC2	-	HWS503	←	←	←	←	Hexa wave	DPDT
IC3	0Ω	MCR006YLPJ000	←	←	-	WFC30B0924FF	NDK	SAW_Filter
L1	3.3uH	VLS201610CX-3R3M-1	←	←	←	←	TDK	VLS-CX series (2016mm)
L2	15.5nH	LQW03AW15NJ00	2.7nH	LQW03AW2N7C00	←	←	Murata Manufacturing	LQW03AW series (0603mm)
L3	6.8nH	LQW03AW6N8J00	←	←	←	←	Murata Manufacturing	LQW03AW series (0603mm)
L4	15.5nH	LQW03AW15NJ00	3.9nH	LQW03AW3N9C00	←	←	Murata Manufacturing	LQW03AW series (0603mm)
L5	36nH	LQP03HQ36NH02	12.5nH	LQW03AW12NJ00	10nH	LQW03AW10N0J00	Murata Manufacturing	LQW03AW series (0603mm)
R1	10kΩ	MCR006YLPJ103	←	←	←	←	ROHM	MCR006 Series (0603mm)
S1	-	B3FS-1000	←	←	←	←	OMRON	SW
X1	-	NX2012SE	←	←	←	←	NDK	32.768kHz Xtal
X2	-	CX2016DB	←	←	←	←	KYOCERA	48MHz Xtal

Revision history

Document No.	Date	Page		Content
		Previous	New	
FEXL7436NDG-01	2021.1.19	–	–	The first edition
FEXL7436NDG-03	2021.1.28	27	27	Update Schematic example
		28	28	Update Bill of materials
FEXL7436NDG-04	2021.2.28	27	27	Update Schematic example
FEXL7436NDG-05	2021.3.17	9	9	Update Recommended TCXO
FEXL7436NDG-06	2021.4.13	27	27	Update Schematic example C27:0.1uF->0.01uF
		28	28	Update Bill of materials C27:0.1uF->0.01uF